Interconnect and Integration Technology

Yenai Ma, Biresh Kumar Joardar, Partha Pratim Pande, and Ajay Joshi

Abstract In the current heterogeneous manycore system regime, the electrical links are not able to provide the bandwidth required by today's diverse applications while staying within a reasonable power budget. As a result, we need to explore alternate link technologies. In this chapter we provide an overview of three different link technologies—photonic link technology, monolithic 3D link technology, and wireless link technology, which are considered as potential replacements for the electrical link technology. Photonic links use light waves to transmit information, monolithic 3D links use monolithic inter-tier vias for communication between adjacent layers of a 3D system, and wireless links use electromagnetic waves for communication. For each link technology, we first discuss why we should explore that link technology and then provide details about the fundamentals of that link technology.

1 Introduction

The development of IC technology is driven by the need to increase both performance and functionality while reducing power and cost at the same time. Thus far, this has been achieved using a combination of device and interconnect scaling,

Yenai and Biresh contributed equally to this book chapter.

Y. Ma · A. Joshi (✉)
Boston University, Boston, MA 02215, USA
e-mail: joshi@bu.edu

Y. Ma
e-mail: yenai@bu.edu

B. K. Joardar · P. P. Pande
Washington State University, Pullman, WA 99164, USA
e-mail: biresh.joardar@wsu.edu

P. P. Pande
e-mail: pande@wsu.edu

M. M. S. Aly and A. Chattopadhyay (eds.), *Emerging Computing: From Devices to Systems*, Computer Architecture and Design Methodologies,
https://doi.org/10.1007/978-981-16-7487-7_4

use of new materials, processing innovations, architecture enhancements, and better design techniques including more efficient place-and-route of critical circuit building blocks. However, conventional planar architectures are not sufficient to satisfy the computational requirements of modern data- and compute-intensive applications. The conventional planar IC has limited design choices, which limits system performance. For instance, large planar architectures require a network of long wires for communication. This can lead to significant amount of area and power overhead in a chip. Moreover, this adds to wiring complexities as long wires are often difficult to physically place-and-route in conventional planar designs.

The move to manycore systems has enabled us to develop a new Network-on-chip (NoC) paradigm for on-chip communication. However, as the number of cores increases, data transfer between two physically far apart blocks can have high latency and power consumption, which in turn affects the overall system performance and power consumption. A variety of solutions at the circuit level and at the architecture level have been proposed. However, they still rely on metal wires which do not scale well with physical distance. According to the International Technology Roadmap for Semiconductors (ITRS) (ITRS 2007), improving characteristics of metal wires will no longer satisfy performance requirements and new interconnect technologies need to be investigated.

A variety of new interconnect technologies and associated integration technologies have emerged in the past decade. Photonic links use light waves to carry and transmit information at the speed of light. These links provide high bandwidth density, low latency, and low data-dependent energy consumption. M3D-based architectures utilize monolithic inter-tier vias (MIVs) for the vertical connections instead of conventional through-silicon vias (TSVs). The physical dimensions of MIVs (50 nm in 14 nm technology node (Samal et al. 2016)) are several orders of magnitude smaller than TSVs which make them highly energy-efficient. Wireless links rely on electromagnetic waves for communication. They provide long-range short-cuts which lead to latency and energy benefits. In this chapter we provide an overview of these three new interconnect technologies—photonic, monolithic 3D and wireless, and their associated integration technologies. In particular we focus on 2.5D, 3D die-stacking and monolithic 3D integration technologies.

2 Photonic Links

2.1 Why Photonic Links?

As we have moved into the Big Data regime, the network bandwidth requirements of the systems running these Big Data applications is continuously increasing and has reached the order of Terabytes per second. It is getting increasingly difficult to meet such bandwidth requirements in an energy-efficient manner using current electrical link technology. To handle this explosive growing demand, photonic links have

been widely explored over the past decade. Compared to traditional electrical links, photonic links provide higher bandwidth density, lower communication latency, and lower data-dependent energy consumption (Batten et al. 2012).

2.2 *Photonic Link Basics*

A photonic link typically consists of a laser source, a modulator, a waveguide, a ring filter, and a photodetector, as shown in Fig. 1. A laser source emits optical waves that are guided into a waveguide using grating couplers. At the transmitter side, a microring modulator controlled by an electrical modulator driver modulates these optical waves. Essentially, the modulator driver and the microring modulator convert the data from the electrical domain to the optical domain. The modulated optical waves propagate along the waveguide. On the receiver side, the modulated optical waves are filtered out using the ring resonator (we have a separate ring resonator for each wavelength), and the signal is converted back into the electrical domain through a photodetector. A receiver samples the photodetector current to convert the data into the digital domain.

One key advantage of photonic links is that we can multiplex multiple wavelengths in a waveguide to increase the bandwidth density of the photonic links. Current solutions have demonstrated the multiplexing of up to 9 wavelengths into a single waveguide (Sun et al. 2015a). As a result a photonic link can have a bandwidth density that is several times larger than electrical links. This capability is particularly critical in case of I/O-constrained systems. Moreover, photonic links also have lower communication latency compared to electrical links. This enables us to provide high-bandwidth density low-latency communication using photonic links.

The bandwidth density and latency benefits, however, come at the cost of large power consumption. The three key components of power are—conversion power (including electrical-to-optical (E-O) conversion power on the transmitter side and

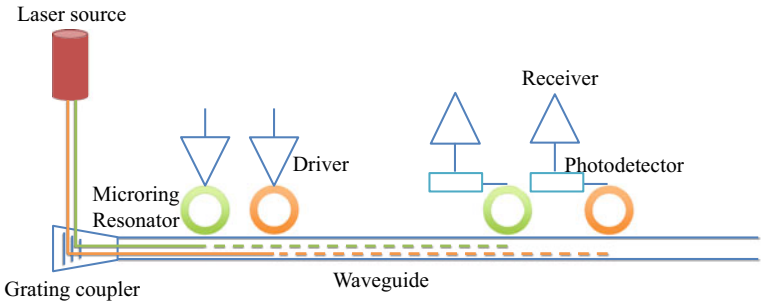

Fig. 1 Illustration of a wavelength-division multiplexed photonic link. Here the link supports two wavelengths

optical-to-electrical (O-E) conversion power on the receiver side), laser power, and thermal tuning power. All three components of power depend on the integration technology (we discuss three different technologies in the later half of this section on photonic links) used to integrate the photonic links. The total E-O and O-E conversion power is on the order of hundreds of fJ/bit (Sun et al. 2015b), and is independent of the length of the link. The rings in the photonic link are sensitive to temperature and so need to be actively tuned. The thermal tuning power is on the order of μW per ring per K. The exact thermal tuning power depends on the thermal gradients on the chip. The laser power depends on the overall layout of the photonic network and the losses in the individual optical devices, and can be on order of tens of watts.

Electrical links consume around 50 fJ/bit per mm when designed to operate at 5 GHz in 22 nm CMOS technology node (Joshi et al. 2009). To make photonic links competitive w.r.t. electrical links in terms of power consumption, several design-time mechanisms and run-time mechanisms to reduce the thermal power and laser power of photonic links have been developed (Pan et al. 2010; Chen and Joshi 2013; Chen et al. 2015; Demir and Hardavellas 2015; Abellán et al. 2017; Zhou and Kodi 2013; Li et al. 2014).

2.3 Integration Technologies for Photonic Links

In this section, we provide an overview of three different integration technologies for designing photonic links.

2.3.1 Photonic Links Using Monolithic Integration

Monolithic integration of photonics (see Fig. 2a) is a promising solution to meet both the energy efficiency and cost effectiveness. The optical devices can be fabricated along with the electrical components through a "zero-change" CMOS process (Stojanović et al. 2018). This state-of-the-art "zero-change" approach maximizes the performance of mixed-signal transceivers without increasing the complexity in processing and packaging.

With monolithic integration, the photonic interconnects are integrated with transistors using the same CMOS process. The photonic devices can be implemented in the high-index crystalline silicon layer. Waveguides are implemented in the crystalline silicon body layer to lower optical loss. Couplers, which are used to couple the light between the light source and the chip, are fabricated by patterning crystalline silicon and polysilicon layers. Microring modulators and photodetectors are implemented using existing source/drain and well implant doping levels and the available silicon-germanium in the process.

The manufacturing of monolithic integration is relatively inexpensive, since the optical devices are all designed to conform to the native electrical silicon-on-insulator (SoI) CMOS process and do not require modifications to the original foundry design

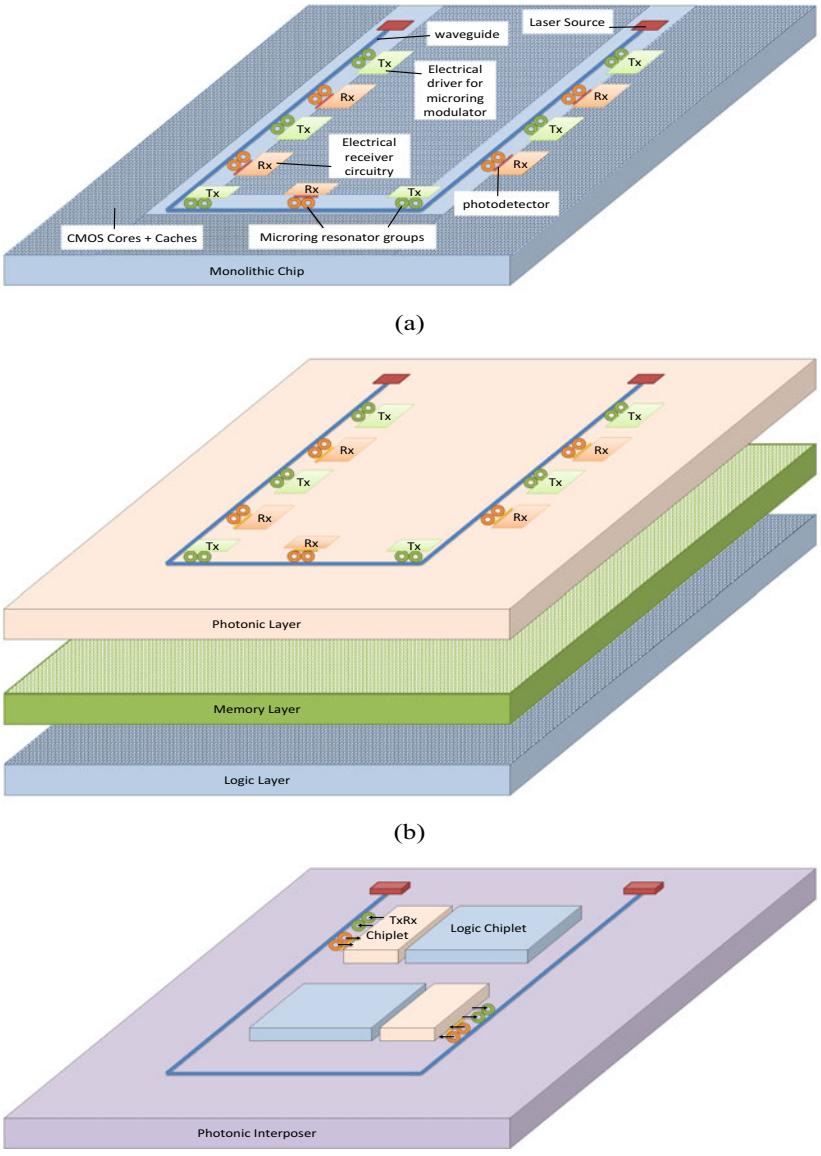

Fig. 2 Illustration of photonic links in **a** monolithic integration, **b** 3D integration, and **c** 2.5D integration

flow (Orcutt et al. 2012). Monolithic integration maximizes transceiver performance and decreases the area and energy required to interface electrical and photonic devices (Beamer et al. 2010). However, it requires larger active area for waveguides and other optical devices.

2.3.2 Photonic Links Using 3D Integration

3D integration technology is an alternate approach that has been adopted for systems with photonic links (see Fig. 2b). With 3D integration technology, the photonic components can be fabricated separately to allow more design options and avoid process complexity. Both IBM (2010) and Biberman et al. (2012) released conceptual photonic systems leveraging 3D integration. The systems stack a processor layer, a memory layer (or layers), and a photonic network layer vertically, and connect these layers using dense and fine-pitch inter-layer vias (Heights 2010) or TSV technology (Biberman and Bergman 2012). The processor layer and the memory layer(s) contain only electrical components, while the photonic layer consists of all optical devices as well as electrical circuitry including amplifiers and drivers (Heights 2010).

Another example of 3D-integrated photonic system is proposed by Chen et al. (2014). In this example, the photonic layer is stacked on top of the electrical logic layer and connected using metal vias. An extra laser source layer which contains lasers is placed on top of the photonic layer. The optical devices other than the laser sources are arranged in the photonic layer.

3D integration provides more options for materials and manufacturing processes to achieve higher performance in photonic devices (Beamer et al. 2010), instead of strictly conforming to the standard CMOS process. For example, the optical devices can be fabricated in monocrystalline SoI with thick layer of buried oxide (BOX) (Gunn 2006), or in silicon nitride (SiN) deposit layer on top of the metals (Barwicz et al. 2007) to provide better performance.

2.3.3 Photonic Links Using 2.5D Integration

2.5D integration technology has also been used to enable systems with photonic links (see Fig. 2c). CEA Leti has proposed a 2.5D manycore system with photonic network, called Processors On Photonic Silicon interposer Terascale ARchitecture (POPSTAR) (Thonnart et al. 2020; Narayan et al. 2020). The system consists of six compute chiplets and eight transceiver and receiver (TxRx) chiplets, which are placed on the top of a photonic interposer. The laser wavelengths are generated by an off-chip laser source, pass through a vertical fiber attachment and grating couplers, and finally enter the waveguides in the photonic interposer. The photonic interposer is fabricated using an optical front-end-of-line (FEOL) technology. The waveguides, microring resonators, and photodetectors are placed in the interposer. The compute chiplets contain the electrical components such as cores and caches. The TxRx chiplets are responsible for the E-O and O-E conversions. The TxRx chiplets contain

the electronic circuitry, including modulation drivers, comparators, transimpedance amplifiers, serializers and deserializers, for the E-O and O-E conversions and they are connected to the microring resonator groups on the interposer. Both the compute chiplets and the TxRx chiplets are fabricated using an STMicro C28FDSOI technology (Narayan et al. 2019).

Similar to 3D integration, 2.5D integration technology also allows for separate fabrication processes for electrical chiplets and photonic chiplets. Therefore, the performance of photonic components could be higher, thanks to customized optical devices, compared to monolithic integration. Both monolithic integration and 3D integration require additional engineering efforts to incorporate photonic devices. Monolithic integration requires redesigning the chip to make room for photonic links, while 3D integration requires modifying the original electrical chip to arrange vertical interconnects such as TSVs and inter-layer vias. However, 2.5D integration technology can use off-the-shelf electrical chiplets and avoid such non-recurring engineering cost.

2.4 Challenges and Future Research/Design Perspectives

Photonic links provide better bandwidth density and latency than electrical links for both intra-chip and inter-chip communication. With microring resonator technology where the microring radius is typically a few μms and waveguide technology that has a sub-10 μm pitch (Barwicz et al. 2004; Xu et al. 2008; Sun et al. 2015b), the area is usually not a concern. For inter-chip communication, the energy consumed for transmitting each bit using photonic links is comparable to that of electrical links. As a result, inter-chip photonic communication is viable and commercial solutions are being developed by several companies including Ayar Labs, Mellanox and Intel. The intra-chip electrical links consume less energy per bit than photonic links. To take advantage of the bandwidth density and latency advantages of the photonic links for intra-chip communication, we need to develop novel mechanisms for reducing the energy per bit number for photonic links. Currently, researchers are exploring a variety of device-level mechanisms, circuit-level mechanisms, physical design-level mechanisms, and architecture-level mechanisms for reducing the energy per bit (Pasricha and Nikdast 2020). Device-level mechanisms are focused on reducing the losses in the photonic devices (which reduces the optical power) and designing thermally-insensitive photonic devices (which reduces the thermal tuning power). The circuit-level mechanisms are targeting the reduction of the transmitter and receiver power. The physical design-level mechanisms are focused on developing power aware placement and routing of photonic devices, while the architecture-level mechanisms are focused on developing runtime laser power and thermal power management solutions. Photonic links are expected to be viable for intra-chip communication in another 5–10 years. The cost of silicon photonic links depend on the choice of integration technology. Monolithic integration increase the chip size to house the photonic devices and drivers, thus, increasing the cost of chip. 3D integra-

tion requires a separate photonic layer, which increases the cost of the system. 2.5D integration leverages the interposer to embedded the photonic devices, so the extra cost is the additional steps to embedding photonic devices in the interposer.

3 Monolithic 3D

3.1 Why Monolithic 3D Links?

3D integrated circuits (3D ICs), which contain multiple layers of active devices, have the potential to dramatically enhance chip performance, functionality, and device packing density (Davis et al. 2005; Venkatesan et al. 2001). In addition, 3D ICs have higher noise immunity, improved power consumption due to lower wire length and capacitance, and superior performance (Banerjee et al. 2001). Due to smaller physical dimensions, wiring and clock tree distribution complexity is reduced. 3D integration also enables us to combine dissimilar technologies (memory, logic with extension to RF, analog, optical, and microelectromechanical systems) to create heterogeneous (Nakahara et al. 1999) and Processing-in-memory architectures (PIM Eckert et al. 2014). Traditionally, a 3D IC is realized by stacking multiple planar layers on top of each other and connecting them using TSVs (Borkar 2011). However, TSVs present some fundamental limitations in high-performance, low-power 3D IC design: (a) fine-grained partitioning of logic blocks across multiple tiers is not possible (Samal et al. 2016) due to which core and uncore elements are planar which constraints achievable performance; (b) The larger dimensions and presence of bonding material makes heat dissipation challenging in TSV-based 3D ICs, especially for tiers further away from the heat sink (Joardar et al. 2019). Processing-in-memory (PIM) architectures, where logic is placed near the memory are one of the worst affected due to bad thermal properties of TSV-based architectures; and (c) TSVs add non-negligible area and power overheads. In addition, TSV-based architectures have alignment problems between adjacent tiers, which compromises performance further (Kuroda 2014).

Overall, TSV-based 3D designs cannot achieve the full-potential of vertical integration. Hence, emerging 3D integration methodologies e.g. Monolithic 3D (M3D), which addresses these challenges are being developed. M3D enables vertical connectivity using Monolithic Inter-tier Vias (MIVs) which are smaller and more energy-efficient than conventional TSVs. This property has been used to design high-performance yet energy-efficient architectures. For instance, a monolithic 3D test chip with logic circuits, sensors and different types of memory is presented by Wu et al. (2015). A monolithically stacked 3D Field-programmable gate array (FPGA) outperforms the 2D baseline in logic density, delay, and dynamic power consumption (Lin et al. 2007). M3D has also been used to design high-performance memory architectures (Yu and Jha 2018). A fully M3D-based CPU core with logic and memory partitioned in two tiers has been demonstrated (Gopireddy and Torrellas 2019).

The N3XT architecture improves the energy efficiency of abundant-data applications 1,000-fold by using new logic and memory technologies, 3D integration with fine-grained connectivity, and new architectures for computation immersed in memory (Sabry Aly et al. 2015). M3D integration has also been used to design high-speed cache (Gong et al. 2019) that outperforms state-of-the-art planar implementations. High-performance NoC design using multi-tier routers is explored in several prior works (Musavvir et al. 2020; Das et al. 2017). The M3D-NoC benefits from multi-tier routers and energy-efficient MIVs which reduces logical distance between cores and leads to significant performance improvements compared to conventional designs.

3.2 M3D-Based Design

Monolithic 3D ICs (M3D) is enabled by sequential integration of device layers in the vertical direction (Batude et al. 2014). A typical two-tier M3D-based architecture is shown in Fig. 3 in a flip-chip configuration. The first set of transistors closer to the "handle bulk" (Fig. 3) are processed with standard SOI process and make up Tier 1. A thin interlayer dielectric (ILD) is deposited over the metal layers for the bonding of the next device layer. This device layer along with the metal layers make up the other tier (Tier 0) of the 3D architecture.

In M3D-based designs, monolithic inter-tier vias (MIVs) are used as vertical links instead of TSVs. The physical dimensions of MIVs (50 nm × 100 nm) are several orders of magnitude smaller than TSVs (1–3 μm × 10–30 μm) and are comparable to standard copper vias (Samal et al. 2016). Similarly, the contact dimensions of M3D are much smaller (∼100 nm (Jung et al. 2007)) while TSV-based systems require contacts of 2–5 μm. This allows us to achieve nanoscale contact pitch using M3D and attain the true benefit of vertical system integration. As a result, monolithic 3D inte-

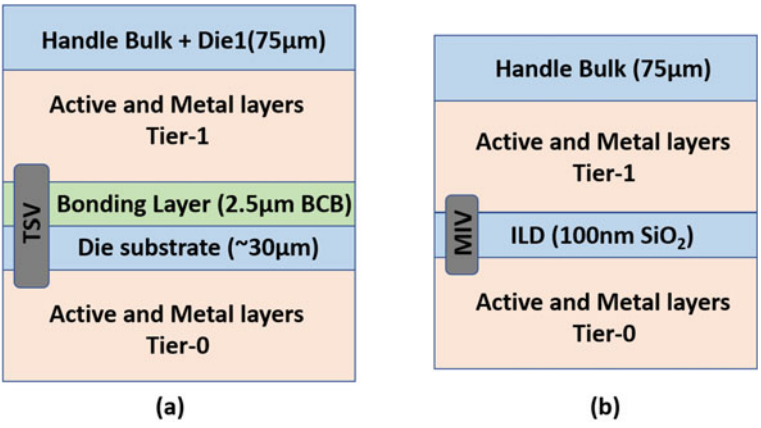

Fig. 3 Physical structure of a 2-layer IC using **a** TSV and **b** M3D integration (Samal et al. 2014)

gration results in performance gain through interconnect dimension reduction (Vinet et al. 2014). In addition, by facilitating nanoscale pitch, M3D enables us to examine gate- and block-level partitioning in circuits (Batude et al. 2012). Depending on the granularity with which different devices are partitioned across the various tiers, monolithic 3D ICs can be categorized into (a) transistor-level monolithic (Bobba et al. 2011), in which n-FETs and p-FETs are placed on two separate tiers and connected through intra-gate MIVs; (b) gate-level monolithic (Bobba et al. 2011), in which gates are implemented on different tiers and connected through inter-gate MIVs; and (c) block-level monolithic (Panth et al. 2013), in which each intellectual property (IP) block is implemented on just one tier. In transistor-level monolithic integration, different materials are used for n-FETs and p-FETs (Ge/Si, InGaAs/Si, InGaAs/SiGe, carbon nanotube/Si (Deshpande et al. 2017)) and optimized separately, which overcomes the thermal budget limitations on the top tier (Andrieu et al. 2018). Gate-level monolithic integration can reuse 2D design platforms and reduce global wire length. Block-level monolithic integration enables close logic-memory interconnects that improves memory bandwidth and latency (Shen et al. 2013). Naturally, NoC architectures can exploit the benefits of gate-/block-level partitioning in M3D integration by fabricating routers that span multiple tiers. In a recent study, M3D-enabled NoCs are shown to achieve 28% better energy efficiency compared to its TSV-based counterpart (Das et al. 2017). In addition, the direct wafer bonding technique in M3D achieves higher yields and lower costs compared to TSV-based integration (Batude et al. 2012; Uhrmann et al. 2014).

Interestingly, monolithic 3D ICs also exhibit better thermal behavior (measured as the maximum on-chip temperature) due to their layer structure compared to TSV-based 3D ICs despite their higher power density (Samal et al. 2014; Joardar et al. 2019). The differences in fabrication process of monolithic 3D and TSV-based 3D result in significant differences in their thermal behavior. Figure 3 highlights differences in the materials used in the two technologies and their conductivity and thickness, which influences the thermal behavior. Table 1 lists their details for a typ-

Table 1 The different materials, thermal conductivity and vertical thickness of layers in M3D and TSV

Layer/structure	Material	Thermal conductivity (W/m-K)	Vertical thickness
Monolithic 3D			
Handle bulk	Silicon	141	75 μm
ILD (Inter-tier)	SiO_2	1.38	100 nm
TSV-based			
Handle Bulk	Silicon	141	75 μm
Die0 Substrate	Silicon	141	30 μm
Bonding Layer	BCB	0.29	2.5 μm
TSV	Copper	401	30 μm
TSV-bump	Solder	50	2.5 μm

ical 45 nm technology process. The relative contribution of each material per tier is also shown in the table. In contrast to TSV-based 3D ICs, the bonding layer and bulk substrate are absent in monolithic 3D ICs while the different tiers are separated by ILD which function as the buried oxide for the SOI process for formation of subsequent device layers. Also the MIVs are tiny compared to the huge TSVs. These particular differences change the heat dissipation phenomenon of monolithic 3D ICs from that of TSV-based 3D ICs. The absence of bulk substrate and the extremely thin device layers reduce the lateral conductivity to almost zero which results in a high heat flow rate in the vertical direction towards the sink. As a result, M3D exhibits significantly better thermal properties (measured as the maximum on-chip temperature) than its TSV counterpart (Joardar et al. 2019).

3.3 Challenges and Future Research/Design Perspectives

Despite the lucrative advantages of M3D, there is no free lunch. During M3D fabrication, each tier is fabricated sequentially, from the bottom to the top. One of the major challenges is to create the top-tier transistors without impacting the already-processed bottom-tier transistors and interconnects. This requires a low temperature process for the top tier, rather than the standard thermal budget (1050 °C), to prevent any deterioration of the bottom transistors. Two common techniques to fabricate the top tier at a lower temperature include: solid phase epitaxy regrowth (SPER) (Pasini et al. 2014) and laser annealing (Fenouillet-Beranger et al. 2014). Although these techniques allow transistors to be built on top of each other (SPER = 500–600 °C (Pasini et al. 2014) and laser annealing = 400–500 °C (Fenouillet-Beranger et al. 2014) thermal budgets), they each have their disadvantages. Transistors created using SPER show three times higher source-drain resistance when compared to conventional transistors (Fenouillet-Beranger et al. 2014). On the other hand, laser-based annealing creates transistors with 15–28% lower on-current (Rajendran et al. 2007), increasing the delay for the top tier. As a result, both processes introduce performance degradation for the top-tier transistors. Additionally, tungsten is required for the back-end-of-line interconnect in the bottom tier since copper only supports temperatures up to the 400 °C range. This increases the resistivity of the interconnect in the bottom tier (copper = 1.68 $\mu\Omega$ cm vs. tungsten = 5.28 $\mu\Omega$ cm) and significantly impacts the performance of the design. This performance degradation of the top-tier transistors and increased delay in bottom-tier interconnects, must be considered during the design and optimization stages of any M3D-based design including the NoC. With these factors, future M3D designs are likely to be far more complex with additional design objectives and constraints.

Another exciting direction in M3D design is the use of carbon nanotube field effect transistors (CNFETs). CNFET-based prior works by Sabry Aly et al. (2015) indicate significant performance benefits. However, CNFET-based M3D architectures are relatively new and yet to be adopted widely. In addition, CNFETs suffer from design

challenges like relatively poor yield, lack of modeling and simulating platforms, etc. (Fadel 2015), which need to be addressed.

4 Wireless

4.1 Why Wireless Links?

In the recent past several researchers have shown that using wireless NoC (WiNoC) is a viable technology for intra- and inter-chip communication in CMOS systems (Lin et al. 2007; Duraisamy et al. 2017; Choi et al. 2018; Duraisamy et al. 2015). Wireless communication links not only alleviate the latency and energy dissipation issues of conventional electrical technologies but also eliminate complex interconnect routing and layout problems. WiNoCs enable the design of efficient architectures, which mitigate the multi-hop communication of traditional networks to achieve significant performance gains. Figure 4 presents how energy dissipated per bit changes as a function of length for both wireless and wired links. From this plot it can be observed that mm-wave wireless links are more energy efficient whenever the link length is 7 mm or more. Hence, implementation of long-range links beyond 7 mm using mm-wave wireless makes the network design energy efficient and simpler in terms of layout.

4.2 Wireless Link Designs

The efficiency of wireless links depends on the design of the on-chip antennas and the wireless transceivers. These on-chip antennas and transceivers need to be designed based on the target frequency range.

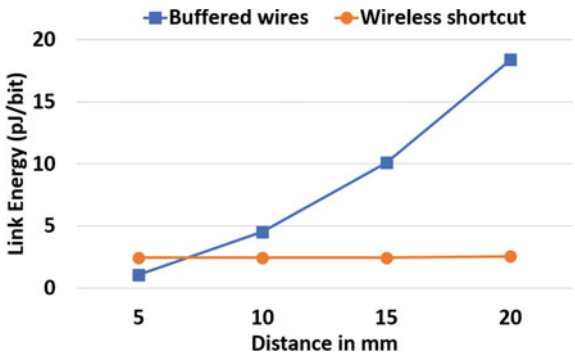

Fig. 4 Energy-per-bit variation for different link lengths (Deb et al. 2012). Each link of the wired channel is designed with the optimum number of uniformly placed and sized repeaters using 65 nm nodes

4.2.1 Ultra Wide Band (UWB) Frequency Range

The links designed in the UWB range can provide high bandwidth, low power and short-range communication. The UWB channel can be shared among multiple nodes, which makes simultaneous communication possible and can improve the communication capacity as well as reduce the communication latency. Fukuda et al. (2006) proposed an example design of UWB antenna for on-chip wireless communication. Similarly, a carrier-free impulse radio-based UWB transceiver has been utilized for on-chip communication (Deb et al. 2010). The transmitter is designed to generate the desired pulse with suitable driving strength so that signal can be efficiently radiated from an on-chip antenna. A CMOS integrated Gaussian monocycle pulse (GMP) generator creates an ultra-short pulse giving rise to extremely low power spectral density. The receiver consists of a wideband Low Noise Amplifier (LNA), a correlator, an analog-to-digital converter (ADC), and synchronization circuits. The antenna used is a 2.98 mm long meander type dipole antenna with 1 mm data transmission range. This UWB transceiver can sustain a data rate of 1.16 Gbps for a single channel at a central frequency of 3.6 GHz. However, the short transmission range of UWB makes it less efficient for long-distance communications as it would require multiple hops.

4.2.2 Millimeter (mm)-Wave

To ensure the high throughput and energy efficiency of the wireless links in mm-wave range, the transceiver circuitry has to provide a very wide bandwidth as well as low power consumption. The mm-wave frequency band can provide abundant bandwidth while not suffering from severe signal degradation for relatively short distances. In designing the on-chip mm-wave wireless transceiver, low power design considerations need to be taken into account both at the architecture and circuit levels. A metal zigzag antenna has been proposed in Lin et al. (2007) that has negligible effect of rotation (relative angle between transmitting and receiving antennas) on received signal strength. This antenna is used to design mm-wave wireless links in Deb et al. (2010). A 0.38 mm antenna achieves 3 dB bandwidth of 16 GHz with a center frequency of 57.5 GHz. By varying the axial length, trace width, arm element length and bend angle the antenna bandwidth can be varied. This type of antenna is also used to design a reconfigurable hybrid 3D wireless NoC. By placing the antennas in different layers of a 3D IC, different frequency channels can be created (More and Taskin 2010). At mm-wave frequencies the effect of metal interference structures such as power grids, local clock trees and data lines on on-chip antenna characteristics like gain and phase have been investigated (Seok and Kenneth 2005). In Yu et al. (2011), a noncoherent on-off keying (OOK) based transceiver is designed for a mm-wave wireless link. OOK is selected as it allows relatively simple and low-power circuit implementation.

Figure 5 shows an example transmitter (Tx) circuitry consisting of an up-conversion mixer and a power amplifier (PA). On the receiver (Rx) side, direct-

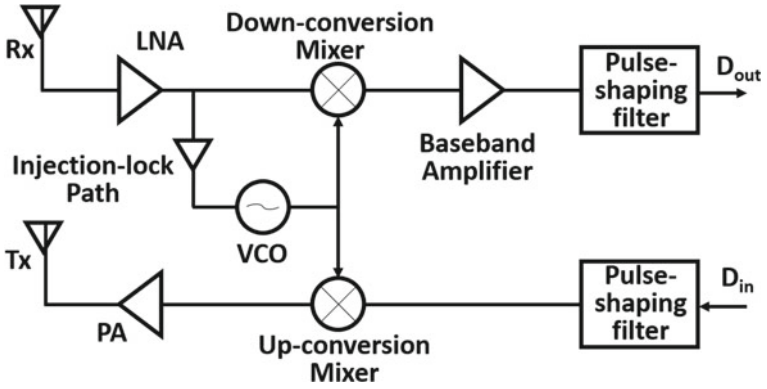

Fig. 5 Tranceiver circuit for a wireless NoC (Deb et al. 2012)

conversion topology is adopted, consisting of a LNA, a down-conversion mixer and a baseband amplifier. An injection-lock voltage-controlled oscillator (VCO) is reused for Tx and Rx. With both direct-conversion and injection-lock technology, a power-hungry phase-lock loop (PLL) is eliminated. The transceiver can sustain a data rate of 16 Gbps with power consumption of 43.6 mW in TSMC 65 nm process with an area requirement of 0.3 mm^2.

Furthermore, using body biasing methodology it is possible to improve energy efficiency without compromising the performance of high-speed analog and RF subsystems. Consequently, body biased mm-wave transceivers are capable of improving the energy efficiency of wireless links (Chang et al. 2012).

An alternative approach to mm-wave wireless links proposes to use waveguide based multi-band transmission lines called RF-I, wherein electromagnetic (EM) waves are guided along on-chip transmission lines created by multiple layers of metal and dielectric stack (Chang et al. 2008). As the EM waves travel at the effective speed of light, low latency and high bandwidth communication can be achieved. RF-I link based NoCs are predicted to dissipate an order of magnitude less power than traditional planar NoCs with significantly reduced latency. Here, RF-I based on BPSK modulation is used. RF-I performance with scaling is elaborated in Chang et al. (2008) and using 65 nm technology it is possible to have eight different frequency channels, each operating with a data rate of 6 Gbps. However, these RF-I transmission line based interconnects face several challenges in the many-core setting [20]. The RF-I transmission line needs to span the entire chip area, and requires excessive branching points to connect to local cores. Moreover, the transmission lines are not as effective as antennas at very high frequencies. The cross-talk or inter-channel interference between adjacent transmission lines may also pose problems for long transmission lines (Lee et al. 2009).

4.2.3 Sub Terahertz (Sub THz)

At Sub-Terahertz frequencies, it is possible to extend the communication range of wireless links to 10–20 mm which enables single-hop long range on-chip communication (Lee et al. 2009). In this work Lee et al. (2009), the feasibility of designing miniature antennas and simple transceivers that operate in the sub-THz frequency range for on-chip wireless communication has also been demonstrated. The proposed methodology uses 16 non-overlapping channels in the frequency range of 100–500 GHz for the on-chip wireless networks. Each channel can transmit at a rate of 10–20 Gbps in 32 nm CMOS process. A simple asynchronous amplitude-shift-keying (ASK) based system is proposed to achieve a low power and simple transceiver design in Lee et al. (2009). This design has one oscillator and one ASK modulator in the TX and one demodulator and simple baseband circuit in the RX. Overall, it uses only 1–2% of the total system power of the considered chip multiprocessor (CMP).

4.2.4 Terahertz (THz)

The antenna sizes in the THz frequency range are smaller compared to antennas at other frequencies. Hence, they occupy much less chip real estate. Characteristics of antennas operating in the THz/optical frequency range have been investigated both theoretically and experimentally (Kempa et al. 2007). These antennas can achieve a bandwidth of around 500 GHz compared to antennas operating in the millimeter wave range that achieve bandwidths of tens of gigahertz only. Thus, antennas operating in the THz/optical frequency range can support much higher data rates. Carbon Nano Tubes (CNTs) have numerous characteristics that make them suitable as on-chip antenna elements for these THz/optical frequencies. Given wavelengths of hundreds of nanometers to several micrometers in the THz range, there is a need for virtually 1D antenna structures for efficient transmission and reception. With possible diameters of a few nanometers and lengths up to a few millimeters, CNTs are the perfect candidate. Such thin structures are almost impossible to achieve with traditional micro fabrication techniques for metals. Virtually defect-free CNT structures do not suffer from power loss due to surface roughness and edge imperfections found in traditional metallic antennas. In CNTs, ballistic electron transport leads to quantum conductance, resulting in reduced resistive loss, which allows extremely high current densities, 4–5 orders of magnitude higher than copper. A 24 non-overlapping channels based architecture, each with 10 Gbps bandwidth can be created (Lee et al. 2008; Ganguly et al. 2011). Hence, CNT antenna-based wireless link is another possibility for WiNoC design as shown in Lee et al. (2008).

4.3 Challenges and Future Research/Design Perspectives

In this section, we discuss some open research issues related to designing wireless links and corresponding WiNoC architectures. Novel on-chip antennas implementations, for example, the CNT antennas, have been recently proposed and studied. However, there are challenges in manufacturing and integrating these on-chip antennas in terms of area, performance, energy overheads. An antenna-less 3D-wireless link network using inductive coupling is another alternative (Matsutani et al. 2013). However, these architectures are hard to manufacture and have thermal hotspot problems that need to be addressed. In addition, wireless links' transmission range and bandwidth (number of channels available) limitation present a major roadblock. As the size of the on-chip network is increasing, more complex topologies like Small-World NoCs, may be needed in future WiNoCs. Therefore, the design of more efficient routing algorithms and flow control mechanisms is equally important. Low-power WiNoC designs is another research direction. In addition, the wireless links in WiNoC have reliability issues which needs to be addressed. Hence, more architectural and circuit level schemes to improve the reliability for WiNoCs need to be developed for widespread adoption of WiNoC.

5 Summary and Future Perspectives

In summary, electrical links will not be able to support the communication bandwidth density and latency requirements of current and future heterogeneous systems. We need to explore novel link technologies as a replacement to the electrical link technology. In this chapter, we have provided a detailed overview of the fundamentals of three different link technologies—photonic link technology, monolithic 3D link technology and wireless link technology. At this point, there is no clear winner in terms of which technology will replace electrical links. Each one of these new link technologies is better than the electrical link technology in some aspects, but they also have their short comings. There is plenty of active ongoing research in the development of each one of these novel link technologies. Overall, given that each link technology provides a unique advantage compared to other link technologies, we believe that future systems will be designed using a mix of electrical, photonic, monolithic 3D and wireless links.

References

J.L. Abellán, A.K. Coskun, A. Gu, W. Jin, A. Joshi, A.B. Kahng, J. Klamkin, C. Morales, J. Recchio, V. Srinivas, T. Zhang, Adaptive tuning of photonic devices in a photonic NoC through dynamic workload allocation. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. **36**(5), 801–814 (2017)

F. Andrieu, P. Batude, L. Brunet, C. Fenouillet-Béranger, D. Lattard, S. Thuries, O. Billoint, R. Fournel, M. Vinet, A review on opportunities brought by 3D-monolithic integration for CMOS device and digital circuit, in *2018 International Conference on IC Design Technology (ICICDT)*, June 2018, pp. 141–144

K. Banerjee, S.J. Souri, P. Kapur, K.C. Saraswat, 3-d ICs: a novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration. Proc. IEEE **89**(5), 602–633 (2001)

T. Barwicz, H. Byun, F. Gan, C. Holzwarth, M. Popovic, P. Rakich, M. Watts, E. Ippen, F. Kärtner, H. Smith et al., Silicon photonics for compact, energy-efficient interconnects. J. Opt. Netw. **6**(1), 63–73 (2007)

T. Barwicz, M.A. Popovic, P.T. Rakich, M.R. Watts, H.A. Haus, E.P. Ippen, H.I. Smith, Microring-resonator-based add-drop filters in sin: fabrication and analysis. Opt. Express **12**(7), 1437–1442 (2004)

C. Batten, A. Joshi, V. Stojanovic, K. Asanovic, Designing chip-level nanophotonic interconnection networks. IEEE J. Emerg. Select. Top. Circuits Syst. **2**(2), 137–153 (2012)

P. Batude, T. Ernst, J. Arcamone, G. Arndt, P. Coudrain, P. Gaillardon, 3D sequential integration: a key enabling technology for heterogeneous co-integration of new function with cmos. IEEE J. Emerg. Select. Top. Circuits Syst. **2**(4), 714–722 (2012)

P. Batude, B. Sklenard, C. Fenouillet-Beranger, B. Previtali, C. Tabone, O. Rozeau, O. Billoint, O. Turkyilmaz, H. Sarhan, S. Thuries, G. Cibrario, L. Brunet, F. Deprat, J. Michallet, F. Clermidy, M. Vinet, 3D sequential integration opportunities and technology optimization, in *IEEE International Interconnect Technology Conference*, May 2014, pp. 373–376

S. Beamer, C. Sun, Y.-J. Kwon, A. Joshi, C. Batten, V. Stojanović, K. Asanović, Re-architecting dram memory systems with monolithically integrated silicon photonics, in *ACM SIGARCH Computer Architecture News*, vol. 38 (ACM, 2010), pp. 129–140

A. Biberman, K. Bergman, Optical interconnection networks for high-performance computing systems. Rep. Progr. Phys. **75**(4), 046402 (2012)

S. Bobba, A. Chakraborty, O. Thomas, P. Batude, T. Ernst, O. Faynot, D.Z. Pan, G. De Micheli, Celoncel: effective design technique for 3D monolithic integration targeting high performance integrated circuits, in *16th Asia and South Pacific Design Automation Conference (ASP-DAC 2011)*, Jan 2011, pp. 336–343

S. Borkar, 3D integration for energy efficient system design, in *2011 48th ACM/EDAC/IEEE Design Automation Conference (DAC)*, June 2011, pp. 214–219

K. Chang, S. Deb, A. Ganguly, X. Yu, S.P. Sah, P.P. Pande, B. Belzer, D. Heo, Performance evaluation and design trade-offs for wireless network-on-chip architectures. J. Emerg. Technol. Comput. Syst. **8**(3) (2012)

M.F. Chang, J. Cong, A. Kaplan, M. Naik, G. Reinman, E. Socher, S. Tam, CMP network-on-chip overlaid with multi-band RF-interconnect, in *2008 IEEE 14th International Symposium on High Performance Computer Architecture*, Feb 2008, pp. 191–202

C. Chen, J.L. Abellán, A. Joshi, Managing laser power in silicon-photonic NoC through cache and NoC reconfiguration. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. **34**(6), 972–985 (2015)

C. Chen, A. Joshi, Runtime management of laser power in silicon-photonic multibus NoC architecture. IEEE J. Select. Top. Quantum Electron. **19**(2), 3700713–3700713 (2013)

C. Chen, T. Zhang, P. Contu, J. Klamkin, A.K. Coskun, A. Joshi, Sharing and placement of on-chip laser sources in silicon-photonic NoCs, in *2014 Eighth IEEE/ACM International Symposium on Networks-on-Chip (NoCS)* (IEEE, 2014), pp. 88–95

W. Choi, K. Duraisamy, R.G. Kim, J.R. Doppa, P.P. Pande, D. Marculescu, R. Marculescu, On-chip communication network for efficient training of deep convolutional networks on heterogeneous many core systems. IEEE Trans. Comput. **67**(5), 672–686 (2018)

S. Das, J.R. Doppa, P.P. Pande, K. Chakrabarty, Monolithic 3D-enabled high performance and energy efficient network-on-chip, in *2017 IEEE International Conference on Computer Design (ICCD)*, Nov 2017, pp. 233–240

W.R. Davis, J. Wilson, S. Mick, J. Xu, H. Hua, C. Mineo, A.M. Sule, M. Steer, P.D. Franzon, Demystifying 3D ICs: the pros and cons of going vertical. IEEE Des. Test Comput. **22**(6), 498–510 (2005)

S. Deb, A. Ganguly, K. Chang, P. Pande, B. Beizer, D. Heo, Enhancing performance of network-on-chip architectures with millimeter-wave wireless interconnects, in *ASAP 2010: 21st IEEE International Conference on Application-specific Systems, Architectures and Processors*, July 2010, pp. 73–80

S. Deb, A. Ganguly, P.P. Pande, B. Belzer, D. Heo, Wireless NoC as interconnection backbone for multicore chips: promises and challenges. IEEE J. Emerg. Select. Top. Circuits Syst. **2**(2), 228–239 (2012)

Y. Demir, N. Hardavellas, Parka: thermally insulated nanophotonic interconnects, in *Proceedings of the 9th International Symposium on Networks-on-Chip, NOCS'15, New York, NY, USA* (Association for Computing Machinery, 2015)

V. Deshpande, H. Hahn, E. O'Connor, Y. Baumgartner, M. Sousa, D. Caimi, H. Boutry, J. Widiez, L. Brévard, C. Le Royer, M. Vinet, J. Fompeyrine, L. Czornomaz, First demonstration of 3D SRAM through 3D monolithic integration of InGaAs n-FinFETs on FDSOI SI CMOS with inter-layer contacts, in *2017 Symposium on VLSI Technology*, June 2017, pp. T74–T75

K. Duraisamy, H. Lu, P.P. Pande, A. Kalyanaraman, High performance and energy efficient wireless NoC-enabled multicore architectures for graph analytics, in *2015 International Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES)* (2015), pp. 147–156

K. Duraisamy, Y. Xue, P. Bogdan, P.P. Pande, Multicast-aware high-performance wireless network-on-chip architectures. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **25**(3), 1126–1139 (2017)

Y. Eckert, N. Jayasena, G.H. Loh, Thermal feasibility of die-stacked processing in memory, in *Proceedings of the 2nd Workshop Near-Data Processing* (2014)

T. Fadel, Realizing the promise of carbon nanotubes: challenges, opportunities, and the pathway to commercialization (2015), https://www.nano.gov/sites/default/files/pub_resource/2014_nni_cnt_tech_meeting_report.pdf

C. Fenouillet-Beranger, B. Mathieu, B. Previtali, M. Samson, N. Rambal, V. Benevent, S. Kerdiles, J. Barnes, D. Barge, P. Besson, R. Kachtouli, M. Cassé, X. Garros, A. Laurent, F. Nemouchi, K. Huet, I. Toqué-Trésonne, D. Lafond, H. Dansas, F. Aussenac, G. Druais, P. Perreau, E. Richard, S. Chhun, E. Petitprez, N. Guillot, F. Deprat, L. Pasini, L. Brunet, V. Lu, C. Reita, P. Batude, M. Vinet, New insights on bottom layer thermal stability and laser annealing promises for high performance 3D VLSI, in *2014 IEEE International Electron Devices Meeting*, Dec 2014, pp. 27.5.1–27.5.4

M. Fukuda, P. Saha, N. Sasaki, M. Nitta, T. Kikkawa, A 0.18 μm CMOS impulse radio based UWB transmitter for global wireless interconnections of 3D stacked-chip system (2006)

A. Ganguly, K. Chang, S. Deb, P.P. Pande, B. Belzer, C. Teuscher, Scalable hybrid wireless network-on-chip architectures for multicore systems. IEEE Trans. Comput. **60**(10), 1485–1502 (2011)

Y. Gong, J. Kong, S.W. Chung, Quantifying the impact of monolithic 3D (M3D) integration on L1 caches. IEEE Trans. Emerg. Top. Comput. 1–1 (2019)

B. Gopireddy, J. Torrellas, Designing vertical processors in monolithic 3D, in *Proceedings of the 46th International Symposium on Computer Architecture, ISCA'19, New York, NY, USA* (Association for Computing Machinery, 2019), pp. 643–656

C. Gunn, CMOS photonics for high-speed interconnects. IEEE Micro. **26**(2), 58–66 (2006)

Y. Heights, Silicon integrated nanophotonics (2010), http://www.nanotech-now.com/

ITRS, ITRS (2007), http://www.itrs.net/Links/2007ITRS/Home2007.htm

B.K. Joardar, P. Ghosh, P.P. Pande, A. Kalyanaraman, S. Krishnamoorthy, NoC-enabled software/hardware co-design framework for accelerating k-mer counting, in *Proceedings of the 13th IEEE/ACM International Symposium on Networks-on-Chip, NOCS'19, New York, NY, USA* (Association for Computing Machinery, 2019)

A. Joshi, C. Batten, Y.-J. Kwon, S. Beamer, I. Shamim, K. Asanovic, V. Stojanovic, Silicon-photonic clos networks for global on-chip communication, in *2009 3rd ACM/IEEE International Symposium on Networks-on-Chip* (IEEE, 2009), pp. 124–133

S. Jung, H. Lim, C. Yeo, K. Kwak, B. Son, H. Park, J. Na, J. Shim, C. Hong, K. Kim, High speed and highly cost effective 72M bit density s3 SRAM technology with doubly stacked Si layers, peripheral only CoSix layers and tungsten shunt W/L scheme for standalone and embedded memory, in *2007 IEEE Symposium on VLSI Technology*, June 2007, pp. 82–83

K. Kempa, J. Rybczynski, Z. Huang, K. Gregorczyk, A. Vidan, B. Kimball, J. Carlson, G. Benham, Y. Wang, A. Herczynski, Z. Ren, Carbon nanotubes as optical antennae. Adv. Mater. **19**, 421–426 (2007)

T. Kuroda, 3D integration, power delivery, and contactless interconnect by near field coupling, in *IEEE ISSCC* (2014)

B.G. Lee, X. Chen, A. Biberman, X. Liu, I. Hsieh, C. Chou, J.I. Dadap, F. Xia, W.M.J. Green, L. Sekaric, Y.A. Vlasov, R.M. Osgood, K. Bergman, Ultrahigh-bandwidth silicon photonic nanowire waveguides for on-chip networks. IEEE Photon. Technol. Lett. **20**(6), 398–400 (2008)

S.-B. Lee, S.-W. Tam, I. Pefkianakis, S. Lu, M.F. Chang, C. Guo, G. Reinman, C. Peng, M. Naik, L. Zhang et al., A scalable micro wireless interconnect structure for CMPS, in *Proceedings of the 15th Annual International Conference on Mobile Computing and Networking, MobiCom'09, New York, NY, USA* (Association for Computing Machinery, 2009), pp. 217–228

C. Li, M. Browning, P.V. Gratz, S. Palermo, Luminoc: a power-efficient, high-performance, photonic network-on-chip. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. **33**(6), 826–838 (2014)

J. Lin, H. Wu, Y. Su, L. Gao, A. Sugavanam, J.E. Brewer, K.O. Kenneth, Communication using antennas fabricated in silicon integrated circuits. IEEE J. Solid-State Circuits **42**(8), 1678–1687 (2007)

M. Lin, A. El Gamal, Y. Lu, S. Wong, Performance benefits of monolithically stacked 3D FPGA. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. **26**(2), 216–229 (2007)

H. Matsutani, P. Bogdan, R. Marculescu, Y. Take, D. Sasaki, H. Zhang, M. Koibuchi, T. Kuroda, H. Amano, A case for wireless 3D NoCs for CMPS, in *2013 18th Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan 2013, pp. 23–28

A. More, B. Taskin, Simulation based study of on-chip antennas for a reconfigurable hybrid 3D wireless NoC, in *23rd IEEE International SOC Conference*, Sep. 2010, pp. 447–452

S. Musavvir, A. Chatterjee, R.G. Kim, D.H. Kim, P.P. Pande, Inter-tier process-variation-aware monolithic 3D NoC design space exploration. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **28**(3), 686–699 (2020)

T. Nakahara, H. Tsuda, K. Tateno, S. Matsuo, T. Kurokawa, Hybrid integration of smart pixels by using polyimide bonding: demonstration of a GaAs p-i-n photodiode/CMOS receiver. IEEE J. Select. Top. Quantum Electron. **5**(2), 209–216 (1999)

A. Narayan, Y. Thonnart, P. Vivet, A. Joshi, A.K. Coskun, System-level evaluation of chip-scale silicon photonic networks for emerging data-intensive applications, in *2020 Design, Automation & Test in Europe Conference & Exhibition (DATE)* (IEEE, 2020), pp. 1444–1449

A. Narayan, Y. Thonnart, P. Vivet, C.F. Tortolero, A.K. Coskun, Waves: wavelength selection for power-efficient 2.5D-integrated photonic NoCs, in *Design, Automation & Test in Europe Conference & Exhibition (DATE)* (IEEE, 2019), pp. 516–521

J.S. Orcutt, B. Moss, C. Sun, J. Leu, M. Georgas, J. Shainline, E. Zgraggen, H. Li, J. Sun, M. Weaver et al., Open foundry platform for high-performance electronic-photonic integration. Opt. Express **20**(11), 12222–12232 (2012)

Y. Pan, J. Kim, G. Memik, Flexishare: channel sharing for an energy-efficient nanophotonic crossbar, in *HPCA - 16 2010 The Sixteenth International Symposium on High-Performance Computer Architecture*, Jan 2010, pp. 1–12

S. Panth, K. Samadi, Y. Du, S.K. Lim, High-density integration of functional modules using monolithic 3D-IC technology, in *2013 18th Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan 2013, pp. 681–686

L. Pasini, P. Batude, M. Cassé, L. Brunet, P. Rivallin, B. Mathieu, J. Lacord, S. Martinie, C. Fenouillet-Beranger, B. Previtali, N. Rambal, M. Haond, G. Ghibaudo, M. Vinet, nFET FDSOI activated by low temperature solid phase epitaxial regrowth: optimization guidelines, in *2014 SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, Oct 2014, pp. 1–2

S. Pasricha, M. Nikdast, A survey of silicon photonics for energy efficient manycore computing, in *IEEE Design Test* (2020), pp. 1–1

B. Rajendran, R.S. Shenoy, D.J. Witte, N.S. Chokshi, R.L. DeLeon, G.S. Tompa, R.F.W. Pease, Low thermal budget processing for sequential 3D IC fabrication. IEEE Trans. Electron Devices **54**(4), 707–714 (2007)

M.M. Sabry Aly, M. Gao, G. Hills, C. Lee, G. Pitner, M.M. Shulaker, T.F. Wu, M. Asheghi, J. Bokor, F. Franchetti, K.E. Goodson, C. Kozyrakis, I. Markov, K. Olukotun, L. Pileggi, E. Pop, J. Rabaey, C. Ré, H.S.P. Wong, S. Mitra, Energy-efficient abundant-data computing: the N3Xt 1,000x. Computer **48**(12):24–33 (2015)

S.K. Samal, D. Nayak, M. Ichihashi, S. Banna, S.K. Lim, Monolithic 3D IC vs. TSV-based 3D IC in 14nm FinFET technology, in *2016 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, Oct 2016, pp. 1–2

S.K. Samal, S. Panth, K. Samadi, M. Saedi, Y. Du, S.K. Lim, Fast and accurate thermal modeling and optimization for monolithic 3D ICs, in *2014 51st ACM/EDAC/IEEE Design Automation Conference (DAC)*, June 2014, pp. 1–6

E. Seok, K.O. Kenneth, Design rules for improving predictability of on-chip antenna characteristics in the presence of other metal structures, in *Proceedings of the IEEE 2005 International Interconnect Technology Conference*, June 2005, pp. 120–122

C. Shen, J. Shieh, T. Wu, W. Huang, C. Yang, C. Wan, C. Lin, H. Wang, B. Chen, G. Huang, Y. Lien, S. Wong, C. Wang, Y. Lai, C. Chen, M. Chang, C. Hu, F. Yang, Monolithic 3D chip integrated with 500ns NVM, 3ps logic circuits and SRAM, in *2013 IEEE International Electron Devices Meeting*, Dec 2013, pp. 9.3.1–9.3.4

V. Stojanović, R.J. Ram, M. Popović, S. Lin, S. Moazeni, M. Wade, C. Sun, L. Alloatti, A. Atabaki, F. Pavanello et al., Monolithic silicon-photonic platforms in state-of-the-art CMOS SOI processes. Opt. Express **26**(10), 13106–13121 (2018)

C. Sun, M. Georgas, J. Orcutt, B. Moss, Y. Chen, J. Shainline, M. Wade, K. Mehta, K. Nammari, E. Timurdogan, D. Miller, O. Tehar-Zahav, Z. Sternberg, J. Leu, J. Chong, R. Bafrali, G. Sandhu, M. Watts, R. Meade, M. Popović, R. Ram, V. Stojanović, A monolithically-integrated chip-to-chip optical link in bulk CMOS. IEEE J. Solid-State Circuits **50**(4), 828–844 (2015a)

C. Sun, M.T. Wade, Y. Lee, J.S. Orcutt, L. Alloatti, M.S. Georgas, A.S. Waterman, J.M. Shainline, R.R. Avizienis, S. Lin, B.R. Moss, R. Kumar, F. Pavanello, A.H. Atabaki, H.M. Cook, A.J. Ou, J.C. Leu, Y.-H. Chen, K. Asanović, R.J. Ram, M. Popović, V.M. Stojanović, Single-chip microprocessor that communicates directly using light. Nature **528**(7583), 534–538 (2015b)

Y. Thonnart, S. Bernabé, J. Charbonnier, C. Bernard, D. Coriat, C. Fuguet, P. Tissier, B. Charbonnier, S. Malhouitre, D. Saint-Patrice, M. Assous, A. Narayan, A. Coskun, D. Dutoit, P. Vivet, POPSTAR: a robust modular optical NoC architecture for chiplet-based 3D integrated systems, in *Design, Automation & Test in Europe Conference & Exhibition (DATE)* (2020)

T. Uhrmann, T. Wagenleitner, T. Glinsner, M. Wimplinger, P. Lindner, Monolithic IC integration key alignment aspects for high process yield, in *2014 SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, Oct 2014, pp. 1–2

R. Venkatesan, J.A. Davis, K.A. Bowman, J.D. Meindl, Optimal n-tier multilevel interconnect architectures for gigascale integration (GSI). IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **9**(6), 899–912 (2001)

M. Vinet, P. Batude, C. Fenouillet-Beranger, F. Clermidy, L. Brunet, O. Rozeau, J. Hartmannn, O. Billoint, G. Cibrario, B. Previtali, C. Tabone, B. Sklenard, O. Turkyilmaz, F. Ponthenier, N. Rambal, M. Samson, F. Deprat, V. Lu, L. Pasini, S. Thuries, H. Sarhan, J. Michallet, O. Faynot, Monolithic 3D integration: a powerful alternative to classical 2D scaling, in *2014 SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, Oct 2014, pp. 1–3

T. Wu, C. Shen, J. Shieh, W. Huang, H. Wang, F. Hsueh, H. Chen, C. Yang, T. Hsieh, B. Chen, Y. Shiao, C. Yang, G. Huang, K. Li, T. Hsueh, C. Chen, W. Chen, F. Yang, M. Chang, W. Yeh, Low-cost and TSV-free monolithic 3D IC with heterogeneous integration of logic, memory and sensor analogy circuitry for internet of things, in *2015 IEEE International Electron Devices Meeting (IEDM)*, Dec 2015, pp. 25.4.1–25.4.4

Q. Xu, D. Fattal, R.G. Beausoleil, Silicon microring resonators with 1.5-μm radius. Opt. Express **16**(6), 4309–4315 (2008)

X. Yu, S. P. Sah, S. Deb, P.P. Pande, B. Belzer, D. Heo. A wideband body-enabled millimeter-wave transceiver for wireless network-on-chip, in *2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug 2011, pp. 1–4

Y. Yu, N.K. Jha, Energy-efficient monolithic three-dimensional on-chip memory architectures. IEEE Trans. Nanotechnol. **17**(4), 620–633 (2018)

L. Zhou, A.K. Kodi, Probe: prediction-based optical bandwidth scaling for energy-efficient NoCs, in *2013 Seventh IEEE/ACM International Symposium on Networks-on-Chip (NoCS)*, April 2013, pp. 1–8