Optical Quadruple New Gate Using SLM and Savart Plate

Supriti Samanta, Aranya Manna, Goutam Kumar Maity, and Subhadipta Mukhopadhyay

1 Introduction

In recent years, the benefits of computer digital circuit technology have made feasible testing and implementation of electronic circuit's operation with over two discrete levels of signals. This provides the concept of multi-valued logic (MVL). Dubrova [1] et al. have proposed and presented MVL circuit design, revealing both the opportunities provided by them and also the challenges faced by them [2–4]. Different arithmetic operations like addition, multiplications in the Galois field and also addition, subtraction and multiplication in modulo-4 arithmetic are demonstrated in the MVL system by Patel and Gurumurthy [5]. Quaternary to binary and binary to quaternary converters are also designed for this purpose [6].

The benefits of technology during the last 20 years have generated an oversized demand for handling a large volume of knowledge at high speed. To fulfill up the wants, the concept of MVL has come forward from the status of the two-valued or binary logic system within the one hand, and on the other side, these include the concept of the optical processor for switches. Simultaneous operation is often performed using optical processors but it absolutely was also felt that it are often possible to represent multi-valued logic using the polarization states of the sunshine beam with the presence or absence of sunshine in the optical system [7]. Avizienis introduced a signed digit numeration system for proper utilization of parallelism of the optical beam rather than cascaded single-bit operating units [8]. The modified

S. Samanta (✉) · S. Mukhopadhyay
Department of Physics, Jadavpur University, Kolkata 700032, India

A. Manna
Department of Physics, Sabang Sajanikanta Mahavidyalaya, Paschim-Medinipur 721166, West Bengal, India

G. K. Maity
Department of Physics, Raipur Block Mahavidyalaya, Bankura 722134, West Bengal, India

C. K. Chanda et al. (eds.), *Advanced Energy and Control Systems*, Lecture Notes in Electrical Engineering 820, https://doi.org/10.1007/978-981-16-7274-3_19

signed digit [9–12] or modified trinary numeration system suggested the carry free operation. The ternary logic system supported three states which were introduced by Lukasiewicz, and further, it absolutely was modified by him to four states logic for a better proposition.

The irreversible operation produces information loss which ends up in energy dissipation. The energy dissipated for each irreversible bit operation is a minimum of KTln2 joules in keeping with Landauer's research; here, T is the operating temperature and K = 1.3806505 * 10^{-2} 3 m^2 kgs^{-2} K^{-1} joule/kelvin is Boltzmann's constant. The above-mentioned energy is often saved if the operation could be reversible operation as described by Bennett in 1973. Reversible operation means inputs also can be derived from the output.

Different applications for lossless data processing are often performed using reversible operation. The design of reversible logic optically is incredibly important for faster operation. With this aim, an optical quadruple new Gate using SLM and Savart Plate is presented in this paper. Savart plate is made with a double-plate device used to transmit polarized light where interference fringes of lights are formed which indicates the presence of a signal. There are two calcite plates of equal thickness, cut parallel to their natural cleavage faces with rotation and cemented together which forms a right angle to each other.

The proposed paper is organized as follows: Section 2 deals with the quadruple valued logic systems and their explanation. Section 3 describes briefly the truth tables of Di-bit representation. Section 4 presents the operation of the basic building block circuit using SLM and Savart Plate. The operating principle and design of Quadruple new Gate are represented in Sect. 5. Theological simulation results and final conclusion with the scope of future works are made in Sect. 6 and Sect. 7, respectively.

2 Quadruple Logic System

The four states of the quadruple logic system are represented as the right, partly right, wrong and the partly wrong. As the quadruple system with states {0, 1, 2, 3} does not satisfy the basic field conditions so, a Di-bit representation of the logic 00 0, 01 1, 10 2 and 11 3 is considered which is similar to basic two-valued logic system.

For quaternary logic, i.e., with four states, Galoisfield may be represented as GF(2^2), i.e., k and r both are considered here 2. The elements and the states {0,1,2,3} of GF(2^2) are represented by di-bit as {00, 01, 10, 11}, respectively. Table 1 represents the states of logic, representation of them and corresponding Di-bit representations and the state of polarization.

Table 1 Quadruple logic system

Logical state	Represented by	Dibit representation	State of polarization
False/wrong information	0	00	No light
Partial information	1	01	Vertical polarization
Partial information (complement of 1)	2	10	Horizontal polarization
True/complete information	3	11	The presence of both the horizontal annd vertical polarization

3 Truth Tables Based on Di-Bit Representation

Truth tables of different quadruple logic gates are represented bit-wise in this section (Table 2).

Table 2 Truth tables for **a** OR, **b** AND, **c** NOT **d** XOR, **e** NAND, **f** NOR and **g** XNOR Gates

A / B	00	01	10	11
00	00	01	10	11
01	01	01	11	11
10	10	11	10	11
11	11	11	11	11

(a)

A / B	00	01	10	11
00	00	00	00	00
01	00	01	00	01
10	00	00	10	10
11	00	01	10	11

(b)

A	Ā
00	11
01	10
10	01
11	00

(c)

A / B	00	01	10	11
00	00	01	10	11
01	01	00	11	10
10	10	11	00	01
11	11	10	01	00

(d)

A / B	00	01	10	11
00	11	11	11	11
01	11	10	11	10
10	11	11	01	01
11	11	10	01	00

(e)

A / B	00	01	10	11
00	11	10	01	00
01	10	10	00	00
10	01	00	01	00
11	00	00	00	00

(f)

A / B	00	01	10	11
00	11	10	01	00
01	10	11	00	01
10	01	00	11	10
11	00	01	10	11

(g)

4 The Basic Building Block

The basic building block performance of the rational processing quadruple valued logic system is shown in Fig. 1. Light output from laser source L after getting polarized at an angle of 45° with respect to the two orbits is incident on the Savart Plate S_1 as shown in Fig. 1. The Savart plate S_1 is used to split the light into two components. The output of S_1 is controlled by electrically addressable negative SLMs—P_1 and P_2. The SLMs are controlled by electrical signals applied on them. The negative SLM becomes opaque when an electric voltage is applied on it and then it becomes transparent when no electric voltage is applied on it. The operation of positive SLM is just the opposite of negative SLM. The outputs from SLM are finally combined by the Savart Plate S2. The flow chart of the basic building block is also provided in Fig. 2 to understand the operational process.

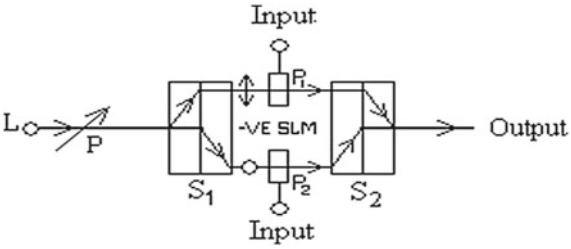

Fig. 1 The basic building block

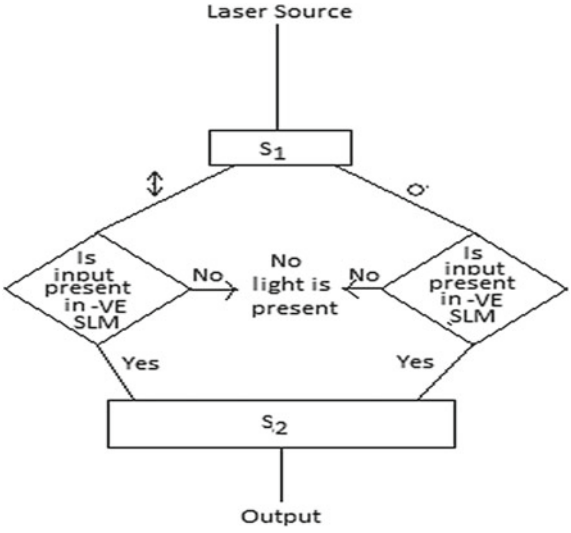

Fig. 2 The flow chart of the basic structure block

5 Theoretical Principles of Design

A quadruple new gate is an integrated circuit of four logic gates. The gates can be of any type of AND, OR, NOT, NOR, NAND, XOR and XNOR. For any given quadruple new gate, all four of the individual gates are considered of the same types. A quadruple new gate is a unique building block of a digital circuit as the logic output mentioned in the truth table of Table 3. As the basic principle of gates, most of the basic logic gates have two inputs and one output. At any time, every gate is in one of the two binary states, low(0) or high(1), represented by different voltages as designed. Quadruple new gates can be used in various digital applications including flip flop, digital switches, voltage-controlled oscillator, waveform generator, etc.

5.1 The Operating Principle and Design of Quadruple New Gate

A quadruple new gate (NG) has three inputs terminal (A, B, C) and three outputs terminal (P, Q, R). It is a combinational circuit of OR, XOR, XNOR, etc. logic gate, and these different types of logic gates are interconnected to each other. The quadruple NAND gate has diverse uses of particular interest, because other basic logic functions can be derived through multiple NAND gates developing different connections of circuits. This property makes the quadruple NAND gate a universal digital substitute for other gates. It satisfies the relations as follows (Fig. 3 and Table 4).

Table 3 Truth table of new proposed gate

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	1	0	0

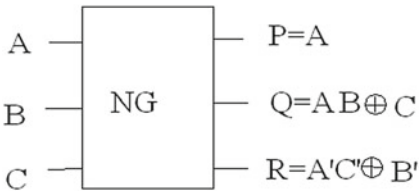

Fig. 3 Schematic diagram of New Gate

5.2 Operating Principle

The operating principle of the quadruple new gate is described in Fig. 4. Every input terminal is consisting of two components and every output terminal is consisting of two components. So, the result of output is of different types: true, partly true, partly false and false. It is evident that the output, P, is similar to that of the input, A, and the outputs of Q and R are dependent upon the inputs of A, B and C. We have described the inputs A, B and C and their corresponding outputs P, Q and R simultaneously.

I. If $A = B = C = 0$, as a result, no light comes out from S_6, S_{10}, S_{14}, $S_{20,}$ S_{24}, S_{28} . So the final results are zero (i.e., $Q = R = 0$).

II. If $A = B = 0$ but $C = 1$ ($c_j = 0$, $c_i = 1$), as a result, light from S_{10}, S_{14} and S_{28} is perpendicular polarized and the final result is perpendicular polarized (i.e., $Q = R = 1$).

III. If $A = B = 0$ and $C = 2$ ($c_j = 1$, $c_i = 0$), as a result, light from S_{10}, S_{14} and S_{28} is straight polarized and the final result is straight polarized (i.e., $Q = R = 2$).

IV. If $A = B = 0$ but $C = 3$ ($c_j = 1$, $c_i = 1$), as a result, light from the S_{10}, S_{14} and S_{28}has been perpendicular polarized. The final results are both straight and perpendicular polarized (i.e., $Q = R = 3$).

V. If $A = C = 0$ but $B = 1$ (i.e., $b_j = 0$, $b_i = 1$), as a result, no light comes out from the S_6, S_{10} and S_{14} but the output of S_{20} is perpendicular polarized and the output, Q, is zero (i.e., $Q = 0$) but the output, R, is perpendicular polarized (i.e., $R = 1$). If $A = 0$ and $B = C = 1$, then the output of $S_{10}$is perpendicular polarized but no light comes out from the $S_{20,}$ S_{24} and S_{28}. So the output, Q, is perpendicular polarized (i.e., $Q = 1$), and the output, R, will be zero (i.e., $R = 0$).

VI. If $A = 0$, $B = 1$ and $C = 2$, as a result, the light that comes out from the S_{10} and $S_{14}$is straight polarized, and output, Q, is straight polarized (i.e., $Q = 2$). But the output of S_{20} is perpendicular polarized and the output of $S_{28}$is both perpendicular and straight polarized. So the output, R, will be both (perpendicular and straight) polarized (i.e., $R = 3$).

VII. If $A = 0$, $B = 1$ and $C = 3$, as a result, the light that comes as output from $S_{10}$is both (straight and perpendicular) polarized and the output of S_{14} will be straight polarized. So the output, Q, will be both (perpendicular and straight) polarized (i.e., $Q = 3$). The output of S_{28} will be straight polarized. So the output, R, will be straight polarized (i.e., $R = 2$).

Table 4 The truth table of proposed new gate

Inputs									Outputs								
A	a_i	a_j	B	b_i	b_j	C	c_i	c_j	P	p_i	p_j	Q	q_i	q_j	R	r_i	r_j
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	1	0	1
0	0	0	0	0	0	2	1	0	0	0	0	2	1	0	2	1	0
0	0	0	0	0	0	3	1	1	0	0	0	3	1	1	3	1	1
0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	1
0	0	0	1	0	1	1	0	1	0	0	0	1	0	1	0	0	0
0	0	0	1	0	1	2	1	0	0	0	0	2	1	0	3	1	1
0	0	0	1	0	1	3	1	1	0	0	0	3	1	1	2	1	0
0	0	0	2	1	0	0	0	0	0	0	0	0	0	0	2	1	0
0	0	0	2	1	0	1	0	1	0	0	0	1	0	1	3	1	1
0	0	0	2	1	0	2	1	0	0	0	0	2	1	0	0	0	0
0	0	0	2	1	0	3	1	1	0	0	0	3	1	1	1	0	1
0	0	0	3	1	1	0	0	0	0	0	0	0	0	0	3	1	1
0	0	0	3	1	1	1	0	1	0	0	0	1	0	1	2	1	0
0	0	0	3	1	1	2	1	0	0	0	0	2	1	0	1	0	1
0	0	0	3	1	1	3	1	1	0	0	0	3	1	1	0	0	0
1	0	1	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1
1	0	1	0	0	0	1	0	1	1	0	1	1	0	1	1	0	1
1	0	1	0	0	0	2	1	0	1	0	1	2	1	0	3	1	1
1	0	1	0	0	0	3	1	1	1	0	1	3	1	1	3	1	1
1	0	1	1	0	1	0	0	0	1	0	1	1	0	1	0	0	0
1	0	1	1	0	1	1	0	1	1	0	1	0	0	0	0	0	0
1	0	1	1	0	1	2	1	0	1	0	1	3	1	1	2	1	0
1	0	1	1	0	1	3	1	1	1	0	1	2	1	0	2	1	0
1	0	1	2	1	0	0	0	0	1	0	1	0	0	0	3	1	1
1	0	1	2	1	0	1	0	1	1	0	1	1	0	1	3	1	1
1	0	1	2	1	0	2	1	0	1	0	1	2	1	0	1	0	1
1	0	1	2	1	0	3	1	1	1	0	1	3	1	1	1	0	1
1	0	1	3	1	1	0	0	0	1	0	1	1	0	1	2	1	0
1	0	1	3	1	1	1	0	1	1	0	1	0	0	0	2	1	0
1	0	1	3	1	1	2	1	0	1	0	1	3	1	1	0	0	0
1	0	1	3	1	1	3	1	1	1	0	1	2	1	0	0	0	0
2	1	0	0	0	0	0	0	0	2	1	0	0	0	0	2	1	0
2	1	0	0	0	0	1	0	1	2	1	0	1	0	1	3	1	1
2	1	0	0	0	0	2	1	0	2	1	0	2	1	0	2	1	0

(continued)

Table 4 (continued)

Inputs									Outputs								
A	a_i	a_j	B	b_i	b_j	C	c_i	c_j	P	p_i	p_j	Q	q_i	q_j	R	r_i	r_j
2	1	0	0	0	0	3	1	1	2	1	0	3	1	1	3	1	1
2	1	0	1	0	1	0	0	0	2	1	0	0	0	0	3	1	1
2	1	0	1	0	1	1	0	1	2	1	0	1	0	1	2	1	0
2	1	0	1	0	1	2	1	0	2	1	0	2	1	0	3	1	1
2	1	0	1	0	1	3	1	1	2	1	0	3	1	1	2	1	0
2	1	0	2	1	0	0	0	0	2	1	0	2	1	0	0	0	0
2	1	0	2	1	0	1	0	1	2	1	0	3	1	1	1	0	1
2	1	0	2	1	0	2	1	0	2	1	0	0	0	0	0	0	0
2	1	0	2	1	0	3	1	1	2	1	0	1	0	1	1	0	1
2	1	0	3	1	1	0	0	0	2	1	0	2	1	0	1	0	1
2	1	0	3	1	1	1	0	1	2	1	0	3	1	1	0	0	0
2	1	0	3	1	1	2	1	0	2	1	0	0	0	0	1	0	1
2	1	0	3	1	1	3	1	1	2	1	0	1	0	1	0	0	0
3	1	1	0	0	0	0	0	0	3	1	1	0	0	0	3	1	1
3	1	1	0	0	0	1	0	1	3	1	1	1	0	1	3	1	1
3	1	1	0	0	0	2	1	0	3	1	1	2	1	0	3	1	1
3	1	1	0	0	0	3	1	1	3	1	1	3	1	1	3	1	1
3	1	1	1	0	1	0	0	0	3	1	1	1	0	1	2	1	0
3	1	1	1	0	1	1	0	1	3	1	1	0	0	0	2	1	0
3	1	1	1	0	1	2	1	0	3	1	1	3	1	1	2	1	0
3	1	1	1	0	1	3	1	1	3	1	1	2	1	0	2	1	0
3	1	1	2	1	0	0	0	0	3	1	1	2	1	0	1	0	1
3	1	1	2	1	0	1	0	1	3	1	1	3	1	1	1	0	1
3	1	1	2	1	0	2	1	0	3	1	1	0	0	0	1	0	1
3	1	1	2	1	0	3	1	1	3	1	1	1	0	1	1	0	1
3	1	1	3	1	1	0	0	0	3	1	1	3	1	1	0	0	0
3	1	1	3	1	1	1	0	1	3	1	1	2	1	0	0	0	0
3	1	1	3	1	1	2	1	0	3	1	1	1	0	1	0	0	0
3	1	1	3	1	1	3	1	1	3	1	1	0	0	0	0	0	0

VIII. If A = 0, B = 1 and C = 3, then the output of S_{10} will be both (perpendicular and straight) polarized, and the output of $S_{14}$is straight polarized. So the output, Q, will be both (straight and perpendicular) polarized (i.e., Q = 3). The output of S_{28} will be straight polarized. So the output, R, will be straight polarized (i.e., R = 2).

IX. When A = C = 0 but B = 2(i.e ., $b_j = 1$, $b_i = 0$), then there will be no light at the output of S_6, S_{10}, S_{14} but the output of S_{20} will be horizontally

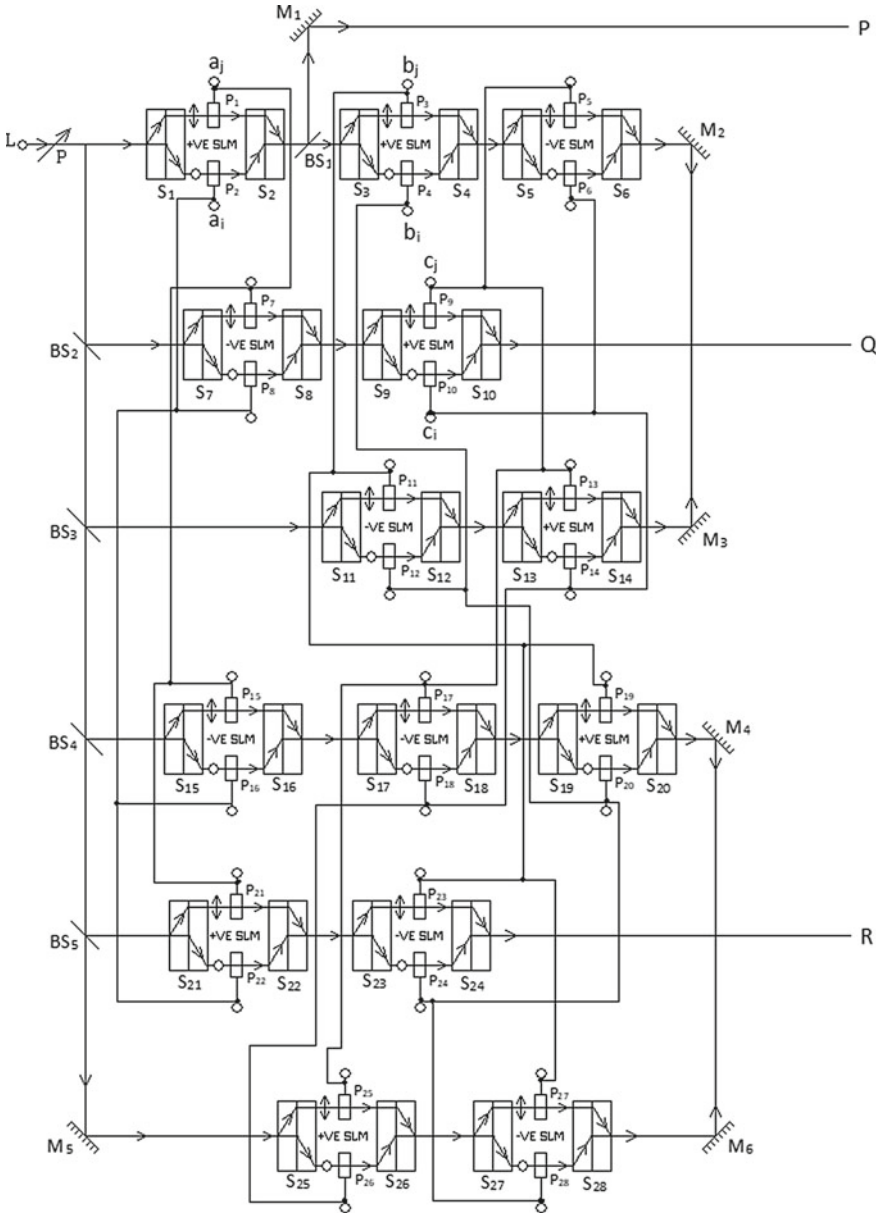

Fig. 4 Circuit diagram of New proposed Gate

polarized. So the output, Q, will be zero (i.e., Q = 0) but the output, R, will be horizontally polarized (i.e., R = 2).

X. If A = 0, B = 2 and C = 1, then as a result, the output of S_{10} and S_{14} has been vertically polarized and output, Q, has been vertically polarized (i.e., Q = 1). But the output of S_{20} has been horizontally polarized and the output of S_{28} is vertically polarized simultaneously and output, R, has been vertically and horizontally polarized (i.e., R = 3).

XI. If A = 0, B = 2 and C = 2, then the output of the S_{10} and S_{14} has been horizontal polarized. As a result, the output Q is horizontally polarized (i.e., Q = 2). For this reason, there is no light at the output of S_{20}, S_{24} and S_{28}. The output of R is zero (i.e., R = 0).

XII. If A = 0, B = 2 and C = 3, then the output of S_{14} and S_{10} is both vertically and horizontally polarized. So the output Q is both horizontally and vertically polarized (i.e., Q = 3). The Output of R is vertical polarized (i.e., R = 1).

Thus, the process will go on and the symmetrical results will be achieved for 64 steps of the new proposed gate.

6 Simulations and Results

Simulation is performed under Mathcad-7 and outputs are shown in Fig. 5 taking the different parameter values same as used in Chapter 2. Other constraints set in this experiment are the power of the input signals is taken as A = 1.13 dBm, B = 2.26 dBm and C = 1.13 dBm. In these experiments, 50:50 beam splitters were used.

The perpendicular orbit shown in Fig. 5 alludes to power in dBm, while straight orbit performs time scale in ps. The timing instances for the occurrence of the bit pattern are at 0, 5, 10, 15, 20, 25, 30 and 35 ps. In Fig. 5, the upper three sets of waveforms indicate the input bit sequences, 00001111, 00110011 and 01010101 for the input parameters of A, B and C, respectively.

7 Conclusion

This paper deals with the design of an optical quadruple Peres Gate circuit based on SLM and Savart Plate. The developed theoretical models are very much useful for the optical reversible logic computing system. This gate can be used to perform different logical and arithmetic operations in the reversible domain. This paper has presented and explored the quadruple logic system in four-state implementation which can process more information at a time. In the future, this gate can be used for the realization of various Boolean expressions in the form of system design, implementations and arithmetic operations of digital circuits.

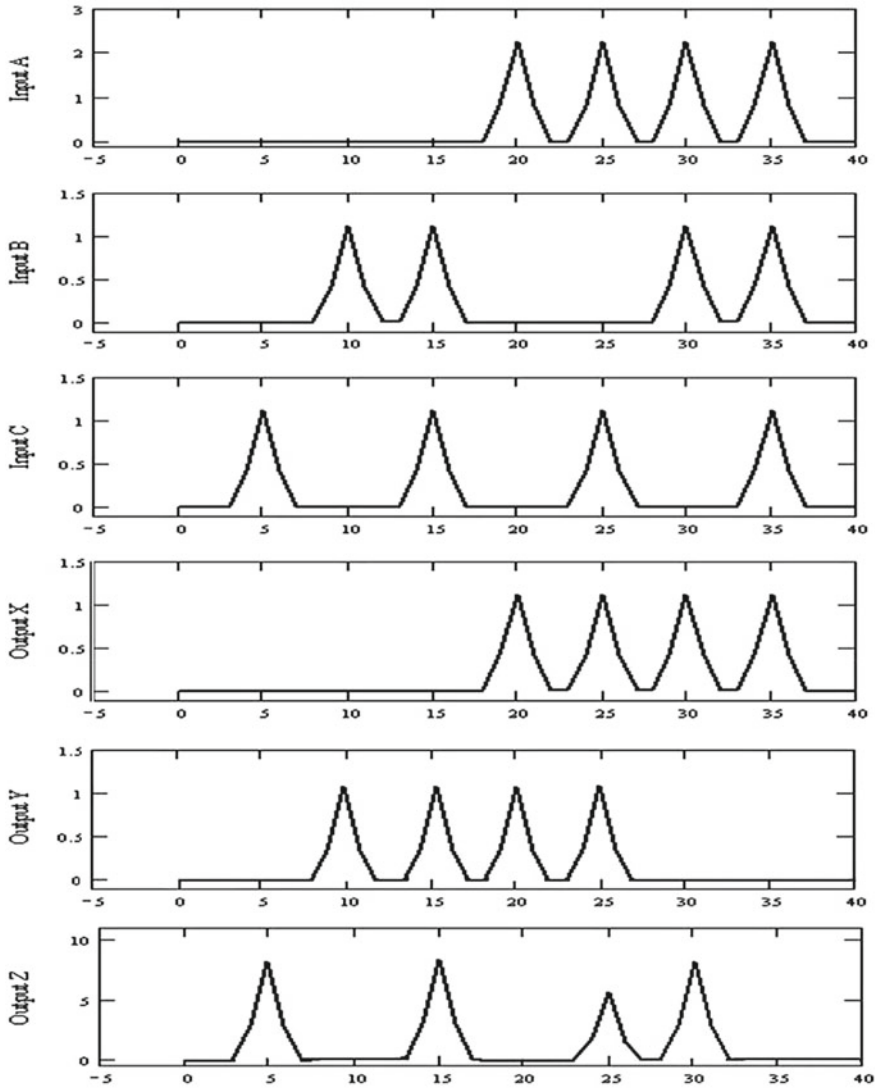

Fig. 5 Simulation result of Fig. 4: [x-axis: Time (ps) and y-axis: Power (dBm)]

References

1. E.V. Dubrova, *Multiple-Valued Logic in VLSI Design, Electronic System Design.* (Royal Institute of Technology, Sweden)
2. S. Liu, C. Li, J. Wu, Y. Liu, Optoelectronic multiple-valued logic implementation. Optics Lett. **14**(14), 713–715 (1989)
3. P. Ghosh, S. Mukhopadhyay, Implementation of tristate logic based all optical flip-flop with nonlinear material. Chin. Opt. Lett. **3**(8), 478–479 (2005)

4. T. Chattopadhyay, G.K. Maity, J.N. Roy, Designing of all-optical Tri-state Logic system withthehelpofopticalnonlinearmaterial. J. Nonlinear Optical Phys. Mater. World Sci. **17**(3), 315–328 (2008)
5. K.S.V. Patel, K.S. Gurumurthy, Arithmetic operation in multi valued logic. Int. J. VLSI Design Commun. Syst. (VLSICS) **1**(1) (2010)
6. A.W. Lohmann, Polarization and opticallogic. Appl. Opt. **25**, pp. 1594–1597 (1986)
7. T. Chattopadhyaya, J.N. Roy, All-optical conversion scheme: Binary to quaternary and quaternary to binary number. Optics Laser Technol **41**, 289–294 (2009)
8. A .Avizienis, Signed-digit number representation for fast parallel arithmetic. IRE Trans. Electron. Comp. EC-10, pp. 389–400 (1961)
9. B.L.Drake, R.P.Bocker,M.E.Lasher, R.H.Patterson, W.J.Miceli, Photonic computing using the modified-signed-digit number representation. Opt. Eng. **25**, 38–43 (1986)
10. R.P. Bocker, B.L. Drake, M.E. Lasher, T.B. Henderson, Modified signed-digit addition and subtraction using optical symbolic substitution. Appl. Opt. **25**(15), 2456–2457 (1986)
11. A.K. Cherri, M.A. Karim, Modified signed digit arithmetic using an efficient symbolic substitution. Appl. Opt. **27**(18), 3824–3827 (1988)
12. A.K. Ghosh, P.P. Choudhury, A. Basuray, Modified Trinary Optical Logic Gates and their Applications in Optical Computation, Innovations and Advanced Techniques in Systems, Computing Sciences and Software (Springer, 2008) pp. 87–92