Two-Stage Folded Resistive String 12-Bit Digital to Analog Converter Using 22-nm FINFET

G. Vasudeva and B. V. Uma

Abstract Data converters play an important role in interfacing digital section with the analog section. During the conversion, there should be minimum loss of information and less propagation delay. FINFETs are devices that operate faster with high current density compared with CMOS circuits. In this work, operational transconductance amplifier (OTA)-based 12-bit digital to analog converter is designed and implemented demonstrating advantageous in terms of DAC specifications. The essential building block in most communication and control system is data converters, including analog to digital converter (ADC) and digital to analog converter (DAC). In this work, a new architecture for digital to analog (DAC) is proposed, designed, and evaluated for its performance. The 12-bit DAC is designed using two stages of 6-bit DAC. Each of the 6-bit DAC comprises of two-step voltage divider-type DAC and folded resistive string network. Device mismatches and area optimization are achieved by using folded resistive string approach, and two-stage DAC improves resolution with coarse and fine voltage generation logic from the two-step voltage divider method. Schematic capture is carried out using Cadence tool. From the simulation results, it is observed that the proposed DAC has a maximum operating bandwidth of 100 MHz, and the gain at 3 dB is 41.86 dB. The power dissipation of proposed DAC is 4.33 mW and, hence, suitable for high speed ADC application. The INL and DNL of the DAC design have been calculated as + 0.034 to −0.001 V and + 0.06 to −0.05 V.

Keywords OTA · High speed · Resistive string folded structure · High resolution · FINFET · Wide bandwidth · Low-power circuits

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1 Introduction

Digital to analog converters (DAC) are one of the primary building blocks of analog to digital converters (ADC). There are several types of DAC architectures such as R-2R, binary weighted, current steering, and resistor string of which resistor string DAC is one of the simple DAC architectures that is used for high-speed data conversion. An N-bit DAC converts N-bit data into analog voltage and requires 2^N taps of resistive ladder. The 2^N number of resistors is connected in series between VDD and VSS, and at every node of the resistor, a switch is used to tap the voltage across the resistor. As the N-bit increases the number of resistors required are 2^N and hence occupies large area. To address the area requirement several other DAC architectures are designed. Resistor string DACs are used as reference voltage in ADCs and in circuits that require rail-to-rail output voltage generations. Kim et al. [1] have presented a 12-bit D/A based on current steering logic, designed using 14-nm FINFET CMOS technology for 4G applications. The spurious tones that arise in the current source mismatch in FINFET are addressed using switching-order shuffling and dynamic element matching. A 6-bit thermometric coding and 6-bit binary coding along with bit segmentations methods are adopted in DAC design. The power consumption of the D/A is limited to 6 mW, and SFDR is 80 dBc. Current steering DAC has limitations of occupying more layout area and is sensitive to mismatches in device properties. With technology scaling, these limitations have not been addressed and have further escalated in nanometer technology.

Murmann et al. [2] have presented FINFET technology-based high-speed DAC for mm-wave applications. Charge redistribution logic is used for design of DAC structure with parallel array logic. The limitations of current steering structure such as pulse timing, level signal mismatches, matching impedance, and power generation are addressed using time-interleaved switched capacitors with operating speed of 120 Gsps. Ting et al. [3] have presented design of segmented resistive string DAC for generation of reference signal or stimulus for ADC. Capacitive loading is reduced using folded string ladder network, and sub-resistor strings are used to reduce area of DAC structure. Aspokeh et al. [4] have presented a 5-bit resistive string DAC structure using capacitive logic which reduces area and power dissipation in 13-bit ADC. Kommangunta et al. [5] have presented a low-power area optimized resistive string DAC operating at 500 ksps, and the design results in reduction in resistor area by 28%, and OPAMP-based buffer is used to minimize offset errors. INL and DNL of 0.024 LSB and 0.004 LSB are achieved, respectively, with power dissipation limited to 65.23 μW. Mahadavi et al. [6] have proposed the 12-bit DAC design with resistive string logic and merged capacitor technique. It is suitable for high speed and high-resolution applications with 800 Msps and power dissipation limited to 1.37 mW. Yenuchenko et al. [7] have developed a 10-bit DAC with identical weighting elements and switches which uses a unified implementation based on transmission gate cells. It is demonstrated to operate at 1.8 V supply voltage with reduced number of switches. Debashis [8] in his thesis has presented an 8-bit DAC which is realized using segmented 3-bit DAC and 5-bit DAC, and the output of the

DACs is processed by the capacitive charge sharing DAC to generate differential input to SAR ADC. Variations in resistor mismatches would be detected for the various floorplans in the arrangement. The INL and DNL curves are used to calculate the fraction of systematic and random mismatches. The causes of variances in these incompatibilities are determined depending on the varied floorplans employed during the layout. Yang et al. [9] have presented a 12-bit CMOS dual-ladder resistor string which saves a considerable chip area. The D/A converter with the power supply of $\pm$ 5 V which adopts a self-adjusted reference circuit to provide differential reference voltages for obtaining better accuracy and symmetry. The results show the INL and DNL which are less than 2 LSB and 0.25 LSB. AB-Aziz et al. [10] present a paper on 12-bit pseudo-differential current source resistor strings hybrid DAC. They discuss a hybrid DAC architecture that combines the concepts of binary weighted resistor DAC and the thermometer coding DAC. This hybrid architecture gives a better INL of 0.375 LSB and DNL of 0.25 LSB, respectively. Huang et al. [11] present a compact 8-bit two-stage DAC with two voltage selector and an optimized area efficient 10-bit DAC with one voltage selector for AMOLED column driver ICs with CMOS technology. The measured DNL is 0.44LSB and INL is 0.68LSB for the 8-bit DAC, and measured DNL is 0.126 LSB and INL is 0.256 LSB for the 10-bit DAC. The proposed two-stage DAC architecture in this paper keeps the size of the 10-bit data driver even smaller than that of the conventional 8-bit driver. Lu et al. [12] introduce a 10-bit RFR-DAC for high color-depth LCD driver ICs and suggest a unique RFR-DAC architecture with a 10-bit resolution for liquid crystal display applications in their work. The proposed RFR-DAC combines a 6-bit RDAC with a 4-bit FR-DAC to provide a novel two-voltage selection and one-voltage selection methods that eliminate the requirement for unity gain buffers to isolate parallel-coupled resistor strings. The technology utilized is CMOS, with the worst DNL being 0.11 LSB and INL being 0.92 LSB using a two-voltage selection method and DNL being 1.37 LSB and INL being 1.45 LSB via a one-voltage selection strategy.

Use of resistors in DAC circuit leads to errors or performance degradation due to mismatches, and due to voltage drop, additional buffers are required to drive the output nodes. Thermometric coding in DAC requires large number of switches that leads to glitches and reduces DNL. Capacitive DAC offers device matching and is power-efficient; however, the number of capacitors exponentially increases with increase in N-bits. C-2C DAC is another structure to achieve high speed and good resolution. The disadvantage in the case of binary weighted resistor DAC as it requires large range of resistors with necessary high precision for low resistors. Also requires low switch resistances in transistors and can be expensive. Hence, resolution is limited to 8-bit size. Power dissipation of binary weighted circuit is extremely high. Current steering DACs are a more common integrated DAC compared to resistor DACs. The drawback of R-2R DAC is it requires two sets of resistors with precision resistance value (R and 2R). For a R-2R-based 12bit DAC, we require 12 switches minimum 6(R) and 6 (2R) resistors and 2 (2R) resistors. At any given point of time, more than one switch will be ON equivalent to the corresponding binary number to generate the equivalent analog voltage. This process increases delay and nonlinearity issues affecting INL and DNL, and suitable matching is not carried out. Based on

various architectures reported in literature, the most successful DAC architecture is the hybrid DAC that combines two different DAC structures or uses segmented principles. In this paper, a novel method for DAC architecture is designed using 22-nm FINFET technology. For high-speed applications and resolution more than 8 bit, resistive string DAC is recommended, because of its reduced delay (only one switch will be on at any point of time) and single value of R. There is uniformity in the circuit element minimizing reliability issues. The folded resistive string is more optimum in terms of area during layout implementation and avoids all device mismatching issues. The two-step voltage divider circuit generates Vout if coarse and fine resolutions including conversion accuracy. The 12-bit DAC is designed using two stages of 6-bit DAC. Each of the 6-bit DAC comprises of two-step voltage divider-type DAC and folded resistive string network.

The paper is organized as follows. Section 1 presents introduction to DAC. Section 2 highlights fundamentals of FINFETs and its device parameters, small-signal model. Section 3 discusses OTA concepts and FINFET-based OTA schematic for DAC. Section 4 discusses voltage divider folded resistive string DAC. Section 5 discusses about two-stage voltage 12-bit folded resistive string DAC. Results and discussions is presented in Sect. 6, and conclusion is presented in Sect. 7.

2 FINFET

FINFET-based analog and digital circuit design is advantages as the FINFET devices support high drain current, operates at low switching voltages generating low leakage current leading to low-power applications. Hu et al. [13] introduced FINFET devices and have demonstrated their advantages over MOSFETs. One of the FINFET device is the double gate-FET (DG-FET) that uses two controlling gates for current flow in the device [14, 15]. Figure 1 presents the generic structure of FINFET device with top gate and bottom gate that control the flow of current in the channel between the source and drain regions.

The small-signal circuit diagram for FINFET is shown in Fig. 2. The intrinsic circuit comprises of parasitic capacitances C_{gd}, C_{gs}, and C_{ds} along with the parasitic resistance R_{gd}, R_{gs}, R_{ds}, and R_{sub}. The capacitances C_{pg} and C_{pd} are considered at

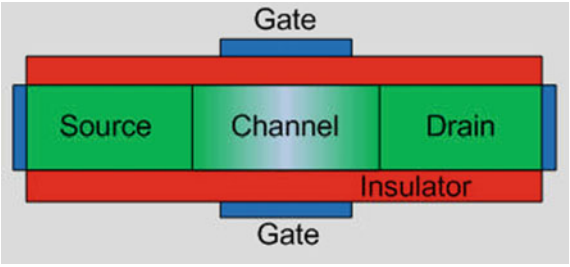

Fig. 1 Structure of FINFET (double gate) [14]

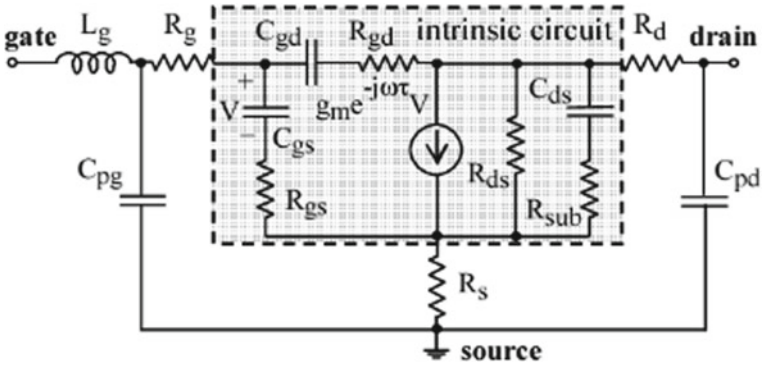

Fig. 2 Small-signal equivalent circuit for FINFET [16]

low frequencies with pinch-off condition. The parameters L_g, R_g, R_s, and R_d are computed considering V_{gs} above pinch-off.

The small-signal model and model file of FINFET considered from predictive technology model (PTM) are considered for design of ADC. The device parameters are presented in Table 1. The source doping and drain doping concentration based on Gaussian doping are considered at 1e + 19/cm^{-3}, the dielectric constant of channel is 11.7, and the dielectric constant of insulator is 3.9. The bandgap and affinity of channel material are considered at 1.12 eV and 4.05 eV with gate contact work function of 4.6 eV. Mobility of electrons and saturation velocity are considered at 1400 cm^2/Vs and 1.07e + 07 cm/s. Considering these structural and electrical properties for FINFET, the device model is simulated for its input and output characteristics.

Figures 3a and b present the input and output characteristics for the FINFET considered with the structural parameters as in Table 1. The parameters chosen in this work are compared with the parameters that have been considered in [17]. The technology selected in this work is 22 nm. The input is obtained by setting the drain

Table 1 FINFET device parameters

Parameter	Value (proposed work)	Value [17]
Channel length	22 nm	32 nm
Oxide thickness 1	2.5 nm	1.6 nm
Oxide thickness 2	2.5 nm	1.6 nm
Gate length	22 nm	–
Source/drain extension length	50 nm	32 nm
Gate to source/drain overlap	2 nm	–
Work function	4.6 eV	4.5 eV
Source/drain doping	1×10^{19} cm^{-3}	2×10^{20} cm^{-3}

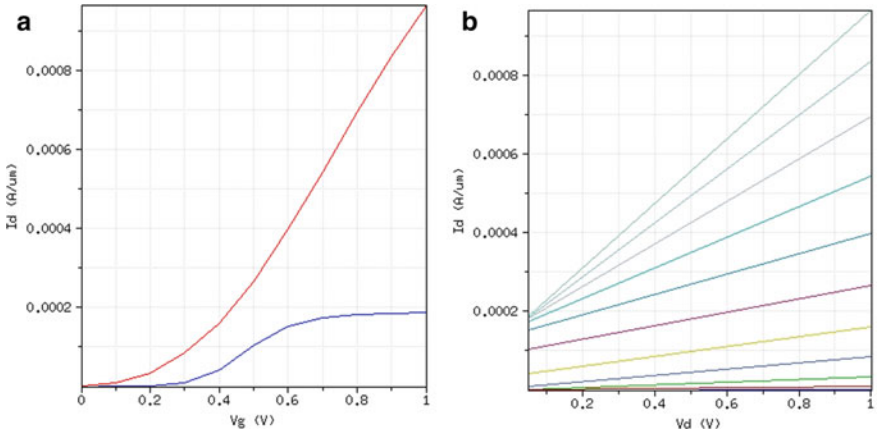

Fig. 3 **a** Input characteristics of FINFET. **b** Output characteristics of FINFET

voltage at 0.5 and 1 V. The output characteristic is obtained by setting the gate voltage between 0 to 1 V with incremental step of 0.1 V.

Figures 3a and b represent the V-I characteristics of FINFET considered at 22-nm technology with high-K dielectric. From the I_{ds}–V_d characteristics in the figure, it is observed that a small change in gate voltage doubles the I_{ds} current. Higher current-driving capability of FINFET leads to high-frequency operation. Power dissipation and transfer characteristics of inverter device are evaluated. The maximum power dissipation is observed to be less than 800nW, and transition width is less than 0.12 V. The leakage current during positive switching and negative switching current is observed to be less than 9 μA. Considering the advantages of FINFET over MOSFET, analog and digital sub-systems are designed, and these blocks are integrated into DAC logic.

3 OTA-Based Voltage Follower

OTA is transconductance device in which the input voltage controls the output current flow. The transconductance of the device gm makes the OTA a voltage controlled current source. The advantage in OTA is the transconductance parameter is controlled by the amplifier bias current. The output current is a function of the difference between the applied voltage, and the current at the output is converted to voltage by connecting a resistive load. The OTA-based circuits do not require negative feedback; the transconductance is one of the design parameters of OTA-based circuit designs. In this work, DAC circuit is designed considering advantages of OTA. OTA-based voltage follower is one of the main circuit used in DAC. High immunity toward short channel effects such as drain-induced barrier lowering (DIBL) and enhanced subthreshold swing FINFET device is preferred for DAC circuit designs. Low power

dissipation and high performance are achieved by use of FINFET in place of CMOS circuits. Design of FINFET-based OTA has advantages such as high gain, low power consumption, wide unity gain bandwidth, better slew rate and CMRR compared with CMOS-based OTA. The primary building blocks of OTA are presented in Fig. 4. The input stage performs level shifting, second stage is the folded cascode stage with feedback, and the last stage is the output stage.

The simple OTA circuit is presented in Fig. 5 that is realized using eleven transistors. The transistors $F1$ and $F2$ are the differential pair and form the transconductance cell that converts the input voltage V^{+}in and V^{-}in (differential input voltages) to current [18]. The differential current output (I_{out}) of the differential pair is converted to single-ended current at the output by using the current mirrors $F3$ to $F8$, $F10$, and $F11$. $F9$ transistor is used to bias the differential pair and is used as current sink circuit. The cut-off frequency of the OTA is decided by setting the appropriate bias current and the load capacitance of the OTA. The transconductance gain g_{m} of the OTA is controlled by setting the current that enters the transistor $F9$, and the gate voltage V_{b} is appropriately set. Design methodology based on $g_{\text{m}}/I_{\text{D}}$ method is the most popular approach [19] that identifies the transistor geometries based on data sheets

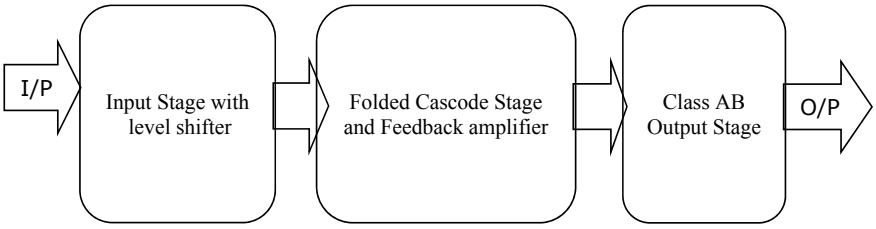

Fig. 4 OTA block diagram

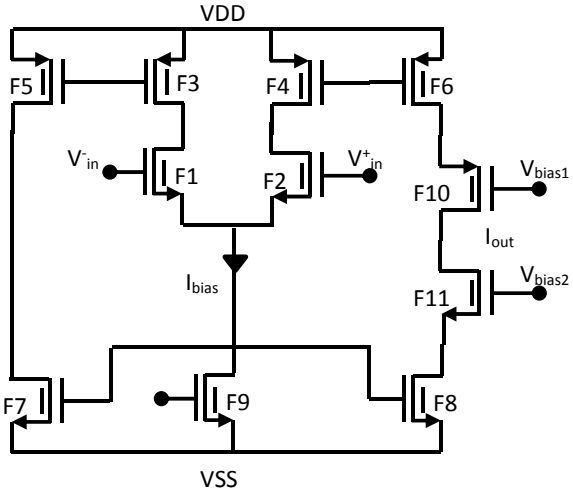

Fig. 5 FINFET-based OTA circuit [20]

and simulation results. In this method, the design of OTA circuits based on datasheet and several design variables that were required for the design were assumed without clear rules. The design specifications meeting input range, common mode rejection, and noise parameters were not considered in this approach. Even, the channel length variations regarding g_m/I_D were not considered in the design process.

Figure 5 presents the circuit schematic of OTA with input stage, differential pair, and output stage including the bias circuits. Operational transconductance amplifier captured in Cadence environment consists of three sub-blocks such as differential amplifier, gain boosting block, and common mode feedback as shown in Fig. 6. The inputs areV_1, V_2, V_3, and the outputs are V_{OM} and V_{OP}.

The N-channel FINFET and P-channel FINFET transistor sizing involved in designing OTA are shown in Table 2.

The simulation results of DC analysis and differential input of OTA are shown in Fig. 7. The DC gain is of 68 dB, but the phase margin is observed to be less than the required (13^0). The FINFET geometries are varied to achieve the desired phase margin.

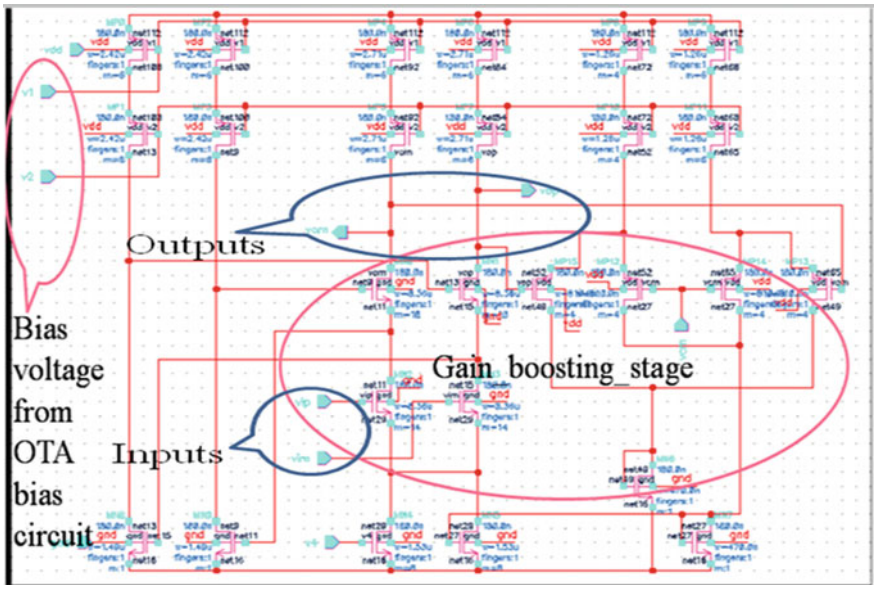

Fig. 6 Schematic diagram of FINFET-based OTA for DAC

Table 2 Transistor sizing for OTA design

Component	(W_n/L_n)nm
N-channel FINFET	$(80.3/22)$
P-channel FINFET	$(180/22)$

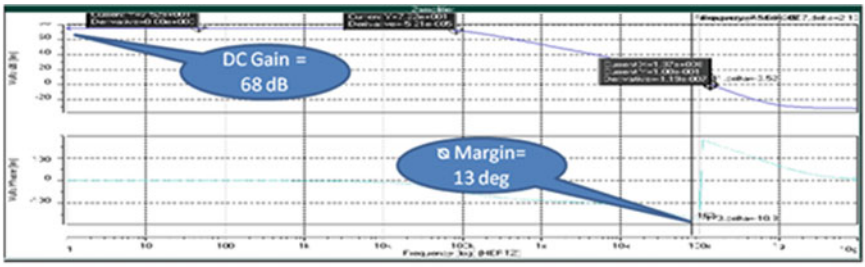

Fig. 7 DC analysis and differential input simulation of OTA

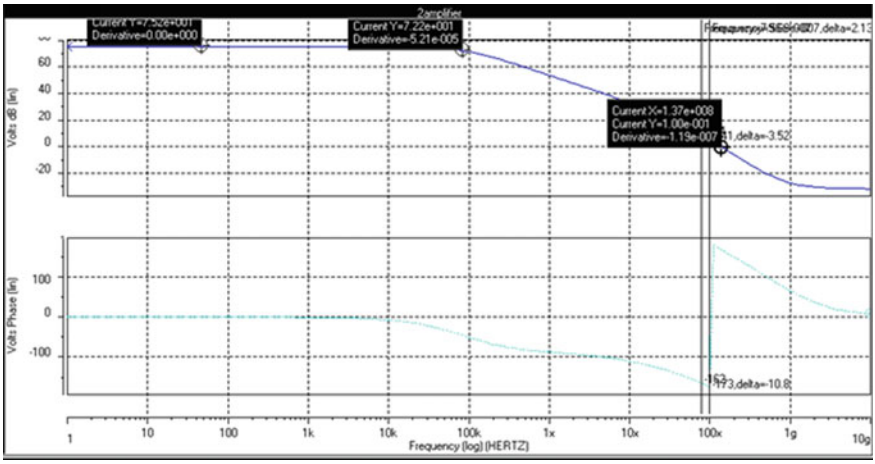

Fig. 8 Gain and phase margin analysis of improved OTA for DAC

The improved OTA design has a unity gain bandwidth (UGB) of 100 MHz, and the gain at 3 dB is 41.86 dB and phase margin of 52^0. The FINFET transistor geometries are increased by a factor of 1.2 times the designed geometries to achieve the required phase margin (Fig. 8).

4 Voltage Divider Folded Resistive String DAC

DAC input–output relation is mathematically expressed as in Eq. (1) [21]. The N-bit input data is $\{b_1, b_2, b_3, b_N\}$, b_1 is MSB and b_N is LSB, N is the data input length, and V_{ref} is the reference voltage.

$$V_{\text{OUT}} = V_{\text{ref}}\left(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}\right) \tag{1}$$

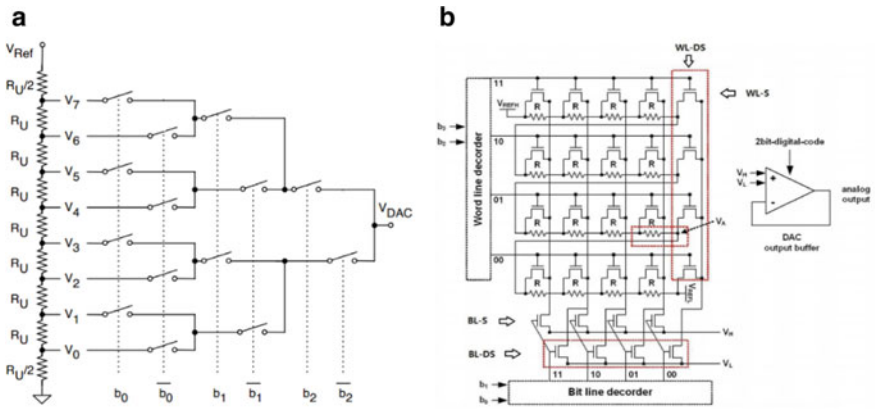

Fig. 9 **a** Resistor string DAC ladder network [22]. **b** Resistor string DAC folded network [22]

The resistor string-based digital to analog converter is shown in Fig. 9a [22]. The resistor string has 9 resistors and 14 transistor switches. The input bits b_0, b_1, and b_2 are inputs are used as control inputs to the 14 switches that allow the corresponding ladder voltage to the output. The voltage follower at the output amplifies the ladder voltages to generate the equivalent analog voltage. The number of switches led to noise due to switching which is addressed by use of folded resistor string structure. Figure 9b [22] presents the resistor string DAC designed using folded string logic. The 4-bit input is split into two groups of b_1, b_2 and b_3, b_4 that are inputs to two 2:4 decoders along the x and y directions, respectively. The output of decoders is used to control the 2D switch matrix to enable one of the node voltages to be connected to the output voltage.

The input bits b_0 and b_1 through the 2:4 decoder enable one of the vertical lines, and the corresponding bits b_2 and b_3 are used to enable one of the horizontal lines through the 2:4 decoder. The ladder voltage along the folded resistor string is directed into the voltage follower as equivalent analog output. The number of switches for a 4-bit DAC is limited to 16 in the folded resistor string DAC. The folded resistor structure is implemented using matching circuits during layout design minimizing mismatches in the device parameters. The folded resistor string DAC is area-efficient but introduces propagation delay and limited resolution. To overcome the limitations of folded resistive string DAC, in this work two-stage resistor string voltage divider type D/A Converter is designed as shown in Fig. 10.

In the first stage, the resistive ladder network and two voltage follower circuits are used. The decoder output controls the switches ON and OFF. In the first stage, two switches are switched on simultaneously between every resistor in the ladder. The second stage is used to generate fine voltage levels between the two voltages references generated from the first stage. In this work, the advantages of voltage divider type and folded resistive string DAC are combined, and a new DAC architecture is designed. Detailed discussion on proposed DAC structure is presented in next section.

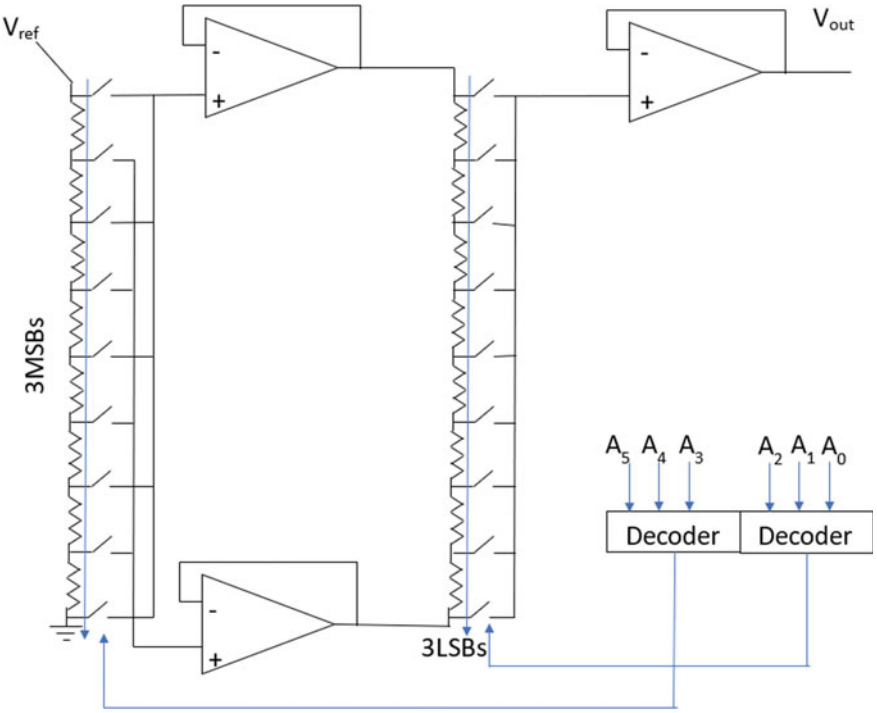

Fig. 10 Two-stage resistor string voltage divider type D/A converter

5 Two-Stage Voltage 12-Bit Folded Resistive String DAC

The proposed 12-bit DAC block diagram is shown in Fig. 11. The DAC structure is split into two groups of 6 bits. The first stage generates V_{out1} corresponding to 6

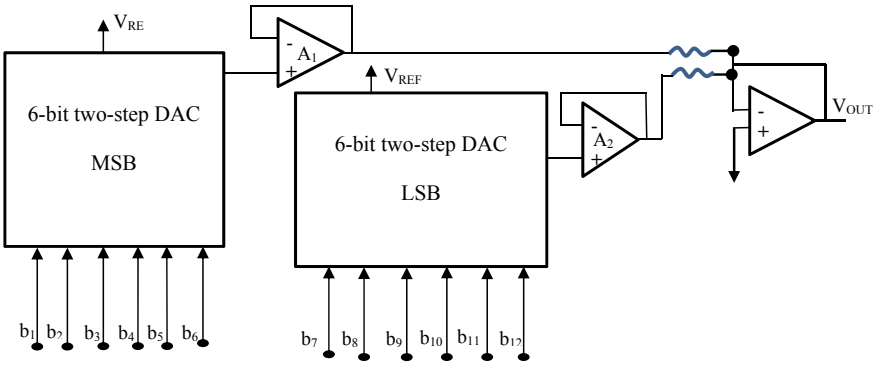

Fig. 11 Proposed 12-bit DAC structure

MSB, and the second stage generates V_{out2} for 6 LSB. The output of two-stage DAC V_{out1} and V_{out2} is accumulated in the adder circuit to generate the final analog output V_{OUT}.

Considering Eq. (1), for $N = 12$ bit, the DAC output is expressed as in Eq. (2),

$$V_{OUT} = V_{ref}\left(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_{12} 2^{-12}\right) \tag{2}$$

Equation (2) is split into two sections of 6 bit each and is presented as in Eq. (3),

$$V_{OUT} = V_{ref}\left(b_1 2^{-1} + b_2 2^{-2} + \ldots . b_6 2^{-6}\right) + V_{ref}\left(b_7 2^{-7} + b_8 2^{-8} + \ldots . b_{12} 2^{-12}\right) \tag{3}$$

Rewriting Eq. (3) by combining the data bits into two groups of 6 bit, Eq. (4) is obtained. The second term in Eq. (3) is reduced by identifying 2^{-6} as common term. The second term is reduced to binary power of 2^{-1} to 2^{-6} as the first term. The V_{ref} in second term is scaled by 2^{-6}.

$$V_{OUT} = V_{ref}\left(b_1 2^{-1} + b_2 2^{-2} + \ldots . b_6 2^{-6}\right) + V_{ref}\, 2^{-6}\left(b_7 2^{-1} + b_8 2^{-2} + \ldots . b_{12} 2^{-6}\right) \tag{4}$$

The first term in Eq. (4) is realized using first-stage DAC with input bits b_1 to b_6, and the second term is realized using second-stage DAC with inputs b_7 to b_{12} and $V_{ref} = V_{ref}/2^6$. The expression in Eq. (4) is simplified and is presented in Eq. (5).

$$V_{OUT} = V_{out1} + V_{out2} \tag{5}$$

where $V_{out1} = V_{ref}\ (b_1\ 2^{-1} + b_2\ 2^{-2} + \ldots . b_6 2^{-6})$, $V_{out2} = V_{ref2}\ (b_7\ 2^{-1} + b_8 2^{-2} + \ldots . b_{12} 2^{-6})$, and $V_{ref2} = V_{ref}/2^6$. The variation between the first stage and second-stage reference voltages is 83%, which will impact the second-stage DAC performance as the V_{ref} is at a lower value. To address these limitations, the second-stage DAC is set with the same reference voltage as in first stage. The output of first stage V_{out1} is amplified by 2^6 and is accumulated with the second-stage DAC output to generate the final output as represented in Eq. (6).

$$V_{OUT} = \mathrm{A}V_{out1} + V_{out2} \tag{6}$$

where A is the gain introduced into the first-stage DAC output and is set to 64. The output of first-stage DAC is amplified by inverting amplifier (not shown in Fig. 11) with gain of 64. The advantages of two-stage DAC proposed are that the number of resistors and the transistors switches is 64/68 of the generic resistive string DAC. The limitations of two-stage DAC are that it requires three voltage followers or buffers. The two buffers between second stage and first stage introduce delay, and appropriate circuit design methodology is required to be considered to overcome these challenges. In this work, to improve the processing speed and further reduce

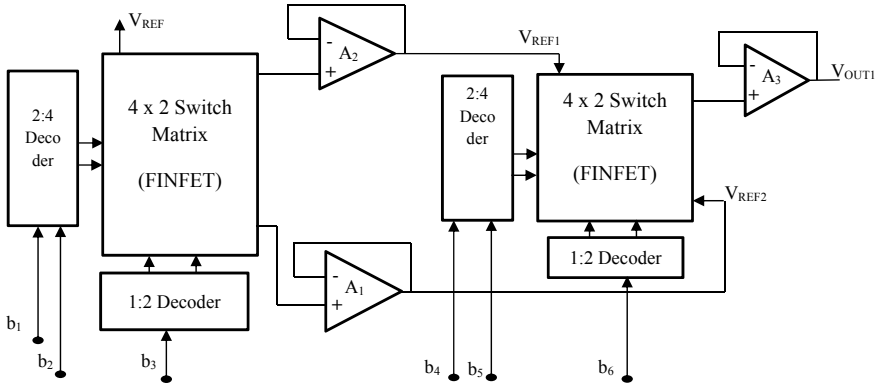

Fig. 12 Proposed 6-bit voltage divider resistive string DAC

the performance degradation in DAC circuit, a new architecture is proposed. The proposed DAC circuit topology is shown in Fig. 12. The 6-bit DAC is realized using voltage divider-type DAC shown in Fig. 10. The 6-bit DAC is split into two 3-bit DACs as shown in Fig. 10. The first stage of 6-bit DAC comprises of 2:4 decoder, 1:2 decoder, 4 × 2 switch matrix, folded resistive string, and two amplifiers A1 and A2. The second stage of 6-bit DAC comprises of all the building blocks of first stage, but there is only one amplifier. The two-stage DAC provides high resolution and low power consumption due to two-stage operation and isolation between switches and output node, respectively. The presence of two amplifiers and resistors in two stages introduces voltage offset and mismatches leading to performance degradation.

The novelty in this proposed work is the realization of the resistive ladder network. The resistive ladder or resistive string is realized using folded string technique to minimize device mismatches and area. The proposed DAC circuit is realized using folded string resistive structure shown in Fig. 13. The voltage offset and delay in the amplifier circuit are addressed by the design of voltage follower using OTA circuit.

The proposed folded string two-stage voltage divider-type DAC comprises of two folded string resistive network with eight resistors in each string and nine transistors connected across. The line 2:4 decoder generates the control signal for the switches based on two input bits, and the word 1:2 decoder generates the word line from one bit input. The two amplifiers $A1$ and $A2$ are used to accumulate the node voltages and generate V_{H} and V_{L} as the two reference voltages for Stage 2. The second-stage folded string two-stage voltage-type structures comprise of 2 × 4 resistor string and eight switches connected across the resistor. The 2:4 decoder along the horizontal axis and the 1:2 decoder along the vertical axis enable the corresponding resistive node voltage that exits between two references V_{H} and V_{L}. The node voltage is amplified by the voltage follower circuit $A3$ to generate the DAC voltage. The proposed circuit requires two 2:4 decoders and 1:2 decoders, two folded string resistive network, three amplifiers or voltage followers, and 21 switches.

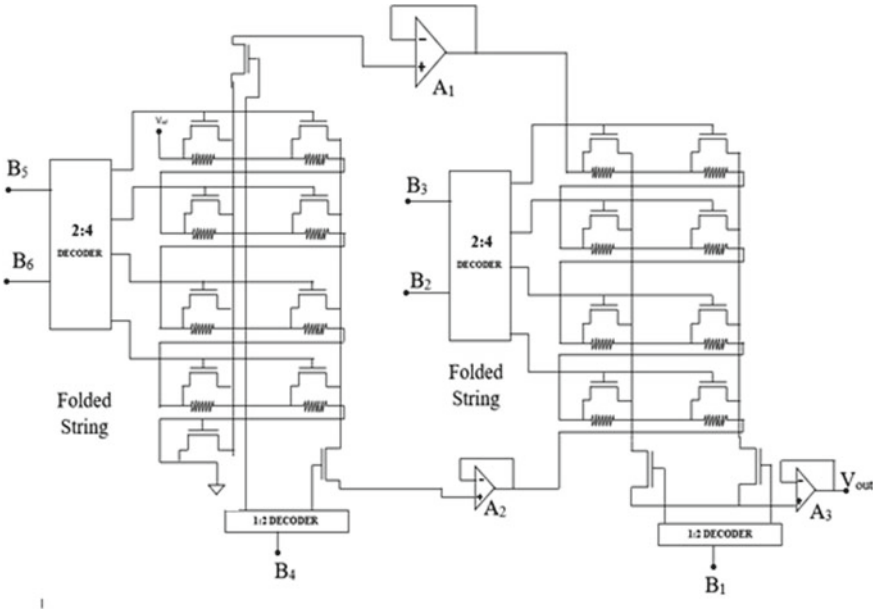

Fig. 13 Internal structure of proposed two-stage 6-bit DAC

The circuit schematic for 12-bit DAC is modeled hierarchically by first designing the 6-bit DAC and combining two 6-bit DAC into top-level module. The 22-nm FINFET model is set and modeled in Cadence environment. Prior to modeling in Cadence environment, the proposed schematic for 12-bit DAC is modeled in SPICE. The performance of the modeled DAC is evaluated considering different metrics and discussed in detail in next section.

6 Results and Discussion

Figure 14 shows the schematic diagram of transmission gated resistor string DAC for 6 bit, where it consists of 64 resistors for 6 bits. Based on the switches *B*6, *B*5, *B*4, *B*3, *B*2, *B*1, the divided voltage has been compared with the analog sampled input by comparator. The circuit presents the digital to analog converter for 6 bit with folded resistive ladder where the reference voltage 1.8 V has been divided as equal to 1 LSB value.

Figure 15 presents the simulation results of 6-bit DAC. Sixty-four combinations of 6-bit input are considered in verifying DAC functionality. Figure 15 shows the simulation result of 6-bit transmission gated digital to analog converter with its input digital bits such as *B*6—MSB, *B*5, *B*4, *B*3, *B*2, *B*1—LSB and its output shown as DAC output. Since, it is 6-bit DAC, the step output of the DAC is equal to 64 steps.

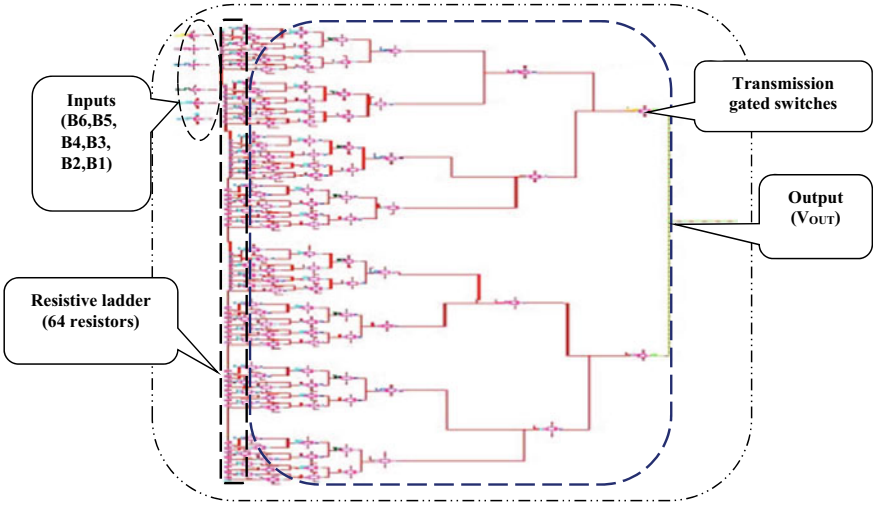

Fig. 14 Proposed two-stage folded resistor string 6-bit DAC schematic

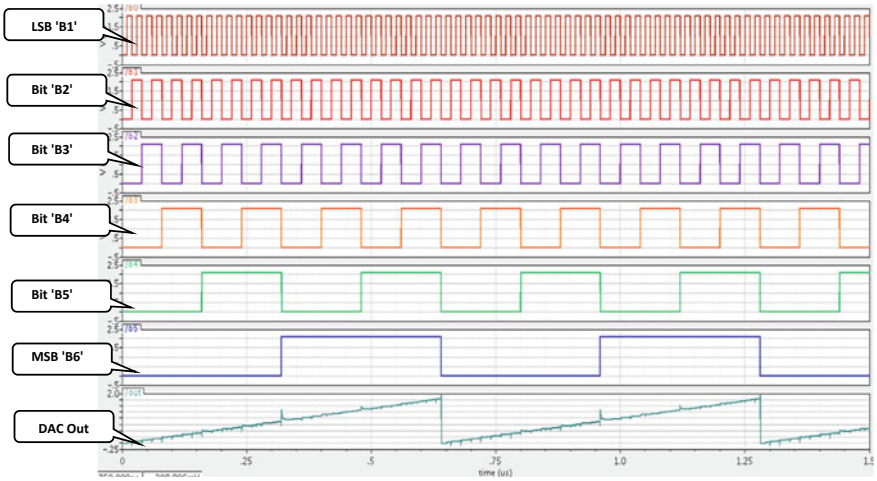

Fig. 15 Simulation result of 6-bit DAC

Figure 16 shows the output of integral nonlinearity (INL).The integral nonlinearity value has been calculated by developing graph manually. This top-level block consists of 12-bit DAC which gives analog output with respect to the 12-bit digital input. Figure 17 shows the simulation result of 12 bit along with 12-bit digital input generating the corresponding analog output.

Table 3 shows the comparison proposed DAC performance with reference design. It is observed from the simulation results that the result of the developed has been

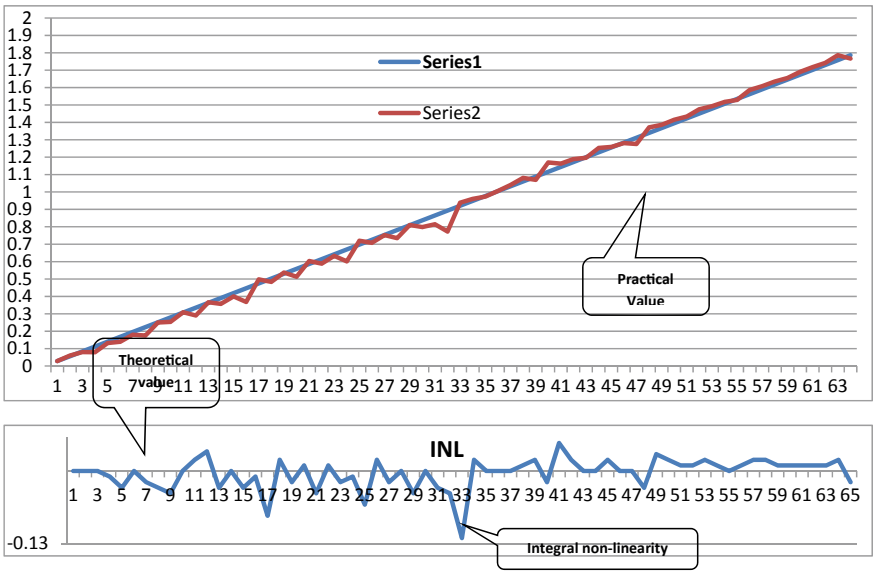

Fig. 16 Integral nonlinearity of the 6-bit DAC

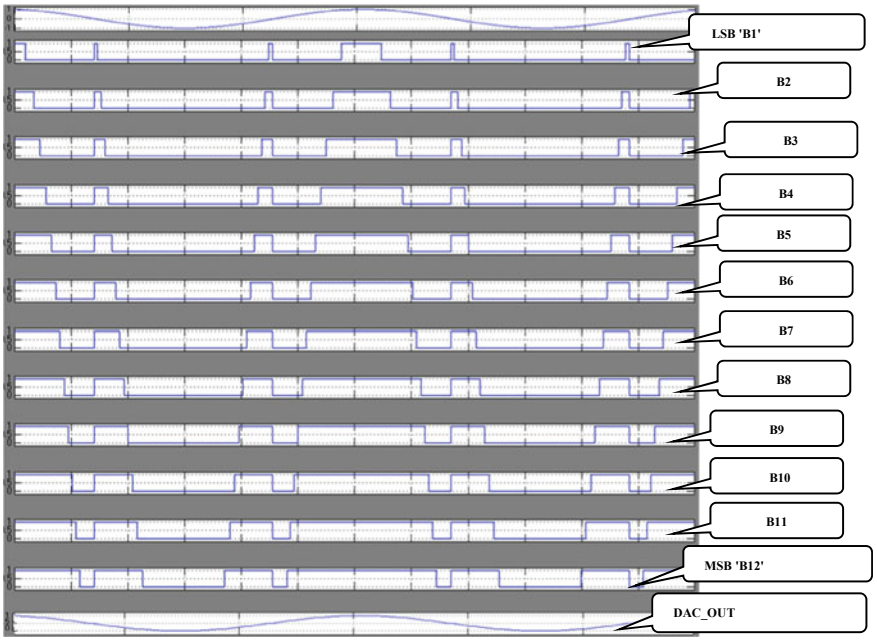

Fig. 17 Simulation results of 12-bit DAC

Table 3 Comparison of existing work and proposed DAC

Parameters	Desired specifications [23]	Obtained specifications
Resolution	12 bits	12 bits
Power supply	1.8 V	1.8 V
Technology	22 nm	22 nm
Input bandwidth	50 MHz	100 MHz
Sampling frequency	–	1 GHz
Total power dissipation	8.98 mW	4.33 mW
INL	$\leq \pm$ 0.3 V	+ 0.034 V / − 0.001 V
DNL	$\leq$ + 0.5 / −0.1 V	+ 0.06 V / − 0.05 V
Area	890 μm^2	450 μm^2

improved much better than the existing work proposed by Beaulieu [23]. The parameter in which improvement achieved is power dissipation, area, INL, and DNL. The power dissipation of designed DAC has been calculated as 4.33 mW, whereas existing work dissipates 8.98 mW. The area of the existing design has been calculated as 890 μm^2, whereas designed proposed DAC occupies 450 μm^2. Reducing the total number of resistors and design of folded resistive string circuits has contributed to low power dissipation and performance improvement in terms of circuit mismatches. Considering the power-delay product, an improvement of 75% is achieved in the proposed design as compared with reference design demonstrating the computing efficiency. Power dissipation per unit area in the proposed design is 9.63 W/m^2 which is an improvement of 4% compared with reference design.

The proposed OTA-based DAC circuit using FINFET device is designed to operate at sampling rate of up to 1 GHz. For a 12-bit DAC with input bandwidth of 100 MHz and maximum sampling frequency of 1 GHz, the power dissipation is limited to less than 4.33 mW which is an advantage for use of DAC in ADC. The INL is computed considering all possible levels of input, and it is limited to + 0.034/−0.001 V which is 100% improvement compared with desired specifications. The DNL error is also limited to less than + 0.06/−0.05 V, and an improvement of 76% is achieved compared with desired specifications. The maximum deviation in INL error is at the 33rd input data that occurs due to switching between the two folded string registers. The INL error is limited at higher input values due to both coarse and fine switching of folded string DAC circuits.

7 Conclusion

This paper presents a novel high-resolution two-stage voltage divider folded resistive string 12-bit DAC circuit designed using OTA, decoders, and switch matrix using 22-nm FINFET transistors. The advantages of two-stage DAC proposed are that the number of resistors and the transistors switches is 64/68 of the generic resistive string DAC. The two-stage DAC provides high resolution and low power consumption due to two-stage operation and isolation between switches and output node, respectively. The 6-bit MSBs are used in generating the coarse voltage, and 6-bit LSBs generate fine voltage in the second-stage DAC. The combination of first and second stage together generates high-resolution DAC output. The first-stage 6-bit DAC operates at V_{ref} to generate V_{out} voltage defining coarse conversion. The second-stage DAC divides this coarse voltage into six voltage references for data conversion defining fine resolution. The INL and DNL errors are within the set limits, and the power dissipation is less than 4.33 mW. The maximum operating bandwidth is 100 MHz with OTA gain of 41.86 dB. The limitations of two-stage DAC are that it requires three voltage followers or buffers. The presence of two amplifiers and resistors in two stages introduces voltage offset and mismatches leading to performance degradation. Further studies are carried out to overcome these limitations by design of OTA circuits that can offer minimum voltage offset and better matching circuits. The proposed DAC design is suitable for high-speed ADC (500 Mbps). The proposed DAC circuit can be used as programmable DAC and can be programmed to either work as 6-bit DAC or work as 12-bit DAC supporting high speed and high-resolution requirements, respectively.

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