Chapter 4
BTI Analysis Tool (BAT) Model Framework—Generation of Interface Traps

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4.1 Introduction

As discussed in the earlier chapters, Negative Bias Temperature Instability (NBTI) became an important reliability concern with the migration from Silicon Dioxide (SiO_2) to Silicon Oxynitride (SiON) gate insulator MOSFETs [1–7]. It continues to remain as a concern for dual layer (SiO_2 or SiON Interlayer (IL) and Hafnium Dioxide (HfO_2) High-K layer) High-K Metal Gate (HKMG) gate insulator-based bulk [8–13] and Fully Depleted Silicon On Insulator (FDSOI) [14, 15] planar MOSFETs, bulk and SOI FinFETs [15–28], as well as Gate All Around Stacked Nanosheet FETs [29–32], with either Silicon (Si) or Silicon Germanium (SiGe) channel. The key features of NBTI are summarized hereinafter (reproduced from Chap. 3, Sect. 3.1).

As described in Chap. 1, Sect. 1.3, NBTI results in gradual buildup of positive charges in a p-MOSFET gate insulator and causes threshold voltage (ΔV_T) in time under the application of a negative gate bias (V_G). ΔV_T accelerates at higher magnitude of V_G during stress ($V_G = V_{GSTR}$) and higher temperature (T), governed by the Voltage Acceleration Factor (VAF) and Arrhenius T activation energy (E_A) respectively. The parametric shift accrued during stress partially recovers after stress when the magnitude of V_G is reduced or removed ($V_G = V_{GREC}$ or 0 V), and therefore, AC stress results in lower ΔV_T than DC. The AC to DC ratio depends on the Pulse Duty Cycle (PDC) and pulse low bias (V_{GLOW}); however, it may or may not depend on the frequency (f) of the gate pulse (depends on AC stress mode). On the other hand, NBTI recovery necessitates the use of ultra-fast methods for artifact free measurements, which is discussed in Chap. 1, Sect. 1.2.

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As described in Chap. 2, the time kinetics of measured ΔV_T and related parameters, such as the power law slope (n) at longer stress time (t_{STR}), VAF, E_A, T dependence of VAF during stress and Fraction Remaining (FR) during recovery after stress (FR is defined as ΔV_T at $t = t_{REC}$ after stress to that at $t = t_{STR}$ at the end of stress) depend on different transistor processes. In modern HKMG gate insulator-based p-MOSFETs, some of the key processes that influence NBTI are Nitrogen content (N%) in the gate insulator and Germanium content (Ge%) in the channel. The magnitude of ΔV_T increases, while the associated n, VAF, E_A, T dependence of VAF and FR reduce with higher N%. On the other hand, the magnitude of ΔV_T reduces, while the associated n, VAF, E_A, T dependence of VAF and FR increase with higher Ge%. Moreover, NBTI reduces with fin length and fin width scaling in FinFETs, sheet length scaling in GAA-SNS FETs and larger spacing (SA) between the Shallow Trench Isolation (STI) and device active in FDSOI MOSFETs; however, it increases with sheet width scaling in GAA-SNS FETs.

Any practical and technologically relevant modeling framework should be able to explain the experimental features listed in Chap. 3, Sect. 3.1. The BTI Analysis Tool (BAT) framework described in this book models NBTI parametric drift using uncorrelated contributions from generated interface traps (density ΔN_{IT}) and bulk gate insulator traps (density ΔN_{OT}), and hole trapping in preexisting bulk gate insulator traps (density ΔN_{HT}). Several independent experimental evidences regarding the impact of these underlying subcomponents are demonstrated in Chap. 3. In this chapter, the Reaction Diffusion (RD) model is explained to calculate the time kinetics of ΔN_{IT}. Other subcomponents are modeled in Chaps. 5 and 6.

4.2 BTI Analysis Tool (BAT) Framework

Figure 4.1 illustrates the BAT framework used throughout this book and the underlying subcomponents of NBTI degradation [12]. The time kinetics of measured ΔV_T is due to uncorrelated contributions from generated interface (ΔV_{IT}) and bulk gate

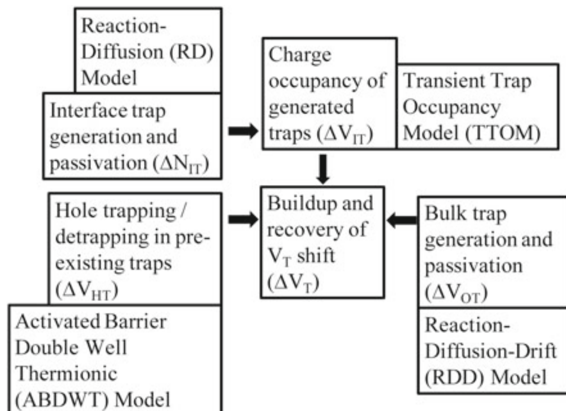

Fig. 4.1 Schematic of the BTI Analysis Tool (BAT) framework used in this book to model measured ΔV_T kinetics during and after DC and AC NBTI stress

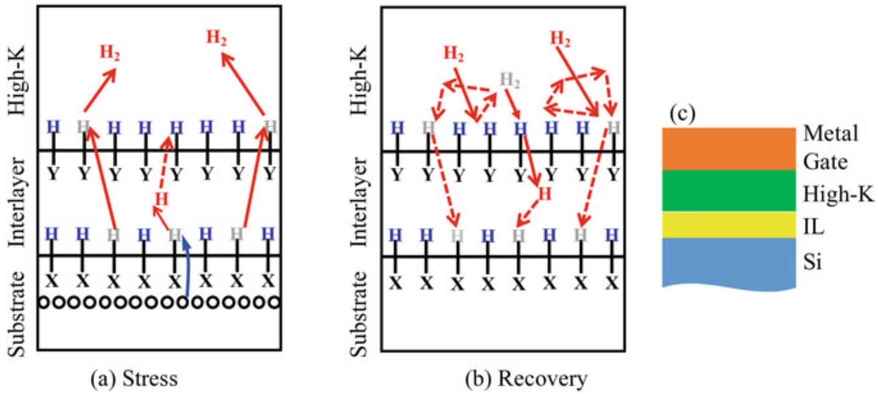

Fig. 4.2 Schematic of the Reaction Diffusion (RD) model with defect-assisted dimerization and reverse process to calculate the time kinetics of trap generation and passivation respectively (a) during and (b) after NBTI stress, example is shown for (c) HKMG gate insulator. The RD model equations are described in Sect. 4.3

insulator (ΔV_{OT}) traps, and hole trapping in preexisting bulk gate insulator defects (ΔV_{HT}). Note that the electrically active gate insulator defects are denoted as traps, and these terms would be interchangeably used in this book.

Figure 4.2 illustrates the double interface Reaction Diffusion (RD) model [12, 33, 34], which is used to calculate the generation and passivation of interface traps in this book. The RD model calculates the depassivation and re-passivation of Hydrogen (H) passivated defects at the channel/interlayer (IL) interface and inside the bulk of the HKMG gate stack. For simplicity, all bulk defects are lumped into a suitable "second interface" which is assigned to the IL/High-K interface for HKMG gate insulator, as illustrated in this example. The "second interface" can be defined at the center of the gate insulator for a single-layer SiO_2 or SiON gate stack. The RD model is discussed in Sect. 4.3.

Figure 4.3 illustrates the energy band diagram of a dual layer HKMG stack (a) during and (b) after stress. RD model calculates trap kinetics at the channel/IL and IL/High-K interfaces. The traps are presumed donor type, and therefore, only the ones energetically located above the Fermi level of the substrate would be positively charged and contribute (ΔV_{IT}) to ΔV_T during stress (any generated traps located below the Fermi level is not shown). During recovery, some of these traps would go below the Fermi level and would capture electrons to neutralize. Therefore, they would not contribute to ΔV_T, although they can physically exist (and at a later time can get re-passivated). Trap occupancy is calculated by the Transient Trap Occupancy Model (TTOM) [12], which is discussed in Chap. 5.

Trapping (and detrapping) of holes into (and out of) preexisting gate insulator defects give rise to hole trapping contribution (ΔV_{HT}) to ΔV_T as shown in Fig. 4.1. This is calculated by the Activated Barrier Double Well Thermionic (ABDWT) model [35], which is discussed in Chap. 5. Contribution due to generated bulk gate insulator traps (ΔV_{OT}) also contributes, Fig. 4.1. This is calculated by the Reaction Diffusion Drift (RDD) model [36] and is discussed in Chap. 6.

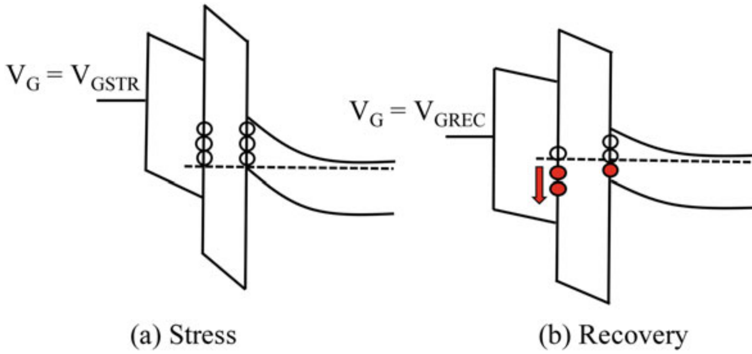

Fig. 4.3 Transient Trap Occupancy Model (TTOM) for the calculation of interface trap occupancy (a) during and (b) after stress; the example is shown for a HKMG gate insulator. The TTOM equations are described in Chap. 5

Note that the bulk trap generation is possibly due to breaking of Si-O-Si bonds (Si: Silicon, O: Oxygen) or other (different) H passivated defects to create Si-Si dimer or other forms of Oxygen vacancy (O_V) [37] (note that the chemical nature of defects is discussed in Sect. 4.6). The bulk trap generation is related to hot holes generated by the Anode Hole Injection (AHI) mechanism [38], which is discussed in Chap. 6. However, the interface trap generation is triggered by the tunneling of inversion layer (cold) holes, which is discussed in this chapter.

4.3 Reaction Diffusion (RD) Model

Figure 4.4 illustrates different versions of the RD model proposed in the literature. The time kinetics of interface traps has been modeled first using the conventional RD framework [39, 40], which suggests the depassivation (during stress) and re-passivation (after stress) of H passivated defects at the channel/gate insulator interface. The released H atoms diffuse into the oxide (and beyond) during stress, as illustrated in Fig. 4.4 (a), and diffuse back toward the interface after stress. The framework is reaction limited at short time and atomic H diffusion limited at long time during stress [40]. Note, this basic version of the RD model could explain the power law time dependence of measured NBTI kinetics during stress with a time slope $n \sim 1/4$, which has been reported in older publications [1, 2, 5, 7]. It could also explain the frequency independence of NBTI during AC stress [41], reported in early experiments [42] (see Chap. 1, Sect. 1.3 and Chap. 14 for a discussion on the f dependence or independence of NBTI).

However, all the direct methods to measure interface trap generation are intrinsically slow and suffer from recovery-related artifacts (lower magnitude and higher time slope n) as the stress is interrupted for measurement. As shown in Chap. 3, Sect. 3.2, measured time kinetics of ΔN_{IT} after delay correction results in $n \sim 1/6$, which is universally observed across different stress conditions.

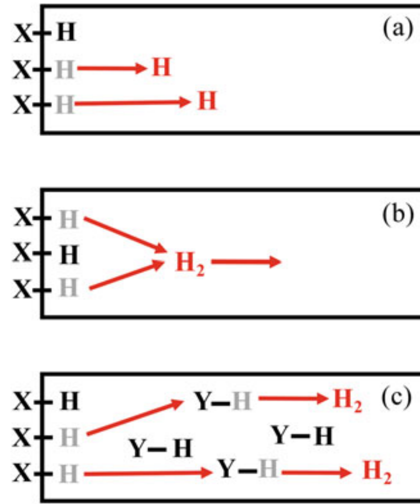

Fig. 4.4 Different versions of RD model: (a) basic with only H diffusion, (b) dimerization of H into H_2 and diffusion of H_2, and (c) defect-assisted dimerization of H into H_2 and diffusion of H_2 (also shown in Fig. 4.2 where the bulk defects are lumped into an effective second interface for simplicity)

Therefore, the RD model has been suitably modified by adding dimerization of atomic H into molecular H_2 as illustrated in Fig. 4.4 (b) [3, 33, 34, 43]. This model is reaction limited at shorter time, governed by the conversion of H to H_2 at moderate time and H_2 diffusion limited at longer time during stress; the opposite processes occur during recovery after stress. The model can explain the measured and delay corrected $n \sim 1/6$ time slope at long-time stress and frequency independence for AC stress [33]. However, it is shown later that the dimerization of two H atoms into H_2 is stochastically less probable in small area devices [44], and moreover, the reverse dissociation of H_2 into H requires a very large T activation energy of $E_A = 4.5$ eV [45]. Therefore, the defect-assisted dimerization model is preferred, Fig. 4.4 (c), which is discussed next. The defect-assisted version is consistent between the deterministic and stochastic implementations, as demonstrated in [46]. The interested reader may refer to [34] for further details on various versions of the RD model.

4.3.1 RD Model with Defect-Assisted Dimerization

Figure 4.2 illustrates the RD model with defect-assisted (a) dimerization of H into H_2 during stress and (b) reverse conversion of H_2 to H during recovery after stress for a (c) HKMG gate insulator stack. During stress, inversion layer holes break the H passivated defects (X-H) at the channel/IL interface, and the detailed mechanism is discussed later in this section. The released H atoms from broken X-H bonds diffuse into the gate insulator and react with other H passivated defects (Y-H bonds, lumped at the IL/High-K interface for simplicity) to produce H_2 molecules (defect-assisted dimerization). The generated H_2 molecules diffuse into the gate insulator bulk and backend. During recovery, H_2 molecules diffuse back and passivate the bulk insulator

defects, and the generated H atoms subsequently diffuse and passivate the defects at the channel/gate insulator interface. The chemical nature of defect precursors is discussed in Sect. 4.6, and due to uncertainties, they are denoted as X-H and Y-H bonds in this book. The model remains valid for single-layer SiO_2 or SiON gate insulators, where the bulk defects can be lumped into an imaginary interface at the center of the gate insulator stack.

The RD model with defect-assisted dimerization is explained by the following chemical reactions:

$$X - H + (\text{hole}) \leftrightarrow X - + H \tag{4.1}$$

$$Y - H + H \leftrightarrow Y - + H_2 \tag{4.2}$$

The charged state (occupancy) of X—at the channel/gate insulator interface and of Y—inside the gate insulator bulk is determined by whether these defects, presumed donor like, are energetically located above (positively charged) or below (neutral) the Fermi level (of the substrate) during stress and post-stress phases, see Fig. 4.3. As mentioned before, this aspect is handled using the TTOM framework and is discussed in Chap. 5. Total ΔV_{IT} is calculated by summing the contributions from ΔV_{IT1} at the channel/IL and ΔV_{IT2} at the IL/High-K interfaces, by using appropriate capacitance ratios, and counting only traps that are energetically above the Fermi level during or after stress from the TTOM framework.

Note that during stress, the released H atoms have to find H passivated defects in the gate insulator bulk to initiate the depassivation reactions, and during recovery, the returning H_2 molecules have to find the un-passivated defects to initiate the re-passivation reactions. However, the diffusivity of H atoms is much larger than that of H_2 molecules [3]. Therefore, the H atoms can quickly find the required precursors during stress, Fig. 4.2 (a), but the H_2 molecules would need to hop till they can find the un-passivated defects during recovery, Fig. 4.2 (b), before the respective forward and reverse reactions can proceed [33]. The H_2 molecules would hop more when the difference between the stress and recovery time is large (relatively shorter stress time and longer recovery time), due to limited availability of the un-passivated defects that can take part in the reverse reaction. Furthermore, a fraction of the H atoms and/or H_2 molecules can get temporarily locked out of the diffusion domain, due to trapping/bonding or otherwise, and become unavailable for the reaction and/or diffusion processes [39, 47]. The H_2 hopping and lock-in processes have been simulated and their roles in slowing down the recovery kinetics have been verified in the stochastic simulation domain [46]. However, in the continuum (deterministic) simulation domain, these effects are handled by slowing down the diffusivity of H_2 molecules with the passage of time *only* during recovery after stress [33, 48].

The forward and reverse reactions at the channel/IL (first) and IL/High-K (second) interfaces, as per the chemical reactions shown in Eq. 4.1 and Eq. 4.2 respectively, are given by the following equations [12]:

$$\frac{dN_{\mathrm{IT}(1)}}{\mathrm{d}t} = K_{\mathrm{F1}}\left(N_{0(1)} - N_{IT(1)}\right) - K_{R1}N_{\mathrm{IT}(1)}N_{\mathrm{H}(1)} \tag{4.3}$$

$$\frac{\mathrm{d}N_{\mathrm{IT}(2)}}{\mathrm{d}t} = K_{\mathrm{F2}}\left(N_{0(2)} - N_{\mathrm{IT}(2)}\right)N_{\mathrm{H}(2)} - K_{R2}N_{\mathrm{IT}(2)}N_{\mathrm{H2}(2)} \tag{4.4}$$

where N_0, N_{IT}, N_{H} and N_{H2}, respectively, are the H passivated defect, trap (after H depassivation), atomic and molecular Hydrogen densities at the first (1) and second (2) interfaces, while K_{F1}, K_{F2} and K_{R1}, K_{R2} are the corresponding forward and reverse reaction rates. The flux balance is done by the following equations:

$$\frac{\delta}{2}\frac{\mathrm{d}N_{\mathrm{H}(1)}}{\mathrm{d}t} = D_{\mathrm{H}}\frac{\mathrm{d}N_{\mathrm{H}(1)}}{\mathrm{d}x} + \frac{\mathrm{d}N_{\mathrm{IT}(1)}}{\mathrm{d}t} \tag{4.5}$$

$$\frac{\delta}{2}\frac{\mathrm{d}N_{\mathrm{H2}(2)}}{\mathrm{d}t} = D_{\mathrm{H2}}\frac{\mathrm{d}N_{\mathrm{H2}(2)}}{\mathrm{d}x} \tag{4.6}$$

where δ is the interfacial layer thickness (=1.5 Å), and D_{H} and D_{H2} are the diffusivities of atomic and molecular Hydrogen respectively. The diffusion of H and H_2 species is governed by the following equations:

$$\frac{\mathrm{d}N_{\mathrm{H}}}{\mathrm{d}t} = D_{\mathrm{H}}\frac{\mathrm{d}^2N_{\mathrm{H}}}{\mathrm{d}x^2} \tag{4.7}$$

$$\frac{\mathrm{d}N_{\mathrm{H2}}}{\mathrm{d}t} = D_{\mathrm{H2}}\frac{\mathrm{d}^2N_{\mathrm{H2}}}{\mathrm{d}x^2} \tag{4.8}$$

The hopping and lock-in related slowing down of H_2 diffusion during recovery is handled by the following equation:

$$D_{\mathrm{H2}}(t) = \frac{D_{\mathrm{H2_STRESS}}}{\left(1 + A * \left(\frac{\mathrm{t}}{t_{\mathrm{STR}}}\right)\right)} \tag{4.9}$$

where t is the recovery time, t_{STR} is stress time and $D_{\mathrm{H2_STRESS}}$ is the diffusivity value used during stress and A is the diffusivity reduction parameter.

The first interface forward reaction rate (K_{F1}) depends on V_{GSTR}, T and transistor process and materials, and is explained below. All other forward (second interface) and reverse (first and second interfaces) reaction rates and diffusivities of H and H_2 are only Arrhenius T activated and are process independent. The diffusivity reduction parameter only depends on the device architecture ($A = 7$ is used for planar MOSFETs and $A = 35$ for FinFETs and GAA-SNS FETs). The process-independent RD model parameters is listed in Table 4.1, and same values are used to analyze different devices throughout this book.

Table 4.1 Process (or technology)-independent RD model parameters used throughout this book. These parameters are Arrhenius T activated: $X = X_0 \exp(-E_A/kT)$, where X_0 is the pre-factor and E_A is the T activation energy of the parameter of interest (X). The diffusivity pre-factors are mentioned for IL//High-K and beyond

Parameter	Unit	Pre-factor	E_A (eV)
K_{F2}	cm^3/s	5750	0.235
K_{R1}	cm^3/s	5×10^{-6}	0.12
K_{R2}	cm^3/s	7.5×10^{-4}	0.2
D_H	cm^2/s	$2 \times 10^{-2}//4 \times 10^{-5}$	0.2
D_{H2}	cm^2/s	$9.5 \times 10^{-11}//9.5 \times 10^{-8}$	0.5

4.3.2 Physical Mechanism of Interfacial Defect Dissociation

Figure 4.5 illustrates the H passivated defect dissociation process at the first interface and lists the equations governing K_{F1} [12, 33, 34]. During stress, the inversion layer holes aided by oxide electric field (E_{OX}) tunnel to the interfacial X-H bonds. These bonds are already polarized (by factor p) in the presence of E_{OX}, and upon hole capture they become weak and are subsequently dissociated by thermal activation. The forward reaction rate K_{F1} depends on the pre-factor K_{F10} (which is proportional to hole density, p_H, tunneling coefficient, T_H, and capture cross section, σ), field acceleration (Γ_E) and T activation of bond dissociation (E_{AKF1}). The field acceleration factor (Γ_E) is a sum of the T-independent (Γ_0) and T-dependent (α/kT) terms, where α is the polarization coefficient of the X-H bond.

The process-dependent RD model parameters are K_{F10}, Γ_0, α and E_{AKF1}, among which, the parameters K_{F10} and Γ_0 depend on the effective mass (m_T) and barrier (φ_B) of the hole tunneling process (and can be determined using bandstructure calculations). Different processes such as Ge% in the channel, N% in the gate insulator stack (near the channel/IL interface) and mechanical strain in the channel can impact the bandstructure and hence m_T and φ_B. These in turn impact the parameters K_{F10} and Γ_0. It is important to note that the pre-factor K_{F10} would also depend on the capture cross section and the quality of the gate insulator. Therefore, when the capture cross section and quality of the gate insulator stay similar, bandstructure calculations can

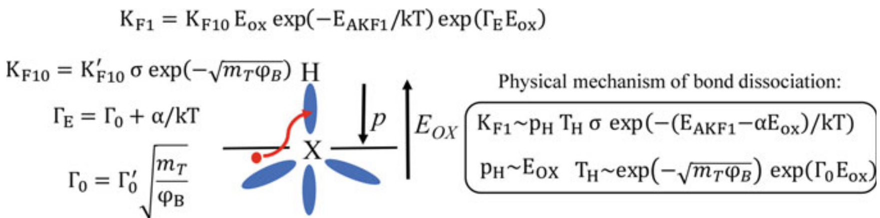

Fig. 4.5 Schematic of the inversion layer hole and oxide electric field induced dissociation of H passivated defects at the channel/gate insulator interface [34]

be used to determine the relative K_{F10} changes across different processes. The other two (α and E_{AKF1}) are pure fitting parameters.

The following process-dependent trends have been observed for the RD model parameters (discussed in detail in Sect. 4.5 and also in later chapters):

- Higher Ge% in the channel increases the valence band offset and hence φ_B with no significant impact on m_T, obtained from bandstructure calculations using the tight binding method [26, 49]. Therefore, both K_{F10} and Γ_0 reduces, although the overall Γ_E (and hence VAF) often increases due to the increase in α at higher Ge%. This remains valid for both (100) and (110) interfaces and also across different devices (bulk and FDSOI planar MOSFETs and FinFET), provided the N% is kept identical between different Ge% devices. Moreover, E_{AKF1} increases at higher Ge%, but the reason for this is not yet identified. The impact of Ge% changes on NBTI is analyzed and modeled in Chap. 8, Chap. 9 and Chap. 11, respectively, for bulk and FDSOI planar MOSFETs and FinFETs.
- Higher N% in the gate insulator near the channel/IL interface reduces the valence band offset (note that SiON has smaller bandgap than SiO_2) and hence reduces φ_B. Lower φ_B results in higher Γ_0, unless m_T also reduces at higher N%. Analysis of different devices indicates reduction in Γ_0 for the Si (100) surface but slight increase in Γ_0 for the SiGe (100) and (110) surfaces at higher N%. The relative changes in φ_B (always reduces) and m_T (reduces for the Si (100) surface but likely remains unchanged for the SiGe (100) and (110) surfaces) impact the overall change in Γ_0 at higher N%. Since α does not change, the variation in Γ_E with N% depends only on that of Γ_0. However, K_{F10} would always increase at higher N%, due to reduction in φ_B and also in m_T when applicable. The T activation E_{AKF1} reduces at higher N% and has been verified using atomistic calculations [50]. Note that the Equivalent Oxide Thickness (EOT) of the gate insulator reduces at higher N%, due to higher dielectric constant of the IL (ε_{IL}) and/or High-K (ε_{HK}), depending on the N profile in the gate stack. Therefore, a device having higher N% in the gate stack shows higher E_{OX} when compared to a lower N% device at iso-V_{GSTR}. Higher E_{OX} results in higher ΔV_{IT}; however, the resultant increase would be lower than expected, since higher ΔV_{IT} in turn would also reduce the effective NBTI stress at fixed V_{GSTR}, due to reduction in the channel electric field and inversion hole density. Therefore, even if Γ_E stays constant (due to the balancing of φ_B and m_T), the stress reduction effect results in lower VAF in higher N% devices (as the magnitude of ΔV_{IT} is higher due to higher K_{F10}). The impact of N% changes on NBTI is analyzed and modeled in Chap. 7, Chap. 9 and Chap. 11, for bulk and FDSOI planar MOSFETs and FinFETs respectively.
- Higher uniaxial compressive stress increases φ_B but does not significantly impact m_T for the (100) surface (relevant for planar, FDSOI, GAA-SNS FET top sheet), while it increases m_T but does not significantly impact φ_B for the (110) surface (relevant for FinFET sidewalls and GAA-SNS FET sheet sides), as obtained from bandstructure calculations. Therefore, both K_{F10} and Γ_0 are appropriately changed, if strain is changed due to changes in the layout or device dimensions. However, no noticeable strain impact is noted for α and E_{AKF1}. The impact of

mechanical strain on NBTI is analyzed and modeled for layout changes in FDSOI MOSFETs in Chap. 9, and for dimension changes in FinFETs and GAA-SNS FETs in Chaps. 12 and 13.

4.4 Experimental Validation of RD model

The RD model is validated using DCIV measured and delay corrected ΔN_{IT} time kinetics from planar MOSFETs and FinFETs, see Chap. 3, Sect. 3.2 for measurement and other details. Table 4.2 lists the four process-dependent RD model parameters for the Gate First (GF) HKMG planar p-MOSFETs (D1 and D2, different N% in the gate insulator) and Replacement Metal Gate (RMG) HKMG p-FinFETs (D3 and D4, different Ge% in the channel and N% in the gate insulator) used in this work. The process-independent parameters are listed in Table 4.1.

The X-H defect density at the channel/IL interface ($N_{0(1)}$) would be different for different devices, and it depends on channel orientation, gate stack thermal budget and Ge% in the channel. Note that $N_{0(1)}$ (in /cm^{2-}) values of 5×10^{12} and 7×10^{12} are, respectively, used for thermal and low T Chemical Oxide IL in (100) surface, and 1×10^{13} is used for Chemical Oxide IL in (110) surface for Si channel throughout the book. Moreover, the values are suitably reduced for SiGe channel depending on Ge%. On the other hand, the Y-H defect density at the second interface ($N_{0(2)}$) is taken as 5×10^{13} /cm^2 for all cases.

Figure 4.6 shows the time evolution of measured and modeled ΔN_{IT} in D1 (left panels) and D2 (right panels) GF planar devices at different V_{GSTR} and T during DC stress. As DCIV is a slow method, the measured data can be obtained only at longer stress time ($t_{STR} > 1$ s), while RD model simulation is shown from short to long time. Note that measured ΔN_{IT} increases with more negative V_{GSTR} and larger T as expected, increases with higher N% in the gate insulator (*e.g.*, for D2 compared to

Table 4.2 Process-dependent RD model parameters for different devices having Silicon (Si) and Silicon Germanium (SiGe) channels. The K_{F10} parameter is not listed for the D3 and D4 FinFETs to maintain confidentiality. The parameters for SiGe devices are strongly dependent on the details of the IL formation process (see Chap. 11 for further details)

Device	Unit	D1	D2	D3	D4
Type	–	Planar	Planar	FinFET	FinFET
Channel	–	Si	Si	Si	SiGe
IL type	–	Thermal	Thermal	Chem-Ox	Chem-Ox
Nitrogen	–	Low	High	Low	Medium
K_{F10}	cm/Vs	0.22	0.05	–	–
E_{AKF1}	eV	0.40	0.18	0.29	0.80
Γ_0	cm/MV	0.38	0.10	0.29	0.43
α	qÅ	1.2	1.2	1.8	2.3

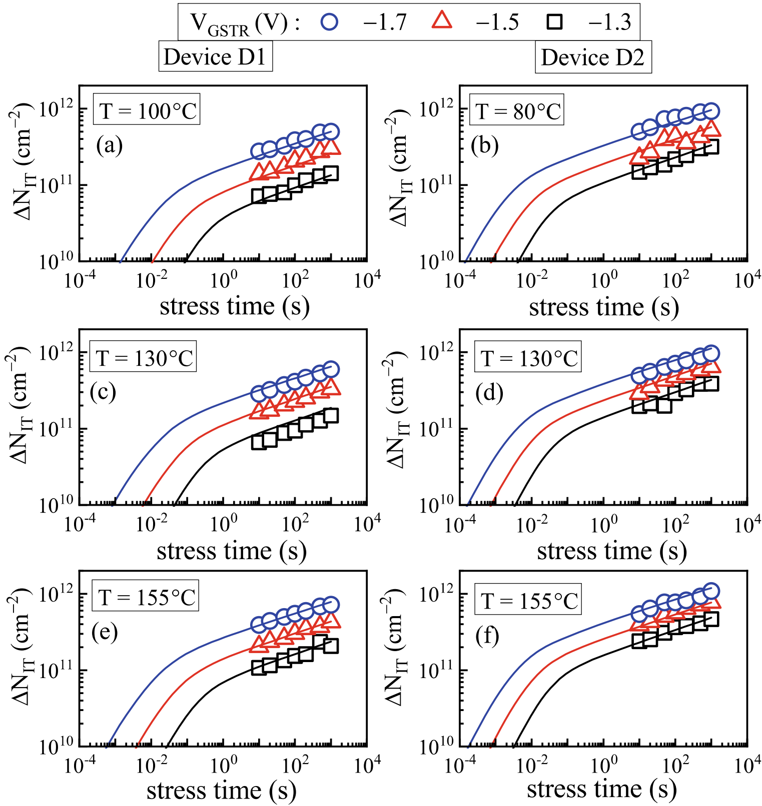

Fig. 4.6 Time evolution of DCIV measured (and delay corrected) and RD model simulated ΔN_{IT} at different V_{GSTR} and T ($V_{\mathrm{GSTR}} \times T$ matrix) for DC stress in GF HKMG Si channel p-MOSFETs with low N% (left panels) and high N% (right panels) in the gate insulator stack. Symbols: experiment, lines: model calculation. Data from [12]

D1, see Table 4.2), and shows power law time dependence with long-time slope of $n \sim 1/6$. It is important to remark that this characteristic time slope is ubiquitously observed across stress conditions and devices.

The simulated ΔN_{IT} time kinetics evolves rapidly at the initiation of stress and asymptotically settles into a power law dependence with identical $n \sim 1/6$ slope at different V_{GSTR}, T and for both devices. As mentioned before, simulated ΔN_{IT} time kinetics using RD model with defect-assisted dimerization is governed by the first interface reaction at shorter time, by defect-assisted dimerization at the second interface at intermediate time, while the long-time part is governed by molecular H_2 diffusion in the gate oxide and beyond. Note that the long-time slope of $n \sim 1/6$ is a *parameteragnostic feature* of the RD model, driven purely by molecular H_2 diffusion [34].

Figure 4.7 shows the time evolution of measured and modeled ΔN_{IT} in RMG HKMG D3 and D4 FinFETs under DC stress at different V_{GSTR} and T (left panels)

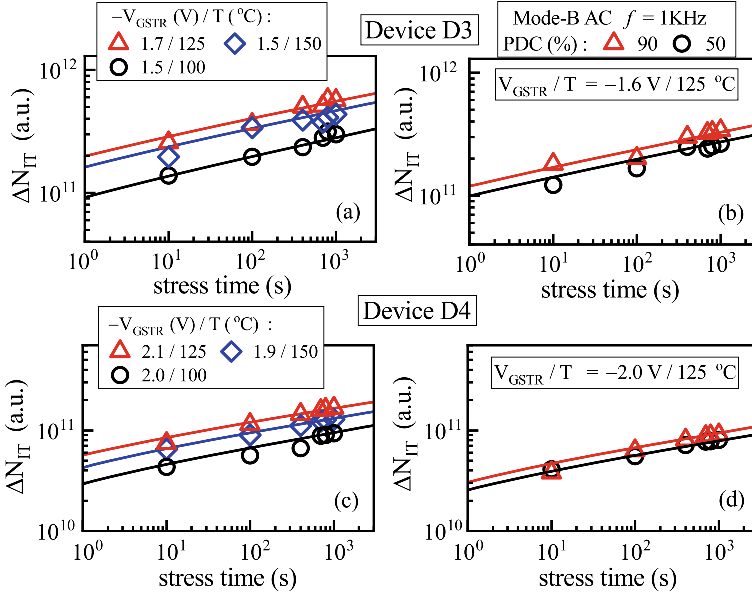

Fig. 4.7 Time evolution of DCIV measured (and delay corrected) and RD model simulated ΔN_{IT} at different (a, c) V_{GSTR} and T for DC stress and (b, d) PDC for AC stress in RMG HKMG (a, b) Si and (c, d) SiGe channel p-FinFETs. Symbols: experiment, lines: model calculation. Data from [23, 24]

and under AC stress at different PDC (right panels). The measured and modeled time kinetics of ΔN_{IT} show power law dependence with slope $n \sim 1/6$ across devices (only the long-time data can be obtained for measurement and are plotted for the simulation), for different V_{GSTR} and T during DC stress and different PDC for AC stress. Note that the ΔN_{IT} magnitude reduces at higher Ge%. Identical model parameters are used to explain the DC and AC stress for a particular device.

The measured and modeled ΔN_{IT} at fixed t_{STR} of 1Ks as a function of V_{GSTR} at different T are shown for DC stress in devices D1 and D2 in Fig. 4.8 and in devices D3 and D4 in Fig. 4.9, and also for AC stress in device D4 in Fig. 4.9, see Table 4.2 for device details. The magnitude of ΔN_{IT} increases with V_{GSTR} and T as expected. The VAF reduces at higher N% but increases at higher Ge% at a given T. Note that the VAF for a particular device reduces at higher T, and the T dependence of VAF is larger (*i.e.*, larger VAF reduction at higher T) for SiGe compared to Si devices, while no significant impact is observed for changes in N%. The reduction in VAF at higher T is due to the bond polarization effect, although the stress reduction effect (*i.e.*, reduction in the effective stress at longer time due to higher degradation-related electrostatic effect) also contributes. The model can explain the T and process dependence of measured VAF. Note that the ΔN_{IT} kinetics during stress depends on E_{OX} and not V_{GSTR}. Therefore, the process dependencies of Γ_{E} (see Fig. 4.5) and E_{OX} in the IL are responsible for the process dependence of VAF when ΔN_{IT} is plotted as a function of V_{GSTR}. This is discussed in the following section.

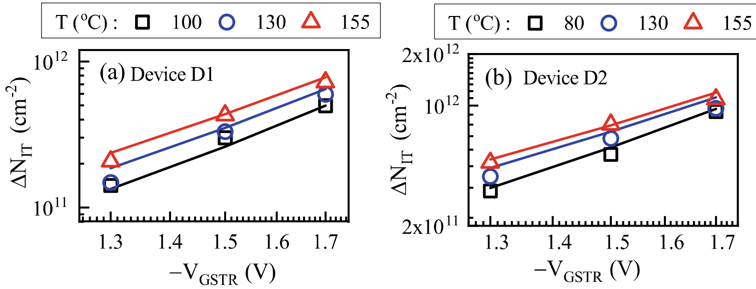

Fig. 4.8 DCIV measured (and delay corrected) and RD model simulated ΔN_{IT} at fixed t_{STR} of 1Ks as a function of V_{GSTR} at different T for DC stress in (a) D1 and (b) D2 devices listed in Table 4.2. Symbols: experiment, lines: model calculation. Data from [12]

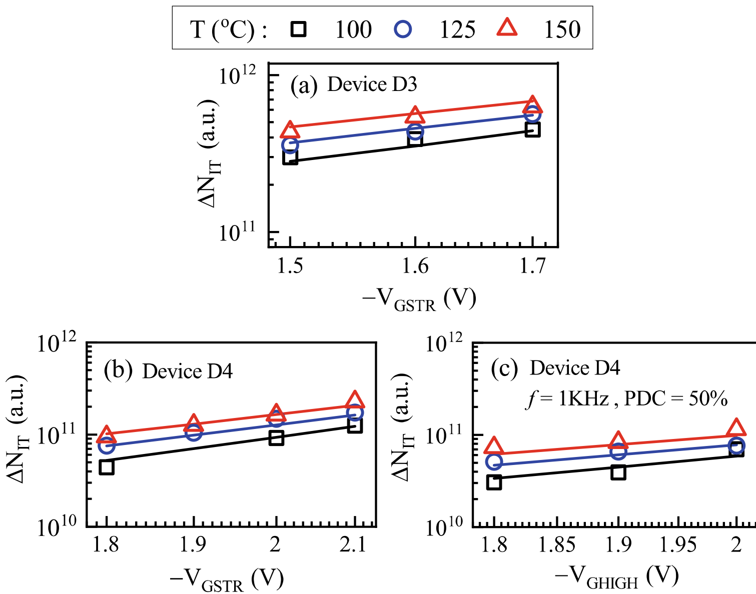

Fig. 4.9 DCIV measured (and delay corrected) and RD model simulated ΔN_{IT} at fixed t_{STR} of 1Ks as a function of V_{GSTR} at different T, for (a, b) DC stress in D3 and D4 devices and (c) AC stress in D4 device listed in Table 4.2. Symbols: experiment, lines: model calculation. Data from [23, 24]

Figure 4.10 shows the measured and modeled ΔN_{IT} at fixed t_{STR} of 1Ks as a function of (a) PDC and (b) frequency of the AC pulse in different devices. Note that identical AC to DC ratio (all data are normalized to DC stress), PDC-dependent shape and f independence are observed for all devices. One interesting aspect to note is the absence of a large jump or "kink" in the PDC dependence of ΔN_{IT} near DC, which is unlike that of the ultra-fast measured PDC dependence of ΔV_T shown in Chap. 1, Sect. 1.4 (also see Chap.14). This aspect is related to occupancy of

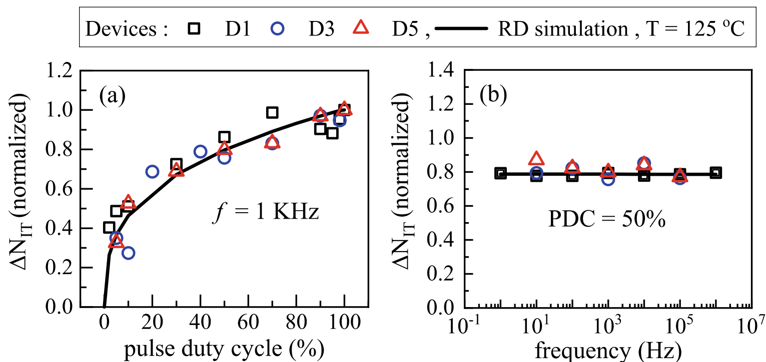

Fig. 4.10 DCIV measured (delay corrected) and RD model simulated ΔN_{IT} at fixed t_{STR} of 1Ks as a function of (a) PDC and (b) frequency. All AC data are normalized to the DC data of the particular device under consideration. Symbols: experiment, lines: model calculation. Data from [12, 24]

generated interface traps and is explained in Chap. 5. The RD model can explain the measured AC to DC ratio at various PDC and f as shown. The remarkable universality of the ΔN_{IT} time kinetics during DC and AC stress (see Fig. 4.6 and Fig. 4.7), as well as the PDC and f dependence during AC stress (see Fig. 4.10), suggests universality of the underlying trap generation mechanism. The f independence is another *parameteragnostic feature* of the RD model.

4.5 Explanation of Process (Ge%, N%) Impact

As shown above, the time kinetics (n ~ 1/6 power law dependence) during DC and AC stress, as well as the PDC-dependent shape and f independence of AC to DC ratio are universal across different devices/processes. However, the magnitude of ΔN_{IT} reduces, while VAF (at a fixed T) and the T sensitivity of VAF (reduction of VAF at higher T) increase with higher Ge% in the channel. On the other hand, ΔN_{IT} increases while VAF slightly reduces with higher N% in the gate stack, and there is no noticeable impact on the T sensitivity of VAF.

As also shown above, except the parameters governing the forward reaction of X-H bond dissociation at the channel/IL interface listed in Table 4.2, all other RD model parameters are process independent as shown in Table 4.1. The E_{OX} and T during stress and the parameters K_{F10}, E_{AKF1} and Γ_E control the bond dissociation rate $_{F1}$, where Γ_E is due to Γ_0 and α, see Fig. 4..4.5. Note, E_{OX} is determined by the thickness (T_{IL} and T_{HK}) and dielectric constant (ε_{IL} and ε_{HK}) of the IL and High-K layers in HKMG gate insulators (or T_{OX} and ε_{OX} for a single-layer gate insulator). K_{F10} and Γ_0 depend on m_T and φ_B, and these can be obtained from bandstructure calculations using the tight binding approach [49] as discussed below.

Figure 4.11 shows the simulated bandstructure, *i.e.*, the light hole (LH) and the

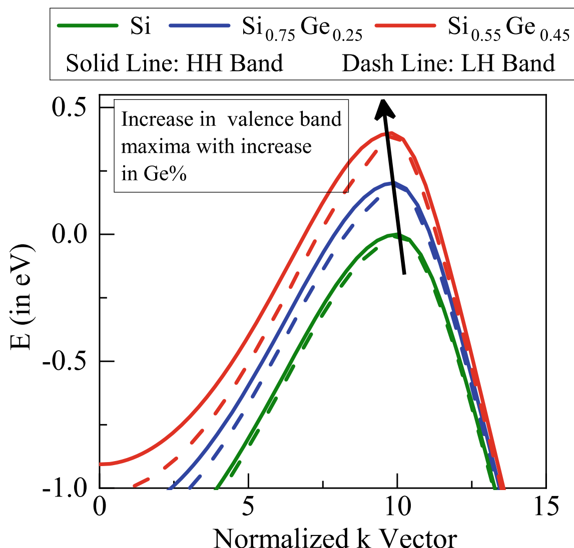

Fig. 4.11 Tight binding model [49] calculated E-k diagrams for valence bands for different Ge% in the channel. Calculations are done for the (110) surface relevant for FinFET sidewalls

heavy hole (HH) sub-bands of the valence band for different Ge% in the channel. Both the LH and HH bands are lifted up at higher Ge%, which indicate increase in φ_B. However, there is negligible change in the curvature of the bands and hence m_T remains unchanged. Higher φ_B reduces both K_{F10} (via the tunneling coefficient T_H) and Γ_0, see Fig. 4.5. The reduction in K_{F10} would result in reduction in ΔN_{IT} at higher Ge%. It is important to remark that above discussion on the impact of φ_B on K_{F10} is valid only if E_{AKF1} remains constant across different Ge%. Since E_{AKF1} is higher at higher Ge%, the relative K_{F10} value is also higher, see Table 2.2. However, the product of K_{F10} and exp $(-E_{AKF1}/kT)$ is lower at higher Ge%, and hence explains the reduction of ΔN_{IT} at higher Ge% shown in Figs. 4.7 and 4.9. Moreover, the above discussion on φ_B on Γ_0 is valid only if N% is kept same across different devices (more on this in Chaps. 8, 9 and 11).

For a particular type of channel (Si or SiGe), higher N% increases K_{F10} due to the reduction in φ_B and m_T when applicable (see Fig. 4.5), while E_{AKF1} reduces, see Table 4.2. The product of $_{F10}$ and exp $(-E_{AKF1}/kT)$ is higher at higher N% and hence explains the increase of ΔN_{IT} at higher N% shown in Figs. 4.6 and 4.8. As mentioned before, the impact of N% on Γ_0 depends on the relative changes in φ_B (always reduces at higher N%) and m_T (reduces for (100) but likely increases for (110) surface at higher N%), more on this in Chap.7, 9 and 11.

Figure 4.12 shows the Arrhenius T dependence of Γ_E, calculated using the T-dependent VAF data for (a) GF devices having different N% and (b) RMG devices having different Ge% and N%. The intercept Γ_0 reduces at higher N% but the slope (~polarization term α) does not change for GF Si channel devices (D2 versus D1). As mentioned before, the barrier φ_B reduces as the bandgap of IL reduces at higher N% near the channel/IL interface. This would imply increase in Γ_0, but the opposite is observed. This is possible if m_T also reduces at higher N%. Reduction in φ_B and

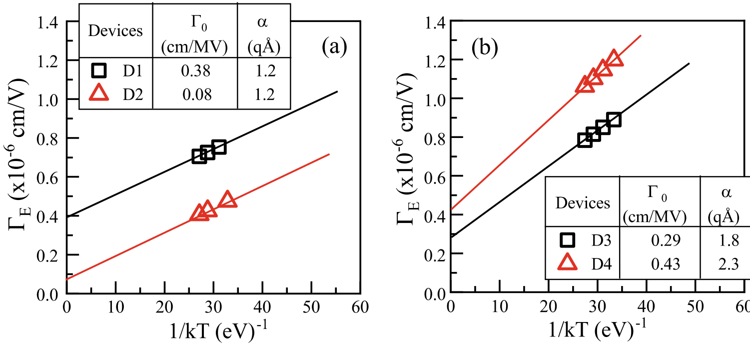

Fig. 4.12 Measured T dependence of the field acceleration factor (Γ_E), using data from (a) GF HKMG MOSFETs at different N% and (b) RMG HKMG FinFETs at different Ge% (the N% is different between D3 and D4). The intercept (Γ_0) and slope (~α) are shown. Symbols: experiment, lines: model calculation. Data from [12, 23]

m_T result in higher K_{F10} for D2 compared to D1 device (as also mentioned before, due to difference in E_{AKF1}, the term K_{F10}*exp($-E_{AKF1}/kT$) is higher at higher N%). Moreover, note that ε_{IL} increases at higher N% in the IL, resulting in lower E_{OX} at a particular V_{GSTR} and can further reduce the VAF. E_{AKF1} reduces with increase in N%, and this is addressed by atomistic calculations [50].

Interestingly, the intercept Γ_0 increases at higher Ge% (D4 versus D3), which is not expected if only changes (increase) in φ_B is considered. Due to differences in N% for the Si and SiGe devices, the m_T is different (higher for SiGe in this case), resulting in higher Γ_0. Note that Γ_0 indeed reduce at higher Ge% if N% is kept low for all devices, see Chaps. 8, 9 and 11. However, the slope increases at higher Ge% and indicates increase in the polarization factor α. Moreover, E_{AKF1} also increases with Ge%. First principles calculation is needed to explain the impact of Ge% on E_{AKF1} and α, which is beyond the scope of this analysis. Note that the term K_{F10}*exp($-E_{AKF1}/kT$) is lower at higher Ge% and explains the reduction of ΔN_{IT}. Note that besides surface orientation, Ge% and N%, the parameters for the SiGe devices are strongly dependent on the details of the IL formation process during gate stack formation.

4.6 Discussion on RD model

The chemical nature of H passivated gate insulator defects, validity of the inversion hole-assisted X-H defect dissociation mechanism at the channel/IL (gate insulator) interface, and the parameters used in RD model are debated in the literature [51] and hence are discussed in this section.

4.6.1 Nature of H Passivated Defects (Defect Precursors)

The H passivated defects at the channel/gate insulator interface are usually presumed to be Si-H bonds, which has been identified as P_b centers in Si (111)/SiO_2 interface and as P_{b0} and P_{b1} centers in Si (100)/SiO_2 interface by using the Electron Spin Resonance (ESR) and Electron Paramagnetic Resonance (EPR) studies [45, 52–54]. However, it has been suggested that not all electrically active defects are paramagnetic and detectable by ESR or EPR; rather the electrically active defects can indeed have much larger density than the spin active defects [53, 55]. Similar conclusions were also drawn from Spin-Dependent Recombination (SDR) studies [56]. Moreover, other (not P_b like) defects were suggested to be more important in technologically relevant gate insulators containing Nitrogen (which is always the case for modern gate insulators) [51–60]. Therefore, due to these uncertainties, the H passivated channel/gate insulator interfacial defects are denoted as X-H bonds in this book, Eq. 4.1.

Moreover, the H passivated bulk insulator defects for defect-assisted dimerization (and reverse reaction) can be H passivated Si-H, N-H, O-H, Oxygen vacancy (O_v-H) defects [61], different H passivated E' centers [62], and/or other complex H-related defects (Hydrogen bridge, Hydroxyl E' centers) [37]. Therefore, they are collectively denoted as Y-H bonds for simplicity, Eq. 4.2, to distinguish them from the interfacial defects (although it should be noted that the difference between interface and bulk becomes blurry in ultrathin HKMG stacks).

Note that the RD model with defect dissociation (at some rate) and subsequent H/H_2 diffusion is agnostic to the nature of H passivated defects at the channel/gate insulator interface and inside the gate insulator bulk. As long as there are H passivated defects, the RD model is applicable and would provide $n \sim 1/6$ power law time dependence during DC and AC stress and f independence during AC stress as discussed earlier in Sect. 4.4.

4.6.2 Dissociation of H Passivated Defects

Although a generic X-H defect is used in Sect. 4.3 due to the uncertainties listed in Sect. 4.6.1, the original reports suggested that inversion layer holes during NBTI stress tunnel to the interfacial Si-H defect precursors, get captured to make them weak, and the weak bonds can subsequently get broken by thermal activation [34, 43]. However, the charge neutrality level (0/+) of Si-H bond was shown at ~4 eV below the Si valence band [63], and therefore, it is suggested that Si-H bonds cannot capture holes via tunneling [51].

As discussed above, there exists a strong possibility that the dominant electrically active defects are something other than the usual paramagnetic Si-H bonds. Moreover, the Si-H charge neutrality level is determined using Density Functional Theory (DFT) calculations in bulk amorphous Si (a-Si) in [63] and not in SiO_2 (or more

appropriately, SiON). Moreover, while DFT calculations presumably work well for thicker and bulk material systems, it faces challenges when a thin amorphous layer is sandwiched between two interfaces, *e.g.*, a thin SiO_2 (or SiON) layer between Si/SiO_2 and SiO_2/poly-Si interfaces for conventional single-layer gate insulator, and even thinner SiO_2 (or SiON) IL between Si/IL and IL/High-K interfaces for HKMG gate insulators. DFT also faces challenges in the presence of different species, *e.g.*, the presence of Hf in IL due to penetration from HfO_2 High-K and also the presence of N in IL due to penetration from spacer or gate material [9], and in the presence of defects *(e.g.*, O_v- [61]). Therefore, DFT simulations are challenging in realistic gate insulator stacks.

The thermal dissociation of Si-H bonds requires very high energy ($E_A = 2.6$ eV) [45, 64] and therefore is presumed to be impossible under normal NBTI experimental conditions [65]. However, the chemical reaction Si-H + H → Si + H_2 is suggested to have very low barrier [45], and hence, it is presumed that the release of H atoms bonded with channel acceptors initiate the H dissociation from interfacial Si-H bonds [65]. However, note that the NBTI degradation magnitude is similar between planar (high channel doping) and FinFET (negligible channel doping) devices for similar V_{GSTR} and T [16, 17], which is inconsistent with the concept of released H from the channel acceptors being responsible for bond dissociation (this theory would imply negligible NBTI in FinFETs). Another recent report has suggested the release of H atoms from the gate and subsequent diffusion toward the channel initiate the Si-H bond dissociation near the channel/gate insulator interface (the Gate Side Hydrogen Release model) [66]. However, this framework is rate limited by H release from the gate and therefore cannot explain the impact of higher Ge% in the channel (reduction in NBTI magnitude and increase in VAF at higher Ge%) as discussed before and later in Chaps. 8, 9 and 11.

On the other hand, the mechanism discussed in Sect. 4.3 can explain measured data under wide range of experimental conditions and channel/gate insulator process changes as discussed in Sect. 4.4 and also in later chapters of this book.

4.6.3 Model Parameters

The Si-H bond dissociation energy has been found to be ~2.6 eV using Electron Paramagnetic Resonance (EPR) studies [45], which is much larger than the E_{AKF1} values listed in Table 4.2. Note that the bond dissociation studied in [45] is under vacuum thermal anneal in Si (111)/SiO_2 (50 nm thickness) samples and is unlikely to represent NBTI defects in Si (100) or Si (110) interfaces with thinner gate insulators as mentioned above. Moreover, as discussed above, the electrically active defects exposed to NBTI in modern devices are not necessarily the standard P_b centers that were studied using EPR in [45].

The Arrhenius T activation values used in Table 4.1 are similar for the forward and reverse reactions governed by Eq. 4.4 (corresponding to the chemical reaction of Eq. 4.2). However, they are respectively found to be exothermic and have very large

thermal barrier from EPR studies in Si (111)/SiO_2 system [45, 67]. Therefore, the choice of these RD model parameter values seems questionable [51]. It is important to note that Eq. 4.4 (or Eq. 4.2) and the corresponding parameter values are for H passivate defects inside the SiO_2 (or SiON) bulk or at the IL/High-K interface, and therefore, identical values as [45, 67] are not expected.

Finally, the H_2 diffusivity values listed in Table 4.1 are presumably different as compared to those in other reports [51]. It is noteworthy that modern gate stacks containing Nitrogen can have significantly lower H_2 diffusion and hence, reduced diffusivity values are expected [3].

It is noteworthy that although the objections raised in [51] seem plausible at the face value, none of them can be justified under a rigorous inspection. On the other hand, the RD model with fixed and adjustable parameters listed in Table 4.1 and Table 4.2, respectively, can quantitatively model the DCIV measured ΔN_{IT} time kinetics during DC and AC stress under different experimental conditions, and on various types of devices. The RD model can also explain a variety of other process dependence as discussed in later chapters.

4.7 Summary

According to the BAT-NBTI framework, device parametric drift is due to uncorrelated sum of different underlying processes, *e.g.*, $\Delta V_T = \Delta V_{IT} + \Delta V_{HT} + \Delta V_{OT}$, where ΔV_{IT} is calculated by the TTOM-enabled RD model. RD model with defect-assisted dimerization remains consistent between the deterministic and stochastic implementations and is used throughout this book. RD model calculates the time kinetics of ΔN_{IT} during and after stress, while TTOM computes their contribution (ΔV_{IT}) to overall ΔV_T. The ΔN_{IT} kinetics simulated by the RD model shows power law time dependence at longer time with exponent $n \sim 1/6$ for both DC and AC stress and f independence for AC stress. The model uses an inversion layer hole-assisted defect dissociation mechanism at the channel/gate insulator interface, with four parameters to quantify process changes. The model is validated using DCIV measured ΔN_{IT} time kinetics during DC and AC stress, in planar and FinFET devices having different processes (Ge% in the channel and N% in the gate stack), and for different experimental conditions. Two of the process-dependent parameters can be obtained by bandstructure calculations, and so the other two are truly adjustable across process changes. The validity of the physical mechanisms governing RD model and the model parameter values are also discussed.

Other components of the BAT framework for NBTI, *i.e.*, TTOM, hole trapping and bulk trap generation, are described in Chaps. 5 and 6.

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