Analysis of Cache Memory Architecture Design Using Low-Power Reduction Techniques for Microprocessors

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1 Introduction

Wireless sensor network production has revolutionized our lifestyles. Sensor networks may be used for different purposes, such as military surveillance, monitoring of the environment, medical diagnosis, etc. A wireless sensor network used for medical diagnosis is defined as the body area network (Istepanian et al. 2004; Gyselinckxet al. 2005). To provide real-time input, body region networks have to do continuous health monitoring. Continuous monitoring of physiological parameters is enabled by body area networks. Compared to the physiological parameters obtained from short-term monitoring, for example, hospital stays, this continuous monitoring for long periods in the natural environment produces better results (Park et al. 2003). Miniature wireless sensor nodes with an extended operating life are needed to further expand the capabilities of the body area network. For the realization of ubiquitous sensing, the sensor nodes must have a very small form factor (Gyselinckx et al. 2005) without interfering with the object being monitored. This miniaturization results in a decrease in the energy capacity of the sensor since the battery size used to store the energy is limited. The intrusive procedure necessity (Malan et al. 2004) complicates the replacement of the embedded medical wireless sensor nodes by the battery [1, 2].

1.1 Power Reduction Techniques

Power reduction techniques are applied over circuits to reduce the power consumption of circuits with no effect on performance, speed, and other parameters.

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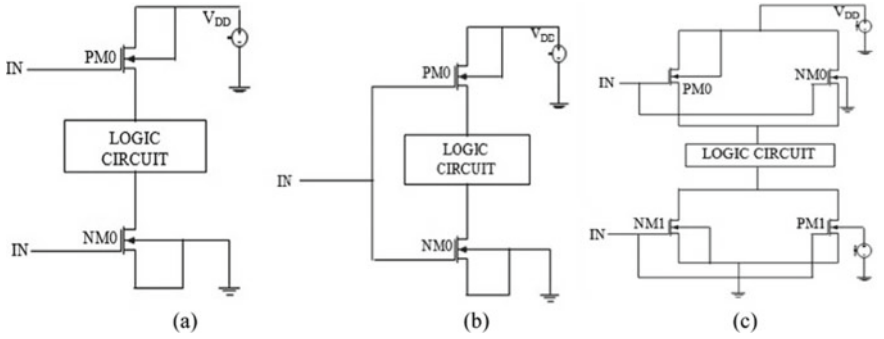


Fig. 1 **a** Sleep transistor technique; **b** forced stack technique; **c** dual sleep technique

1.1.1 Sleep Transistor Technique

The state-destructive technique disrupts both P_{MOS} and N_{MOS} transistors from sleep transistors to supply voltage or ground. These methods are called V_{DD} and gated-GND. These are technological varieties. When the logic circuits are in standby mode, the sleep transistor is disabled. By uninflecting sleep transistor operation from the logical networks, the technique of sleep semiconductor significantly reduces sleep power as shown in Fig. 1a [3].

1.1.2 Forced Stack Technique

Figure 1b demonstrates a forced stack technique. This second technique decreases the power by stacking transistors. When two or more transistors are uniformly switched OFF, the effect of stacking the semiconductor device reduces the sub-threshold leakage current [4].

1.1.3 Dual Sleep Technique

Both types of transistors are used in this technique: two PMOS (PM0 and PM1) and two NMOS (NM0 and NM1). Both PMOS and NMOS transistors are used in the header and footer. One transistor is ON in active mode, and another transistor is switched ON in OFF state mode. PMOS and NMOS are both used in standby mode to reduce power, as shown in Fig. 1c [5].

These circuits became known as high-density circuits because of their numerous transistors used and also because of the high leakage rate concerning technological developments. The input power supply was then reduced by attempting to reduce the energy consumption rate [6–8]. As compared with SRAM memories, they have higher percentages of portable devices with static memory because more power is

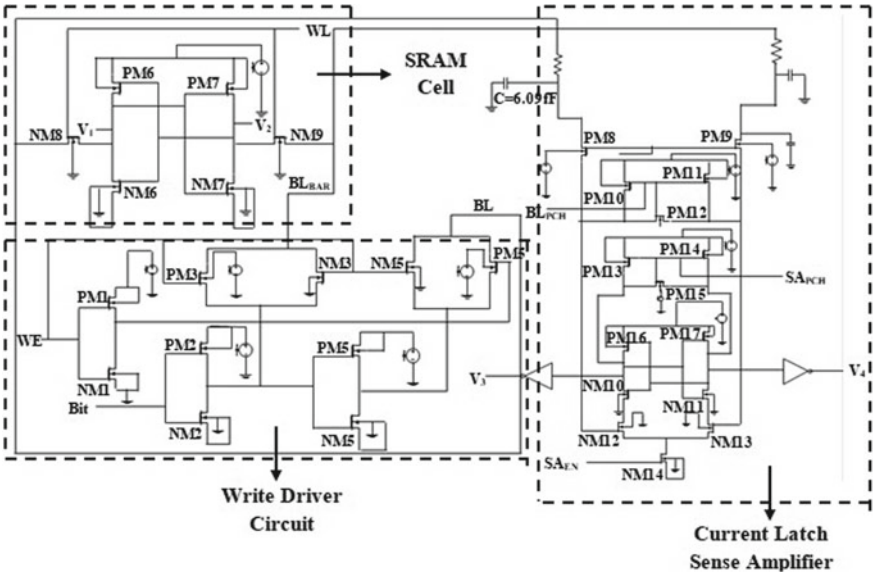


Fig. 2 Schematic of single-bit cache memory architecture

spent on data stability in DRAM memory. In both static and dynamic memories, the access time is approximately the same [9–11].

2 Single-Bit Memory Architecture

WDC, SRAMC, and CLSA as shown in Fig. 2 [12, 13] are the single-bit cache memory architectural blocks. The description is divided into three different parts: (a) the WDC with two input pins (word enable (WE) and Bit) and two output pins (BL and BL_{BAR}), (b) the SRAMC, which is attached to the WDC via bit lines (i.e., BL and BL_{BAR}), and an input pin [word line (WL)] and two output pins (V_1 and V_2) and connected through bit lines having capacitance and resistance as a connector between them, (c) CLSA which has 4 input pins (Y_{sel}, BL_{PCH}, $SA_{PCH,}$ and SA_{EN}) and two output pins (V_3 and V_4).

3 Write Driver Circuit

Figure 3 shows the write driver schematic developed in this work. The bit line is discharged from its high pre-load level to below the SRAMC writing margin by the WDC. The voltage required to enter the desired value in the bit line is determined

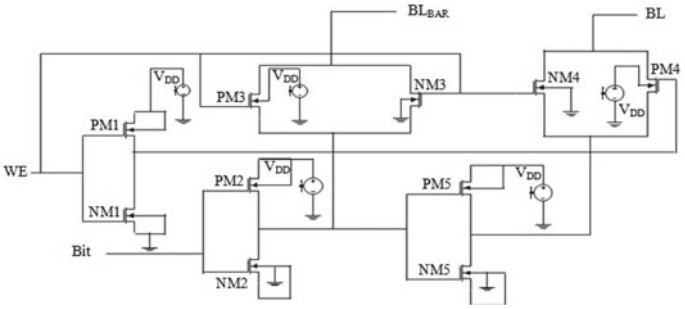


Fig. 3 Write driver circuit schematic

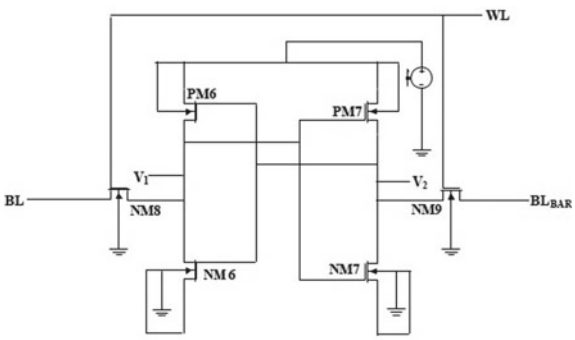
by the WDC. When "WE = 1" (write enable pulled high), data from the data input pin are entered in bit lines and transferred to the corresponding memory cell through the access transistors.

To obtain the glitch-free bit lines, the buffer circuit has been positioned before the output of the WDC. It has to enter a certain value in the bit cell up to the WDC. The circuit has the purpose of charging and discharging the bit lines in the memory cell to the desired bit being written [14].

3.1 Conventional SRAM

The 6T SRAMC circuit diagram is shown in Fig. 4. SRAMC is called a static ram cell because the data could be held for a long time until the power is being provided forever. Six transistors are used in SRAMC; PM6, PM7, NM6, and NM7 are composed of the two cross-coupled CMOS inverters plus two N_{MOS} transistors (NM8 and NM9) known as access transistors. It is known as the 6T cell. Each bit is a transistor-compatible SRAMC, which forms two cross-coupled inverters. This cell has two stable states either 0 or 1 [15, 16].

Fig. 4 SRAM cell schematic



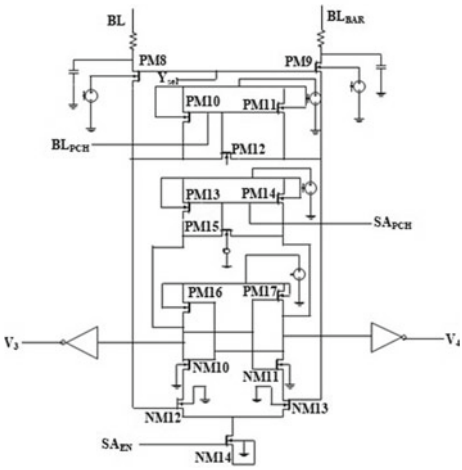


Fig. 5 Current latch sense amplifier schematic

3.2 Current Latch Sense Amplifier

The sense amplifier is a circuit of great importance in cache memory architecture. One of the bit line releases during reading operation while the other bit line remains at supply voltage. Due to the capacity of the large bit line, the slow discharge is small and the bit cells access the transistor. To accomplish this, a minor difference between the values of the bit line voltages [17, 18] is amplified by the SA at digital levels. Figure 5 indicates the current latch sense amplifier schematic.

The circuit operation is as follows [19, 20]. On bit lines, the differential voltage is transferred to SA_3 and SA_4 CLSA inputs. If both SA_1 and SA_2 start discharge at high outputs SA_{EN} is pulled high. These results in a higher power by NM12 compared to NM13 because of its higher V_{gs}. This allows the output V_3 to be discharged faster than V_4.

4 Analysis of Result

Figure 6 describes the output waveform of WDC, for cases arise: (a) when Bit = 0 V and WE = 0 V BL = V_{DD} and BL_{BAR} = V_{DD}, (b) Bit = 0 V WE = V_{DD} so, BL = 0 V and BL_{BAR} = $V_{DD}/2$, (c) Bit = V_{DD} WE = 0 V so, BL = 0 V and BL_{BAR} = $V_{DD}/2$ and (d) Bit = V_{DD} WE = V_{DD} so, BL = V_{DD} and BL_{BAR} = 0 V.

Figure 7 describes the both write operation and hold operation of the SRAM cell. There is a pull-up network (PM6 and PM7), pull-down network (NM6 and NM7), and access transistor (NM8 and NM9) which allows data to store and sense amplifier to read the data. Figure 8 describes the read operation of CLSA when both SA_{EN} and

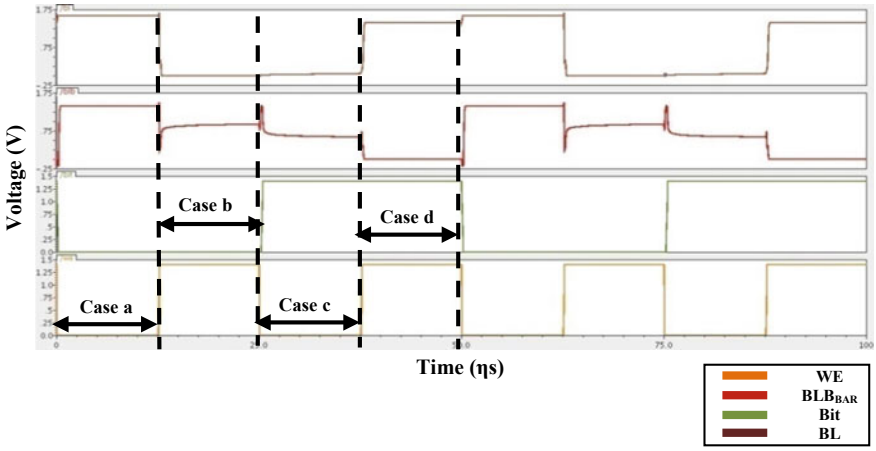


Fig. 6 Output waveform of WDC

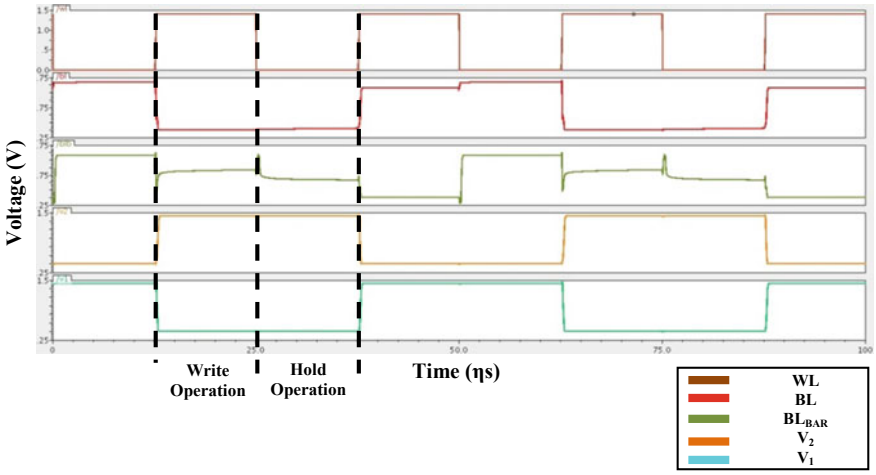


Fig. 7 Output waveform of SRAM cell

WL are pulled high, during that time only the sense amplifier senses the data from the SRAM cell at bit lines and gives output at V_3 and V_4.

Table 1 describes that as increasing in value of resistance power consumption decreases as because resistance is a path stopper for current in a circuit and no effect on the area, performance, and speed whereas Table 2: describes the power reduction techniques applied over CLSA.

Table 3: describes the power consumption of single-bit cache memory architecture on applying power reduction techniques over SRAM cell and CLSA consume less power 111.58 μW up to 56%. All the table's results depicted that single-bit

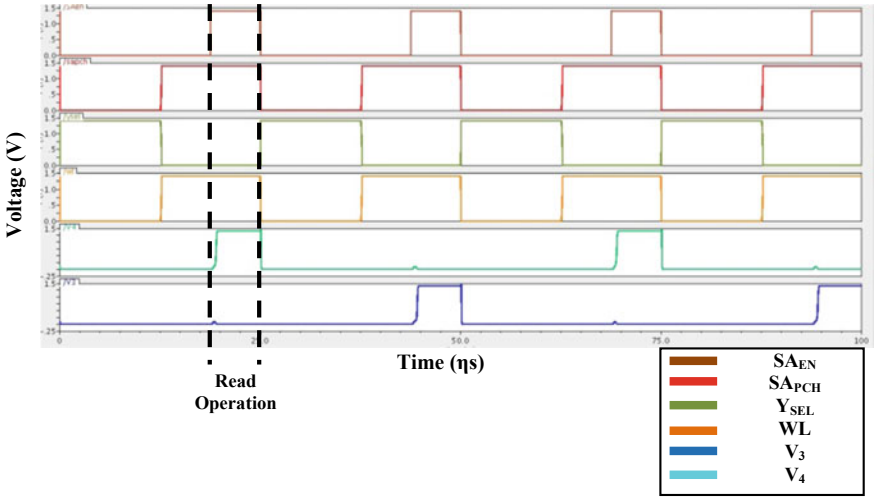


Fig. 8 Output waveform of CLSA

Table 1 Different parameter of single-bit cache memory architecture

S. No.	Parameters	Power consumption (μW)	No. of transistors	Sensing delay (ηs)
1	$R = 42.3\ \Omega$	73.92	35	18.75
2	$R = 42.3\ \text{K}\Omega$	26.78	35	18.75

Table 2 Single-bit cache memory architecture analysis of different parameters with power reduction techniques applied over CLSA

S. No.	Techniques	Power consumption (μW)	Sensing delay (ηs)	No. of transistors
1	Sleep transistor technique	25.89	18.81	37
2	Forced stack technique	13.4	19.37	37
3	Dual sleep technique	25.9	18.68	39

Table 3 Single-bit cache memory architecture analysis of different parameters with power reduction techniques applied over SRAM cell and CLSA

S. No.	Techniques	Power consumption (μW)	Sensing delay (ηs)	No. of transistor
1	Sleep transistor technique	24.62	18.88	39
2	Forced stack technique	11.58	19.59	39
3	Dual sleep technique	24.64	19.12	43

cache memory architecture with forced stack technique over SRAM cell and CLSA consume the lowest power 11.58 μW with an increase in the number of the transistor from 35 to 39. There is always a trade-off between power consumption and area.

5 Conclusion

In the proposed work, single-bit cache memory architecture has been implemented and it is comprised of WDC, SRAM cell, and a current latch sense amplifier. Apart from its different parameters of single-bit cache memory architecture has been analyzed at different values of resistance (R). Furthermore, power reduction techniques such as sleep transistor technique, forced stack technique, and dual seep technique are applied over SRAM cell and CLSA. Results depicted that on the increasing value of R power consumption reduce at $R = 42.3\ \text{k}\Omega$ consume 26.78 μW power and a single-bit cache memory architecture having SRAM cell and CLSA with forced stack technique consume 11.58 μW. In future scope, this work can be done in form of an array.

References

1. He, Y., Zhang, J., Wu, X., Si, X., Zhen, S., Zhang, B.: A half-select disturb-free 11T SRAM cell with built-in write/read-assist scheme for ultralow-voltage operations. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **27**(10), 2344–2353 (2019). https://doi.org/10.1109/TVLSI.2019.2919104
2. Fragasse, R., et al.: Analysis of SRAM enhancements through sense amplifier capacitive offset correction and replica self-timing. IEEE Trans. Circ. Syst. I Regul. Pap. **66**(6), 2037–2050 (2019). https://doi.org/10.1109/TCSI.2019.2902102
3. Tripti, T., Chauhan, D.S., Singh, S.K., Singh, S.V.: Implementation of low-power 6T SRAM cell using MTCMOS technique. In: Advances in Computer and Computational Sciences. Springer, Singapore (2017)
4. Geetha Priya, M., Baskaran, K., Krishnaveni, D.: Leakage power reduction techniques in deep submicron technologies for VLSI applications. In: International Conference on Communication Technology and System Design. Elsevier (2011)
5. Sridhara, K., Biradar, G.S., Yanamshetti, R.: Subthreshold leakage power reduction in VLSI circuits: a survey. In: 2016 International Conference on Communication and Signal Processing (ICCSP), pp. 1120–1124 (2016)
6. Gupta, S., Gupta, K., Calhoun, B.H., Pandey, N.: Low-power near-threshold 10T SRAM bit cells with enhanced data-independent read port leakage for array augmentation in 32-nm CMOS. IEEE Trans. Circ. Syst. I Regul. Pap. **66**(3), 978–988 (2019). https://doi.org/10.1109/TCSI.2018.2876785
7. Dounavi, H., Sfikas, Y., Tsiatouhas, Y.: Periodic aging monitoring in SRAM sense amplifiers. In: 2018 IEEE 24th International Symposium on On-line Testing and Robust System Design (IOLTS), Platja d'Aro, pp. 12–16 (2018). https://doi.org/10.1109/IOLTS.2018.8474169
8. Ahmad, S., Iqbal, B., Alam, N., Hasan, M.: Low leakage fully half-select-free robust SRAM cells with BTI reliability analysis. IEEE Trans. Device Mater. Reliab. **18**(3), 337–349 (2018). https://doi.org/10.1109/TDMR.2018.2839612

9. Reddy, B.N.K., Sarangam, K., Veeraiah, T., Cheruku, R.: SRAM cell with better read and write stability with minimum area. In: TENCON 2019—2019 IEEE Region 10 Conference (TENCON), Kochi, India, pp. 2164–2167. https://doi.org/10.1109/TENCON.2019.8929593
10. Surkar, A., Agarwal, V.: Delay and power analysis of current and voltage sense amplifiers for SRAM at 180 nm technology. In: 2019 3rd International Conference on Electronics, Communication, and Aerospace Technology (ICECA), Coimbatore, India, pp. 1371–1376 (2019). https://doi.org/10.1109/ICECA.2019.8822122
11. Gomes Iuri, A.C., Cristina, M., Butzen Paulo, F.: Design of 16 nm SRAM architecture. In: South Symposium on Microelectronics (2012)
12. Kaushik, C.S.H., Vanjarlapati, R.R., Krishna, V.M., Gautam, T., Elamaran, V.: VLSI design of low power SRAM architectures for FPGAs. In: 2014 International Conference on Green Computing Communication and Electrical Engineering (ICGCCEE), pp. 1–4 (2014)
13. Choudhary, R., Padhy, S., Rout, N.K.: Enhanced robust architecture of single bit SRAM cell using drowsy cache and super cut-off CMOS concept. Int. J. Ind. Electron. Electr. Eng. **3**, 63–68 (2011)
14. Gajjar, J.P., Zala, A.S., Aggarwal, S.K.: Design and analysis of 32 bit SRAM architecture in 90 nm CMOS technology. Int. Res. J. Eng. Technol. (IRJET) **03**(04), 2729–2733 (2016)
15. Agrawal, R., Tomar, V.K.: Analysis of cache (SRAM) memory for Core I™ 7 processor. In: 9th International Conference on Computing, Communication and Networking Technologies (ICCCNT), p. 402 (2018)
16. Vanama, K., Gunnuthula, R., Prasad, G.: Design of low power stable SRAM cell. In: 2014 International Conference on Circuit Power and Computing Technologies (ICCPCT), pp. 1263–1267 (2014)
17. Chandankhede, R.D., Acharya, D.P., Patra, P.K.: Design of high-speed sense amplifier for SRAM. In: IEEE International Conference on Advanced Communication Control and Computing Technologies, pp. 340–343
18. Wei, Z., Peng, X., Wang, J., Yin, H., Gong, N.: Novel CMOS SRAM Voltage Latched Sense Amplifiers Design Based on 65 nm Technology, pp. 3281–3282
19. Mohammad, B., Dadabhoy, P., Lin, K., Bassett, P.: Comparative study of current mode and voltage mode sense amplifier used for 28 nm SRAM. In: 24th International Conference on Microelectronic (2013)
20. Sinha, M., Hsu, S., Alvandpour, A., Burleson, W., Krishnamurthy, R., Borhr, S.: High-performance and low-voltage sense-amplifier techniques for sub-90 nm SRAM. In: IEEE International [Systems-on-Chip] SOC Conference (2003)