Lecture Notes in Electrical Engineering 781

Trupti Ranjan Lenka
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Preface

The book presents state-of-the-art research and developments in micro- and nanoelectronics devices, circuits and systems through selected papers of **2021 Springer International Conference on Micro/Nanoelectronics Devices, Circuits and Systems (MNDCS-2021)** held during 29–31 of January 2021 virtually hosted by the Department of Electronics and Communication Engineering, National Institute of Technology Silchar, Assam, India. The high-quality contributions cover emerging trends in semiconductor materials and device technology, integrated circuit technology, system-on-chip (SoC), MEMS and sensors for emerging applications. The contributed papers from India and Italy are included in this book.

The micro- and nanoelectronics devices include semiconductor device physics, quantum electronics, heterostructure transport, compact device modeling, nanowire LED, organic LED, MOSFET, OTFT, OFET, FinFET, TFET, HEMT, THz devices, photonics devices, UWB semiconductor materials, 2D materials, nanotechnology: nanowires, nanostructures, carbon nanotubes, graphene, flexible electronics, high-efficiency solar cells: Perovskite, CZTS, Kesterite and novel photovoltaic concepts as outlined in chapters on various emerging applications. From device domain, the best paper was awarded to "*Comprehensive Analysis of α- and β-form of Copper (II) Phthalocyanine for Organic Field-Effect Transistors*".

The micro- and nanoelectronics circuits part includes analog VLSI circuits, digital VLSI circuits, mixed-mode VLSI circuits, bioelectronics circuits, circuit optimization techniques, reconfigurable circuits, HDL-based FPGA design and semiconductor memories: DRAM and SRAM. They are listed in various chapters for emerging applications such as 5G technology, IOT and biomedical. From circuits domain, the best paper was awarded to "*A 0.7 V 0.144 μW Frequency Divider Design with CNTFET Based Master Slave D-Flip Flop.*"

The micro- and nanoelectronics systems in various chapters include System on Chip (SoC), MEMS/NEMS, antennas, sensors, actuators, nanogenerators, energy harvesters (Piezoelectric and MEMS based), micromachining, microfluidics, Lab-on-Chip, healthcare systems, embedded system design, biomedical systems, IoT and

smart systems. From micro- and nanosystems domain, the best paper was awarded to "*Exploiting RF MEMS Switches for Pattern Reconfigurable Parasitic Antennas*."

Silchar, India — Trupti Ranjan Lenka
Newark, USA — Durgamadhab Misra
Asansol, India — Arindam Biswas

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The editors acknowledge the Department of Electronics and Communication Engineering, National Institute of Technology Silchar, Assam, India, for providing the platform to organize 2021 Springer International Conference on Micro/Nanoelectronics Devices, Circuits and Systems (MNDCS-2021) held virtually during 29–31 of January 2021.

The editors also acknowledge IEEE Nanotechnology Council Chapter and IEEE EDS NIT Silchar Student Branch Chapter and Institute Innovation Cell for their technical collaboration and providing international platform to organize MNDCS-2021.

Acknowledgment also goes to all the authors and co-authors for their valuable and quality contributions and presentations in MNDCS-2021. All the potential reviewers of MNDCS-2021 are also well acknowledged for their voluntary contributions for selecting good-quality manuscripts.

The keynote speakers (Prof. C. Jagadish, The Australian National University, Australia; Prof. Ilya Sychugov, KTH Royal, Stockholm; Prof. Samar Saha, Prospicient Devices, CA, USA; Prof. Lan FU, The Australian National University, Australia; Prof. Zoran Jaksic, University of Belgrade, Serbia; Prof. Yong Shi, Stevens Institute of Technology, New Jersey, USA; Prof. Hieu P. T. Nguyen, New Jersey Institute of Technology (NJIT), New Jersey, USA; and Prof. Ajay Agrawal, CEERI, Pilani, India) and invited speakers (Ravi Teja Velpula, NJIT, USA; Prof. P. Susthitha Menon, Universiti Kebangsaan Malaysia (UKM), Malaysia; Dr. Jacopo Iannacci, Fondazione Bruno Kessler, Italy; Dr. Olga Jaksic, University of Belgrade, Serbia) of MNDCS-2021 are highly acknowledged for their keynote and invited talks respectively on micro- and nanoelectronics devices, circuits and systems.

All the chairs/co-chairs and organizing committee of MNDCS-2021 are acknowledged for the successful organization of the international conference.

Finally, the editors acknowledge Springer Nature for being the publishing partner of MNDCS-2021.

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Exploiting RF MEMS Switches for Pattern Reconfigurable Parasitic Antennas

Paul Ssejjuuko, Massimo Donelli, and Jacopo Iannacci

Abstract New generation Radio Frequency Microelectromechanical Systems (RF MEMS) Switches with high performance have been developed recently and the capability to exploit them for designing reconfigurable antennas is presented in this paper. A parasitic antenna on a planar structure with the Yagi-Uda concept is used as a proof of concept. The structure is composed of a dipole of half the wavelength of the operational frequency (the driven element) and a set of parallel parasitic elements on the sides that are exploited to tune the antenna characteristics. Four antenna configurations are obtained by adjusting the length of the parasitic elements using RF MEMS switches placed at suitable discontinuities. The preliminary results demonstrated that the considered antenna structure (operating in the X-band) is able to steer the beam from broadside to end fire pattern keeping a return loss below −10 dB and a good gain in all the antenna configurations.

Keywords Pattern reconfigurable antennas · RF MEMS switches · Parasitic elements

1 Introduction

Carried out the study and drafted this paper. In the last decade, reconfigurable antennas have gained a great deal of attention and played a significant role in intelligent systems which are the future of communication systems and actually are driven

Carried out the study and drafted this paper.

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by the evolution of 5G and Internet of Things (IoT) [1–3]. By purposefully altering the radiation properties, polarization, or frequency, reconfiguration of the antenna can be attained. In order to obtain a reconfigurable antenna, some switching mechanism must be employed [4] and standard devices that have mostly been employed include; PIN Diodes, RF relay Switches, varactor diodes, and FETs. Recently RF MEMS switches demonstrated their superior performance characteristics compared to the other switching techniques [3, 5] and they have been successfully adopted for long-range wireless sensor [6].

In particular, reconfigurable antennas are very attractive for wireless communications owing to their capability to steer the beam in different azimuth directions, hence increasing coverage and connectivity, simultaneously delivering miniaturization since one antenna can perform several roles substituting many single role antennas [7]. They also provide beam steering away from the jamming signal which is important for radar and any radio communication systems. RF MEMS switches demonstrated to provide very good RF performance behavior regarding Isolation and Insertion loss as opposed to their semiconductor counterparts, moreover they require very low power [5] which make them suitable for IoT and wireless sensor networks applications.

RF MEMS also present the capability of operating from a few MHz up to more than 100 GHz while maintaining very good performance. Evaluation of RF MEMS through experiments demonstrated that they can be used in a wide range of applications and they are the best candidate for the new 5G and mm wave frequency bands [8]. In this regard, they serve as vital components that can be utilized to enhance performance of RF systems. The capabilities of RF MEMS are well known in the microelectronic research community, but they still need affirmation in the electromagnetic community and in particular in antenna design and this is the contributions of this paper.

In wireless applications, parasitic antennas are attractive for providing variations in radiation pattern because they provide a transitional solution between a dipole element with poor performance and the complexity and cost of phased array structures [9, 10]. As compared to the regular phased arrays, they present a new and less complex way to realize change in the antenna radiation characteristics [11]. The possibility of varying antenna radiation properties by use of parasitic elements was first exhibited by the Yagi Uda Antenna and the parameters such as length, spacing between and number of parasitic elements impacts the antenna performance. For changing the mechanical separation between the antenna elements some mechanical actuators can be used which means increased size of the design and shorter life of the device due to mechanical movement of the structures. The use of switches to electronically vary impedance of the parasitic elements through changing the length dimensions of the elements is a practical solution in this scenario as an option.

This work illustrates the use of the new generation RF MEMS switches for the creation of pattern reconfigurable parasitic antennas by using the switch to vary the length and thus the impedance of the parasitic components of the antenna structure. In particular, the new generation of RF MEMS switching devices are able to provide excellent performances in terms of scattering parameters (up to 110 GHz)

and mechanical stability [12] has been used to design a planar microstrip reconfigurable antenna. The preliminary numerical results obtained considering a planar reconfigurable yagi structure are quite promising.

2 Proposed Antenna Design

The proposed structure is a planar yagi antenna composed of one driven element and two parasitic elements printed on one side of the PCB board (see Fig. 1). The antenna structure is simulated on 1.6 mm FR4 substrate of relative permittivity $\varepsilon_r = 4.6$. The cut in the parasitic elements for switch insertion is 0.2 mm and the substrate dimension is 13 × 13 mm. The motivation of using printed antenna structures is that they are cheap owing to their low power consumption and light weight [13]. Moreover, it is particularly suitable for the RF MEMS switches assembly. The active element is a dipole of half wavelength, connected with a subminiature type A coaxial connector (SMA) and the parasitic elements are made to be of equal length with the driven element so that they are resonant and hence have a maximum impact on the beam properties of the designed antenna when activated by the switch [10]. The capability of the parasitic elements to behave as reflectors or directors is derived by use of an RF MEMS switch attached in series at the center and these switches are used to activate or deactivate the reflectors as in [14].

The antenna has been designed to be operating in the X-band microwave frequency band (8–12 GHz), in particular a working frequency of 8 GHz was chosen for the proposed antenna structure, with a wavelength of $\lambda = 17.48$ mm (considering the electrical length in the dielectric material). It is worth noticing that the MEMS ohmic switch used present a broadband behavior up to 100 GHz, however for this kind of

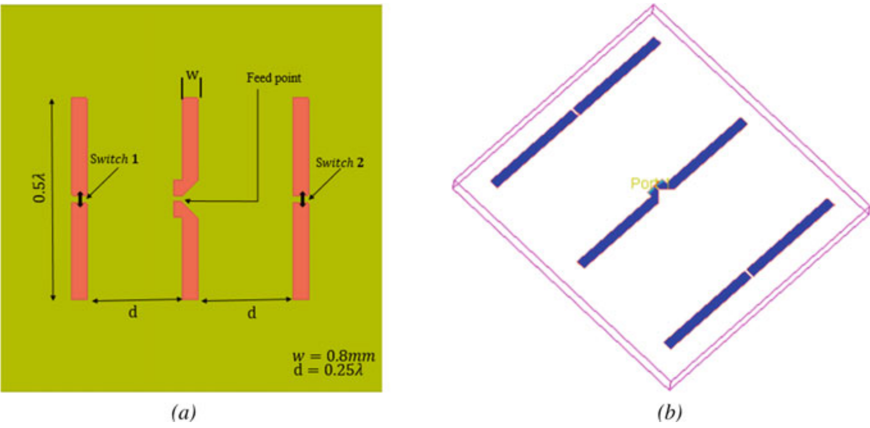

Fig. 1 Antenna geometry of the parasitic yagi antenna on planar surface. **a** Antenna geometry with its dimensions. **b** View of the planar antenna structure

application only the behavior up to 20 GHz, has been reported in Fig. 3c, d. The separation between the antenna elements has an impact on the radiation pattern and was obtained after an optimization procedure to be 0.25λ. The radiation characteristics of the structure were studied before introducing modifications that aid reconfigurability. The geometric characteristics of the antenna structure considered is reported in Fig. 1 and has been numerically assessed by using a commercial software namely ADS from keysight.

3 RF MEMS Switch Performance

Measurements of data depicting the performance of RF MEMS switching devices fabricated at Fondazione Bruno Kessler [12, 15–17] were performed prior to the study. Subsequently the scattering parameters were used to characterize the radio frequency behavior of the devices by importing the data within the Keysight ADS simulation environment. The measurement data included both ohmic and capacitive switching devices that make use of electrostatic actuation with good RF behavior and all show great potential for exploitation in electronically changing the antenna structure resulting in a variation of the antenna beam pattern. A series ohmic switch whose functionality is obtained by electrostatic actuation is used for the purpose of this study and its RF performance are reported below. The switching device's operating mechanism is that the switch is OFF when in OPEN state and this causes the RF signal coming from the input port to be blocked whereas when in CLOSED state, the switch is ON and allows the RF signal to pass with a negligible insertion loss [18].

The schematic cross sections in Fig. 2 shows the typical operation an electrostatically actuated RF-MEMS cantilever ohmic series switch. The pads Act_1 and Act_2 are used to apply the bias voltage between the suspended electrode and the fixed electrode at the bottom. With no bias voltage applied between the terminals as in Fig. 2a, there is a large impedance between the input and output (OFF state) so the RF signal into the switch is reflected.

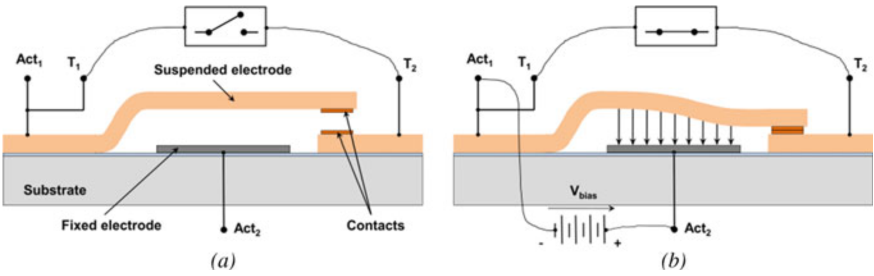

Fig. 2 Schematic cross section of a series ohmic switch utilizing electrostatic actuation, **a** OFF State, when no bias voltage is applied. **b** ON state when actuation voltage is applied [19]

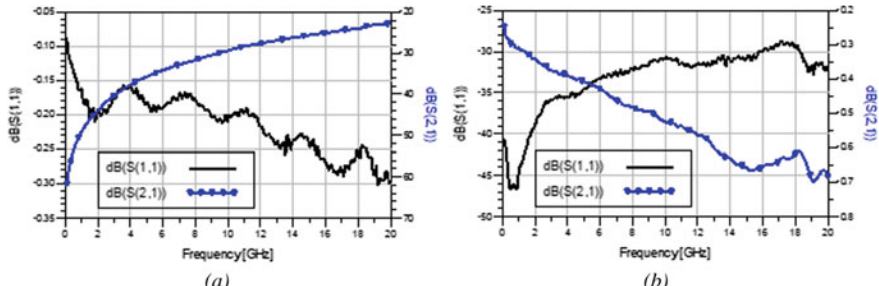

Fig. 3 **a** Measured S-parameters of the ohmic switching device from 100 MHz to 20 GHz in OPEN State showing the reflection (S11) and Isolation (S21). **b** Measured S-Parameters of the ohmic switching device from 100 MHz to 20 GHz in CLOSED State showing the reflection (S11) and transmission (S21)

On the contrary, when a bias voltage that is sufficient to cause actuation is applied between the pads, there is an electrostatic field build up in the device causing the cantilever to collapse onto the contact at the bottom, closing the switch (ON state) and leading to a low impedance between the input and output terminals of the device allowing RF signal to flow through the device [19].When the bias voltage is removed, the cantilever returns to its rest position and the voltage required to cause actuation of the cantilever and return to rest position is 65 V and 50 V respectively.

The scattering parameters (S-parameters) plot of the switch in Fig. 3 shows the RF characteristics of RF MEMS switching device measured from 100 MHz to 20 GHz. The performance in the OPEN state of the switch is reported in Fig. 3a, where S11 represents the reflected power at port 1 and is between −0.16 dB to −0.4 dB. The S21 is the isolation and is better than −20 dB up to 20 GHz.

The CLOSED state performance of the switch is illustrated in Fig. 3b with S11 better than −27 dB up to 20 GHz which is a satisfactory behavior indicating good impedance matching between the RF signal source and MEMS switching device. The S21 indicates the transmission and the loss the RF signal is subjected to when traveling across the device is better than −0.8 dB over the measured frequency range indicating remarkable performance of the switch contact.

The OFF/ON state RF characteristics of the switch shown above are good over the measured frequency and the switching characteristics can be utilized for applications that operate within this range to give a satisfactory performance. The antenna presented in this paper operates at 8 GHz hence with an S11 better than −0.2 dB and S21 better than −30 dB in the switch OPEN state as well as S11 better than −32 dB and S21 better than −0.5 dB in the CLOSED state of the switch, thus guaranteeing a good performance for this scenario.

4 Pattern Reconfiguration with RF MEMS Switches

The mechanism of pattern reconfiguration is described in this section. By switching the ON/OFF state of the RF MEMS switches that have been inserted in series at the discontinuities of parasitic elements, they can be tuned to different length translating into a change in its role of being either a director or reflector leading to alteration in the antenna radiation properties. With the switch in the OFF state, the parasitic strip is an open circuit leading to two strips of equal length that are shorter than that of the driven element. Moreover, it has a capacitive behavior thus acting as a director. Conversely, the parasitic element assumes an inductive behavior and acts as reflector when the switch is turned ON since the two elements of which its composed are short circuited and the induced current in the parasitic elements flows through. Four antenna configurations are obtained while making use of the switches as summarized in Table 1.

When the switches in the two parasitic arms of the antenna are both OFF as in the configuration 1, the parasitic segments act as directors and the antenna behaves like the traditional yagi antenna leading to a bi-directional end fire radiation pattern on the plane of the antenna. In the second configuration, the parasitic element with the ON switch behaves as a reflector causing the RF energy to be radiated back toward the driven element. This results into a uni-directional end fire pattern. The third configuration operates similar to the second one with the radiation pattern in the opposite direction. In the fourth configuration, both parasitic elements are activated by the switches thereby extending their length and act as reflectors, which leads to a broadside radiation pattern. The obtained configurations are useful as the radiation characteristic of the antenna can be altered dynamically to obtain a certain required performance.

The impact of the length and width of the strip lines that make up the active and parasitic elements of the antenna is shown in Fig. 4. The resonant frequency of the antenna depends on the length of the dipole active elements and this is seen by the increase of frequency as the electrical length of the dipole reduces. This is shown in Fig. 4a where L is the length of each monopole and is equal to 0.25λ.

The width of the antenna elements affects the impedance matching characteristics of the antenna depicted by the return loss curves in Fig. 4b where the matching improves with reduction in the strip width. Despite the improvement of the return loss as the width of the strip lines reduces, we need to choose a reasonable value that

Table 1 Switching configurations

	Switch 1	Switch 2	Radiation pattern
CONFIG I	OFF	OFF	Bi-directional end fire
CONFIG II	ON	OFF	Uni-directional end fire
CONFIG III	OFF	ON	Uni-directional end fire
CONFIG IV	ON	ON	Broadside

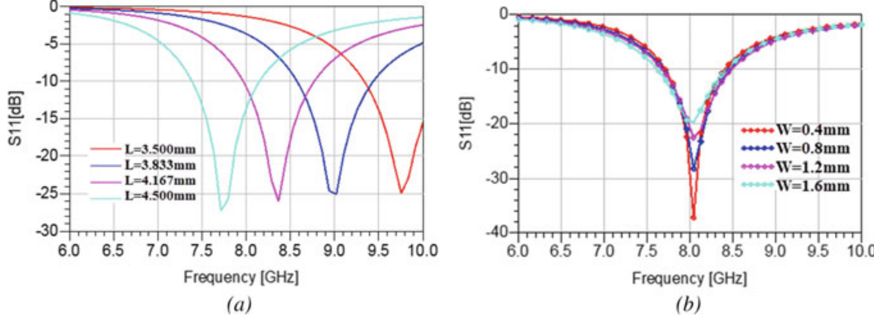

Fig. 4 **a** Variation of antenna return loss characteristics with change in the electrical length of the dipole structure. **b** Impact of the strip width on the return loss characteristics of the antenna

would make fabrication easier. The length of $L = 4.37$ mm and W = 0.8 mm was used in this work and a small size antenna was simulated.

5 Numerical Assessment and Discussion of Results

The proposed antenna structure has been numerically assessed within the Keysight ADS environment by making use of the EM co-simulation feature, as stated above, the measured scattering matrix of the RF MEMS switches, have been inserted in the ADS schematic model for the purpose of obtaining a realistic behavior. It is important to ensure proper impedance matching between the RF source and the antenna and how well this has been achieved is observed from the return loss performance metric for any of the antenna configurations. Figure 5 shows the return loss performance of the antenna in all the obtained configurations.

The return loss for all the configurations is less than -10 dB at 8 GHz indicating good impedance matching to the antenna structure. The configurations 2 and 3%

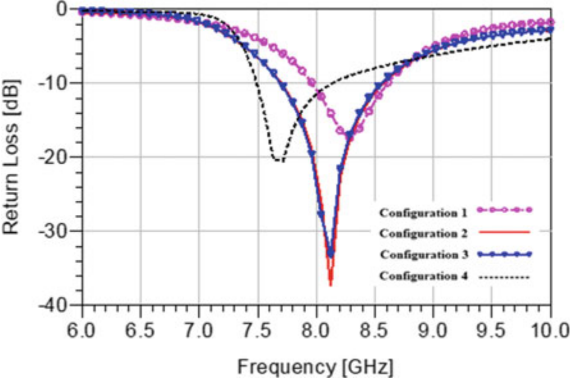

Fig. 5 Simulated return loss of antenna structure in all the four reconfiguration cases

very good return loss below −30 dB at the same resonant frequency. As shown in Fig. 5, the return loss depends on the loading of the antenna and the MEMS device that has been inserted. Hence, care must be taken in the design to choose a switch with insertion loss as low as possible at the intended frequency. There is also some notable frequency shift in the configurations 1 and 4 which may be attributed to the coupling effects of the parasitic reflectors which cause a change in the impedance of the antenna structure. This frequency reconfiguration is the drawback of this design as it leads to reduced bandwidth at the intended operational frequency.

The 2D radiation patterns obtained with different switching configurations are reported in Figs. 6a–d. All the configurations have been obtained with a working frequency of 8 GHz. The obtained radiation pattern in configuration 1 is shown in Fig. 6a and is bi-directional which is expected when the parasitic elements on both sides of the dipole are deactivated and the beam pattern is similar to a standard planar half wavelength dipole. In this arrangement, a gain of 3.6 dBi maximum is obtained in the $\emptyset = 0$ and $\theta = \pm 90$ direction. The results in Fig. 4b, c depict the observed

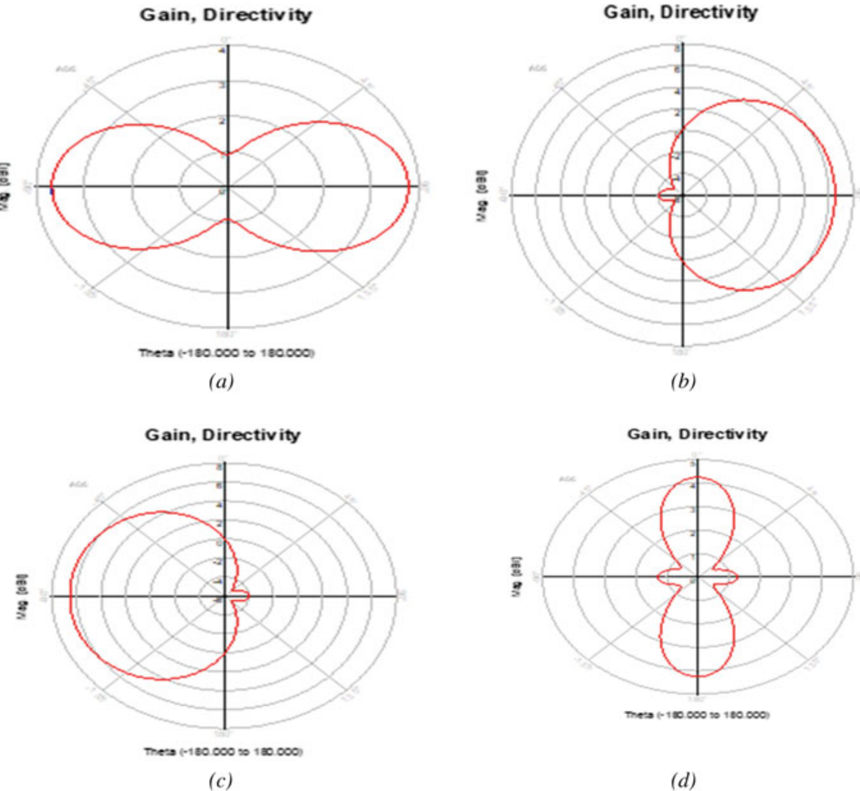

Fig. 6 The 2D radiation pattern for each of the switching configurations, **a** E-field pattern in Configuration 1, **b** Radiation pattern in configuration 2, **c** Radiation pattern in configuration 3, **d** Radiation pattern in the configuration 4 (all switches on)

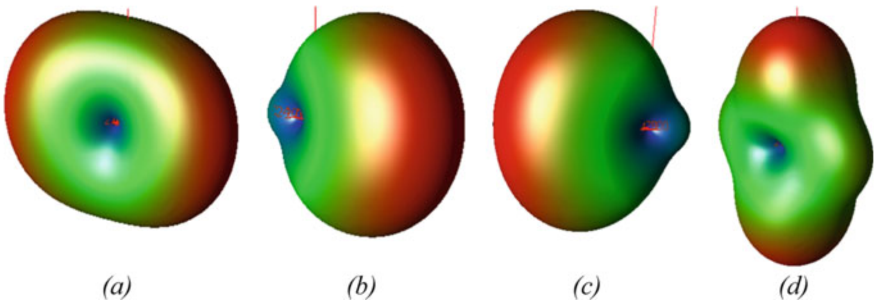

Fig. 7 The simulated 3D beam pattern in all operation modes. **a** When both switches are OFF. **b** Switch 1 ON while Switch 2 is OFF. **c** Switch 1 OFF while Switch 2 ON. **d** Both Switches ON

radiation pattern in configurations 2 and 3 which is an end fire pattern and is a single main lobe. They are complementary to each other due to symmetry of the antenna design and the obtained gain in the two cases is 6.443 dBi and 6.515 dBi respectively.

Figure 6d shows the radiation pattern when both parasitic elements are activated by the switches hence they act as reflectors and a broadside like beam pattern with the main lobes orthogonal to plane of the antenna and a gain of 4.21 (dBi), but a frequency shift of about 100 MHz is observed. The frequency shift is probably due to the coupling effects of the two reflectors. It is worth mentioning that the antenna structure achieves maximum gain when highly directive corresponding to having only one parasitic element activated by the switch.

The 3D visualization of the simulated radiation beam patterns in the obtained operation modes of the antenna at 8 GHz is presented in Fig. 7

The current distributions in the elements of the antenna in the obtained pattern configurations are presented in Fig. 8a–d indicating how a switch in closed state (ON) acts as a short circuit for the current induced in the parasitic elements and as an open circuit between the parasitic elements when the switch is OPEN state (OFF). The current distributions help to show the role of each parasitic element on the antenna performance based on the switch state.

The simulated antenna geometry has been compared with other pattern reconfigurable antennas structures in some of the available studies as presented in Table 2. The antenna presented in the study exhibits acceptable performance based on the simulation results and can be utilized for X band communication applications. Due to the small electrical length of the active and parasitic elements, the antenna structure is compact.

6 Conclusions

The efficacy of RF MEMS switches for the design of pattern reconfigurable antennas has been demonstrated in this paper. The study has been performed on a planar

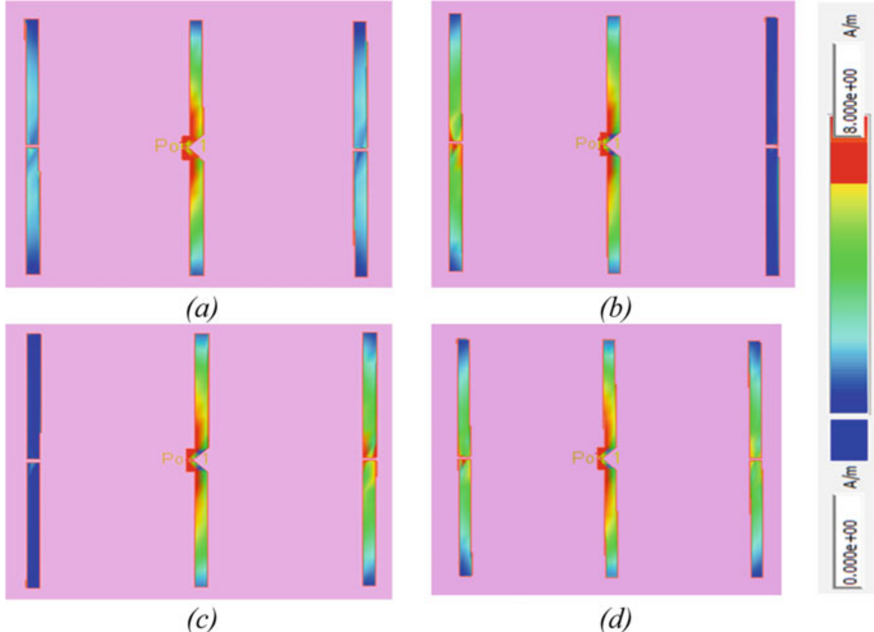

Fig. 8 Current distribution in the antenna elements, **a** In configuration 1 when both Switches are OFF. **b** In Configuration 2. **c** In Configuration 3. **d** In Configuration 4 when both parasitic elements are activated by the switches

Table 2 Comparison of presented antenna structure with some of the literature

Literature	Antenna structure	Switching mechanism	Frequency (GHz)	Beam directions	Antenna size (mm)	Gains (dBi)
[5]	Yagi-Uda	RF MEMS	5.6	$\pm 25^0$	50 × 50	5.7
[2]	Yagi-Uda array	PIN Diode	2.4	0°, 90°, 180°, 270°	44.5 × 37.6	5.9
[20]	Patch	RF MEMS	12.5	±30°	55 × 55	7.5
[14]	Yagi-Uda	PIN photo diode	0.78	±90°	150 × 200	6.3
This paper	Yagi-Uda	RF MEMS	8	0°, ±90°	13 × 13	6.515

microstrip structure based on a Yagi Uda antenna comprising of a half wave dipole as the driven element and two equal length parasitic elements with discontinuities at their center is placed on either side. These tunable elements are chosen to have a total length equal to half the operational wavelength so they be resonant and in turn exert a maximum effect on the radiation pattern. The antenna is simulated in ADS environment and Touchstone files of the switch S-parameters are used to incorporate the experimental ON/OFF characteristics of RF MEMS micro-relays in antenna

simulations. The antenna can be reconfigured to obtain bi directional or end fire patterns by acting on the integrated RF MEM switch states. For all the considered configurations a good return loss less than −10 dB has been obtained. The study has demonstrated the potential of realizing pattern reconfigurable antennas by utilizing RF MEMS switches. Further study is to be aimed at optimizing different antenna structures incorporating RF-MEMS switches to obtain pattern reconfiguration and to move to an experimental prototype.

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Comparative Analysis of Two-Stage Miller Compensated OPAMP in Bulk CMOS and FinFET Technology

Angsuman Sarkar, Ankita Das, and Anindita Das

Abstract This paper aims to compare the performance of miller compensated two-stage operational transconductance amplifier using FinFET and bulk CMOS technologies. Simulations have been performed in SPICE to analyze performance parameters using Predictive Technology Model (PTM) of 16-nm FinFET and 22-nm bulk CMOS from Arizona State University for same supply voltage of 1.1 V, common-mode voltage of 0.6 V and input bias current of 5 μA. The CMOS process showed open loop DC gain of 53.05 dB, Unity Gain Bandwidth (UGB) of 208.62 MHz, Phase Margin of 68.66° and Gain Margin of 14.53 dB, whereas comparative analysis with FinFET demonstrates an improvement of 33.6% in DC gain and 85.93% in Unity Gain Bandwidth with Phase Margin of 80.47° and Gain Margin of 18.10 dB. In terms of Power Supply Rejection (PSR), the FinFET Technology outperformed that of CMOS technology by 1.53 dB.

Keywords Bulk CMOS · FinFET · OPAMP · Open loop DC gain · Unity Gain Bandwidth · Phase Margin · Power Supply Rejection

1 Introduction

In the past few years in VLSI industry, demand for low power and portable electronic devices has increased manifold that requires less power consumption, improved battery life and high bandwidth [1]. Such applications require methods to decrease

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power consumption such as supply voltage scaling, which has proved to be beneficial since it significantly decreases both static and active components of power [2, 3]. However, the lowering of supply voltage gets hindered by the threshold voltage of metal-oxide semiconductor (MOS) transistors, after a particular value is reached. For proper functioning of MOS transistors, the voltage supply must be greater than or equal to the threshold voltage. To achieve low power consumption, rapid CMOS process scaling is favorable for digital circuit design; however it is not suitable for analog circuits because of non-ideal effects resulting in reduced gain, low impedance, etc. [4–7].

The traditional planar CMOS Technology has pushed constantly for shorter channel lengths leading to improvement of various performance metrics such as speed, total power dissipation, etc. However, bulk CMOS devices require high channel doping density so as to restrict short channel effects, resulting in huge transversal electric fields along with electron mobility degradation which gives rise to higher leakage currents, threshold voltage shift, increased mismatch and noise. As a result of threshold voltage shift and device mismatch, current through device and offset voltage of op-amp gets affected. Thus, bulk CMOS may be replaced by novel device structural designs such as FinFETs in the nanometer region owing to improved subthreshold slope, leakage current reduction, better short channel performance and static electricity property, superior mobility and stability [2, 8, 9].

Operational amplifier is one of the basic structural blocks in analog and mixed-signal systems. With increasing demand for low-power mixed-signal circuits, designing analog circuits, for instance, operational transconductance amplifier (OTA) using CMOS technology turns out to be challenging. Moreover, there is a trade-off between bandwidth, gain and consumption of power while designing of op-amp [10]. To overcome the drawback of single stage OTA having limited gain, two-stage OTA is implemented. The first stage differential amplifier provides large gain followed by common-source amplifier stage to allow maximum output swing [11].

This study compares the performance of conventional two-stage OPAMP using PTM for bulk CMOS and high-performance FinFET at 22-nm and 16-nm technology nodes, respectively [12]. Section 2 describes the device structure of FinFET and its properties in detail. Design specifications and parameters for comparison of two-stage OPAMP are given in Sect. 3. Section 4 illustrates the simulated plots and results for op-amp implemented in CMOS and FinFET technologies being operated at 1.1 V supply voltage performed in Spice environment. The concluding remarks are provided in Sect. 5.

2 FinFET Device Structure

Due to extensive technology scaling and requirement of higher packaging density for lesser area, chip performance keeps on degrading and design of circuits in nanometer regime becomes critical as the subthreshold leakage current increases drastically. In planar MOSFETS, with increasing distance from gate, the electrostatic control over

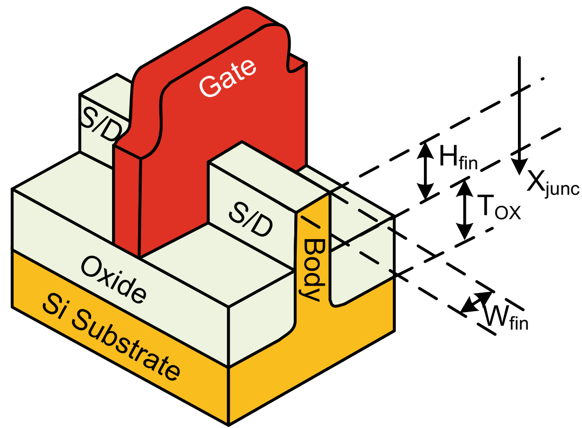

Fig. 1 Three-dimensional schematic of FinFET

the channel goes on decreasing which enhances short channel effects [3]. Thus, FinFET transistors are being preferred over conventional planar bulk CMOS devices in the sub-25 nm region since they use multiple gates for better control over the inversion channel without increasing thickness of gate oxide. As a result, short channel effects are significantly reduced along with lower leakage current. Here, the body comprises a thin fin structure built on an SOI substrate which is kept perpendicular to the wafer surface, for carrying current parallel to the plane of wafer. The fin, surrounded by independently controlled gates, is constructed extremely thin to geometrically inhibit the non-ideal effects [7, 13, 14]. It is also revealed that leakage current due to DIBL is well suppressed and roll-off of a FinFET is well controlled [15].

Though the FinFET architecture demonstrates superior characteristics, they still have to deal with a few issues such as introduction of parasitic capacitances because of the non-planar structure, width quantization effects and process complexity [2]. The unique property of width quantization, due to constraint of constant fin height (H_{fin}), has to be taken care of in analog circuit applications (Fig. 1).

The channel width for a FinFET architecture is represented as follow:

$$W \sim 2\text{H}_{\text{fin}} + W_{\text{fin}} \quad (1)$$

Here, W_{fin} and H_{fin} stand for the width and height of fin, respectively. The height of fin is represented as the distance between top of the fin body and isolation oxide surface. T_{OX} defines the field oxide thickness isolating the gate from the body. The depth of the source/drain junction is given by x_{junc} [16].

In addition, flexibility in designing can be enhanced using multiple fins and smaller fin heights, as taller fins requiring less area may sometimes lead to structural instability. Also, on enlarging channel width, silicon footprint of the chip increases [17]. The advantage of FinFET is that it has better control of short channel effects in the nanometer regime, allowing scaling of transistors at larger extent. Hence,

small-length transistors can achieve a higher intrinsic gain and lesser leakage current compared to bulk CMOS.

3 Design Methodology of Op-Amp

Two-stage operational amplifier comprises a series of I–V and V–I stages shown in Fig. 2. The differential amplifier of first stage converts the differential voltage at input to differential currents, which are then given to a load in current-mirror configuration recovering the differential voltage. A MOSFET in common-source configuration, employed as the second stage, helps in the conversion of this differential input voltage to current. It is finally loaded by a current-sink load, converting the incoming current to output voltage [18].

The first-stage gain (A_{v1}) of two-stage operational amplifier can be calculated as the multiplication of trans-conductance of M2 (g_{mI}) and net output resistance (r_o) at M2 drain terminal. The differential signal applied at the input terminals of the first stage is amplified according to the differential amplifier gain. The benefit of implementing active load transistors in current mirror configuration is that they provide a large output resistance leading to higher differential gain and also convert differential input signal to a single-ended one which acts as input to the second stage [19]. It is given as,

$$A_{v1} = g_{mI}*(r_{o1,2}//r_{o3,4}) \tag{2}$$

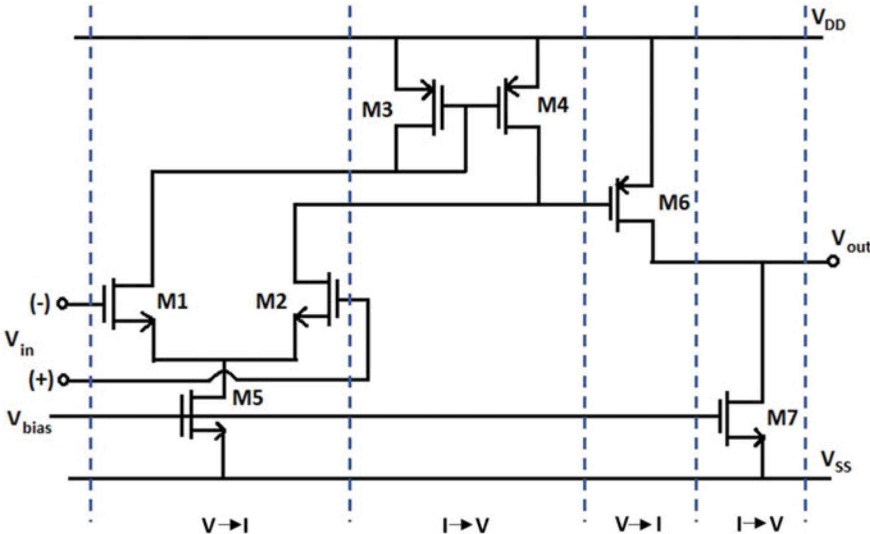

Fig. 2 Two-stage operational amplifier showing V–I and I–V stages

The second stage having common source configuration is used to provide additional gain in the amplifier and higher swing. Here, the gain (A_{v2}) is given by the transconductance of M6 (g_{mII}) multiplied with effective load resistance which consists of the output resistance of M6 and M7,

$$A_{v2} = g_{mII} * (r_{o6} // r_{o7}) \tag{3}$$

Hence, the overall gain (A_v) can be represented by,

$$A_v = A_{v1} * A_{v2} \tag{4}$$

As the op-amp has high input impedance, it draws very little current and acts as isolation buffers which isolate a circuit, disturbing its power to a minimal extent. Furthermore, the close-loop output impedance ($R_{o,closed}$) is almost independent of the open-loop output impedance ($R_{o,open}$) which aids in designing of op-amps having higher gain. This is achieved by increasing the open-loop output impedance, while still keeping the close-loop output impedance relatively low [20, 21].

Output impedance is given by,

$$R_{o,closed} = \frac{R_{o,open}}{1 + \beta A_{v,open}} = \frac{(r_{o1,2} // r_{o3,4})^* (r_{o6} // r_{o7})}{1 + g_{mI} g_{mII} (r_{o1,2} // r_{o3,4})^* (r_{o6} // r_{o7})} \approx \frac{1}{g_{mI} g_{mII}} \tag{5}$$

where $\beta =$ feedback factor and $A_{v,open}$ is the open-loop gain of operational amplifier.

However, the transfer function of an uncompensated two-stage operational amplifier comprises of two poles located below the unity gain frequency given as,

$$p_1 = \frac{1}{R_1 C_1} \tag{6}$$

$$p_2 = \frac{1}{R_2 C_2} \tag{7}$$

where R_1, R_2 are the effective output resistances and C_1, C_2 are the effective output capacitances of first and second stage, respectively. Thus, pole splitting RC miller compensation has been implemented achieving dominant and non-dominant poles, which makes the system to act as a first-order system so as to ensure stability. In this method, a compensation capacitor (C_c) is connected from the output of the first stage to the input of the second stage which also introduces a zero on the right half-plane [18]. The equations for zero and two poles of the compensated operational amplifier are represented as,

$$z_1 = \frac{g_{mII}}{C_c} \tag{8}$$

$$p_1 \cong -\frac{1}{g_{mII} R_1 R_2 C_c} \tag{9}$$

$$p_2 \cong -\frac{g_{mII}C_c}{C_1C_2 + C_1C_c + C_2C_c} \cong -\frac{g_{mII}}{C_1 + C_2} \tag{10}$$

To overcome the disadvantage of the additional right-hand plane zero due to Miller effect, a zero-nulling resistor is used for its elimination [22]. The zero, moved depending on the value of R_z, is given as,

$$z = \frac{1}{(1/g_{mII} - R_z)C_c} \tag{11}$$

The Unity Gain Bandwidth of two-stage op-amp is defined to be approximately [23, 24],

$$\text{UGB} = \frac{g_{mI}}{C_c} \tag{12}$$

For a stable operation we need an optimum phase margin of 60°. It can be shown that if the location of zero is at least ten times greater than unity-gain bandwidth, then to achieve a phase margin of 60°, P_2 must be positioned approximately 2.2 times higher than UGB, given by the below relationships:

$$\frac{g_{mII}}{C_c} > 10\left(\frac{g_{mI}}{C_c}\right) \tag{13}$$

$$|p_2| > 2.2\ \text{UGB} \tag{14}$$

$$C_C > \frac{2.2C_2}{10} = 0.22C_2 \tag{15}$$

4 Simulation Results

For designing of a low power operational amplifier, voltage supply is scaled down to 1.1 V for both technology nodes for easier comparison. The following list describes the input conditions that were considered while designing (Table 1):

Examining the required conditions, it is determined that the best type of configuration will be Unity-gain Buffer where $V_{\text{in-n}}$ has been connected to V_{out} and $V_{\text{in-p}}$ is supplied with V_{CM} (Fig. 3).

Under the same input conditions, comparative analysis has been carried out. The simulation results for two-stage operational amplifier in both bulk CMOS and FinFET technologies are provided in the plots given below (Figs. 4, 5, 6 and 7).

From the above simulation graphs, the values of various design metrics in Bulk CMOS and FinFET technology are provided in Table 2.

Table 1 Input parameters chosen for design

Parameter	Description	Unit	Typical value
V_{DD}	Supply Voltage	V	1.1
V_{CM}	Common Mode Voltage	V	0.6
V_{SS}	Ground Voltage	V	0
C_2	Load Capacitance	fF	500
I_{ref}	Reference Current	μA	5

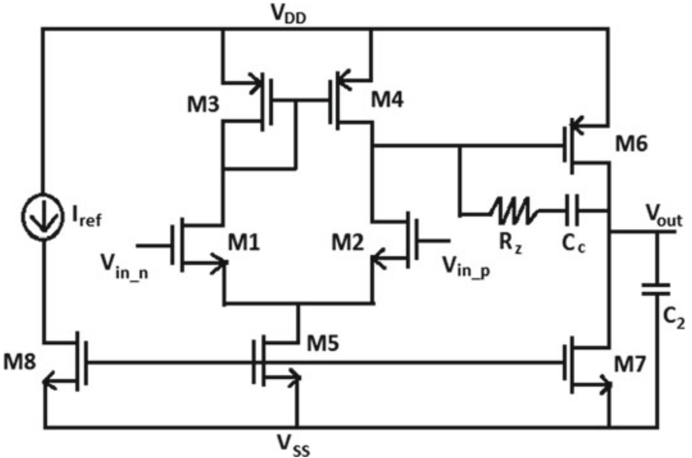

Fig. 3 Basic two-stage op-amp

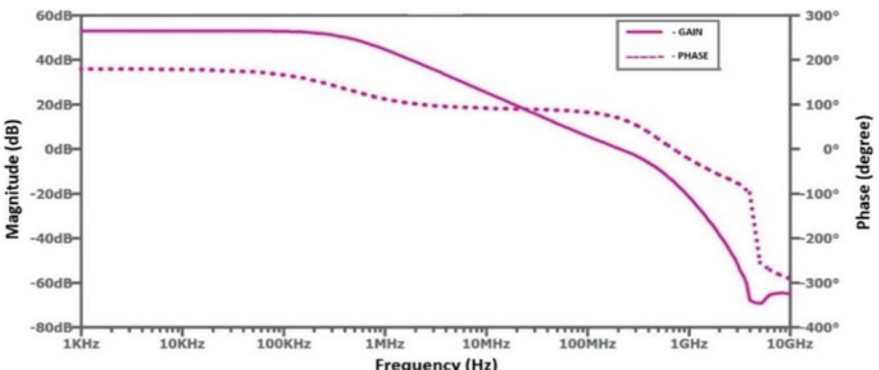

Fig. 4 AC response for two-stage operational amplifier using bulk CMOS technology

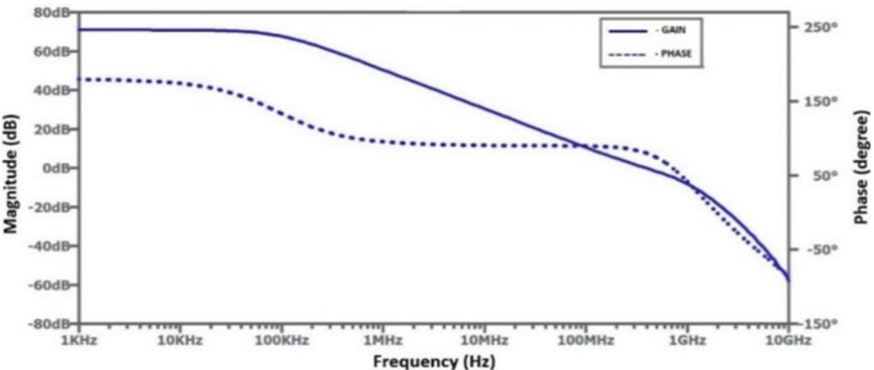

Fig. 5 AC response for two-stage operational amplifier using FinFET technology

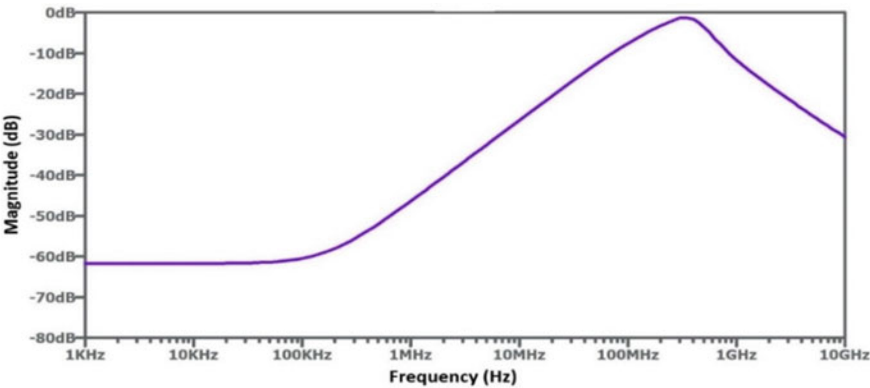

Fig. 6 PSR plot for two-stage operational amplifier using bulk CMOS technology

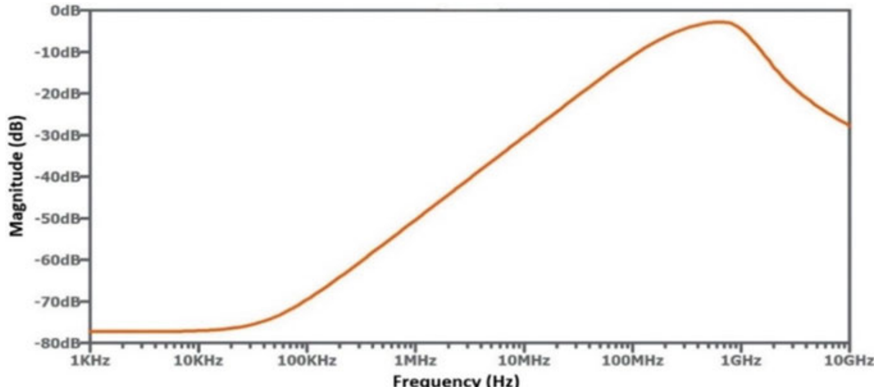

Fig. 7 PSR plot for two-stage operational amplifier using FinFET technology

Table 2 Comparison of performance parameters for two-stage op-amp utilizing bulk CMOS and FinFET

Design Metrics	Specification obtained in bulk CMOS	Specification obtained in FinFET
Process (nm)	22	16
Gain (dB)	53.05	70.88
Unity-gain bandwidth (UGB) (MHz)	208.62	386.81
Phase Margin (degree)	68.66	80.52
Gain Margin (dB)	14.53	18.10
Power Supply Rejection (PSR) at DC (dB)	−61.75	−77.28
Worst PSR (dB)	−1.23	−2.76
Systematic Offset (μV)	540	60

Table 2 shows that, under same input parameter considerations along with same bias current mirroring in each stage, larger gain is observed for op-amp using FinFET compared to conventional CMOS. This is in accordance with FinFET providing higher transconductance in comparison to CMOS, under same DC operating point [24]. It also illustrates that UGB and Phase Margin for FinFET is much higher than bulk CMOS leading to improved speed and stability. Moreover, DC PSR for FinFET is better than that of CMOS as the DC gain itself is higher for the former. In this regard, it is worth mentioning that FinFET has already demonstrated its ability to replace conventional MOSFET devices in digital application and linear radio frequency application [25, 26] primarily owing to its superior scalability, higher transconductance and superior subthreshold slope [27]. In other words, FinFETs can achieve a specific transconductance at a lower inversion level as compared to a bulk MOSFET. The result shown in this paper uncovers the potential of FinFET also for realizing analog amplifier such as two-stage op-amp circuit [28]. The FinFET offers better immunity to Short-Channel Effects (SCEs) and higher transconductance due to the coverage of the channel by three sides (multi-gate architecture) as compared to a conventional MOSFET. Due to this superior gate control ability, FinFET offers lower output conductance (G_{DS}) than a corresponding conventional MOSFET [29, 30]. An enhanced transconductance and reduced G_{DS} translate into higher intrinsic gains for the FinFET. As a result, due to the higher intrinsic gain and lower parasitic capacitances [28–30], the gain and Unity-gain bandwidth product of FinFET-based op-amp is higher than the corresponding conventional CMOS-based op-amp.

5 Conclusion

A two-stage operational amplifier has been designed in 22-nm bulk CMOS and 16-nm FinFET technology whose performances have been examined extensively in this work. Simulation plots illustrate that the FinFET-based op-amp is superior to bulk CMOS in mirroring accuracy, gain, phase margin, unity-gain bandwidth and power supply rejection for same input conditions. At a deeper nanometer regime, performance of CMOS deteriorates due to critical short channel effects while that of FinFET continues to improve at all aspects due to excellent gate control of the channel. Hence, FinFET appears to be the most promising device technology in VLSI industry.

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Performance-Based Comparative Study on Single- and Dual-Gate OTFT: Modeling and Simulation Using TCAD

Srishti Gupta and Manish Kumar Singh

Abstract The study on organic electronics attracted the researcher and the industrialist for its novel features. In this paper, a comparative analysis has been performed for the single- and the dual-gatebased organic thin-film transistors (OTFTs) to examine the performance parameters such as on/off current ratio, subthreshold swing, mobility, and threshold voltage, etc. The analytical modeling and simulation have been carried out with the help of the ATLAS 2D numerical device simulator, and it is observed that the variation in the structural dimension of the OTFT is widely affecting these performance parameters. Furthermore, it is also observed that the reduction in the channel length by 80% (from 50 μm to 10 μm having a step size = 10) leads to an increase in the drive current by 81% in the dual-gatebased OTFT and 80% in the case of single-gatebased OTFTs, respectively, and the variation in thickness of active layer from 60 nm to 20 nm (under the same step size) leads to an enhancement in the on/off current ratio by 99% with the subsequent reduction in leakage current. Decreasing the dielectric thickness from 10 nm to 2 nm (with a step size of 2) leads to an enhancement in these performance parameters. Finally, it is witnessed that the dual-gate OTFT is showing excellent performance over single-gate OTFT, which sanctions to achieve high-speed applications.

Keywords Organic thin-film transistors · Single-/dual-gate OTFT · Performance parameter analysis · TCAD simulation of OFET · Organic semiconductor thickness · Effect of dielectric thickness

1 Introduction

Organic electronics, a modern area to explore electronics-based research, slightly differs from conventional electronics in terms of materials while holding the same goal. An organic thin-film transistor has prime importance based on qualities such as better solution processability, low-temperature fabrication, cheap, light in weight,

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being used in a large area, and easy implementation of the flexible substrates such as glass, plastic, paper, and fiber [1–6]. Due to such excellent features, it is much probable to be utilized in integrated circuits, e-paper, sensors, radio frequency identification (RFID) tag [7–11], light-emitting diode (LED), and flat panel displays. In 1962, Weimer, with an inorganic semiconductor, that is, cadmium sulfide, proposed the idea of a thin-film transistor [12]; after that, many researchers come up with a similar concept but different usages of material, and ultimately in the 1980s, Tsumura, Kudo, and Ebisawa developed an organic transistor over the glass and plastic [13–15]. For the improvement in the operation, different structures have been studied in which a dual-gate organic thin-film transistor (DG-OTFT) came into the picture in 2005 by Cui and Liang [16], which was mainly consisting of two gates. There is a provision to connect these two gates with a common voltage or different voltages. The structure consists of a top gate and dielectric, organic semiconductor, source/drain, and a bottom gate and dielectric, where the bottom gate forms the channel and biasing the top gate increases the conductivity in the channel, moreover, because the extra gate helps in controlling threshold voltage and produces a better result such as high current and on/off current ratio, high mobility, and low subthreshold slope when compared with that of a single gate.

In this paper, with the help of 2D numerical simulator TCAD tools [17], single-gate (SG) and dual-gate (DG), OTFTs performance study is carried out. All the electrical parameters of the OTFT devices are studied and compared with the help of Silvaco ATLAS device simulator. Some significant parameters are mobility, on/off current ratio, threshold voltage, and subthreshold slope. This paper is arranged in four segments, involving an introductory segment 1. Afterward, segment 2 inspects the simulation process of SG and DG devices. The extraction parameter with comparison results is examined in segment 3. Finally, segment 4 includes a summary of the findings.

2 Single-/Dual-Gate Simulation Setup and Extraction of Parameter

Structures of single-gate (SG) as well as dual-gate (DG) OTFTs have been modeled with the help of the TCAD ATLAS Silvaco device simulator. Bottom-gate configuration technology is used to make SG-OTFT here; we considered the bottom-gate top contact structure. The single- and dual-gate OTFT has a channel length and a width of 10 μm and 200 μm, respectively. In the formation of SG-OTFT structure, aluminum (Al) is used as a bottom-gate electrode with 0.02um thickness. Then, Al_2O_3 used as a bottom dielectric with thickness 5.7×10^{-3} μm is deposited on the bottom-gate electrode. A layer of active material pentacene is deposited on the bottom dielectric with 0.03 μm thickness. Then, a layer of source and drain contact of gold material is deposited on the active layer with 10 μm length and 0.02 μm thickness. Figure 1a shows the TCAD simulation of the SG-OTFT structure [1].

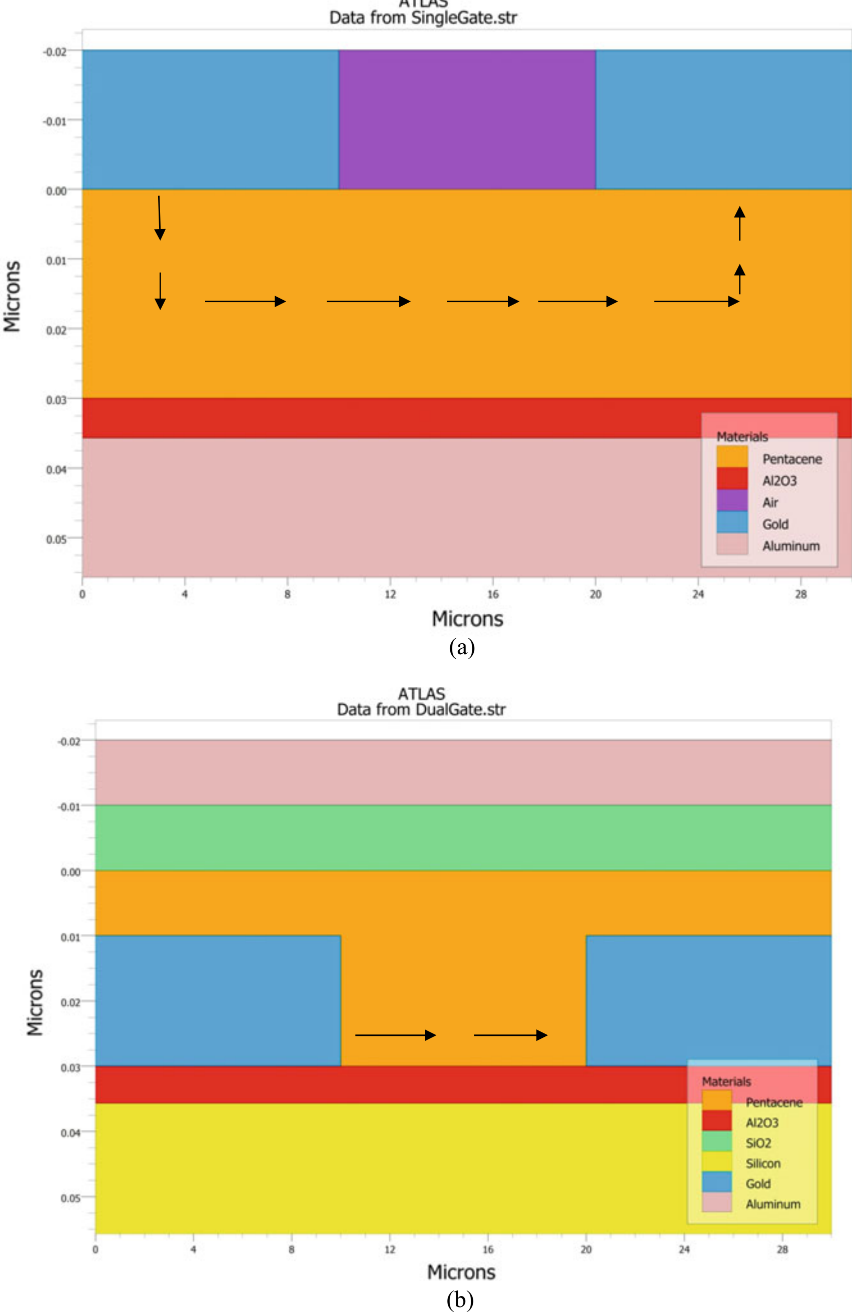

Fig. 1 Simulated structure using TCAD, **a** single- and **b** dual-gate OTFT. The arrows represent the flow of current direction

Table 1 Structural dimension of SG- and DG-OTFTs with the material and thickness

Dimension	Material	Value
Thickness of OSC (t_{OSC})	Pentacene	30 nm
Thickness of bottom dielectric layer (t_{BOX})	Al_2O_3	5.7 nm
Thickness of top dielectric layer (t_{TOX})	SiO_2	10 nm
Thickness of top-gate electrode (t_{BG})	Aluminum	10 nm
Thickness of bottom-gate electrode (t_{TG})	Silicon/aluminum	20 nm
Thickness of S/D contact ($t_{S/D}$)	Gold	20 nm
Channel length (L)	–	10 µm
Channel width (W)	–	200 um

In the formation of DG-OTFT structure, silicon (Si) is used as a bottom-gate electrode of the doping concentration of 10^{17} with 0.02 µm thickness, and aluminum (Al) is used as a top-gate electrode of thickness 0.01 µm. The Al_2O_3 used as a bottom dielectric with a thickness of 5.7×10^{-3} µm is fabricated on the bottom-gate electrode, and SiO_2 is used as a top dielectric with a thickness of 0.01 µm. Further, the deposition of gold layer was done over the bottom dielectric for source and drain electrode having length 10 µm with 0.02 µm thickness each. For the active layer, p-type organic material is used with high mobility, with a thickness of 0.03 µm. Finally, the top layer of the dielectric and the electrode is deposited on the active layer. Figure 1b shows the TCAD simulation of the DG-OTFT structure.

The structural layout related to the fabrication of SG- and DG-OTFT is given in Table 1.

Here, for active pentacene channel, we utilize the Poole–Frenkel mobility model for simulation, which defines the relation and dependency of mobility and electric field; the model is used for single- and dual-gate OTFT, which is stated as

$$\mu(E) = \mu_0 \exp\left[-\frac{\Delta}{\mathrm{KT}} + \left(\frac{\beta}{\mathrm{KT}} - \gamma\right)\sqrt{E}\right] \tag{1}$$

where $\mu(E)$ is the field-dependent mobility, Δ and β are the activation energy and hole Poole–Frenkel constant, respectively, γ is the fitting parameter, E is the electric field, and μ_0 is zero-field mobility, which is analyzed when the drain voltage is zero, and other simulation parameters used during the structuring of devices are listed in Table 2 [1].

The SG- and DG-OTFT parameters such as mobility, threshold voltage, current ratio, subthreshold slope, and transconductance are gathered from transfer characteristics. Drain current characteristics of SG- and DG-OTFT help in modeling and simulation, which are analogous to MOSFETs and determined by linear region ($V_{ds} <= (V_{gs} - V_{th})$) given in equation 2 and saturation region ($V_{ds} > (V_{gs} - V_{th})$) given in Eq. 3 [18].

Table 2 Evaluation parameters used during TCAD simulation

Parameters	Values
Work function of gate (Al)	4.28
Work function of gate (Si)	3.9
Work function of source and drain (Au)	5.1
Silicon doping concentration	10^{17}
Pentacene doping concentration	3×10^{17} cm^{-2}
SiO_2 dielectric constant	3.9
Al_2O_3 dielectric constant	8.5
Permittivity for pentacene	4.0
Holes' activation energy (zero electric field)	1.792×10^{-2} eV
Poole–Frenkel factor for holes	7.758×10^{-5} eV(cm/v)$^{1/2}$
Energy gap at 300 K	2.8
Effective density of state in the conduction band (N_c)	1.0×10^{21} cm^{-3}
Effective density of state in the valance band (N_V)	1.0×10^{21} cm^{-3}

$$I_{ds} = \frac{W}{L}\mu C_i\left(V_{gs} - V_{th}\right)V_{ds} - \frac{V_{ds}^2}{2} \tag{2}$$

$$I_{ds} = \frac{W}{L}\mu C_i\left(V_{gs} - V_{th}\right)^2 \tag{3}$$

where W and L denote the channel width and length, respectively, μ denotes the mobility, C_i denotes the dielectric capacitances per unit area, and V_{th} denotes the threshold voltage. From the slope of the drain current versus gate voltage curve, the transconductance g_m given in Eq. 4 is achieved. Further, it is utilized in extracting the mobility parameter shown in Eq. 5.

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{4}$$

$$\mu = \frac{L \times g_m}{W \times C_i \times V_{ds}}. \tag{5}$$

3 Simulation Results and Discussion

The operation of single- and dual-gate OTFT is examined through a change in dimensional parameters such as channel length, active layer, and dielectric thickness through which electrical parameters such as threshold voltage, subthreshold slope, on/off ratio, transconductance, and mobility are varied accordingly, and the outcomes are computed and matched with the help of TCAD simulation.

3.1 Comparison and Functioning of the Single- and Dual-Gate OTFT

In a comparison of single-gate vs and dual-gate OTFTs, it is noticed that DG-OTFT shows the superior result when the electrical attributes of both OTFT devices are being matched, which are outlined in Table 3. These electrical parameters, which are listed in Table 3, are decided by the usage of the dimensional parameter given in Tables 1 and 2 during the numerical simulation. The transfer curves of both gate-type OTFTs are shown in Fig. 2, which shows the linear regime ($V_{ds} << V_{gs}$) between gate

Table 3 Electrical parameter extraction of single and dual gate

Parameters	SG-OTFT	DG-OTFT
Threshold voltage V_{th}(V)	−0.525	−0.901
Subthreshold slope SS (V/decade)	0.347	0.018
Current on–off ratio$I_{ON/OFF}$	1.0×10^4	1.7×10^{11}
Transconductance g_m (μS)	1.74×10^{-6}	2.36×10^{-6}
Mobility μ (cm^2/VS)	0.0659	0.0710

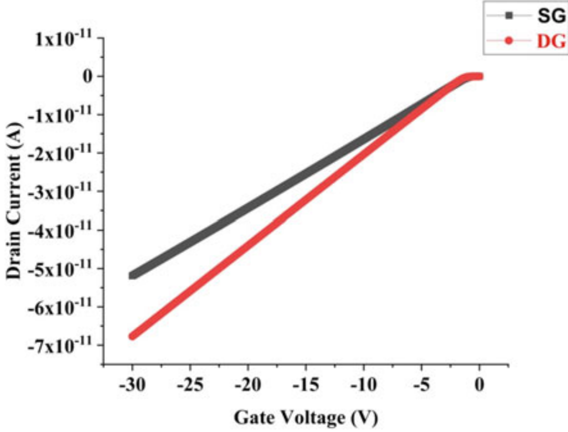

Fig. 2 Single- and dual-gate OTFT transfer curve at −1 V drain voltage

to source voltage and drain current. The relationship between I_{ds} and V_{gs} is defined by Eq. 6.

$$I_{ds} \approx \frac{W}{L}\mu C_i(V_{gs} - V_{th})V_{ds}. \tag{6}$$

Single and dual gate shows slight variation at low gate voltage, but large variation is observed above 5 V gate voltage. Hence, the dual-gate OTFT shows the superior result with an increase in gate voltage due to the top and bottom gate, which helps in the formation of conducting channels between sources and drain where the carriers traveled, unlike path. The breakdown voltage is the threshold voltage at which the initiation of breakdown occurs, as given in Table 3. It is studied that high drive current, steep subthreshold slope (SS), high current ratio ($I_{ON/OFF}$), and mobility in the dual gate are observed when compared to the single-gate OTFT. Furthermore, less leakage current is seen in the dual gate [19].

3.2 Channel-Length Variation in Single- and Dual-Gate OTFT

In this portion, the channel-length shift from 50 μm to 10 μm with a step size of 10 at −1 V drain voltage shows a modification in a different electrical parameter outlined in Table 4. However, there is a slight increment in the ON current related to the drive current, i.e., 81% and 80% in the DG- and SG-OTFTs, respectively, due to a subsequent decrement in the channel length. The drive current (I_{ON}) increases when the path travel by the charge carrier between source and drain is less. As it is well known that the relation between channel length and drive current is inversely proportional, so by decreasing the channel length, the drive current increases [6]. Here, we are reducing the channel length by 80% (from 50 μm to 10 μm) leading to 81% increment (from -1.277×10^{-11} to -6.769×10^{-11}) in DG and 80% increment (from -1.029×10^{-11} to -5.188×10^{-11}) in SG in drive current, which impact the current ratio given in Table 4. Moreover, when the channel length decreases, the improvement in other electrical parameters is observed, such as a high drive current (I_{ON}) and low leakage current (I_{OFF}), which leads to an increase in the current ratio ($I_{ON/OFF}$), which is more in dual gate. Slightly high mobility with steep subthreshold voltage is observed in the dual gate with the variation of channel length by this comparison; we can say the dual-gate OTFT is superior (Fig. 3).

Table 4 Extracted characteristics parameter of SG-/DG-OTFT at the time of channel-length variation

Channel length	Device type	Threshold voltage V_{th}(V)	I_{ON}(A)	I_{OFF}(A)	$I_{ON/OFF}$	Subthreshold Slope SS (V/decade)	Mobility μ (cm^2/VS)	Transconductances g_m(μS)
10 μm	SG	−0.525	-5.188×10^{-11}	-4.912×10^{-15}	1.0×10^{4}	0.347	0.0659	1.743×10^{-6}
	DG	−0.901	-6.769×10^{-11}	-3.962×10^{-22}	1.7×10^{11}	0.018	0.0710	2.366×10^{-6}
20 μm	SG	−0.541	-2.594×10^{-11}	-2.404×10^{-15}	1.0×10^{4}	0.353	0.0669	8.847×10^{-7}
	DG	−0.915	-3.280×10^{-11}	-1.950×10^{-22}	1.6×10^{11}	0.017	0.0688	1.147×10^{-6}
30 μm	SG	−0.549	-1.724×10^{-11}	-1.589×10^{-15}	1.0×10^{4}	0.359	0.0671	5.911×10^{-7}
	DG	−0.920	-2.157×10^{-11}	-1.307×10^{-22}	1.6×10^{11}	0.016	0.0679	7.549×10^{-7}
40 μm	SG	−0.555	-1.289×10^{-11}	-1.186×10^{-15}	1.0×10^{4}	0.364	0.0671	4.432×10^{-7}
	DG	−0.922	-1.605×10^{-11}	-1.011×10^{-22}	1.5×10^{11}	0.016	0.0674	5.618×10^{-7}
50 μm	SG	−0.559	-1.029×10^{-11}	-9.464×10^{-16}	1.0×10^{4}	0.370	0.0671	3.543×10^{-7}
	DG	−0.923	-1.277×10^{-11}	-7.535×10^{-23}	1.6×10^{11}	0.016	0.0670	4.470×10^{-7}

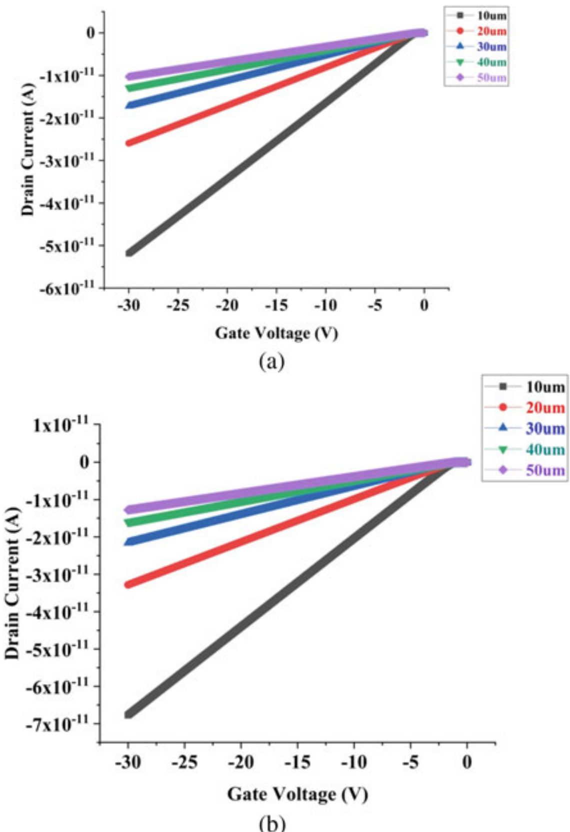

Fig. 3 Variation in drain current due to channel-length variation from 10 μm to 50 μm, **a** single-gate and **b** dual-gate OTFT

3.3 *Active Layer Thickness Variation in Single- and Dual-Gate OTFT*

In this part, variation in active layer thickness from 60 nm to 20 nm with a step size of 10 at Vds $= -1$ V varies electrical parameters summarized in Table 5, which determines that on reducing the thickness, the increment in current is observed. This is due to the reduction in bulk resistance [20]. The transfer curve is shown in Fig. 4. I_{ON} current slightly increases and decreases in the single and dual gate, but the I_{ON} valve is seen more in the dual gate. I_{OFF}, that is, leakage current decreases, so the current ratio increases by 99% in both the gates, and reduction in leakage current is seen more in the dual gate, and subthreshold slope decreases and the slight variation in mobility parameter is observed.

Table 5 Extracted characteristics parameter of SG/DG at the time of active layer thickness variation

OSC thickness	Device type	Threshold voltage V_{th}(V)	I_{ON}(A)	I_{OFF}(A)	$I_{ON/OFF}$	Subthreshold Slope SS (V/decade)	Mobility $\mathscr{M}$ (cm^2/VS)	Transconductances g_m (μS)
20 nm	SG	−0.571	-5.302×10^{-11}	-2.232×10^{-18}	2.3×10^7	0.049	0.0682	1.804×10^{-6}
	DG	−0.943	-6.768×10^{-11}	-2.287×10^{-24}	2.9×10^{13}	0.036	0.0711	2.370×10^{-6}
30 nm	SG	−0.525	-5.188×10^{-11}	-4.912×10^{-15}	1.0×10^4	0.347	0.0659	1.743×10^{-6}
	DG	−0.901	-6.769×10^{-11}	-3.962×10^{-22}	1.7×10^{11}	0.018	0.0710	2.366×10^{-6}
40 nm	SG	−0.484	-5.099×10^{-11}	-3.571×10^{-14}	1.4×10^3	0.846	0.0641	1.696×10^{-6}
	DG	−0.873	-6.763×10^{-11}	-1.816×10^{-19}	3.7×10^8	0.036	0.0708	2.361×10^{-6}
50 nm	SG	−0.444	-5.028×10^{-11}	-9.571×10^{-14}	5.2×10^2	1.143	0.0627	1.658×10^{-6}
	DG	−0.832	-6.767×10^{-11}	-2.214×10^{-16}	3.0×10^5	0.108	0.0707	2.358×10^{-6}
60 nm	SG	−0.406	-4.968×10^{-11}	-1.592×10^{-13}	3.1×10^2	1.321	0.0615	1.627×10^{-6}
	DG	−0.801	-6.765×10^{-11}	-6.717×10^{-15}	1.0×10^4	0.315	0.0706	2.354×10^{-6}

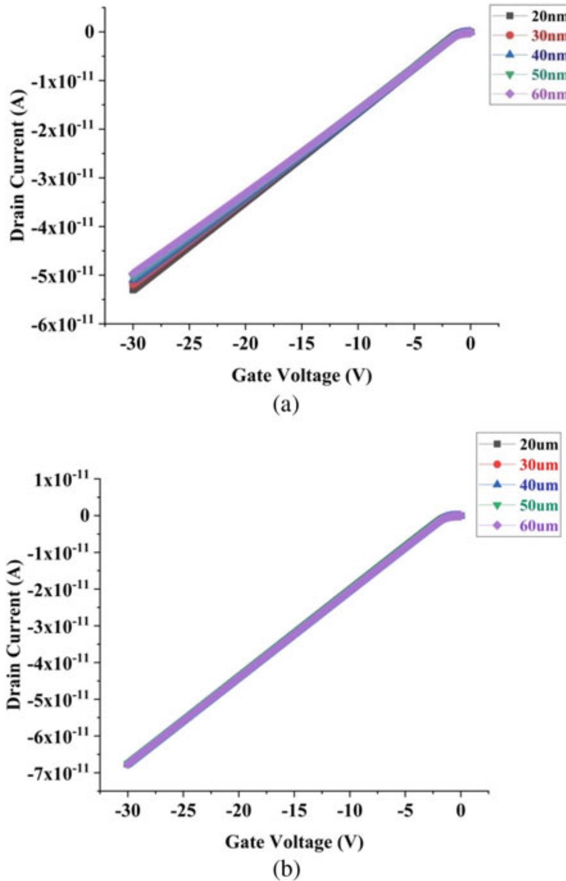

Fig. 4 Variation in drain current due to active layer thickness variation from 10 to 50 nm, **a** single-gate and **b** dual-gate OTFT

3.4 Dielectric Thickness Variation in Single- and Dual-Gate OTFT

In this section, it is shown how variation in thickness of dielectric from 10 nm to 2 nm with a step size of 2 affects the electrical characteristics at $V_{ds} = -1$ V. It is examined by reducing the dielectric thickness of Al_2O_3, that is, the bottom dielectric thickness in single- and dual-gate increases, the current and transfer curve is shown in Fig. 5, $I_{ON/OFF}$ ratio increases by 95.2% in the dual gate and 92.0% in the single gate, and mobility increases in the dual gate but reduces in a single gate because of the high slope of the transfer curve. The main cause is the high electric field due to low dielectric thickness, which further helps in the increment in drain current. The current ratio and mobility of the dual-gate OTFT are more in contrast to those of the single gate, leakage current also reduces [21], and other characteristics parameter is given in Table 6.

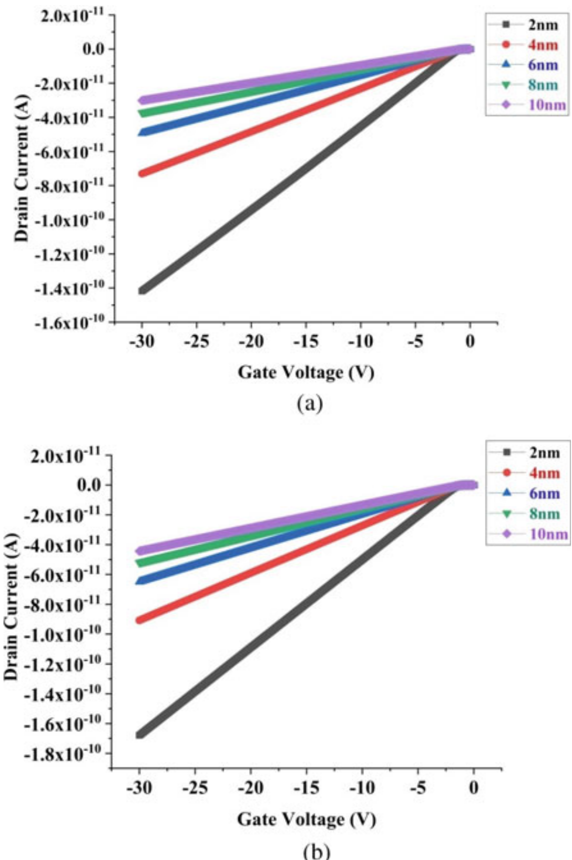

Fig. 5 Variation in drain current due to dielectric thickness differs from 10 to 2 nm, **a** single-gate and **b** dual-gate OTFT

4 Conclusion

The respective performances of single- and dual-gate OTFTs based on pentacene have been analyzed. We observed that the dual-gate OTFT shows relatively improved results than the single gate by varying different structural dimensions such as channel length, active layer, and dielectric thickness. The respective changes in the performance parameter were analyzed by numerical simulation, which exhibits that lower channel length provides a high drive current, and the active layer should be low to achieve a high current ratio and limit the leakage current. Besides this, the low dielectric thickness is liable to increase the current ratio. The performance analysis based upon such study will be much supportive in the formation of better and high-speed devices in the various future applications.

Table 6 Extracted characteristic parameter of SG/DG-OTFT at the time of dielectric thickness variation

Dielectric thickness	Device type	Threshold voltage V_{th}(V)	I_{ON} (A)	I_{OFF} (A)	$I_{ON/OFF}$	Subthreshold slope SS (V/decade)	Mobility $\mathscr{M}$ (cm^2/VS)	Transconductances g_m (μS)
2 nm	SG	−0.611	-1.418×10^{-10}	-2.942×10^{-15}	4.8×10^4	0.284	0.0624	4.701×10^{-6}
	DG	−1.021	-1.679×10^{-10}	-1.773×10^{-22}	9.4×10^{11}	0.017	0.0716	5.893×10^{-6}
4 nm	SG	−0.563	-7.301×10^{-11}	-3.947×10^{-15}	1.8×10^4	0.318	0.0649	2.445×10^{-6}
	DG	−0.951	-9.074×10^{-11}	-2.770×10^{-22}	3.2×10^{11}	0.017	0.0713	3.178×10^{-6}
6 nm	SG	−0.519	-4.93×10^{-11}	-5.094×10^{-15}	9.6×10^3	0.352	0.0661	1.660×10^{-6}
	DG	−0.893	-6.497×10^{-11}	-4.193×10^{-22}	1.5×10^{11}	0.018	0.0709	2.271×10^{-6}
8 nm	SG	−0.478	-3.737×10^{-11}	-6.376×10^{-15}	5.8×10^3	0.387	0.0668	1.259×10^{-6}
	DG	−0.845	-5.208×10^{-11}	-6.427×10^{-22}	8.1×10^{10}	0.019	0.0706	1.817×10^{-6}
10 nm	SG	−0.437	-3.010×10^{-11}	-7.786×10^{-15}	3.8×10^3	0.422	0.0673	1.015×10^{-6}
	DG	−0.802	-4.344×10^{-11}	-9.711×10^{-22}	4.5×10^{10}	0.019	0.0703	1.545×10^{-6}

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Structural and Morphological Properties of Indium-doped Titanium Dioxide Nanoparticles Synthesized Using Sol–gel Process

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Abstract In this paper, we have investigated undoped and indium-doped titanium dioxide (TiO_2) nanoparticles prepared using sol–gel method. The aim of this work is to analyse the effect of indium incorporation on the structure and morphology of the materials. X-ray diffraction (XRD) pattern reveals a significant influence of In-doping on crystallinity and average grain size of the TiO_2 nanoparticles. The morphology of the nanoparticles analysed using transmission electron microscopy (TEM) and scanning electron microscopy (SEM) images confirms the formation of spherical- and triangular-shaped nanoparticles with large surface area. Further, study of TEM images confirmed the obtained XRD results. Moreover, X-ray photoelectron spectroscopy (XPS) and electron diffraction spectroscopy (EDS) approve the electronic states and composition of all different chemicals existing in the samples. All the results are found and verified with the literature.

Keywords Sol–gel · Metal oxide · Nanoparticles · Doping · Morphology

1 Introduction

Titanium dioxide (TiO_2) has attracted great interest among researchers as it has excellent properties which make it suitable for a wide range of applications such as photocatalysis, environmental pollution and photovoltaic [1–4]. Generally, introduction of

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dopant atoms of proper oxidation state into any semiconductor material causes modification of properties which depends on the distinction in the estimation of ionic radii of dopant particles [5]. Doping also affects the formation of donor and/or acceptor levels, resulting in the change in the carrier concentration and semiconducting properties of the materials [6]. Additionally, chemical stability can also be improved, and therefore, doping of suitable foreign atoms into TiO_2 presents wonderful avenue to enhance its functionality. Indium is considered as one of the promising materials due to its exceptional properties like non-toxicity, cost effectiveness, high mobility and variable oxidation states [1]. Also, it can reduce recombination of carriers and produce large number of free carriers due to the presence of d orbitals in the outer shell. So, in this work, we have prepared pure and doped TiO_2 (1at.%, indium) nanoparticles using sol–gel technique to investigate the structural and morphological properties of the materials. Thereafter, the samples were characterized and their observations were studied and discussed.

2 Experimental Procedures

Titanium(IV) isopropoxide ($Ti(OC_4H_9)_4$, TTIP, 97%) and indium(III) chloride ($InCl_3$), ethyl alcohol, de-ionized (DI) water and concentrated HCl (ACS reagent, 37%), were bought from Sigma-Aldrich Co. Ltd. and utilized without additional purification. At room temperature, 0.083 gm of $InCl_3$ powder was mixed with 2.5 mL ethyl alcohol and stirred continuously at 800 rpm until it got dissolved properly. Then, TTIP (0.75 mL) was added drop-wise to the solution followed by addition of concentrated HCl solution to maintain the acidic nature of the solution. The resulting solution was then stirred continuously for an hour and the homogeneous solution was kept undisturbed for 1 day at ambient condition to form thick gel. It was then dried accordingly at 100 °C and pulverized to powder. The obtained materials were further calcined at 400 °C for 2 h and triturate in an agate mortar to get the In-doped TiO_2 nanoparticles. Pure TiO_2 has been prepared using the technique mentioned in Ref. [7]. The chemical reaction involved and their resulting by-products in the synthesis process of pure TiO_2 are:

$$R_1O\text{–}\overset{|}{\underset{|}{Ti}}\text{–}OR_1 + R_2\text{–}OH \leftrightarrow R_2O\text{–}\overset{|}{\underset{|}{Ti}}\text{–}OR_2 \leftrightarrow HO\text{–}\overset{|}{\underset{|}{Ti}}\text{–}OH \leftrightarrow \text{----------------} \leftrightarrow nTiO_2 + H_2O.$$

In case of indium doping end products are $O\text{–}\underset{\underset{In}{|}}{Ti}\text{–}O$, $Cl_2\uparrow$ and H_2O, where R_1 and R_2 are carboxyl groups.

3 Results and Analysis

3.1 X-ray Diffraction (XRD) Investigation

The study was carried out with X′Pert[3] PANalytical instrument and the peak positions were compared with the joint committee on powder diffraction standards (JCPDS) datasheet (89-4921). The intensity versus 2θ graph representing X-ray diffraction of as-synthesized pure and doped titania particles is shown in Fig. 1. Pure TiO_2 has been confirmed as anatase phase with the space group $I4_1$/amd. Various peaks can be observed in both doped and undoped which correspond to crystal planes at (101), (004), (200), (211), (204), (220) and (215), respectively. The doped material exhibits a decrease in intensity and right shift with respect to pristine counterpart. XRD pattern could not reflect the presence of indium, as doping percentage is very small, whereas increase in indium concentration leads to the appearance of the highest intensity peak of In_2O_3 at 31° which can be seen in inset image of Fig. 1. Also, it can be observed that the width of the peaks is slightly larger as compared to pristine, which illustrates the shrink in crystal size. The parameters calculated from XRD analysis are shown in Table 1. The lattice parameters of the pristine TiO_2 are larger compared to the doped sample which verify the slight shift in positions of the diffraction angle and propose the possibility of substitutional doping [8]. However, ionic radius of indium is larger compared to titanium, so substitutional doping is hardly possible. Hence, it is reasonable to say that indium is present mostly on the surface of the synthesized material. The average crystal size (*D*) of the particles can be calculated mathematically from the diffraction peaks using the Debye–Scherrer formula [9]. The average crystallite size of pure form appeared to be above 11 nm, and that of doped one is 7.4 nm.

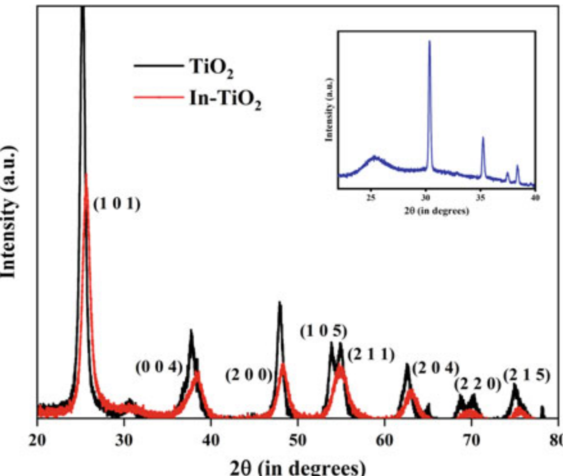

Fig. 1 Intensity versus 2θ graph of pure and In–TiO_2 nanoparticles

Table 1 Lattice boundaries (a, b, c in Å), cell volumes (V) and crystal sizes (D) of the synthesized materials

Parameters	Pure TiO_2		In–TiO_2	
	This work	Reported	This work	Reported
$a = b$	3.792	3.788[b]	3.769	3.769[a]
c	9.515	9.516[b]	9.386	9.474[a]
V (Å)^3	136.93	136.5[b]	133.34	134.4[a]
D (nm)	11	12.6[b]	7.4	8.8[b]

[a]Ref. [9], [b]Ref. [1]

3.2 TEM and EDS Analysis

The TEM micrographs of pristine and doped metal oxides at scale of 20 nm and 10 nm are shown in Fig. 2a–d. It can be seen that pure nanoparticles (Fig. 2a, b) are uniform, spherical in shape. The controlled hydrolysis in the synthesis process has resulted in the formation of uniform-shaped nanoparticles [1]. Similarly, In-doped TiO_2 also has the uniform shape as displayed in Fig. 2c, d, but the particle diameters are found to be smaller. The average particle sizes are calculated using ImageJ software. The mean sizes are observed to be 10 nm and 7 nm for pure and In-doped TiO_2 nanoparticles, respectively. Even, the selected area electron diffraction

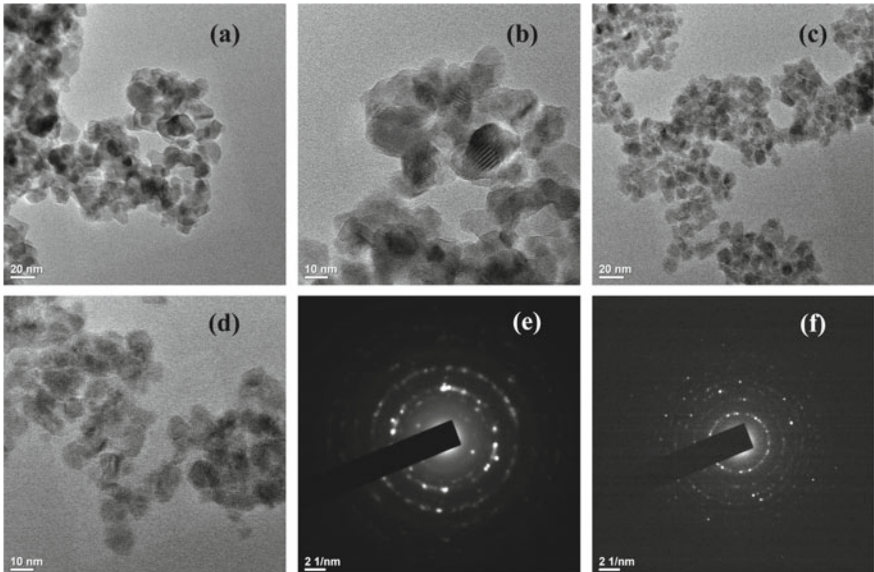

Fig. 2 TEM micrographs, **a** 20 nm scale pure TiO_2, **b** 10 nm scale pure TiO_2, **c** 20 nm scale In-doped TiO_2, **d** 10 nm scale In-doped TiO_2, **e** SAED of pure TiO_2 and **f** SAED of In-doped TiO_2

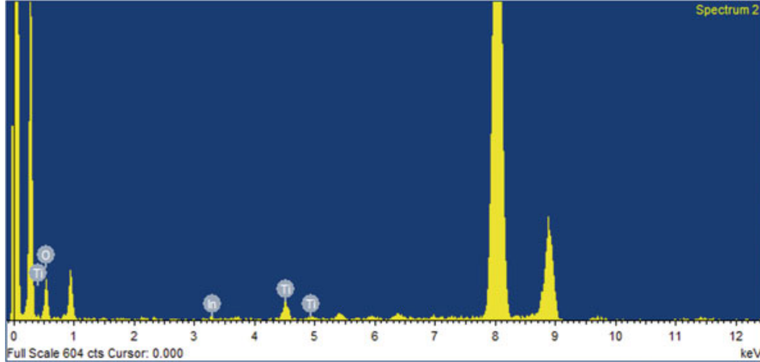

Fig. 3 EDS spectra of In-doped TiO_2 nanoparticles

pattern (SAED) images in both the cases (Fig. 2e, f) are showing concentric rings with bright spots, which signifies the polycrystalline nature of the particles. Also, the crystal planes and crystallinity as observed from SAED pattern are same as found from XRD results. The chemical composition of any material and their stoichiometry can be investigated using EDS analysis. It can be seen from the EDS spectra of In-doped TiO_2 (Fig. 3) that only peaks of titanium (Ti, 28.2%), oxygen (O, 71%) and indium (In, 0.8%) are present. The absence of any other extra peak indicates that the material is free from impure compound. This further assures the successful fabrication.

3.3 SEM Assessment

The size and morphology of the as-synthesized nanoparticles can be studied by SEM characterization. Figure 4a–b shows the SEM micrographs of pure and In-doped TiO_2 at 10 μm scale. It can be seen that a large numbers of small nanoparticles present in both the cases except few very large agglomerated structures. Altogether, these

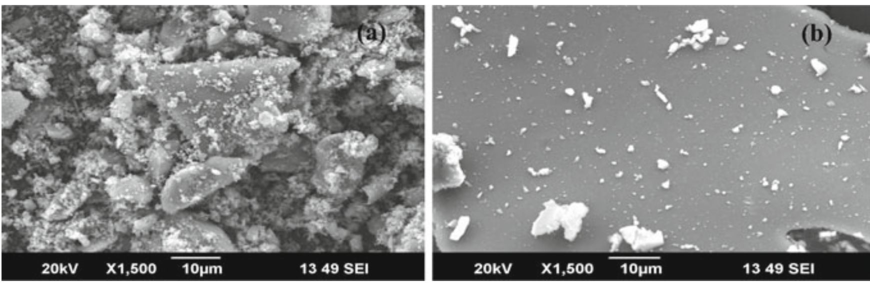

Fig. 4 SEM micrographs of **a** pure TiO_2 and **b** In-doped TiO_2

are dispersed nanoparticles with varying geometry. The presence of mesoporous structure is attributable to the development and agglomeration of nanoparticles [1]. The significant influence of doping on the surface structure is clearly visible. The doped nanoparticles are small in size and the presence of agglomeration is visible due to the smaller sizes.

3.4 Fourier Transform Infrared Spectroscopy (FTIR) Analysis

This is used for identification of bonds and their nature in any materials**.** As can be seen from Fig. 5, the peak below 500 cm^{-1} corresponds to the Ti–O bending mode. The peaks near 1600 cm^{-1} and 2300 cm^{-1} are because of carbon and its associates present in the materials, which may come from the ambient environment. The stretching and bending modes of a hydroxyl group (−OH) on the surface of titania are identified from the downward peaks present near 1500, 3700 and 3800 cm^{-1}. Indium incorporation has made a change in intensity of the transmittance value but peaks remain on the same wave number as pristine TiO_2. The rise in intensity after doping signifies the increase in density of functional group. It also affirms the structural changes due to doping. The absence of any peak of indium bond indicates that the doping is not interstitial.

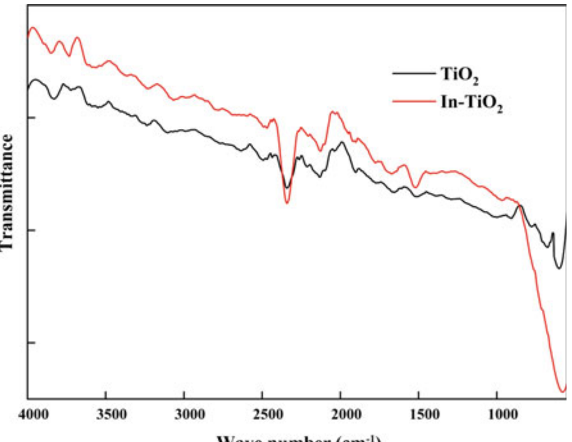

Fig. 5 FTIR spectra of pure and In-doped TiO_2

3.5 XPS Analysis

It has been employed to adjudicate the chemicals present and study their electronic states. The observed spectra of each element present in pure and indium-doped TiO_2 are presented in Fig. 6a–d. The peak positions in terms of binding energy (eV) are mentioned and compared with the reported results in Table 2. The presence of In-3d state confirms the presence of indium which could not be confirmed from XRD and TEM analysis. Firstly, it can be observed there is a significant shift in binding energy for each element in the doped oxide. The higher electronegativity of indium makes the system electron deficient which made the shift in case of Ti and O towards higher binding energy range [10]. The peak for carbon at ~283.29 eV and 286.54 eV is due to (C–C) and C=O bond, respectively. The existence of carbon might be due to contaminant on the repository as the presence of the carbon was not detected in EDS analysis. In case of doped titania, an extra peak of Ti 2p states at 450.84 eV can be seen which is not present in the pure compound, that may be accredited to the existence of lower oxidation state of Ti because of doping. The peaks at 457.06 ($2p^{3/2}$) and

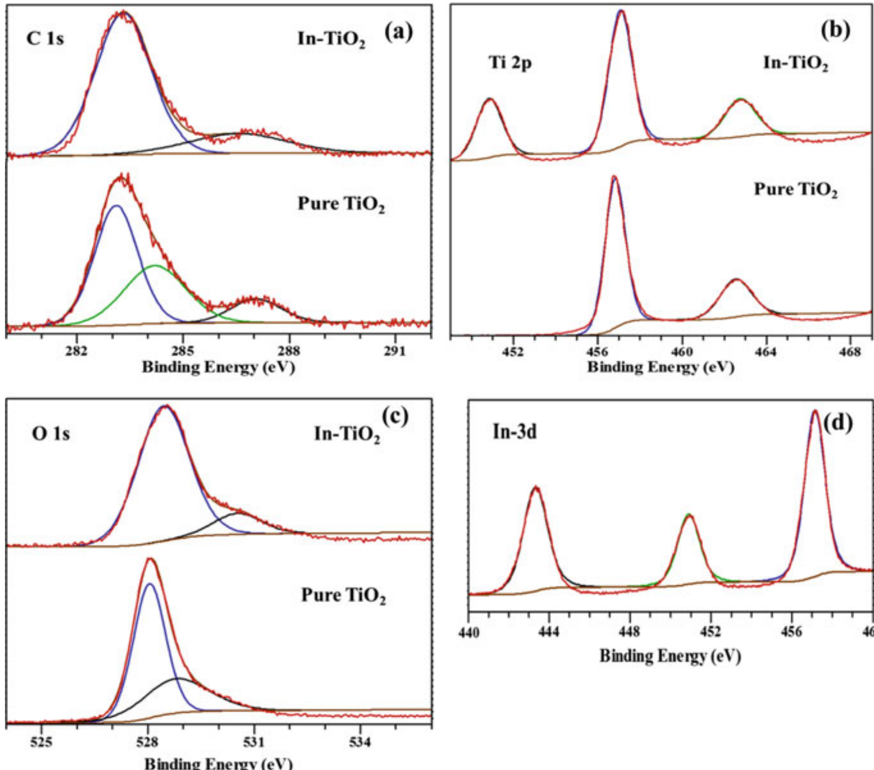

Fig. 6 **a**–**d** XPS spectra C, Ti, O and In present in pure and In–TiO_2

Table 2 Peak positions of elements in terms of binding energy obtained from XPS spectra of pure and In-doped TiO_2

Element	Pure TiO_2 (Binding Energy in eV)		In–TiO_2 (Binding Energy in eV)	
	This work	Reported	This work	Reported
C 1s	283.105, 284.26, 287.05	284.4[b]	281.94, 283.29, 286.54	282.32, 284.6, 286.64[a]
Ti 2p	456.82, 462.53	458.3, 464[c]	450.84, 457.06, 462.75	458.6, 464.3[a]
O 1s	528.05, 528.78	529.5[c]	528.44, 530.53	528.3, 531.2[a]
In 3d	–	–	443.32, 450.89, 457.12	443.8, 451.3[a]

[a]Ref. [1], [b]Ref. [2], [c]Ref. [6]

462.75($2p^{1/2}$) validate the Ti^{4+} state in the compound. The height of peak depends on the Coster–Kronig effect [11]. The O 1s spectrum is comprised of two peaks at 528.44, 530.53. The primary peak at 528.44 is attributed to (O^{2-}) while the peak at 530.53 is due to free (OH^-) hydroxyl groups. The peaks at 443.32 and 450.89 are representing $3d^{5/2}$ and $3d^{3/2}$ of In^{3+} peaks present in the form of In_2O_3, respectively. The peak at 457.12 eV is due to loss features of $3d_{3/2}$ spin–orbit component for indium metal.

4 Conclusions

The impact of indium doping on the structural and morphological characteristics of TiO_2 is systematically studied by comparing the results with the pristine TiO_2. The results depict that indium is an efficacious dopant which could hold the anatase crystal phase of TiO_2. XRD spectra revealed that crystallinity decreases due to replacement of Ti with In^{3+}. The formation of small-size particles and the mesoporous structures after doping are witnessed clearly from TEM and SEM images. The successful synthesis of the compounds and surface electronic states are observed from XPS analysis. Further, the formation of undoped and doped titania and the bonds present in the samples are analysed from FTIR analysis. Although, traces of carbon can be seen from XPS and FTIR spectra due to contaminant present in the holder, but EDS spectr confirm the absence of any unwanted chemicals in the synthesized powdered materials.

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Review of Emerging Tunnel FET Structures

Urmila Bag and Brinda Bhowmick

Abstract Tunnel field effect transistor (TFET) is considered as the probable successor of traditional MOSFET and has gained lots of concentration for ultralow-power application because of lower OFF current and steep switching mechanism. Instead of using thermionic conduction like MOSFET, it operates under gate-controlled band-to-band tunneling mechanism. This paper reviews different structures of TFET, modeling available for design and parameters like speed, I_{ON} /I_{OFF} ratio, power consumption, subthreshold swing, etc., which replaces the conventional MOSFET for greater efficiency.

Keywords Band-to-band tunneling · MOSFET · Subthreshold swing · Thermionic conduction · TFET

1 Introduction

Ongoing downscaling of the metal oxide semiconductor field effect transistors (MOSFETs) dimensions (nanometer range) introduces severe short channel effects (SCEs) like punch-through, drain-induced barrier lowering (DIBL), threshold voltage (V_T) roll-off, etc., are the reason for increasing leakage current. Main constraint of conventional MOSFETs to a minimal inverse subthreshold slope of $S_{\min} = \frac{KT}{q}\ln(10) = 60$ mV/dec (at 300 K) is a major barrier to further reduce the operational voltage because this indicates a minimal voltage range needed to achieve a certain I_{ON}/I_{OFF} ratio. In this situation the tunnel FET technology suits best for the low-power application.

Tunnel FET is an asymmetrical p-i-n device, where gate is the controlling terminal, operated in reverse biased condition. Instead of using thermionic conduction of carrier like MOSFET, it operates under gate-controlled band-to-band tunneling (BTBT) mechanism. Though one of the major limitations of tunnel FET is low ON current (I_{ON}) as compared to ITRS requirement, the biggest benefits of using

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TFET over MOSFET are that at room temperature it exhibits subthreshold swing less than 60 mV/dec. To elevate the I_{ON}, instead of using Si, different materials at source or channel or drain region and several heterojunction tunnel FET structures are promised [1, 2]. Besides, high-k materials as a gate dielectric are also used to reduce the gate leakage and increase the ON-state current significantly. However, there are compatibility issues between polysilicon gate and high-k dielectric due to phonon scattering [3] and Fermi level pinning [4]. By using metal gate in place of polySi gate, this incompatibility can be overthrown [5].

Furthermore, at both high +ve and −ve applied gate voltages, ambipolar conduction of current is another headache. In order to promote the overall characteristics of tunnel FETs, researchers have proposed several structural and material modifications; a few important structures include double-gate (DG) tunnel FET [6], circular-gate TFET [7], dual material gate TFET [8], heterojunction TFET [9], ultrathin body TFET [10], cylindrical-gate TFET [11], PNPN TFET [12], PNIN TFET [13], gate–drain underlap TFET [1] and heterogate dielectric TFET [1]. Instead of using silicon as channel material, materials like Ge TFET [2], InAs TFET [2] and nanoribbon TFETs [14] have also been studied for better performance of TFET.

2 Novel TFET Structure to Boost On Current (I_{ON}) and for Ultralow-Power Applications

Toshio Baba developed tunnel transistor in 1992 by, as one of the ideal substitutes to the traditional MOSFET based on its low subthreshold swing, low OFF current, high I_{ON}/I_{OFF}, efficiency to work on subthreshold and superthreshold region.

2.1 Surface Tunnel Transistor

A3-terminal tunnel device: surface tunnel transistor (STT) was developed by Toshio Baba in 1992. The STT structure is similar to Si-MOSFET that can operate in extreme small dimensions with gate lengths of less than 10^{-4} nm at 300 K. The surface tunnel device has an n^+-i-p^+ diode structure, with a separated gate terminal, which control tunneling mechanism. The basic difference of STT from the conventional FETs is that the doping polarity of the drain terminal and source terminal is opposite. One of the important requirements is that the drain region must be strongly degenerated to have a edgy doping profile for a substrate (lightly doped), and because of this a tunnel junction create under the gate with the 2D electron channel.

This tunnel device is shaped using a GaAs/AlGaAs heterojunction to observe the fundamental characteristics [15]. By applying a adequately high gate voltage to make the electrons in the accumulation layer at the semiconductor surface highly degenerate, and also to decrease the surface depletion layer width to less than several

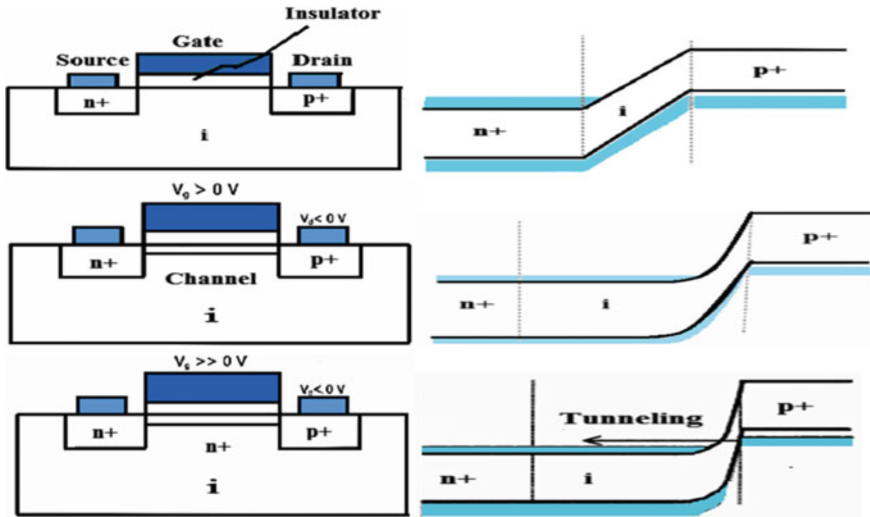

Fig. 1 Schematic of the STTs and Energy band diagram under, **a** thermal equilibrium, **b** weak carrier accumulation and **c** strong carrier accumulation condition [15]

tens of nanometers, electron tunneling from the valence band of drain region to conduction band of the accumulation layer through the surface depletion layer takes place. This is the situation of interband tunneling, shown in Fig. 1c due to which the drain current starts flowing. Similar to MOSFET the drain current is controlled by the applied gate voltage and the tunneling current is also varied by the source to drain bias voltage, and the STT is expected to exhibits basic transistor characteristics without a saturation region of drain current. Beside this, electron tunneling occurred in the STT is near to the drain region which signifies that the length of gate can be comparable to the depletion layer width.

2.2 Basic p-i-n TFET

The p-i-n tunnel FET was developed to obtain steep swing in 2004 by T. Baba. The device structure is basically the same as the Lubistor, as shown in Fig. 2a. High doping levels and an abrupt source or drain junction are the strong constraints on the TFET device structure to secure the tunneling mechanism. The working principle of TFET is quite similar to a PN diode at reverse biased condition, where the gate is insulated and controls the tunneling mechanism. One of the shortcomings of this device is that it gives steep swing only in a very limited voltage range [16].

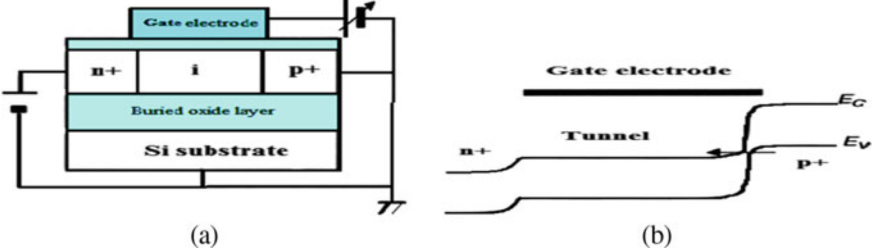

Fig. 2 **a** Schematic view, **b** energy band diagram of the basic p-i-n tunnel FET [16]

2.3 Feedback FET

The feedback FET is proposed in 2008 to earn a steep swing [8]. Beside the similarity with the Lubistor, it has underlapped gate electrode. The feedback FET has gate side walls in gate-offset spaces. SOI body regions under the gate side walls work as an energy barrier to electrons around the source junction ($n^+ - i$ junction) and that of holes around the drain junction (i-p^+ junction). By applying a positive gate voltage, some holes are trapped in the low energy well beneath the gate side wall near the source junction and some electrons are trapped in the low energy well beneath the gate side wall near the drain junction. Few holes which are trapped reduce the potential barrier of carrier (electrons and holes) close to the source junction and drain junction, respectively. Because of this, an abrupt reduction in potential barrier height and an abrupt subthreshold swing (2 mV/dec) takes place. Change of state from the non-active (OFF) state to the active (ON) state claims that the side wall insulator be charged up. Due to this, device also has few matter of concern: the threshold voltage (V_T) on the forward sweep is completely different from that on the reverse sweep and the threshold voltage (V_T) depends on the drain voltage (V_D) (Fig. 3).

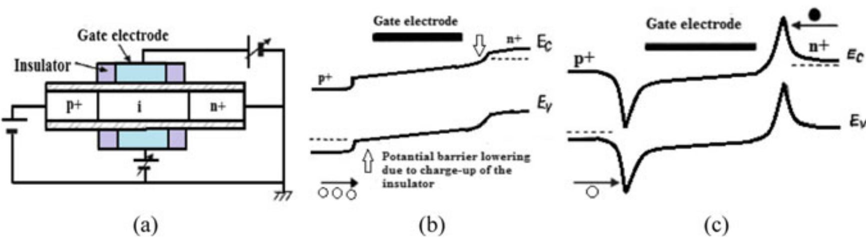

Fig. 3 Schematic device structure of feedback FET: **a** device structure, **b** energy band diagram at the ON state and **c** at the OFF state [8]

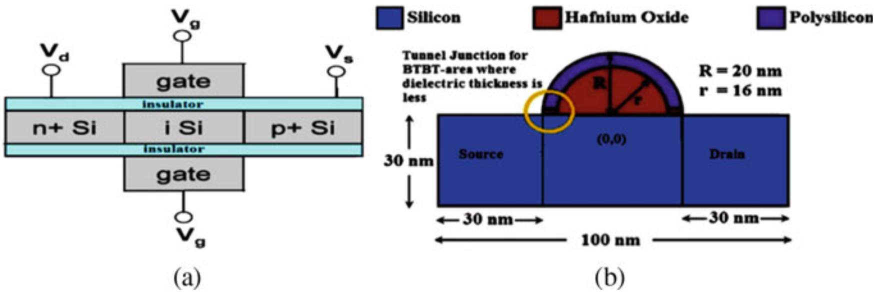

Fig. 4 **a** Schematic of DG tunnel n-FETs [6]. **b** 2D structure of CG-TFET [7]

2.4 Double-Gate (DG) TEFT

For tunnel FETs, because of increased gate capacitance, the coupling in between the tunneling barrier and the gate region is improved. Due to this, an exponential behavior of current can be seen rather than a linear one in MOSFET. Depending on the barrier width between the p^+ source and intrinsic region, the ON-state current of a TFET increases exponentially with a decreased energy barrier width. For a compact double-gate tunnel FET process, by adding an additional gate the TFETs current increases twice. Due to this reason, both the ON and OFF current are enhances. However, the OFF current in the order of pA or fA remains very low. Boucart and Ionescu [6] proposed a double-gate tunnel n FET structure with HfO2 and ZrO_2 as a high k gate dielectric material and described that at gate voltage (V_g) = 1.8 V an ON-state current to 0.23 mA reduced average subthreshold swing 57 mV/dec, and a minimum point swing of 11 mV/dec is possible (Fig. 4).

2.5 Circular TFET

Goswami and Bhowmick [7] proposed a novel architecture of circular shape gate silicon tunnel FET and reported the electrical noise effect on the device with a comparison to heterojunction tunnel FET device (HJ-TFET). Instead of using Boltzmann statistics, Fermi Dirac statistics has employed in this device for source and drain degeneration. In comparison with heterojunction tunnel FET, drain current of circular-gate structure has a tendency to suffer from traps, which is a major limitation. By using gate–drain underlap under the consideration of Gaussian traps, the cut-off frequency of the circular-gate tunnel FET can be increased which makes it a favorable candidate for digital applications. Advantage of circular-gate TFET over heterojunction TFET is that, by changing the radius of circular-gate two structural modifications (1) enhance in gate–drain underlap and (2) retrenchment of dielectric thickness close to tunnel barrier, can be done. Due to this, noise is less pronounced in circular-gate TFET as compared to heterojunction TFET.

2.6 Heterojunction TEFT

In comparison with MOSFET, Si-based TFETs experience lower ON-state current (I_{ON}) because of the high carrier effective mass and bandgap in Si. To mitigate this problem, III-V compound lower bandgap materials can be used in the place of Si. However, the subthreshold swing in some of the devices is set much higher than the conventional value (60 mV/dec), mainly due to poor material qualities and gate/channel interface characteristics. Bae et al. [9] developed a Ge (source region)/Si (channel region) heterojunction tunnel FET and explained the effect of impurity concentration ($>10^{20}$ cm^{-3}) in source region (which calculates depletion width and tunneling distance) on the device. It is experimentally exhibited that this heterojunction structure has the potential to obtain a high I_{ON} of 82.3 nA, higher $I_{ON}/I_{OFF} = 6.8 \times 10^6$ and a low subthreshold swing of 60.6 mV/dec (for 1.1% tensile strain).

2.7 Cylindrical-Gate Tunnel FET (CG-TFET)

Cylindrical-gate tunnel FET reduces different types of short channel effects and floating body effect, and therefore, it gives good control of the channel. Due to this, better scalability is possible compared to single-gate, double-gate, tri-gate and circular-gate structures. Dash and Mishra [11] developed a two-dimensional analytical potential model for cylindrical-gate tunnel FET. The potential distribution along the channel of the device has been calculated by using 2D Poisson's equation under the consideration of parabolic approximation. By using a generalized Kane's model, drain current has estimated as a function of gate voltage. Tunneling distance (minimal value) is an important character for the calculation of device characteristics, like subthreshold swing, I_{ON} and g_m which allows cylindrical gate the device to be an ideal candidate for high-performance and ultralow-power applications.

2.8 p-n-i-n TFET

Reliability is one of the major limitations of the conventional p-i-n tunnel FET because of the strong electric field close to the source-intrinsic junction. The basic difference between p-n-i-n structure and basic tunnel FET structure is an ultrathin layer of n type material is implanted at the tunneling junction (p-i) with a SiO_2 layer as a gate dielectric material. Cao et al. [13] reported a p-n-i-n structured TFET and described how reliability can be improved. Practically, by forming a controlled dimension spacer prior to the dopant ion implantation process at the source region, the underlap structure can be easily done. Figure 5b represents an underlap ΔL_{UL} between the interface of tunnel junction and gate.

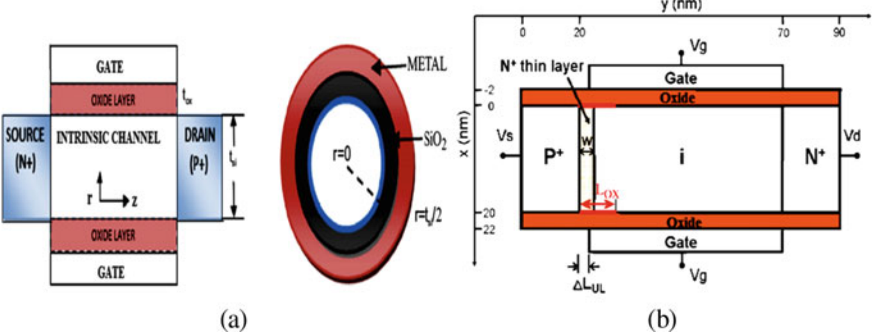

Fig. 5 **a** Schematic of p-channel cylindrical-gate TFET structure: cross-sectional (left) and side (right) view [11], **b** Schematic view of the p-n-i-n tunnel FET [13]

The band-to-band tunneling (BTBT) current density $j(E)$ can be written for this p-n-i-n TFET as

$$j(E) = \alpha T(E) f(E_{\mathrm{fl}}, E_{\mathrm{fr}}) \Delta E \tag{1}$$

where $T(E)$ and $f(E_{\mathrm{fl}}, E_{\mathrm{fr}})$ represent the tunneling coefficient (energy dependent) based on WKB approximation and states occupancy, respectively. α is constant for whole tunneling process in range of energy ΔE. The ON-state figure of merit for the overall characteristics of the tunnel FET combining both ON current and reliability can be expressed as:

$$\tan\theta = \left|\frac{E_{x,\mathrm{peak}}}{E_{y,\mathrm{peak}}}\right| \tag{2}$$

Here θ is the channel y-direction deviation angle of the electric field. With the placing of an ultrathin n layer at the source channel junction, this structure increases the tunneling field E_y, reduces field E_x (normal component) and because of these gate leakage reduces. In addition to higher drive current I_d, the variation of the threshold voltage can be reduced and thus the reliability can be improved significantly.

2.9 p-n-p-n Tunnel FET

The p-n-p-n tunnel FET consists of a gated $p^+p^-n^+$ diode with the insertion of ultrathin n^+ pocket region between the source (p^+) and channel (p^-) region; this is mainly done to enhance the tunneling mechanism [17]. For improving the gate controllability over channel and I_{ON} of TFET devices, high k materials are used as a

gate dielectric. Ning et al. [18] introduced a p-n-p-n tunnel FET with a high k gate dielectric and a low k fringe dielectric.

The BTBT rate as per Kane and Keldysh models is:

$$G_{\mathrm{BTBT}} = A\left(\frac{\xi}{\xi_0}\right)^P \exp\left(-\frac{B}{\xi}\right) \tag{3}$$

where $\xi_0 = 1$ V/cm for entire tunneling mechanism, electric field magnitude is ξ, $P = 2.5$ and A, B are fitting coefficients [18]. The TFET device with this structure has good switching characteristics, high process tolerance and enhanced ON current. This structure is compatible for low-power applications (Figs. 6, 7 and 8).

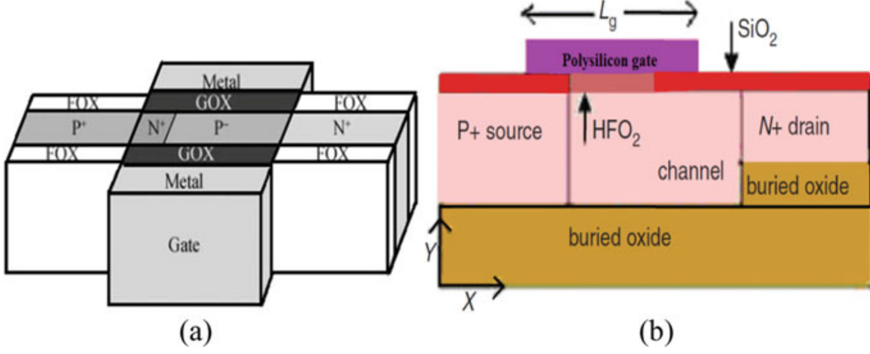

Fig. 6 **a** Schematic diagram of the p-n-p-n tunnel FET with a high k gate dielectric and a low k fringe dielectric [18], **b** Schematic of SOI Si tunnel FET with drain-raised buried oxide [19]

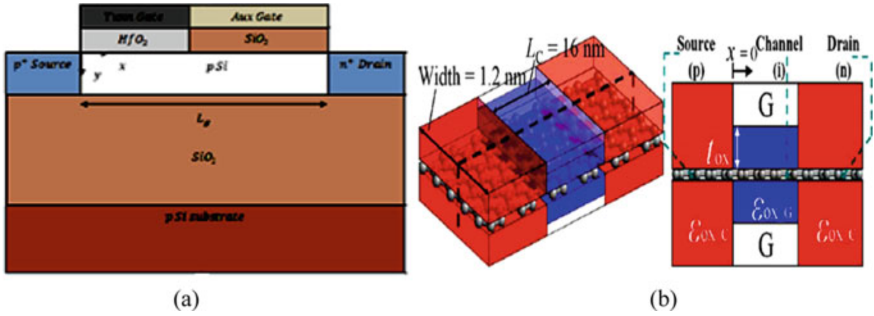

Fig. 7 **a** Schematic view of HD-DMG SOI tunnel FET [20]. **b** 3D structure of double-gate GNR TFETs. **c** Schematic view of DG GNR TFETs [14]

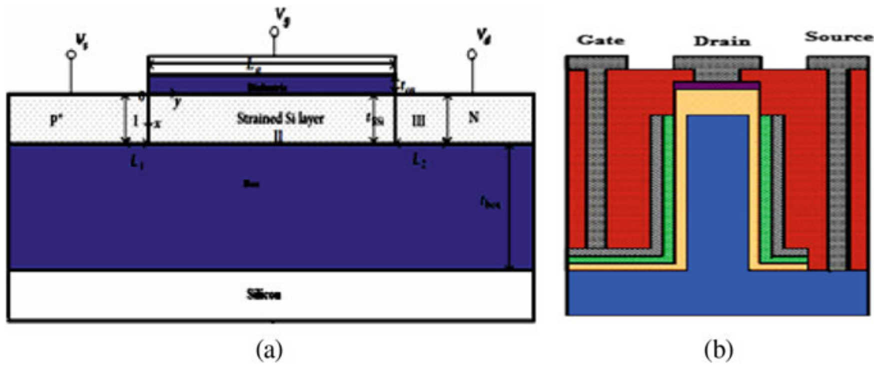

Fig. 8 **a** Schematic view of fully depleted strained SOI TFETs [21], **b** core–shell (CS) vertical nanowire TFET [22]

2.9.1 Raised Buried Oxide Tunnel FET

TFET operates under gate-controlled band-to-band tunneling mechanism. Si-based tunnel FET suffers from low tunneling probability and low I_{ON} because of the higher carrier effective mass and bandgap in Si. By using a raised buried oxide in the drain region, I_{ON} increases and I_{OFF} reduces which is desirable. With the drain-raised buried oxide, the scattering due to surface roughness in the channel and source region enhances as the peak electron concentration appears at the source-intrinsic junction a few distances from buried oxide in the drain region. Due to this, the total channel mobility is conserved and an enhanced I_{ON} and transconductance (g_m) can be acquired. By using raised buried oxide, B. Bhowmick obtained good value of I_{ON} and g_m at gate length (L_g) = 40 nm. The I_{ON}/I_{OFF} value for this device is around 10^7 with a negligible scaling effect on the threshold voltage (V_T) [19]. Further gate length optimization is needed to acquire higher I_{ON}, excellent g_m, lower I_{OFF}, low V_T and steep subthreshold slope. Therefore, raised buried oxide tunnel FET is the ideal candidate for high-performance and ultralow-power applications.

2.9.2 Dual Material Double-Gate All Around (DMDGAA) TFET

The advantage of DMG tunnel FET is its additional gates which results in boosted ON current, although the OFF current is still in the order of fA. H. R. Bharathi R and P. Karthikeyan presented an analytical model of DMDGAA tunnel FET [23]. Surface potential distribution, electrical field and drain current have been modeled by two dimensional Poisson conditions. This structure has the ability to provide excellent ON current, low subthreshold swing (SS) and also superior immunity to short channel effects [23].

2.9.3 Heterodielectric Dual Material Gate (HD-DMG) SOI TFET

HDDMGSOI structure combines the advantages of both dual material gate and heterodielectric material. S. Mathew reported HD-DMG SOI tunnel FET with both tunnel and auxiliary gates. For improving tunneling rate as well as ON current significantly, HfO_2 is used as a high k dielectric material near the source to channel junction and comparatively low k dielectric material (SiO_2) is used near the drain junction [20]. This structure is least prone to different types of SCEs like punch-through, DIBL, threshold voltage roll-off, etc., and can provide superior properties and better characteristics than the basic TFET structure.

2.9.4 Graphene Nanoribbons (GNRs)-Based Ultimately Thin Body TFETs

The 2-D materials (2DMs) have the competency to control the channel thickness, resulting in elevated gate control over the channel and minimize the short channel effects. Due to this adaptability, in TFET by using 2-D materials as a channel, ON current can be enhanced. But the design of the 2-D materials-based TFET is not yet familiar. This is mainly due to the complicacy of interband tunneling between two 2D layers. Lam et al. [14] developed a ultimately thin body graphene nanoribbons (GNRs)-based tunneling FET (UTB-TFETs) using low k spacers to improve I_{ON}. For the study of GNR TFETs, Green's function and Dirac equation-based quantum transport simulator [24] has been used. By increasing the tunneling distance, the I_{OFF} can be reduced up to 0.20 pA/µm, I_{ON} can be enhanced up to 0.572 mA/µm, and a subthreshold swing of to 37.6 mV/dec can be achieved [14].

2.9.5 Gate–Drain Underlap Nanoscale Tunnel FET

Goswami and Bhowmick [1] designed a analytical model for a Si-based gate–drain underlap tunnel FET with a gate overlap $\delta p + Si_{1-x}Ge_x$ layer close to source region. Depending on the mole fraction of Ge and by using Poisson's equations, electric field and surface potential have been modeled for three cases: SiO_2 ($k = 3.9$) as gate dielectric with PolySi (wf = 4.25 eV) gate, Al_2O_3 ($k = 10$) as gate dielectric with Al (wf = 4.05 eV) gate and HfO_2 ($k = 22$) as gate dielectric with Al (wf = 4.05 eV) gate. Materials with low work function reduce V_T and increase I_{ON}. Fermi Dirac statistics is mostly preferred because of higher doping concentration. As the device is nanoscale dimension, Masetti mobility model has been used to insure the effect of velocity saturation on the overall device performance.

2.9.6 Fully Depleted Strained SOI TFETs

Tensile strained silicon has the compatibility with conventional silicon processing due to its smaller bandgap comparing to silicon which helps to enhance the tunneling current and the Si on insulator (SOI) technology has the potential of removing latchup action and the deduction of parasitic capacitance. Strained SOI structure unites the benefits of both SOI film and strained Si and reduces leakage current. Fully depleted strained SOI tunnel FET has the ability of to enhance I_{ON} and steep subthreshold slope. Li et al. [21] reported a fully depleted strained SOI TFETs and described how dimension and strain affect threshold voltage (V_T). This design is able to deliver point subthreshold swing of 17 mV/dec (without strain), 11 mV/dec (with strain) and average subthreshold swing ranges 63–46 mV/dec. It is experimentally demonstrated that V_T improves with increment in strained Si layer thickness.

2.9.7 Core–Shell (CS) Silicon Vertical Nanowire TFETs

In basic TFET it is very challenging to fulfill lower subthreshold swing, higher ON current and high ION/IOFF because of the electrostatic effect from the drain terminal. Vertical structure has the ability to reduce this effect without any scalability penalty by providing a long enough channel. Core–shell TFET structure allows lower subthreshold swing and higher I_{ON} than basic tunnel FETs through their superior surface to volume ratio. Because of this ratio, tunneling region increases without increasing the device area, and hence, ON current increases significantly. Yoon et al. [22] proposed Si-based TFETs placing a core–shell vertical nanowire structure and made a comparison of DC characteristics between this proposed model and the basic TFETs for important metrics like I_{ON}, I_{OFF}, point SS and geometrical parameters like the nanowire diameter (D_{NW}) and height (H_{NW}). By increasing the nanowire height (H_{NW}) and reducing equivalent oxide thickness (EOT), ON current can be enhanced significantly. This model (CS TFETs) is able to exhibit 5×10^{-7} A ON current (I_{ON}) and I_{ON}/I_{OFF} 10^{12} at a fixed diameter (D_{NW}) of 20 nm, EOT = 0.8 nm, height (H_{NW}) = 400 nm and drain to source voltage (V_{ds}) of 0.5 V. For maintaining low gate leakage current, EOT can be reduced up to 0.8 nm. By doing this, the gate-to-channel controllability increases, and a sharp band bending at the tunnel junction enhances the electric field and I_{ON}. Besides high ON current, it shows subthreshold swing 60 mV/dec of SS_{point} due to their high surface-to-volume ratio (Table 1).

Table 1 Comparison of ON current (I_{ON}), I_{ON}/I_{OFF} and subthreshold swing for various design structures

Device structure	References	On current (10^{-6}A/μm)	I_{ON}/I_{OFF}	Subthreshold swing (mv/dec)
Double-gate (DG) TEFT	[10]	230	1.2×10^{11}	56
Circular-gate(CG) TFET	[7]	5.213	6.12×10^{6}	–
Cylindrical TFET	[11]	2.2	1.8×10^{7}	27–56
Dual material SOI TFET	[20]	0.1	1.6×10^{11}	–
P-N-P-N TFET	[18]	160	3.44×10^{11}	40
Ultimately thin body (UTB) TFET	[14]	572	2.86×10^{9}	37.6
Core–shell vertical nanowire TFET	[22]	0.5	1.0×10^{12}	60
FD strained SOI TFET	[21]	300	1.5×10^{11}	46

3 TFET for Low-Power Application

3.1 Ultralow-Power and Sensitive UHF RFID Rectifier

In the batteryless passive RFID (Radio Frequency Identification System) tags, by using the proper rectifier circuit RF signal will be converted to dc to prevent the limitation of the communication range. But for this the rectifiers must have the ability to extract adequate dc power from the incident power. However, this process sometimes is not easy when the incident power is not very high. Tunnel FET is one of the most attractive options for this rectifier design. Liu et al. [25] presented a design insight for improving the performance of a heterojunction TFET-based differential rectifier. The design topology for the TFET-based differential RF rectifier is shown in Fig. 9 under the consideration of unidirectional transport of tunnel FETs. When a differential input signal ($V_{in,AC}$) is applied between RF+ and RF-, a dc output voltage $V_{out,DC} = V_H$ appears across the load resistance. During the +ve half of input RF signal, transistor M1 and M4 will remains off but transistor M2 and M3 will on and current flows to the load as shown in Fig. 9. For the −ve half of the input RF signal, M1 and M4 will be on and M2 and M3 will turn off. Power conversion efficiency (PCE) can be defined as the ratio of output power (average) at the load to input power (average). PCE can be expressed as

$$PCE = \frac{P_{DC,out}}{P_{RF,in}} = \frac{I_{DC,out} V_{DC,out}}{\frac{1}{T} \int_0^T I_{in,AC}(t) V_{in,AC}(t) dt}$$

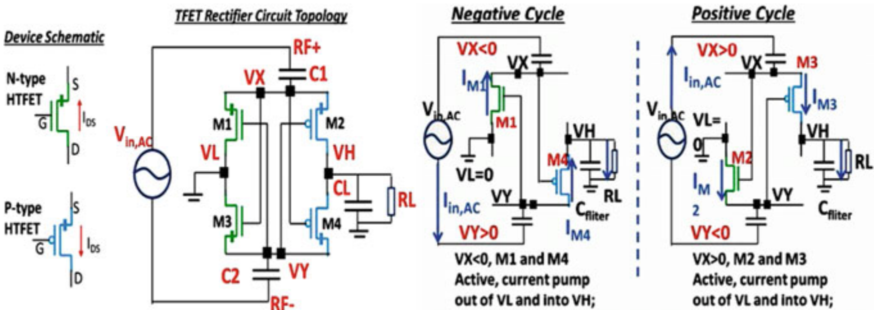

Fig. 9 TFET-based differential RF rectifier circuit and its operation during half cycle [25]

$$= \frac{\frac{V_{\mathrm{DC,out}}^2}{R_{\mathrm{L}}}}{\frac{V_{\mathrm{DC,out}}^2}{R_{\mathrm{L}}} + P_{\mathrm{Loss}}} \tag{4}$$

$$P_{\mathrm{Loss}} = P_{\mathrm{Leakage}} + P_{\mathrm{Reverse}} + P_{\mathrm{switching}} + P_{\mathrm{Ron}} \tag{5}$$

where $P_{\mathrm{DC,out}}$ is the output dc power, P_{Loss} and $P_{\mathrm{RF,in}}$ represent power loss and input RF power, respectively. $P_{\mathrm{Leakage}}$is leakage power, P_{Revserse} is reverse conduction power. $P_{\mathrm{switching}}$, P_{Ron} and $I_{\mathrm{in,AC}}$ denote induced dynamic power due to capacitance switching, induced thermal power loss and branch current, respectively. It is experimentally demonstrated that this HTFET-based rectifier has the capability of 98% power conversion efficiency with power consumption of 500 μW, sensitivity of −24 dBm for dc output power of 9 μWatt 915 MHz [25].

3.2 *nTFET-Based Dynamic Circuit*

Conventional CMOS designs take p channel and n channel transistors as pull-up and pull-down devices, respectively, to forego the waste of threshold voltage (V_{T}). But as, n-type TFET does not have a serious V_{T} loss; thus, it can be applied both in the pull-down and pull-up devices without any performance compensation. It gives the flexibility to the designer to waive pTFETs completely and build circuits with utilizing nTFETs only. However, it is important for nTFET-based dynamic circuits to drive both the pre-charge and evaluation phase by an active high clock signal; hence, Fig. 10 shows a dual-phase clock [26]. Use of TFETs provides an efficient level restoration of output voltage, which mainly degraded because of charge sharing. Figure 10c shows the energy vs delay graph of NAND and NOR gates. For nTFET device, advancement in both energy and delay is observed.

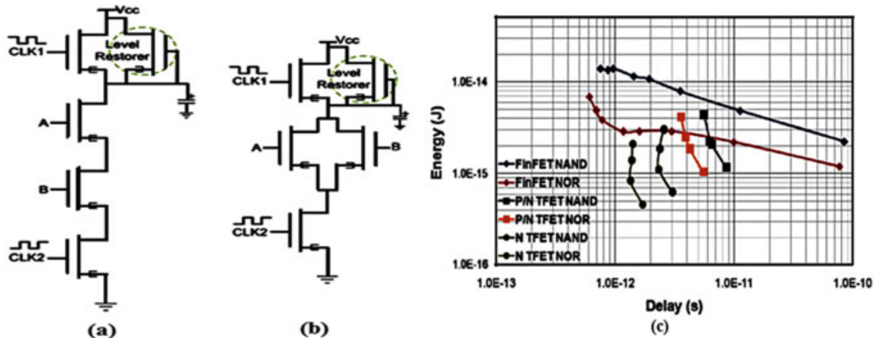

Fig. 10 nTFET-based dynamic dual clock, **a** NAND, **b** NOR, **c** energy versus delay graph of NAND and NOR gates [26]

3.3 TFET-Based Pass Transistor Logic (PTL)

Instead of using a pull-up or pull-down device to immediately linked output to supply voltage, pass transistor logic exhibits logic selection to activate or deactivate the conducting paths from input to output. One of the important key factors of PTL is that all transistors must have capability of conducting in both directions. But as TFET is a unidirectional device, some additional design trick must be adopted to satisfy this key feature.

i. TFET-based Static PTL: One of the easiest ways to utilize tunnel FETs in a bidirectional manner is to employ an extra tunnel FET in reversed direction for providing an opposite path, making a bidirectional switch, which has the capability of satisfying the bidirectional conduction requirement.

ii. TFET-based Dynamic PTL: For the dynamic pre-charge design, the orientation of TFET is such that at the time of evaluation only discharge may happen at the output node. For the prevention of short circuit between supply voltage and ground, during pre-charge isolation of stack input is needed. This isolation can be done by introducing an extra nTFET between output terminal and the stack.

4 Challenges of TFET

4.1 Asymmetrical Structure and Unidirectional Conduction

TFET is a p-i-n gated diode under reverse biased condition exhibiting band-to-band tunneling at the tunneling (source-intrinsic) junction and enables steep subthreshold slope. As the source and drain region are doped with opposite types of materials, the output characteristics of TFET under +ve and −ve drain voltages are dissimilar in nature. Under reversed drain voltage, negligible lower current is seen, whereas by

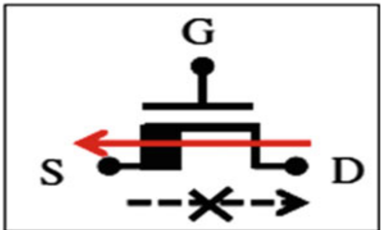

Fig. 11 Schematic of an n-TFET, red arrow indicates flow of current and bold line shows source to channel tunneling barrier [28]

applying forward drain voltage TFET behaves like a traditional MOSFET. Due to the asymmetrical structure and unidirectional flow of current, various issues appear in a TFET-based circuits like (1) maintaining proper doping and orientation of source and drain region and (2) reliability issue because of the disabled path at the time of charging or discharging internal circuit nodes [27] (Fig. 11).

4.2 *Point TFET and Line TFET*

In point TFET, tunneling takes place at the source channel (n-i or p-i) interface when gate aligns with tunnel junction. With an applied positive gate voltage, depletion region is developed at tunnel junction due to which potential distribution along the channel changes and corresponding flow of current available. To attain a high value of ON current, heavily doped source region can be used. In Line TFET, tunneling mainly occurs at the source region in the direction normal to the gate (source gate overlap structure) [29, 30]. At applied high gate voltage, this tunneling mechanism plays a significant role. The main key factors, which govern the tunneling current, are doping level (mainly source region), gate dielectric thickness and bandgap of the material. A small bandgap material has the ability to give an enhanced ON current and a reduce onset voltage for both line and point tunneling. Lower value of gate dielectric thickness enhances the ON current for point tunneling and lowers the onset voltage for line tunneling. In case of line tunneling both the ON current and onset voltage increases with a raised sourced doping concentration where as in case of point tunneling onset voltage decreases.

4.3 *Raised Miller Capacitance*

The overall performances of the capacitances of TFET are not same as traditional MOSFET. For MOSFET, after forming the inversion channel, the drain and source regions are linked through the inversion channel with similar type of carrier. At that time C_{GG} (total gate capacitance) is divided into gate-to-drain capacitance (C_{GD}) and gate-to-source capacitance (C_{GS}). But in case of TFET, because of the tunnel barrier

the C_{GG} is linked by the electrons of channel-to-drain region, gate-to-drain capacitance governs the entire C_{GG} [31, 32]. For the improved capacitive coupling between the drain and gate region, this large amount of C_{GD} increases Miller capacitance, which induces important undershoot or overshoot during switching operation of TFET-based circuits. This leads to large amount of power consumption and degrades the overall contribution of TFET. This Miller coupling effect can be removed by (1) introducing large load capacitance C_L to suppress the coupling factor, (2) using material with small bandgap.

4.4 Delayed Saturation

For low-voltage application, TFET gives good drive current and steep subthreshold slope. But when V_{DD} increases, output characteristics of TFET exhibit a broad transition before it reaches into saturation; thus, simply a delayed saturation can be observed. For a MOSFET by applying a gate voltage, a conducting channel is induces and the saturation current is controlled by pinch off of the channel close to the drain region. In case of tunnel FET, the resistivity of the channel region is high because of lightly doped intrinsic region. Thus, a series resistor comes into the picture along with source to channel tunneling barrier. By applying low drain voltage, current increases significantly with increasing V_{DS}. As drain voltage increases, voltage drops across the series resistance (channel resistance), resulting in a slowly increasing saturation current. The output characteristics of TFET at gate-to-source voltage = 0.5 V are shown in Fig. 12c [33, 34]. To mitigate delayed behavior problem, it is desirable to use a degenerated source region.

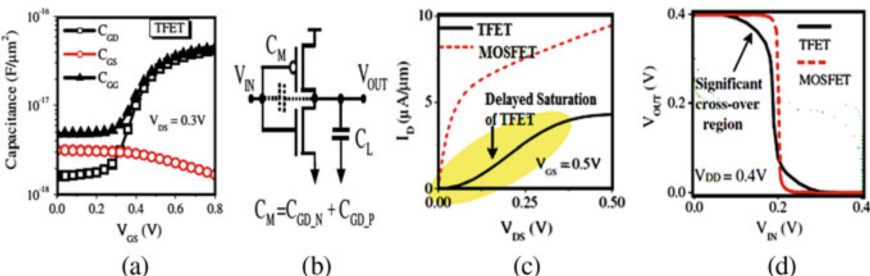

Fig. 12 **a** Overall capacitance vs gate-to -source voltage characteristics of n-TFET, **b** equivalent Miller capacitance [28], **c** output characteristics, **d** voltage transfer curve (VTC) for TFET and MOSFET [28]

5 Conclusions

This survey of tunnel FET exhibits that, in comparison with conventional MOSFET the steep subthreshold devices are advantageous because of its potential to have lower subthreshold swing, lower OFF current (I_{OFF}) without any performance reparation, ability to work on subthreshold and superthreshold voltage. But one of the major constraints of tunnel FET is low ON current (I_{ON}) as compared to ITRS requirement. To enhance the I_{ON}, several novel architectures from the initial surface tunnel transistor to recent dual material SOI TFET, gate–drain underlap TFET, ultimately thin-body (UTB) TFET, FD strained SOI TFET and core–shell (CS) silicon vertical nanowire TFETs are reviewed in this paper. This paper also explains some TFET application for ultralow-power and high-sensitive rectifier, digital logic design especially at ultralow voltages and few challenges of TFET-based circuit due to its unidirectional conduction, asymmetric structure, etc. It is clearly visible that TFET devices are attractive successor of MOSFETs ultralow power. To realize the best performance of TFET-based circuit in comparison with conventional MOSFET, further alternation and optimization are needed.

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Performance Analysis of Defective 1D Photonic Crystal Structure for Detection of Hemoglobin Concentrations in Blood

Abinash Panda and Puspa Devi Pukhrambam

Abstract We report a defective 1D photonic crystal for real-time sensing of blood hemoglobin concentrations. The proposed structure is configured as adjacent thin films of Na_3AlF_6 and ZnSe including a defect remain at the middle. The cornerstone of this research is based on the analysis of the transmission spectrum by manipulating the transfer matrix method (TMM). Upon infiltrating the defect layer with blood containing different hemoglobin concentrations, the shift in the resonant mode wavelength is observed within the photonic band gap (PBG). Sensor performance is evaluated by varying the incident light angle and thickness of the defect medium. Numerous sensing characteristics such as sensitivity, figure of merit and signal-to-noise ratio are computed for studying the effectiveness of the proposed sensor. Additionally, the simple structure with notable sensing performance makes the proposed sensor a suitable candidate for biosensing applications.

Keywords 1D photonic crystal · Transmittance spectrum · PBG · Sensing characteristics

1 Introduction

Photonic crystals (PhCs) belong to special class of multilayer structures, where the dielectric constant of different layers is repeated in a periodic manner along different dimensions, which result in 1D, 2D and 3D configurations of PhCs [1–3]. 1D PhCs are the most investigated owing to their low manufacturing cost and wide range of applications. When electromagnetic (EM) waves interact with PhCs, a distinctive property is perceived known as photonic band gap (PBG), where light of certain frequency ranges is prohibited to pass through the structure [4, 5]. When the incident light frequency matches with the defect mode frequency, the photons are positioned within the band gap, which form a resonant peak [6–8]. The resonant peak wavelength (λ_{res}) is a strong function of various structure parameters like thickness

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of dielectric layers, dielectric constant of the constituent materials and number of periods. Reflectance spectrum, transmittance spectrum and absorption spectrum can be vigorously controlled by changing the PBG and resonant mode characteristics [9]. A sensitivity of 428 nm/RIU is achieved by Zhang et al. [10], by deploying a photonic crystal cavity sensor to detect various concentrations of NaCl. A 1D PhC sensor showing a high sensitivity of 2200 nm.RIU^{-1} is demonstrated by Aly et al. [11], where the structure is realized through an alternate dielectric layers of SiO_2 and GaAs. The authors studied a 1D PhC-based transducer for application in sensing of biomolecules, where refractive index of various bioanalytes is sensed by measuring the fluorescence shift [12]. Chen et al. [13] investigated a 1D PhC for realization of gas sensor in terahertz regime. Aly et al. [14] presented a simple 1D structure to detect different creatinine levels present in the blood, where the sensing principle is based on analysis of the transmission spectra.

In the recent decades, researchers have shown keen interest in detection of hemoglobin concentration in blood as any deviation from the normal level may lead to various deadly diseases like anemia, thalassemia, liver disorder, cancer, etc. [15]. Refractive index (RI) is one of the most accepted biophysical parameters to quantify the amount of hemoglobin concentrations in blood. The refractive index of hemoglobin can be effectively measured by fluorescence spectroscopy and optical coherence tomography techniques. Biswas et al. [16] reported an optical resonator configuration designed with periodically arranged air holes for sensing various Hb concentrations present in the blood using FDTD method, but low sensitivity of the structure is a major concern. Natesan et al. [17] investigated transmission spectrum of a dual-core 2D photonic crystal fiber for detection of hemoglobin level in blood. A 1D PhC with central defect has been investigated for sensing hemoglobin concentrations [18], but the authors obtained a sensitivity of only 167 nm/RIU, which is considerably low. Here, a defected PhC with 1D configuration has been investigated with an aim to efficiently detect the hemoglobin concentrations at a wavelength of 680 nm. Table 1 displays the refractive index data of various hemoglobin concentrations [19].

Here, we have picked Na_3AlF_6 and ZnSe for the design of the proposed 1D PhC. The alternate combination of these material leads to high contrast in refractive index, which results in wide bandgap [20]. Also, these materials show omnidirectional wide band gap over a broad frequency range. Moreover, Na_3AlF_6 and ZnSe are characterized with feeble absorption loss in the visible and near-infrared wavelengths. This work has couple of benefits such as selection of novel materials for the design

Table 1 Refractive index information of hemoglobin concentrations at $\lambda = 680$ nm

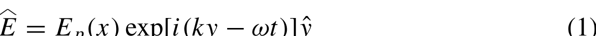
Hemoglobin concentration (g/L)	Refractive index	Measuring wavelength (nm)
0	1.3301	680
65	1.3403	
87	1.3482	
173	1.3633	
260	1.3771	

of different layers and detail assay of different sensing performances. In addition to this, a thorough investigation is performed to disclose the effects of variation in defect medium thickness and incident angle on the sensing characteristics. Moreover, the simple structure, easy way of analysis and cost-effective fabrication techniques make the proposed structure worth to fabricate.

2 Theoretical Treatment

Figure 1 depicts the proposed 1D photonic structure with $(A/B)^N/D/(A/B)^N$ configuration, where the first layer (A) is designed with Na_3AlF_6 having refractive index $n_A = 1.34$ and thickness $d_A = 500$ nm, whereas the second layer (B) is realized with ZnSe having refractive index $n_B = 2.61$ and thickness $d_B = 500$ nm. The period of the dielectric layer is considered as $N = 5$. A defect with thickness d is introduced at the center, where blood with different hemoglobin concentrations is infiltrated.

When the EM waves are interacted with the said structure, a certain number of photons are transmitted in the PhC, whereas some photons with certain range of frequencies are prohibited to pass, giving rise to band gap. Here, we have considered that the EM waves are incident at an angle θ_i and travel along the z-direction, and the dielectric layers lie in the x–y plane. The transmittance characteristic is scrutinized by manipulating transfer matrix method (TMM). We have used TMM because this method is the most efficient and easy to study the reflection/transmission spectrum for multilayer structures, as compared to other existing techniques like PWE and FDTD. In TMM, the complete transfer matrix is obtained by multiplying the transfer matrixes of each discrete layers. The well-known Maxwell equations are manipulated for exploring the transmission characteristics of EM signal in the pth layer, which can be written as below [21],



$$\widehat{E} = E_p(x)\exp[i(ky - \omega t)]\hat{y} \quad (1)$$

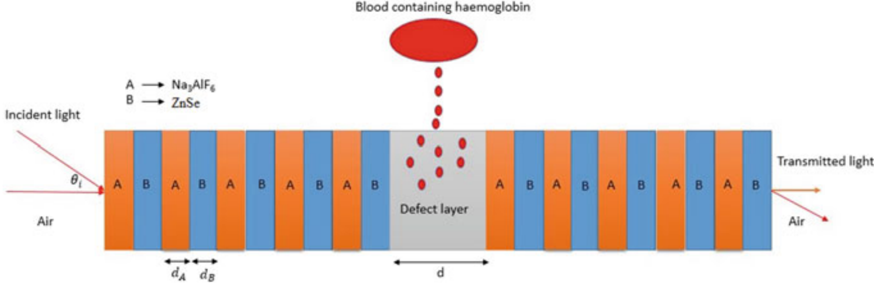


Fig. 1 Schematic of defect-based 1D photonic crystal structure

$$\widehat{H} = H_p(x)\exp[\mathrm{i}(ky - \omega t)]\hat{z} \tag{2}$$

where $E_p(x)$ and $H_p(x)$ denote the field components persisted in the pth layer, ω represents angular frequency, and k signifies the wave vector. The transfer matrix for pth layer can be expressed as,

$$M_s = \begin{pmatrix} \cos(k_p\theta_p) & -(i/\Psi_p)\sin\left(k_p\theta_p\right) \\ -(i\Psi_p)\sin\left(k_p\theta_p\right) & \cos(k_p\theta_p) \end{pmatrix} \tag{3}$$

where $\theta_p = d_p\cos\theta_i$ and $\Psi_p = \sqrt{\mu_0/\varepsilon_0}\, n_p\cos\theta_i$. Here, θ_i denotes the angle of incidence in the pth layer. The characteristics matrix representation of the complete configuration can be mathematically expressed as below,

$$M = \begin{pmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{pmatrix} = (M_A\ M_B)^N M_D (M_A\ M_B)^N \tag{4}$$

where M_A, M_B and M_D represent the individual transfer matrix of each considered layers. By using Eq. (4), the coefficients of transmittance and reflectance [22] can be computed, namely

$$t = \frac{2\Psi_0}{(M_{11} + M_{12}\Psi_P)\Psi_0 + (M_{21} + M_{22}\Psi_P)} \tag{5}$$

$$r = \frac{(M_{11} + M_{12}\Psi_P)\Psi_0 - (M_{21} + M_{22}\Psi_P)}{(M_{11} + M_{12}\Psi_P)\Psi_0 + (M_{21} + M_{22}\Psi_P)} \tag{6}$$

where $\Psi_0 = \sqrt{\mu_0/\varepsilon_0}n_0\cos\theta_0$ and $\Psi_P = \sqrt{\mu_0/\varepsilon_0}n_0\cos\theta_P$. Here, n_0 is the refractive index of air. The aforementioned equations allow us to evaluate the transmittance and reflectance, which can be expressed as,

$$\text{Transmittance} = \frac{\Psi_P}{\Psi_0}\left|t^2\right|, \quad \text{Reflectance} = |r|^2 \tag{7}$$

3 Results and Interpretations

The mainstay of the current work is the analysis of the resonant modes created in the transmission spectrum of the suggested configuration, in order to detect different concentrations of hemoglobin in blood. We have studied the sensing characteristics for different defect layer thicknesses such as 800, 850 and 900 nm. The TMM

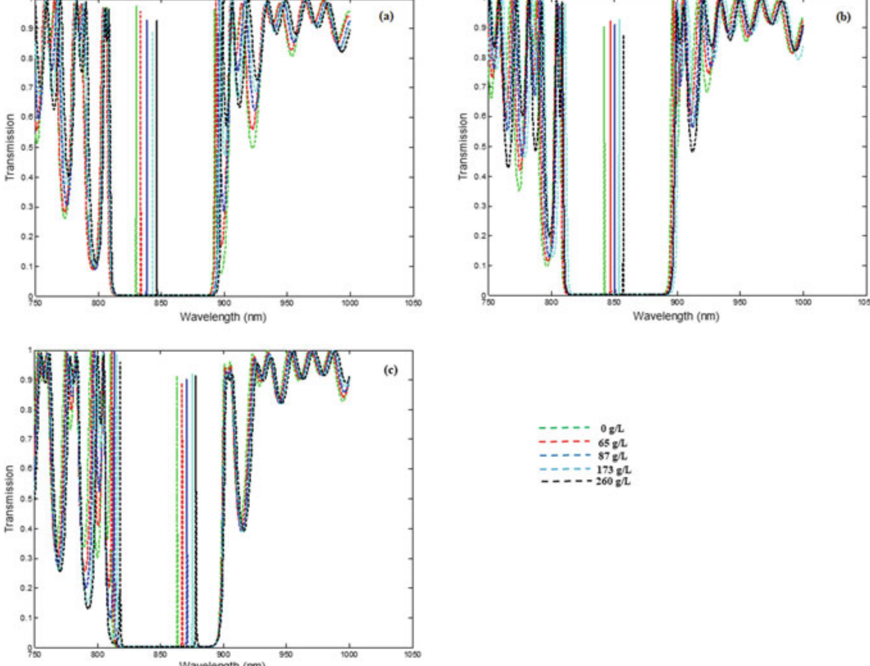


Fig. 2 Transmission spectrum of different hemoglobin concentrations at normal incidence of light **a** $d = 800$ nm, **b** $d = 850$ nm, **c** $d = 900$ nm

technique is used for computation of transmission spectrum of the proposed structure, which is shown in Fig. 2. Upon infiltration of the defect layer with different concentrations of hemoglobin, it is observed that resonant modes are red shifted in wavelength with the rise in hemoglobin concentrations. Besides, it can be witnessed that resonant modes are red shifted upon increasing defect layer thickness. From Fig. 3, it is seen that resonant wavelengths are sifted toward higher wavelengths for higher concentrations of hemoglobin. A remarkable total shifts of 16.4, 14.8 and 15 nm are marked for $d = 800$ nm, $d = 850$ nm and $d = 900$ nm, respectively, for the slight difference in refractive index.

Figure 4 shows the variation in resonant wavelength (λ_{res}) for different hemoglobin concentrations for different defect layer thicknesses. Here, it can be clearly seen that (λ_{res}) increases with rise in defect layer thicknesses.

From Fig. 4, the relation between the resonant peak (λ_{res}) and different hemoglobin concentrations (C) can be mathematically represented as below,

$$\lambda_{\text{res}} = 4.24 * C + 825.72, \quad \text{having } R^2 = 0.9955 \text{ at } d = 800 \text{ nm}$$

$$\lambda_{\text{res}} = 3.64 * C + 839.24, \quad \text{having } R^2 = 0.9911 \text{ at } d = 850 \text{ nm}$$

$$\lambda_{\text{res}} = 3.8 * C + 859.72, \quad \text{having } R^2 = 0.9975 \text{ at } d = 900 \text{ nm}$$

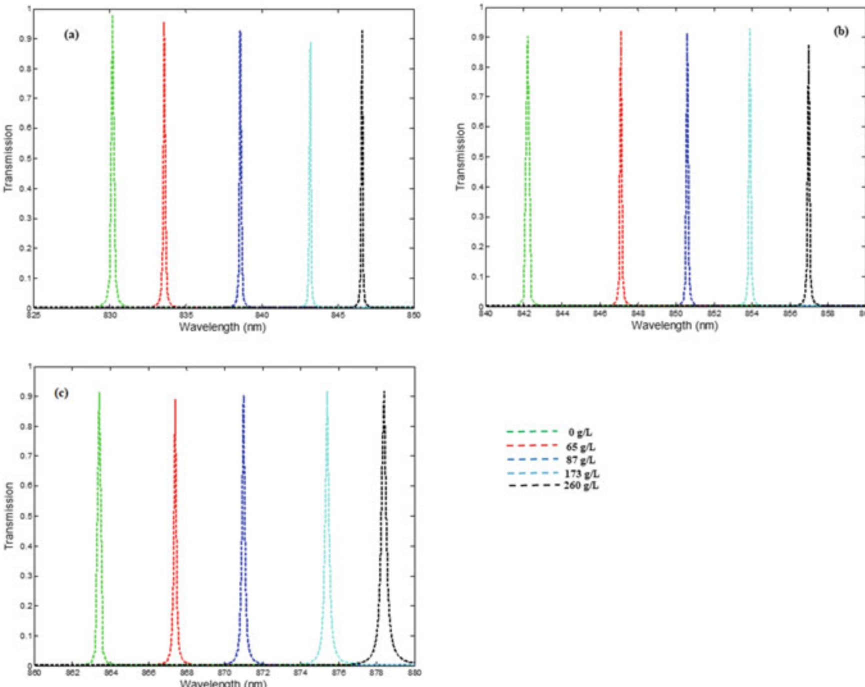


Fig. 3 The defect mode wavelengths at **a** $d = 800$ nm, **b** $d = 850$ nm, **c** $\mathbf{d} = 900$ nm at $\theta_i = 0°$

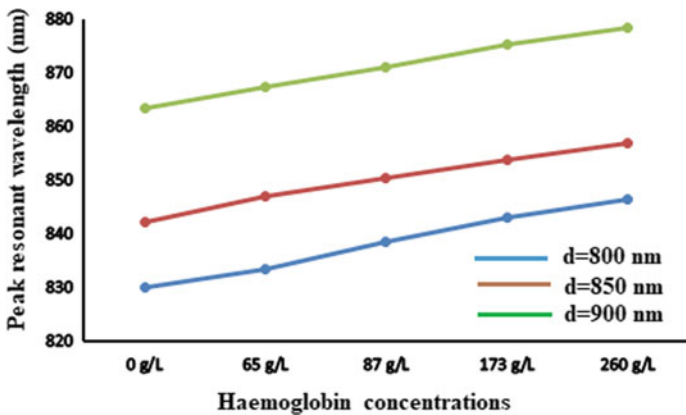


Fig. 4 Shift in the resonant wavelength w.r.t. different defect layer thicknesses and $\theta_i = 0°$

The aforementioned equations are in agreement with linearship, which ensures the precise detection of various hemoglobin concentrations. Sensitivity is one of the key parameters to appraise the performance of the suggested device [49], which can be calculated by the fraction of variation in the resonance wavelength (λ_{res}) to the RI contrast (Δn). Sensitivity is expressed as [23],

$$S\left(\frac{\text{nm}}{\text{RIU}}\right) = \frac{\Delta\lambda_{res}}{\Delta n} \tag{8}$$

Sensitivity, which is delineated in Fig. 5, is the utmost significant parameter for appraising the sensor performance, where it is perceived that a maximum sensitivity of 475.6 nm.RIU^{-1} is acquired for hemoglobin concentration of 87 g/L at $d = 850$ nm.

Apart from sensitivity, SNR and FOM are other two key parameters to judge the performance of any sensing device. SNR is computed by dividing the change in defect mode wavelength ($\Delta\lambda_{res}$) by the spectral half-width of the transmission dip $\left(\Delta\lambda_{1/2}\right)$. FOM is explained as the capability of a sensing device to identify a feeble change in the position of the resonance peak. SNR and FOM are computed with the help of references [24, 25]. Table 2 enumerates the numerically calculated values of SNR and FOM for numerous hemoglobin concentrations.

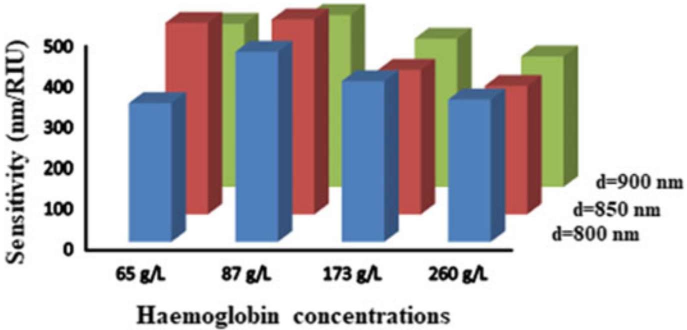


Fig. 5 Effect of defect layer thickness on sensitivity at $\theta_i = 0°$

Table 2 SNR and FOM of the proposed sensor

Hemoglobin concentration (g/L)	SNR			FOM (1/RIU)		
	$d =$ 800 nm	$d =$ 850 nm	$d =$ 900 nm	$d =$ 800 nm	$d = 850$ nm	$d = 900$ nm
65	340	470	400	1133.3	1566.66	1333.33
87	466.6	478.6	422.2	1866.4	1914.4	1688.8
173	393.9	354.5	363.6	1969.5	1772.5	1818
260	348.9	314.8	319.9	3489	3148	3199

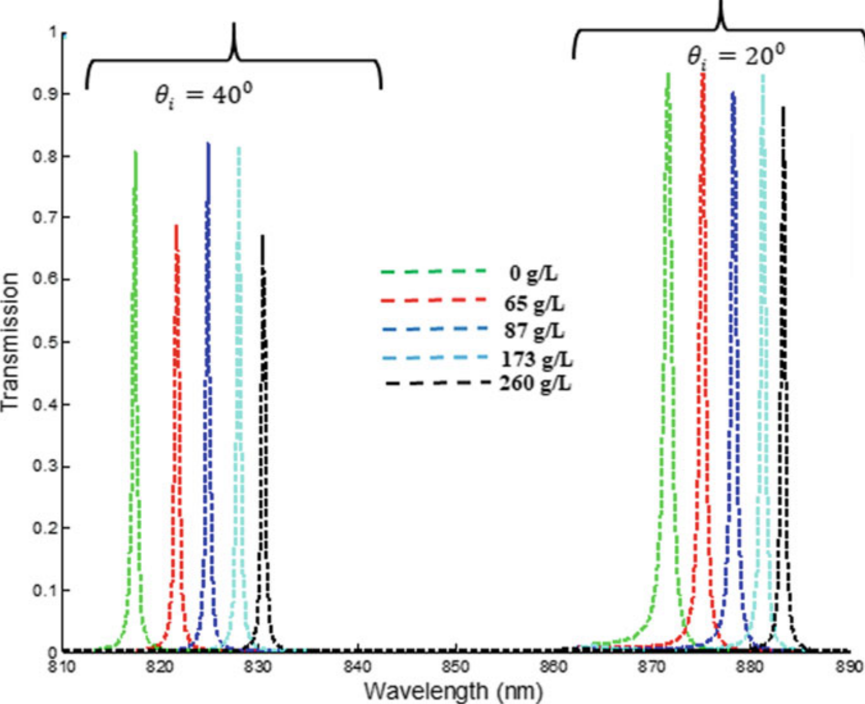


Fig. 6 Transmittance spectrum at $d = 850$ nm for incident angle, $\theta_0 = 20°$ and $\theta_0 = 40°$

Finally, we analyzed the nature of variation of the transmission spectra with reference to the variation in the incident angle for the projected structure, which is represented in Fig. 6. We have simulated the structure for higher incident angles ($\theta_i = 20°,\ 40°$) and compared the results with the outcomes of $\theta_i = 0°$ (shown in Fig. 3b) with $d = 850$ nm. Here, it can be envisaged that with an increase in incident angle, resonant modes are blue shifted. The primary reason for this blue shift phenomenon can be described by the Bragg condition, which is expressed as [26, 27],

$$m\lambda_{\text{res}} = 2N\sqrt{n_{\text{eff}}^2 - \sin^2\theta_i} \tag{9}$$

where λ_{res} is the resonant mode wavelength, m denotes the constructive diffraction order, θ_i represents the incident angle, n_{eff} signifies effective RI of the dielectric layers, and N denotes the period of dielectric layers. So, with an increase in θ_i, the wavelength is blue shifted, to satisfy Bragg condition. Aside this, the aforesaid behavior is perceived in the researches mentioned in the literature.

4 Conclusion

A defect-based 1D PhC is reported in this article for effective sensing of various concentrations of hemoglobin in blood. TMM technique is employed for computation of transmission spectrum for the analysis of shift in the resonant wavelength formed within the PBG. Numerous structure parameters such as dielectric constant of different dielectric layers, thickness of the dielectric layers and defect medium, period of dielectric layers and incident angle play vital role in determination of position of resonant mode wavelengths. Sensing characteristics like sensitivity, SNR, FOM are thoroughly analyzed for different defect layer thicknesses and angles of incident. The obtained performance characteristics indicate that the suggested sensor can be the most apposite contender in biosensing research area.

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Comparative Analysis of Different FET-Based Biosensor: Recent Advances in Device Structure and Sensitivity

Pamulapati Teja, N. Nagendra Reddy, and Deepak Kumar Panda

Abstract Basically, next-generation powerful building blocks are represented using semiconductor nanowires. These semiconductor nanowires have attractive properties, and along with that, they have bio-molecules, high surface-to-volume ratios, and nanometer scale footprint comparable to sub-cellular structures. Hence, in this article, the field of nanowire bioelectronics is discussed in a detailed manner and also summarizes the recent progress of nanowire bioelectronics. This article mainly focuses on the four types of biosensors they are, planar biosensor, cylindrical biosensor, DGFET, and EGFET. Each biosensor is discussed in a detailed manner and results re-obtained from the nanowire bioelectronics.

Keywords Bioelectronics · Biosensor · Electrophysiological recording · Field Effect Transistor · Nanowire · Nanotechnology

1 Introduction

Over the most recent couple of a very long time, there has been incredible interest in the advancement of lab-on-a-chip gadgets because of their focal points over conventional analytic techniques. The capacity to recognize organic specialists in a financial, simple to utilize, the convenient gadget is a significant examination center in the medical services industry [1]. These gadgets work in two stages: location and transduction. Initially, a ligand is immobilized onto a surface and afterward, and an example liquid is placed in contact with it. In the event that the objective analyte is available in the liquid, it ties to the ligand, and a sign corresponding to the measure of the analyte is created. There are numerous transduction techniques, for example, potentiometric [2], amperometric [3], magneto resistive [4], conductive [5], and so forth; however, the interface between the example and the sensor is commonly comparative in every one of them.

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It regularly includes the utilization of a self-assembled monolayer (SAM) as an intend to accomplish proficient immobilization [6–10], as it favors the connection of the catch atom and improves the particular authority of the analyte by decreasing the vague adsorption of random particles lab-on-a-chip gadget normally coordinate miniature fluidic networks for test and reagent taking care of with the detecting segment. The issue with this methodology is that inside the miniature fluidic (<100 μm) channels, the adjective inertial powers in the liquid are little contrasted with gooey powers, as shown by the low Reynolds number (Re $\ll$ 1). The outcome is an absolutely laminar stream, where the liquid streams in equal layers. This is a significant impediment for miniature fluidic frameworks in which the detecting segment is bound to a solitary surface. Just the particles in the least layer associate with the catch atoms, while the majority of the analyte contained in the liquid does not come into contact with the sensor.

Parallel dissemination could permit more atoms to come into contact with the detecting surface, yet at the length sizes of standard microfluidic streams, it is irrelevant. When planning and exploring components with an enormous and intermittent structure, the blend of the finite element method (FEM) and the Eigen mode extension strategy (EEM) can be utilized as a ground-breaking mathematical recreation strategy. This joined technique was created by the creator of this investigation, who has additionally distributed a few examinations on elite SPR biochemical sensors. The central idea of the FEM depends on the strategy for Fourier arrangement development. Fourier arrangement extension computations require an adequate number of development bases to stay away from enormous blunders. The FEM is likewise influenced by this issue. Since subjective waveguide structures contain numerous discrete guided modes and nonstop radiation modes, the entirety of the constant radiation modes cannot be remembered for mathematical reproductions, and blunders are unavoidable. In this examination, the perfectly matched layer (PML) and perfectly reflecting boundary (PRB) were incorporated with the FEM to limit the hole between recreation results and genuine application.

Basically, an extensive disadvantage of utilizing the improved FEM is that it utilizes uniform three-sided components to perform the fitting. Since planning and investigating SPR sensors unavoidably includes nano-metal particles and nanoscale waveguides, viable control of the lattice goal is vital for limiting the reproduction time and required memory limit. Along these lines, in this investigation, the object meshing method (OMM) and the boundary meshing method (BMM) were utilized to improve the FEM coinciding technique. In simple to ordinary bioelectronics built at the micrometer scale, diminishing the element of electrical transducers to the nanometer scale can essentially improve the presentation. For instance, a decrease in size can expand the force effectiveness, reaction time, and adaptability just as considering multi-useful stages. All the more particularly, forceful scaling down of transducers down to sub-micrometer and nanometer scale, particularly utilizing base up incorporated structure blocks, can empower exact one-to-one coupling between bioelectronics gadgets and individual organic elements at the cell, sub-cellular, or even sub-atomic level, and open up gadget models unrealistic with customary planar manufacture of the semiconductor business.

2 Literature Survey

The most encouraging and financially savvy configuration, because of its generally basic manufacture system, was the one proposed by Stroock, et al.: inserting microstructures in the floor of a channel to present a 3D stream collapsing as a way to blend liquids. The creators tried two distinct shapes, angled arranged edges and an amazing herringbone blender, acquiring a more homogeneous blending in with the subsequent choice. Following this strategy, a few creators built up the idea further by reenacting the conduct of the liquid inside these channels to improve the plan of miniature blenders. Different creators applied similar guideline for different applications, for example, the catch of circulating tumor cells (CTCs) and expanding objective conveyance to resistant sensors.

Foley et al. attempted to decide the impact of the herringbone blender in the authoritative of a protein (streptavidin) to the surface-functionalized with its ligand (biotin). For this situation, the creators tried a herringbone and a converse herringbone plan. The primary end was that for the underlying part of a channel (1.5 mm), there was no contrast between the herringbone and standard cross-segment diverts in normal protein authoritative.

The creators additionally noticed that the coupling design was math subordinate. Given the need to expand the association of the majority of the biofluid with the detecting surface for some recognition applications, implanted 3D miniature fluidic structures in miniature channels were planned and tried. The expanded collaboration inside the framework was tried with a standard corrosive ended SAM and amine-covered nano-circles for approval of the idea. Moreover, a novel cycle for statement of the SAM after gadget manufacture is introduced. This flexible arrangement offers the chance of utilizing similar plan for different applications where another kind of covering is required, regardless of whether it is another sort of SAM or other explicit atoms.

In 2004, Wang et al. [11, 12] revealed an early exhibit of VLS amalgamation of expanded Si and GaN nanowires in a controlled way by consecutively rehashing the impetus affidavit and nanowire development steps. The VLS development system can likewise be utilized for balanced plan and combination of wrinkled nanowire structures, where crimps are presented by an annoyance in the development cycle (for example cleansing or once again introducing reactant gases) at characterized positions with a fixed points of 120°. Additionally, by controlling dopant-balance during crimped nanowire development measure, explicit gadget work, for example, *p–n* diodes and field-impact semiconductors, can be unequivocally limited at the wrinkled intersections in the nanowires.

The ability to plan and make the previously mentioned 2D and 3D nanowire structures in a sane way has opened incredible open doors for the plan and manufacture extraordinary nanoscale bioelectronics gadgets to screen and control nano-bio interfaces [13–15]. For example, nano-sensors dependent on crimped nanowires, which will be additionally talked about in the later areas, can be covered with phospholipid

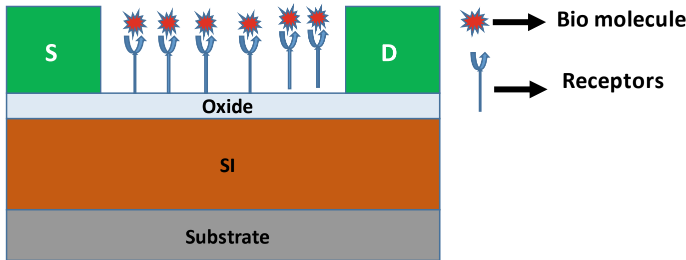

Fig. 1 Planar biosensor [16–19]

'cell-like' layers to empower tight electrical coupling with cell films for intracellular account [16–19].

3 Biosensor Arrays Using Nano-Wires

3.1 Planar Biosensor

The planar biosensor surface disposes of outside boosts to the cells brought about by substrate geology to all the more precisely reflect smooth surface climate experienced by numerous cell types in vitro. Here, a manufacture approach that consolidates nano-copy forming and a level plunging measure is utilized to planarize the outside of the PC biosensor. The below Fig. 1 shows the planar biosensor structure.

The planar PC biosensor keeps up a high location affectability that empowers the checking of live cell–substrate connections with spatial goal adequate for noticing intracellular connection strength angles and the expansions of filopodia from the cell body. The development of cell morphology during the connection and spreading cycle of 3T3 fibroblast cells is thought about among planar and grinding organized PC biosensors. The planar surface successfully dispenses with the directionally one-sided cell connection practices that are seen on the grinding organized surface. This work speaks to a significant advance forward in the improvement of mark free strategies for noticing cell measures without unintended outer natural adjustment (Figs. 2 and 3).

3.2 Cylindrical Nano-Wire Biosensor

Albeit most nanowires are round and hollow fit as a fiddle; existing base up procedures are equipped for changing their cross-sectional shape, delivering round, square, and three-sided forms. The detecting cycle begins with developing Si nanowires utilizing

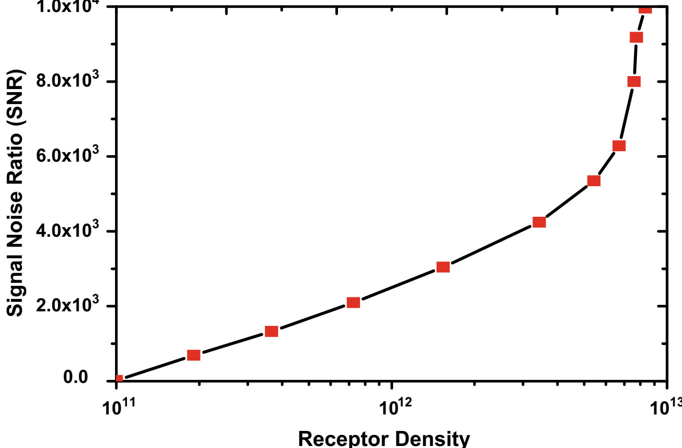

Fig. 2 SNR of biosensor in the presence of parasitic molecules

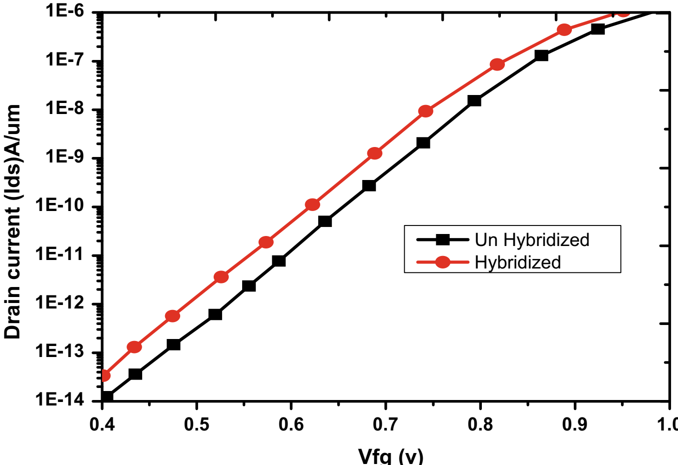

Fig. 3 Transfer characteristics I_{ds} versus V_{fg} for hybridized and un-hybridized cases

the chemical vapor deposition (CVD) strategy. Si nanowires can be filled chemically in the CVD response by means of the vapor–liquid–solid (VLS) system (Fig. 4).

Consequently, the Si nanowires suspended in ethanol arrangement are kept onto a silicon substrate. A photoresist is then turn covered onto the substrate with kept Si nanowires, and afterward, the metal cathodes are designed by the takeoff technique measure. The base up manufacture closes with passivation and surface adjustment with receptor official. The disconnection layer on the nanowire surface is handily accomplished by presenting it to air or an oxygen climate (Figs. 5, 6 and 7).

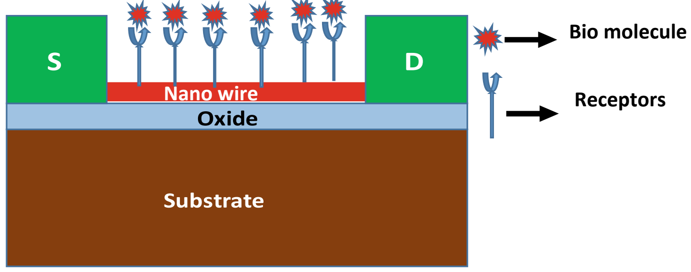

Fig. 4 Cylindrical nanowire FET biosensor [16–18]

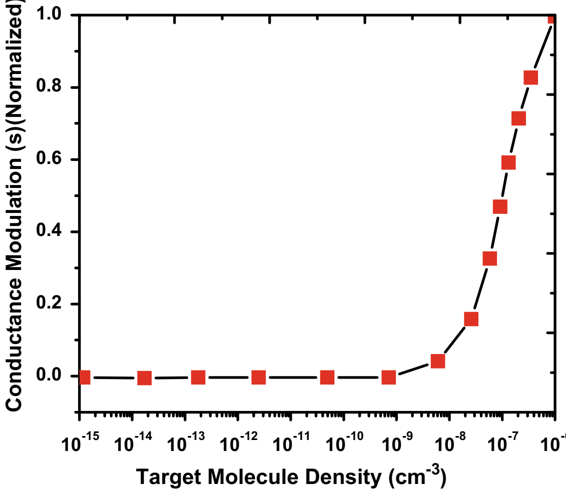

Fig. 5 Conductance modulation versus analyte concentration

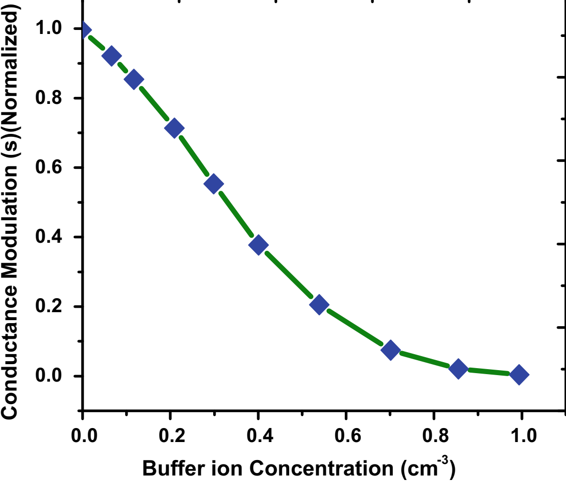

Fig. 6 Conductance modulation versus Bufferion concentration

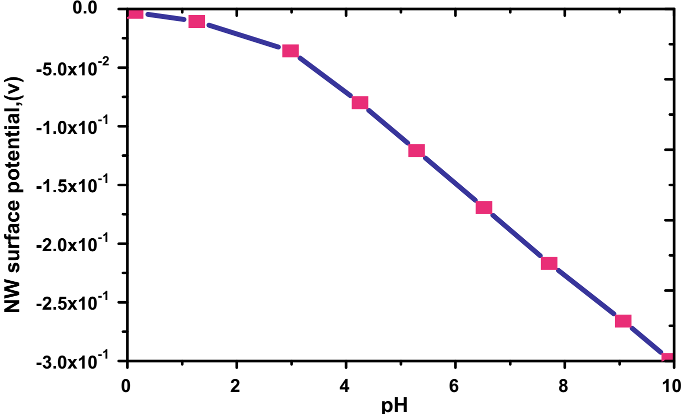

Fig. 7 Conductance modulation versus pH of buffer

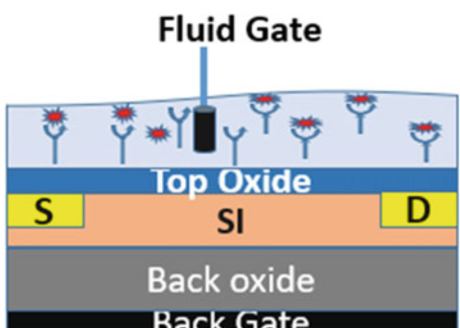

Fig. 8 DGFET-based biosensor design [16–18]

3.3 *Double Gate FET-Based Biosensor*

Recently, research on the FET-based DNA identification is massively persuading for the nano-detecting applications. Nonetheless, a wide report has been researched on single-door FETs, and a couple of endeavors have zeroed in on double gate FET (DGFETs). They zeroed in on the divert math regarding round and hollow, planar and circular state of the silicon nanowire channel to investigate the exhibition boundary for their examination (Figs. 8, 9, 10 and 11).

3.4 *Extended Gate FET-Based Biosensor*

The improvement of extended–gate–field–effect–transistor (EGFET) sprang from ISFET innovation and was first proposed by J. Van der Spiegel in 1983. Not at all like

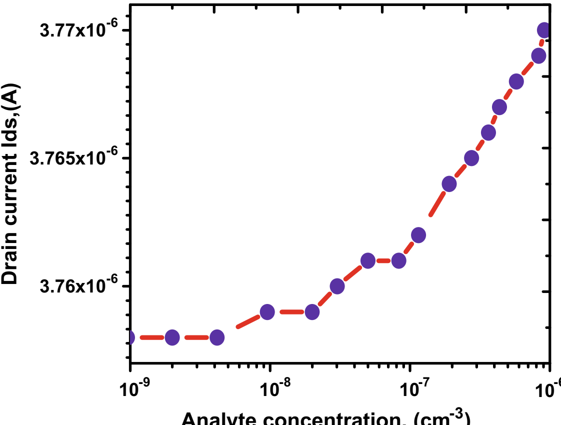

Fig. 9 Current versus analyte concentration DGFET biosensor

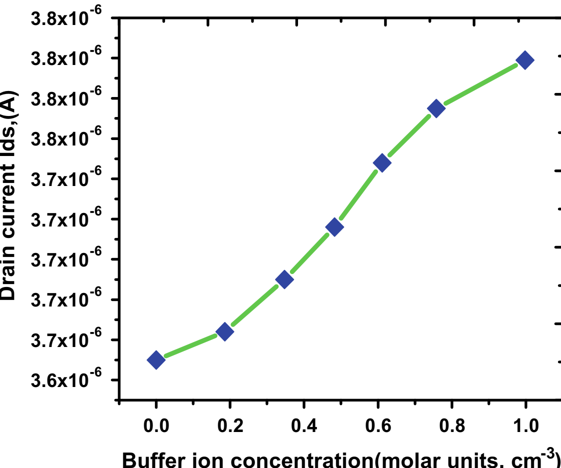

Fig. 10 Current versus buffer concentration of the DGFET biosensor

ISFET, EGFET jam the gate locale as a standard metal–oxide–semiconductor–field–effect transistor (MOSFET), and the detecting film is situated outwardly (Fig. 12).

In this manner, the action of target break down outcomes in an extra compound commitment 48 on the threshold voltage (Vth). The primary utilizations of EGFETs are related with the discovery 49 of ionic species, pH, and explicit particles (through the functionalization of delicate surfaces, for example, urea and glucose. Aside from its common use in the field of biosensors, actual sensors for high recurrence ultra-sound identification (for example hydrophone) have been acknowledged through the EGFET innovation, regularly alluded to as POSFET (piezoelectric oxide semiconductor field effect transistor) or PiGoFET (piezoelectric gate on a FET) (Figs. 13 and 14).

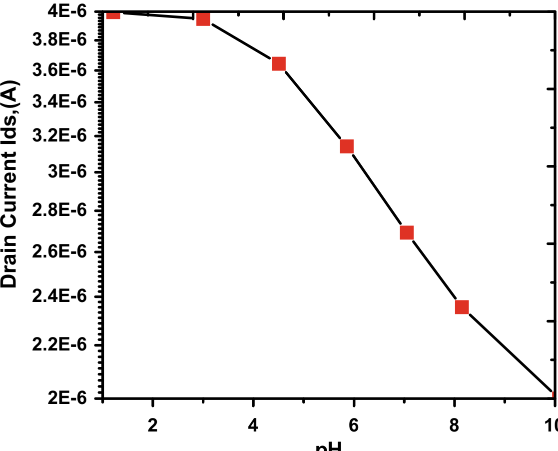

Fig. 11 Current versus pH DGFET biosensor [16–18]

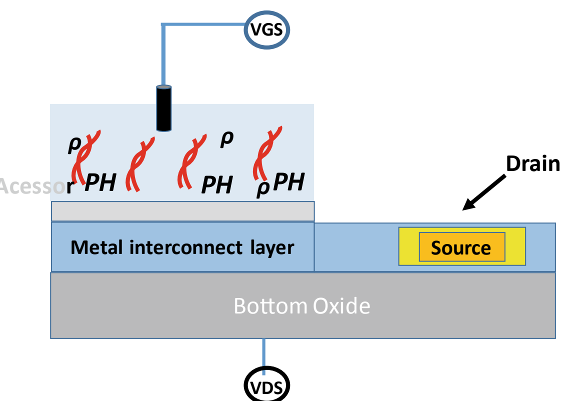

Fig. 12 Extended gate FET-based biosensor

Table 1 represents the comparison of the physical parameters which effect the performance of the above discussed different kinds of the biosensor, and from the table, it is evident that every biosensor is best at some point, and overall, they depend on the application and the type of the environment. It is our responsibility to select the biosensor that suitable for our application and conditions of working. Table 2 illustrates the performance comparison among the planar biosensor and the extended gate FET structure biosensor in terms of on current and off current and their ratio. The planar biosensor lags behind the extend gate because of the controllability of the channel then the extend gate and the signal to noise ration also high for the extended gate. The double gate structure biosensor shows a better on current then the cylindrical structure, but due to the compact model in the cylindrical, it shows better sensitivity then the double gate structure.

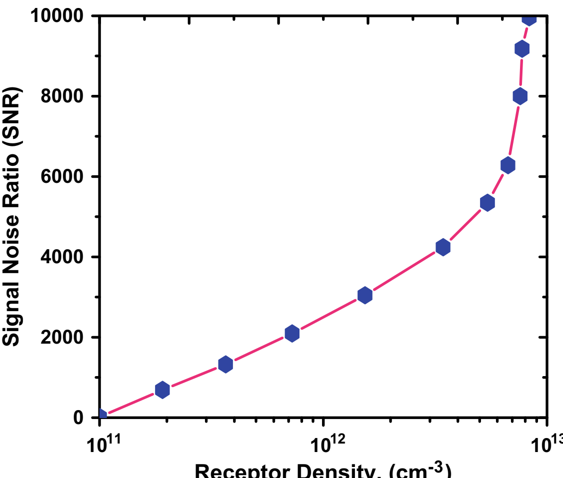

Fig. 13 Current versus analyte concentration DGFET biosensor

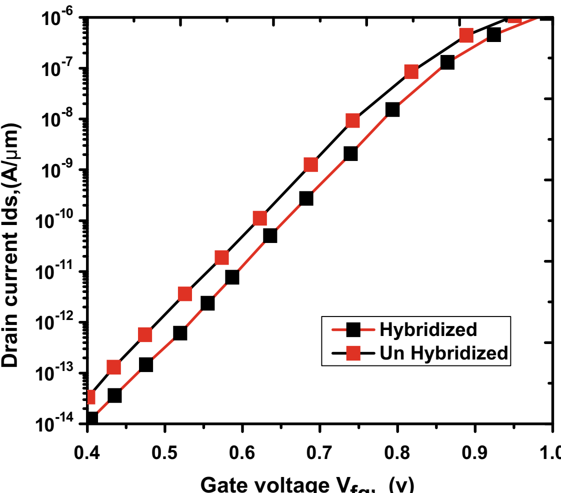

Fig. 14 Transfer characteristics Ids versus Vfg for hybridized and un-hybridized cases

The double gate and the planar biosensor show a high selectivity than the other structures of the biosensors because the interaction of the bio-molecules shows a very high selectivity for their structures.

4 Conclusion

Finally, we discussed biosensor array based on planar biosensor, cylindrical Nano wire biosensor, DGFET, EGFET. The limitations of conventional approaches are

Table 1 Performance attributes of the different biosensors

Type of biosensor	No of gates	Fabrication difficulty	Gate controllability over the channel	Sensitivity	Selectivity
Planar biosensor	1	Simple	Low	Low	High
Cylindrical nanowire biosensor	1	Medium	Medium	High	Medium
Double gate FET biosensor	2	Simple	High	High	Medium
Extend gate FET biosensor	1	High	medium	Medium	High

Table 2 Performance comparison of biosensors

Type of biosensor		On current(Ion)	Off current(Ioff)	Ion/Ioff	SNR at density of receptor (1.009E+012)
Planar biosensor	Hybridized	1.44E−06	1.18E−14	1.22E+08	4.06E+02
	Un-hybridized	1.83E−06	3.93E−14	4.66E+07	
Extend gate FET biosensor	Hybridized	5.64E−07	1.33E−14	4.24E+07	4.58E+02
	Un-hybridized	7.25E−07	4.66E−14	1.56E+07	

overcome by using these four types of biosensors. They mainly overcome the ultra-small dimensions and minimize the damage to the cells and allow for long-term recording. By using large arrays, the development of biosensor nanowire problems will be enable to use the powerful measurement platform. This includes high density multiplexed intracellular mapping activity also. From the above analysis of the different structures of the biosensor, it is clear that every structure is having its own priority in its own way like the planar structure is suitable for the high selectivity, and double gate structure is having high sensitivity, and the fabrication complexity also differs from one structure to another structure. As from the overall analysis, it is recommended that we have to choose the suitable structure for specific application. In future, we can study about the synaptic plasticity and dynamic signal processing in neural networks.

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Study of Noise Behavior of Heterojunction Double-Gate PNPN TFET for Different Parameter Variations

Karabi Baruah, Radhe Gobinda Debnath, and Srimanta Baishya

Abstract In this work, low-frequency noise behavior is studied for a proposed dual dielectric spacer-based heterojunction double-gate PNPN TFET structure. Electrical parameters of the proposed structure are investigated with regard to I_{ON} (ON-state current), I_{OFF} (OFF-state current), and SS (subthreshold swing). Noise quantity, such as noise spectral density in terms of current ($S_{ID,}$ unit A^2/Hz) and voltage (S_{VG}, unit V^2/Hz), is studied for different trap conditions and different mole fractions, lengths, and doping concentrations of the pocket material. The study reveals that the pocket parameters have a significant influence on the noise behavior of the proposed structure.

Keywords Flicker noise · Band-to-band tunneling · Heterojunction · Noise power spectral density · Subthreshold slope · Tunnel field-effect transistor (TFET)

1 Introduction

Continuous scaling of CMOS transistor for obtaining improved performances causes severe undesirable effects which leads to the investigation of the reliability issue of device properties [1]. Many researchers have been working on new devices for the last few decades to improve the characteristics of device performances [2, 3]. Tunnel FET is one such device that can withstand against short channel effects and yield improved features [3–5]. TFET uses an interband tunneling mechanism for current conduction rather than thermionic emission, thus improving ON-state current, subthreshold swing, and current switching ratio. However, due to tunneling, the ON-state current is below the ITRS limit in TFET, which is the primary concern for the researchers [4]. The double-gate TFET structure can enhance the control over the channel compared to the single-gate structure, thereby improving the ON-state performance of the device [6]. A recent study on various TFET structure also provides promising results in the nanometer regime [7–11].

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Low-frequency noise is a significant concern nowadays in the digital application of the semiconductor device; because of the shrinkage of the device dimension, low-frequency noise in a device increases [12]. Noise creates current and voltage fluctuations in electrical circuits, and it is a random phenomenon. In comparison to other electrical parameters, the analysis of noise impact in various TFET structures is very negligible, and hence, this area needs more attention to check the reliability of the device. Some work has been done in this area [13–16] which gives a promising result on noise impact over various TFET structures. In this work, noise analysis of the proposed heterojunction DG TFET at low frequency is presented with some parameter variation.

2 Dimension and Simulation Setup of the Proposed Device

The suggested double-gate structure's cross-sectional view in two dimensions is shown in Fig. 1. The structure contains a $Si_{1-x}Ge_x$ layer (pocket) between the channel and the source region [17, 18]. A lower energy bandgap semiconductor (germanium) is used in the source region to enhance the ON-state performance of the device [19]. A high *k* dielectric material HfO_2 (dielectric constant, 22) with thickness 2 nm (EOT = 0.35 nm) is employed as a dielectric between the gate and body for further improvement of the performance of the proposed device [20]. The length and the thickness of the body part of the proposed device are 82 nm and 10 nm, respectively, with a channel of 22 nm length. A metal of work function 4.25 eV is used as a gate for the proposed structure. The gate has a 4-nm overlap on the source and a 2-nm underlap on the drain to obtain a high ON-state current and to overcome unwanted ambipolar current with minimum leakage. A high k material HfO_2 of length 2 nm, followed by a low *k* material SiO_2 of length 6 nm, is used as spacer material on both sides of the gate over the body [21]. The proposed structure is basically a PNPN structure which has following doping concentration: source (1×10^{20} cm^{-3}, p-type), SiGe layer (5×10^{18} cm^{-3}, n-type), channel (1×10^{16} cm^{-3}, p-type), and drain (1×10^{18} cm^{-3}, n-type). All the values mentioned above are optimized for getting the best device performance. A list of parameters dimension is mentioned in Table 1.

The simulation process is carried out using the SENTAURUS TCAD 2D device simulator [22]. Various models have been utilized in the simulation process, such

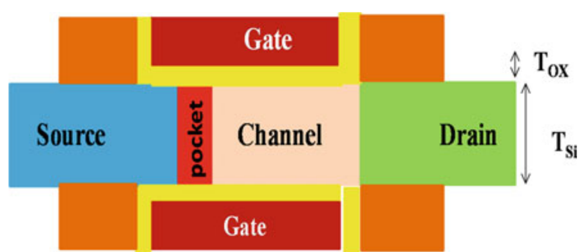

Fig. 1 Cross-sectional view of the proposed PNPN DG structure

Table 1 List of parameters dimension used in device simulation

Device parameters	Dimension
Channel length	22 nm
Body thickness (T_{Si})	10 nm
Gate dielectric thickness (T_{OX})	2 nm (EOT = 0.35 nm)
Source doping (N_S)	1×10^{20} cm^{-3}
Pocket doping (N_P)	5×10^{18} cm^{-3}
Channel doping (N_{Ch})	1×10^{16} cm^{-3}
Drain doping (N_D)	1×10^{18} cm^{-3}
Pocket length (L_P)	2 nm
Gate work function (WF)	4.25 eV
Trap density	1×10^{14} cm^{-2} eV^{-1}
Mole fraction of SiGe	0.3
Gate–source overlapped	4 nm
Gate–drain underlapped	4 nm
High k spacer (HfO_2) length	2 nm
Low k spacer (SiO_2) length	6 nm

as the nonlocal band-to-band tunneling model, bandgap narrowing model, doping-dependent mobility model, Shockley–Read–Hall recombination model, and Fermi–Dirac statistics. To analyze the noise impact, traps are considered at the oxide–semiconductor interface with concentration 1×10^{14} cm^{-2} eV^{-1}. Gaussian distribution of trap with energy level 0.035 eV is considered for all the cases [23, 24]. Flicker noise, also known as 1/f noise, is used at a frequency of 1 MHz for the simulation process [25].

3 Results and Discussion

The drain current characteristic with the variation of the gate voltage of the proposed device is shown in Fig. 2 for three distinct drain voltages. The result indicates that the ON-state current of the device increases with an increase in drain voltage. However, the unwanted ambipolar current also increases with drain voltage. Hence, an optimized value of 0.7 V is considered for drain voltage for the remaining simulation. The proposed structure gives an ON current of 1.94×10^{-3} A/µm and an OFF current of 1×10^{-16} A/µm with a switching ratio of 10^{11}.

Figure 3 shows the drain current variation with gate voltage for different types of traps present at the interface. The figure shows that the trap impact is more in the subthreshold area in comparison to the superthreshold area. The ON-state current is almost constant for donor and acceptor type of trap charges as well as no trap condition. However, leakage is low when interface traps are not present. In the presence

Fig. 2 Transfer characteristics, i.e., $I_{DS}-V_{GS}$ graph of the proposed device at three different drain voltages

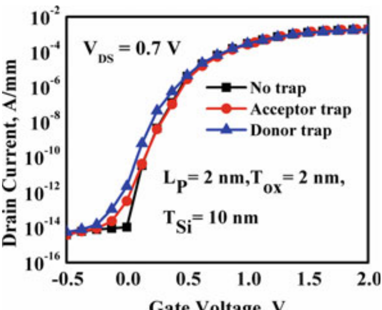

Fig. 3 $I_{DS}-V_{GS}$ characteristics for different conditions of interface trap

of donor traps, the device has a higher leakage current compared to the presence of acceptor traps.

Noise power spectral density is a necessary quantity to analyze the noise impact on a device, which gives details about how noise power is distributed in frequency [26]. Drain current noise power spectral density (S_{ID}) vs. gate voltage (V_{GS}) characteristics for different mole fractions are shown in Fig. 4a and b for the presence of both donor

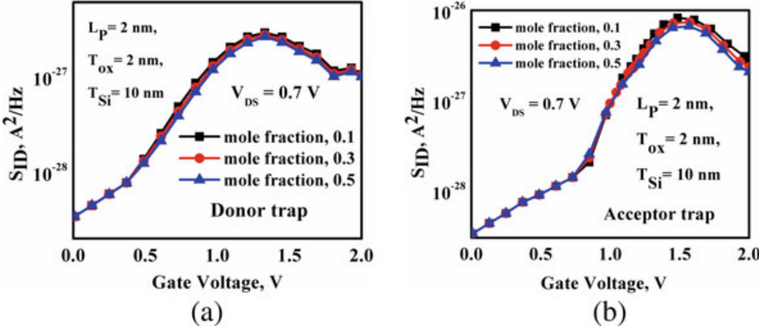

Fig. 4 $S_{ID}-V_{GS}$ graph for different mole fractions of silicon germanium layer in the presence of **a** donor trap and **b** acceptor trap, respectively

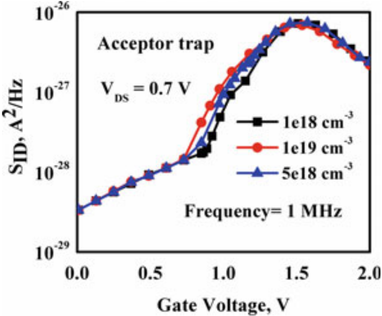

Fig. 5 S_{ID} versus V_{GS} curve for different pocket doping concentrations

and acceptor traps, respectively. From the figure, it can be visualized that the noise power spectral density first gradually increases up to some peak value and then decreases rapidly in both the case. However, the noise power is less when the mole fraction is increased.

Figure 5 shows how pocket doping concentration variations affect noise performance. Three doping concentrations 1×10^{18} cm^{-3}, 1×10^{19} cm^{-3}, and 5×10^{18} cm^{-3} are considered for this purpose, and it can be noticed that up to the peak value, the noise power is minimum for lower pocket doping; however, after the peak value is reached, the noise power is minimum for higher doping. At low gate voltage, pocket doping concentration variation has a negligible impact on noise power.

Figure 6 describes the S_{ID} versus V_{GS} curve for different pocket length (2 nm, 4 nm, and 6 nm) conditions. The figure shows that noise is less when the pocket length is small (2 nm) for the low gate voltage range. But the noise will increase at high gate voltage due to a higher number of carrier injection and trapping de-trapping mechanism.

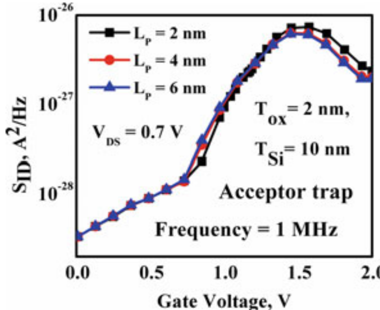

Fig. 6 S_{ID} versus V_{GS} for different pocket length conditions

4 Conclusion

This work explores the noise behavior of the proposed PNPN structure with different parameter variations. The proposed design is optimized before this work to get the best results of ON current, OFF current, and ON–OFF current ratio. An optimum value of I_{ON}, 1.94 mA/μm, and the I_{ON}/I_{OFF} of 1.81×10^{11} have been obtained from the optimized proposed structure. The low-frequency noise behavior of the optimized proposed structure is studied considering flicker noise at 1 MHz in the presence of interfacial trap charges. The study shows that the pocket doping concentration, pocket length, and mole fraction variation affect device performance at low frequency.

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Analysis of Optical Effects of Different Anodes on Organic Light-Emitting Diode

B. M. Chaya, Koushik Guha, A. Vaishnavi, and K. Narayan

Abstract In this work, the effect of replacing traditional indium tin oxide (ITO) anode with different anode materials is reported. The detailed simulation is conducted on organic light-emitting diode (OLED) consisting of commonly used emissive or organic layers with tris(8-hydroxyquinoline) aluminum (Alq3) at an operating wavelength of 540 nm. Different device simulations using aluminum zinc oxide (AZO), zinc mono-oxide (ZnO), graphene (7 nm/12 nm), and silver (Ag) anode materials with different work functions are modelled and simulated. For measuring OLED's optical results, the finite difference time domain (FDTD) approach was used. The angular distribution of OLEDs with reference to viewing angle with different anodes is reported. The results show the optical effects of the anode material with Graphene has better enhancement in light output compared to other materials. This work shows the far field contours of all the anode materials that improve light production and that optimum emission from an OLED to check the alternative to indium tin oxide anode material.

Keywords Finite difference time domain · Far-field intensity · Organic light-emitting diode

1 Introduction

OLEDs had already emerged in display categories and lighting systems due to quick response time, enhanced color emission, and broad viewing angle. The advantages of the use of inorganic materials over organic materials is fluorescence quality. The rapid radiative decay of the molecular orbital states induces light in emissive materials. The color of the light on your screen shows the energy difference between molecular

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orbitals. High-function metal (anode) includes the highest occupied molecular orbital level of active material as a hole-injection layer. A majority of OLEDs use ITO as anode ranging from 4.5 to 5 eV. The researchers and the science world attempting to analyze different OLED parameters, such as performance, improvement in panel products, operating reliability, etc. [1, 2]. Researchers highlighted the growth of different transparent conductive oxide (TCO) materials as a choice to widely utilized ITO-based anode. While ITO provides better optical clarity, and its voltage levels are hard to monitor. The ITO is dangerous, expensive, and non-flexible focus on fixing transport and injection of load at OLED's electrode and organic interface [3].

Numerous TCO materials for anode use on the OLEDs like zinc mono oxide (ZnO), indium zinc oxide (IZO), hydrogen zinc oxide (HZO), gallium zinc oxide (GZO), etc. The work involved Al, Ga substituted for Zn on ITO anode thin films as stated in [4]. The research group stated that OLED is made on GZO as anode and performs extremely over AZO as anode. Another research team substitutes ITO with GZO-based thin films from laser deposition, and these OLEDs are equally effective than ITO-based OLED as outlined in [5].

Researchers Park et al. team applied atomic layer deposition Al-doped ZnO films and found higher external quantum efficiency [6]. They have enhanced reliability [7] and enhanced power performance of HZO, GZO, etc. Due to higher sheet resistance and lower chemical stability, AZO-based OLEDs are unable to show optimal performance when voltages applied are below 8 V as outlined in [8].

The use of a buffer layer of homogeneous AZO can enhance OLED output is described in the literature [9] and Graphene based OLED research has been showcased in [10, 11]. The light outcoupling efficiency of the OLEDs with silver nanomesh electrodes tested and simulated in [12]. In the research work as demonstrated in [13], the ITO layer in conventional multilayer OLED has been replaced by thin film-based ZnO material. The electrical and optical specifications of the ZnO anode layer are extracted from the available material directory. ZnO anodes can increase the reliability of the system at a lower cost per area per unit. ZnO's work function is consistent with the material of the hole transport layer (HTL) which assists at the metal- emissive layer interface with an effective electron transfer.

A prototype in the paper [14] that the manufacture of flexible active matrix is directly applicable to Graphene anode OLEDs have been developed. Besides the technology, these displays must also be fabricated and deal with various technical problems caused by the technology. On a glass support, an oxide TFT was developed. Displays containing pixelated graphene are available on the TFT displays. In this research, the suggested approach is believed to imply substantial progress in the realization of the ultra-thin flexible and transparent display, where the distinctive features of graphene are distinctive.

A comparative analysis for the thorough discussion of the graphene-based analysis was carried out in the work [15]. When making organic light-emitting diodes, the materials as an electrode, it was discovered that the derivatives of graphene may be seen as a better alternative to enhancing the efficiency of OLEDs. In addition, if one is looking forward to the optimization of the unit, graphene oxide would be advisable. The development of indium-free OLEDs is recorded using transparent metal mesh

in [16] that includes top-based electrodes that include choice of metal, Ag, Au, or copper (Cu) and also outline tunability of work function of metal electrodes that allows the energy levels inside the system to be subtly balanced.

In this work, the optical effects of different anode materials with different work function is analyzed and simulated. This helps to find an alternative anode material to be used instead of ITO.

2 Design of Organic Light-Emitting Diode

Figure 1 demonstrates the OLED structure modelled with Lumerical finite difference time domain (FDTD). OLED structure contains a thin-layer active organic layer embedded in the electrons from cathode and inject holes. The transport layers and organic layers, around 200 nm, are located between anode and cathode, and organic layer, Alq3-tris (8-hydroxyquinoline) aluminum present in the OLED structure is designed to emit green light. The materials used in OLED and its refractive index, work function, thicknesses are as taken from research paper [17]. The OLED introduced in this paper, aimed at achieving maximum light output of fluorescence light emitting at 540 nm operating wavelength. The OLED with different anode materials is modelled as given in Table 1. The OLED modelling of different devices

Fig. 1 Design of the Structure of an OLED

Air Medium
Glass Substrate
Anode material
Hole Injection Layer (HIL)
Hole Transport Layer (HTL)
Organic Layer/ Emission Layer
Hole Blocking Layer (HBL)
Cathode material

Table 1 OLED devices with different anode materials

Device	Anode materials	Work function (eV)
Device A	Zno	4.82
Device B	Graphene (7 nm/12 nm)	~4.6
Device C	ITO	4.4 -4.5
Device D	AZO	3.7–4.9
Device E	Ag	4.3

mentioned in table is modelled and simulated using commercially available Lumerical FDTD software [18]. Different OLED devices such as Device A/B/C/D/E with different materials such as ZnO/Graphene/ITO/AZO/Ag respectively is modelled. The modelling is done using FDTD method to find an alternative material to ITO.

As shown below, the mathematical modeling of the angular distribution of the far-field intensity is derived from Eq. (1) [17]

$$|E_2|^2 = \left[\left(T_s \times |E_s|^2\right) + \left(T_p \times \left|E_p\right|^2\right)\right]\frac{d\theta_1}{d\theta_2}, \quad (1)$$

The light extraction efficiency (LEE) or far-field intensity of an OLED is ratio of light intensity for patterned versus unpatterned OLED designs is obtained by placing far-field monitor near glass substrate/air interface. The emissive/organic layer of an OLED that escapes from air above the substrate air interface within range of viewing angles as shown in Eq. (2), to obtain angular distribution of light with respect to viewing angle [18].

$$\text{LEE}_{\text{enhancement}} = \frac{\text{LEE}_{\text{pattern}}}{\text{LEE}_{\text{nopattern}}} \quad (2)$$

3 Numerical Simulation and Results

The far-field intensity contours of the OLED are shown in Fig. 2a–e, each device with various anode materials. The findings reveal that the tabulated anode materials though it has slight variations in the work function can be considered as an alternative to ITO anode material.

Figure 3 shows angular distribution with reference to viewing angle of different OLED devices with different anode materials is shown. The analysis is carried out for different anode materials having different work functions. The electric field intensity plot for various anode materials is observed with reference to viewing angle.

Table 2 shows the detailed analysis of OLED devices with varying electric field intensities for different anode materials. The OLED devices are modelled to obtain electric field intensity of each device. It is clear from the analysis that the graphene could be an alternative to the ITO anode material at an operating wavelength of 540 nm.

4 Conclusion

In this work, the optical effects of different anode materials on OLED is analyzed and simulated. The FDTD method is used to calculate the far field or LEE an OLED.

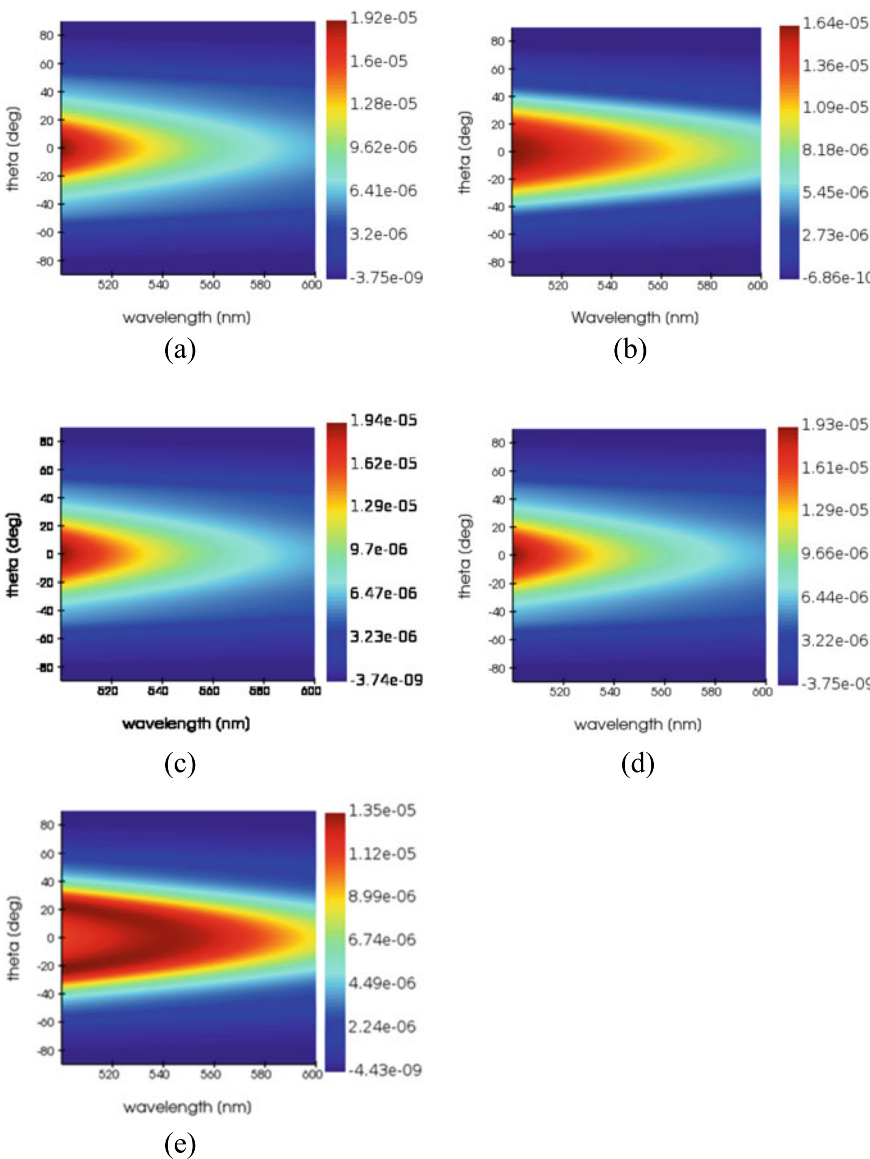

Fig. 2 Far-field contours of electric intensity of OLED **a** Device A, **b** Device B, **c** Device C, **d** Device D and **e** Device E

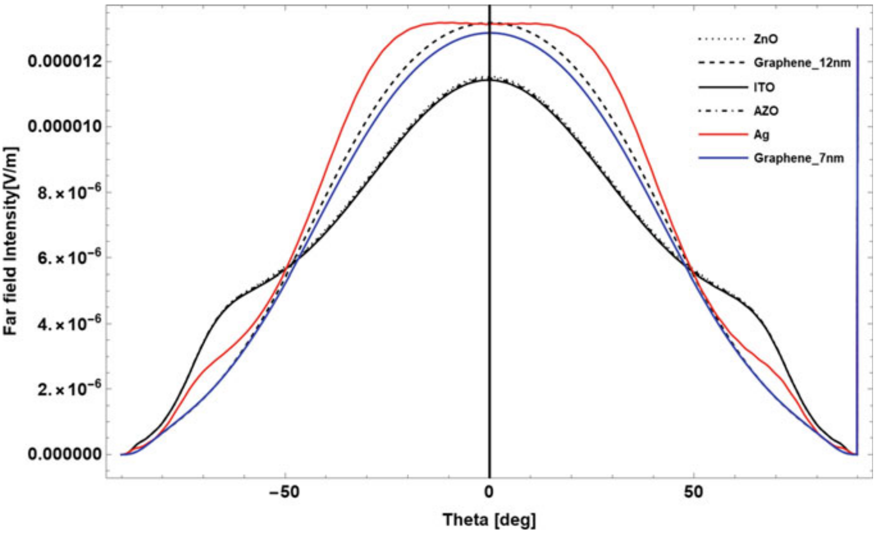

Fig. 3 Angular distribution of various anodes on OLED

Table 2 OLED devices with varying electric field Intensity

Device	Anode materials	Electric field intensity (V/m)
Device A	Zno	1.15382×10^{-5}
Device B	Graphene (7 nm/12 nm)	1.31877×10^{-5}
Device C	ITO	1.14346×10^{-5}
Device D	AZO	1.14932×10^{-5}
Device E	Ag	1.31447×10^{-5}

The angular distribution of OLEDs with reference to viewing angle with different anodes is reported. The results show that Graphene could be an alternative to ITO. The work also shows the far filed contours of different devices in an OLED with different anode materials. Further, there is still large scope for further work to find other alternatives of ITO anode material in an OLED.

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Analysis and Design of Surface Plasmon Resonance Waveguide for Sensing Application

N. K. Suryanarayana, K. Asha, Koushik Guha, and Narayan Krishnaswamy

Abstract A surface plasmon resonance waveguide sensor operating in the visible wavelength range is presented for refractive index-based sensing. The silver material is used because of its chemical stability and its strong electromagnetic fields on surface of the nanoparticle. The simulation and modeling of surface plasmon resonance sensor are discussed. The aluminum oxide surface coating material improves the resonance of the sensor because of its stable material properties in optical and chemical application. The three modes of the sensor discussed here are transfer electric, transfer magnetic and the surface plasmon waveguide mode. The effective index value of 1.5178 is observed for the surface plasmon mode of the SPR waveguide sensor. The attenuation loss of 21 dB/cm is obtained at visible wavelength. The sensitivity when averaged for two analyte refractive index is 354 nm/refractive index unit (RIU). The proposed surface plasmons resonance sensor is used as refractive index-based sensor for environmental and chemical monitoring. This proposed work can be used to sense analyte refractive index based on the variation of the change in the resonant wavelength.

Keywords Surface plasmon resonance · Waveguide mode · E-field intensity · Loss · Effective index · Sensitivity

1 Introduction

Surface plasmon resonance sensor constructed using surface plasmons are important designs in the lab-on-a-chip (LOC) application. Waveguide-coupled devices have applications in optical coupling as a coupler and Mach–Zehnder interferometer waveguide devices. The silver-coated magnesium fluoride is used as a buffer layer.

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The operating wavelength is 500–600 nm [1]. The surface plasmon resonance (SPR) mode is obtained by coating the different dielectric materials on the surface of the metal in the sensor. These devices are used in bulk refractive index (RI) sensing [2]. The materials such as silver–magnesium fluoride (Ag-MgF2), gold–silica or silver–silica are the material of interest in surface plasmons [1, 2].

The interface between the metal and dielectric place an important role in the SPR waveguide sensor. Such sensor design along with transfer magnetic modes are of most important in recent years [3–5]. The SPR was first explained by Otto configuration in 1986, and later other types of configuration become most popular including the concept of prism coupling also called as Kretschmann configuration or also called as attenuated total reflection (ATR) method. These configurations are used in SPR devices, and these includes waveguide coupling, resonant waveguide grating structure and optical fiber coupling [6, 7].

The SPR waveguide sensing devices include optical ring resonator [8, 9], Mach–Zehnder interferometer waveguide [1], metal strip-based waveguides [10, 11], dielectric waveguide [12], metal insulator metal [13] and metal dielectric metal [14] and also polyester overhead projector (OHP) sheet waveguide [15]. The sensitivity of the SPR sensor is an important factor when sensor used in the LOC application or in point-of-care diagnostic application. The different methods are used for sensitivity measurement such as absorbance-based sensing and refractive index-based sensing [13, 16–19]. SPR also finds application in communication system. One such example is graphene-based attenuator using concept of surface plasmon polaritons excitations [20]. The plasmon waveguide with gap can be constructed using the metal Ag electrodes used in the nano-antenna design [21].

The application of SPR devices includes microfluidic for multiple analyte sensing [22], affinity-based biosensor for measuring DNA, RNA and proteins. SPR also used in cell-based detection analysis in the field of proteomics, tumor DNA markers and protein biomarkers [23].

Section 1 is introduction to the SPR waveguide sensor. Section 2 gives details about the surface plasmons. Section 3 is about the design and modeling. Section 4 is the result analysis for the design. Section 5 is about the conclusion of the work carried out.

2 Surface Plasmons

Surface plasmons are constructed using metal and dielectric materials. If only metal and dielectric is used, then it is called as conventional SPR. The Maxwell's equation is used to solve electric field decaying phenomenon. Surface plasmon biosensor can be broadly classified as SPR, long SPR, waveguide-coupled SPR and coupled plasmon waveguide resonance.

In waveguide-coupled SPR sensor along with transverse electric (TE) and transverse magnetic (TM) mode, we observe the other mode know as surface plasmon resonance mode. The electric filed present in the surface plasmons is described by

Eq. (1).

$$E = E_0^{\pm} \exp\left[+i(k_x x \pm k_z z - \omega t)\right] \quad (1)$$

In the surface plasmons, " + " is for $Z \geq 0$, "–" for the $z \leq 0$, k_z as the imaginary axis. The combination of positive and negative charges produces the electric field with exponential decay as shown in Fig. 1. The wavevector k_x appears parallel to the x direction. $k_x = {}^{2\pi}/_{\lambda}$ where the λ is the plasmon oscillation wavelength.

From the Maxwell's equation, we can write Eq. (2) for the retarded dispersion relationship for the metal with dielectric function ε_1, adjacent to air or vacuum with dielectric value as ε_2. The rearranged equations are given in (3) and (4).

$$D_0 = \frac{k_{z1}}{\varepsilon_1} + \frac{k_{z2}}{\varepsilon_2} \quad (2)$$

$$\varepsilon_i \left(\frac{\omega}{c}\right)^2 = k_x^2 + k_{zi}^2 \quad (3)$$

$$k_{zi} = \left[\varepsilon_i \left(\frac{\omega}{c}\right)^2 - k_x^2\right]^{1/2} i = 1, 2, \ldots \quad (4)$$

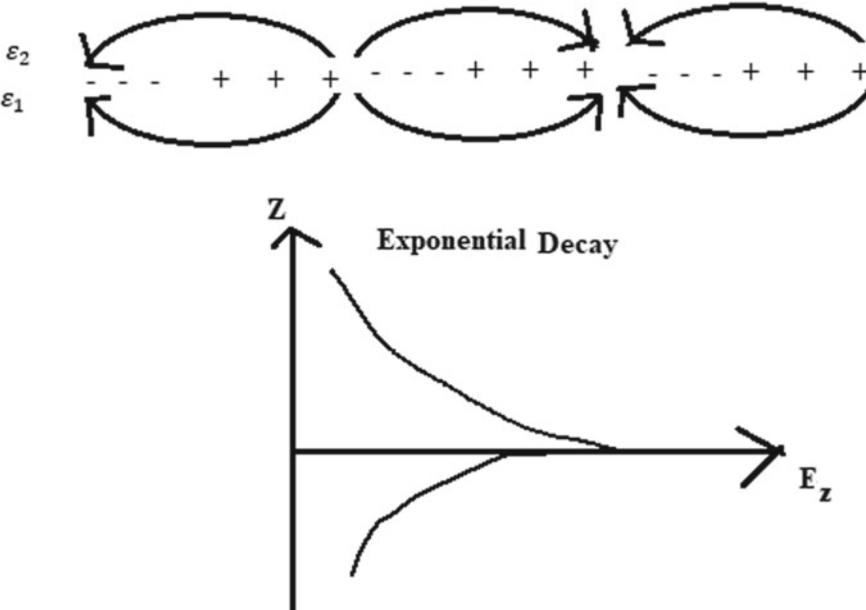

Fig. 1 Electric field with exponential decay

The wavevector k_x is continuous through the interface. The surface plasmon wave (SPW) and its propagation constant are given by Eq. (5) [7].

$$\beta_{SP} = k_0 \sqrt{\frac{\varepsilon_1 \varepsilon_2}{\varepsilon_1 + \varepsilon_2}} \tag{5}$$

where in Eq. (5), k_0 is known as wavenumber. ε_1 and ε_2 are known as metal relative permittivity and dielectric permittivity.

3 Design and Analysis

The design of the SPR biosensor design is explained in this section. The design parameters are listed in Table 1. The operating wavelength is used in the visible wavelength for the simulation of the SPR waveguide (SPRW) sensor [4].

3.1 *Design of SPR Waveguide Sensor*

The SPR sensor is modeled using mode structure shown in Fig. 2.

Table 1 Refractive index of the material

S. No	Parameters	Thickness value (μm)	Refractive index
1	BK7 glass substrate	10	$1.5151 + i1.2122e^{-8}$
2	Waveguide layer[a]	2	$1.521 + i0$
3	Al_2O_3 Dielectric layer	0.3	$1.70 + i0$
4	Silver metal coating	0.04	$0.056253 + i4.2760$
5	Biolayer (Hemoglobin)[b]/air	1	$1.3373 + i1.000$

[a]Waveguide layer (soda lime silicate glass) layer
[b]Biolayer is a 260 g/l concentration of hemoglobin at room temperature 23 °C [24].

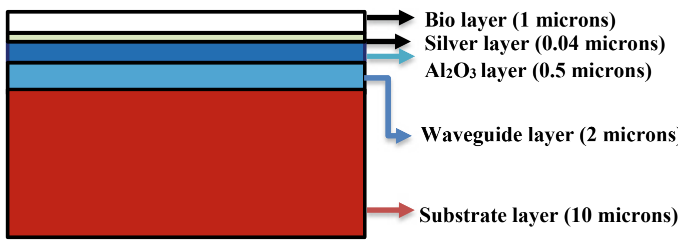

Fig. 2 Structure of SPR waveguide sensor

The glass substrate with 10 μm width and 20 μm length and 1 μm height is used in the simulation [2]. The doped glass polymer is used as waveguide layer which has RI value of 1.521. The waveguide layer is a soda lime silicate glass polymer.

The Al_2O_3 dielectric layer is used in between silver metal and waveguide, which has refractive index of 1.71 [25]. The Johnson and Christy silver metal are used in the design [26]. The biolayer used is blood, and its refractive index value in the visible range is given by 1.3645 at 546 nm [27]. The biolayer has 1.3373 refractive index 260 g/l concentration of hemoglobin at room temperature 23 ºC [24].

The fabrication steps of SPR waveguide sensors include a glass substrate BK7 which has many applications in optics, prism and also in semiconductor industry. A waveguide layer is a soda lime silicate glass polymer with chemical composition of 78.41% of silicon dioxide (SiO_2), 12.14% of sodium oxide (Na_2O) and 13.05% of calcium oxide (CaO) which is fabricated. [28]. The Al_2O_3 is deposited with vacuum evaporation method. A second overlayer was evaporated across the channel waveguide to form SPR waveguide [1].

4 Result Analysis

Eigenmode solver used in the modeling and simulation of the waveguide-coupled SPR mode biosensor. The material index field profile of the proposed waveguide SPR senor is shown in Fig. 3. The BK7 glass substrate refractive index used is 1.5151.

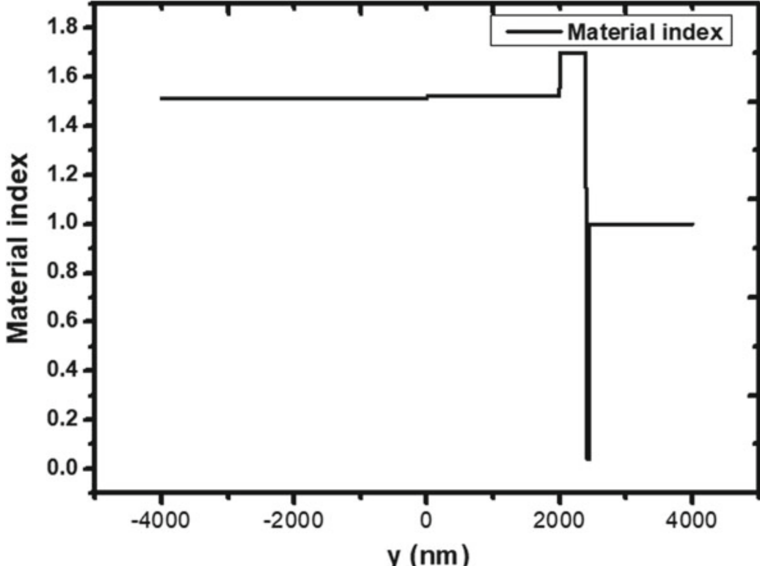

Fig. 3 Material index profile of SPR waveguide sensor

The polymer layer has RI of 1.521, and the Al_2O_3 dielectric layer index is 1.70 [29], and if sensor is used with bulk or biolayer, the index value changes.

The $Al_2O_3$is the surface coating material used to improve the response of the sensor designed in the polymeric waveguide. It improves the monotonic behavior of the device; hence, Al_2O_3 is a stable material used in electrical and optical application. It is used as a barrier layer and shows good resistance to chemicals or organic material used in the sensor. The analyte examples include ethanol water mixture, blood and glucose. The sensing of the aqueous polar solution is reported with gold SPR waveguide [29]. The Al_2O_3 is also used as coating material for sensing humidity in environmental monitoring application. The analytes considered for modeling the design are blood, albumin solution in water and hemoglobin solution in water at 24 °C temperature [27].

Modal analysis is performed by using eigenmode solver. The three modes will be observed after the simulation. The first one is surface plasmon (SP) mode and other two are transfers electric (TE) and transfers magnetic (TM) waveguide modes. The surface plasmon mode has higher losses compared to waveguide modes. The waveguide modes are confined to polymer waveguide layer. The electric field intensity plot for SPR sensor is shown in Fig. 4 for three modes.

The variation of effective refractive index with respect to the wavelength is shown in Fig. 5. The effective index value of 1.5178 is observed for the surface plasmon mode. The high loss is observed at this mode, and the highest electric filed intensity is observed near the silver layer. Since we have three modes present in the waveguide sensor, TM mode suffer with very high loss at operating wavelength 550 nm because

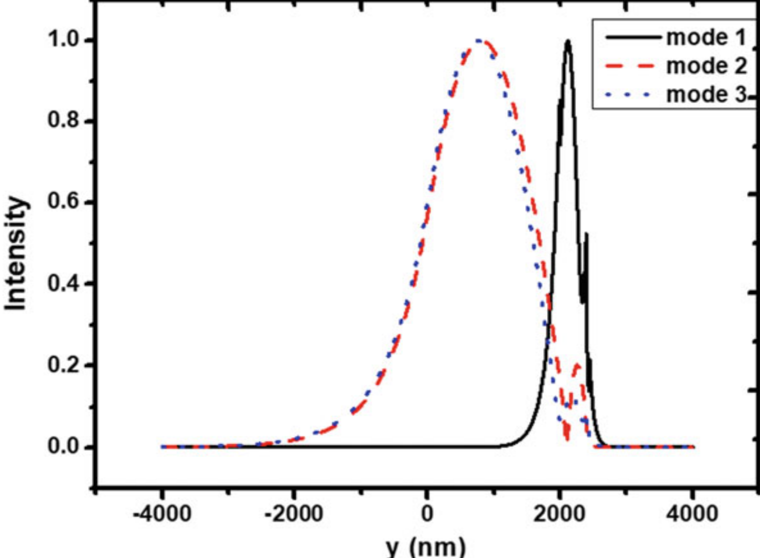

Fig. 4 Modes in the waveguide-coupled SPR sensor

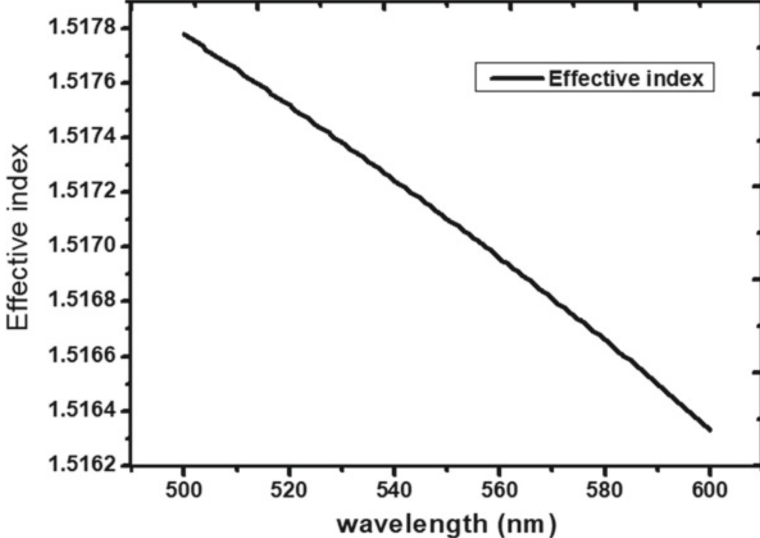

Fig. 5 Effective index versus wavelength

energy from the TM waveguide mode will couple light into the high loss SP mode. The 1.5180 dB/cm loss is observed for TM equation mode of the SPR waveguide sensor.

The loss 21 dB/cm is obtained at 550 nm wavelength for SP mode, and it is a lesser attenuation loss obtained compared to the loss discussed in Lavers et al. article [1]. The variation of real value of loss sweep versus wavelength for different analyte refractive index at different wavelength is shown in Fig. 6

The sensitivity of waveguide-coupled SPR sensor is given by Eq. (6)

$$\text{Sensitivity} = \frac{\nabla\lambda_{\text{peak}}}{\nabla n_a} \tag{6}$$

The sensitivity is defined as the change in the resonant peak wavelength to the change in the analyte refractive index. The sensitivity values calculated for the SPR waveguide sensor are given in Table 2 along with the resonant peak wavelength. The average sensitivity of the sensor is 354 nm/refractive index unit (RIU).

The proposed SPR waveguide sensor shows the highest sensitivity of 410 nm/RIU, at the analyte RI of 1.3449. The resonance peaks are found at wavelength of 540.984, 548.983, 556.18 and analyte refractive index of 1.3449, 1.3645 and 1.3885, respectively, as shown in Table 2 [24].

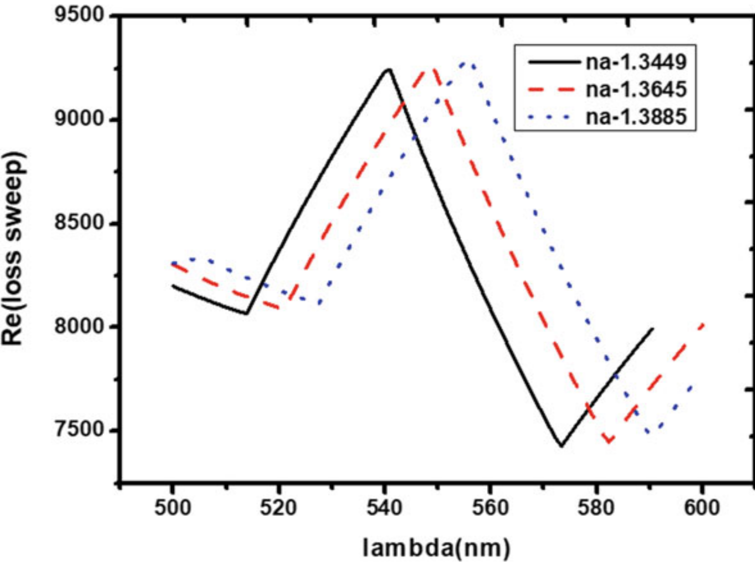

Fig. 6 Real value of loss versus wavelength lambda

Table 2 Performance analysis for different analyte refractive index

S. No	Analyte	RI	Sensitivity (nm/RIU)	Resonant peak wavelength (nm)
1	Albumin solution in water (55 g/l)	1.3449	410	540.984
2	Blood	1.3645	299.875	548.983
3	Hemoglobin solution in water (260 g/l)	1.3885	–	556.18

5 Conclusion

The design and simulation of SPR waveguide mode sensor are designed. The effective index value is 1.5178 for surface plasmon mode. The designed sensor is excited for surface plasmon mode by using operating wavelength in the visible range. Three modes are observed in the SPR waveguide sensor, and they are TE mode, TM mode and SP mode. The 21 dB/cm loss is observed for SP mode, and 1.5180 dB/cm loss is found for the other two modes of the sensor.

The Al_2O_3 is the dielectric surface coating material used to improve the response of the sensor designed in the polymeric waveguide. The analyte RI range is 1.3449–1.3885. The average sensitivity of the sensor is 354 nm/refractive index unit (nm/RIU). The proposed SPR waveguide sensor finds the application in the analysis of the different analytes based on the refractive index sensing.

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Iterative Approach for Low Actuation Voltage RF MEMS Switch

Lakshmi Narayana Thalluri, M. Koti Reddy, Shaik Rahil Hussain, G. Chandra Reddy, S. S. Kiran, and Koushik Guha

Abstract In this paper, we have investigated high isolation and low actuation voltage offering triangular membrane-based shunt capacitive RF MEMS switch. Unlike conventional analysis, here we have extended the switch design up to the packaging stage. The triangular membrane is designed with slot and perforation. The triangular membrane is micromachined with a gold (Au) thickness of 0.5 μm, the air gap is 3 μm, and the eventually required actuation voltage is 2.4 V. The membrane resonant frequency is 57.5 kHz. Because of the incorporation of multiple triangular membranes (M_1 and M_2) and HfO_2 as a dielectric material, the switch is offering high isolation of −80 dB. The overall switch has six pins, i.e., RF_{in}, RF_{out}, VB_1, VB_2, GND_1, and GND_2.

Keywords Vibration analysis · RF MEMS switches · Material science · FEM tools analysis

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1 Introduction

MEMS technology is popular because it offers low-power consumption and high linearity devices like switches, resonators, and filters [1]. RF MEMS is one of the vital branches of MEMS technology, which has great potential in high-frequency wireless communication applications. RF MEMS technology-based switches become prominent in wireless mobile communication transceivers; because of low-power consumption, the battery life will improve. In the comprehensive analysis with the solid-state technology RF switches, i.e., PIN diodes, the RF MEMS switches offer tremendous performance in terms of isolation and high operating frequency. One primary advantage with the solid-state RF switches is high switching speed, but these switches are failed to demonstrate good performance in terms of insertion and isolation at high frequency [2]. So, RF MEMS switches are the best alternative for high-frequency wireless communication applications. Compared with DC contact, capacitive RF MEMS switches are popular because of their good performance in high-frequency applications.

Despite the immense performance and ability, RF MEMS technology has potential research challenges like reducing actuation voltage and switching time. An electrostatically actuated RF MEMS switches, the membrane structure will decide the required actuation voltage and the switching speed [3]. Till now, all the RF MEMS switches are micromachined with the traditional structures like a serpentine, cantilever, folded, and clamped–clamped. Till now, few researchers are proposed RF MEMS switches with triangular structures that offer low actuation voltage, and because of the non-uniform sides, the insertion property of the switch is also improved. The capacitive RF MEMS switch isolation property completely depends on the dielectric thin film incorporated. Si_3N_4 ($\varepsilon_r = 7.5$), AlN ($\varepsilon_r = 9.8$), and HfO_2 ($\varepsilon_r = 25$) are the popular dielectric materials [4, 5].

2 Related Work and Problem Statement

In related state-of-art, the RF MEMS switches proposed can be classified into two categories: DC contact and capacitive. For high-frequency applications, shunt capacitive switches are preferable [6]. Traditional capacitive RF MEMS switches offers quality performance, but because of high operating voltage, it is almost not possible to interface with the IC technology which limiting the scope of RF MEMS switches [7]. However, by incorporating novel and sturdy microstructures, we can reduce the switch operating voltage. As on state-of-art, it is clear that the switching speed of RF MEMS switches is very low. It is very essential to improve the switching speed of the switch. Unlike the traditional structures in this paper, we have used the triangular structure and extended the structure by applying multiple iterations on the structure which helps to improve the performance. Slots to the membrane help to reduce the required actuation voltage [8].

3 Mathematical Analysis

The electrostatically actuated shunt capacitive RF MEMS switch performance majorly depends on the electrical (pull-in voltage, capacitance), mechanical (switching time, resonant frequency), and radio frequency (insertion and isolation) parameters. For the extended triangle membrane, the expression for the pull-in voltage and the spring constant (K) is [9],

$$V_{\text{pull_in}} = \sqrt{\frac{8K}{27\varepsilon_0 A g^3}} \tag{1}$$

$$K = \frac{\xi}{\delta_{\max}} = \frac{3EI}{l^2} \tag{2}$$

The capacitive switch insertion and the isolation properties completely depend on the switch capacitance. The RF MEMS switch upstate and down state capacitance can be expressed as,

$$C_{\text{up}} = \frac{\varepsilon_0 A}{g_1 + \frac{t_{\text{d}}}{\varepsilon_{\text{r}}}} \tag{3}$$

$$C_{\text{down}} = \frac{\varepsilon_0 \varepsilon_{\text{r}} A}{t_{\text{d}}} \tag{4}$$

The cross-sectional is between membrane and CPW strip line is 'A,' dielectric thickness '$t_{\text{d.}}$' The insertion losses (S_{21}) is when the membrane is in upstate when no actuation voltage is applied,

$$|S_{21}|^2 = \frac{1}{|S_{11}|^2}\left(\frac{C_{\text{up}}}{C_{\text{down}}}\right)^2 \tag{5}$$

The isolation losses (S_{21}) are when the membrane is in downstate when actuation voltage is applied, i.e.,

$$|S_{21}|^2 = \begin{cases} \frac{4}{\omega^2 C_{\text{down}}^2 Z_0^2} & \text{for } f \ll f_0 \\ \frac{4R_s^2}{Z_0^2} & \text{for } f \approx f_0 \\ \frac{4\omega^2 L^2}{Z_0^2} & \text{for } f \gg f_0 \end{cases} \tag{6}$$

4 Iterative Approach

Triangular structure-based electrostatically actuated shunt capacitive RF MEMS switch design, performance improving, and the packaging aspects are discussed. Unlike the traditional structures, we have designed the switch with the triangular structure and performed the iterative analysis on the triangular structure by adding the perforation and the slot. The analysis is done with a gold (Au) membrane of 1 μm thickness. Because of the slot to the membrane, the required operating voltage is reduced significantly as shown in Figs. 1 and 2. Because of the perforation, the required actuation voltage is slightly reduced, but the incorporation of the slot has reduced the actuation voltage significantly.

The gold (Au) membrane thickness analysis is precise in the design of MEMS devices. However, we also performed the membrane thickness analysis and noticed that the membrane with 0.5 μm thickness is offering a low actuation voltage of 2.4 V for 3 μm displacement as shown Fig. 3. For 0.3 μm thickness, the actuation voltage is 1.2 V, but the structure will come fatigue so we are preferred 0.5 μm thickness other than 0.3 μm. And for 1 μm thickness, the membrane is requiring approximately 6 V.

To make the analysis sturdy, we have extracted the precise performance analysis like Eigen frequency, switching time, and the resonant frequency analysis. The designed membrane three Eigen frequencies (0.96, 4.6, 5.9 kHz) are extracted shown in Fig. 4. The switching time is 96 μs shown in Fig. 5. The resonant frequency of the membrane is extracted by electrostatic actuation, and the extended triangle membrane resonant frequency is 57.5 kHz shown in Fig. 6.

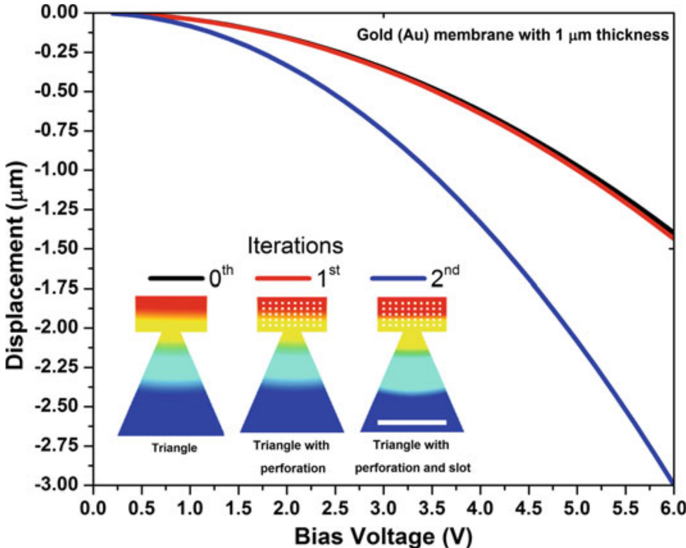

Fig. 1 Iteration in triangular micromechanical membrane

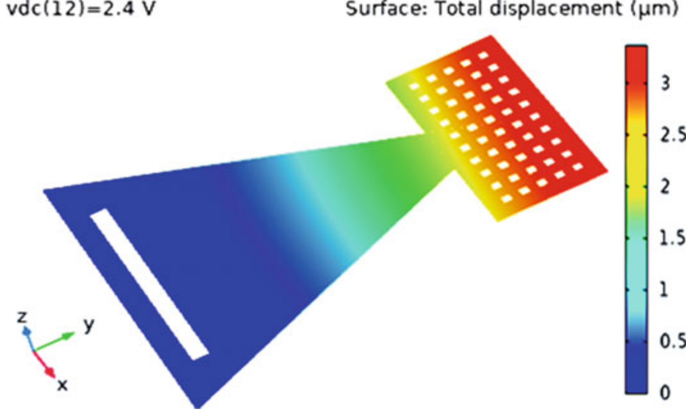

Fig. 2 Performance improved extended triangular structure

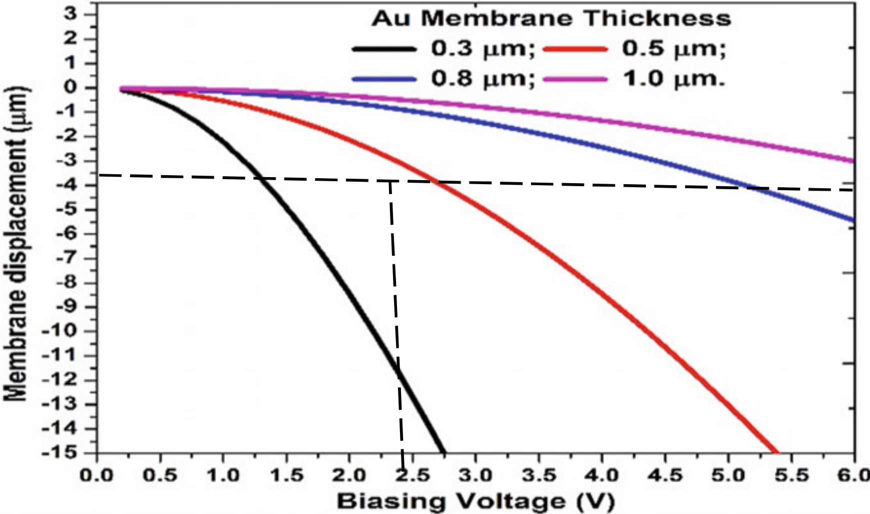

Fig. 3 Membrane thickness analysis

By incorporating the performance improved, extended triangular membrane, we have designed a shunt capacitive RF MEMS switch with two identical triangular membranes. The switch design flow is as shown in Fig. 7. The complete switch is designed on 1800 μm × 1800 μm size silicon substrate. A SiO_2 thin film is placed on the top of the substrate for better insulation. CPW RF transmission line is used with G-S-G of 100 μm-80 μm-100 μm. Some portion of the CPW GND lines is etched to place the bottom electrodes and the membranes. HfO_2 dielectric material with relative permittivity of 25 is used for better isolation. The final switch is designed by placing two identical extended triangular membrane, i.e., M_1 and M_2. Two separate

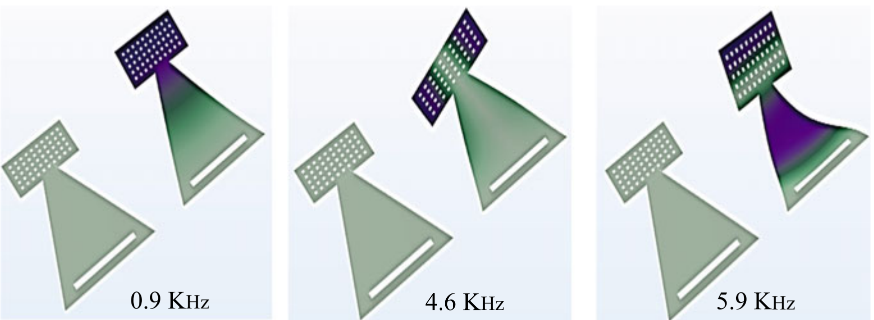

Fig. 4 Eigen frequencies analysis

bias voltage pads for VB_1 and VB_2 are placed. The overall switch has six pins, i.e., RF_{in}, RF_{out}, VB_1, VB_2, GND_1, and GND_2.

The designed switch dimensions are listed in Table 1. The switch RF performance is analyzed in three conditions, i.e., M_1- Actuated and M_2-Not Actuated, M_1- Not Actuated and M_2- Actuated, M_1- Actuated and M_2- Actuated. The electrical potential distribution and the triangular membranes (M_1, M_2) displacement under three conditions are clearly shown in Figs. 8 and 9. Because of the extended triangular structure, the switch is able to offer low insertion loss of −0.18 dB. The key advantage of placing two membranes is, it offers high isolation unlike the traditional switches. The isolation loss of the switch is −80 dB when M_1- Actuated and M_2- Actuated. The switch is offering good performance in the range of 1–20 GHz, so it is preferable in that frequency range. Overall we are able to improve the shunt capacitive RF MEMS switch performance deciding parameters like actuation voltage and radio frequency properties (Figs. 10 and 11; Table 2).

5 Conclusion

Unlike the traditional structures, in this work, we have designed RF MEMS switch with extended triangular structure, and because of incorporation slot, the required actuation voltage is reduced, i.e., 2.4 V. The resonant frequency is 57.5 kHz, and switching time is 96 μs. Because of the two identical membranes (M_1, M_2), the switch is offering high isolation of -80 dB. HfO_2 is used as a dielectric material. The air gap maintained is 3 μm. Because of the sufficient air gap and advantage with the structure, the switch is offering very low insertion of −0.18 dB. Overall switch has six pins, i.e., RF_{in}, RF_{out}, VB_1, VB_2, GND_1, and GND_2. The switch is preferable in the frequency range 1–20 GHz applications like Wi-Fi, Mi-MAX, GPS, and GSM.

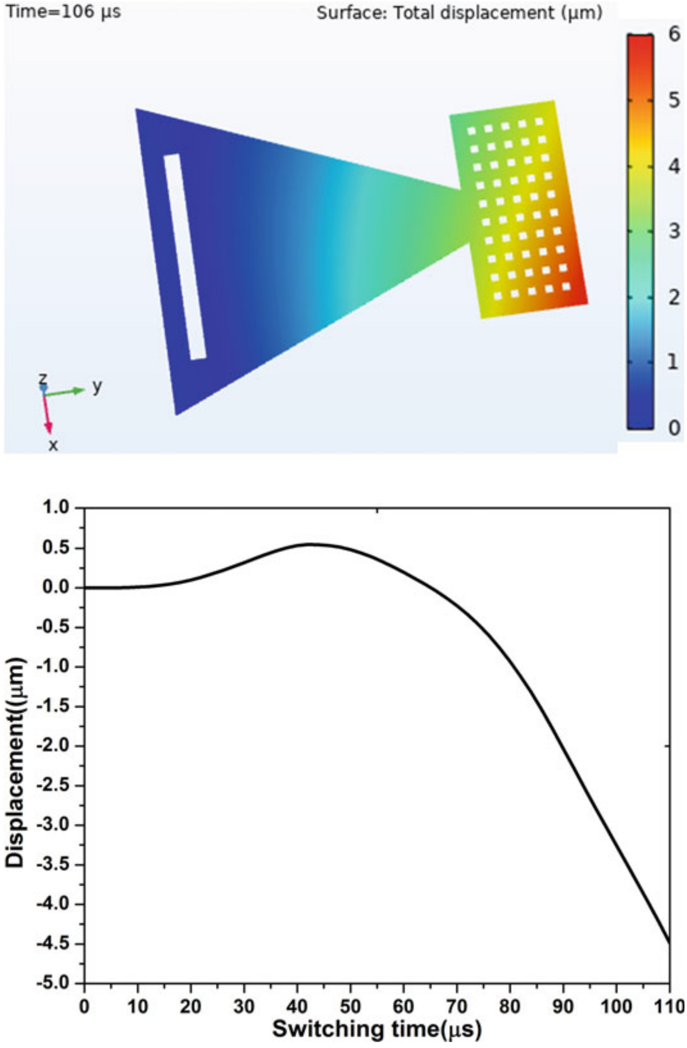

Fig. 5 Switching time (µs)

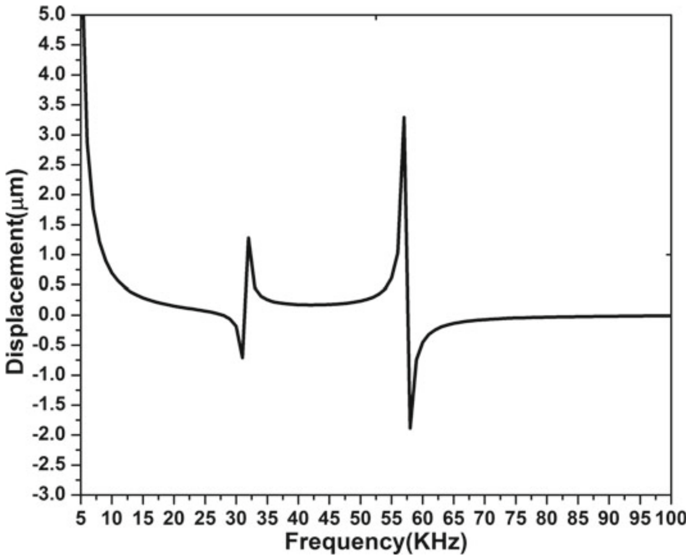

Fig. 6 Resonant frequency (KHz)

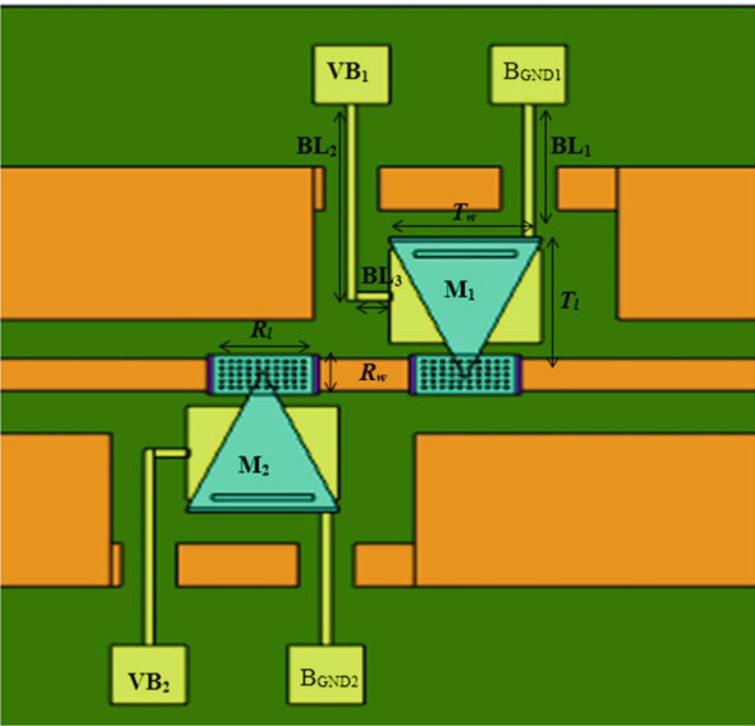

Fig. 7 RF MEMS switch with dual membranes

Table 1 Extended triangular membrane-based RF MEMS switch dimensions

Parameter	Description	Value(μm)	Parameter		Description	Value (μm)
S_l	Substrate dimensions	1800	BL (l, w)	1	Bias lines	20,350
S_w		1800		2		20,500
G-S-G	Gap-strip-gap	100–80-100		3		20,70
$K_1 = K_2 = K_3 = K_4$	Gaps for bias lines	100	$M_1 = M_2$	T_w	Extended triangle membrane	300
$E_1(l, w) = E_2(l, w)$	CPW etching slots	600,280		T_l		350
$\mathrm{BE}_1(l, w) = \mathrm{BE}_2(l, w)$	Bottom electrodes	300,240		R_w		200
$D_1(l, w) = D_2(l, w)$	Dielectrics	220,100		R_l		100
$\mathrm{V}B_1(l, w) = \mathrm{VB}_2(l, w)$	Biasing voltage	150,150	P_l		Packaging dimensions	1250
$\mathrm{BGND}_1\ (l, w) = \mathrm{BGND}_2\ (l, w)$	Biasing ground	150,150	P_w			1200
Membrane slot dimensions(l, w)		200,20	Membrane perforation (l, w)			7,7

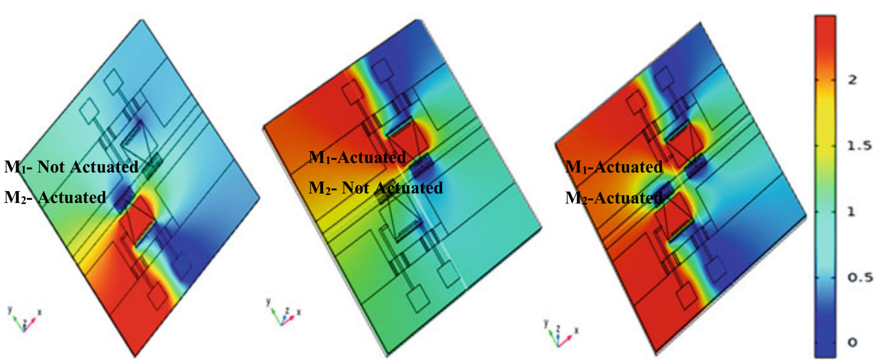

Fig. 8 Electric potential

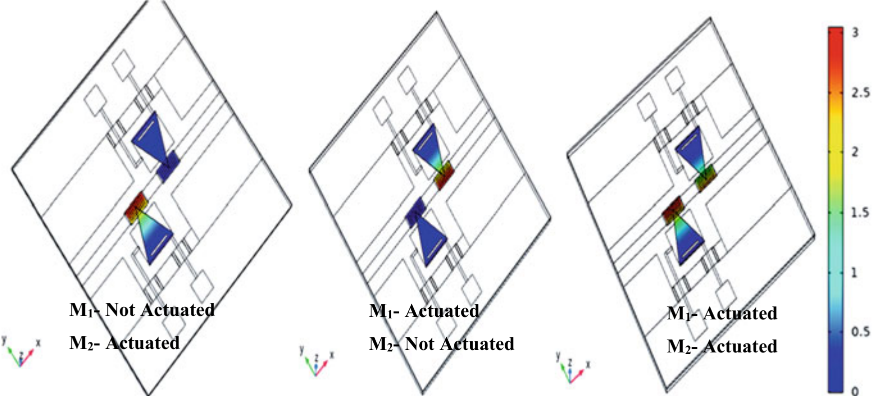

Fig. 9 Switch membranes displacement with electrostatic actuation

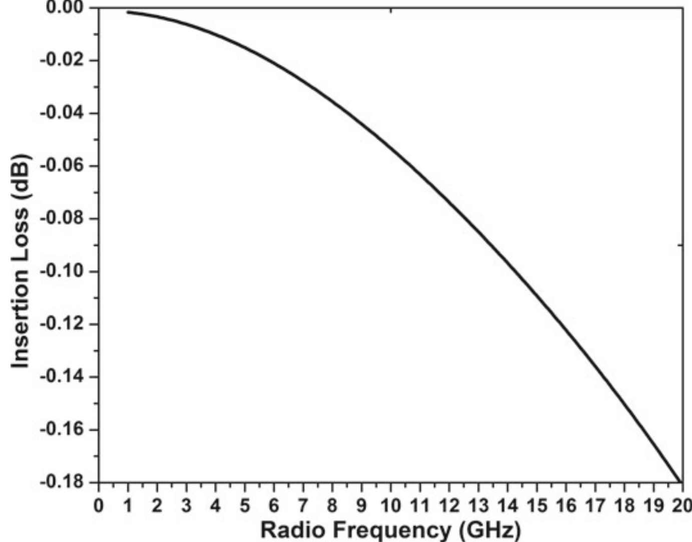

Fig. 10 Insertion loss

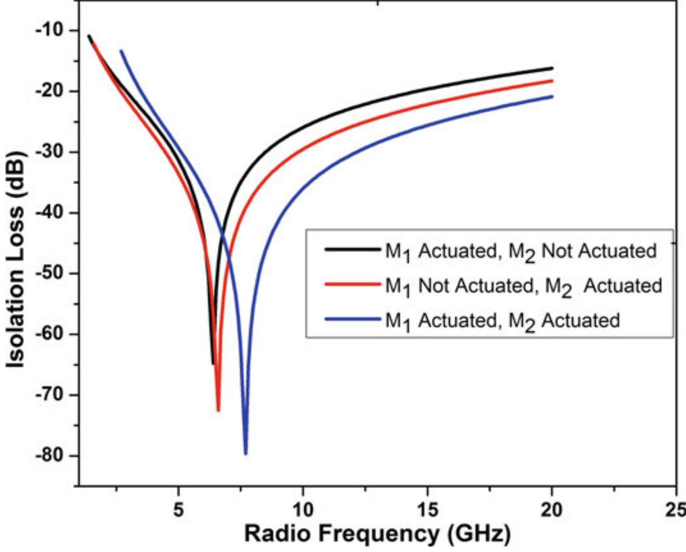

Fig. 11 Isolation loss

Table 2 Our work comparison with state-of-art

Parameter	[10]	[11]	Our work
Substrate	Glass	Silicon	Silicon
Insulator	–	SiO_2	SiO_2
Membrane	Gold(Au)	Gold(Au)	Gold(Au)
Air gap (μm)	3	2	3
Membrane thickness (μm)	1.5	2	0.5
Bias actuation voltage(V)	12.5	18.3	2.4
Switching time (μs)	–	–	96
Resonant frequency (KHz)	–	–	57.5
Insertion loss (dB)	–	−0.29	−0.18
Isolation loss (dB)	−43	−20.5	−80

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Investigating the Effect of Various Bragg's Reflector Configurations on the Performance of Flexible FBAR Sensors

Arun Kishor Johar, Gaurav Kumar Sharma, C. Periasamy, Koushik Guha, Ajay Agarwal, and Dharmendar Boolchandani

Abstract This work investigates the effect of Bragg's reflector configuration stages and its material on the performance of flexible FBAR sensor. Bragg's reflector configuration has been formed with various high and low acoustic Impedance layers such as Mo/SiO_2, W/SiO_2, and W/Al. The detailed investigation of flexible FBAR sensor has been done using 2-D finite element method (FEM) simulations performed on COMSOL Multiphysics software. Acoustic impedance versus frequency and frequency versus quality factor plots were drawn for the detailed investigation of material and number of Bragg's reflector configuration stages on the performance of the flexible FBAR sensor. The comparative results for various Bragg's reflector configurations have been summarized and reported. It is reported that spurious modes were present while using even number of stages to form Bragg's reflector configuration. Thus, to remove spurious harmonic modes odd number of Bragg's reflector configuration stages are required. The present work also states that W/SiO_2-based Bragg's reflector configurations are best suited to achieve enhanced performance in terms of enhanced coupling coefficient and figure of merit. This investigation offers new framework for the design of a flexible FBAR sensor with high performance.

Keywords Bragg's reflector configuration · Finite element method (FEM) · Quality factor · Coupling coefficient and figure of merit

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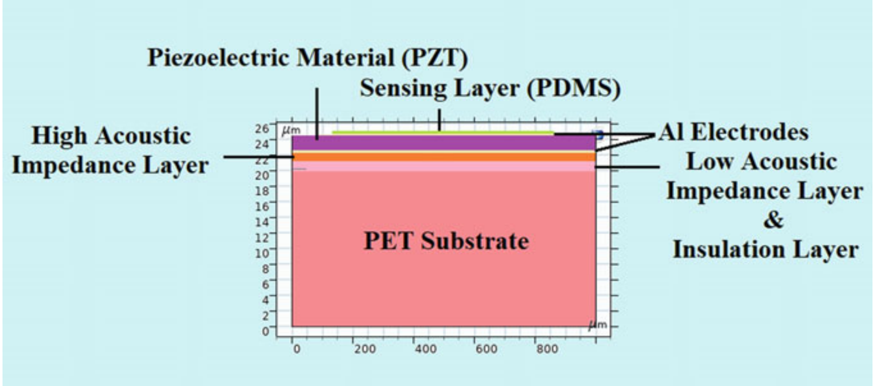

Fig. 1 2-D structure of flexible FBAR sensor

1 Introduction

Flexible electronics have become popular and have shown wide attention in various applications in the last few years. Flexible electronic-based devices such as diodes, transistors, and sensors have been reported earlier. As the film bulk acoustic resonator (FBAR) sensor having large quality factor (Q) and high resonant frequency; therefore, these devices show enriched sensitivity. Basically, FBAR sensor is formed by fixing a piezoelectric material layer (PZT) between two metal electrodes (Al). Various applications of FBAR sensors such as temperature, pressure, humidity, and gas sensing have been reported already. Integration of FBAR systems into flexible electronics results in numerous applications such as flexible lab-on-a-chips, smart healthcare, intelligent robots, Internet of things (IoTs), and wireless sensor networks. The polyethylene terephthalate (PET) substrates have been extensively employed in flexible electronics because of its good transparency and low cost. This work investigates the effect of Bragg's reflector configuration stages and its material on the performance of flexible FBAR sensor. Bragg's reflector configuration has been formed with various high and low acoustic impedance layers such as Mo/SiO_2, W/SiO_2, and W/Al. The performance of FBAR device has been investigated through FEM simulations and compared with the results obtained from silicon substrate using COMSOL Multiphysics software. Also, the effect of Bragg's reflector configuration on sensor performance has been analyzed through FEM simulations. Figure 1 shows the basic 2-D structure of a flexible FBAR sensor with single Bragg's reflector configuration.

2 Flexible FBAR Structure and Its Operation

In a flexible FBAR sensor, Bragg's reflector reflects the acoustic waves downwards inside the resonator. The high and low acoustic impedance materials layers such as

Table 1 Dimensions used for simulation

Parameter	Dimensions
PET substrate thickness	20 μm
Low acoustic impedance layer thickness	1 μm
High acoustic impedance layer thickness	1 μm
Electrode thickness	0.2 μm
Sensing layer (PDMS) thickness	0.5 μm
Piezoelectric layer (PZT) thickness	2 μm
Sensor's active area	750* 750 μm^2
Sensor's total area	1000*1000 μm^2

Mo/SiO_2, W/SiO_2, and W/Al are stacked one over another to form a Bragg's reflector [1–5]. Additional SiO_2 layer is deposited on the PET substrate to provide proper insulation. The piezoelectric material (PZT) has been selected due to their favorable piezoelectric properties for fabricating highly sensitive FBAR devices [6]. Al electrode has been chosen because of its low-cost and simple fabrication process [7]. The resonance is achieved through piezoelectric effect in flexible FBAR. Application of a direct current (DC) signal to flexible FBAR results in mechanical deformation. However, the application of an alternating current (AC) electric signal to flexible FBAR produces acoustic waves that are propagated in longitudinal direction to the electric field [8, 9]. The acoustic wave confinement inside the piezoelectric layer can be achieved by perfect matching of acoustic wave inside flexible FBAR. It can be accomplished by the unity magnitude of reflection coefficient [10]. The essential boundary conditions to perform the FEM simulations are: (1) Bottom electrode must be connected to ground, whereas top electrode should be connected to terminal voltage (+1 V); (2) sensor must be fixed from both sides by applying fixed constraints to it; and (3) perfectly matched layers must also be defined. The dimensions used for simulating the flexible FBAR sensor are listed in Table 1.

The fundamental resonance frequency of flexible FBAR is given by Eq. (1)

$$f = \frac{\vartheta}{2t_p} \quad (1)$$

where ϑ and t_p represent acoustic wave velocity and thickness of piezoelectric material layer, respectively [11]. The phase mismatch condition produces both mechanically induced and dielectric polarizations for acoustic wave inside the structure. Thus, parallel resonance takes place and a subsequent reduction in net current occurs. The electrical impedance (Z_{elec}) for flexible FBAR with external excitation can be determined by

$$Z_{elec} = \frac{1}{j\omega C_0}\left[1 - k_{eff}^2 \frac{\tan\left(\frac{\beta t_p}{2}\right)}{\left(\frac{\beta t_p}{2}\right)}\right] \quad (2)$$

where ω, k_{eff}^2, β and t_{p} denote the angular frequency, effective piezoelectric coupling coefficient, propagation constant, and piezoelectric layer thickness, respectively [12, 13].

3 BVD and MBVD Equivalent Models of Flexible FBAR

Figure 2a and b represent the basic Butterworth–Van Dyke (BVD) and modified BVD (MBVD) equivalent circuits of flexible FBAR sensor, respectively. BVD equivalent circuit is formed by connecting a dynamic inductor (L_{m}), a capacitor (C_{m}), and a resistor (R_{m}) in series and connecting this to a static capacitance (C_{o}) through parallel connection. The electrical losses of the electrodes (R_{s}) and dielectric loss (R_{o}) of piezoelectric material are also additionally connected to the basic BVD model for developing the MBVD equivalent [14–17].

These elements of the electrical equivalent circuit can be obtained using the following equations:

$$\text{Static capacitance } (C_0) = \frac{\varepsilon A}{t_{\text{p}}} \tag{3}$$

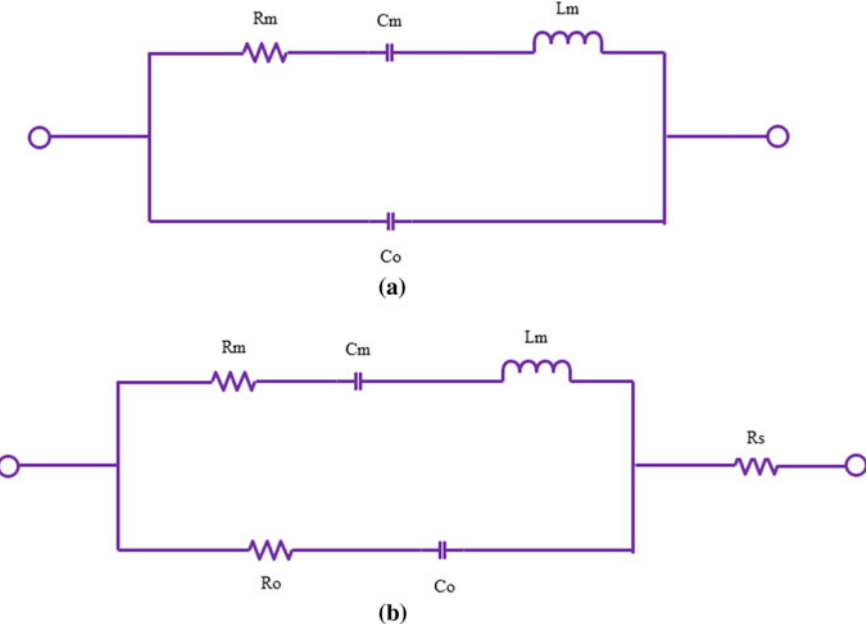

Fig. 2 **a** Basic Butterworth–Van Dyke (BVD) and, **b** modified BVD (MBVD) equivalent circuits of Flexible FBAR sensor

$$\text{Dynamic inductance}(L_m) = \frac{\pi^3 \vartheta_a}{8\varepsilon A\omega^3 k_{\text{eff}}^2} \tag{4}$$

$$\text{Dynamic capacitance } (C_{\text{m}}) = \frac{8}{\pi^2} k_{\text{eff}}^2 C_0 \tag{5}$$

$$\text{Dynamic resistance}(R_{\text{m}}) = \frac{\pi \eta \varepsilon}{8k_{\text{eff}}^2 \rho A\omega \vartheta_{\text{a}}} \tag{6}$$

$$\omega^2 = \frac{1}{L_{\text{m}} C_{\text{m}}} \tag{7}$$

where ε, ρ, η, ϑ_{a}, t_{p}, k_{eff}^2, A and ω denote the permittivity, density, acoustic viscosity, acoustic velocity, thickness, coupling coefficient of piezoelectric layer, area of the resonator, series resonant frequency, and piezoelectric layer coupling coefficient, respectively [18, 19]. Mathematically, coupling coefficient of piezoelectric layer can be obtained by

$$k_{\text{eff}}^2 = \frac{\pi^2}{4}\left(\frac{f_{\text{ar}} - f_{\text{r}}}{f_{\text{ar}}}\right) \tag{8}$$

where f_{r}, and f_{ar} denote the series and parallel resonance frequencies of flexible FBAR sensor, respectively [20, 21]. The piezoelectric material's acoustic velocity can be estimated by:

$$\vartheta_{\text{a}} = \sqrt{\frac{c_{33}^D}{\rho}} \tag{9}$$

where ρ and c_{33}^D denote piezoelectric layer density and elastic stiffness at constant electric displacement [22, 23]. The quality factor of flexible FBAR sensor can be obtained from the phase slope of the impedance at series/parallel resonant frequency and is given by

$$Q_{\text{s/p}} = \frac{f_{\text{r/ar}}}{2} \frac{d < Z_{\text{in}}}{\text{d}f}\bigg|_{f = f_{\text{r/ar}}} \tag{10}$$

where $f_{\text{r/ar}}$ denotes the series or parallel resonant frequency of FBAR and $< Z_{\text{in}}$ is the electrical impedance of the FBAR [24]. The product of coupling coefficient and quality factor is known as figure of merit of flexible FBAR devices.

4 Results and Discussions

Figure 3a–c shows the resonance characteristics of the flexible FBAR sensor for with Bragg's reflector configuration composed of materials such as Mo/SiO_2, W/SiO_2 and W/Al and different number of Bragg's reflector stage resonator.

The overall performance results of flexible FBAR sensor with different Bragg's reflector configurations are summarized in Table 2. From Table 2, it can be seen that, Bragg's reflector configuration composed of Tungsten (W) and SiO_2 as high and low acoustic impedance layers were found to be best suitable for flexible FBAR sensor.

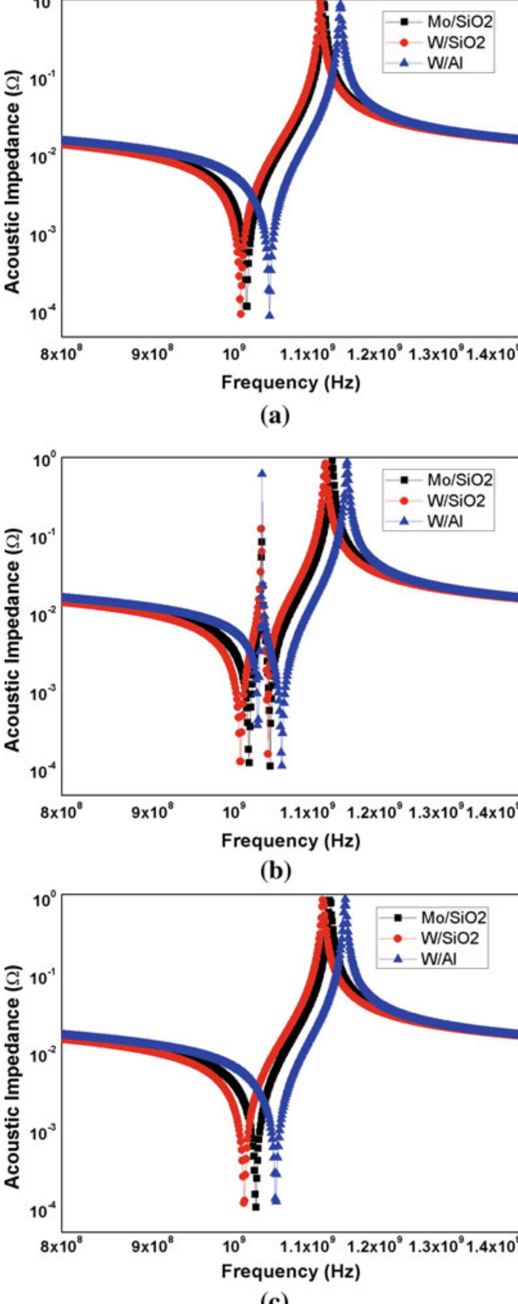

Fig. 3 Acoustic impedance versus frequency plot for **a** flexible FBAR sensor with 1-stage Bragg's reflector, **b** flexible FBAR sensor with 2-stage Bragg's reflector, and **c** flexible FBAR sensor with 3-stage Bragg's reflector

Table 2 Performance summary of the proposed flexible FBAR sensor

No. of Bragg's reflector stages	Coupling coefficient			Quality factor			Figure of merit		
	Mo/ SiO_2	W/ SiO_2	W/ Al	Mo/ SiO_2	W/ SiO_2	W/ Al	Mo/ SiO_2	W/ SiO_2	W/ Al
1	0.232662	**0.240317**	0.217251	992.92	973.99	993.16	231.0147	**234.0661**	215.7652
2	0.190943	**0.258311**	0.200087	511.96	1129.5	1180.11	97.75516	**291.7623**	236.1245
3	0.22428	**0.23946**	0.211277	1020.6	955.94	1015.7	228.8999	**228.9094**	214.5942

5 Conclusions

This work investigates the effect of Bragg's reflector configuration stages and its material on the performance of flexible FBAR sensor. Bragg's reflector configuration has been formed with various high and low acoustic impedance layers such as Mo/SiO_2, W/SiO_2, and W/Al. The detailed investigation of flexible FBAR sensor has been done using 2-D finite element method (FEM) simulations performed on COMSOL Multiphysics software. Acoustic impedance versus frequency and frequency versus quality factor plots were drawn for the detailed investigation of material and number of Bragg's reflector configuration stages on the performance of the flexible FBAR sensor. The comparative results for various Bragg's reflector configurations have been summarized and reported. It is reported that spurious modes were present while using even number of stages to form Bragg's reflector configuration. Thus, to remove spurious harmonic modes odd number of Bragg's reflector configuration stages are required. The present work also states that W/SiO_2-based Bragg's reflector configurations are best suited to achieve enhanced performance in terms of enhanced coupling coefficient and figure of merit.

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Predictive Analysis of Step-Quantum Well Active Region for Quantum Cascade Detectors

Sumit Saha and Jitendra Kumar

Abstract A predictive analysis of step-quantum well (SQW) active region (AR) for quantum cascade detectors (QCDs) has been performed. Different active well designs using SQW are presented and investigated for QCD performance improvement. A coupled quantum well design is taken for the analysis where the active well is made of SQW. Electron energies and corresponding wavefunctions are calculated by solving the time-independent Schrödinger equation using finite difference method. Different non-radiative scattering rates are calculated, and further, the escape probability of photoexcited carriers from the active well is predicted. The effect of step-barrier width on the oscillator strength of optical transition in the SQW has been investigated. The effect of step-barrier width on the non-radiative transition rates in the active well as well as escape probability from the active well has been further investigated. It is observed that SQW ARs provide higher escape probability by reducing non-radiative scattering rates of photoexcited carriers back into the active well; therefore, improved responsivity performance can be achieved. The escape probability has been analyzed for different operating temperatures. It is also observed that by using SQW as the AR, a higher barrier thickness can be achieved without degrading the responsivity performance significantly. A higher barrier thickness gives higher thermal resistance, hence higher detectivity performance.

Keywords Step-quantum well (SQW) · Quantum cascade detector (QCD) · Non-radiative scattering rates

1 Introduction

Quantum cascade detectors (QCDs) [1–3] are photovoltaic type, unipolar photon detectors. They are based on the semiconductor quantum cascade structures (QCSs)

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which is the basic construction element of well-known laser counterpart of QCDs, i.e., quantum cascade lasers (QCLs). The carriers in the active region of the QCS get excited by the incident photons of specific wavelength, and then the photoexcited carriers are extracted through an extractor of multiple quantum wells (QWs), specially designed to provide cascaded transport through the energy steps in the QWs to the next period. The quantum cascade transport through these QCSs allows them to operate under zero bias voltage, hence photovoltaic operation. This photovoltaic operation gives zero dark current which drastically reduces the performance degradation of the QCDs at higher temperatures and solves the problem of capacitance saturation by the dark current in readout integrated circuits (ROICs). QCDs cover almost the whole infrared (IR) spectral region [4] and also the terahertz (THz) spectral region [5] for detection with a very good responsivity and detectivity performance due to intersubband (ISB) device operation. Recently, a broad spectral response starting from mid-infrared to the visible has been achieved in a *GaN/AlN* QCD [6]. The ISB carrier lifetime is extremely small (~1 ps) which allows very high-speed detection and high-frequency response.

Although the ISB operation of these QCDs is advantageous in terms of wavelength coverage and high-speed operation, it also imposes some disadvantages on the QCD performance. They suffer from low quantum efficiency as surface normal incidence of photons cannot be absorbed due to ISB optical transition selection rule, hence very low responsivity. The problem of non-absorption of surface normal incidence is mitigated through use of surface plasmons [7] and photonic crystal slab resonant cavity [8]. The performance of QCDs is further improved by using diagonal carrier transition in the active region of QCDs [9]. Using diagonal transition design, escape probability as high as 70% of the photoexcited carriers is achieved. Use of photonic metamaterials made of patch-antenna micro-cavities enhances room temperature responsivity of the QCDs up to 50 mA/W [10].

Performance of QCDs strongly depends on the choice of semiconductor material systems and also on the design of the active well and the extractor well. In this paper, major focus has been made on the design of active well in order to improve QCD performance. Step-quantum well (SQW) is used as the active well and extractor region is the multiple quantum well structure having energy steps equal to the longitudinal-optical (LO) phonon energy of the material. Photo-absorption will take place in the active well, and the photoexcited carriers will be extracted and transported to the next period using the energy steps in the extractor wells. Yuh and Wang [11] have shown that the SQWs when exposed to small electric fields give large Stark shift but at the same time maintain the oscillator strength. Due to their asymmetric design, SQWs are suitable for two-color lasing or detection application by allowing the forbidden optical transitions which were prohibited in symmetric quantum wells. Infrared (IR) [12, 13] and terahertz (THz) [14–16] optical transitions in SQWs are investigated using different material systems. SQWs show higher-order optical nonlinearities due to their asymmetric design and the same have been studied intensively in recent years [17–19].

In this paper, SQW is incorporated in the AR of the QCD and analysis has been carried out to predict its usefulness as the active quantum well in QCDs.

Eigenenergies and corresponding wavefunctions have been calculated by solving time-independent Schrödinger equation using finite difference method. Energies and wavefunctions are used to calculate non-radiative scattering rates using Fermi's golden rule. In Sect. 2, theoretical aspects considered for the analysis are highlighted, and in Sect. 3, results are discussed.

2 Theoretical Considerations

For a photodetector, general equation of photo-responsivity is given as follows

$$R = \frac{\lambda q}{hc} \eta q_{\mathrm{p}}, \tag{1}$$

where λ is the wavelength of photo-absorption, q is the charge of electron, h is Plank's constant, c is the speed of light, η is the absorption efficiency, and g_{p} is the photodetector gain, and it is given for a QCD as

$$g_{\mathrm{p}} = \frac{p_{\mathrm{e}}}{N_{\mathrm{QW}} p_{\mathrm{c}}}, \tag{2}$$

where N_{QW} is the number of cascade periods of the QCD, p_{c} is the capture probability of carriers into the active well which is approximated as unity [20–22], and p_{e} is the escape probability of the photoexcited carriers to the extractor well. The escape probability is approximately given as [23]

$$p_{\mathrm{e}} \approx \frac{\tau_{\mathrm{esc}}^{-1}}{\tau_{\mathrm{esc}}^{-1} + \tau_{\mathrm{rel}}^{-1}}, \tag{3}$$

where τ_{esc}^{-1} is the escape transition rate of photoexcited carriers from the excited state in the active well to the extractor well state due to non-radiative scattering processes, τ_{rel}^{-1} is the relaxation transition rate of photoexcited carriers back to the ground state in the active well due to non-radiative scattering processes. From the equation, it can be inferred that higher escape transition rate or lesser the relaxation transition rate gives higher escape probability, hence higher photodetector gain and higher responsivity. Higher escape transition rate can be achieved by using resonant tunneling transport design or scattering tunneling transport design of QCD [24]. Here we have considered the more convenient scattering tunneling transport design. In scattering tunneling transport design, the extractor well state is in phonon resonance with the active well-excited state so that the escape transition rate is maximum due to resonant longitudinal-optical (LO)-phonon scatterings of carriers. A scattering tunneling transport design is shown in Fig. 1, and the desired carrier transport path

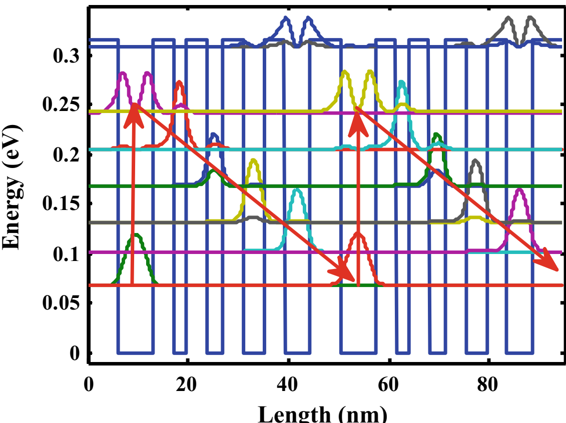


Fig. 1 Conduction band diagram with energies and corresponding wavefunctions for two consecutive periods of a QCD. The dimension of the wells and **barriers** are as follows (starting from the active quantum well): 7,**4**,2.6,**4**,3.3,**4**,4.2,**4**,5.2,**6**

is displayed by the arrows. *GaAs* material is used in quantum wells and $Al_{0.4}Ga_{0.6}As$ material is used in the barrier region. The active quantum well is supposed to be *n*-doped with a doping density of 5×10^{17} cm^{-3}.

The non-radiative scatterings of carriers are dominated by LO-phonon scatterings in polar semiconductor systems. The mean scattering rate is given as [25]

$$\frac{1}{\tau_{\text{if}}} = \frac{\int_{E_{\text{i}}}^{E_{\text{i}}+10k_BT} W_{\text{if}} f_{\text{i}}(E)\left\{1 - f_f\left(E \mp E_{\text{phn}}\right)\right\}\text{d}E}{\int_{E_{\text{i}}}^{E_{\text{i}}+10k_BT} f_{\text{i}}(E)\text{d}E}, \tag{4}$$

where E_{phn} is the LO-phonon energy (36.1 meV for *GaAs* at 300 K), f is the Fermi–Dirac function, and W_{if} is the total scattering rate. Negative sign denotes phonon emission process, and positive sign denotes phonon absorption process. The total LO-phonon scattering rate is given as [25, 26]

$$W_{\text{if}}^{\text{LO}} = W_{\text{if-emission}}^{\text{LO}} + W_{\text{if-absorption}}^{\text{LO}}, \tag{5}$$

where

$$W_{\text{if - absorption/if - emission}}^{\text{LO}} = \frac{Y''}{2}\Theta\left(k_{\text{i}}^2 - \frac{2m^*\Delta}{\hbar^2}\right) \times \int_{-\infty}^{\infty} \frac{\pi|G_{\text{if}}(k_z)|^2}{\sqrt{k_z^4 + 2k_z^2\left(2k_{\text{i}}^2 - \frac{2m^*\Delta}{\hbar^2}\right) + \left(\frac{2m^*\Delta}{\hbar^2}\right)^2}}\text{d}k_z, \tag{6}$$

where $Y'' = \left\{2m^*e^2\omega_{\text{phn}}/(2\pi\hbar)^2\varepsilon_0\right\} (1/\varepsilon_\infty - 1/\varepsilon_s)(N_0 + 1/2 \mp 1/2)$, $G_{\text{if}}(k_z) = \int \psi_f^*(z)e^{-ik_z z}\psi_{\text{i}}(z)\text{d}z$ and $\Delta_{\text{absorption/emission}} = \left(E_f - E_{\text{i}} \mp \hbar\omega_{\text{phn}}\right)$. All other terms carry their usual significance [25, 26].

The absorption efficiency is given as [23]

$$\eta = 1 - \exp\left(-N_{\mathrm{QW}}\alpha_{abs}^{\mathrm{if}}\right) \approx N_{\mathrm{QW}}\alpha_{abs}^{\mathrm{if}}, \quad (7)$$

where absorption coefficient is given as

$$\alpha_{abs}^{\mathrm{if}} = \frac{n_{\mathrm{if}}e^2\hbar}{2\varepsilon_0 c n_{\mathrm{ref}} m^*} f_{\mathrm{if}} \frac{\gamma}{\left(E_f - E_{\mathrm{i}} - \hbar\omega\right)^2 + \gamma^2}, \quad (8)$$

where n_{if} is the effective population density, 2γ is the full width at half maximum (FWHM), and f_{if} is the oscillator strength, and it is given as [27]

$$f_{\mathrm{if}} = \frac{2m^*\omega_{\mathrm{fi}}}{\hbar}\left|\langle\psi_{\mathrm{i}}|z|\psi_f\rangle\right|^2. \quad (9)$$

The temperature dependencies of FWHM can be found using the following relationship [28]

$$\frac{2\gamma_{\mathrm{if}}(T)}{2\gamma_{\mathrm{if}}(300)} = \frac{(1 + 2n_q(T))}{(1 + 2n_q(300))}, \quad (10)$$

where the phonon number is given as $n_q(T) = 1/[\exp(\hbar\omega_{\mathrm{phn}}/k_B T) - 1]$.

The position-dependent electron wavefunctions $\psi(z)$ and electron energies E are obtained by using the position-dependent potential profile $V(z)$ in the time-independent Schrödinger equation. The time-independent effective mass Schrödinger equation is given as [27]

$$-\frac{\hbar^2}{2}\frac{d}{\mathrm{d}z}\left(\frac{1}{m^*(z)}\frac{\mathrm{d}\psi(z)}{\mathrm{d}z}\right) + V(z)\psi(z) = E\psi(z), \quad (11)$$

where $\hbar$ is the reduced Plank's constant and $m^*(z)$ is the position-dependent electron effective mass.

3 Results and Discussion

Conduction band diagram, eigenenergies, and corresponding wavefunctions are calculated by solving time-independent effective mass Schrödinger equation by finite difference method. MATLAB codes are developed and used for this research analysis. Calculated energies and wavefunctions are further used to estimate LO-phonon scattering rates between states. The LO-phonon scattering rates are further used to calculate escape probability using Eq. (3).

Figure 2 shows the variation of escape probability with temperature for the QCD structure shown in Fig. 1. The figure is plotted for two different extractor-barrier widths (4 and 6 nm). It is observed that the escape probability decreases with increase in temperature due to increase in relaxation rate of photoexcited carriers back into the active well ground energy state from the active well excited state by LO-phonon scatterings. From the figure, it is also observed that the escape probability decreases due to increase in extractor-barrier width, which is mainly because of weak coupling between active well excited state and the extractor well ground state.

Therefore, smaller extractor-barrier width gives larger escape probability but at the same time it reduces the detectivity performance of QCDs because of decrease in thermal resistance of the QCD structure due to smaller barrier. Therefore, for a QCD design, one should choose the extractor-barrier width properly to increase responsivity as well as detectivity performance.

To increase the escape probability and also the thermal resistance of the structure, we have proposed to use the SQW as the active region in QCDs. Schematics of a single SQW and a coupled SQW are shown in Fig. 3. The 7 nm active well is of *GaAs* material, where the step barrier is of $Al_{0.2}Ga_{0.8}As$ material, and the extractor

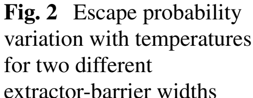
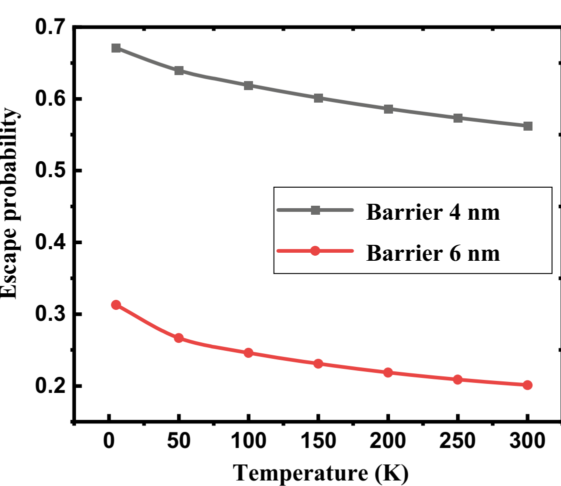


Fig. 2 Escape probability variation with temperatures for two different extractor-barrier widths



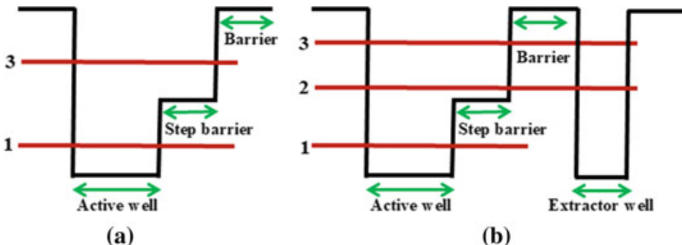


Fig. 3 Schematic of **a** a single SQW and **b** a coupled SQW

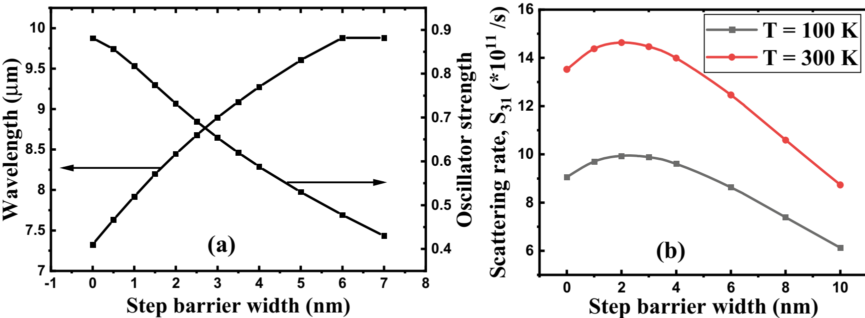


Fig. 4 **a** Variation of oscillator strength of optical transition and absorption wavelength with step-barrier widths for a single SQW, **b** LO-phonon scattering rate variation with step-barrier widths for a single SQW

barrier is of $Al_{0.4}Ga_{0.6}As$ material. The step-barrier and the extractor-barrier widths are varied to observe their effect on the escape probability.

From the schematics, it can be observed that due to use of SQW, the effective barrier width (combination of step-barrier width and extractor-barrier width) increases, which in return gives higher thermal resistance of the structure.

Figure 4a shows the variation of absorption wavelength and oscillator strength of optical transition with step-barrier width for a single SQW structure. It is observed that the absorption wavelength experiences a redshift due to increase in step-barrier width and oscillator strength decreases as the dipole moment decreases between the states due to increase in step-barrier width. We have also calculated the LO-phonon scattering rate variation with step-barrier width at two different temperatures which are shown in Fig. 4b.

Next, the effect of step-barrier width on the oscillator strength has been analyzed for the coupled-SQW structure which is shown in Fig. 5a. The figure is plotted for three extractor-barrier widths. The oscillator strength decreases with the increase in step-barrier width. From the figure, we can see that there is a large drop in oscillator strength at around 3 nm step-barrier width. This is because of the energy crossing between the active well excited state and the extractor well ground state which can be easily seen in Fig. 5b.

Figure 6 shows the variation of escape probability and LO-phonon scattering rate for the coupled-SQW structure for two different temperatures. It is observed that escape probability increases with increase in step-barrier width which is mainly because of decrease in relaxation rate in the active well by LO-phonon scattering as shown in Fig. 6. It can be seen that a very high escape probability can be predicted by increasing step-barrier width.

Based on the analysis and observation of coupled SQW presented here, two different coupled-SQW designs have been proposed for the use in QCD as shown in Fig. 7 and the escape probability at different temperatures is predicted as shown in Fig. 8. It can be seen that a very high escape probability of the order of **≈ 0.85** can be achieved with the help of SQW design. In the first design "**Design 1,**" the width

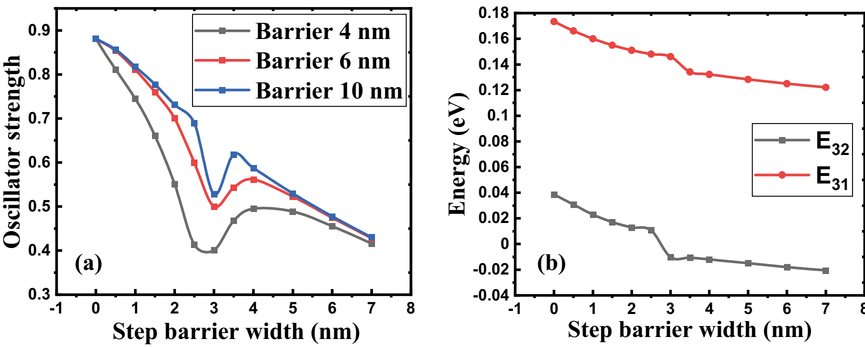


Fig. 5 **a** Variation of oscillator strength with step-barrier width for the coupled SQW with three different extractor-barrier widths, and **b** variation of energy difference between active well states and the active well excited state and the extractor well state with step-barrier widths for the coupled SQW with 4 nm extractor-barrier width

Fig. 6 Variation of escape probability and LO-phonon scattering rate with step-barrier width for the coupled SQW

Fig. 7 Coupled-SQW designs for QCDs. **a** Design 1. **b** Design 2

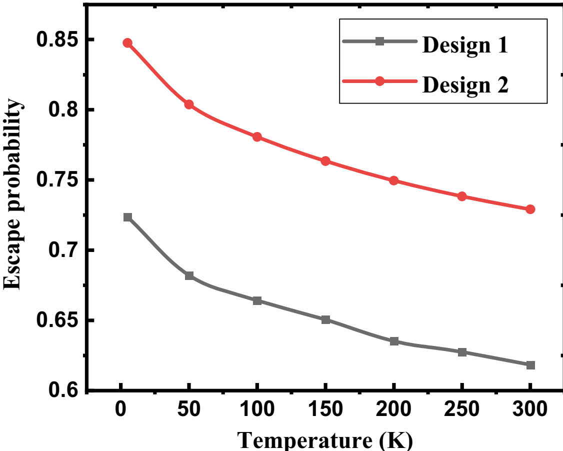


Fig. 8 Escape probability variation with temperatures for the coupled-SQW designs

of the *GaAs* active well is 7 nm, step-barrier width is 6 nm, extractor-barrier width is 1.5 nm, and the extractor well width is 3.6 nm. The rest of the extractor wells shall be designed following the standard procedure for making the phonon-ladder for efficient extraction through the extractor period. In the second design "**Design 2,**" the width of the *GaAs* active well is 6 nm, step-barrier width is 6 nm, extractor-barrier width is 1.5 nm, and the extractor well width is 2.9 nm.

Using coupled SQWs, a very high escape probability as high as $\approx 85\%$ of the photoexcited carriers can be achieved. Therefore, the coupled-SQW designs along with the extractor well period can provide a very high responsivity and detectivity performance of the QCDs.

4 Conclusion

In this paper, SQWs are analyzed for the use in the active region of QCDs and their usefulness is highlighted. A thorough investigation of the effect of step-barrier widths on the escape probability has been carried out. It is observed that with the increase in step-barrier width, oscillator strength of optical transition decreases and the absorption wavelength shifts toward the longer wavelengths. Most importantly, the escape probability of the photoexcited carriers from the active well to the extractor well increases with the increase in step-barrier width. It is a well-known fact that for a photodetector more the photoexcited carriers extracted, larger the responsivity performance is. It is also observed that due to use of step barriers, the effective extractor-barrier width is increased which gives larger thermal resistance to the structure; hence, higher detectivity performance as the detectivity of QCDs is limited by the Johnson noise. Therefore, by using SQW in the active region of the QCDs with proper choice of step-barrier width, high responsivity, and detectivity performance

can be predicted. In this research work, only the active well design for the QCDs using SQW has been presented. Further, a thorough investigation needs to be performed considering a complete QCD structure in order to predict the detector performance more accurately.

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Design of High Speed and Power Efficient 16 × 8 SRAM Memory Using Improved 4 × 16 Decoder

Ankit Kulshrestha, Sajal Samaiya, Onkar Nath Jha, and Gaurav Saini

Abstract At present, more than half the chip area is occupied by memory. So, it becomes imperative to find an efficient design of memory and deal with issues of power, delay, and reliability. A significant amount of memory delay is caused by its decoder. The optimized decoder used in this paper is faster than the conventional decoder by approximately 80% and consumes 92% lesser power. In this paper, four types of decoders are discussed with their performance comparison. A pre-charge pulse generator is also used in the design to pull up the bit-lines before performing the read operation. This paper aims to provide the optimal design of static random-access memory (SRAM) and an efficient address decoder. In the quest for efficient design, the focus remains on reducing total transistor counts and their optimum sizing.

Keywords SRAM · Pre-decoders · Logical effort · CMOS · Sizing

1 Introduction

Memory plays an imperative role in data manipulation and storage. The performance of memory is determined by three important factors—speed, power, and reliability. As speed and power are interdependent parameters, it often becomes difficult to optimize both simultaneously. Hence, optimization of one parameter is often sacrificed for the other. In this paper, static random-access memory (SRAM) is being used as a basic building block for our memory. Among various memories, SRAM is faster and consumes less power. Minimum 6-transistors are used to build an SRAM cell. A significant amount of delay and power consumption in memory is contributed by an address decoder [1]. This paper is concerned with the comparative study of various decoders in a quest for a better decoder design having a smaller number of transistors compared to a conventional decoder. First, the technique of pre-decoding has

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been used here and then combined the common transistors to reduce its logical effort [2]. This practice reduces access time and increases the frequency of the decoder. Another major factor that influences the performance of memory is its reliability. The reliability of an SRAM cell is measured by its static noise margin (SNM) [3].

2 Memory

2.1 SRAM Cell

A typical 6-T SRAM cell consisting of two cross-coupled inverters and two access transistors is shown in Fig. 1. 'BL' and 'BL_bar' are used as bit-lines to provide the data for reading and write operations in a memory cell, and 'WL' is the word line which decides which cell is read or written into [4].

Sense Amplifier. Sense amplifier is used to make memory operations faster and power efficient. A sense amplifier speeds up the operations by amplifying the difference between 'BL' and 'BL_bar.' Since bit-lines are not required to fully charge or discharge, it is quite evident that sense amplifier would bring down our power needs [5]. This operation can be achieved with the circuit as shown in Fig. 2.

Decoders. Address decoder contributes a notable amount of access time and consumes significant power and area in SRAM. Based on the design, a decoder can be implemented in two ways—static and dynamic. A dynamic decoder has a very complex design due to many transistors [1]. Therefore, the focus is given on the static decoder design. In this paper, decoders are designed in two steps- first selecting the right design architecture and then properly size the transistors to make it more efficient.

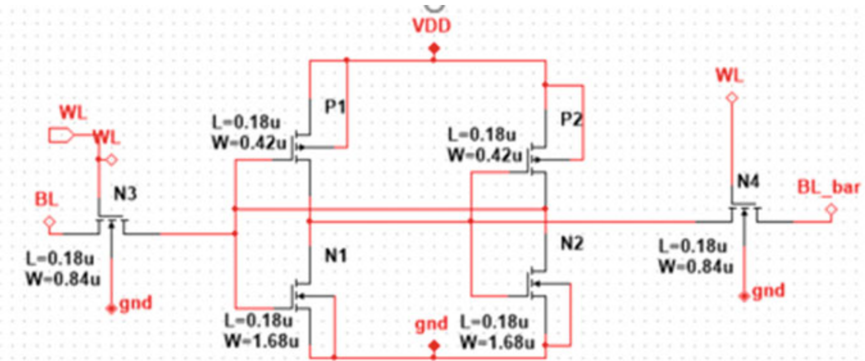

Fig. 1 SRAM cell

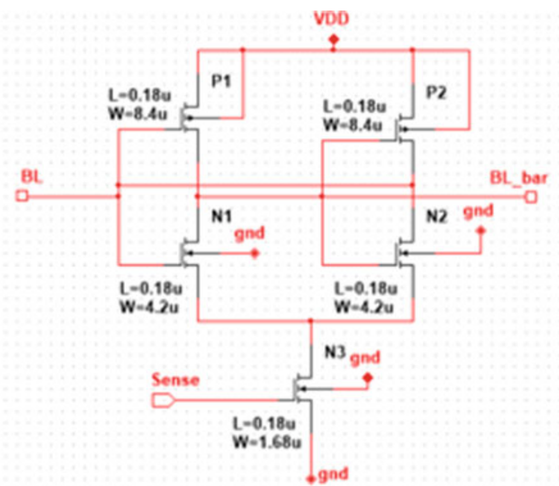

Fig. 2 Sense amplifier

Conventional Decoder. In Fig. 3, a schematic of 4 × 16 conventional type decoder is implemented in Cadence Virtuoso 180 nm SCL technology. Here sixteen 4-input NAND gates, followed by sixteen NOT gates, are used. This circuit provides 16 different addresses for four different inputs. For the optimized operation of the decoder, an optimum number of stages is determined depending upon total load, logical effort (LE), and its branching effort (LE for 4-input NAND gate is 2, and that for the inverter is 1). The number of stages obtained is four, and therefore, two additional inverters must be used. This ensures optimum delay for the present circuit. 4-input NAND gates have a large internal load and high LE. Due to this reason, the delay could be further decreased by using 2-input NAND gates.

Decoder using Pre-decoding. Here 2-input NAND gate is being used instead of a 4-input NAND gate along with 2-input NOR gates. This circuit has a comparatively better logical effort (LE for 2-input NAND gate is 4/3). A combination of 4-input

Fig. 3 Conventional decoder

NAND gate and NOT gate is replaced by 2-input NAND and 2-input NOR gate [6]. This new circuit has fewer transistor counts. Hence, this circuit consumes less area, power, and delay. The 4 × 16 decoder shown in Fig. 4 is made using two 2 × 4 decoders. In this circuit, NOR gates are used which consist of PMOS transistors in series. As PMOS is comparatively slower, this increases the delay.

Proposed Decoder with pre-decoding. In this circuit, two PMOS, having the same input, are replaced by a single PMOS in the NOR circuit as shown in Fig. 5. This results in a reduction of area, power, and delay.

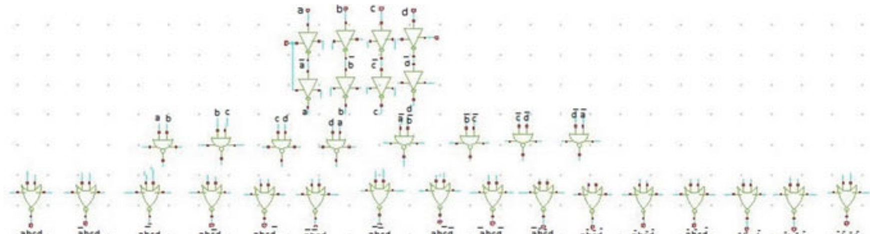

Fig. 4 Pre-decoders

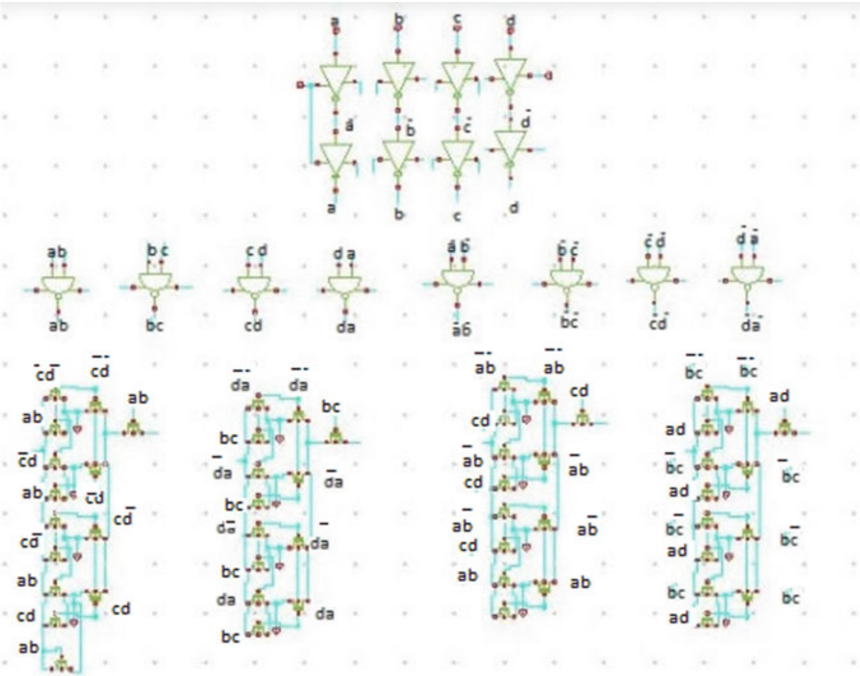

Fig. 5 Proposed decoder with pre-decoding

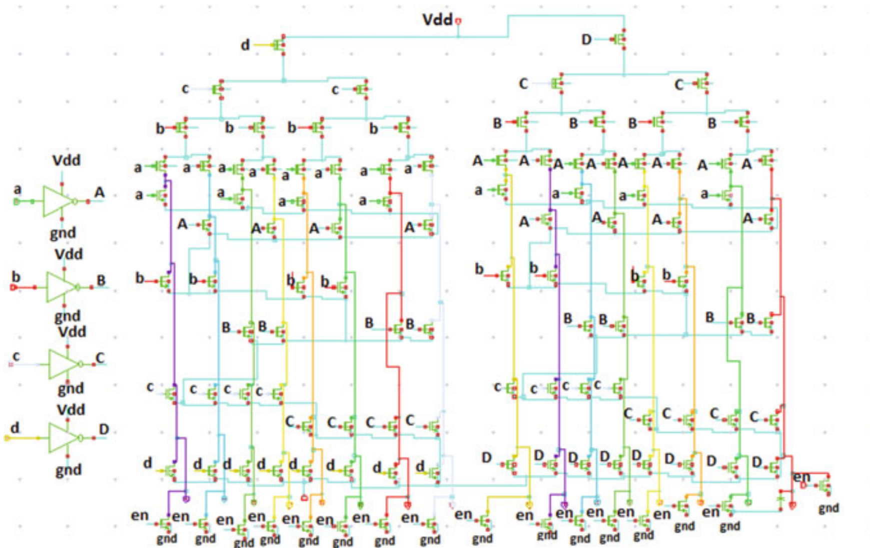

Fig. 6 Optimized decoder

Optimized Decoder. Further improvisation has been done on the Lyon decoder [7] by sizing its transistors. The critical path is optimized by reducing the path effort. Path effort depends on the output load, logical effort, and branching. Sharing PMOS of gates having common inputs results in better speed and power performance. Since only one output of a decoder is high at a time, PMOS transistors can be shared across all the decoder gates, Fig. 6.

Pre-charge pulse generator. The pre-charge pulse is required to be generated as soon as the read signal is active so that 'BL' and 'BL_bar' can be charged to Vdd for further operations. If '1' is stored in SRAM cell, 'BL' remains charged and 'BL_bar' discharges. If '0' is stored, 'BL_bar' remains charged and 'BL' discharges. It is to be noted that NMOS of inverter should be stronger than access transistors to discharge the bit-lines in case of '0.' Figure 7 shows the pre-charge pulse generator which has been proposed in this design.

16 × 8 Memory with Decoder. Interfacing of the decoder with memory is shown below in Fig. 8. For a read operation, first, the read signal (active low) is activated then enable signal helps to get an address on which read operation needs to be performed. This signal makes the desired word line high, and the corresponding cell is selected. The pre-charge pulse is activated (active low) for some interval such that both bit-lines, that is, 'BL' and 'BL_bar' are charged to Vdd as shown in Fig. 13. A decoder having delay, such that word line becomes high as soon as bit-lines are charged, is used. When the word line goes high, the value stored in a cell affects the bit-lines accordingly.

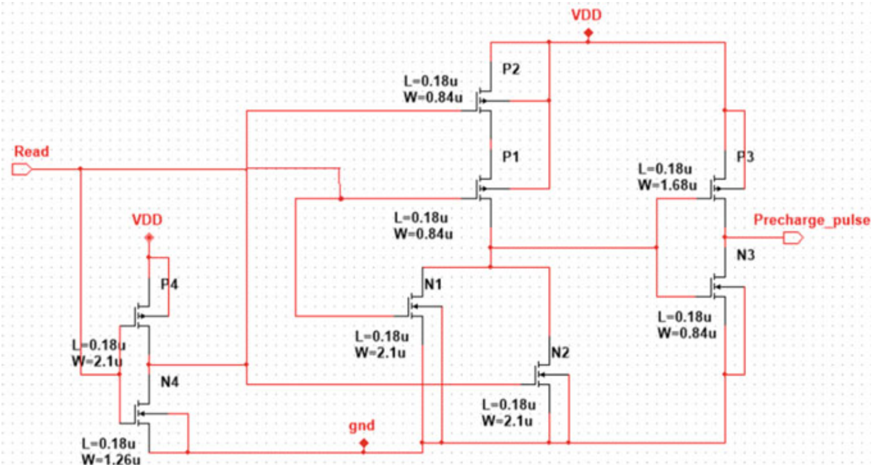

Fig. 7 Pre-charge pulse

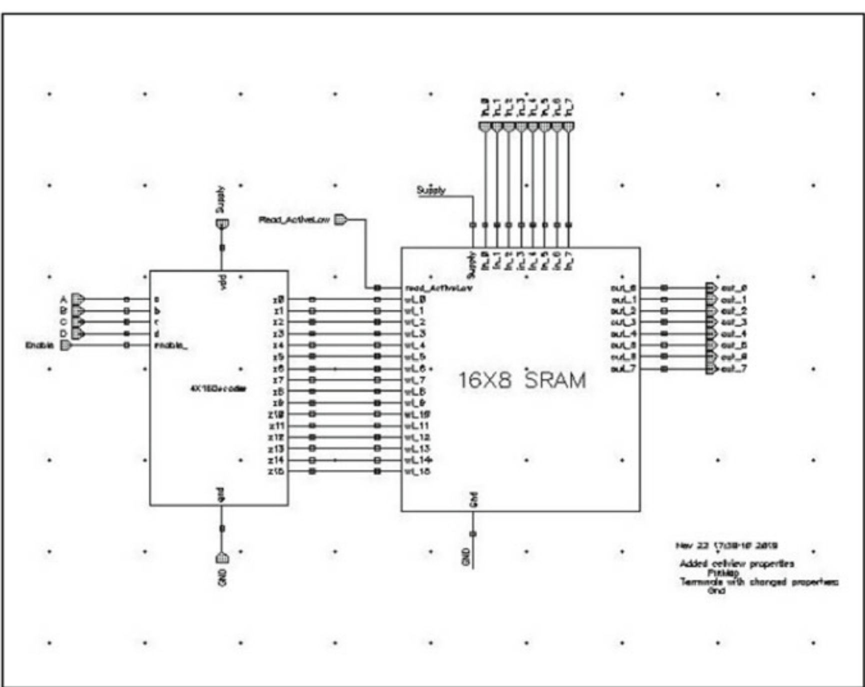

Fig. 8 16 × 8 Memory

For example, if the stored value is ‘0,’ then ‘BL_bar’ remains charged and ‘BL’ starts discharging. A sense signal (a delayed version of the read signal) is applied which amplifies the difference between ‘BL’ and ‘BL_bar,’ and consequently, stored value is availableon ‘BL.’

3 Simulation and Results

It can be observed from the waveforms shown in Figs. 9, 10, 11, and 12 that delay has been reduced significantly while going from conventional to an optimized decoder.

These observations have been summarized in Table 1.

Table 1 also suggests significant improvement in power consumption in subsequent decoder designs.

Power and delay performance come at the cost of reliability of the design, and it can be observed that delay comes down to 479 ps and power consumption also reduces. But if the decoder input signal comes after 74 ps of enable signal from the driving system, it fails as it can be observed in Fig. 13.

All four types of decoders are compared on account of their performance in terms of power and time delay, and their respective results are given as shown in table.

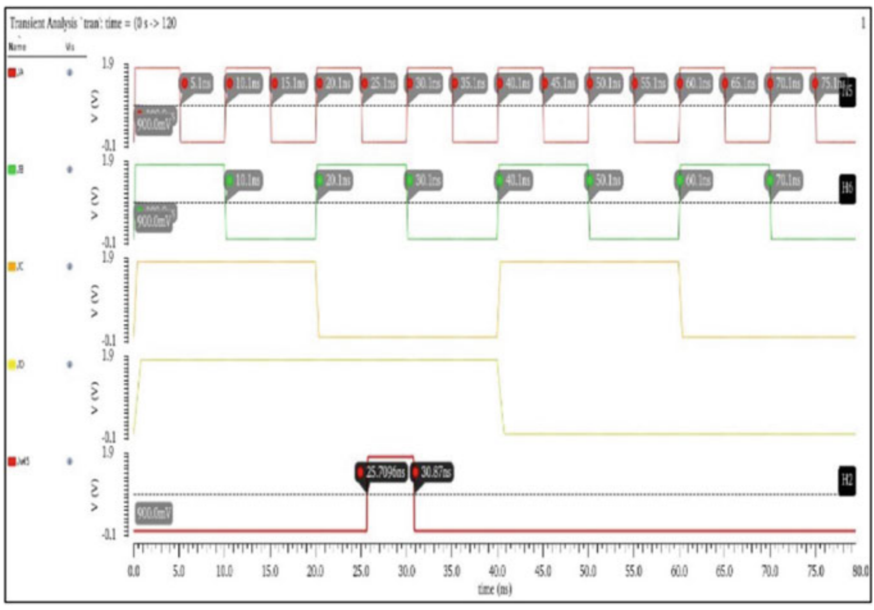

Fig. 9 Input and output waveforms of conventional decoder

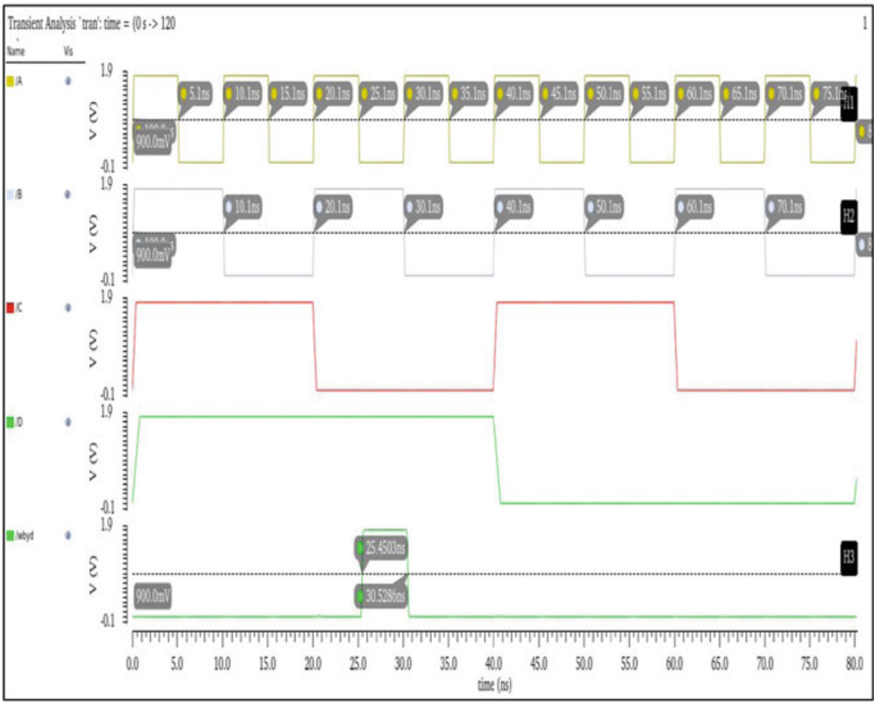

Fig. 10 Input and output waveforms of decoder with pre-decoding

4 Conclusion

16 × 8 SRAM memory along with 4 × 16 decoder is implemented using Cadence Virtuoso. Different designs of decoders are compared in terms of their power consumption and delay. An optimized decoder consumes 18.33 μW power and has the worst-case delay of 135 ps. Consequently, the delay has been reduced by approximately 5 times and power by 13 times as compared to the conventional decoder. The optimized design of 16 × 8 SRAM memory interfaced with 4 × 16 address decoder performs read operation with a worst-case time delay of 0.479 ns. These performance parameters are achieved by compromising the reliability of the design. In the future, the focus can be on improving noise margin and hence the reliability.

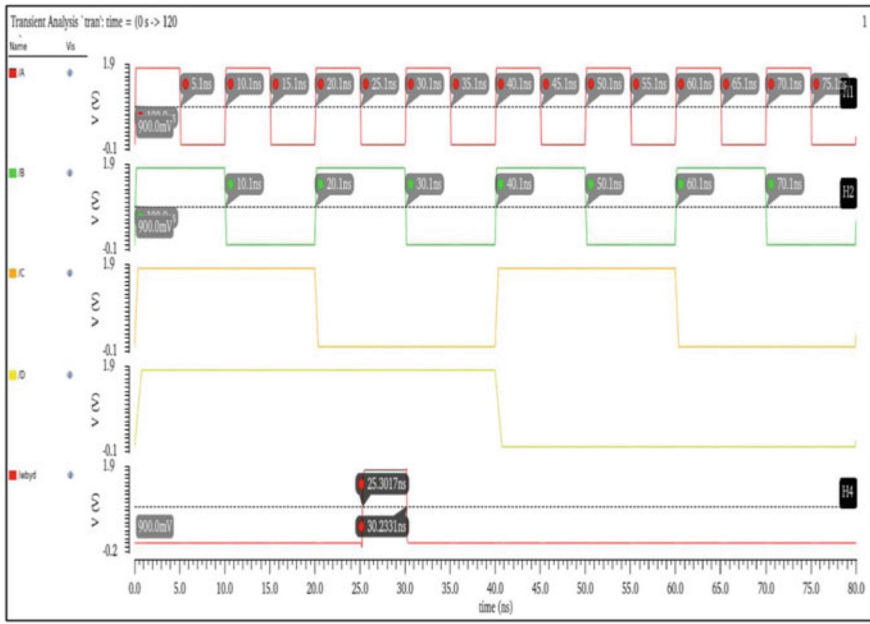

Fig. 11 Input and output waveforms of decoder with modified NOR gates

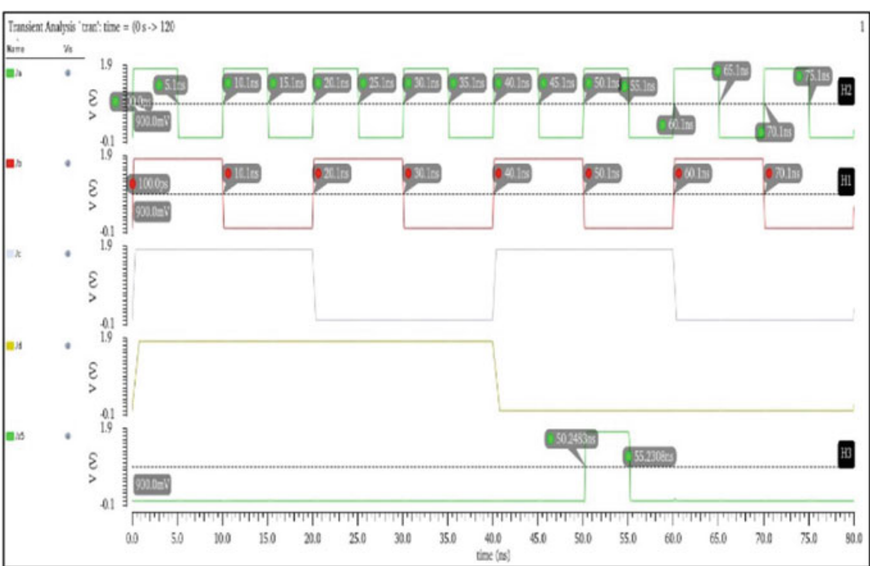

Fig. 12 Input and output waveforms of optimized decoder

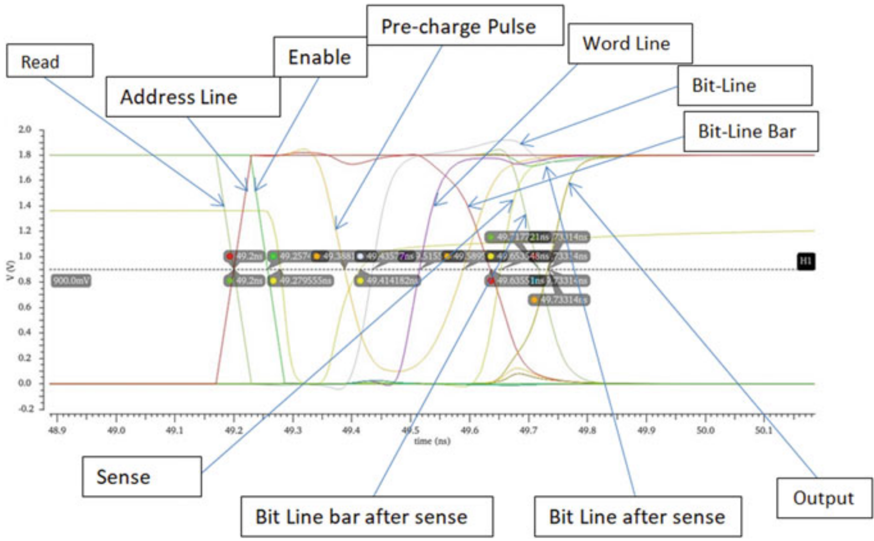

Fig. 13 Timing waveforms for read and write operation

Table 1 Power and delay comparison

Parameter	Conventional decoder	Decoder with pre-decoding	Proposed decoder using NOR gates	Optimized decoder
Power(μW)	230.7	114.6	21.9	18.33
Delay(pS)	685	385	165	135

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A Divide-By-5 Pre-scaler Design Approach for 5G Applications

Subhanil Maity, Lokenath Kundu, and Sanjay Kumar Jana

Abstract The pre-scalers are extensively used in high-speed multi-GHz applications to scale down the high frequencies before it reaches to the frequency divider block of a frequency synthesizer. In this paper, a new approach to design the metal–oxide–semiconductor CML (MCML) pre-scaler compliant with the 5G communication standard is presented. A hand calculation-based general analysis is shown in this work. A couple of delay cells have been introduced in the proposed architecture, and the theoretical foundations of the design approach have been established analytically. An MCML divide-by-5 pre-scaler is designed following the proposed design approach.

Keywords MOS Current Mode Logic (MCML) · Divide-by-5 · Pre-scaler · 5G

1 Introduction

The fifth-generation (5G) system is being developed to connect everyone, and everything, everywhere. The specifications developed for the first version of the 5G system by the 3rd generation partnership project (3GPP), the de facto standardization body for mobile communication systems, are presently being introduced commercially across the globe both at sub-6 GHz and at mm-Wave frequencies [1]. The stringent specifications of the 5G system have a large impact on the design of radio frequency (RF) phase-locked-loops (PLLs), with challenging design aspects [2]. Again, the PLL became a crucial building block due to the rapid development of coherent wireless

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communication systems. The high-speed divider is a power-hungry block within PLL synthesizers that transform a high-frequency input signal from a voltage-controlled oscillator (VCO) into a relatively low-frequency signal for the following stages [3]. In particular, the pre-scaler that is often the first stage inside dividers, operates at the highest frequency, and determines the operating frequency, and saves considerable power [4].

Pre-scalers or static frequency dividers also can be used along with PLLs for the generation of local oscillatory (LO) signals. One such single PLL-based LO generator for 5G has been proposed in [5] that can support multiple frequency bands concurrently. In [6], a current mode logic (CML) based divide-by-5 pre-scaler is proposed that can work up to an operating frequency of 12.12 GHz in the worst-case process corner that is realized in 180 nm technology node. A combination of five CML latches and two CML XOR gates is used to design the said pre-scaler.

In this work, a new approach is presented for the design of a divide-by-5 pre-scaler that is compliant with the 5G communication standard. Two CML latches, one CML XOR gate, and a couple of delay cells are utilized in this architecture. The hand calculations to design the delay cells are shown that establish the theoretical foundation of the proposed design approach.

Section 2 of this paper explains both the conventional and proposed architecture of the divide-by-5 pre-scaler. The calculations for the design of the delay cells are presented in Sect. 3, followed by conclusions in the last section.

2 Divide-By-5 Pre-scaler Architecture

2.1 Conventional Architecture

The majority of the conventional stand-alone divide-by-5 frequency dividers or pre-scalers are designed using injection-locked frequency divider (ILFD) [7] or complementary metal-oxide-semiconductor (CMOS) topology. ILFD occupies a large chip area as it uses an inductor which naturally requires a large silicon area, although ILFD can give a higher frequency of operation and larger bandwidth. On the contrary, CMOS may occupy less chip area, but traditionally it cannot support a high frequency of operation which is an important feature of any pre-scaler.

An inductor-less divide-by-5 ILFD is proposed in [8], where the 4th and 6th harmonics of the output signal frequency are produced by the circuit nonlinearities. The injection frequency is mixed with these harmonics to generate the intermodulation components. These components are made equal to the output frequency of the divider in a locked condition, and hence, we get a stabilized divide-by-5 frequency. It has less silicon coverage, but the operating frequency is limited.

A CML-based divide-by-5 pre-scaler is presented in [6], where five CML latches and two CML XOR gates are used. It operates at 12.12 GHz frequency with an excellent power head performance, leaving high-hard count a challenge.

2.2 Proposed Architecture

In this design, two MCML latches (latch I, and latch II), one MCML XOR gate, and two delay cells (delay cell I, and delay cell II) are used. The transistor-level diagram of the MCML latch is shown in Fig. 1, and the same for the MCML XOR gate is shown in Fig. 2. A set of two CMOS inverters is used to form the delay cells (see Fig. 3). The proposed pre-scaler architecture is shown in Fig. 4.

Divide-by-5 pre-scaler output signal is expected to remain in a certain voltage level for consecutive 2.5 clock cycles, and then, a transition of state and again it is supposed to remain in the other voltage level for consecutive 2.5 clock cycles. The delay cells are playing a crucial role in this process. The conceptual timing diagram of the proposed circuit is shown in Fig. 5. The delay cell I and II are functioning complementary to each other. If we consider low to high transitions of Z, and R for delay cell I, and X, and Y for delay cell II then, we can see, delay cell I is contributing 1 clock cycle delay and delay cell II is contributing 1.5 clock cycle delay. The high to low transitions of $\bar{Z}$ and R for delay cell I, and X, and Y for delay cell II show that delay cell I is introducing 1.5 clock cycle delay, and delay cell II is introducing 1 clock cycle delay.

This complementary nature of delay cells I, and II are interesting. As a whole, for a full input clock cycle, the delay cells are introducing exactly 5 clock cycle delay together, that is, required to achieve a divide-by-5 output.

A couple of CMOS inverters are used to design the delay cells so that we get a delayed output without any phase shift in the signal. As the delay of an inverter is majorly decided by its aspect-ratios hence, the aspect ratios of the inverters are found out through a hand calculation that is shown in Sect. 3. Also, the delays are set in such a way so that the proposed pre-scaler can be used in the sub-6 GHz standard of 5G systems.

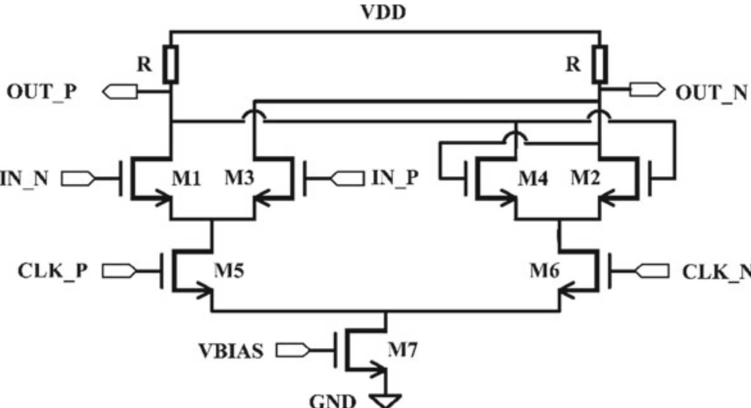

Fig. 1 Schematic of MOS current-mode-logic latch

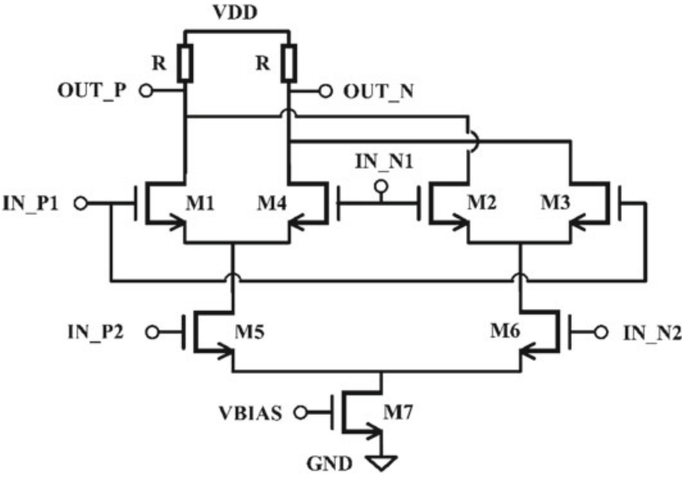

Fig. 2 Schematic of MOS current-mode-logic XOR gate

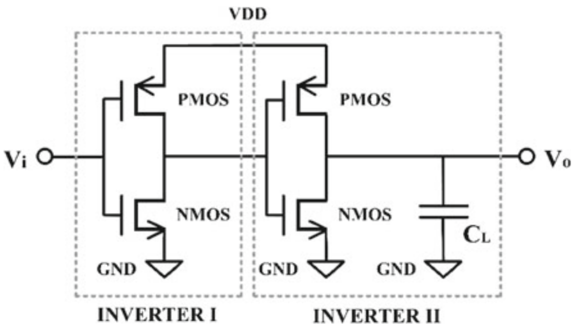

Fig. 3 Schematic of delay cell

Finally, a comparative analysis of the proposed divide-by-5 pre-scaler with the recently reported works is summarized in Table 1. Mainly, the architectural differences are highlighted. However, this may not produce a fair comparison because of several reasons, such as different CMOS technology nodes, power supply, different simulation environments, etc. But it gives an idea about the architecture of several divide-by-5 pre-scalers in terms of overall hard count. Here, it is observed that the proposed pre-scaler has a lesser hard count in terms of the number of components such as transistors, resistors, capacitors, inductors, etc. So, it is expected that the proposed pre-scaler will be covering less chip area.

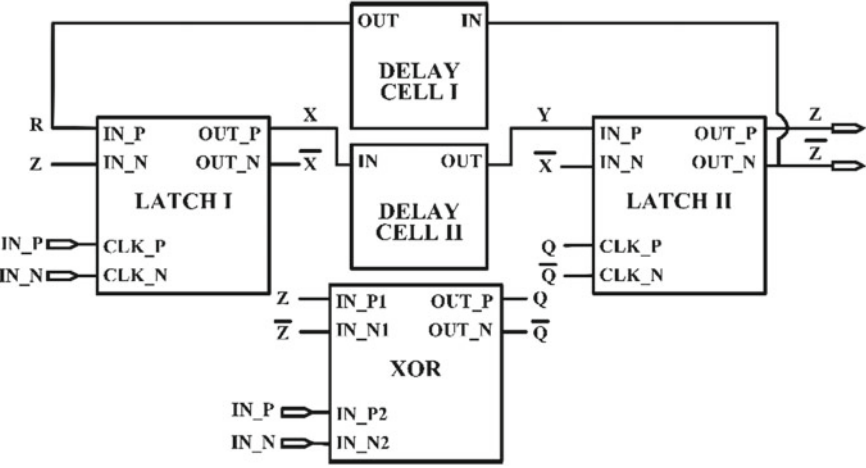

Fig. 4 Proposed divide-by-5 pre-scaler architecture. The circuit schematics of the latches, XOR gate, and delay cells are as in Figs. 1, 2, and 3, respectively

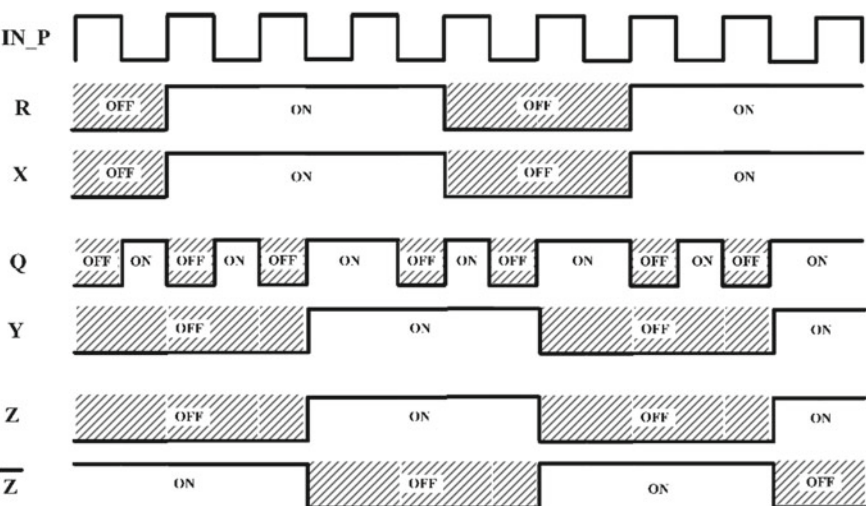

Fig. 5 Conceptual timing diagram of proposed pre-scaler. The square pulses are considered only for illustration purpose

3 Design of Delay Cells

Figure 3 shows the schematic of delay cells where a combination of two CMOS inverters is used. In this section, the aspect ratios of PMOS and NMOS transistors of a single inverter are derived for making the proposed pre-scaler compliant with sub 6 GHz 5G applications.

Table 1 Comparison of the proposed divide-by-5 pre-scaler with recent reported works

	IEEE ASPCON 2020 [6]	IEEE MTT-S 2013 [7]	IEEE TCAS-I 2020 [8]	Springer AICSP 2016 [9]	IEEE APMC 2009 [10]	This work
Division Ratio	5	5	5	5	5	5
Topology	CML	ILFD	ILFD	CML	Emitter coupled logic (ECL)	CML
Hard Count	Transistors 49 Resistors 14	Transistors 14 Resistors 8 Capacitors 13 Inductors 5	Transistors 24 Resistors 8 Capacitors 8 Injection Sources 8	Transistors 38 Resistors 4	Transistors 65 Resistors 20	Transistors 29 Resistors 6

3.1 Calculation of W_n/L_n of NMOS Transistor from the Current Equation

From Fig. 3, the NMOS transistor current equation in the linear region can be written as-

$$C_{\mathrm{L}}\frac{\mathrm{d}V_{\mathrm{o}}}{\mathrm{d}t}=-\frac{K_{\mathrm{n}}}{2}\frac{1}{\left(1+\frac{V_{\mathrm{o}}}{E_{\mathrm{n}}\ L_{\mathrm{n}}}\right)}\left[2\left(V_{\mathrm{i}}-V_{\mathrm{t,n}}\right)V_{\mathrm{o}}-V_{\mathrm{o}}^{2}\right] \tag{1}$$

where C_{L} stands for load capacitance at the output node, V_{o} stands for the output voltage, $E_{\mathrm{n}}L_{\mathrm{n}}$ stands for the short channel effect of the NMOS, L_{n} stands for the channel length of the NMOS, K_{n} stands for the transconductance parameter of NMOS, V_{i} stands for the input voltage, $V_{\mathrm{t,}}$ stands for the threshold voltage of NMOS. Now, taking integration in both sides and considering the output voltage swing from 0.2 to 1.8 v we get,

$$\int_{0}^{t_{\mathrm{d}}}\mathrm{d}t=-\frac{2C_{\mathrm{L}}}{K_{\mathrm{n}}}\int_{1.8}^{0.2}\frac{\left(1+\frac{V_{\mathrm{o}}}{E_{\mathrm{n}}\ L_{\mathrm{n}}}\right)\mathrm{d}V_{\mathrm{o}}}{\left[2\left(V_{i}-V_{\mathrm{t,n}}\right)V_{\mathrm{o}}-V_{\mathrm{o}}^{2}\right]}$$

$$t_{\mathrm{d}}=-\frac{2C_{\mathrm{L}}}{K_{\mathrm{n}}}\int_{1.8}^{0.2}\frac{\left(1+\frac{V_{\mathrm{o}}}{E_{\mathrm{n}}\ L_{\mathrm{n}}}\right)\mathrm{d}V_{\mathrm{o}}}{\left[aV_{\mathrm{o}}-V_{\mathrm{o}}^{2}\right]} \tag{2}$$

where t_{d} stands for delay time and $a=2\left(V_{\mathrm{i}}-V_{\mathrm{t,n}}\right)$

$$t_{\rm d} = -\frac{2C_{\rm L}}{K_{\rm n}} \int_{1.8}^{0.2} \left[\frac{1}{\left[aV_{\rm o} - V_{\rm o}^2\right]} + \frac{\frac{V_{\rm o}}{E_{\rm n}\ L_{\rm n}}}{\left[aV_{\rm o} - V_{\rm o}^2\right]} \right] {\rm d}V_o$$

$$t_{\rm d} = -\frac{2C_{\rm L}}{K_{\rm n}} \int_{1.8}^{0.2} \left[\frac{1}{[a - V_{\rm o}]V_{\rm o}} + \frac{\frac{1}{E_{\rm n}\ L_{\rm n}}}{[a - V_{\rm o}]} \right] {\rm d}V_{\rm o}$$

$$t_{\rm d} = -\frac{2C_L}{K_n} \int_{1.8}^{0.2} \left[\frac{1}{a} \left\{ \frac{1}{(a - V_{\rm o})} - \frac{1}{V_{\rm o}} \right\} + \frac{1}{E_{\rm n}\ L_{\rm n}} \frac{1}{(a - V_{\rm o})} \right] {\rm d}V_{\rm o}$$

$$t_{\rm d} = \frac{2C_{\rm L}}{K_{\rm n}} \int_{1.8}^{0.2} \left[\frac{1}{a} \left\{ \log_{\rm e}(V_{\rm o} - a) - \log_{\rm e} V_{\rm o} \right\} + \frac{1}{E_{\rm n}\ L_{\rm n}} \log_{\rm e}(V_{\rm o} - a) \right]$$

$$t_{\rm d} = \frac{2C_{\rm L}}{K_{\rm n}} \left[\frac{1}{a} \log_{\rm e} \frac{(V_{\rm o} - a)}{V_{\rm o}} + \frac{1}{E_{\rm n}\ L_{\rm n}} \log_{\rm e}(V_{\rm o} - a) \right]_{1.8}^{0.2} \tag{3}$$

The delay cell is supposed to provide a certain amount of delay without creating any phase difference in the input and output signal. So, a combination of two inverters is used here. Also, the delay cell must be compliant with the sub 6 GHz 5G standard, as per the scope of this work. For this application, the calculated time period is 166 ps. Again, the delay element has to provide a total delay ($t_{\rm total\ delay}$) of 166 ps < $t_{\rm total\ delay}$ <249 ps to get a divide-by-5 output. So, the delay of every inverter ($t_{\rm d}$) is fixed to 83 ps. The circuit is designed for 180 nm technology node, and accordingly, the process defined parameters are set, where supply voltage ($V_{\rm dd}$) = 1.8 V, input voltage ($V_{\rm i}$) = 1.8 V, threshold voltage of NMOS ($V_{\rm t,n}$) = 0.477 V, threshold voltage of PMOS ($V_{\rm t,p}$) = − 0.513 V, saturation voltage of NMOS ($V_{\rm sat,n}$) = 0.0409 V, saturation voltage of PMOS ($V_{\rm sat,p}$) = − 0.0364 V, transconductance parameter of PMOS ($K_{\rm p}$) = $\mu_{\rm p}C_{\rm ox}$ ($W_{\rm p}/L_{\rm p}$) = 40 μA/v^2, and transconductance parameter of NMOS ($K_{\rm n}$) = $\mu_{\rm n}C_{\rm ox}$ ($W_{\rm n}/L_{\rm n}$) = 140 μA/v^2, where $\mu_{\rm n}$ stands for the carrier mobility of NMOS, $\mu_{\rm p}$ stands for the carrier mobility of PMOS and $C_{\rm ox}$ stands for the oxide capacitance. Width of NMOS ($W_{\rm n}$) = 2 $W_{\rm p}$ (width of PMOS), $K_{\rm R} = K_{\rm n}\ K_{\rm p} = 7$, $C_{\rm L}$ = 10 × 10^{-15} F and

$$a = 2(V_{\rm i} - V_{\rm t,n}) = 2(1.8{-}0.477) = 2.645 \tag{4}$$

3.1.1 Calculation of $\frac{E_{\rm p}}{E_{\rm n}}$ Value

We know,

$$\frac{W_{\rm p}}{W_{\rm n}} \frac{V_{\rm sat,p}}{V_{\rm sat,n}} = \frac{K_{\rm p}}{K_{\rm n}} \frac{E_{\rm p}}{E_{\rm n}} \tag{5}$$

Considering $L_n = L_p = L_{min} = 180\,nm$, we get,

$$\frac{E_p}{E_n} = \frac{\mu_n C_{ox}}{\mu_p C_{ox}} \frac{V_{sat,p}}{V_{sat,n}} = 3.117 \quad (6)$$

3.1.2 Calculation of *K* Value

$$K = \frac{E_p}{E_n} \frac{w_p}{w_n} \frac{L_n}{L_P}$$

where K is the ratio of design constraints, L_p is the channel length of PMOS

$$K = \frac{w_p}{2w_p} \frac{1}{\frac{E_p}{E_n}} = 0.1603 \quad (7)$$

3.1.3 Calculation of V_{th} CMOS Inverter

$$V_{th} = \frac{V_{t,n} + \sqrt{K}(V_{dd} - |V_{t,p}|)}{1 + \sqrt{K}} \quad (8)$$

where V_{th} is the threshold voltage of CMOS

$$V_{th} = \frac{0.477155 + \sqrt{0.1603889}(1.8 - |0.513692|)}{1 + \sqrt{0.1603889}} = 0.7085 \quad (9)$$

3.1.4 Calculation of $E_n L_n$

$$V_{sat,n} = V_{D,sat,n} = \frac{(V_{th} - V_{t,n}) E_n L_n}{\left(V_{th} - V_{t,n}\right) + E_n L_n} \quad (10)$$

$$0.0409632 = \frac{(0.708541 - 0.477155) E_n L_n}{(0.708541 - 0.477155) + E_n L_n}$$

$$E_n L_n = 20.0903 \quad (11)$$

3.1.5 Calculation of $E_p L_p$

As we know,

$$V_{\mathrm{SD,sat,p}} = V_{\mathrm{D,sat,p}} = \frac{(V_{\mathrm{dd}} - V_{\mathrm{th}} - |V_{\mathrm{t,p}}|)E_{\mathrm{p}}L_{\mathrm{p}}}{\left(V_{\mathrm{dd}} - V_{\mathrm{th}} - |V_{\mathrm{t,p}}|\right) + E_{\mathrm{p}}L_{\mathrm{p}}} \tag{12}$$

where $E_{\mathrm{p}}L_{\mathrm{p}}$ is the short channel effect of the PMOS

$$0.0364 = \frac{(1.8 - 0.708541 - 0.513692)E_{\mathrm{p}}L_{\mathrm{p}}}{(1.8 - 0.708541 - 0.513692) + E_{\mathrm{p}}L_{\mathrm{p}}}$$
$$E_{\mathrm{p}}L_{\mathrm{p}} = 25.677 \tag{13}$$

Now, from (2) we get,

$$83 \times 10^{-12} = \frac{2 \times 10 \times 10^{-15}}{140 \times 10^{-6} \times \frac{W_{\mathrm{n}}}{L_{\mathrm{n}}}}\left[\left\{\frac{1}{2.64569}\left(\log_{\mathrm{e}} \frac{9(0.2 - 2.64569)}{(1.8 - 2.64569)}\right)\right\} + \left\{\frac{1}{20.09037}\left(\log_{\mathrm{e}} \frac{(0.2 - 2.64569)}{(1.8 - 2.64569)}\right)\right\}\right]$$
$$\frac{W_{\mathrm{n}}}{L_{\mathrm{n}}} = 2.211 \tag{14}$$

3.2 Calculation of $\frac{W_p}{L_p}$ from K Value

$$K = \frac{\frac{W_{\mathrm{p}}}{L_{\mathrm{p}}}}{\frac{W_{\mathrm{n}}}{L_{\mathrm{n}}}} \frac{E_{\mathrm{n}}}{E_{\mathrm{p}}} \tag{15}$$

$$\frac{W_{\mathrm{p}}}{L_{\mathrm{p}}} = (0.1603889 \times 2.211 \times 3.117422) = 1.105 \tag{16}$$

3.3 Calculation of $\frac{W_n}{L_n}$ from Propagation Delay Constraint

$$\frac{W_{\mathrm{n}}}{L_{\mathrm{n}}} = \frac{C_{\mathrm{L}}}{\Gamma_{\mathrm{p,HL}}\ \mu_{\mathrm{n}}\ C_{\mathrm{ox}}} \frac{2}{E_{\mathrm{n}}L_{\mathrm{n}}} \frac{V_{50\%}[\left(V_{\mathrm{OH}} - V_{\mathrm{t,n}}\right) + E_{\mathrm{n}}L_{\mathrm{n}}]}{(V_{\mathrm{OH}} - V_{\mathrm{t,n}})^2} \tag{17}$$

where, $\Gamma_{\mathrm{p,\,HL}}$ stand for the input to output propagation delay time during high to low transition of the output, V_{OH} is the maximum output voltage when the output level is at logic “1”. Now, putting $\Gamma_{\mathrm{p,\,HL}} = 43$ ps we get,

$$\frac{W_n}{L_n} = \frac{10 \times 10^{-15}}{43 \times 10^{-12} \times 140 \times 10^{-6}} \frac{2}{20.09} \frac{1[\{1.8 - 0.47\} + 20.09]}{(1.8 - 0.47)^2} = 2.023 \quad (18)$$

Now, it can be noticed that the aspect ratio (W_n/L_n) found in (18) is smaller than (14). Thus, we take the larger ratio, which will satisfy both timing constraints, and determine the size of the NMOS transistor as $W_n = 397.9$ nm, for $L_n = 180$ nm.

3.4 Calculation of $\frac{W_p}{L_p}$ from Propagation Delay Constraint

$$\frac{W_p}{L_p} = \frac{C_L}{\Gamma_{p,LH}\, \mu_p\, C_{ox}} \frac{2}{E_p\, L_p} \frac{V_{50\%}[(V_{OH} - V_{OL} - |V_{t,p}|) + E_p\, L_p]}{(V_{OH} - V_{OL} - |V_{t,p}|)^2} \quad (19)$$

where, $\Gamma_{p,LH}$ stand for the input to output propagation delay time during low to high transition of the output, V_{OL} stands for the minimum output voltage when the output level is at logic "0".

$$\frac{W_p}{L_p} = \frac{10 \times 10^{-15}}{40 \times 10^{-12} \times 40 \times 10^{-6}} \frac{2}{25.67} \frac{1[\{1.8 - 0.2 - 0.51\} + 25.67]}{(1.8 - 0.2 - 0.51)^2} = 11.04 \quad (20)$$

Now, it can be noticed that the aspect ratio (W_p/L_p) found in (20) is larger than (16). Since the larger ratio will satisfy both the timing constraints and the K constraint, we determine the size of the PMOS transistor as $W_p = 1987$ nm, for $L_p = 180$ nm.

4 Conclusions

In this paper, a new approach to design the MCML divide-by-5 pre-scaler is presented. The proposed architecture utilizes two latches, two delay cells, and one XOR gate. The delay cells are so designed that the proposed pre-scaler can function at sub 6 GHz 5G communication standard. The theoretical foundations of the approach are established that may also be used for other communication standards.

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Analyzing the Effect of Various Reducing Agents and Their Concentrations on Gas Sensing Performance of Graphene Aerogel-Based Ammonia Sensor

Anju Yadav, Praveen Saini, and Ajay Agarwal

Abstract The reducing agents and their concentrations used during the synthesis of graphene aerogel (rGO, i.e., reduced graphene oxide) highly effect the chemical characteristics and gas sensing properties of the resulted material. Therefore, in this paper, in order to investigate their effect on gas sensing properties of graphene aerogel, we have synthesized graphene aerogel using three different reducing agents, i.e., thio urea, ammonia, and ethylene glycol. Further, to study the effect of reducing agent's weight ratio/concentration on the properties, we have used three different weight amounts of thio urea. In total five rGO samples were synthesized and characterized. In order to investigate their gas sensing properties, the gas sensing response characteristics of all five rGO samples were recorded toward 100 ppm ammonia concentration at room temperature. It is found that the two rGO samples, i.e., ammonia-treated rGO aerogel and thio urea-treated rGO aerogel (300 mg), show good gas sensing response toward 100 ppm concentration of ammonia gas (1.4% and 1.21%, respectively) at room temperature, while remaining three samples' gas sensing responses were very poor (0.102%, 0.205%, and 0.640%).

Keywords Graphene aerogel · Reduced graphene oxide (rGO) · Ammonia sensing · Gas sensor

1 Introduction

The rapid development of industry inevitably produces toxic gases like CO, NO_X, and NH_3 which are detrimental to human health. Among these, ammonia (NH_3) is irritating and corrosive in nature [1] and causes cellular destruction and tissue necrosis

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[2, 3]. Thus development of ammonia gas sensors has drawn a huge attention in the recent past, and different technologies have evolved [3]. Among them chemiresistor is frequently used in gas sensing due to its easy fabrication process, simple configuration, amenity for miniaturization, low cost, and its use in MEMS technology. Different materialistic candidates exploited as sensing element of chemiresistor are metal/metal oxide (such as SnO_2, WO_3, Fe_2O_3, ZnO), carbonaceous materials, and conducting polymer. However, the metal oxide-based gas sensors suffer from complex device fabrication process as these sensors require a micro-heater to achieve the required temperature. For room temperature gas sensing, conducting polymers and their composites have been widely utilized for ammonia gas sensing. Recently, graphene/rGO (reduced graphene oxide) has been widely considered for gas sensing applications [4–6]. It has shown significant improvements in gas sensing performance due to its excellent physical and electrical properties [7] exploited for gas sensing applications such as high carrier mobility, high carrier capacity, good thermal stability, high signal-to-noise ratio (due to their chemical structure and high quality of their crystal lattices), large surface area, and enhanced intrinsic charge transport due to high carrier mobility [8–10].

In this present work we report preparation and characterization of graphene aerogel-based ammonia gas sensor using different reducing agents. Use of graphene aerogel provides ease in sensor fabrication and moderate sensitivity due to its 3D morphology which increases surface area/volume ratio. This paper presents two important contributions. First, we have investigated the effect of three different reducing agents on ammonia gas sensing properties of graphene aerogel-based gas sensor. Second, we have analyzed the effect of reducing agent weight ratio/concentration on ammonia gas sensing properties of graphene aerogel-based gas sensor.

2 Material Synthesis, Characterization, and Gas Sensing Results

Materials Used for Synthesis of reduced Graphene Oxide (rGO): Different materials used for synthesis of rGO were graphite powder (CDH, India), sodium nitrate (Fisher Scientific, India), sulfuric acid (98% Merck, India), potassium permanganate (Fisher Scientific, India), hydrochloric acid (37%, MERCK, India), hydrogen peroxide (Specpure Chemicals, India), and hydrazine hydrate (Thomas Baker, India). All these materials were of analytical grade and used on as-received basis. Distilled water was used for synthesis and washing.

Synthesis Process: Synthesis of rGO from natural graphite powder involves three major synthesis steps, i.e., synthesis of graphene oxide (GO), synthesis of reduced graphene oxide (rGO) hydrogel, and synthesis of reduced graphene oxide (rGO)

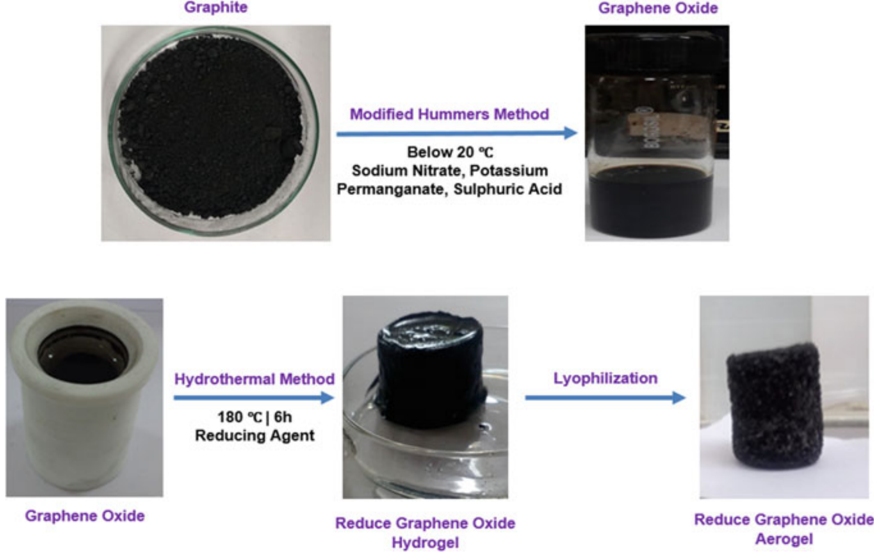

Fig. 1 Illustration of rGO Aerogel Synthesis Process

aerogel. The complete synthesis process explaining these major steps is shown in Fig. 1 and explained in the following text.

Synthesis of Graphene Oxide: Synthesis of graphene oxide (GO) was done by using modified Hummers method [11, 12]. It is obtained by oxidizing graphite powder. In this synthesis procedure, 70 mL sulfuric acid was magnetically stirred in a glass beaker followed by successive addition of 3 g of graphite powder and 3 g of sodium nitrate. A homogenous mixture was formed by stirring of the mixture for 30 min. It is followed by gradual addition of 9 g potassium permanganate ($KMnO_4$) flakes to the reaction mixture at ice bath while keeping temperature below 20 °C. The mixture was kept at continuous stirring at room temperature. After 18 h, a purple color paste was formed. 140 mL distilled water was added to this thick paste gradually which has changed its color to brown and increased reaction temperature to 98 °C. Mixture is stirred for 20 min followed by dilution with 440 mL distilled water and addition of 20 mL hydrogen peroxide. This has changed mixture color to bright yellow. Natural pulp of GO was obtained from this bright yellow color mixture by its filtering and washing several time with hydrochloric acid and distilled water which has removed the salt and acidic impurities. This pulp was then dried in vacuum oven at 45 °C to obtain the GO flakes.

Synthesis of reduced Graphene Oxide (rGO) Hydrogel: Synthesized graphene oxide (GO) flakes were added to 100 mL of distillated water (2 mg / mL). After 1 h of sonication, 35 mL of this obtained solution and 5 mL of ammonia solution were taken in a 40-mL capacity Teflon-stainless steel autoclave which was then kept into an oven under autogenous pressure at a temperature of 180 °C for 6 h. It was

followed by cooling of the autoclave to the room temperature. So obtained graphene hydrogel in the autoclave was dipped for 24 h into distilled water to remove the residual material.

Synthesis of reduced Graphene Oxide (rGO) Aerogel: rGO aerogel was obtained by keeping the prepared rGO hydrogel in the lyophilizer for 24 h.

It is generally believed that the reducing agent used and its weight amount used during rGO synthesis can affect the properties and morphology of rGO, which would change the gas sensing characteristics of the synthesized rGO material. Therefore, in order to evaluate the effect of reducing agent type on the gas sensing characteristics, the rGO was synthesized by using three different reducing agents, i.e., thio urea, ammonia, and ethylene glycol. Further to evaluate the effect of weight amount, rGO with thio urea reducing agent was synthesized for three different weight amounts of thio urea, i.e., 500 mg, 300 mg, and 200 mg. For all these three cases, 80 mg of GO amount was taken. rGO with ammonia reducing agent was synthesized by taking 70 mg GO and 5 ml ammonia. For synthesis of rGO with ethylene glycol reducing agent, 80 mg of GO was taken, and 10 mg of ethylene glycol was taken. The details of all these five synthesized rGO samples are shown in Table 1.

Gas Sensor Device Preparation: Five chemiresistive gas sensor devices were prepared over glass substrates (with platinum-patterned interdigitated electrodes (IDEs) structure) by using ammonia-treated rGO aerogel, ethylene glycol-treated rGO aerogel, thio urea-treated rGO aerogel (500 mg), thio urea-treated rGO aerogel (300 mg), and thio urea-treated rGO aerogel (200 mg). To prepare the device, solution of synthesized sample was spin coated onto glass substrate (with platinum-patterned interdigitated electrodes) at 1000 RPM to realize the thin film constituted of synthesized sample.

Ammonia Gas Sensing Results: The gas sensing response characteristics of the five prepared devices were studied toward 100 ppm ammonia concentration at room temperature in terms of their relative response (%) characteristics [(100 x (R_a −

Table1 Details of synthesized rGO samples

Material/sample	Reducing agent	Reducing agent amount	GO amount (mg)
Ammonia-treated rGO aerogel	Ammonia	005 mL	70
Ethylene glycol-treated rGO aerogel	Ethylene glycol	010 mg	80
Thio urea-treated rGO aerogel (500 mg)	Thio urea	500 mg	80
Thio urea-treated rGO aerogel (300 mg)	Thio urea	300 mg	80
Thio urea-treated rGO aerogel (200 mg)	Thio urea	200 mg	80

Table 2 Gas sensing response of different rGO samples

Material/sample	Ammonia concentration (PPM)	Gas sensing response (%)
Ammonia-treated rGO aerogel	100	1.400
Ethylene glycol-treated rGO aerogel	100	0.102
Thio urea-treated rGO aerogel (500 mg)	100	0.205
Thio urea-treated rGO aerogel (300 mg)	100	1.210
Thio urea-treated rGO aerogel (200 mg)	100	0.640

$R_g)/R_a$) where R_a is initial resistance in pure air and R_g is resistance in presence of ammonia gas]. The results are tabulated in Table 2.

It is observed that ammonia-treated rGO has resulted in better gas sensing response (1.4%) as compared to ethylene glycol and thio-treated rGO. Thio urea-treated rGO aerogel (300 mg) also shows the comparable gas sensing response (1.2%) toward 100 ppm concentration of ammonia gas at room temperature. The remaining three samples (ethylene glycol-treated rGO aerogel, thio urea-treated rGO aerogel (500 mg), and thio urea-treated rGO aerogel (100 mg)) exhibited very poor gas sensing response (i.e., 0.102%, 0.205%, and 0.640%, respectively). The surface morphologies of the two rGO samples, i.e., ammonia-treated rGO aerogel and thio urea-treated rGO aerogel (300 mg), were observed using FESEM (Fig. 2) to investigate their properties causing the better gas sensing response. It is clear from the FESEM images that the ammonia-treated rGO aerogel (Fig. 2b) is highly porous in nature as compared to thio urea-treated rGO aerogel (300 mg) and this could

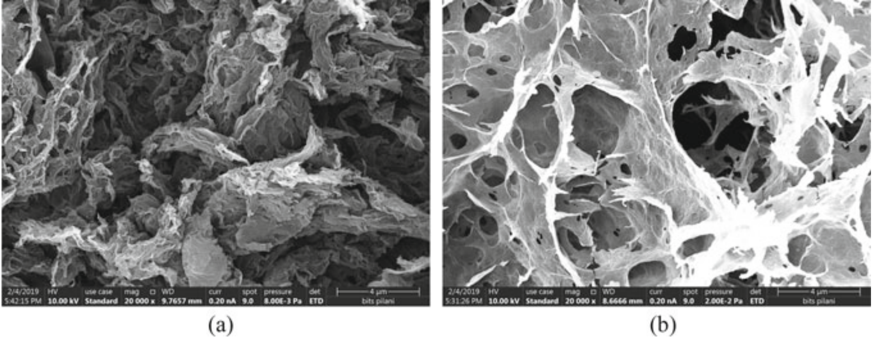

Fig. 2 **a** Thio urea-treated rGO aerogel (300 mg) and **b** ammonia-treated rGO aerogel

be considered among the main reasons causing the better gas sensing performance toward ammonia.

3 Conclusions

In this work, graphene oxide was synthesized from natural graphite power by using the modified Hummers method. This was followed by synthesis of reduced graphene oxide (rGO) hydrogel and reduced graphene oxide (rGO) aerogel. The reducing agents used during the synthesis of rGO highly effect the chemical characteristics and gas sensing properties of the resulted material. We have investigated this by synthesizing rGO using three different reducing agents, i.e., thio urea, ammonia, and ethylene glycol. Further, to study the effect of reducing agent weight ratio/concentration on the properties, we have considered three different weight amounts of thio urea, i.e., 500 mg, 300 mg, and 200 mg. In total five different rGO samples were synthesized, i.e., using ammonia reducing agent, using ethylene glycol reducing agent, and using three different weight amounts of thio urea reducing agent. In all cases of thio urea reducing agent, 80 mg of GO amount was taken during synthesis. rGO with ammonia reducing agent was synthesized by taking 70 mg GO and 5 ml ammonia. For synthesis of rGO with ethylene glycol reducing agent, 80 mg of GO was taken and 10 mg of ethylene glycol was taken. In order to investigate their gas sensing properties, the gas sensing response characteristics of all five rGO samples were recorded toward 100 ppm ammonia concentration at room temperature. It is found that the two rGO samples, i.e., ammonia-treated rGO aerogel and thio urea-treated rGO aerogel (300 mg), show good gas sensing response toward 100 ppm concentration of ammonia gas (1.4% and 1.21%, respectively) at room temperature, while remaining three samples' gas sensing responses were very poor (0.102%, 0.205%, and 0.640%). Surface morphology studies revealed that ammonia-treated rGO aerogel sample is porous in nature as compared to thio urea-treated rGO aerogel (300 mg) sample and this could be considered among the main reasons causing the better gas sensing performance toward ammonia.

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Performance Evaluation of Double-Gate Tunnel Field-Effect Transistor with Germanium Epitaxial Layer

Radhe Gobinda Debnath and Srimanta Baishya

Abstract In this study, a double-gate tunnel field-effect transistor with germanium epitaxial tunnel layer (Ge ETL-DGTFET) combining line tunneling orientation was proposed. This CMOS process compatible structure shows better performance in terms of ON-state current and subthreshold swing than silicon-based ETL-DGTFET and GOSO TFET due to the low bandgap ETL region. It exhibits an average subthreshold swing (SS_{avg}) of 30 mV/decade and I_{ON} of 0.7 mA/μm. Furthermore, the simulation results show a high cut-off frequency (f_T) of 65 GHz, a decent intrinsic delay of 3 pSec, and an energy-delay product (EDP) of 0.006 fJ.nS/μm at a supply voltage (V_{DD}) of 0.7 V. The design concept and effect of design parameters on the device performance are thoroughly discussed in this study.

Keywords BTBT · Double-gate TFET · Epitaxial tunnel layer · Line tunneling

1 Introduction

During the last decade, there has been extensive research to develop a novel MOS device using material and structural engineering [1, 2]. Tunnel field-effect transistor (TFET) is capable of overcoming MOSFET limitations. Despite the sub-60 mV/dec subthreshold swing, the significant restriction of TFET is low ON-state current. It is difficult to improve the on-current of TFET while sustaining low OFF-state conduction [3]. The gate overlapping on the source and drain region is another approach to enhance the device performance in TFETs at the cost of high onset of tunneling [4]. Furthermore, to strengthen conduction, counter-doped source pocket line tunneling TFET has also been explored [5, 6]. Recently, to make the TFETs suitable for low-power/low-voltage applications, epitaxial layer (ETL) TFET structures based on line tunneling were proposed [7, 8]. Various researches were conducted to boost the on-current of TFET using heterojunction structure [9, 10]. The literature shows that all

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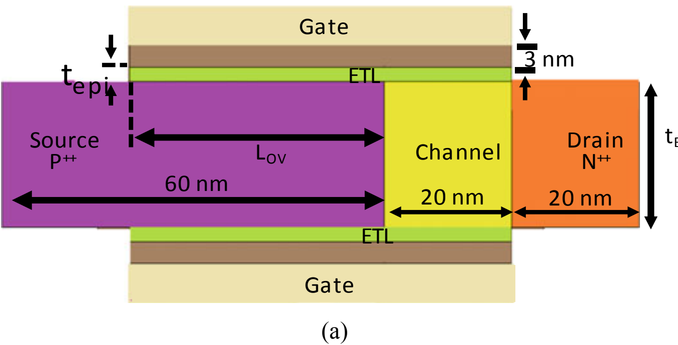
the heterostructure TFET used low bandgap material (germanium) as the source and high bandgap material as a channel and epitaxial layer [11, 12].

This paper proposed a Ge epitaxial layer-based double-gate TFET and shows that TFET with low bandgap material as epitaxial region achieves high ON-current and improved SS. The study's approach is straightforward: Line tunneling in ETL structure is boosted by growing a low bandgap material as the epitaxial layer on the silicon substrate and overlapping the gate to the source. Due to the double gate and gate-to-source overlap, the gate controllability increases, which increases the tunneling efficiency [13]. Therefore, TFET structures based on line tunneling due to the low bandgap epitaxial layer can be a promising applicant for efficient device performance. In contrast to the low bandgap source structure, our proposed structure with the germanium ETL region achieves improved I_{ON} and SS. The operation and design parameters of the proposed ETL-DGTFET were thoroughly explored.

2 Device Model and Simulation Setup

The 2D structures of the proposed ETL-DGTFET based on Si/Ge heterojunction is shown in Fig. 1. The device dimensions shown in Fig. 1 were used for the study unless stated otherwise. As shown, ETL-DGTFET employs an epitaxial layer above the source and channel regions under the gate-oxide stack. The conventional DGTFET has only point tunneling where tunneling occurs perpendicular to the gate field [14], whereas in the proposed device, in addition to point tunneling (Source to intrinsic channel), line tunneling (source to ETL), where tunneling occurs parallel to the gate field, also contributes to conduction. The drain and source regions were doped with an optimized arsenic concentration of 1×10^{19} cm^{-3} and a boron concentration of 5×10^{20} cm^{-3}, respectively. The intrinsic region and epitaxial region were very lightly doped with an arsenic concentration of 1×10^{15} cm^{-3}. Both the regions act



(a)

Fig. 1 Two-dimensional structure of ETL-DGTFET

as a channel for the device under consideration. At the interface, an abrupt doping profile was considered.

The ON-state current (I_{ON}) and OFF-state current (I_{OFF}) were evaluated at $V_{GS} = V_{onset} + V_{DD}$, and $V_{GS} = 0$ V, respectively, keeping $V_{DS} = 0.7$ V. The onset voltage (V_{onset}) is demarcated at the V_{GS} considering I_{DS} of 50 pA/μm [15]. The constant current method at 1×10^{-7} A was used to extract the threshold voltage (V_{th}). The subthreshold swing (SS) reported is the average SS calculated using the inverse slope of the transfer characteristics curve within the range of V_{OFF} (V_{GS} corresponding I_{DS} = 50 pA/μm) and Vth.

The Santaurus TCAD tool [16] was used for the numerical simulation of the device. Different models like the Slotboom mobility model, the bandgap narrowing model and Fermi distribution were activated. High field mobility saturation model was also incorporated to estimate the carrier transport at the thin ETL layer. Doping dependence SRH model and Hurkx TAT model with calibrated parameters taken from [17] were included in the simulation. A minimal offset for Γ and L valley CB minimum leads to direct BTBT in Ge material. Hence, the calibrated fitting parameters of the direct BTBT model for Ge were considered in the simulation. Simultaneously, the CB minima for both Γ, Δ valley for Si and Γ, L valley for Ge were also used [18]. The twofold strategy has been used to consider the quantization effect on the thin ETL layer [19]. The density gradient model parameter (γ) is calibrated with the results obtained from the Schrodinger–Poisson solver. Quantum potential obtained from the density gradient model was used to calculate redistributed carrier density. Simultaneously, the calculated quantum potential was added to the bandgap by incorporating the quantum potentials into the dynamic non-local BTBT model [16]. The parameters A_{dir}, B_{dir}, A_{ind} and B_{ind} for Ge were taken from [20], whereas A_{ind} and B_{ind} for Si were used from [18].

3 ETL-DGTFET Design Concept

The Si/Ge heterostructure was recently found to be a potential material combination for TFET device design [21–24]. Generally, a source with low bandgap material and a channel with a high bandgap are used to design TFET devices [5, 25]. The lower bandgap of source material enhances I_{ON} and simultaneously increases the leakage current [26]. I_D-V_G curve for the ETL-DGTFET structure employing different material combinations is shown in Fig. 2a. The Si/Ge combination showed better performance than other material combinations due to the boosted High electric field BTBT (HE BTBT) because of the low bandgap epitaxial layer, whereas VB offset at the epitaxial region suppresses the low electric field (LE) BTBT generation (Fig. 2b) [26]. Hence, the leakage current reduces, and the subthreshold swing improves.

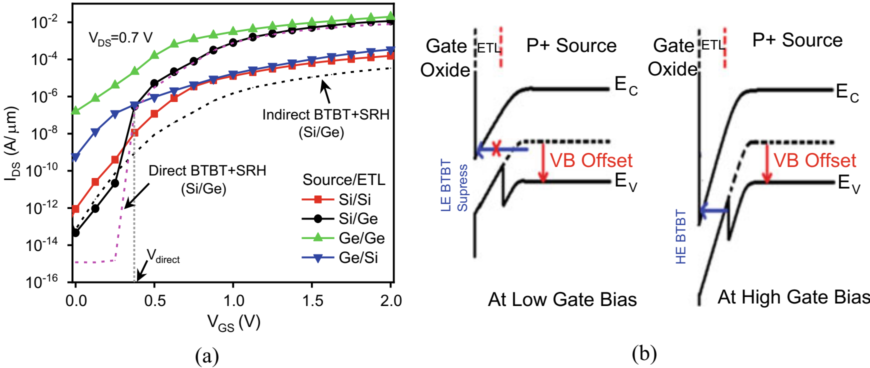


Fig. 2 **a** ETL-DGTFET transfer characteristics with different material combinations (*Source* / ETL material), **b** energy band profiles to illustrate LE BTBT suppression due to VB offset

4 Impact of Structural Variation

This section explains device design parameters' influence on the I_{ON}/I_{OFF} ratio, SS, and V_{th}. The design parameters considered are epitaxial layer thickness (t_{epi}) and gate-to-source overlap length (L_{OV}). The transfer characteristics of ETL-DGTFET is susceptible to the design parameter t_{epi}. To analyze the impact of t_{epi} on the device performance, t_{epi} was varied from 2 to 5 nm, while other design parameters were kept constant. As shown in Fig. 3a, the I_{OFF} increases with the increase in t_{epi}. The thickness of the ETL region should be small to enhance performance. This enhanced device characteristics with thinner t_{epi} are elucidated with the energy band profile extracted at a vertical cutline $x = 40$ nm. Figure 3b shows that at higher t_{epi}, the CB and VB of the ETL region are aligned, and a BTBT occurs at OFF state, which increases the leakage current in the device. But at a significantly smaller t_{epi} ($t_{epi} =$

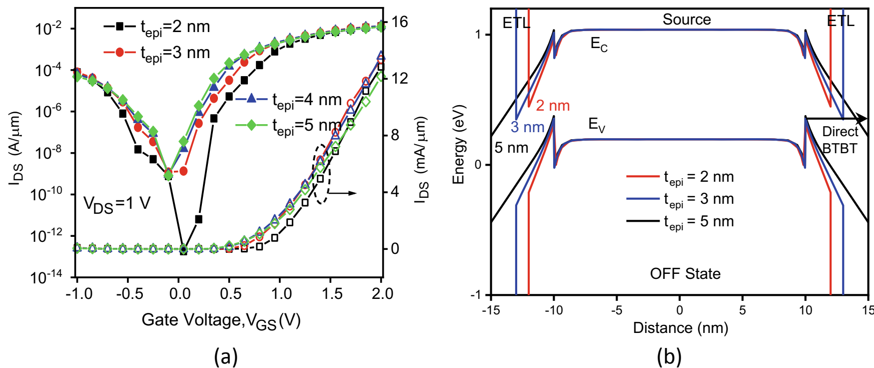


Fig. 3 **a** Influence of ETL thickness on transfer characteristics, **b** energy band profile along with $X = 40$ nm at the OFF state of ETL-DGTFET

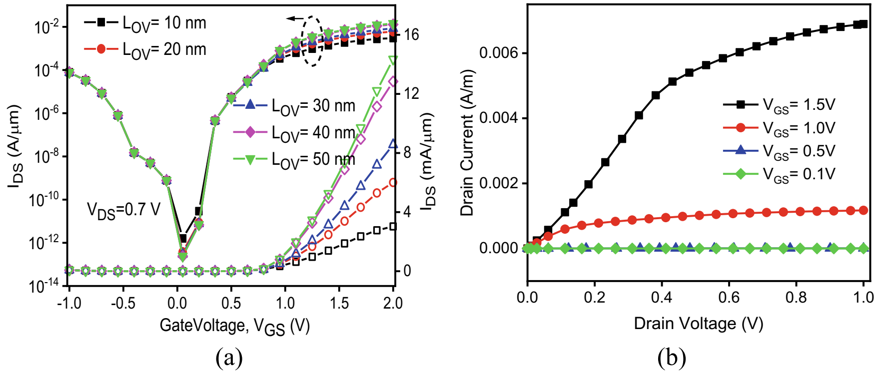


Fig. 4 **a** Impact of L_{OV} on the transfer characteristics, **b** output characteristics of ETL-DGTFET

2 nm), the misalignment of the CB and VB of the ETL region suppresses this direct BTBT.

Gate to source overlap length (L_{OV}) is also a key design parameter for ETL-DGTFET. The impact of L_{OV} variation on the device performance is studied by varying it from 10 to 40 nm, keeping the remaining structural parameters constant. An increase in L_{OV} enhances the ON-state current, as shown in Fig. 4a. The effective cross-sectional area for BTBT from source to ETL increases with the rise in L_{OV}, which leads to increased line tunneling and thus improves the ON-state conduction. The output characteristics of the proposed device for different gate bias is shown in Fig. 4b. For a particular gate voltage, increasing drain bias will initially reduce the electron density at the ETL region above the source; hence, the current increases linearly with V_{DS}. But this becomes independent once the V_{DS} reached saturation voltage (soft saturation region) due to complete depletion of the area. A further rise in V_{DS} drops across the ETL over the channel region. Finally, it becomes independent of V_{DS} once the region becomes depleted of carriers, and the device enters into the deep saturation [27].

The proposed structure has shown an improved DC performance in terms of SSavg and I_{ON}. But a high ambipolar current (I_{amb}) was also witnessed in the device characteristics. As the ambipolar has an impact on TFET-based circuit operation, different approaches were adopted to improve the ambipolar behavior of the TFET device [28]. In this work, the gate to drain underlap was incorporated in the structure to improve its ambipolar current, and the effect of underlap length (L_{und}) on the device performance has been investigated [29]. Increasing L_{und} reduces the Iamb by reducing the BTBT at the drain side (Fig. 5a). The gate underlap reduces the lateral electric field at the drain channel junction as shown in Fig. 5b, and hence suppresses the BTBT from drain-to-channel region at very low or negative gate voltage. An optimized value of L_{und} = 15 nm is obtained for the proposed device because increasing L_{und} above 15 nm significantly affects the $I_{ON,}$ as shown in Fig. 5a. This is because the extreme increase in underlap length significantly decreases the

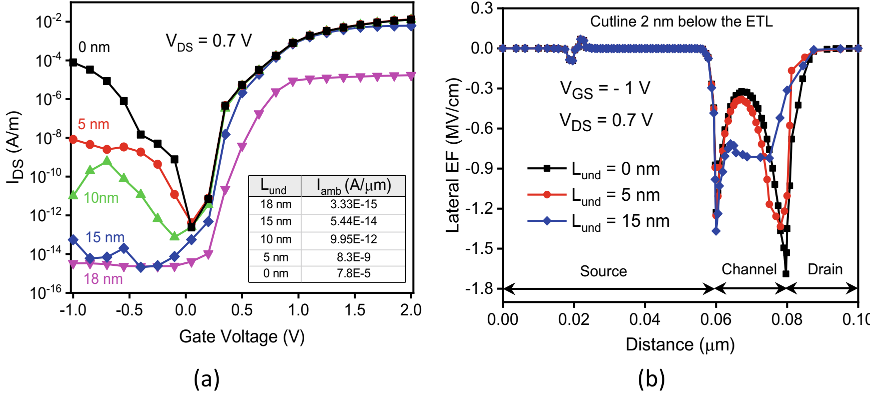


Fig. 5 Impact of L_{und} on **a** the transfer characteristics of ETL-DGTFET **b** lateral electric field along y cutline

epitaxial layer area, which leads to the reduction in the direct BTBT in the ETL region at higher V_{GS}.

5 DC Performance Comparison

To get a deep insight into the DC performance of the proposed device, the I_D–V_G characteristics of ETL-DGTFET is compared with silicon-based ETL-DGTFET and gate on source only (GoSo) TFET with L_{gc} (gate channel overlap) [30]. The workfunction is optimized to maintain approximately the same I_{OFF} in all the device structures for better comparisons. Figure 6a shows the comparative plot of transfer characteristics for different devices considering the same gate length. It is observed

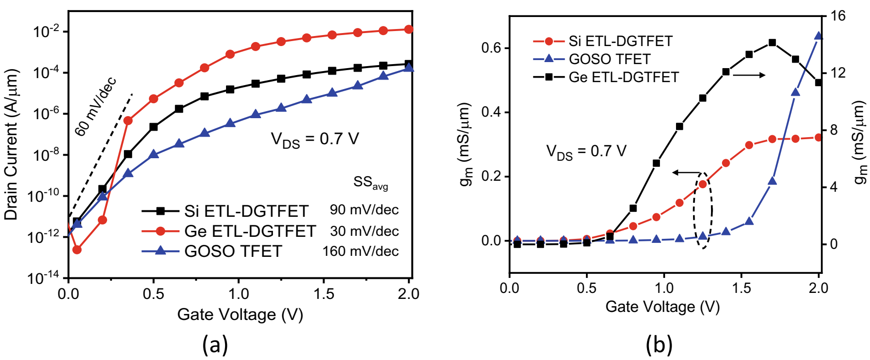


Fig. 6 Comparative **a** transfer characteristics plot **b** g_m variation with V_{GS} of Ge ETL-DGTFET, Si ETL-DGTFET, and GoSo TFET at $V_{DS} = 0.7$ V

that the proposed device Ge ETL-DGTFET delivers enhanced performance in terms of I_{ON} and SS_{avg} than its counterparts. The I_{ON}/I_{OFF} ratio is increased in the case of Ge ETL-DGTFET by two orders of magnitude compared with Si ETL-DGTFET, and three orders of magnitude with GoSo TFET at $V_{DS} = 0.7$ V. Improved SS_{avg} of 30 mV/dec is also observed for Ge ETL-DGTFET. A higher I_{ON} of 0.7 mA/μm is obtained in the case of Ge ETL-DGTFET, whereas 7 μA/μm and 0.1 μA/μm ON-current are witnessed for Si ETL-DGTFET and GoSo TFET, respectively. This improvement is attributed to the low bandgap ETL region, which boosts the ON-state tunneling and suppresses the LE BTBT due to VB offset with the source region.

The transconductance (g_m) variation with V_{GS} for all the considered devices is shown in Fig. 6b. With the increase in V_{GS}, g_m increases initially due to the enhanced BTBT rate. But as V_{GS} increases further, there is a deterioration in gm owing to the mobility degradation [31]. The Ge ETL-DGTFET shows a higher gm than its counterpart Si ETL-DGTFET and GoSo TFET. This is due to the enhanced SS of the device attributed to the low bandgap ETL region.

6 Analog/RF Performance

The figure of merits (FOMs) like intrinsic capacitances, f_T, intrinsic delay (τ), and EDP are evaluated for the proposed device. Its performance is compared with silicon-based ETL-DGTFET and GoSo structures with the same gate length. Transconductance generation factor (TGF = g_m/I_{DS}), an essential parameter for low-power analog applications, is desired to be high for any device to operate at a lower voltage. A comparison of TGF is shown in Fig. 7a. Our proposed device offers a higher value of TGF than its counterparts. It is also observed that Ge ETL-DGTFET surpasses the theoretical limit (38.5 V^{-1}) of the MOSFET at a higher I_{DS}.

Small signal ac analysis was carried out at a constant frequency (1 MHz) to evaluate the intrinsic capacitance. Due to the gate-source overlap for all the considered devices, both *C*gd and *C*gs' contribution in the total gate capacitance (C_{gg}) are accountable, unlike in conventional DGTFET, where the C_{gd} dominates C_{gg} due to the high source/channel potential barrier. The variations of C_{gg} and C_{gs} with V_{GS} are shown in Fig. 7b. It is observed that GOSO TFET shows higher C_{gs} and C_{gg} than ETL-DGTFET. The much-reduced C_{gg} of Ge ETL-DGTFET is beneficial for improvement in intrinsic delay and cut-off frequency. The variation of f_T with V_{GS} is shown in Fig. 7c. The unity current gain frequency (f_T) is directly related to gm and inversely proportional to C_{gg} [32]. Hence, an increase in f_T with V_{GS} is witnessed due to increased g_m. Our proposed device showed a higher f_T than its counterparts. The improvement in f_T is attributed to the enhanced transconductance of Ge ETL-DGTFET. The proposed device exhibits a high f_T of GHz range ($f_T = 65$ GHz at $V_{DS} = 0.7$ V), making the device more suitable for high-frequency applications than the rest two.

The device performance is also analyzed using two additional FOMs for TFET, the intrinsic delay ($\tau = C_{gg}\, V_{DD} / I_{ON}$) and energy-delay product (EDP = $C_{gg} V_{DD}^2$

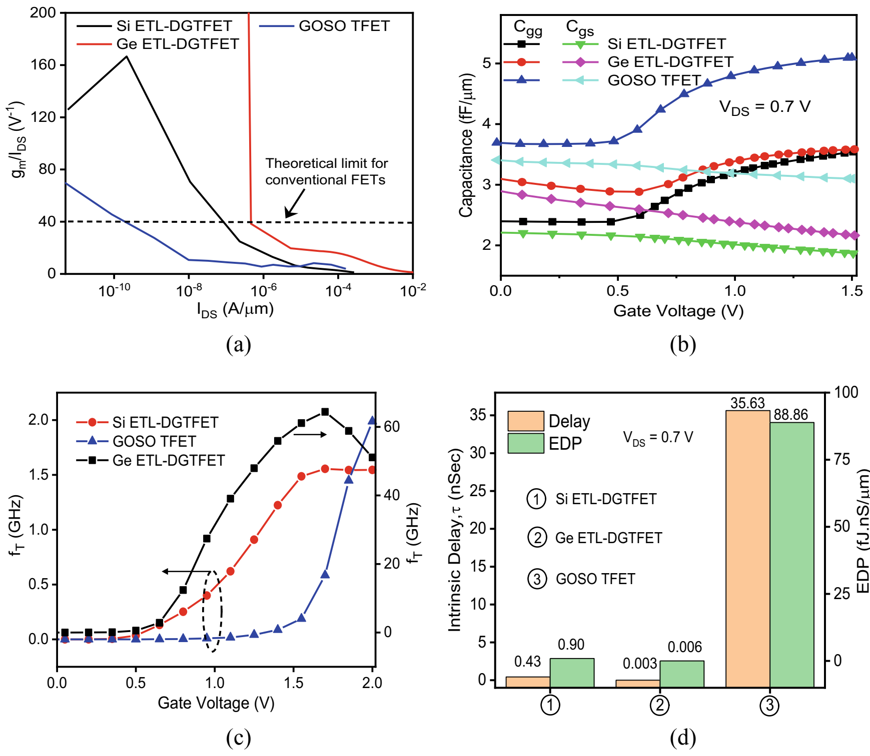


Fig. 7 A comparative plot of **a** TGF versus drain current, **b** C_{gg} and C_{gs} variation with V_{GS}, and **c** f_T as a function of V_{GS} **d** Intrinsic delay and EDP for different devices at $V_{DS} = 0.7$ V

τ). EDP represents the device's energy efficiency, which is the product of delay and intrinsic switching energy [33]. Figure 7d shows the τ and EDP for Ge ETL-DGTFET, Si ETL-DGTFET and GoSo TFET at a supply voltage of 0.7 V. Our proposed device Ge ETL-DGTFET shows the lowest delay and EDP. The delay of 3 pSec and EDP of 0.006 fJ.nSec/μm is witnessed for the proposed device. Lower C_{gg} and higher I_{ON} are responsible for the improved delay and EDP; hence more energy efficient than the rest two. Therefore, Ge ETL-DGTFET shows good digital performance and is more suitable for low-voltage and low-power digital applications.

7 Conclusion

In this work, double-gate TFET with Ge ETL structure (Ge ETL-DGTFET) is proposed, and its performance vis-à-vis other TFET devices is compared. Simulation results of the design parameters suggest an enhanced device performance of the proposed ETL-DGTFET. To achieve an enhanced ON-state current, 2 nm is the most

optimum ETL thickness for the device. Moreover, a gate-to-source overlap length of 40 nm is suitable for the device to achieve a better SS and an enhanced switching ratio. A comparative study of the device performance of the ETL-DGTFET based on Ge and Si epitaxial layer and GoSo TFET is evaluated comprehensively. The proposed device has an advantage of VB offset between the source and ETL region, which suppresses the LE BTBT and improves the proposed device's SS. A switching ratio of 2×10^8 with an SS_{avg} of 30 mV/decade is obtained for Ge ETL-DGTFET. The investigation shows a high cut-off frequency of 65 GHz, furthermore, with an optimized design parameter, a 3 pSec intrinsic delay, and 0.006 fJ. nSec/ μm EDP is also witnessed. The proposed structure can provide improved performance compared with other TFETs regarding DC and analog/RF. The implementation of ETL structure with low bandgap material could be a possible solution for the performance boosting of DGTFET.

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Rapid Detection of Biomolecules Using Dielectric Modulated Ferroelectric GaN HEMT

V. Hemaja and Deepak Kumar Panda

Abstract Biosensors are such devices that discover employment in our everyday life in various fields. In this manuscript, we have designed a ferroelectric GaN HEMT biosensor by using the dielectric modulation technique of cavity formation consisting of both ferroelectric layers and biomolecules. Ferroelectric GaN HEMT biosensor is reported for recognization of biomolecules such as protein, streptavidin, chox, and uricase. This work emphasis on the characterization and sensitivity performance of ferroelectric GaN high electron mobility transistor-based biosensor using SILVACO ATLAS software. The immobilization of biomolecules under the gate region results in a large variation of electrostatic properties such as drain current, threshold voltage which can be used as sensing metrics. A significant rise in the drain current with the increasing permittivity value of biomolecule in the nanocavity region. There is a maximum positive shift in threshold voltage that is scrutinized in case of protein as it bears low dielectric constant and also device offers good sensitivity performance.

Keywords Biosensor · High electron mobility transistors · Sensitivity

1 Introduction

The current COVID-19 widespread gathered focused on the detection of biomolecules, bio-weapons by virtue of the electronic biosensors. So, these electronic biosensors might find their employment in the actual time observation of airborne molecules via transportation systems like an airplane, railway, etc. Therefore, there is an ongoing requirement for the development of sophisticated, accurate, and rapid response biosensors [1].

GaN-based HEMT has attracted enormous attention for future generation radio frequency power, high-efficiency power switching applications that help in suppressing the gate leakage current, current collapse, and the enhancement of the breakdown voltage [2–11]. In comparison to traditional oxides and nitride dielectrics,

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ferroelectric materials are placed under the gate to obtain E-mode operation due to inherent nature i.e., strong polarization and gets switchable with the application in the electric field and that could be controlled by polarization of the ferroelectric gate insulator and threshold voltage control, higher maximum current density, lower value of R_{ON} and better V_{th} temperature stability in GaN-based transistors [12–15]. Ferroelectric devices have brought out its attention due to its potential device application in a wide range of uses like neuromorphic computing, steep slope transistors, memory, high speed memory applications, neural network application, and tunable microwave applications [16–20]. The combination of strong polarization in nitrides and switching polarization in Ferroelectrics provides better possible results in 2DEG enhancement and dynamic control in the threshold voltage, and it shifts to more change in positive value [20–24].

In this manuscript, we have carried out a simulation of ferroelectric GaN HEMT biosensor for label-free recognization of various biomolecules like protein, streptavidin, uricase, and chox by considering their dielectric constant values. The device structure is investigated and performed using the dielectric modulation technique. The device simulation is carried out using Silvaco Atlas software. Section 2 deals with the working principle of the biosensor. Section 3 deals with device architecture and simulation set up. Section 4 deals with results and discussion. Section 5 deals with the conclusion.

2 Working Principle

The working principle functions on the mechanism of biomarker and biomolecules introduced in the device. These biomarkers bind or link a huge number of samples. Once it gets into contact with it, there is sudden rise in the concentration level of biomolecules which leads to variation in the electrical characteristic of the device in terms of the electron concentration, drain current, threshold voltage, etc. Therefore, these sensors can detect how faster a device works.

3 Device Architecture

Figure 1 spotlight the schematic view of ferroelectric GaN HEMT. The device structure is composed of a 2-μm-thick GaN buffer layer, and a stack arrangement of $Al_{0.25}Ga_{0.75}$ N with the following dimensions of 2 nm, and two 5-nm-barrier layers, GaN substrate. Initially, the region under the gate is made cavity which was filled with HfO_2 as ferroelectric material, and later, two cavities of 0.6 μm HfO_2 and 0.5 μm dielectric layers of each are considered into the region I and II. In this work, the biomolecules are introduced in the cavity under the gate electrode. The permittivity values of these biomolecules are specified in Table1. All simulations are performed using silvaco atlas software. The different models

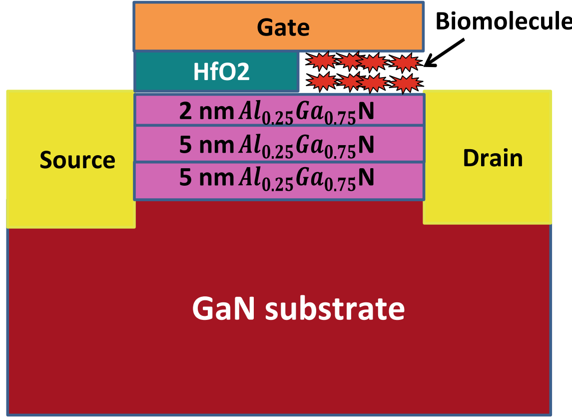

Fig. 1 Schematic view of ferroelectric GaN HEMT

Table 1 Permittivity values of biomolecules [1]

Biomolecules	Dielectric constant
protein	2.5
cho_X	3.5
uricase	1.5
streptavidin	2.1

which are used during simulation are the polarization model, field-dependent drift velocity(FLDMOB) model, concentration-dependent mobility model (CONMOB), and Shockley-Read-Hall(SRH) recombination model.

4 Results and Discussions

Figure 2 shows the output characteristic of ferroelectric-based HEMT. At first, we can observe here that without the introduction of biomolecules in the cavity region there is a lower range in current variation is observed. With the increase in permittivity value of biomolecules, there is a noticeable increase in drain current is depicted. From this figure, we can determine maximum rise that drain current is observed in the case of protein due to its low dielectric constant. A higher value in drain current leads to greater sensitivity.

Figure 3 depicts that without the application of biomolecules in the nanocavity region there is a negative change in threshold value is observed, whereas there is a fewer increase in the value of drain current that is observed as in the case of protein biomolecule. Higher drain current leads to higher transconductance value. With the rising increase in drain current value, we observe a positive shift in threshold voltage.

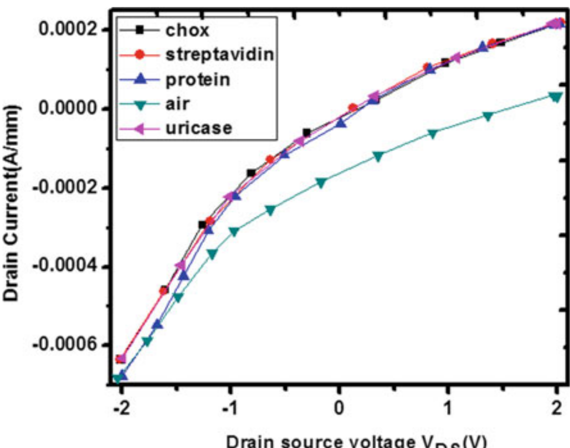

Fig. 2 Output drain current characteristic response for different biomolecules

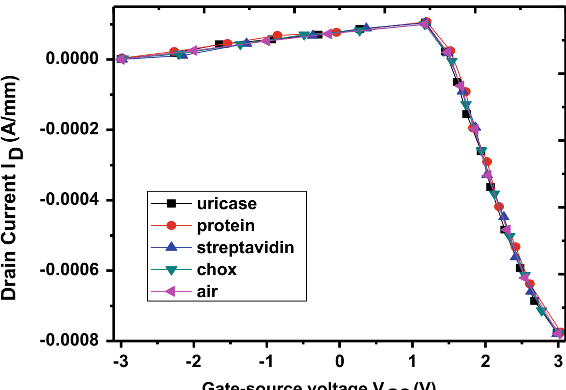

Fig. 3 Output drain current characteristic response for different biomolecules

From Table 2, It's clear that with the increasing permittivity value of biomolecules introduction in the nanocavity region there is a positive shift in threshold voltage is observed which implies a higher sensitivity performance in the device.

Figure 4 shows that change in threshold voltage is considered as useful sensing parameter for recognition of biomolecules. The two factors which reflect the change

Table 2 Comparison performance for the shift in threshold voltage versus dielectric constant (K)

Dielectric constant (K)	Threshold voltage (V)
Air	−0.1553
Uricase	1.451
Streptavidin	1.488
Protein	1.52
ChOx	1.51

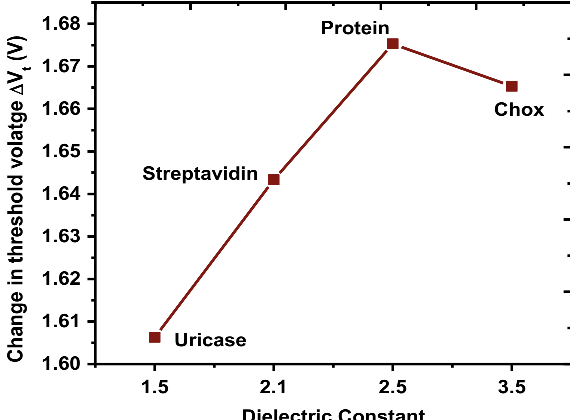

Fig. 4 Change in threshold voltage for different biomolecules

in ΔV_t are dielectric constant and charge effect. Higher change in ΔV_t leads to higher sensitivity as per the given Eq. 1.

$$\Delta V_{\text{th}} = V_{\text{th}}\,(\in_{\text{bio}}) - V_{\text{th}}(\in_{\text{air}}) \tag{1}$$

5 Conclusion

In this paper, we have implemented a ferroelectric GaN HEMT with a new concept of cavity formation under the gate layer consisting of ferroelectric in one region and biomolecules in another region with a varied dielectric constant value for acquiring higher value in sensitivity performance. The results obtained give a clear vision in the electrostatic performance improvement of drain current, threshold voltage which makes it feasible for AC and DC analysis. There is a significant improvement in the positive shift of threshold voltage on increasing permittivity value of biomolecules. The increase in sensitivity performance of the device is due to the higher drain current by varying its dielectric constant values. Therefore, its concluded that ferroelectric GaN HEMT proves significant improvement in sensing applications.

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A Low Leakage with Enhanced Write Margin 10T SRAM Cell for IoT Applications

Vaishali Yadav and V. K. Tomar

Abstract An increasing demand of on-chip assessment of data in IoT-based devices requires the design of low power on board memory circuits. In this context, a novel 10 T SRAM cell with lower power consumption and improved stability has been design and simulated on 45-nm technology node with cadence virtuoso tool. The loop cutting technique is utilized to improve the stability and minimize the power dissipation of 10 T SRAM cell. It has been noticed that read power consumption is reduced by 11.4% in 10 T SRAM cell as of standard 6 T SRAM cell. The read/write stability is enhanced by 2.4 times/ 2.36 times in comparison with standard 6 T SRAM cell. It occurs because of read decoupled structure. However, the read delay in 10 T SRAM cell is increased by 1.31 times in comparison with six-transistor SRAM cell.

Keywords Stability · Power consumption · Access time · Leakage

1 Introduction

Recently, Internet of Things (IoT)-based products like smart appliances, wearable health monitors, etc. are in the large demand in present-day electronic market [1, 2]. These devices are lightweight and small in size and require smaller rechargeable kind of battery which can support long lives. A processor is one of the main components of embedded system being utilized for the manipulation of the data, and an on-chip static random access memory (SRAM) is employed to store the information [3]. The total power consumed in system-on-chip (SoC) devices is basically elaborated in terms of power consumed by on-chip memory circuits. In SRAM cell, reduction in power consumption can be achieved by well-established methodology such as supply voltage scaling and operates SRAM cell in sub-threshold region. However,

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operating the SRAM cell in the weak inversion region faces many challenges like an increase in sensitivity to process variations.

Therefore, design of low power SRAM cell is very essential for IoT-based devices to minimize the power consumption with greater reliability. SRAM is a semiconductor memory cell which stores one bit data in the form of binary. SRAM cell has higher speed and also consumes less power as compared to dynamic random access memory [4]. Various SRAM circuits are proposed that consists of five transistors to twelve transistors. Multiple techniques to reduce power dissipation and improve access time and stability have been proposed. However, every technique has its own pros and cons. For instance, an increase in area overhead leads to the reduction in the number of SRAM bit cells per unit area. The six-transistor (6 T) SRAM cell has very simple architecture and also known as for industry standard due to its low power requirements. It works efficiently in super-threshold region. However, it faces many challenges like reduction in cell stability and increase in leakage current at lower supply voltage. An 11 T SRAM cell [5] operates in differential read and single-ended write mode which shows commendable increase in read/write stability along with reduction in power dissipation. Authors have also determined out the data retention voltages of the cell. Ashish Sachdeva et al. [6] presented a 10 T SRAM cell in which read/write stability increased along with the ion-to-bit-line leakage current ratio (Ion/Ioff). In this cell, half-select issue has resolved and loop cutting methodology used to minimize the power dissipation. Harekrishna et al. [7] presents a 12 T SRAM cell operates in sub-threshold region. In this cell, the reduction in the power dissipation is achieved along with improvement in read/write stability. Ahmad et al. [8] have reported Schmitt trigger-based variation-tolerant eleven-transistor SRAM cell. This cell works with enhanced read static noise margin (RSNM) due to read decoupled technique. Furthermore, authors in this paper have done comprehensive evaluation of proposed design while comparing the same with six already reported designs to prove its novelty. In this work, authors have also eliminated half-select issues in order to implement bit interleaving technique.

A ST12T SRAM topology [9] has been reported with the reduction in the power consumption and improvement in read/write delay. It is because of the Schmitt trigger-based design utilized in core latch of the cell. This cell also supports bit interleaving format and free from half-select issue. Another Schmitt trigger-based 10 T cell is reported by Kulkarni et al. [10] with improved read static noise margin. In addition to this, the reduction in the leakage/dynamic power has also been achieved with such arrangement. Authors have also claimed regarding improvement in access time and variation tolerance. In this work, analytical model for switching threshold voltage of Schmitt trigger inverter has also been reported. A novel 9 T cell has been characterized by Pal et al. [11] in which write operation is performed using feedback cutting technique. The stability of the cell is improved along with the reduction in the power dissipation. The cell shows resilience to process variations and mitigates half-select issue. Lo et al. [12] reported a PPN10T SRAM cell with improved read stability. These all discussed approaches show various trade-off with respect to area, delay and power dissipation. With the consideration of the above-discussed issues,

authors have designed and simulated a 10 T SRAM cell with enhanced characteristics like read/write stability, read/write power consumption and read/write access time. This paper is structured in the following manner. The working mechanism of the 10 T SRAM is discussed in Sect. 2. In Sect. 3, obtained results are simulated. The concluding remarks are included in Sect. 4.

2 10 T SRAM Bit-Cell Working Mechanism

Figure 1 presents the schematic diagram of 10 T SRAM cell. The core latch circuitry is made up of P1, N1 and P2, N2 transistors. N3 and N4 transistors work as access transistors. These transistor gate terminals are connected to WL signal. N5 and N6 transistors have the series connection with N1 and N2 transistors, respectively. N5 and N6 transistors work as dynamic loop cutting transistors. The gate terminals of these transistors are connected to BL and BLB, respectively. This 10 T SRAM cell has the separate read structure and works in a read decoupled mechanism. This resolves the access transistor conflicts issue and increases the RSNM. The utilized read decoupled structure facilitates the change in dimensions of N3 and N4 transistors which help to

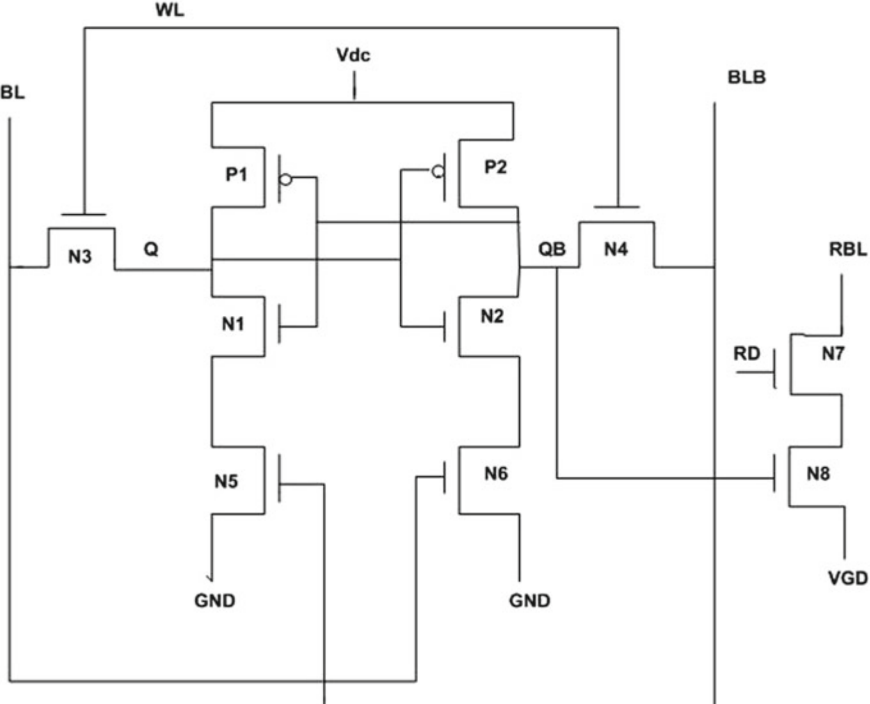

Fig. 1 10 T SRAM cell

Table 1 Logic level for different mode of operation in 10 T SRAM Cell

Signals	Read	Write ‘1’	Write ‘0’	Hold
RD	‘1’	‘0’	‘0’	‘0’
WL	‘0’	‘1’	‘1’	‘0’
VGD	‘0’	‘1’	‘1’	‘1’
BL	‘1’	‘1’	‘0’	‘1’
BLB	‘1’	‘0’	‘1’	‘1’
RBL	‘1’	‘0’	‘0’	‘0’

improve the write signal-to-noise margin. In this cell, it is possible to vary the size due to the read decoupled structure. Moreover, virtual read ground (VGD) signal is used to minimize the bit-line leakage current. The control signal status for different modes of operation is shown in Table 1.

2.1 Read Mode

Read bit-line (RBL) is connected to Vdd and VGD signal is attached to ground in read operation as shown in Table 1. Bit-lines and RD signals are attached to supply voltage. The bit-line effect at storage nodes is eliminated by WL signal connected to logic ‘0.’ Assume storage node Q stored logic ‘0’ which enables P1 transistor to create logic ‘1’ at node (QB). The node voltage at QB turns on N7 transistor which discharges the RBL through N7 and N6 transistors. This denotes logic ‘0’ is stored at the node Q as depicted in Fig. 2a.

2.2 Write Mode

Logic ‘0’ and logic ‘1’ are kept at RD and VGD signals in write operation. Both the bit-line (BL and BLB) signals work as input line which is connected to the write access transistor. The WL signal is connected to Vdd and RD signal is kept at logic ‘0.’ The bit-lines are attached to supply voltage and ground, respectively, to write logic ‘0’ at node Q. Due to this, the loop cutting transistors N5 and N8 are enabled and disabled, respectively. The written data are maintained by the core latch of the cell.

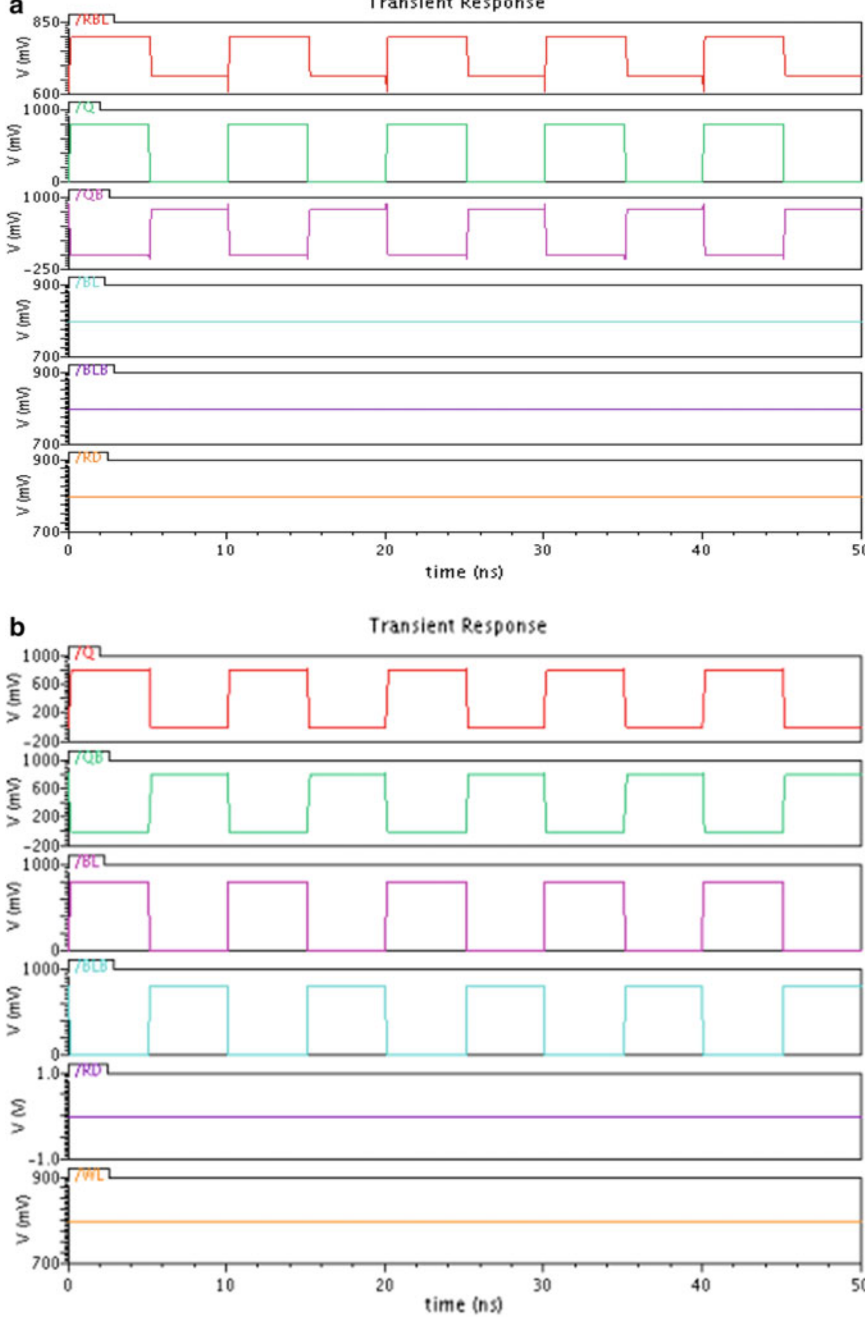

Fig. 2 **a** Read transient waveform, **b** write transient waveform of the proposed 10 T cell.

2.3 Hold Mode

It is well known that SRAM cell remains most of the time in hold state. During this state, bit-line leakage current plays a significant role when logic '1' is stored at storage nodes. Therefore, it is necessary to perform the analysis of power dissipation during hold mode. During this state, WL signal is maintained at logic '0' which disables the write access transistors to maintain the data at the storage node. RD signal is allied to logic '0,' whereas VGD signal is allied to '1' to minimize the leakage power consumption.

3 Result and Discussion

A 10 T SRAM cell is designed and simulated at 45-nm technology node on cadence virtuoso tool. A comparison of obtained characteristics of designed 10 T SRAM cell has been made with conventional 6 T and 8 T SRAM cells. These cells are tested with changing the supply voltages 0.5 V to 1 V.

3.1 Read/write Stability

Stability in SRAM cells can be expressed as the smallest value of DC noise voltage which is needed to alter the state of a cell [13]. RSNM is one of the important factors and measured graphically during read operation. This is calculated from the lobes of the butterfly curve. The measured side length of the largest square is termed as RSNM. The obtained values of RSNM of simulated SRAM cells are depicted in Fig. 3.

In 10 T SRAM cell, due to the use of read decoupled structure, RSNM is increased with a factor of 2.4 $\times$ and 2.26 $\times$ as of 6 T and 8 T SRAM cells. Further, conventional 6 T SRAM has smallest value of RSNM at 0.5 V because of weaker pull-down path. The write static noise margin (WSNM) at different supply voltages is shown in Fig. 4. The write margin of 10 T SRAM cell is enhanced by 2.36 $\times$ and 1.83 $\times$ as of conventional 6 T and 8 T SRAM cells. It occurs because loop cutting transistors are employed in core part of latch circuit [16].

3.2 Power Dissipation

In digital logic circuits, particularly in SRAM cell design, power dissipation got the major attention. SRAM cell is widely utilized in portable devices. Read power dissipation of the considered cells is depicted in Fig. 5 at various supply voltages.

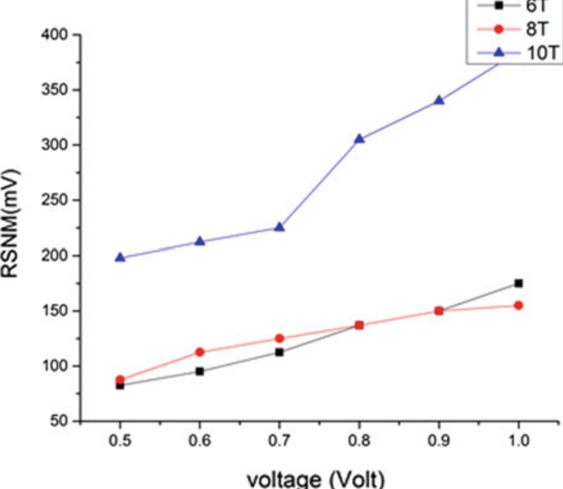

Fig. 3 RSNM at different supply voltage

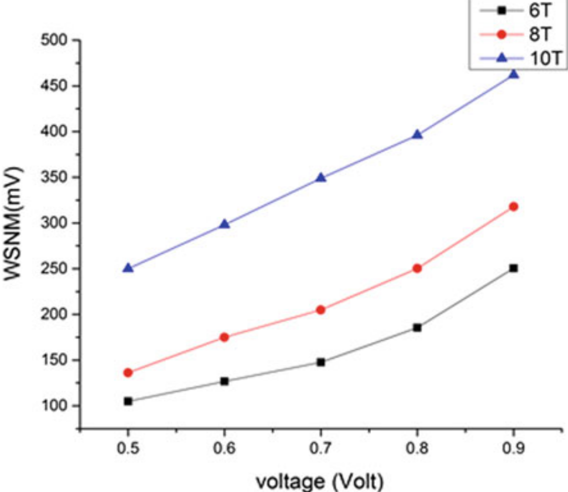

Fig. 4 Write ability with variation in supply voltages

This is noticeable that read power is reduced by 1.48 × and 1.45 × as achieved for 6 T and 8 T SRAM cells. Minimized activity factor can be the cause of such reduction in read power dissipation [14, 15]. Figure 6 shows the write power consumption of considered cells. The write power consumption of 10 T SRAM cell is reduced by 2.11 × and 1.34 × as of compared to 6 T and 8 T SRAM cells. It happens due to connection of pull-down network to the bit-lines.

In hold mode, standby power dissipation of considered SRAM cells is calculated at various supply voltage as depicted in Fig. 7. It is noticeable that leakage power of 10 T SRAM cell is found to be lowest among considered cells. It is because of

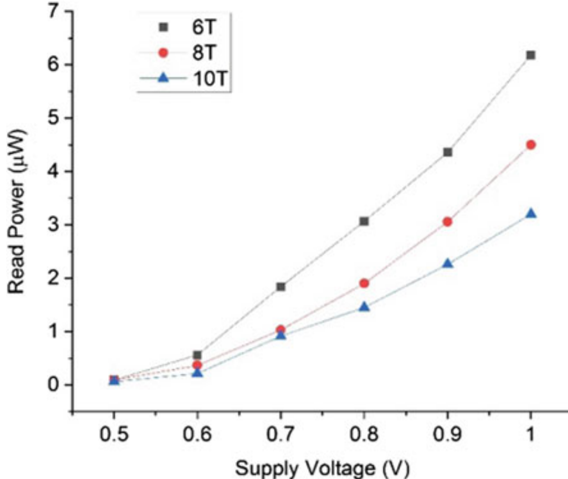

Fig. 5 Read power consumption at various supply voltages

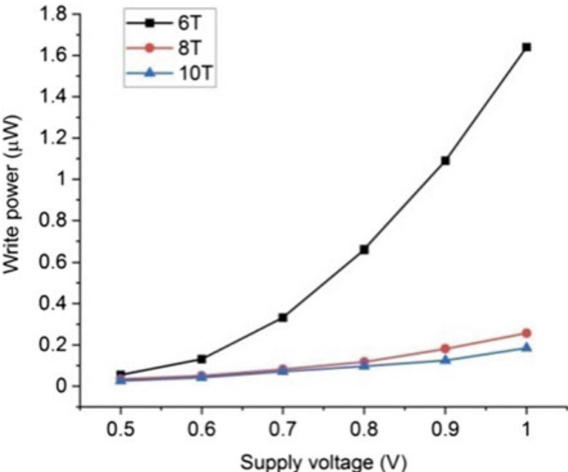

Fig. 6 Write power consumption at various supply voltages

stack transistors at pull-down network. The 6 T SRAM cell has the largest value of leakage power consumption because of higher width of pull-down transistors.

3.3 Read/write Delay

In low-voltage memory circuits design, read/write delay is a very prominent parameter. The write delay is defined as the duration between 50% of WWL activation and flipping the cell data at 0.1 of Vdd. Figure 8 illustrates the write access time of

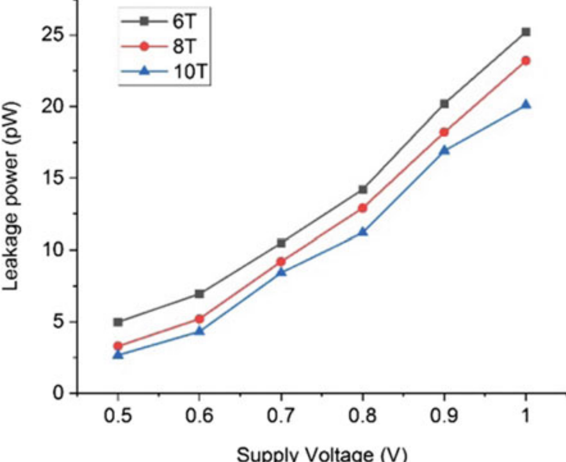

Fig. 7 Leakage power consumption at different supply voltages

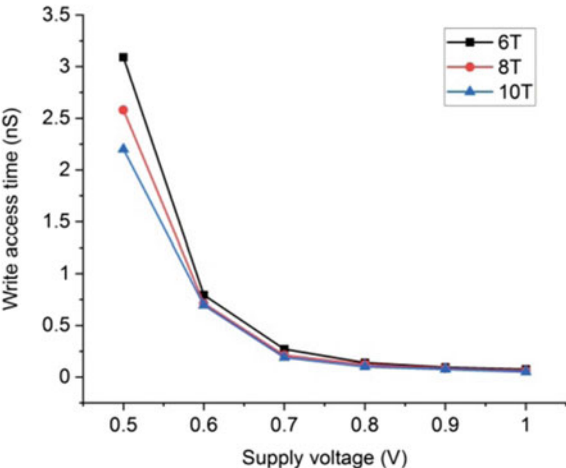

Fig. 8 Write delay at different supply voltages

reference cells. The minimum value of write delay has been observed in 10 T SRAM cell in comparison with conventional 6 T and 8 T SRAM cells at 0.5 V.

Further, in 10 T SRAM cell, write delay is improved by 1.20 × and 1.40 × in comparison with Con.6 T and 8 T SRAM cells at 0.5 V. This happens due to loop cutting technique which disconnects the path from supply voltage to ground. Read delay of the reference SRAM cells is displayed in Fig. 9. It is worth noticeable that read delay is increased by 1.31 × and 1.64 × in 10 T cell as of Con.6 T and 8 T SRAM cells at 0.5 V. It happens due to read decoupled structure which takes higher time to discharge the bit-line capacitance [14, 17].

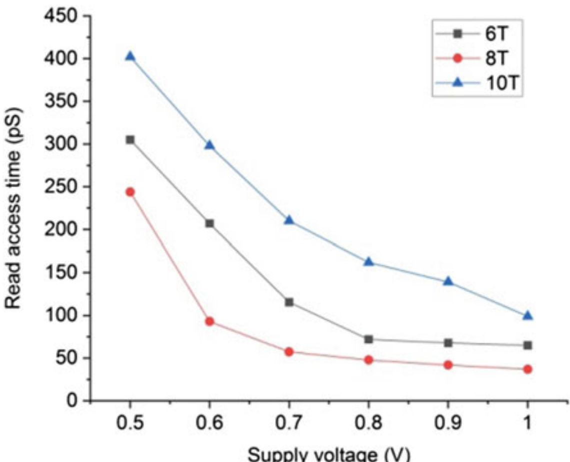

Fig. 9 Read delay at supply voltages

4 Conclusion

This paper presents a 10 T SRAM cell which works in single-ended read and differential write mode. The novel 10 T and considered cells are simulated at 45-nm technology node in cadence virtuoso tool. A commandable increase in stability of 10 T SRAM cell is noticed as of 6 T SRAM cell. The write stability of the cell is upswinged by loop cutting transistors. Additionally, the commandable reduction in power dissipation has been noticed which makes 10 T SRAM cell more suitable for low power application.

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Energy-Efficient Hardware Implementation of K-means Clustering Algorithm

Sourav Nath, Swagata Devi, Merin Loukrakpam, Koushik Guha, and Krishna Lal Baishnab

Abstract Clustering analysis is considered as one of the most vital analytical techniques for unsupervised machine learning and data mining. The algorithm technique influences the clustering results directly. Clustering has been a widely explored in various application domains such as neural networks, artificial intelligence (AI), statistics, image and video segmentation, and many more. This paper discusses the standard K-means clustering algorithm with its three respective modules: random initialization, training and testing. The work discussed in this paper implements the clustering algorithm in MATLAB tool and then verifies the theoretical results. It also modifies some parts of the algorithm to improve the time and space complexity. Further the algorithm is realized in Verilog and verified in Xilinx ISE tool.

Keywords K-means · Clustering · FPGA · Machine learning

1 Introduction

In the research area of unsupervised machine learning and data mining, a fundamental method known as "clustering" is well accepted and is used to group data objects into different classes or clusters. Hence, it plays an important role in data analysis. K-means is considered as the most popular technique among the various clustering algorithms due to its simplicity and efficiency. The other model-based clustering methods are density-based clustering, model-based clustering and fuzzy clustering. Filho et al. [1] have put forward a co-design technique involving software as well as hardware, which implements K-means clustering method. This algorithm is used for collecting and processing information from the electromagnetic spectrum. This process is an image clustering technique involving hyperspectral images. In this

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method, the spectrum for every pixel of the image is extracted to recover the objects, spot the materials, or to perceive the processes. A work proposed by Maruyama et al. [2] shows real-time K-means clustering for coloured impressions through the implementation of FPGA, and simultaneously a filtering algorithm is also employed in its hardware. Another work proposed by Estlick et al. [3] exhibits algorithmic conversion on field-programmable gate-array (FPGA) hardware using K-means method. The trade-off which takes place while mapping of K-means algorithm to the hardware has been analysed. In the work of Alves et al. [11], parallel processing capability is explored by using fully parallel programming, and no sequential blocks are used in this work; for this, it can handle in parallel large data in the era of Big Data. The key purpose of this work is focused on the hardware implementation of K-means clustering algorithm and its verification. The software execution part of this method is performed using MATLAB tool, and the hardware is realized using Verilog. In this algorithm, the whole process is divided into three parts: random initialization, training and testing parts. The functions of the individual parts are described later in detail.

2 K-Means Clustering Algorithm

K-means is described as an unsupervised clustering algorithm which groups a set of unlabelled data into K clusters based on their similarities. It represents clusters by their means and assigns a set of data points to their nearest clusters. Hence, the outcome of the K-means algorithm is K cluster centroids, with each data point assigned to a corresponding cluster [4–10].

In the simplest form of the traditional K-means, a set of n number of data points (D), the number of desired clusters (K) and threshold Th are considered as inputs, for which K clusters outputs are generated. The algorithm which is followed is listed below:

1. Select K points as initial centroids.
2. Form K clusters by assigning each data point to its nearest centroid.
3. Re-compute the centroid for each cluster.
4. Repeat the step 3 until the centroids do not change beyond Th (threshold value).

Usually, K-means algorithms are executed in general purpose processing units such as CPUs or GPUs, but these processors are inefficient and not optimized to compute such algorithms. They consume immensely large area and consume high energy for its operation, which makes them unsuitable for battery operated devices. Hence, there arises a need for a specific hardware to implement K-means algorithm so as to improve its energy efficiency keeping in account the trade-offs among area, power and delay. This algorithm is widely used in battery operated devices like drones to cluster a wide area such as forest, in pattern detectors for brain disease detection through MR image segmentation.

3 Random Initialization

The function random_initialization() takes all the data points as an input and gives K numbers of initial centroids.

3.1 Working Principle

In random initialization process, we have to assign K numbers of initial centroids. To do that, the first centroid is assigned to the value of the first data point. Clearly, the first data point must fall under a cluster and immediately assigning that without calling any function or operation saves the computational time. And the process will begin from the remaining data points and calculated from the first centroid. Then if it is greater than the threshold value, then it can be said that it is a new centroid and it will be assigned to the next centroid; in this iteration, 2nd centroid would be assigned and then it will check for next data. Else centroid assignment will not be done, and again it will check for next random data. Generally, if there are k numbers of centroid assigned and the rth data come, the algorithm checks the Manhattan distance from the data and all k centroids. If all the Manhattan distance is greater than the threshold distance, then it can be said that it is a new centroid. Again, when number of assigned centroids k will be equal to the total number of cluster K, that means the function successfully found K centroids and there is no need to run further. So, this will complete the random initialization and give output of K initial centroids and all the data points excluding the initial centroids.

4 Training

The output from the random initialization () function is directly fed into the training () function, which generates the final centroid as its result.

4.1 Working Principle

The output from random initialization function is the input or the initial centroids for the training module. Thus, the starting point of the training part is the initial centroids. A data point is fetched from the final data points, and then, the Manhattan distance is calculated between the data points and the initial centroids. Now for the minimum Manhattan distance the associated centroid is updated using Eq. (1). This is repeated for each dimension, for example twice for 2 dimensions.

$$C_{\text{new}} = C_{\text{old}} + \frac{d - C_{\text{old}}}{t} \tag{1}$$

where t is the number of iteration, C_{new} is the updated centroid and will be used in the next iteration, d is the data point and C_{old} is the previous centroid. Therefore, iterating over all the data points will provide the final value of the centroid. In this algorithm, after a few iterations if the centroid does not move too much, then the centroid becomes a final centroid. When all the centroids have converged, then the whole function will end the computing process and return the final centroids. The complete process saves the computation time. The convergence checking is done using Eq. (2):

$$\frac{C_{\text{old}} - C_{\text{new}}}{C_{\text{old}}} \leq \text{threshold percentage} \tag{2}$$

5 Testing

Once when the final centroid value from the training part is generated, then whenever a random data comes in, it can be successfully plotted and clustered.

5.1 Working Principle

Firstly, the Manhattan distance of the new data points and the final centroids will be calculated. Secondly, the centroid having the minimum distance would be the associated centroid. Then it assigns the data point to that cluster.

6 Results and Analysis

6.1 Random Initialization

In the designed MATLAB program for this work, three hundred data points have been randomly generated and have three distinct clusters. The random initialization function creates three centroids. The three hundred data points, prior to random initialization, are illustrated in Fig. 1. After running the function, two hundred ninety-seven data points plus three 3 centroids are generated which is shown in Fig. 2. The centroids are marked in star as depicted in the plots of Fig. 2. It has been observed that the random data points are selected from each cluster and owing to the use of random

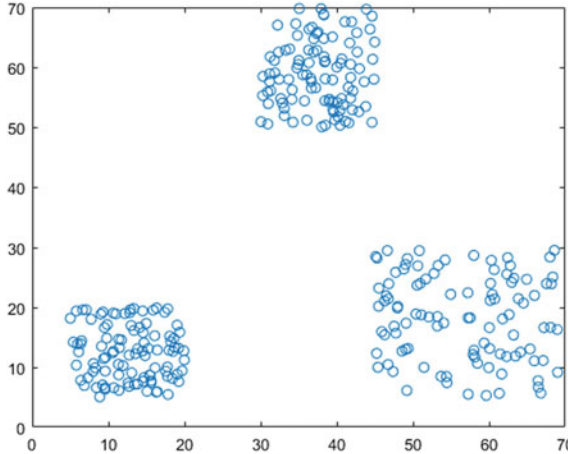

Fig. 1 Data points before random initialization

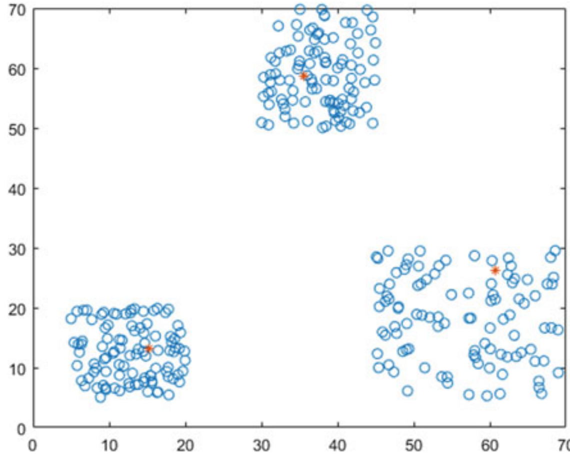

Fig. 2 Data points and initial centroids after random initialization

numbers; this algorithm generally takes only four to seven iterations to completely find the initial centroids.

6.2 Training

The output data from random initialization function are fed to the training function, and its output plot is shown in Fig. 3.

As depicted in Fig. 3, it has been observed that the final centroids are different from the initial centroids, and they have moved to the centre approximately. The accuracy of the final centroids can be increased by decreasing the threshold percentage;

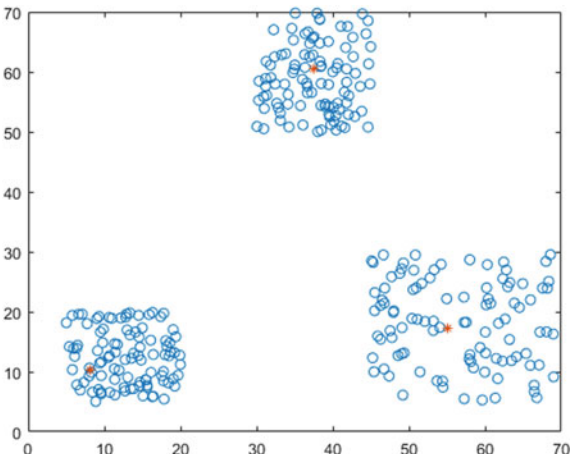

Fig. 3 Result after training function

however, there exists a trade-off between accuracy and computation time. The increased computation time again reflects as increased power that is generally avoided. Therefore, it has been observed that in this algorithm for three hundred data points it takes 202 iterations to converge at 90% accuracy and 0.1 threshold percentage. On the other hand, for 100% accuracy, the total the number of iterations required is equal to the total number of final data points i.e. two hundred and ninety-seven, which exhibits an overall improvement of 31.96%.

6.3 Testing

In the testing part, verification process is executed for the final centroids by introducing a new data point. The resultant output is shown in the plot Fig. 4, where the new data are marked as' + '.

7 Hardware Implementation

In this part, the algorithm is realized in three modules; first, the random initialization module is realized, and after that, the training/testing module is being realized.

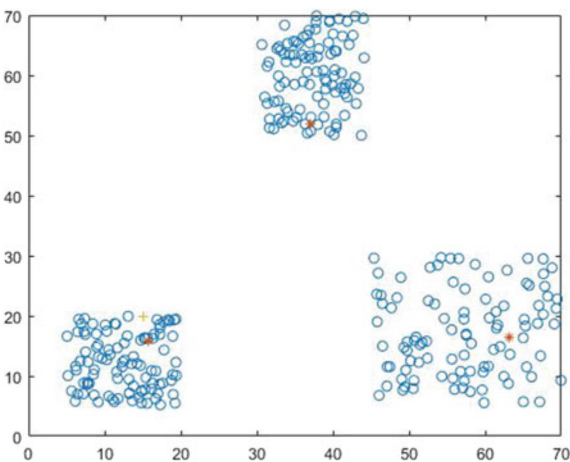

Fig. 4 The result of the testing function

7.1 Random Initialization

The random initialization module will be functionally same as described in the software implementation part. The whole module can be realized into sub-modules. The required sub-modules are Manhattan distance calculator, comparator, ICG, LFSR, centroid assignment module. The data points are stored in a *data.hex* file. This module will fetch from the data file randomly and checks if the new data can be a centroid. The working principle of each modules is described below. Here all the data points are 32 bits consisting two dimensions, the x-coordinate and y-coordinate. So 16 bits are associated with each value. This value also consists of two 8 bits which denotes the decimal and fractional part using fixed point notation.

7.1.1 Manhattan Distance Calculator

This module will take input the random data point from the *data.hex* file, and it gives the 3 Manhattan distance as output. The process is described below.

- At first, the x-coordinate and y-coordinate parts are separated from all the inputs.
- The formula for Manhattan distance calculation is:

$$\text{MD} = |x_1 + x_2| + |y_1 + y_2| \tag{3}$$

Now in this manner, the Manhattan distances from the data points and all the initially assigned centroids are calculated and this module will return those values.

7.1.2 Comparator

In this module, the input is the previously calculated Manhattan distance and the value of the counter. So that the output of the convergence module *conv_out* will give whether the data point is new centroid or not. According to the value of counter, this module will check which Manhattan distance is greater than the threshold value. If all the required MD(s) are greater than the threshold, then it will give output *comp_out* = 1 so that it will inform that the data point is a new centroid. For example, if the counter value is 2'b10, then this comparator module will take account of the MD between the data point and the first two assigned centroids.

7.1.3 ICG

This module is for clock gating. We need to reach the *comp_out* signal at the same time with the clock. Sometimes if the *comp_out* reaches with a delay, then there will be a glitch in the circuit and it can malfunction or consume energy when it does not need to. So clock gating ensures us that two signal reaches the next module with no delay to each other. It uses a D latch to hold the previous value of *comp_out*, and it will get the new value of that at the next clock. It removes the glitch mentioned earlier.

7.1.4 LFSR

In the random initialization module, a crucial operation is to generate a random number. Here we are using an LFSR as a pseudorandom number generator. The output of the LFSR will be used to fetch the data point with associated memory address.

7.1.5 Centroid Assignment

If the output of the comparator *comp_out* is 1, then we need to set the newly found centroid i.e. the associated data point to the register to store as initial centroids.

7.2 Training/Testing

In the software implementation part, the training and testing parts were done separately but here both can be implemented together. This module uses Manhattan distance calculator which is previously designed along with two new module, centroid update module and convergence checker module. Here the data points are fetched as

same manner in the random initialization module. The formats of all data are also same as the random initialization.

7.2.1 Working Principle

- At first, the counter *n* is initialized to 4’b0001.
- Then the first address is fetched and MD is calculated with it and the initial centroids.
- The centroid update will check the minimum MD, and the centroid associated with minimum distance will be updated and other centroids will not be affected.
- Then the convergence checker module will check the convergence of any centroid. If any centroid is converged, then it will store its value in the output register.
- If all the centroids are converged or there are no more data point, then the HALT will be assigned as HIGH i.e. the circuit will stop.
- The final centroids will be stored in the registers.

8 Results and Discussion

As discussed above about under the flow of hardware implementation, the Verilog code for each and every required module is written and simulated in the Xilinx ISE simulator. The RTL view of both random initialization and training/testing module along with their simulated output is shown below. The data are given in the testbench written in Verilog for testing both the module separately, and the output is verified from the waveform obtained after simulation (Figs. 5, 6, 7 and 8).

9 Conclusion

In this work, the K-means clustering algorithm is successfully implemented in MATLAB tool. The designed program can successfully accept random data from the input data point and initialize the cluster centroids, and then it can compute the final centroid. In the training part, it can successfully test the convergence accordingly. It saves computing time for the algorithm and makes it efficient, but it does not give fully perfect cluster centroid and instead returns a very close value saving a good amount of energy. The hardware implementation is done but its effects on power, area, frequency and delay of the circuit, its implementation for different dimensions, and also a part can be added in future to determine the number of clusters so that it would be more versatile. As machine learning currently is an emerging domain, and there is a lot of ongoing work in the field of unsupervised clustering, hence this work can be extended in many different prospects.

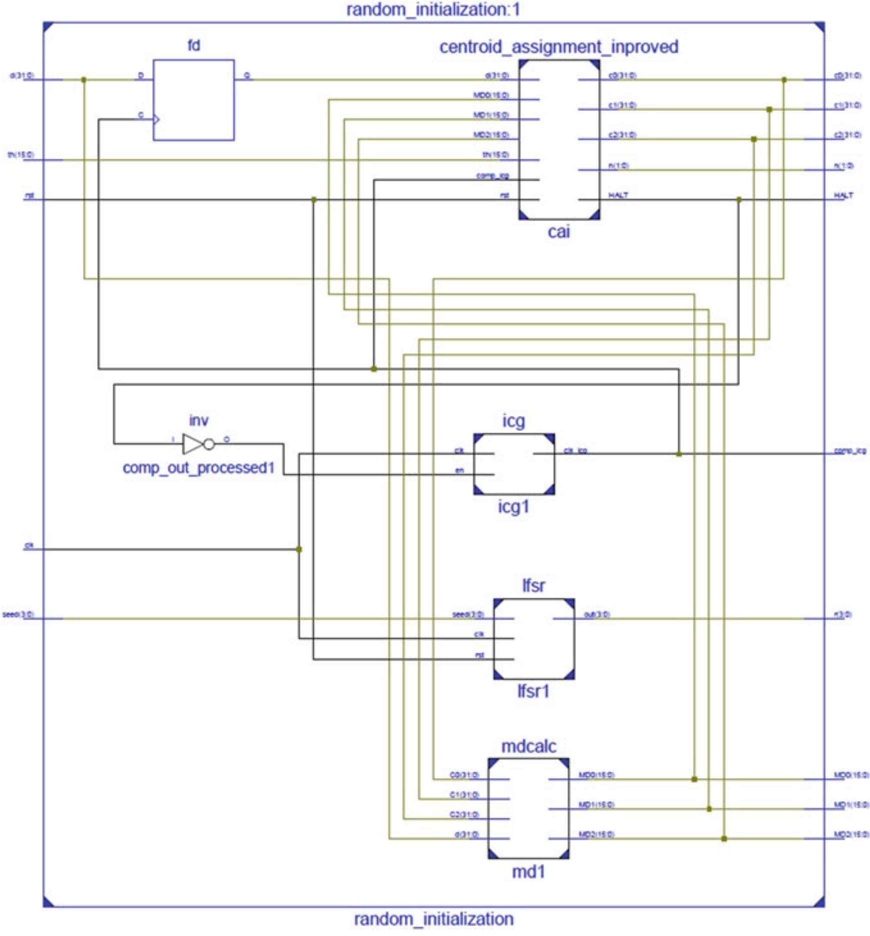

Fig. 5 RTL view of the random initialization module

Fig. 6 Output waveform of the random initialization module

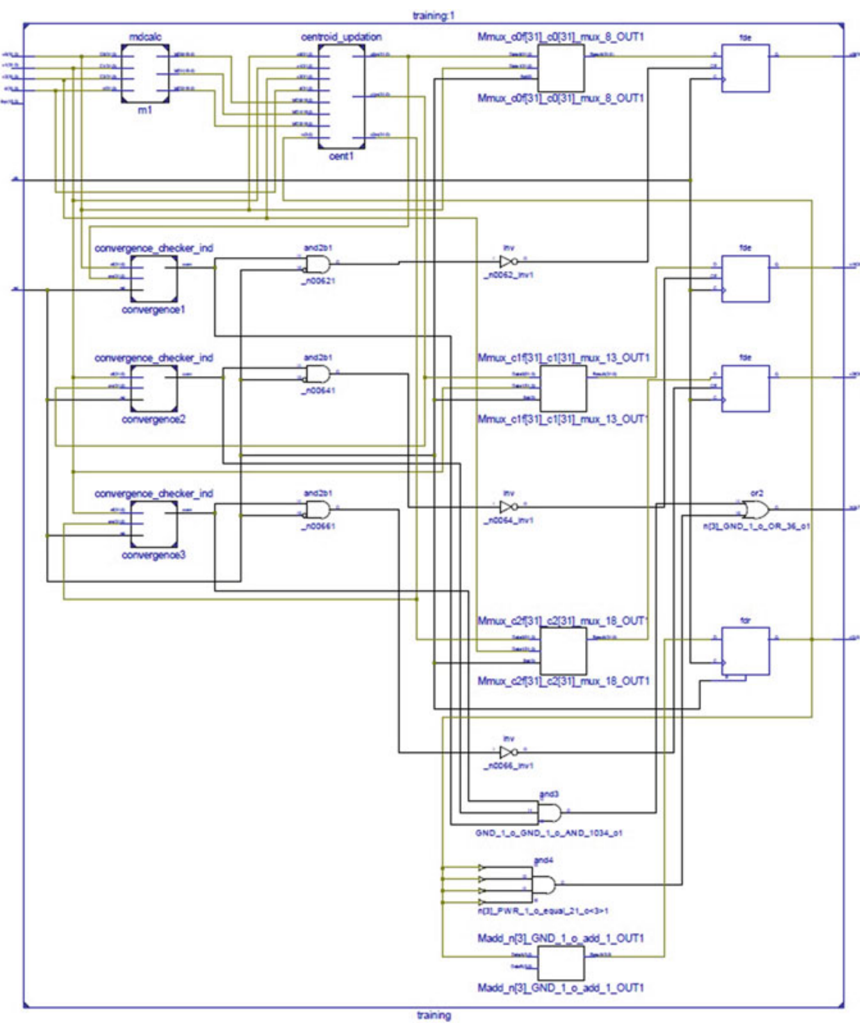

Fig. 7 RTL view of training/testing module

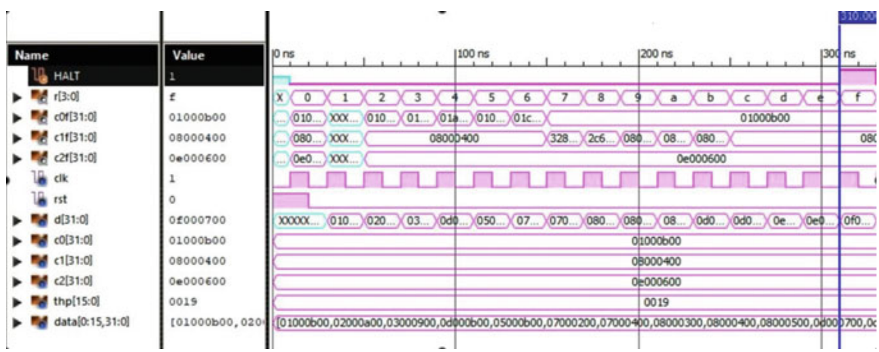

Fig. 8 Output waveform of training/testing module

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Performance Analysis of HIT-CZTS Tandem Solar Cell Towards Minimizing Current Losses

Sivathanu Vallisree and Trupti Ranjan Lenka

Abstract In this work, we report on Heterojunction with intrinsic thin layer-Cu_2ZnSnS_4 (HIT-CZTS) tandem solar cell modelled using Silvaco TCAD simulator. Initially the HIT and the CZTS solar cells are modelled and validated. Then the tandem structure is designed using HIT as bottom module and CZTS as top module and various loss mechanisms are investigated. From the simulation study, it is revealed that current mismatch among the top and bottom modules has contributed to low short-circuit current density and hence the efficiency of the tandem device. The thickness of CZTS absorber is varied as an attempt to equalize the absorption in top in bottom modules and the performance optimization of the tandem structure is carried out for different tunnelling layers. The tandem structure produces maximum efficiency of 20.93% with Titanium Nitride (TiN) as tunnelling material whereas the maximum efficiency exceeds more than 22% for Si-CZTS tandem solar cell with ITO as tunnelling material. The efficiency can be enhanced further by reducing the overlapping portion of the EQE graph in the tandem structure.

Keywords Device modeling · CZTS · HIT · Tandem Solar Cell

1 Introduction

Nowadays, multi-junction solar cells are gaining attractive attention and the current generation is looking at combining Silicon with thin film technologies for efficiency enhancement as it exceeds the Shockley-Queisser limit. Several researchers have reported multi-junction solar cells with two, three and four junctions for improving the overall spectrum absorption and increasing the open-circuit voltage. Monolithic perovskite/silicon tandem solar cell has been optimized in [1]. Copper Zinc Tin

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Sulfide (CZTS) based tandem solar cells have been designed and the effect of different interconnect layers are studied in [2]. The requirements for designing the top cells with various absorber materials such as $CuInS_2$, CZTS, Sb_2S_3, hydrogenated amorphous silicon, and crystalline Silicon material as bottom cell absorber has been explored by Thomas P. White [3]. The band gap of the top cell absorber material should be in the range of 1.6 to 1.9 eV [4] and the bottom cell should be in the range of 1.0–1.2 eV for effective light absorption in the dual junction tandem solar cell. F.M.T. Enam et al. has studied the design prospects of CdTe/Si tandem solar cells using AMPS-1D simulation software [5]. The carrier transport mechanisms of Si/CZTS solar cell has been investigated in [6]. Perovskite/CZTS tandem solar cell was designed using multilayer spectrum filter for enhancing the performance of the device [7]. The nonlocal behavior of tunneling junctions in multi-junction solar cells have been studied by Yiming Liu et al. [8]. Different light management techniques have been studied by A.J. Blanker for 2 T hybrid tandem solar cells [9]. Modeling of these tandem devices would elucidate the device physics and the factors which have a major influence on the device performance. In the present work, Heterojunction with intrinsic thin layer-Cu_2ZnSnS_4 (HIT-CZTS) tandem structure was designed and the major factors influencing the efficiency are identified and mitigated to the possible extent by analyzing the EQE graphs and Generation\Recombination profile of the top and bottom modules. The methodology used for designing the HIT-CZTS tandem structure is discussed in Sect. 2 and the results and discussion are detailed in Sect. 3 with the conclusion in Sect. 4.

2 Simulation Methodology

Initially, HIT solar cell and CZTS solar cell models has been developed using the Silvaco ATLAS simulator [10] as shown in Fig. 1. The material parameters used for the model are listed elaborately in Table 1 which are obtained from literature [11–14]. The optical constants such as refractive index and extinction coefficient covering the visible portion for different materials [15, 16] are given as input to the simulator. The details of CZTS solar cell model has been reported in [17]. After analysing the performance of the device, HIT-CZTS tandem solar cell device is modelled and optimized for improving the overall spectrum absorption aiming at efficiency enhancement of the device. Indium Tin Oxide (ITO) is initially identified as the suitable tunnel layer [18] as it can act as transparent conducting oxide layer which passes the infra-red light to the bottom cell and provides electrical connectivity between the top and bottom modules. The potential at each and every mesh point is evaluated by self consistently solving the Poisson's equation and carrier continuity equations [6] in (1) (2) and (3) as follows.

$$\mathrm{div}(\varepsilon \nabla \psi) = q\left(n - p - N_D^+ + N_A^-\right) - Q_T \tag{1}$$

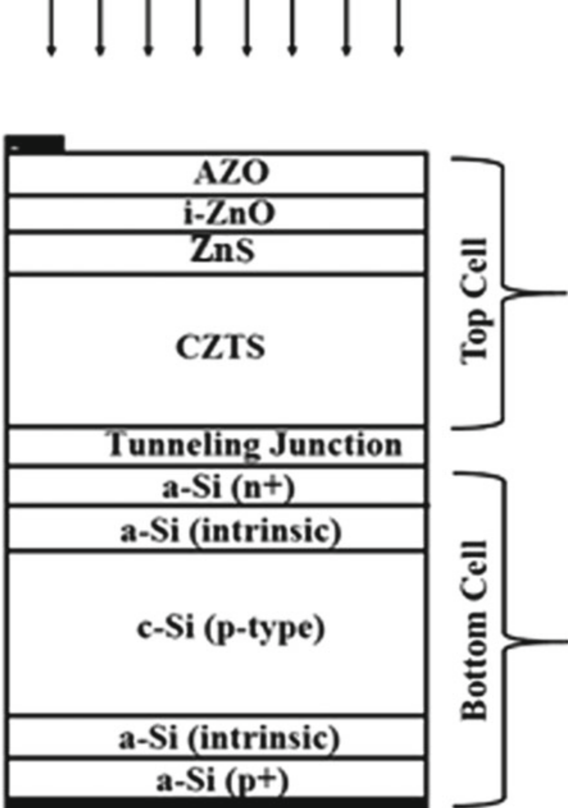

Fig. 1 HIT-CZTS tandem solar cell structure

$$\frac{\partial n}{\partial t} = \frac{1}{q}\mathrm{div}\overrightarrow{J_n} + G_n - R_n \tag{2}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\mathrm{div}\overrightarrow{J_p} + G_p - R_p \tag{3}$$

The appropriate models are incorporated based on the physical mechanisms which occur in the device. The SRH recombination mechanism is included for recombination which occurs due to the presence of traps or defects and radiative recombination for direct band gap materials. Appropriate material based models are also incorporated in the developed Si-CZTS tandem structure. The thermionic emission and tunnelling mechanisms are considered along with the drift-diffusion mechanism of carrier transport for the abrupt heterojunctions. The device is illuminated by applying the standardized Air Mass 1.5 G spectrum having intensity of 100 mW cm^{-2}.

Transfer Matrix method is applied to obtain the optical generation rate. Light is considered as the electromagnetic wave and the transfer matrix method relates

Table 1 Material parameters used for the modeling of tandem solar cell

Parameters	CZTS	ZnS	i-ZnO	AZO	Si	a-Si
Eg (eV)	1.45	3.58	3.37	3.37	1.12	1.7
Permittivity	7	9	9	9	11.8	11.8
Electron affinity (eV)	4.16	3.8	4.0	4.0	4.05	3.9
Conduction band DOS	1.91×10^{18}	6.35×10^{18}	2.2×10^{18}	2.2×10^{18}	2.8×10^{19}	10^{21}
Valence band DOS	1.5×10^{19}	6.03×10^{19}	1.8×10^{19}	1.8×10^{19}	1.04×10^{19}	10^{21}
Donor concentration (cm^{-3})	–	1.1×10^{17}	1.5×10^{17}	1×10^{18}	–	10^{20}
Acceptor concentration (cm^{-3})	1×10^{16}	–	–	–	4.31×10^{15}	10^{20}
Electron mobility (cm^2/Vs)	100	230	100	50	990	5
Hole mobility (cm^2/Vs)	25	40	20	5	269	1
Thickness (μm)	0.1	0.1	0.08	0.3	180	0.005

the electric field amplitudes of transmitted and reflected wave to the incident wave amplitude. The electric and magnetic fields are obtained using (4, 5) and the photogeneration rate is calculated using (6) as follows [10].

$$E(Z) = E(z_j)\cos(\varphi) - iH(z_j)\sin(\varphi)/Y(j) \tag{4}$$

$$H(Z) = H(z_i)\cos(\varphi) - iE(z_i)\sin(\varphi)/Y(i) \tag{5}$$

$$G(z) = \frac{\lambda}{hc}\alpha\frac{|E(z)|^2}{2\eta} \tag{6}$$

3 Results and Discussions

The efficiency of initial HIT solar cell model is 17.45% as shown in Table 2. The parameters having major influence on the solar cell performance such as short-circuit

Table 2 Comparison of solar cell parameters of tandem structure with the HIT solar cell

Model	J_{sc} (mA cm^{-2})	V_{oc} (V)	FF (%)	η (%)
HIT Solar cell	29.93	0.728	80.13	17.45
HIT-CZTS solar cell	16.40	1.75	76.87	22.05

current density (J_{sc}), open-circuit voltage (V_{oc}), fill factor (FF) and efficiency (η) are obtained from the simulation for the tandem structure. The efficiency of the tandem structure was initially 7.76%. The open-circuit voltage is almost the summation of the V_{oc} of the top module and bottom module as expected and the fill factor also does not contribute to the low efficiency of the device. The low efficiency of the tandem structure is owing to the low value of J_{sc}. As a next step, External Quantum Efficiency (EQE) analysis is carried out for the tandem structure for analysing the cause of low efficiency.

3.1 EQE Analysis of HIT-CZTS Tandem Solar Cell

The EQE graphs were analysed for the top and bottom modules as shown in Fig. 2. From the EQE graphs, it is revealed that the top cell absorbs most of the photons leaving behind less number of photons for the bottom cell as clearly evident from Fig. 2. Hence the thickness of top cell absorber material is tuned in order to obtain current matching between top and bottom modules.

The solar cell parameters for varying CZTS absorber thickness from 600 to 100 nm is shown in Fig. 3. J_{sc} shows increasing trend on reducing the thickness of CZTS absorber as more amount of photons are transferred to the bottom cell for obtaining current matching scenario. There is no major change in the V_{oc} and it is almost the sum of open circuit voltage of top and bottom modules. The fill factor decreases

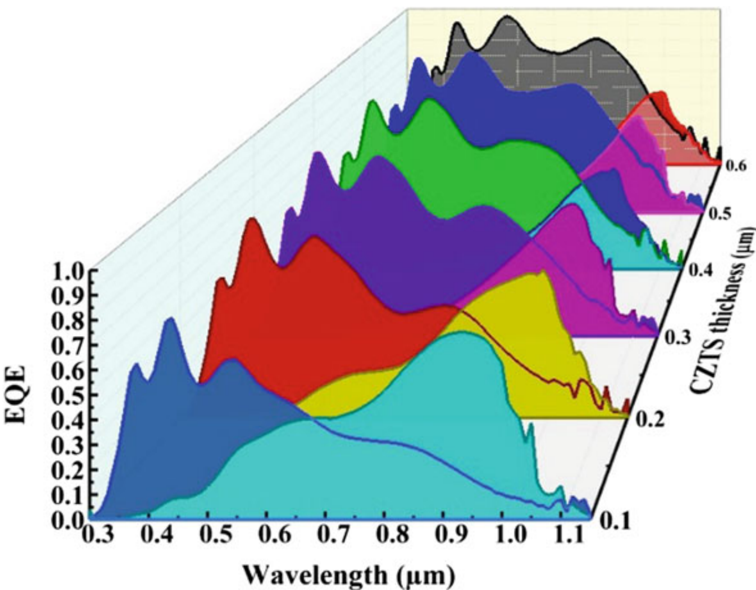

Fig. 2 EQE graphs of top and modules in HIT-CZTS tandem structure for varying CZTS thickness

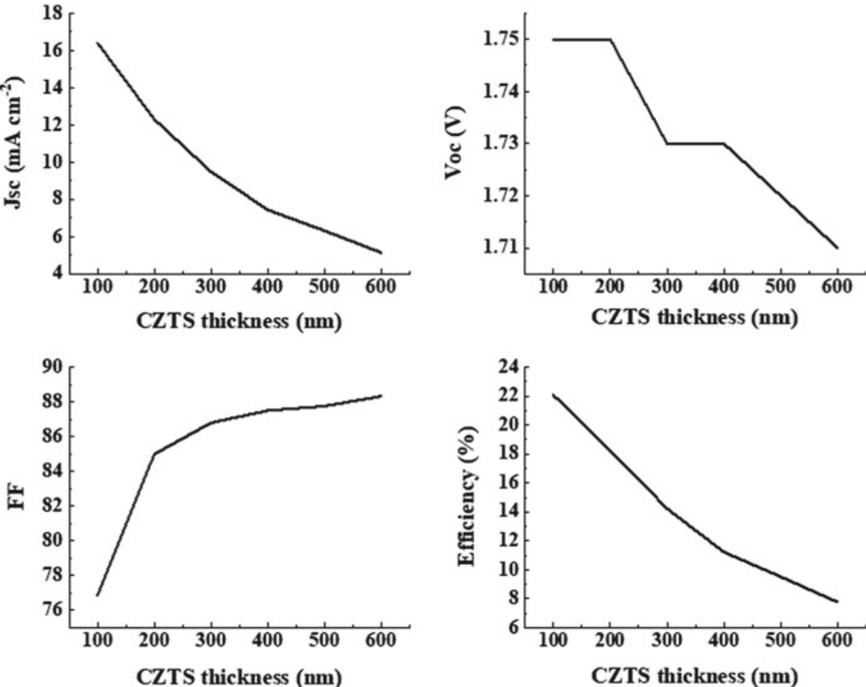

Fig. 3 Solar cell parameters of HIT-CZTS tandem structure for varying CZTS thickness

because of the increase in the series resistance of the device. The efficiency increases with the decrease in CZTS absorber thickness owing to the increase in J_{sc}. The solar cell parameters for the HIT solar cell and the HIT-CZTS tandem structure are listed in Table 2. The V_{oc} shows a high boost in value and J_{sc} shows a reduction in value. The short circuit current density can be improved further by examining the photon absorption profile and choosing proper material combinations in order to minimize the overlap portion of the spectrum.

3.2 Photo Generation and Recombination Profile

The photo generation profile for varying thickness of CZTS absorber material is extracted as shown in Fig. 4a. With the decrease in the CZTS thickness, the overall photogeneration rate in the top module decreases while the photogeneration rate in the Silicon region near the junction increases as more amount of photons reaches on to the bottom cell which is clearly evident from Fig. 4a and inset of Fig. 4a. The recombination rate has increased drastically for 100 nm thickness owing to the increase in carrier generation rate and more number of carriers having finite diffusion length are available for recombination.

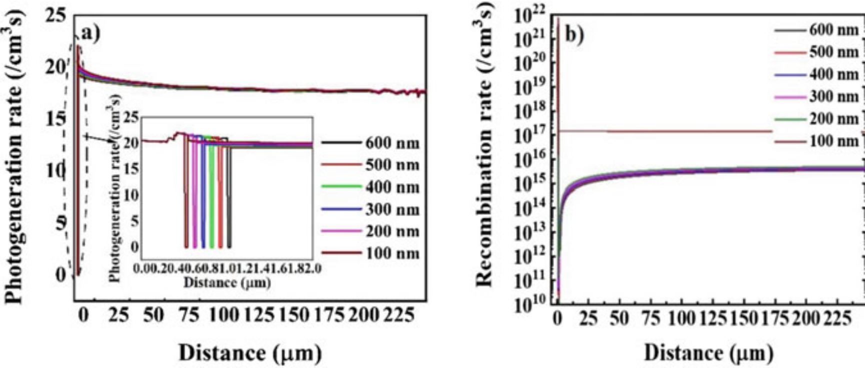

Fig. 4 **a** Photogeneration rate of the tandem solar cell with the inset figure showing the photogeneration rate in the CZTS module. **b** Recombination rate for the Silicon-CZTS tandem solar cell.

3.3 Current Densities in the Tandem Solar Cell

The electron, hole and total current densities are extracted for the tandem solar cell model which are represented by dashed, dotted and solid lines respectively for varying CZTS thickness of 600–100 nm in Fig. 5. The current is controlled by lower of the two current densities of top and bottom modules and with the decrease in CZTS thickness from 600 to 100 nm, total current density shows an increase in trend as it progresses towards obtaining current matching among the top and bottom modules in the tandem cell. From the electron hole current density (EHCD) graph, it is revealed that the current losses are minimized for CZTS thickness of 100 nm.

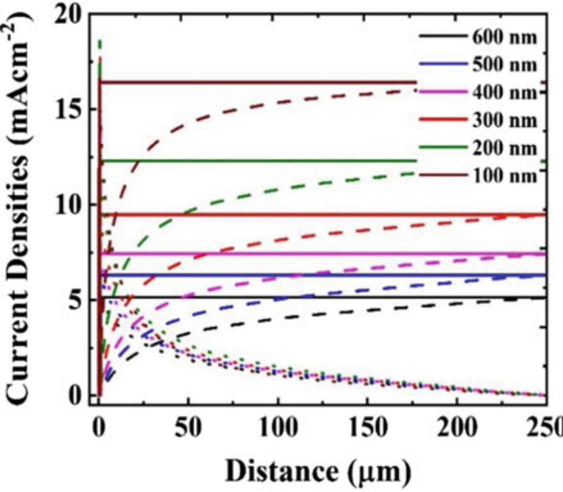

Fig. 5 Electron, hole and total current densities of Si-CZTS tandem solar cell plotted with dashed, dotted and solid lines respectively for varying thickness of CZTS absorber material

Hence the optimum thickness of CZTS material for the tandem solar cell model is considered to be 100 nm.

3.4 Nitride Based Interfacial Layers

According to the literature, Nitride based interfacial layers can be utilized as tunnel layers in Si-CZTS monolithic tandem solar cells to protect the Si bottom cell from high-temperature reactive processes [19]. Hence the ITO tunnel layer is replaced by Titanium Nitride (TiN) layer in the above model and the performance is investigated. The absorption data for TiN material is obtained from [20]. The CZTS-Si tandem solar cell yielded low efficiency of 10.52% for TiN tunnel layer thickness of 25 nm. With the reduction in thickness of TiN material from 25 to 5 nm [19], more amount of photons is transferred to the bottom cell thereby minimizing the current losses. Table 3 lists the comparison of solar cell parameters of CZTS based tandem solar cell modelled using different tunnelling layers with previously reported literatures. CZTS-Silicon tandem solar cell with ITO tunnelling layer (25 nm) provides better performance than its counterpart TiN tunnelling layer of 5 nm thickness. Hence ITO is suggested to be a more suitable material when compared to TiN tunnelling layer. This study reveals that depending on the fabrication processes and the operating temperatures involved, appropriate tunnelling material or p-n tunnelling junction can be selected for the monolithic tandem solar cell.

Table 3 Performance comparison of CZTS based tandem solar cell with previously reported literatures

CZTS based tandem solar cells	Year	J_{sc} (m A cm^{-2})	V_{oc} (V)	FF (%)	η (%)
CZTS-Si tandem solar cell with ITO tunnel layer (25 nm)	This work	16.40	1.75	76.87	22.05
CZTS-Si tandem solar with TiN tunnel layer (25 nm)	This work	6.998	1.72	87.35	10.52
CZTS-Si tandem solar with TiN tunnel layer (15 nm)	This work	10.61	1.73	85.19	15.68
CZTS-Si tandem solar with TiN tunnel layer (5 nm)	This work	15.3	1.744	78.45	20.93
CZTS/CZTSe tandem solar cell	2020 [2]	23	1.72	72.69	28.86
CZTS/CZTSe tandem solar cell	2017 [21]	19.59	1.492	73.4	21.44
CZTGS/CZTS tandem thin film solar cell	2019 [22]	18.53	1.35	62.17	17.51

4 Conclusion

HIT-CZTS 2 T tandem structure was modeled using Silvaco ATLAS simulator by inputting the suitable material parameters and optical constants. Upon analyzing the EQE graphs, Generation/Recombination profile of top and bottom modules, current mismatch was identified as the major cause contributing to low J_{sc} as the current is limited by the lower of the top and bottom module currents. The reduced thickness of CZTS absorber has favored the performance by attempting to equalize the current generation in the top and bottom modules. The efficiency of Si-CZTS tandem solar cell with ITO tunneling layer (25 nm) has increased from 7.76 to 22.05% after minimizing the current losses. Also, TiN tunnel layer of 5 nm thickness produces maximum efficiency of 20.93%. Hence, depending upon the reactive processes involved, appropriate tunneling material can be chosen for the fabrication of Si-CZTS tandem solar cell. The efficiency can be further improved either by maximizing the overall photon absorption (reducing parasitic absorption) or by developing Si-CZTS four terminal tandem solar cell.

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Triple Linear Congruential Generator-Based Hardware-Efficient Pseudorandom Bit Generation

Gegerin Konsam and Merin Loukrakpam

Abstract Many of the Internet of things applications are employed on power and resource-constrained devices. Pseudorandom bit generator (PRBG) is one of the crucial components to manage privacy and security on these devices. Among popular PRBGs, linear congruential generator (LCG)-based methods have lower hardware complexity. However, bit sequences generated using single LCG fail to meet the randomness and uniform distribution requirements. In this paper, a triple linear congruential generator (Tri-LCG)-based PRBG method is proposed which can generate pseudorandom bits at uniform clock rate. The proposed method passes 14 tests out of the 15 benchmark tests of NIST standard. Two designs of 8 bits and 24 bits of the proposed Tri-LCG are implemented and synthesized in 45 nm CMOS technology. The proposed designs showed up to 19.87, 14.60 and 38.05% reductions in energy, energy–delay product and area–delay–power product when compared with those of state-of-the-art PRBG methods.

Keywords Hardware-efficient · Linear congruential generator (LCG) · Pseudorandom bit generator (PRBG) · VLSI architecture

1 Introduction

Privacy and security are critical concerns in various Internet of things (IoT) applications. Many of these IoT applications are employed on power and resource-constrained devices. There can be privacy issues due to the big data generated from the millions of devices [1, 2]. Moreover, devices with limited resources and heterogeneous technologies have security challenges [3, 4]. One of the crucial components to manage privacy and security in these resource-constrained devices is the pseudorandom bit generator (PRBG). However, a cryptographically secure PRBG for IoT

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applications is difficult to attain since it demands an efficient hardware architecture to produce the required randomness within the energy and area budget of the devices.

The National Institute of Standard and Technology (NIST) benchmark tests are often used to validate the randomness of a PRBG. Linear congruential generator (LCG) and linear feedback shift register (LFSR) are among the widely used lightweight PRBGs because of its low complexity. However, they fail most of the randomness tests due to their linearity [5]. Different PRBGs based on congruent modulo and chaotic map have also been reported in the literature. Blum Blum Shub (BBS) generator has proven to generate unpredictable and cryptographically secure keys in polynomial time [6, 7]. However, it consumes large area due to the requirement of large prime factorization [8, 9]. To address this, a coupled LCG (CLCG) method was proposed in [10, 11] which has low hardware complexity and is more secure than PRBG with single LCG. Katti et al. [12] proposed a dual-CLCG method to improve the randomness of CLCG. However, the dual-CLCG method fails to generate pseudorandom bits at every clock cycle. The dual-CLCG method is modified in [13], wherein a modified dual-CLCG hardware architecture is proposed to generate pseudorandom bit at every clock cycle. Different architectures of modified dual-CLCG have been proposed in [14–16]. Although dual-CLCG and modified dual-CLCG can generate cryptographically secure pseudorandom bits, they require four LCG units which consume high area, especially for large data widths. Therefore, there is a need to develop a hardware efficient PRBG method for IoT applications.

In this paper, a triple linear congruential generator, termed as Tri-LCG, is proposed which uses three LCG units, two comparators and an XOR logic to generate pseudorandom bit. Two designs of the Tri-LCG were implemented with different data widths. Design parameters of the hardware were analyzed in terms of area, power and delay. Energy, energy–delay product and area–power–delay product were also assessed to evaluate the hardware efficiencies of the designs.

The rest of the paper is organized as follows. Section 2 describes the proposed Tri-LCG method in detail. The proposed hardware architecture of Tri-LCG is presented in Sect. 3. Section 4 discusses the NIST test analysis along with the synthesis results of the VLSI implementation. Finally, a brief conclusion is drawn in Sect. 5.

2 Proposed Tri-LCG Method

The proposed Tri-LCG method generates pesudorandom bits by using three linear congruential generators and is mathematically defined as follows:

$$x_{i+1} = a_1 \times x_i + b_1 \bmod 2^n \tag{1}$$

$$y_{i+1} = a_2 \times y_i + b_2 \bmod 2^n \tag{2}$$

$$p_{i+1} = a_3 \times p_i + b_3 \bmod 2^n \tag{3}$$

Here, n is the data width, $a_1, b_1, a_2, b_2, a_3, b_3$ are the constant parameters and x_0, y_0, p_0 are the initial seeds. The conditions to get the maximal period are as follows:

1. b_1, b_2 and b_3 are relatively prime with 2^n.
2. $(a_1 - 1), (a_2 - 1)$ and $(a_3 - 1)$ must be divisible by 4.

Congruential modulo-2 addition is used to obtain the pseudorandom bit sequence as shown in Eq. (4). In the proposed Tri-LCG design, the modulo-2 addition of the outputs from three LCGs has the maximum length period of 2^n since output of each LCG has the maximal period [10].

$$Z_i = B_i + C_i + D_i \bmod 2 = B_i \oplus C_i \oplus D_i \tag{4}$$

where

$$B_i = \begin{cases} 1, & x_{i+1} > y_{i+1}; \\ 0, & \text{otherwise.} \end{cases} \tag{5}$$

$$C_i = \begin{cases} 1, & p_{i+1} > x_{i+1}; \\ 0, & \text{otherwise.} \end{cases} \tag{6}$$

$$D_i = \begin{cases} 1, & y_{i+1} > p_{i+1}; \\ 0, & \text{otherwise.} \end{cases} \tag{7}$$

Algorithm 1 shows the procedure to generate k pseudorandom bit sequences using Tri-LCG. The number of bits (n) and the desired length of pseudorandom bit sequences (k) are given as input. The constant parameters $a_1, b_1, a_2, b_2, a_3, b_3$ are initialized using the conditions to get the maximal period. The initial seeds x_0, y_0 and p_0 are then set. The output of the three LCGs x_{i+1}, y_{i+1} and p_{i+1} is computed using Eqs. (1)–(3). The output from the three LCGs is then compared using Eqs. (5)–(7) to compute B_i, C_i and D_i. The final random bit (Z_i) is then generated as specified by the mathematical Eq. (4). The process runs for k cycles to generate pseudorandom bit at every clock cycle without missing any value at the output. The generated pseudorandom bit sequence using the proposed Tri-LCG method has the maximum length of 2^n for n-bit operand since the output is generated using modulo-2 addition of three LCGs which have maximum period.

3 Proposed Architecture of Tri-LCG Method

This section discusses the proposed hardware architecture of the Tri-LCG PRBG. Equations (1)–(3) are mapped to three LCG blocks in the proposed architecture as shown in Fig. 1. Consider the LCG equation

Algorithm 1 Pseudocode for the Tri-LCG Algorithm

```
1: Input: n, k.
2: Initialization:
3:     b1, b2, b3: relative primes with 2^n.
4:     (a1 − 1), (a2 − 1), (a3 − 1): divisible by 4.
5:     Initial seeds x0, y0 and p0 < 2^n.
6: Output: Zi
7: for i = 0 to k do
8:     Compute x_{i+1}, y_{i+1} and p_{i+1} using equations (1), (2) and (3);
9:     if (x_{i+1} > y_{i+1}) then
10:        Bi = 1
11:     else
12:        Bi = 0;
13:     end if
14:     if (p_{i+1} > x_{i+1}) then
15:        Ci = 1
16:     else
17:        Ci = 0;
18:     end if
19:     if (y_{i+1} > p_{i+1}) then
20:        Di = 1
21:     else
22:        Di = 0;
23:     end if
24:     Zi = Bi + Ci + Di mod 2;
25: end for
26: return Zi;
```

$$p_{i+1} = a_3 \times p_i + b_3 \bmod 2^n.$$

The multiplication of $a_3 \times p_i$ can be implemented using shifters by considering a_3 to be $(2^r + 1)$ where r is a positive integer such that $1 < r < 2^n$. Hence, the LCG equation can be rewritten as

$$\begin{aligned} p_{i+1} &= (2^r + 1) \times p_i + b_3 \bmod 2^n \\ &= (2^r \times p_i) + p_i + b_3 \bmod 2^n \end{aligned}$$

The $(2^r \times p_i)$ term is implemented using a shifter. The left shifted result is then added with p_i and b_3 to compute p_{i+1}. The *start* signal is used as a MUX select line to load the initial seed value (p_0) at the starting of the computation. The remaining LCG equations are implemented using two more LCG blocks to generate x_{i+1} and y_{i+1}. The comparison Eqs. (5)–(7) are implemented using three comparators to generate B_i, C_i and D_i. A 3-input XOR gate is then used to implement Eq. (4) to generate the bit sequence Z_i.

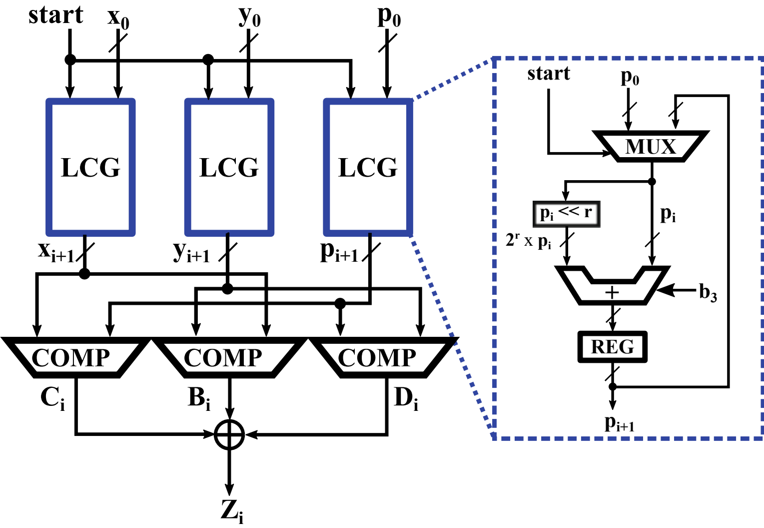

Fig. 1 Proposed architecture of Tri-LCG method

4 Results and Discussion

4.1 NIST Test Analysis of the Proposed Tri-LCG

The randomness of the bit sequence generated from the proposed Tri-LCG was analyzed by studying its statistical properties using the National Institute of Standards and Technology (NIST) statistical test suite *sts-2.1.2* [17]. The proposed Tri-LCG was used to generate $T = 100$ different binary sequences of length 10^6 bits, and the binary sequences were used for the NIST statistical tests. The initial seeds (x_0, y_0, p_0) were selected from a true random source [18], and the parameters $(a_1, b_1) = (129, 32177)$, $(a_2, b_2) = (65, 1533)$ and $(a_3, b_3) = (4097, 571)$ were used to generate all the sequences for the tests. The size of the proposed Tri-LCG is considered as $n = 24$ bits. Table 1 shows the NIST test results of the proposed Tri-LCG. The significance level (α) of 0.01 was considered for the tests. In a particular test, the randomness of the sequence is indicated by the P-value of the test. P-value ≥ 0.01 indicates that the sequence is random with a confidence of 99%. Moreover, the distribution of the sequences is analyzed using the U-value which is computed by performing a goodness-of-fit distribution test on P-values of $T = 100$ sequences. The sequences are considered to be uniformly distributed if U-value ≥ 0.0001. Prop. value in Table 1 the proportion which represents the ratio of the successes to the number of trials. For passing the test, Prop. value ≥ 0.96 and U-value ≥ 0.0001 were considered.

Table 1 NIST statistical test results

S. No.	Test	CLCG		Modified dual-CLCG		Proposed Tri-LCG	
		Prop.	U value	Prop.	U-value	Prop.	U-value
1	Frequency (monobit)	1.00	0.0000	0.98	0.3669	0.99	0.8343
2	Block frequency	0.99	0.3504	1.0	0.8513	0.99	0.0711
3	Cumulative sum (F)	1.00	0.00237	0.98	0.0965	1.00	0.6579
	Cumulative sum (R)	1.00	0.0032	0.99	0.6993	1.00	0.7791
4	Runs	0.88	0.0000	1.0	0.6579	0.99	0.4749
5	Longest run	0.99	0.0251	0.99	0.7981	0.99	0.5141
6	Binary rank	0.98	0.3190	0.99	0.0589	1.00	0.4011
7	Spectral(DFT)	0.00	0.0000	0.98	0.0375	0.06	0.0000
8	NOT($m = 9$)	0.95	0.3041	0.96	0.0456	0.96	0.2622
9	OLT	1.00	0.9834	0.96	0.5544	0.97	0.4749
10	Universal	0.99	0.3190	1.0	0.4011	0.99	0.3504
11	Entropy	1.00	0.7791	0.99	0.0668	0.99	0.4011
12	Rand excursion	0.952	0.6241	0.968	0.2757	0.95	0.1453
13	Rand Ex. Var.	0.964	0.3404	0.968	0.7061	0.96	0.1815
14	Serial	1.00	0.2133	0.99	0.4749	1.00	0.2133
15	Linear complexity	0.99	0.4943	0.98	0.9114	0.98	0.9914

The NIST statistical tests were also run on CLCG and modified dual-CLCG methods for comparison. It can be inspected from Table 1 that the proposed Tri-LCG method and the modified dual-CLCG method successfully pass the non-overlapping template (NOT) test while CLCG method fails the test. The NOT test is considered the most difficult test [12] and consists of 149 subtests to detect occurrences of non-periodic pattern. The CLCG method fails the uniformity check for three tests, viz., 'Frequency,' 'DFT' and 'Runs.' It also fails to achieve the target Prop. value for four tests viz., 'DFT,' 'Runs,' 'NOT' and 'Rand Excursion'. The modified dual-CLCG method passes all the tests. It can be inspected from Table 1 that sequences generated by the proposed Tri-LCG method pass all the NIST tests except the DFT test.

4.2 VLSI Implementation

Two designs of 8 bits and 24 bits of the proposed Tri-LCG method were implemented using Verilog HDL. Synopsys Design Compiler was used to synthesize the proposed designs in 45 nm CMOS technology. Table 2 shows the synthesis results of the proposed Tri-LCG designs. The synthesis results showed that the area, power and delay of the proposed 8-bit Tri-LCG design were 26.16 μm^2, 217.71 mW and 0.74 ns,

Table 2 Synthesis results of different LCG-based PRBGs

Architecture	Design	Area (μm^2)	Power (mW)	Delay (ns)	Energy (pJ)	EDP (pJ $\times$ ns)	ADP ($\times 10^3$) (pJ $\times$ μm^2)	NIST Test
CLCG	8-bit	400.59	145.29	0.52	75.55	39.28	30.26	10/15 Pass
	24-bit	1319.35	456.38	1.29	588.73	759.46	776.75	
Modified dual-CLCG	8-bit	802.78	289.09	0.65	187.91	122.14	150.85	15/15 Pass
	24-bit	2640.31	907.87	1.37	1243.79	1703.99	3,284.01	
Proposed tri-LCG	8-bit	626.16	217.71	0.74	161.10	119.21	100.87	14/15 Pass
	24-bit	2041.28	682.65	1.46	996.67	1455.13	2,034.48	

respectively, while those of the 24-bit Tri-LCG design were 2041.28 μm^2, 682.65 mW and 1.46 ns, respectively. The energy, energy–delay product (EDP) and area–delay–power product (ADP) of the 8-bit (24-bit) Tri-LCG design were 161.10pJ (996.67 pJ), 119.21 pJ $\times$ ns (1455.13 pJ $\times$ ns) and 100.87 pJ $\times$ μm^2 (2,034.48 pJ $\times$ μm^2), respectively.

Table 2 also shows the synthesis results of 8-bit and 24-bit designs of CLCG and modified dual-CLCG. Since CLCG requires only two LCG blocks, its hardware design parameters are better than those of the proposed Tri-LCG design. However, CLCG method fails 5 of the NIST benchmark randomness tests while the proposed Tri-LCG fails only 1 out of the 15 NIST benchmark randomness tests. The proposed 8-bit Tri-LCG design showed reductions of 22% and 24.69% in area and power, respectively, as compared with 8-bit design of the modified dual-CLCG. While the delay of the proposed Tri-LCG increased by 13.85%, the energy, EDP and ADP were 14.26, 2.39 and 33.13% lower than those of the 8-bit modified dual-CLCG. Moreover, the proposed 24-bit Tri-LCG design showed significant reductions of 22.69, 24.81, 19.87, 14.60 and 38.05% in area, power, energy, EDP and ADP when compared with those of the 24-bit modified dual-CLCG design. It can be noted that the reductions in the design parameters are larger for designs with higher data widths. Hence, the hardware efficiency of the proposed method improves as data width increases.

5 Conclusion

In this paper, a hardware-efficient pseudorandom bit generation method, termed as Tri-LCG, is proposed. The proposed PRBG method uses three LCG units, two comparators and a XOR logic to generate pseudorandom bits at uniform clock rate. The pseudorandom bit sequences generated using the proposed method passed 14 out

of the 15 NIST statistical tests. Two designs of 8 bits and 24 bits of the proposed Tri-LCG method were implemented and synthesized in 45 nm CMOS technology. The synthesis results revealed that the proposed Tri-LCG exhibited significant reductions in area, power, energy and energy–delay product when compared with those of modified dual-CLCG. The hardware efficiency of the proposed designs improved with increase in data widths. The area–power–delay product of the proposed 24-bit Tri-LCG design showed 38.05% reduction when compared with that of the 24-bit modified dual-CLCG highlighting the improved hardware efficiency of the proposed PRBG method over the existing PRBG method.

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Flicker Noise Analysis of Non-uniform Body TFET with Dual Material Source (NUTFET-DMS)

Jagritee Talukdar, G. Amarnath, and Kavicharan Mummaneni

Abstract Noise analysis is an important parameter to study the insight of device parameters. At low frequency, mainly flicker noise prevails and effects different performance parameters of a device. This work presents the flicker noise analysis of non-uniform body TFET with dual material source (NUTFET-DMS). The effect of the absence and presence of donor type of interface trap charges at both front and back silicon and gate oxide interface (Si-HfO_2 and Si-SiO_2) has been incorporated. Further, the analysis also includes the effect of temperature variation (200, 300 and 400 K) in different noise defining parameters such as drain current noise power spectral densities (S_{id}) and gate voltage noise power spectral densities (S_{vg}). It has been perceived that the occurance of interface trap charges has a unfavorable behavior on both noise power spectral densities (S_{id} and S_{vg}) mainly at low temperatures. However, when temperature increases, the effect of trap charges becomes negligible, but noise behavior degrades severely.

Keywords TFET · Noise power spectral density · Trap charges · Flicker noise

1 Introduction

To conserve the Moore's law, various creative devices have been discovered by many groups of researchers to deliver better performance as well as lower cost at the same time [1, 2]. Conventional metal oxide semiconductor (CMOS) devices are one of the promising solutions up to a certain limit of gate length when scaling of devices comes into play. The scaling of conventional MOSFET leads to various benefits in terms of compactness enhances cost, operating speed, etc. However, it promoted some negative impact on leakage current, subthreshold swing (SS), various short channel

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effects, etc. So, alternative devices become new interest and various novel devices have been developed with better electrical performance. One of the advanced devices, which enticed many researchers, is the tunneling FET, i.e., TFET. The field effect transistor (FET) encountering interband tunneling, i.e., tunneling of carriers from source to channel is found to be the likely looking entrance to replace the traditional FET with thermionic emission [3, 4]. In the modern era of extremely scaled device, low power, SS, leakage currents, etc., become the major concern [5–7]. The tunnel FET transistor having interband tunneling as the current conduction mechanism becomes the appropriate solution, but drive current is an issue in these types of FET [8, 9]. Therefore, researchers developed different types of TFET modifying the material and structural view of conventional TFET [10]. Some significant TFETs having lower SS, leakage, etc., with considerable ON current are SOI-TFET [11], double gate TFET [12], single (SG-ESTFET) and double gate extended source TFET (DG-ESTFET) [13, 14], high valued dielectric TFET [15], GAA-TFET [16], Group III-V semiconductor material TFETs [17], NUTFET-DMS [18], etc. Apart from fixing the ON current of TFET, when application-oriented real-time scenario comes into play, some second-order analysis becomes necessary. Moreover, to achieve reliable and optimum device characteristics under the presence of low frequency noise is also a serious impediment. Hence, the effect of noise on various performance parameters of devices needs to be analyzed. The innumerable noise in devices is because of the fleeting irregular variations of charge carrier, whereas the scattering and various trapping processes influence the mobility of the charge carriers [19, 20]. Hence, to check the reliability of a device, it is important to observe the performance parameters in the occurrences of trap charges and different noise components in some intolerable situations.

In this study, we have considered the NUTFET-DMS where source is made up of two materials to obtain lower average SS and channel region is non-uniformed to obtain higher ON current, lower OFF current and ambipolar current [18]. A preliminary study of the NUTFET-DMS device has been performed for different electrical parameters. We have performed low frequency-based noise analysis in the presence of interface trap charges (ITC) and absence of ITC under varying temperature conditions. The noise in a device is because of the temporary random fluctuations caused by trap charge, where different scattering mechanisms and different trapping processes hinder the movability of the carrier. The low frequency-based noise mainly consists of flicker noise ($1/f$) and generation-recombination (G-R) noise. Flicker noise is basically the superimposition of G-R noise spectra from different trap charges with various time constants [21]. The following study has been carried out to analyze the behavior of flicker noise of the device. Section 2 explains the description of device structure and simulation environment, Sect. 3 represents the results and its analysis and Sect. 4 offers the conclusion.

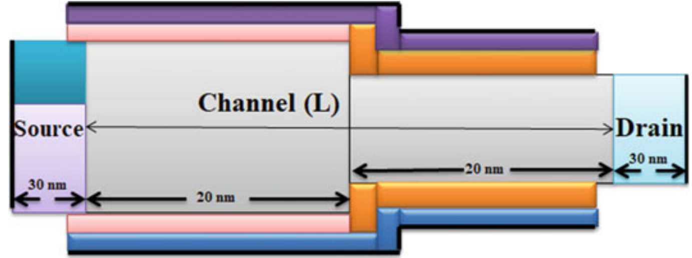

Fig. 1 Schematic structure of the simulated NUTFET-DMS

2 Structure and Simulation Description

The structure non-uniform body TFET with dual material source (NUTFET-DMS) is shown in Fig. 1. As already mentioned source consists of silicon (Si) on the upper half and germanium (Ge) on the lower half with a concentration of doping of about $1 \times 10^{20}/\text{cm}^3$ to maintain a lower average SS for the device, channel and drain are made up of only Si with doping concentration of 1×10^{15} cm^{-3} and 1×10^{18} cm^{-3}, respectively. In addition, to maintain high ON current, low OFF current and ambipolar current, different channel thicknesses are incorporated. Further, high-k (HfO_2) and low-k (SiO_2) dielectrics of different dielectric thickness near source and drain ends are considered, respectively. The channel length (L) is of 40 nm. Both front and back gate oxide dielectric thicknesses are of 1 and 7 nm in drain and source side, respectively. For the simulation of this device, Sentaurus TCAD software has been used [22]. As TFET works on interband tunneling, band gap narrowing model and non-local BTBT models are activated. For mobility and recombination process, doping dependence and Schokly-Read-Hall (SRH) models are considered. The presence of donor ITC is considered at both front and back gate oxide semiconductor interface. In case of distribution of ITC, uniform distribution as well as Gaussian distribution has been considered. Different device parameters used in the analysis are enumerated in Table 1.

3 Results and Analysis

In this section, drain current and gate voltage noise power spectral densities (S_{id} andS_{vg}) are calculated considering the low frequency flicker noise at 1 MHz. Further, in the study, the absence of ITC and presence of donor type of ITC at silicon-oxide interface (Si-HfO_2 and Si-SiO_2) have been considered followed by a temperature variation at 200, 300 and 400 K.

The current noise power spectral densities of the device in the presence of trap charges and absence of ITC are presented in Fig. 2. Figure 2a shows the variation of S_{id} at 200 K and room temperature (300 K) for different conditions of trap charges.

Table 1 Values of different parameters of the device

Parameters	Value
Channel length (*L*)	40 nm
Dielectric thickness over higher body thickness	0.7 nm
Dielectric thickness over lower body thickness	1 nm
Source length	10 nm
Drain length	10 nm
Source doping concentration	1 × 1020 cm^{-3}
Drain doping concentration	1 × 1018 cm^{-3}
Body doping concentration	1 × 1015 cm^{-3}
Thickness of higher body thickness	15 nm
Thickness of lower body thickness	7 nm
Total device length	60 nm

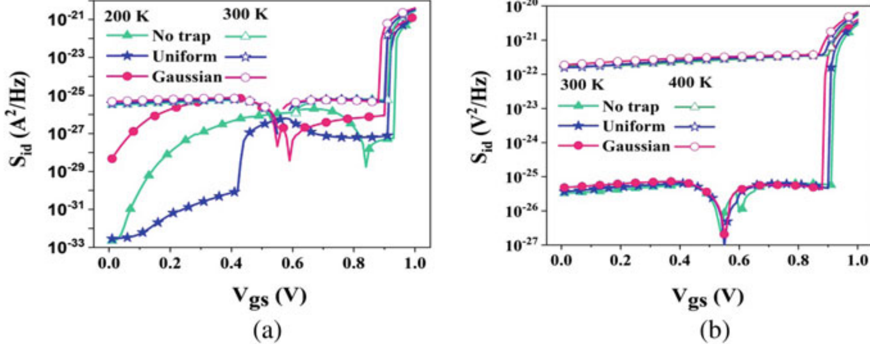

Fig. 2 Plot of S_{id} versus V_{gs} of NUTFET-DMS under variation of temperatures at **a** 200 and 300 K, **b** 300 and 400 K

It can be perceived that if temperature decreases from room temperature, the value of S_{id} decreases. This is because of the decrease in drain current with temperature as shown in Fig. 3a [23]. The relationship between I_d and S_{id} in the presence of trap charges and absence of ITC is presented in the Eq. 1 [24].

$$S_{\text{id}} = I_D^2 \frac{N_t}{N^2} \frac{\tau}{1 + (2\pi f \tau)^2} \tag{1}$$

where I_D is the drain current, f is the frequency, τ is the transition time constant, N is the number of device charge carriers, N_t is the number of ITC present, where $N_t = N_{\text{trap_filled}} + N_{\text{trap_empty}}$, $N_{\text{trap_filled}}$ is the trap with filled state and $N_{\text{trap_empty}}$ is the trap with empty state. Equation 1 clearly displays that the drain current of a

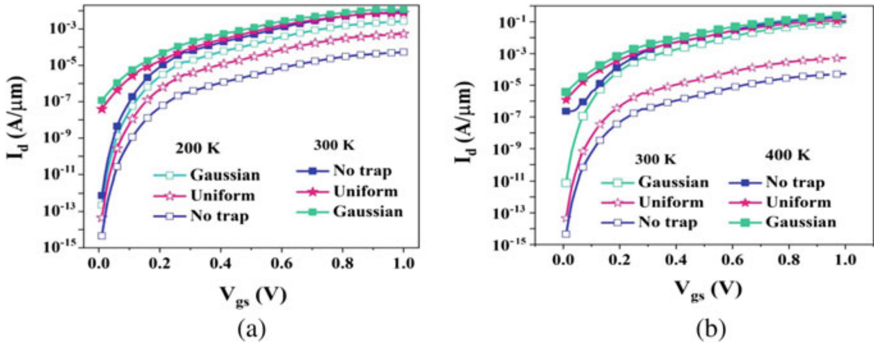

Fig. 3 Plot of drain current of NUTFET-DMS under variation of temperatures **a** 200 and 300 K, **b** 300 and 400 K

device is direct proportionate of the drain current noise power spectral density of the device. Similarly, S_{id} comparison for temperature of 300 and 400 K is presented in Fig. 2b which shows that at high temperatures, S_{id} increases due to increase in drain current as displayed in Fig. 3b. Now, it can be perceived that inception of trap charges increases the S_{id} of the considered device and shows higher degradation in the situation of Gaussian distribution of ITC because of higher fluctuations of carriers. The degradation caused due to trap charges is more severe at low temperatures and becomes negligible at very high temperatures because of more electron density generated due to thermal process. It can be observed that various peaks exist in S_{id} at different gate to source voltages which is because of the irregular generation rate of BTB at different temperature and gate to source voltages [25]. On the contrary from the Fig. 2b of S_{id} and Fig. 4b of S_{vg}, it can be seen that at high temperatures mutually for the presence and absence of ITC to a certain value of gate to source voltage, no peaks appear in the plot. This may be due to the higher thermal agitation in the device

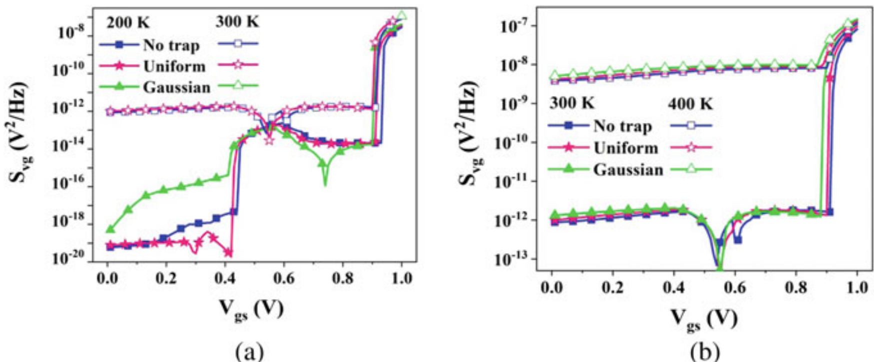

Fig. 4 Plot of gate voltage noise power spectral density (S_{vg}) versus gate to source voltage (V_{gs}) of NUTFET-DMS under variation of temperatures at **a** 200 and 300 K, **b** 300 and 400 K

makes the noise power spectral densities negligibly affected by the change in band to band generation at different gate to source voltage.

Figure 4 shows the gate noise power spectral density vs. gate to source voltage for the absence and presence of ITC under the occurrence of both uniform and Gaussian distribution. The analysis has been performed under flicker noise consideration at 1 MHz frequency. Figure 4a, b represent the comparison of S_{vg} at room temperature with both low and high temperature is similar to S_{id} variation. This is because of the S_{vg} of the device is directly proportional to S_{id} which is evident from the relationship between S_{id} and S_{vg} can be seen from Eq. 2 [21, 26].

$$S_{\mathrm{id}} = I_d^2 \frac{(\beta T)^2}{SS^2} S_{\mathrm{vg}} = G_m^2 . S_{\mathrm{vgfb}} \tag{2}$$

where SS is the subthreshold swing, G_m is the transconductance, β is the Boltzmann constant, T is temperature. The above equation also validates the fact of increasing noise power spectral densities with temperature. Finally, it can portray that at high values of temperature, the presence of donor trap charges has negligible effect on flicker noise of the device and the reverse is true for low temperatures.

4 Conclusion

The study incorporated the flicker noise characterization of non-uniform body TFET with dual material source (NUTFET-DMS) in terms of drain current and gate to source voltage noise power spectral densities (S_{id} and S_{vg}). In the study, different conditions of trap charges (occurrence and absence of donor ITC) and temperature variation (200, 300, and 400 K) have been included in the analysis of noise to explore the reliability of the device. In the situation of the occurrence of donor ITC, both type of distribution such as uniform and Gaussian have been considered to account for the real time scenario. It has been perceived that at high temperatures degrades the flicker noise of the device but nullifies the trap charges effect. However, at low temperatures, though noise of the device decreases, but trap charge effect becomes significant.

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Study of Temperature Effect on MOS-HEMT Small-Signal Parameters

G. Amarnath, Manisha Guduri, A. Vinod, and M. Kavicharan

Abstract This paper presents an effect of temperature on small-signal equivalent circuit parameters that have been analyzed for AlInN/AlN/GaN metal-oxide-semiconductor high electron mobility transistor (MOS-HEMT). The analysis has been performed with the temperature range from −50 to 100 °C by S-parameter calculations at 100 GHz frequency. The thermal analysis of equivalent circuit parameters was investigated for the first-time with the proposed device. The equivalent circuit parameters such as intrinsic delay time (τ), gate–source capacitance (C_{gs}), extrinsic resistances (R_g, R_s, R_d), and intrinsic resistances (R_{ds}, R_{gd}, R_{in}) show a positive shift with increasing temperature. On the other hand, intrinsic transconductance (g_m), drain–source capacitance (C_{ds}), and gate–drain capacitance (C_{gd}) show a negative shift with temperature. Obtained results will give some valuable information for design optimizations of GaN-based Monolithic microwave integrated circuits (MMICs) and other high power/frequency applications.

Keywords Small-signal equivalent circuit · MOS-HEMT · Temperature analysis · Intrinsic parameters · Extrinsic parameters

1 Introduction

AlInN/GaN metal-oxide-semiconductor high-electron-mobility-transistors (MOS-HEMTs) are greatly suitable for low-noise [1], high frequency [2], high-power [3], and good linearity applications in RF, millimeter and microwave frequency ranges

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due to attracted compound semiconductor material properties. The distinctive properties and an advancement of GaN-technology results in MMICs growth of mixers, low noise amplifier (LNA), and voltage controlled oscillator (VCO), etc. [4]. GaN-based heterostructure devices give higher sheet charge density (n_s) due to large number of carriers confined in the channel quantum-well and large discontinuity in conduction band at the heterostructure interface. Hence large current-density and transconductance are attainable and high-frequency and high-power device operation is possible.

These high-capable devices are appropriate for operate over large temperature ranges and are required for different applications, including space, aircraft, and automotive technology [5]. The temperature-dependent device characteristics at high temperature range has become a critical thing in the MMIC designs state-of-the art [6]. There have few reports [7] presenting the temperature influence on different small-signal-equivalent-circuit (SSEC) parameters of HEMTs with GaN. Caddemi et al. [8] investigated the dc and SSEC parameters with temperature. Also, the thermal effect on large-signal circuit parameters measurement have been analyzed for GaN HEMT with different temperatures [9].

However, with the constant progress in GaN, microwave range heterostructure devices are needed to analyze with different parameters to develop efficient active circuits in present communication systems. Presently, there is no study investigating the effect of SSEC parameters with temperature using the considered device structure. It is quite important to effectually analyze the transistor behavior with ambient temperature. Therefore, in this paper, the investigation is focused on the temperature influence on SSEC parameters. of AlInN/GaN MOS-HEMT SSEC parameters.

2 2-D Structure View and Its Equivalent Circuit

An investigated AlInN/GaN MOS-HEMT structure cross-sectional schematic interpretation is presented in Fig. 1. This structure is developed and simulated with physics based 2-D numerical simulations using GIGA and BLAZE modules from SILVACO Atlas TCAD. The 2-D structure is having 2.5 μm thickness of GaN channel sheet with 1.5 nm thickness of Aluminum Nitride (AlN) intervening sheet and AlInN restriction layer of 15 nm with 83% of Al-content. The AlN sheet is utilized at the AlInN/GaN intersection to improve the charge and mobility. The device at ambient temperature shows a 2-DEG (2-Dimensional-electron-gas) charge density of $1.3 \times 10^{13}/\text{cm}^2$ and the mobility of charge carrier is 1270 $\text{cm}^2/\text{V s}$. The HfO_2 oxide layer of 10 nm thick is used for this device. The gate length of 100 nm, a distance of drai-to-source is 1 μm, distance of gate-to-drain is 0.6 μm and distance from source-to-gate is 0.3 μm. The width of the gate region is 100 μm is considered.

The SSEC of the considered structure of AlInN/GaN MOS-HEMT is presented in Fig. 2. Commonly, the elements of equivalent-circuit are distributed into an extrinsic and intrinsic portion which comprise of (C_{pg}, C_{pd}, C_{pgd}, L_g, L_s, L_d, R_d, R_{s}, and R_{g}) and (C_{gd}, C_{gs}, C_{ds}, R_{gd}, R_{in}, R_{ds}, τ and g_m) respectively.

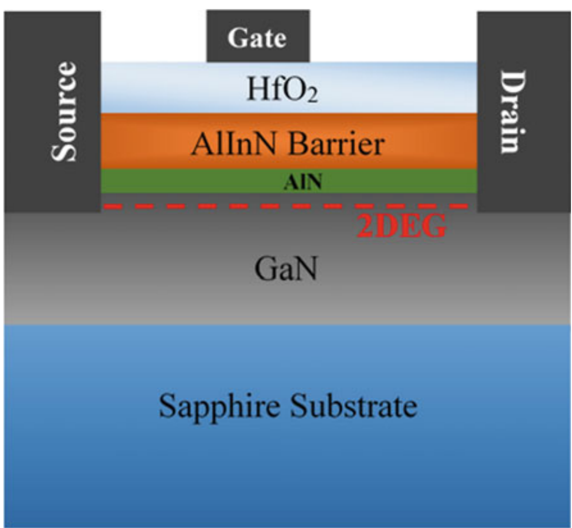

Fig. 1 Schematic 2-D view of considered AlInN/GaN MOSHEMT

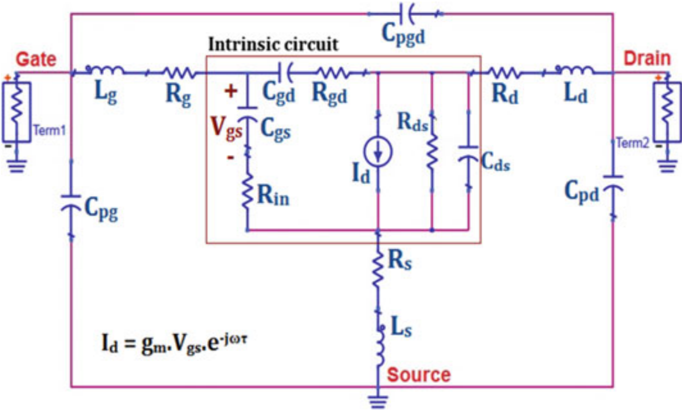

Fig. 2 AlInN/AlN/GaN MOS-HEMT small-signal-equivalent-circuit with intrinsic and extrinsic parameters

The parasitic (or extrinsic) parameters are accounted to be independent of bias (V_{ds} and V_{gs} are at 0 V) as they are specifying in model the transistor and outer side of the inter-connections. The intrinsic part parameters are accounted to be dependent of bias ($V_{gs} = -4$ V, V_{ds} and $V_{gs} = 0$ V, $V_{ds} = 5$ V,). The parasitic part consist of three parasitic resistances and inductances with each contact and wire connection as three-terminal device. The extrinsic inductances, L_g, L_d, and L_{ds} shows the influences of inductance arises from pad connections. The extrinsic resistances R_g, R_d, and R_s comes from the gate (g), drain (d) and source (s) contacts, respectively. The extrinsic inductances are to be calculated from the Z-parameters slope of the imaginary part

and the extrinsic resistances are to be estimated from the Z-parameters real parts of the slope as explained in [10]. The pad capacitances C_{pg}, C_{pgd} and C_{pd}, are to be estimated from Y-parameters imaginary parts of the slope as in [10].

The SSEC intrinsic part consists of eight elements are gate-source capacitance and input channel resistance (C_{gs} and R_{in}); voltage controlled current source (g_m and τ); gate-drain charging capacitance and resistance with (C_{gd} and R_{gd}) a feedback RC-series network; drain-source capacitance and resistance (C_{ds} and R_{ds}) with output RC-parallel network; a vital parameter in SSEC is an obtaining of parasitic elements. Hence, a prior consideration given to parasitic elements with a condition of $V_{\text{gs}} = -4$ V and $V_d = 0$ V. The equivalent circuit extrinsic portion elements are needed to estimate a physically presented elements of intrinsic equivalent circuit [11].

3 Temperature Dependent Parameter Modeling

The most considerable semiconductor device properties that depends on temperature are material bandgap (E_g), electron mobility (μ), electron velocity saturation (ϑ_{sat}), built-in-potential (V_{bi}), dielectric-constants (ε), barrier height, and specific-contact-resistance. The bandgap energy change with temperature, $E_g(T)$, expressed as [12],

$$E_g(T) = E_g(T_0) - \frac{\alpha T^2}{(T + \beta)} \tag{1}$$

where α and β are constant and features of a considered material and $E_g(T_0)$ is the energy bandgap at a temperature. The effects of surface potential and Schottky barrier height with change in temperature is represented in built-in potential terms as,

$$V_{\text{bi}}(T) = V_{\text{bi}}(T_0) + m\left[E_g(T) - E_g(T_0)\right] \tag{2}$$

where parameter m is lies in 0 and 1. The change in temperature of device parameters, due to ϑ_{sat}, specific contact resistance and ε, are expressed in common parameter $A(T)$ expression as

$$A(T) = A(T_0)[1 + \delta(T - T_0)] \tag{3}$$

where $A(T_0)$ is the parameter for temperature in degree Celsius. δ is the coefficient of temperature with units per degree. The representation of (3) permits one to estimate the slope, δ, for any parameter which depends on temperature.

4 Results and Discussion

During the extraction of small signal parameters with temperature, extrinsic elements are the device parasitics C_{pd}, C_{pg}, C_{pgd}, L_d, L_g, L_s, R_d, R_g, and R_s are (independent of bias condition) extracted first then the intrinsic parameters. The considered device is simulated to analyze the thermal influence on equivalent circuit parameters with SSEC. The structure is developed in TCAD environment and equivalent circuit is modeled using Keysight ADS tool. The parasitic capacitances are estimated by using the cold-FET technique [13]. When gate voltage is less than the threshold voltage and $V_{\mathrm{ds}} = 0$ V, the conductivity of the channel is trivial and S-parameters of the device exhibits capacitive behavior [14].

The parasitic capacitances are calculated by Y-parameters of Y_{22}, $Y_{12} = Y_{21}$ and Y_{11},) imaginary parts of the slope as in [10]. Figure 3 shows the effect of parasitic capacitances with temperature changes. The extrinsic capacitances are observed to be unchanged with the temperature. Due to the existence of gate differential resistances, the extraction of extrinsic resistances and inductances in heterostructures are commonly execute at zero or nearly negative bias [10]. The extrinsic are calculated from the Z-parameters imaginary part of the slope of ω. $\mathrm{Im}(\omega Z_{ij})$ versus ω^2 by linear fitting [15]. These parameters are calculated for temperature range of −60 to 100 °C. The effect of parasitic inductances L_g, L_s, and L_d, with respect to changes in temperature is shown in Fig. 4. The extrinsic inductances observed to be remains same with the temperature.

The parasitic resistances are near to the device terminals along the gate, drain and source and change linearly with temperature. The effect of extrinsic resistances along with temperature changes is presented in Fig. 5. The variations in the extrinsic resistances are due to the change in metallization conductivity and semiconductor material properties.

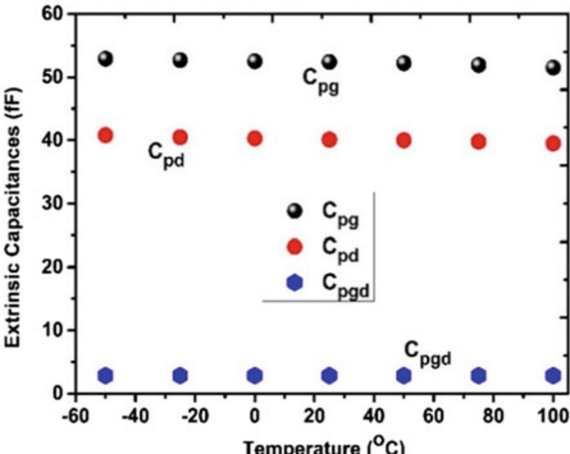

Fig. 3 Effect of parasitic capacitances C_{pg}, C_{pd}, and C_{pgd} with temperature

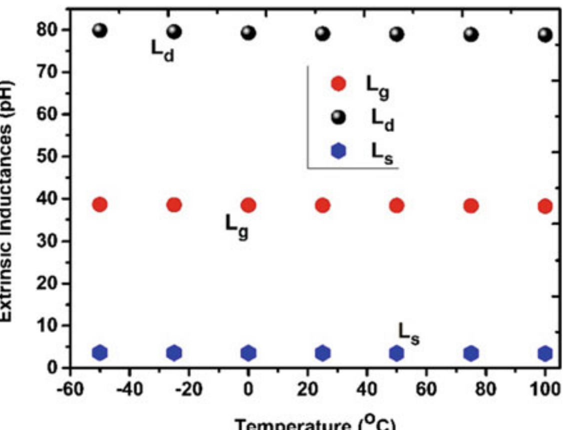

Fig. 4 Effect of parasitic inductances (L_g, L_s and L_d) with temperature

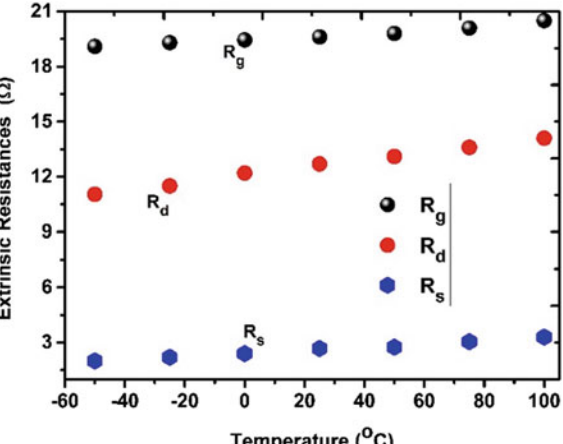

Fig. 5 Effect of parasitic resistances (R_g, R_s, and R_d) and with temperature

The applied bias dependent intrinsic parameters are investigated with respect to temperature changes and different biasing conditions. Figure 6 shows C_{gs}, C_{gd}, and C_{ds} variation along with temperature and biasing conditions. These capacitances are related to depletion area below the gate. The depletion area width changes with the alteration in bias as intrinsic capacitances will change accordingly. From Fig. 6, it is observed that the C_{gs} is increasing with temperature increases due to the thermally energized carrier phenomena [16]. C_{gd} and C_{ds} is relatively decreasing as temperature decreasing due to temperature dependent charge confinement. The substrate material, device geometry and depletion width are affect the C_{ds} value.

Figure 7 shows the effect of intrinsic resistance R_{ds}, R_{gd}, and R_i with temperature. It is observed that the R_{ds} and R_{gd} rises with temperature. R_{ds} is an essential parameter that will effect directly to the output-power and the efficiency.

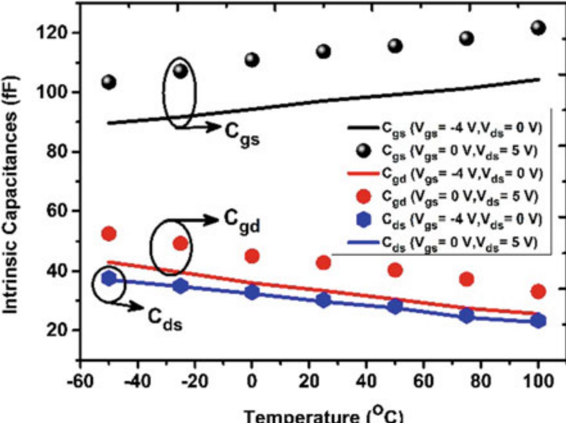

Fig. 6 The intrinsic-capacitances variation with temperature at different biasing conditions

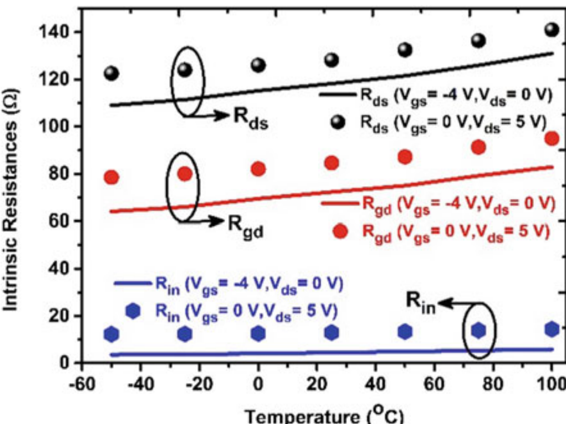

Fig. 7 The intrinsic resistance variation with temperature at different biasing conditions

The input resistance R_{in} is the intrinsic resistance created at beneath gate region at the channel and source area. It is primarily incorporated to improve the S_{11}. Figure 8 shows the effect of intrinsic transconductance and intrinsic delay time with respect to temperature changes. The intrinsic transconductance, g_{mo} is decreasing linearly with temperature. The transconductance is an important parameter of the quality of the device for high frequency applications. A high transconductance of the device will provide superior frequency performance and higher gains. The delay time, τ is increasing linearly with temperature shows a lengthy time delay. The temperature-dependent intrinsic parameters are significantly changed with respect to change in bias conditions.

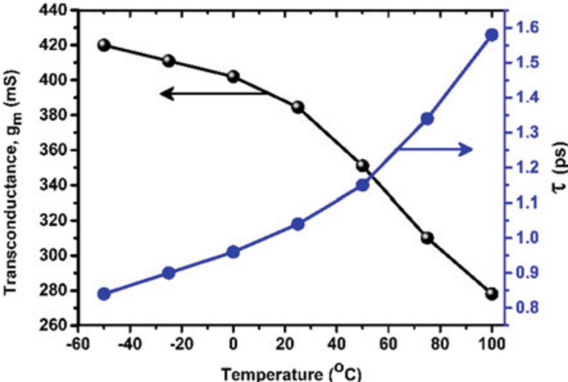

Fig. 8 The intrinsic transconductance and intrinsic delay time variation with respect to temperature

5 Conclusion

This paper presents the effect of temperature on SSEC-parameters for AlInN/AlN/GaN metal-oxide-semiconductor high-electron-mobility-transistor. Substantial small signal parameters are showing the positive increment with temperature increases. The transconductance, gate-drain and drain-source capacitances are showing decrement with wit temperature increases. Among all the small-signal parameters, the gate-source capacitance provides the smaller sensitivity temperature. The analysis shows that the temperature effect has various degrees of impact on different device parameters gives valuable penetration for further optimizations GaN-based MMICs.

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Numerical Simulation-Based Comparative Study of FinFET and MOSFET with Gallium Oxide

G. Amarnath, Manisha Guduri, A. Vinod, and M. Krishnasamy

Abstract This paper presents a TCAD-based comparative study of vertical power transistors with gallium oxide specifically to FinFET and MOSFET. Also, an electrothermal performance of FinFET and MOSFET is studied with different operating conditions. Semiconductor devices with gallium oxide (Ga_2O_3) are contemplated to change the applications of power electronics in coming years. There is a possibility to develop Ga_2O_3-based power semiconductor devices with low on-resistance and large breakdown voltage compared to silicon carbide (SiC)- and silicon (Si)-based devices. The normally off condition can be achieved in FinFET devices by proper Fin design in donor concentration and width. This study will be helpful in analytical model development and fabrication of Ga_2O_3-based power transistors.

Keywords Ga_2O_3 · FinFET · MOSFET · TCAD

1 Introduction

In recent years, gallium oxide (Ga_2O_3) has achieved a significant interest due to superior material properties which are 4.85 eV of wide band gap, ~8.1 MV/cm of large breakdown field and resulting in good figures of merit [1–4]. Ga_2O_3-based devices with high figures-of-merit results in chance to fabricate and characterize with large breakdown voltage low on-resistance and higher switching speeds [5]. Also, there is a possibility to fabricate high-quality Ga_2O_3 material wafers with high reliability and low-cost transistors [6]. The remarkable downsides of Ga_2O_3 are low

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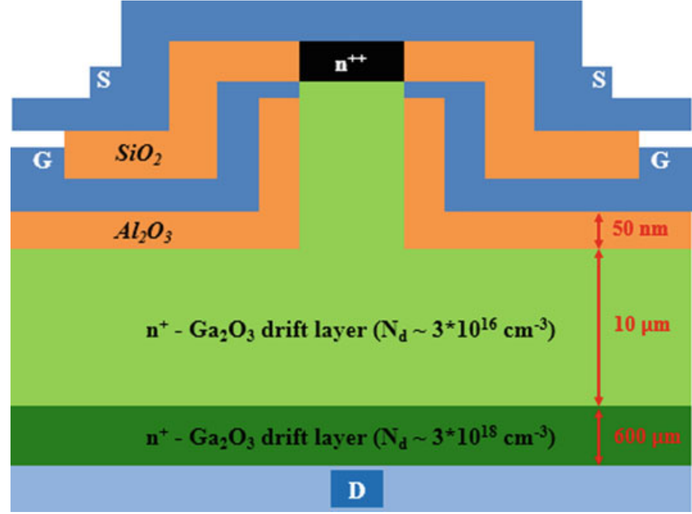

Fig. 1 Cross-sectional view of simulated vertical FinFET structure

carrier mobility and less thermal conductivity in comparison with leading GaN and SiC semiconductor materials [7].

Recently, different Ga_2O_3-based devices are reported [8] with enhancement mode and lateral depletion mode and also with different vertical transistors. The lateral depletion transistors are commonly not applicable for breakdown voltages higher than 600 V and other applications [9]. The vertical structures are not having these limitations. So it can cover large range of applications including motor drivers, power electronics, high-voltage modular and DC converters and photovoltaic inverters [10]. The two vertical device structures, FinFET and MOSFET, with β-Ga_2O_3 are considered for the study and are shown in Figs. 1 and 2, respectively.

A physics-based technology computer-aided design (TCAD) models are used for numerical simulations of the vertical FinFET and planar vertical MOSFET. Different mixed-mode studies are performed to estimate the performance of electrothermal analysis of vertical structures. The p-type doping effects on vertical MOSFET and geometry effect of the Fin on vertical FinFET are evaluated in terms of current gain and threshold voltage.

2 Simulation Methods

The considered transistor structures are shown in Figs. 1 and 2 with defined doping profiles and thicknesses. The performance of the transistors is simulated by considering 2-D hole and electron continuity equation, time-domain finite difference analysis, thermodynamic equations and Poison's equation.

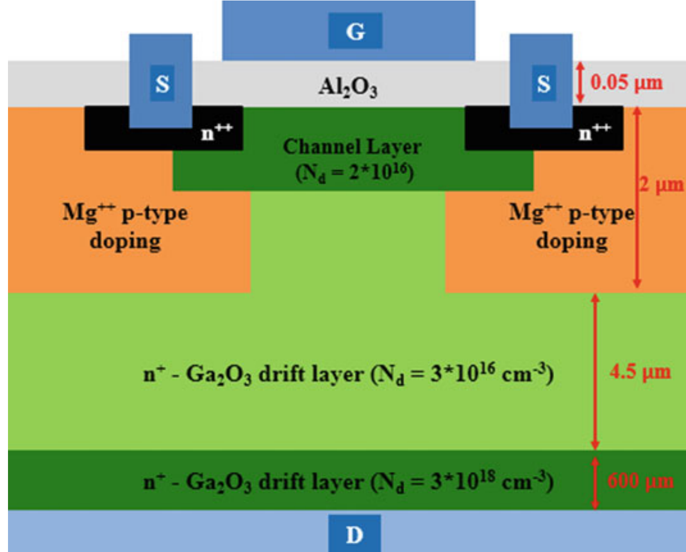

Fig. 2 Cross-sectional view of simulated planar MOSFET structure

The alternating current (AC), direct current (DC), electrothermal and transient characteristics are extracted to estimate the suitability of Ga_2O_3 based FinFET and MOSFET. The DC analysis has been performed to extract the DC output and transfer characteristics. A small-signal AC analysis has been performed to extract capacitance characteristics with respect to applied voltages.

3 Results and Discussion

3.1 Planar Vertical MOSFET

The planar vertical MOSFET of Fig. 2 uses a body layer with current blocking of p-type and n-type Ga_2O_3 drift layer. The considered structure is similar to planar shielded-vertical MOS devices with shielding region p-type Mg doped and extends to the N− base and N+ source regions. The edges of the body region channel region are located at the body region extension of the N+ source excess edges. The threshold voltage can be estimated from the doping concentration and the thickness of N− base side, and hence, a PN junction is formed between fully depleted N-base and body region.

An external potential is applied to the metal gate terminal for conduction of the current. This applied bias makes an accumulation region which creates current conduction with electrons beneath the oxide region at N-base region of the surface.

The shielding area at the terminal of the body protects the oxide area from the drift area with negative electric fields. A high negative voltage will be reinforced at depletion region created between the N-drift area and P+ body area at the transistor blocking mode.

The reinforced transistor breakdown voltage maximum and drift area resistance form an essential trade-off. In [11], the threshold voltage of Ga_2O_3-based MOSFET has been reported to −55 to −60 V as shown in Fig. 3. Figure 4 shows different Mg-doped device transfer characteristics obtained by TCAD with a concentration of acceptor is $5 \times 10^{17}/cm^3$ and is similar to [11]. Figure 5 shows the output characteristics of planar vertical MOSFET. The threshold voltage of this device is different from the required performance of the transistor which is useful for switching applications. The threshold voltage goes more positive which is essential for power electronic applications when concentration of acceptor is high and N-base area thickness is low. Hence, N-base area thickness and doping concentrations were properly adjusted to achieve the needed threshold voltage.

Figures 4 and 5 show the transfer and output characteristics of Ga_2O_3-based Mg-doped MOSFET, respectively. The heavily dopant Mg concentration in the device body area is 10^{17} to $10^{19}/cm^3$, N-base area donor concentration is $3.5 \times 10^{16}/cm^3$, and the thickness of N-base area is 0.5 μm. This device acquired a −0.3 V of threshold voltage which is larger than the reported in [11], and also it decreases in the current with increase in acceptor concentration. These results lead to negative trade-off in planar vertical MOSFETs. Also, the drain current decreases with increase in gate voltage due to increase in drift resistance.

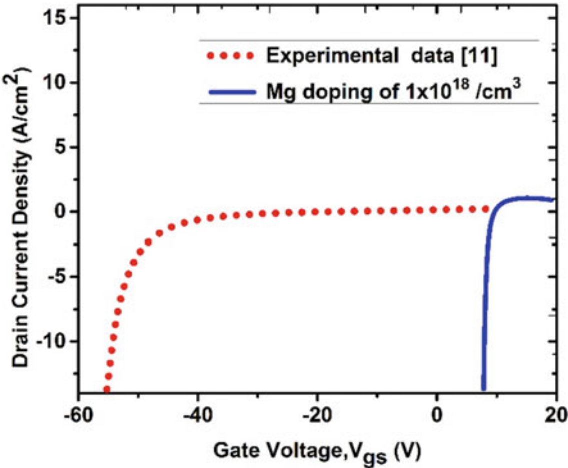

Fig. 3 Simulated I_D-V_{GS} characteristics in comparison with experimental data [11]

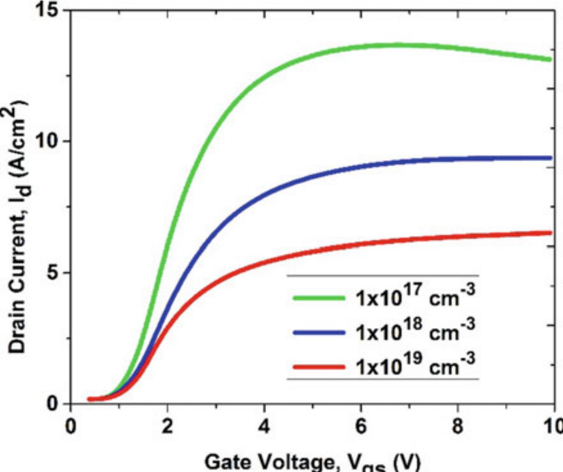

Fig. 4 Simulated I_D-V_{GS} characteristics with different Mg doping levels

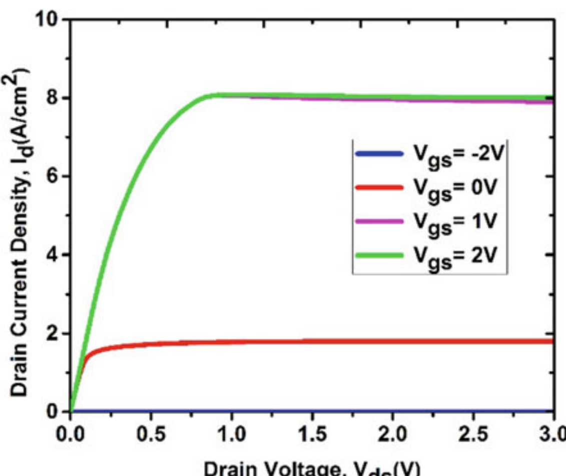

Fig. 5 Simulated I_D-V_{DS} output characteristics of MOSFET

3.2 FinFET Structure in Vertical Mode

The FinFET is another significant device which is predominant in recent years with Ga_2O_3 and GaN materials. Figure 2 shows vertical Ga_2O_3-based FinFET cross-sectional view. This device is used to avoid the problems in getting the required acceptor p-type concentration unlike the planar vertical MOSFET. For different analog CMOS integrated circuits, FinFET lateral structures have gained an advanced market place. An n-type drift layer formed with a concentration of donor is 10^{16}/cm^3 on top of the unintentionally doped Ga_2O_3 substrate with 10^{18}/cm^3.

The channel current at on-state is conducted through a Ga_2O_3 vertical Fin-shaped area covered under the oxide and gate metal regions. The electron charges in the Fin-structured channel area are fully depleted in any gate external bias absence due to difference in work function of metal semiconductor. The width of Fin is arranged to make normally off operation from the depletion region on each side of the middle area. The n-drift area developed on β-Ga_2O_3 substrate supports applied large reverse voltage to the transistor. The drift area doping concentration and width are adjusted to get the required large reverse breakdown voltage.

The DC transfer and output characteristics of FinFET are shown in Figs. 6 and 7, respectively. From the transfer characteristics, it is observed that the threshold voltage is near to 1.2 V for a 0.005 μm width of Fin, evolving to a normally off

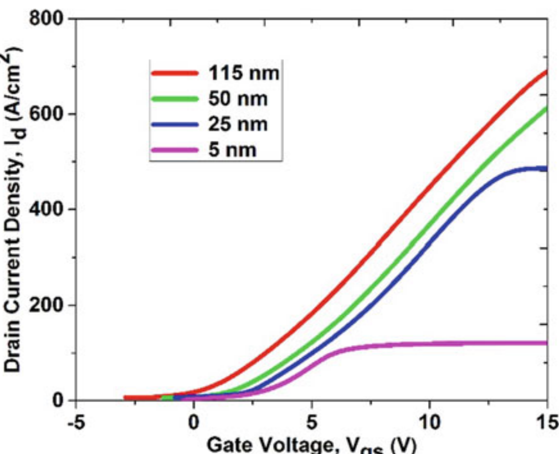

Fig. 6 Simulated I_D-V_{GS} characteristics with different Fin widths

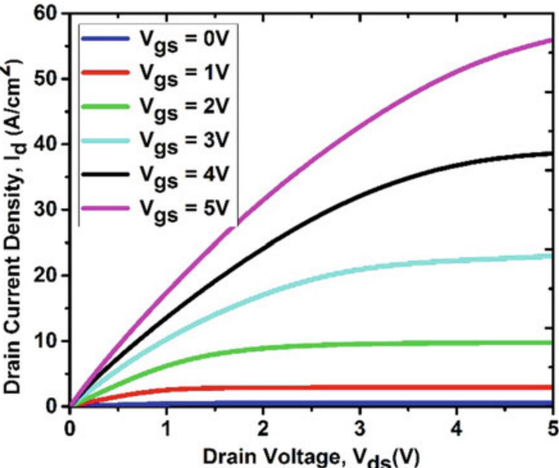

Fig. 7 Simulated I_D-V_{DS} output characteristics of FinFET

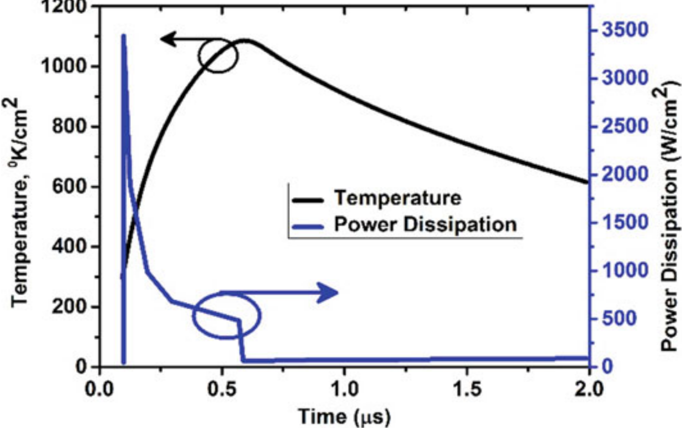

Fig. 8 Power dissipation and temperature characteristics of FinFET

operation of the device with strong current saturation. The current gain increases with increase in width of Fin to 0.005–0.115 μm, and the threshold voltages became more negative. The output characteristics demonstrate that the intrinsic resistances and capacitances are quite small for 0.005 μm width of the Fin.

Figure 8 shows the vertical FinFET electrothermal characteristics. From this analysis, the decrease in static current for each bias condition with increase temperature at junction is observed because on-resistance increases. The junction transient temperature and dissipation of power increase for short-circuit condition. The junction transient temperature goes up to 1120 K and power dissipation rises to 3550 W/cm^2 with 1 kV DC voltage when the transistor short circuited. It shows that the stability of electrothermal can be discussed through proper solutions in system level or fabrication level.

4 Conclusion

This manuscript shows TCAD-based comparative analysis of Ga_2O_3 substrate vertical FinFET and MOSFET structures. These numerical simulation results are compared with experimental data available in the literature and found in good agreement. The analysis reveals that the planar vertical MOSFET has depletion-mode operation and less threshold voltage. Also, these results suggest that the threshold voltage is enhanced with acceptor concentration increasing and N-base area thickness adjustment at a cost of current gain. Other side, the FinFET device eliminates the p-type doping requirement and gives a direction for normally off devices by proper channel doping concentration and width of the Fin. The simulation-based FinFET

characteristics suggests that it could be more possibility in developing Ga_2O_3-based power devices with significant performance.

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Optimization of 2D Ge-Pocket Asymmetric Dual-Gate Tunnel FETs

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Abstract This work reports a Tunnel field-effect transistor based on Ge-source pocket technique. The main aim is to improve the current ratio and Subthreshold Slope (SS). A dual-material asymmetric dielectric gate has been used to optimize the device performance. The critical parameters such as current ratio, SS, threshold voltage, ambipolarity are studied in this work. This work also includes capacitive analysis of the proposed structure. A comparative analysis with existing structures shows the effectiveness of the proposed work. A significant reduction in SS and threshold voltage is reported in this structure. A current ratio of 10^{12} is obtained along with much reduction in ambipolarity.

Keywords Band-to-band tunnelling (BTBT) · Tunnel FET (TFET) · Ge-pocket · TCAD

1 Introduction

The threshold voltage of MOSFET is limited as the Subthreshold Slope (SS) in MOSFET cannot be reduced below 60 mV/Dec at 300 k [1]. Thus, this limits the supply voltage scaling which is very important parameter for low-power device designs [2]. There comes the need for an alternate device having low SS [2–4]. Thus, for future low-power device applications one of the promising candidate is TFETs because of its performance potential compared to conventional MOSFETs under reduced voltage supply (V_{DD}) [5–7]. Among all design system currently being explored, pocket TFET has great potential making it a great alternative for future VLSI technologies. The experimental research reports that in TFETs as the content of Ge increases there is significant improvement in on-state current (I_{on}) [8]. However, as the Ge content in the proposed device increases, there is increase in leakage in the off-state has been reported. Low band gap material such as germanium is known to improve BTBT and thereby improves current ration and SS [9]. The tunnelling

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efficiency and SS are related as follows.

$$\begin{aligned} SS &= \left[(\partial \log(I_{DS}\ )|\partial V_{GS}\ )\right] \propto \left[\partial \log T \frac{\lambda}{\partial V_{GS}}\right]^{-1} \\ &= \left[\ln(10)\left(\frac{4\sqrt{2m} * E_g^{1/2}}{3q\hbar} | \frac{\delta\lambda}{\delta V_{GS}}\right)\right]^{-1} \end{aligned} \quad (1)$$

Equation (1) depicts that the SS significantly depends on tunnelling length (λ). As shown in Eq. (1), the tunnelling probability T is influenced by on the bandgap of material, effective mass, etc.

Thus, this work mainly focuses on improvement across the tunnel junction by incorporating pocket as well as using asymmetric dielectric in the device. It is shown that the on-state current (I_{on}) of Ge-Pocket TFETs increases considerably. Also, the off-state current can be reduced using an asymmetric dual gate. In this work, the idea asymmetric dual-gate TFET, Ge-pocket and variable gate metal work function are proposed. The steep SS and high I_{on} are achieved by using Ge-Pocket at reduced $V_{DD,}$ and reduced off-state current is achieved by different gate metal work function. The proposed TFET shows exceptional scalability in terms of physical channel length (L_{gate}) and $V_{DD,}$ that makes it a favourable candidate for low-power applications. The various sections in paper include describing the architecture in Sects. 2 and 3 discusses the results and reports comparisons. Finally, the conclusion is drawn in Sect. 4.

2 Device Structure and Simulation Setup

The conventional Dual-Gate TFET device structure is shown in Fig. 1, and proposed Ge-Pocket ADGTFET device structure is depicted in Fig. 2. This device utilizes the concept of using pocket structures at the source-channel junction. The tunnel junction uses a small pocket made of germanium. The confinement of Ge layer at the junction is found to improve the device efficiency without degrading the leakage current across the device. The device parameter used and doping concentration across

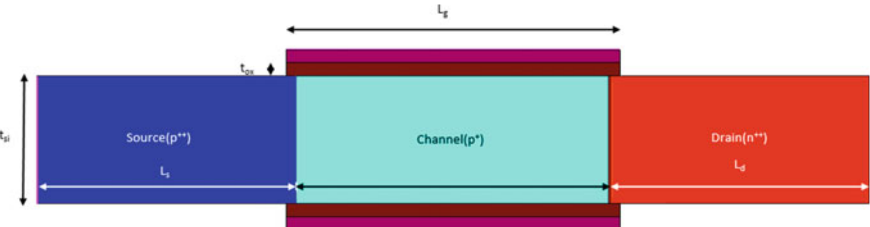

Fig. 1 Conventional DGTFET device structure

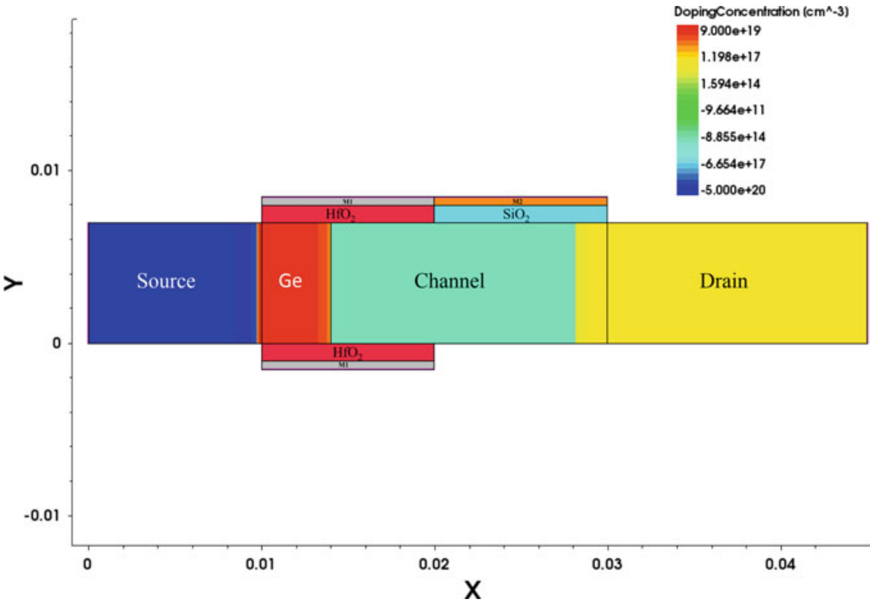

Fig. 2 Proposed Ge-Pocket ADGTFET device structure

the various regions are in Table 1. A dielectric layer of high K material [10] of length 12 nm is inserted on the top and bottom of tunnel junction for higher gate control. Also, the rest of the channel till the channel drain interface includes a low k dielectric material SiO_2 of length 10 nm. TCAD [11] simulation tool is used to perform the

Table 1 Proposed Ge-Pocket ADGTFET device structure

Parameters	Symbols	Values
Device layer thickness	(t_{si})	10 nm
Gate length	(L_g)	22 nm
Oxide thickness	(t_{ox})	1 nm
Gate work function	M1(WF1)	4.36 eV
	M2(WF2)	4.64 eV
Doping concentration	Source (p^{++})	$5 \times 10^{20}/cm^3$
	Pocket (n^{++})	$9 \times 10^{19}/cm^3$
	Channel (p^{+})	$1 \times 10^{15}/cm^3$
	Drain (n^{++})	$9 \times 10^{16}/cm^3$
Source length	(L_s)	10 nm
Pocket length	(L_p)	4 nm
Channel length	(L_c)	16 nm
Drain length	(L_d)	15 nm

simulations. Due to higher source and drain doping, Fermi–Dirac statistics and Band Gap narrowing models are used.

3 Results and Discussion

Figures 3 and 4 represent the band structure of proposed Ge-pocket ADGTFET structure in the off-state and on-state. From Fig. 4, it can be inferred that due to Ge-Pocket in proposed device structure there is substantial band bending due to which charge carriers can easily tunnel and it results in increase in on-state current as compared to conventional DGTET. It was also observed that there is a significant

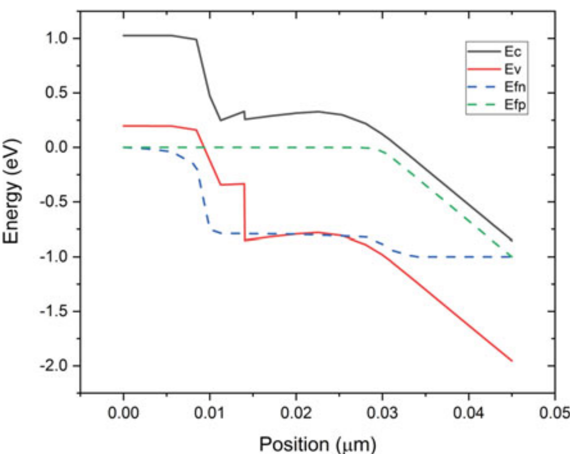

Fig. 3 Energy band diagram of proposed Ge-Pocket ADGTFET in off-state

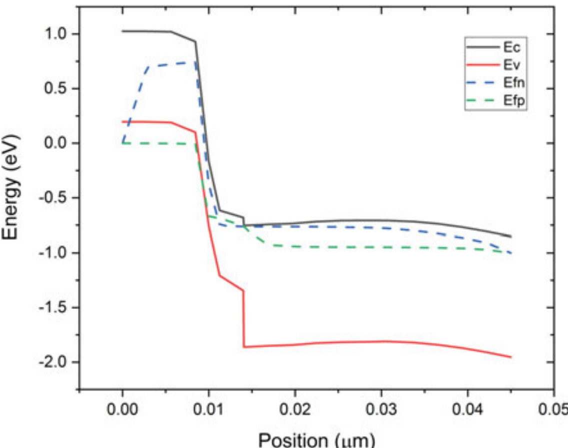

Fig. 4 Energy band diagram of proposed Ge-Pocket ADGTFET in on-state

reduction in ambipolar current in the proposed device structure. Figures 5 and 6 represent the transfer characteristics, and Fig. 7 represents total gate capacitance of Proposed Ge-pocket ADGTFET structure. Also, Fig. 8 represents the electric field in the proposed device from it can be inferred that the electric field in the tunnelling junction is high, resulting in high tunnelling probability. The on-state current is found out to be 390 μA/μm in the proposed device which is higher than DGTFET which was 2.9 μA/μm [12, 13]. The point subthreshold swing(SS) is found to be 5 mV/dec, and the average SS is 24.29 mV/dec when compared to DG TFET, it is significantly improved. The ambipolar current is found to be 1.8×10^{-17} A/μm.

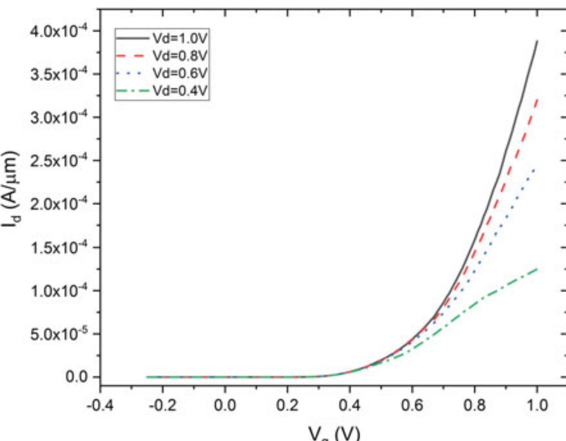

Fig. 5 Proposed Ge-Pocket ADGTFET transfer characteristics

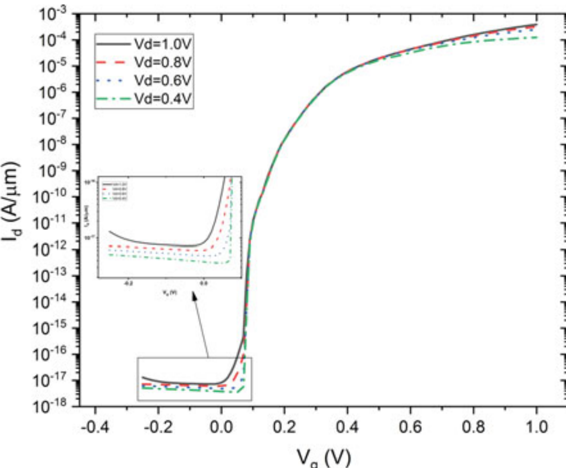

Fig. 6 Effect of V_g on I_d ($\log_{10}$scale) in proposed Ge-Pocket ADGTFET

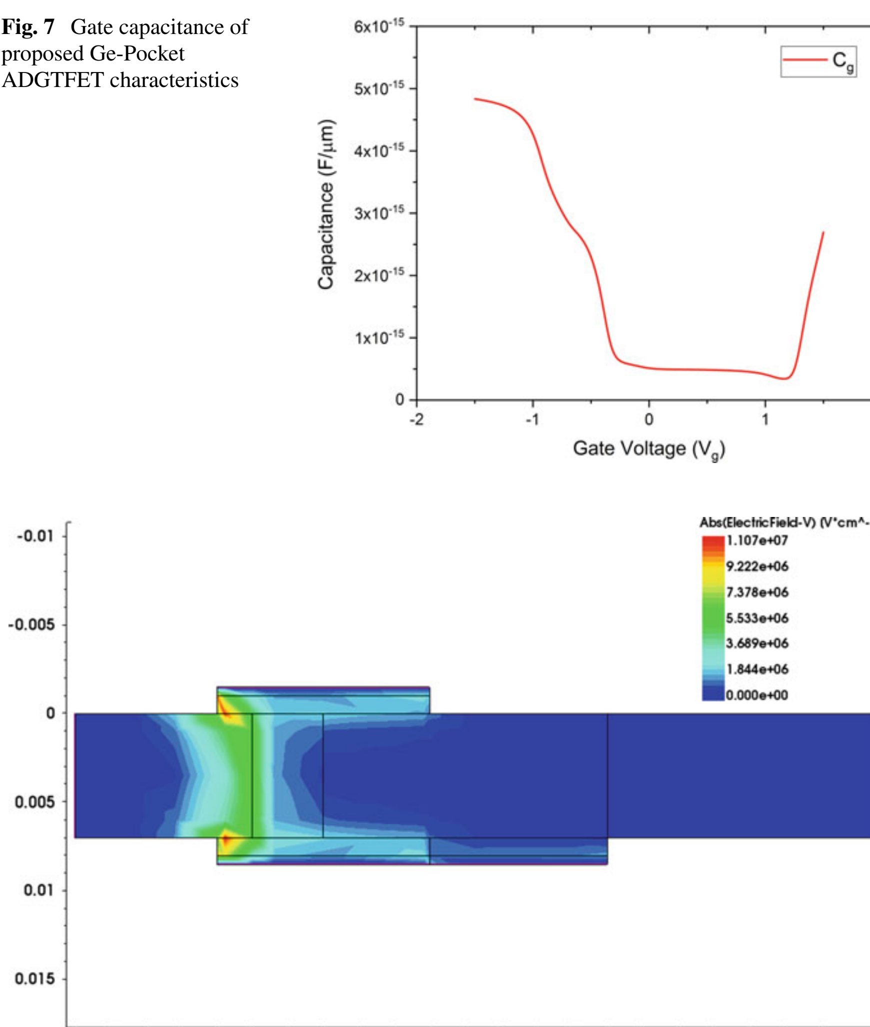

Fig. 7 Gate capacitance of proposed Ge-Pocket ADGTFET characteristics

Fig. 8 Electric field in proposed Ge-Pocket ADGTFET characteristics

4 Conclusion

A TFET designed with asymmetric dielectric and a pocket structure for enhancing electric field across the tunnel junction exhibiting SS of 5 mV/dec is presented with an I_{ON}/I_{OFF} ratio of 1×10^{12} for 1 V operation. The use of germanium has improved the tunnelling efficiency across the junction. This pocket Ge structure along with hetero-asymmetric dielectric results in better gate control across the tunnel junction. The asymmetric dielectric has resulted in the much lesser electric field across the

channel drain interface and thus, effectively reduces leakage current along with the reduction in leakage. The structure is very similar to the existing structures, and thus, fabricating it will be comparatively easier. This work highlights only the theoretical simulation of the proposed structure and has a scope of further analysis.

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Investigation of Electrical Parameters and Low-Frequency Noise Analysis of a Heterojunction TFET

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Abstract This work demonstrates the influence of electrical noise in a dual dielectric pocket heterojunction silicon-on-insulator (SOI) tunnel field-effect transistor (TFET). Electrical noise behavior is analyzed by considering the low-frequency noise component, flicker noise to remark on reliability aspects of the device. The impact of characteristic deviation is also investigated for various electrical parameters. Further, the device characteristic is explored under the influence of various design parameters.

1 Introduction

The continuous escalation of power dissipation stands out as a principal road block in the growth of microelectronics industry. This has led to the demand of severe attention with regard to low-power and applications which are compatible for energy efficiency. Further, the attempt to maintain the integrity of Moore's Law as well as to offer enhanced performance along with cost maintenance has led to the dawn of several innovative semiconductor devices which can survive scaling down trend [1]. Metal oxide semiconductor field-effect transistors (MOSFETs) owing to various short channel effects (SCE's), subthreshold swing limitation are on a trail of replacement as an efficient device for low-power applicability [2, 3]. MOSFET has a subthreshold slope (SS) limit of 60 mV/dec at 300 K due to its thermionic emission constraint. Various structures and designs with different materials have been investigated to enhance the overall performance of the TFETs. TFETs have evolved as potential device in this matter. The unconventional phenomenon of band-to-band tunneling (BTBT) inherent in TFET facilitates sub-60 mV/dec SS and reduced OFF state current (I_{OFF}) [4, 5]. However, despite a suitable ratio of I_{ON} and I_{OFF} is achieved by TFET, yet TFETs suffer from low I_{ON} issues. To combat such effects numerous innovative architectural designs like double gate TFET [6], silicon on insulator (SOI) TFET [7], dual material gate TFET [8], heterojunction TFET [9], PNPN TFET [10],

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nano-ribbon TFET [11], and cylindrical TFET [12] have been introduced in order to assure reliable performance for commercial utility.

However, when reliability of a device is a concern, the effect of noise on nanoscale regime is utmost important. The behavior of various TFET architectures in the presence of noise is not much inspected in comparison with investigation of other electrical factors. The causes of low-frequency noise, such as the flicker noise and random-telegraph noise (RTN), degrade the behavior of both analog and mixed-mode circuit along with semiconductor-based memories [9, 13].

In this brief, a heterojunction-SOI TFET with double dielectric pocket is presented. High-k dielectric is utilized as gate oxide to enhance ON current. Dielectric pocket enhances the effectiveness of device and makes the design well-suited for upcoming low-power applications [14]. SOI TFET provides lower effect of parasitic capacitance due to isolation of silicon (Si)-body and enhances switching-speed. Electrical parametric variation in the considered device along with inspection of noise characteristic considering current spectral density of noise. The paper starts with a description on basic working principle and considered device architecture in Sect. 2. The simulation scenario is defined in Sect. 3. The results and their discussions are outlined in Sect. 4. Lastly, the conclusion is deliberated in Sect. 5.

2 Working Principle

MOSFET operates on the principle of charge modulation in the channel, whereas TFET operates on the principle of potential variation which allows or prevents the mechanism of tunneling. In TFET, on applying positive gate voltage (V_{GS}) corresponding energy band on the channel gets suppressed, narrowing the energy-barrier between source and channel. The gate voltage of TFETs is varied until the valence band (VB) at source and conduction band (CB) at the channel is aligned. This allows flow of current throughout the device. BTBT is employed by TFET to drive its current, whereby charge carriers are allowed to tunnel across a potential barrier between VB and the CB. TFET is principally a reverse biased p-i-n diode. A reverse biased diode can carry large amount of current by different mechanisms like BTBT, impact ionization, and thermal instability [15]. The basic difference between MOSFET and TFET is the current control mechanism. BTBT and TFET switch to OFF state. In this state, electrons in the valence band of source do not have any available energy states in the channel where electron tunneling can occur.

TFET is advantageous over conventional MOSFETs due to low subthreshold swing (SS) and low leakage current. This guarantees high ON–OFF ratio as well as low dissipation per device to facilitate to memory applications. There is limitation of V_{DD} and V_T scaling in modern scaling [19]. The variation of leakage energy (E_L) and dynamic energy (E_{DYN}) with changes in voltage supplied for TFET and MOSFET is presented, where E_L and E_{DYN} are related as given by Eqs. (1) and (2),

$$E_{\mathrm{DYN}} \propto V_{\mathrm{DD}}^2 \tag{1}$$

$$E_{\mathrm{DYN}} \propto V_{\mathrm{DD}}^2 \tag{2}$$

Therefore, it is clearly seen that both E_L and E_{DYN} are proportional to V_{DD}^2. In addition, E_L is exponentially dependent on SS. Therefore, leakage energy will decrease with SS reduction. It is also known that V_{DD} cannot be scaled beyond certain extent in modern scaling. This has fueled the need of new device with lower SS. TFET facilitate such characteristics. Therefore, TFET provides lower total energy in comparison with conventional MOSFETs [17]. The phenomenon of BTBT in TFETs can be approximated by Wentzel, Kramer's and Brillouin (WKB) approximation [17]. The tunnel barrier is deliberated as a potential barrier with triangular shape. According to WKB approximation,

$$T = \exp\left[-\frac{4}{3}\frac{\sqrt{2m*}}{qF\hbar}(E_g)\,E_g^{\frac{3}{2}}\right] \tag{3}$$

In Eq. (1), $m*$ is the effective electron mass, $\hbar$ is basically Planck's constant divided by $2 \times 2\pi$, E_g is semiconductor material bandgap and F is electric field measured in V/m.

The BTBT rate (G_t) is expressed as [9]

$$G_t = A\frac{|F|^2}{E_g}\exp\left(-B\frac{E_g^{1.5}}{|F|}\right) \tag{4}$$

where A and B are constants and E_g is bandgap.

In this work, a heterojunction TFET with double dielectric pocket designed on SOI has been considered. The considered 2D architecture is presented in Fig. 1. A high-k dielectric gate configuration with δp^+ $Si_{1-x}Ge_x$ layer present at the between interface of source and the channel offers enhanced I_{ON}. The structure comprises of twofold dielectric pockets each at source-channel and drain-channel junction to permit reliable operation providing for low-power applications high I_{ON}, low I_{OFF}, steeper SS, low threshold voltage (V_{th}) and reduced parasitic capacitance in comparison with conventional TFETs [18].

3 Simulation Format

The simulation work has been performed utilizing Sentaurus 2-D technology computer aided design (TCAD) simulator that commercial accessibility [19]. Fermi–Dirac statistics is employed as an alternative of Boltzmann statistics owing to the use of higher doping concentration in both source and drain. This elevated rate of doping concentration utilized causes bandgap narrowing in semiconductor materials. Bandgap narrowing model (OldSlotBoom) is activated as the likelihood of tunneling

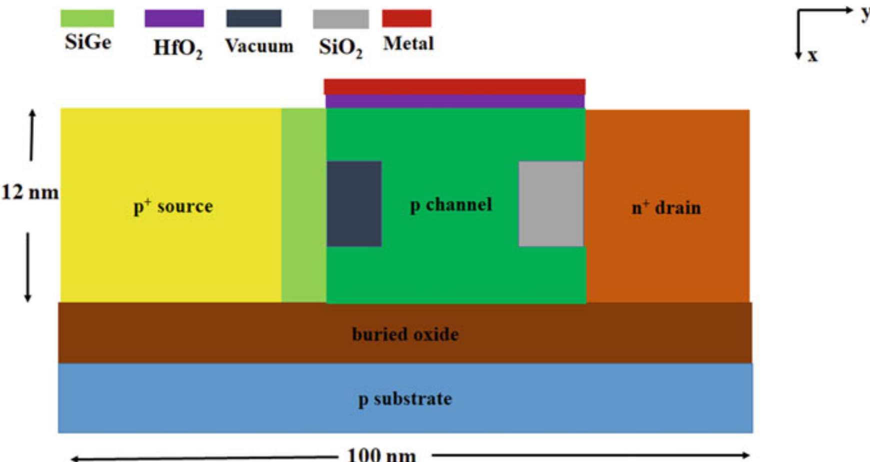

Fig. 1 2D structure of the proposed SOI TFET

depends on bandgap at tunneling junction. A doping-dependent model is employed to take account of the effect of doping concentration on carrier mobility. Non-local BTBT model is initiated to evaluate the effect of inter-band tunneling of TFETs in lateral direction further effectively. Shockley-read-hall recombination model is also activated. The electrical noise behavior is investigated by taking into consideration the low-frequency source that is flicker noise.

4 Results and Discussion

The various results extracted from this work are elaborated in this section.

4.1 Effect of Drain Bias

The impact of variation in drain bias (V_{DS}) on the transfer characteristic of the proposed heterojunction-TFET has been evaluated and offered as Fig. 2. It has been observed that the change in V_{DS} has affected the I_{OFF} only and the I_{ON} remains almost intact. With increase in V_{DS}, the Fermi potential rises to cause a gradual decline in inversion charge of channel along with high rate of BTBT generation owing to improved electric field. This phenomenon is comparable to rise in V_{GS} which has prominent influence in OFF condition. On the other hand, in the ON condition, high V_{GS} rises BTBT more prominently, acting as the prime controlling parameter and thus, V_{DS} does not control the I_{ON} [20]. However, a trade-off needs to be adjusted for V_{TH} for low I_{OFF} to maintain low static power dissipation. The V_{TH}

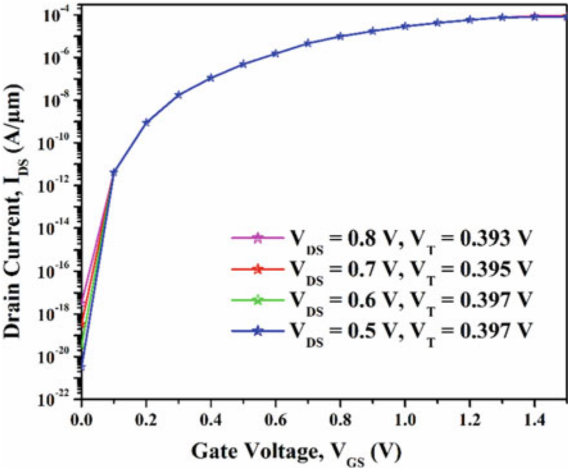

Fig. 2 Transfer characteristic of the heterojunction TFET for different V_{DS}

is obtained by constant current method [21] and indicated in Fig. 2. It is observed that V_{TH} reflects almost fixed value for different V_{DS}. A key challenge faced with the downscaling of conventional MOSFETs is Drain-induced barrier lowering (DIBL) as given by Eq. (5)

$$\text{DIBL} = (V_{TH1} - V_{TH2})/(V_{DS2} - V_{DS1}) \tag{5}$$

Here V_{TH1} and V_{TH2} are the threshold voltages obtained for drain bias of V_{DS1} and V_{DS2}, respectively. The DIBL is calculated considering V_{DS} of 0.5 V and 0.8 Vas V_{DS1} and V_{DS2}. It is found to be 0.01333 mV/V that seems a negligible value. This fundamentally indicates that the DIBL free effect.

4.2 *Effect of Source Doping*

The transfer characteristic behavior of the proposed heterojunction TFET considering variation in source doping concentration is presented in Fig. 3. Here, the doping concentration of drain has been fixed at 5×10^{18} cm^{-3}. The source doping concentration has been changed from 1×10^{18} cm^{-3} to 5×10^{19} cm^{-3}. It is observed from Fig. 3 that the I_{ON} gets enhanced for higher source doping. The higher value of I_{ON} is reflected at high source doping owing to reduction in tunneling width which further causes increased tunneling rate of electrons [22]. The source doping plays a noteworthy part in line tunneling in the considered TFET structure. Thus, a highest I_{ON} of 9.993×10^{-5} A/µm is obtained for source doping concentration of 5×10^{19} cm^{-3} compared to I_{ON} of 1.02×10^{-5} A/µm is obtained for source doping concentration of 1×10^{18} cm^{-3}.

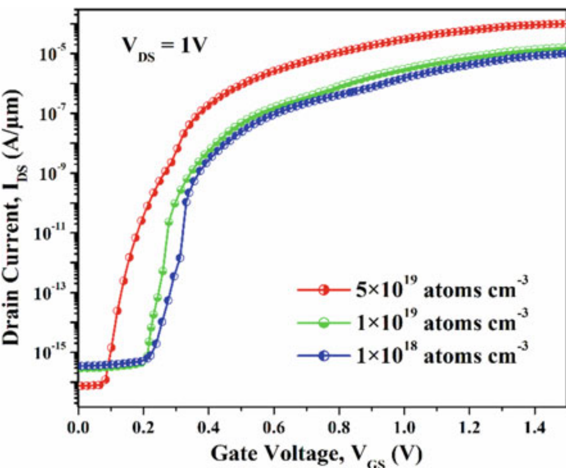

Fig. 3 Influence of source doping on the transfer characteristic of the heterojunction TFET

4.3 *Effect of Silicon Body Thickness*

The effect of varying thickness of Si body ($T_{\text{Si-body}}$) at $V_{DS} = 1$ V is presented in Fig. 4. The TFET characteristic is found to be sensitive to this parameter, $T_{\text{Si-body}}$. It has been observed that I_{ON} degrades for thicker body due to the reduction in tunneling probability [23]. Thus, thin $T_{\text{Si-body}}$ is preferred for enhanced performance. The maximum BTBT appears at the junction between source/channel near the Si-oxide interface [9]. Thus, the impact of reduction in $T_{\text{Si-body}}$ does not influence the BTBT rate expressively up until the area of noteworthy BTBT is touched. Hence, the impact of variation in is observed to be more at higher V_{GS}.

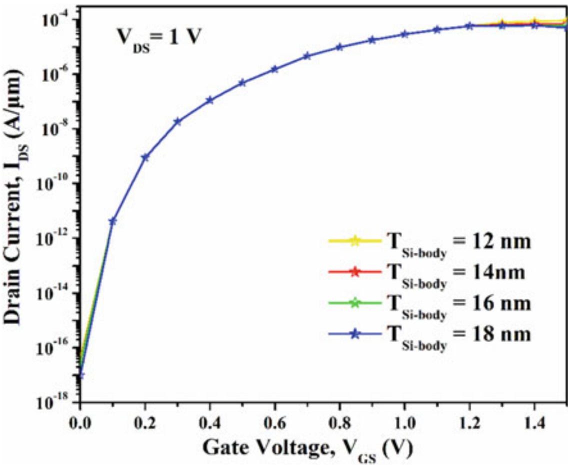

Fig. 4 Impact of varying body thickness on transfer characteristic of the heterojunction TFET

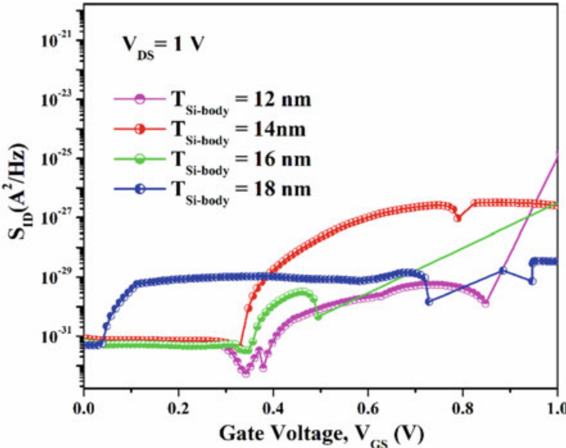

Fig. 5 Impact of varying S_{ID} versus gate voltage behavior for varying $T_{Si\text{-body}}$

4.4 Influence of Current Noise-Spectral Density on Si Body Thickness

The influence of current noise-spectral density (S_{ID}) on varying $T_{Si\text{-body}}$ is observed and presented in Fig. 4. Here, the low-frequency noise component, Flicker noise, is considered for the analysis. The addition of numerous generation–recombination centers has an outcome of flicker noise [24–26]. The current noise-spectral density of flicker noise is given by Eq. (6),

$$S_{ID}(f) = \left(\frac{2}{F} + \frac{B}{F^2}\right)\frac{q^2 I_D^2 N_t(E_{FN})}{\varepsilon_{ox}^2 W L' \alpha f^{\gamma}} \tag{6}$$

where F is electric field, B is a constant, I_D is drain current, $N_t(E_{FN})$ is interface-trap, L' is effective gate length, W is gate width, α is attenuation factor, ε_{ox} is dielectric constant of gate oxide, f is frequency, and γ define how S_{ID} relies upon frequency [13]. It has been observed from Fig. 5 that the S_{ID} behavior has rising trend for thinner $T_{Si\text{-body}}$ at higher value of gate voltage owing to the fact that BTBT is not affected until significant V_{GS} is reached as already explained in Sect. 3. Further, from Eq. (4), it is also reflected that S_{ID} is directly proportional to I_{DS}. Thus, S_{ID} behavior in Fig. 5 follows a trend similar to Fig. 4.

5 Conclusion

In this paper, a twofold dielectric pocket heterojunction TFET has been proposed. Hetero-dielectric gate configuration and a δp + $Si_{1-x}Ge_x$ layer near source-channel

junction are adopted to offer enhanced I_{ON}. The device is examined for various parametric variations and their various impacts are studied. The device is investigated for different drain bias conditions, impact of various source doping concentration, and different Si body thicknesses. Further, to analyze the reliability aspect of the device, electrical noise behavior is also investigated. To guarantee optimum dominance of a device performance, investigation of electrical noise is very essential, although this area is less explored yet. Noise analysis of TFET is extremely important to judge the superiority of a device. It is because different frequency noise sources seem to be severe obstacles for analog/RF application of a device.

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Design and Fabrication of a Cost-Effective, Electrochemical Detection-Based, Polymeric Capillary-Electrophoresis Microfluidic Devices for Diverse Bioanalytical Functions

Amit Prabhakar, Deepti Verma, Nimisha Roy, Prashant Nayak, and Soumyo Mukherji

Abstract In recent decades, Micro-total analytical systems (μ-TAS)/lab-on-chip devices with the electrochemical detection scheme have attracted much attention owing to their label-free detection capability and cost-effective instrumentation. In situations like a pandemic, these detection systems become all the more relevant. However, cost-effective microfabrication technique and proper electrode alignment with the microchannel remain a huge challenge. To resolve these issues through a novel approach, we present an efficient and cost-effective method of fabricating various micro-total-analysis systems, employing a fully integrated end-column electrochemical detection (ED) system. In this study, various substrates used while fabricating the microchannel substrates were Glass, Silicon, Polymethyl Methacrylate (PMMA)-sheet, Disposable syringes, micropipette tip, etc. These were finally integrated and aligned at their end-columns with the conductivity electrodes. The microchannels and the spaces for linear-alignment of working-electrode with the channel were fabricated using a simple and single-step process of casting the Polydimethylsiloxane (PDMS) polymer on a micro-scale template like metal wire/nylon thread, and electrode-space-shaping elements, and releasing of all intended microstructures of devices, in a certain prescribed manner. Due to the simplicity of the single-step fabrication-processes, the microdevices production was quite repeatable without any possible failure resulting in identical dimension fluidic-chips each time, provided that the same sized fabrication-templates were utilized for these procedures.

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The microelectrode alignment with microchannel endings was efficiently proved by using a simple detection-circuit.

Keywords Microfabrication · Lab-on-chip · Micro-total analytical system · Capillary electrophoresis · Microfluidic device · Cost-effective microfabrication · End-column electrode alignment · Electrochemical detection circuit · Multiple-substrates for microchannel · Electropherogram

1 Introduction

Micro-total analysis systems (μ-TAS) are the current trend in analytical chemistry [1]. They have gained immense importance in recent decades due to their sensitivity, portability, low reagent consumption, and simplicity. Also, meticulous consideration has been offered to capillary electrophoresis (CE) microchips owing to its reward over usual analysis methods, such as speedy separation, elevated separation competence, small reagent utilization, reduced waste production, utilization of power, easy disposal, and portability [2–5]. Until now, the micro-total analysis system has been advanced sophisticated, and functional to rectify a multiplicity of chemical/biological analytical issues [4].

In a recent study, the Lego toy concept was used to design a novel capillary electrophoresis device coupled with laser-induced fluorescence (LIF) detection. These devices provide the scope of high standardization by the user devoid workshop facilities [6]. Laser-induced fluorescence (LIF) [7] has been a predominant detection mode. However, the key downside that prevents the integration of LIF with the microchips is the requirement of bulky and complex optical device components. A microchip-based CE–ED system for indirect electrochemical detection of DNA was reported by Woolley et al. [8], and this detection approach has presented an immense potential for contriving autonomous and not reusable TAS. Adamski et al. proposed the application of 3D printing for fabricating a gel-electrophoresis lab-on-a-chip device. With a separation capability of 50/800 bp DNA ladder, this device consisted of all the requisite compartments like sample injection and sample separation microchannels of 20 mm and 50 mm length, respectively [9].

Ruecha et al. demonstrated a rapid direct amperometric quantification of cholesterol utilizing PDMS microchip capillary electrophoresis based on a combination of electrochemical detection and enzymatic assay [10]. Wei et al. developed a low-cost thin polyester thread-based microfluidic platform, instead of a liquid separation channel, based on electrophoresis separation and electrochemical (EC) detection [11]. In another work, Wei et al. developed a novel concave 3D sensing electrodes that considerably enhanced the sensing performance of thread-based microfluidic devices for capillary electrophoresis electrochemical detection [12]. Horng et al. fabricated a microchannel on PMMA substrate using a novel method where screen printed electrodes were used to demonstrate the electrophoretic functions to quantify uric acid and L-ascorbic acid in human urine [13]. Several reviews [8, 14, 15] have

been available since the first description on a capillary electrophoresis chip with integrated amperometric detection [8].

In the initial years, majorly silicon and glass were utilized to fabricate microfluidic devices using photolithography followed by dry or wet etching procedure [16, 17]. In recent years, polymeric microchips are of growing attention since they can present striking mechanical and chemical properties, inexpensive, simplicity of fabrication, biocompatibility, and elevated elasticity [18, 19]. Some commonly employed polymeric materials used in the fabrication of microfluidic devices include polycarbonate [5], Polydimethylsiloxane (PDMS) [20], polyethylene terephthalate (PET)[21], Polymethyl methacrylate) (PMMA) [21], and Polystyrene (PS) [22], etc. Usually, these polymeric chips including CE-ED systems are fabricated using a two-step process. Initially in this process, an open microchannel is fabricated using photolithography, soft-lithography [20], compression-moulding [14], hot-embossing [23], imprinting [24], injection-moulding [25], and plasma-etching [26] techniques. Some recent studies have also reported the use of 3D printing to fabricate these devices. However, the 3D printing setup is not entirely cost-effective and is a bit complicated. The electrodes patterned on a flat substrate separately. Further, after proper alignment, this flat electrode patterned substrate is bonded to an open channel containing a microchip so that all electrodes should come inside the periphery of the separation channel ending [27]. Here, the alignment of the working electrode with microchannel is a major cause of concern [28] and to tackle this issue an external X, Y, Z positioner becomes necessary. In a recent study, it was concluded that 3d printed microdevice for electrophoresis analysis showed nearly the same or even reduced performance as compared to conventional microfluidic devices [29]. Recently, fabrication of an amperometric flow-injection Microfluidic Biosensor, based on *Laccase* for in situ determination of *Phenolic* Compounds [30], as well as electrochemical detection based on nanomaterials in CE [31] has been reported; however, problem related to microfabrication is a major cause of concern in all these approaches.

Although few similar approaches have been reported recently [32], none of them addressed the electrode alignment issues for electrochemical detection devices. Table 1 gives a brief account of various approaches that have been used to develop capillary electrophoresis microdevices for diverse bioanalytical functions.

In this paper, new cost-effective techniques for fabricating different types of electrochemical-detection-based CE micro-fluidics chips have been discussed.

2 Device Design and Fabrication

PDMS (Sylgard 184, Dow Corning) polymer was used to fabricate microchannel. Vacuum grease, in addition to chloroform, was used as the polymer swelling agent to easily release the wire or nylon thread, during the proposed microfabrication process. Moreover, PMMA sheets, silicon wafers, polyethylene containers, disposable-syringes, Polypropylene Micropipette Tip (MPT) of 1000 μL volume, and syringe-needles were used as cost-effective substrates to cast the PDMS-prepolymer

Table 1 A comparative account of various microfluidic approaches to design capillary electrophoresis detection devices

Techniques	Pros	Cons
Thread-based (nylon, polyester, etc.)	Simple, low cost, many options for electrode alignment, limit of detection	In a few cases, electrode alignment is disturbed by temperature variations
3D printing	Precise control over microchannel geometry	Lengthy procedures like 3D printer calibration, resin pretreatment and printer preparation, not much improvement in device performance
Photolithography	Highly reproducible, facile	Channels have a rectangular geometry, cumbersome and require expensive cleanroom facilities
Paper-based	Simple, portable, low cost	Require hydrophobic barrier patterning

into diverse microfluidic devices. The electrodes(Cu, Ag/AgCl and copper/platinum electrode) to be used in the experimental setup were also developed and designed using a cost-effective technique (Fig. 1).

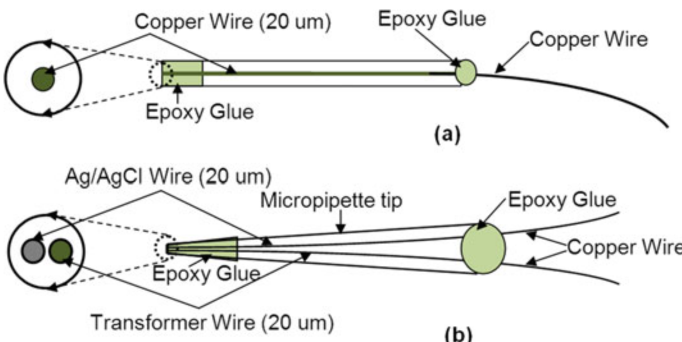

Fig. 1 Schematic diagram of a cost-effective **a** single copper wire electrode; and **b** dual-electrode, with copper/platinum-wire (working electrode) and Ag/AgCl wire (reference-electrode)

2.1 *Microchannel Fabrication and Electrode Integration*

2.1.1 Plain Microchannel Inside MPT for Easy End Column Electrode Alignment

In a unique approach, a PDMS microchannel was fabricated inside the pool-space created by coupling two micropipette tips along with their wider bases (Fig. 2).

2.1.2 Cross-Shaped Microchannel Arrangement with End Column Electrode Alignment Space

Figure 3 explains in detail the fabrication of a cross-shaped microchannel arrangement.

2.1.3 Y- or T-Shaped Microchannel Arrangement and End Column Electrode Alignment Space

This section explains the fabrication of three reservoirs based on Y- or T-shaped microchannel arrangement along with the alignment working electrode to a channel (as shown in Fig. 4).

2.1.4 Microchannel Inside a Disposable-Syringe Substrate, and Aligned End Column Electrode

The fabrication of a PDMS microchannel inside a perpendicularly placed disposable-syringe substrate integrated with the electrode sensing tip at the end of the microchannel is mentioned in this section (Fig. 5).

2.1.5 Microchannel Inside a Disposable-Syringe Substrate, and Coupled End Column Electrode Alignment Space

Here, the micropipette tip (MPT) was incised from its tip side (of length: 1 cm) and placed inside the through-hole of 3 mm diameter made in the plastic-piston of the Polypropylene disposable syringes of volume 5 ml and length 8 cm (Fig. 6).

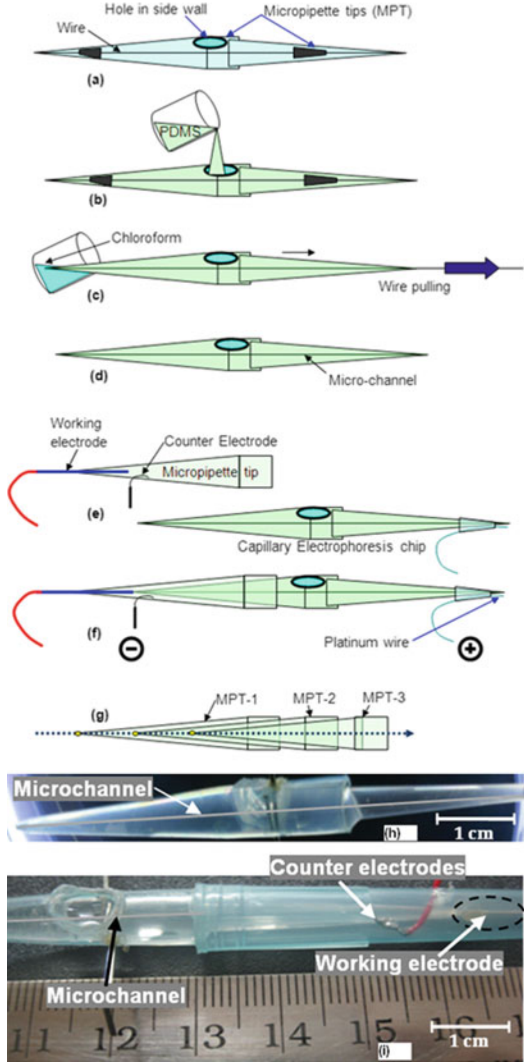

Fig. 2 **a** Two MPT coupled/glued through its respective wider-base to form an MPT-pool for PDMS-polymer casting. A metal-wire template of 50 μm diameter was stretched across the MPT-tip and a through-hole was created on the wall of the micropipette tip for pouring the mixture of PDMS prepolymer and curing agent. **b** a mixture of Sylgard 184 elastomer and curing agent (9:1 ratio) was poured into the MPT-pool and cross-linked by curing at 70 °C for about 40 min. **c** Wire-template was removed out of the semi-cured PDMS block via pulling, **d** Cured for another 40 min at 70 °C, **e** Working electrode for electrochemical detection were attached through another micropipette tip (i.e., *detection reservoir*-MPT) after its proper alignment with the tip of the microchannel, **f** Counter electrode was attached from sidewalls of *detection reservoir*-MPT along with electrophoresis electrode at the tip of the channel. **g** Three MPT joined in succession, which shows the co-linear arrangement of its MPT-tip. **h** Photograph of the final MPT structure containing microchannel. **I** Photograph of the microchannel coupled with another *detection reservoir*-MPT containing electrodes for EC detection of the analyte

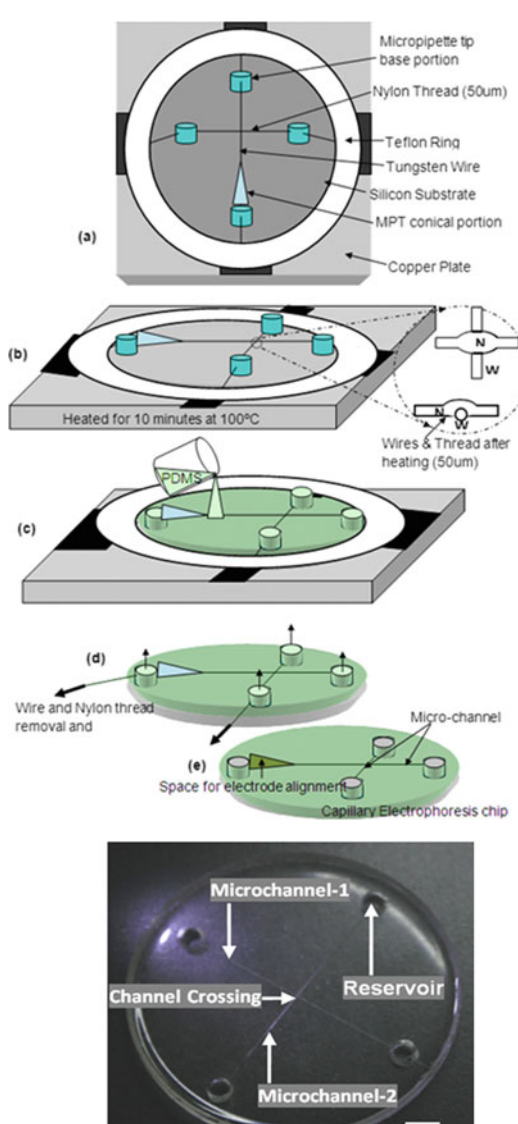

Fig. 3 **a** The BMPT & TMPT inserted metal wire *(W)* and nylon thread *(N)* were stretched in a criss-cross fashion, on the cleaned flat glass/silicon substrate; **b** The whole assembly was heated at 100 ºC for 10 min; **c** Mixture of Sylgard 184 elastomer and its curing agent (9:1 by weight ratio) was poured on the whole assembly and cured at 70 °C for about 40 min. **d** *(W)* and *(N)* templates were removed out of the semi-cured PDMS block via pulling; **e** Additionally, cured for another 40 min at 70 °C; **f** Photograph of the microfluidic chip with the cross-shaped microchannel

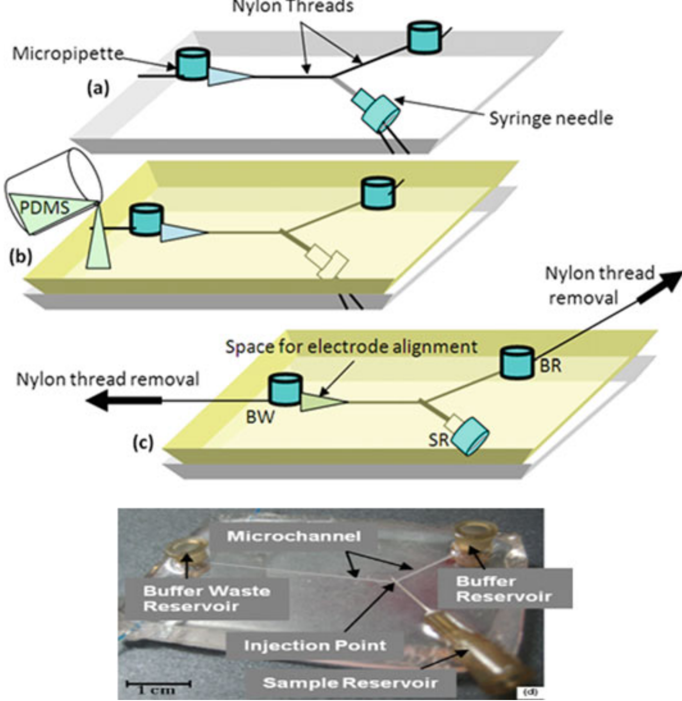

Fig. 4 **a** Two BMPT were incised and inserted in through-hole in PMMA sheet, called buffer reservoir (BR) & buffer waste reservoir (BWR), respectively. Two metal wires/nylon threads templates were separately passed through each of the two BMPT. Another end of both templates was inserted in syringe-needle through the needle tip portion so that it comes out of another end of the needle. The needle and the templates were stretched across the PMMA substrate in a Y-shaped fashion in between BR, BWR, and injection point using cello tape **b** Sylgard 184 elastomer prepolymer liquid was poured on it and cross-linked by curing it at 70 °C for about 40 min. **c** metal wires/nylon threads templates were removed out of the semi-cured PDMS block by pulling and Cured for another 40 min at 70 °C; **d** Photograph of the microfluidic chip with Y-shaped microchannel

3 Experimental Setup

3.1 End Column Detection of the Analyte *Detection Instrumentation*

A simple detection circuit for current to voltage conversion is explained in Fig. 7. Here, the feedback-resistance (R) is 1 M ohm and, ‘C’ and ‘A’ are cathode and anode, respectively.

As in biosensing enzyme–substrate reaction (e.g., while the substrate: glucose analyte interacts with enzyme: glucose-oxidase), the released electro-active species (i.e., hydrogen peroxide) is in nanomolar concentrations; hence, during its oxidation

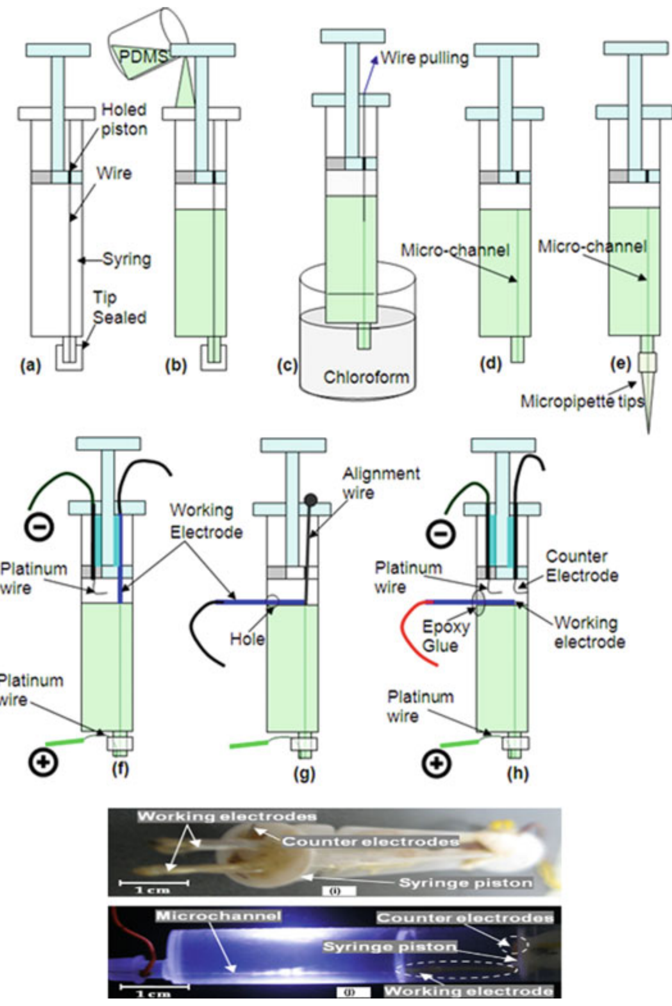

Fig. 5 **a** Tungsten metal-wire stretched between the sealed aperture of a disposable-syringe and the pin-holed plastic-piston of the same disposable-syringe; **b** PDMS mixture poured and cured at 70 °C for about 40 min; **c** Metal-wire were removed out of the semi-cured PDMS-block via normal pulling process, while keeping syringe tip dipped in the chloroform solvent; **d** The released microchannel was cured at 70 °C for another 40 min; **e** MPT coupled at the tip of a disposable-syringe to increase the separation-length of microchannel for the electrophoresis process; **f** Electrodes for the electrochemical detection process were inserted and attached through the piston side after their proper alignment; **g** Electrodes for electrochemical detection (EC) process were inserted through the through-holes created in the sidewalls of the disposable-syringe, after their proper alignment via alignment-wire; **h** The counter electrode was attached along with electrophoresis-electrode, in to the plastic-piston; **i** Photograph of syringe plastic-piston, containing electrodes for EC detection process. **j** Photograph of the microchannel coupled with electrodes for the EC detection of analytes

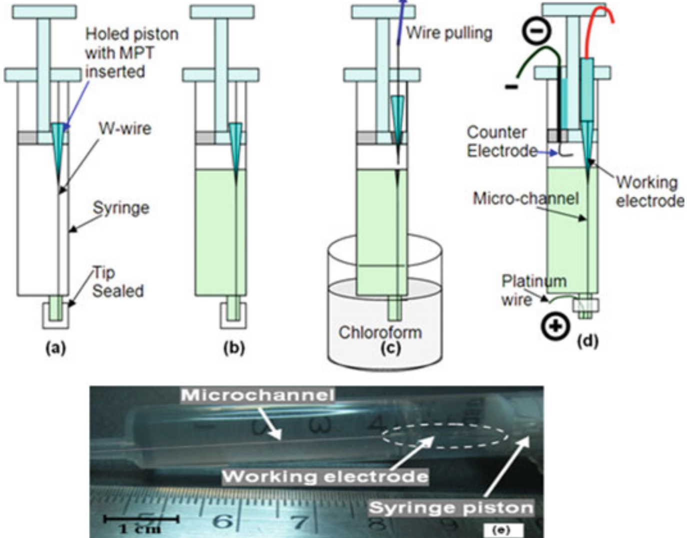

Fig. 6 **a** Tungsten metal-wire was stretched between sealed aperture of disposable-syringe and tip of micropipette tip (TMPT) incised, inserted and glued in a through-holed plastic-piston of the same disposable-syringe; **b** Mixture of Sylgard-184 elastomer and its curing agent (in ration of 10:1 w/w) was poured via the through-hole created in the plastic-piston side, and cured at 70 °C for about 40 min; **c** Metal wire was removed out of the semi-cured PDMS-block via normal pulling process, while keeping syringe tip dipped in the chloroform solvent; **d** The released microchannel and *electrode alignment space* were cured at 70 °C for another 40 min; and working electrodes for electrochemical detection were fabricated via using the same TMPT glued in holed piston, Counter electrode was also attached along with electrophoresis electrode. **e** Photograph of the microchannel coupled with the electrodes (attached to syringe piston) for EC detection of the analyte

reaction at the anode (Eq. 1), the current produced is in the order of nano-ampere. For the oxidation of hydrogen peroxide at the anode, a stable voltage of about 650 mV needs to be applied between the anode and cathode to obtain an oxidation–reduction current. The detection-circuit was designed in a way that we can change the voltage in ranges of -2.5 to $+2.5$ V, in between both the electrodes. Two Zener-diodes (Zener voltage $= 2.5$ V) were connected serially at one end and connected to suitable resistances, at the other ends. The other end of each of the resistance was connected to the +Vcc and −Vcc of the Op-amps, respectively. The connection-point between the Zener-diodes was coupled to the electrical-ground. Also, a trimming-potentiometer was connected parallel to the two connected Zener-diodes. The wiper of trimming-potentiometer was connected to the cathode, to offer it a different voltage of 650 mV, concerning the anode (the reference-electrode), which was connected to the inverting end of the Op-amps.

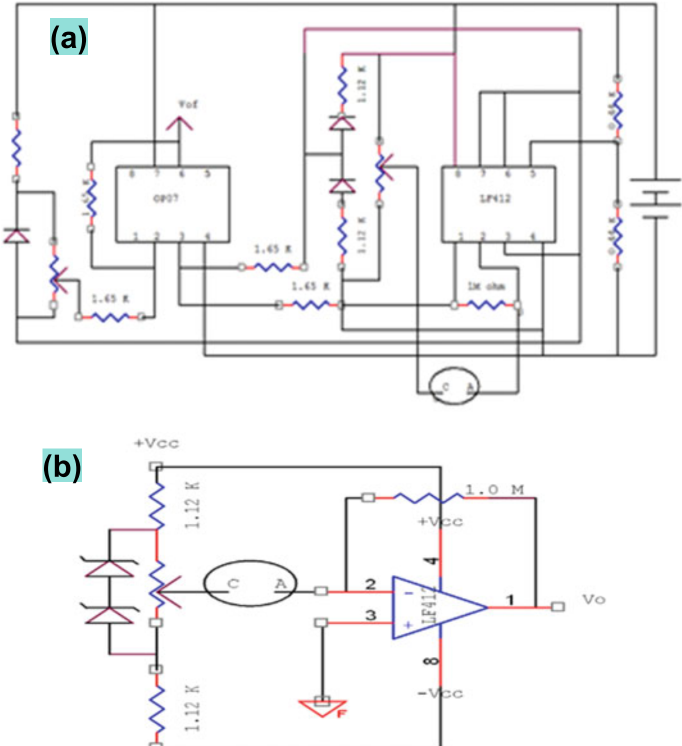

Fig. 7 **a** Showing circuit diagram of complete instrumentation part for current to voltage conversion, needed for EC detection; **b** Circuit diagram of current to voltage conversion unit used for the electrochemical detection of analyte at end column

4 Results and Discussion

4.1 Detection of Analyte

Figure 8a describes the experimental setup which includes two syringe pumps to sequentially pump hydrogen peroxide and DI-water into the two in-let of Y-shape microchannel of the device. A 650 mV voltage was applied, which caused the oxidation of hydrogen peroxide at the anode. As a result, an oxidation–reduction current proportional to the diffused hydrogen peroxide was generated. Figure 8b represents the related variation in voltage output concerning the introduction of different concentrations. The reaction at the anode may be explained as below:

Anodic reaction:

$$H_2O_2 \xrightarrow{\text{650mv versus Cathode}} O_2 + 2H^+ + 2e^- \quad (1)$$

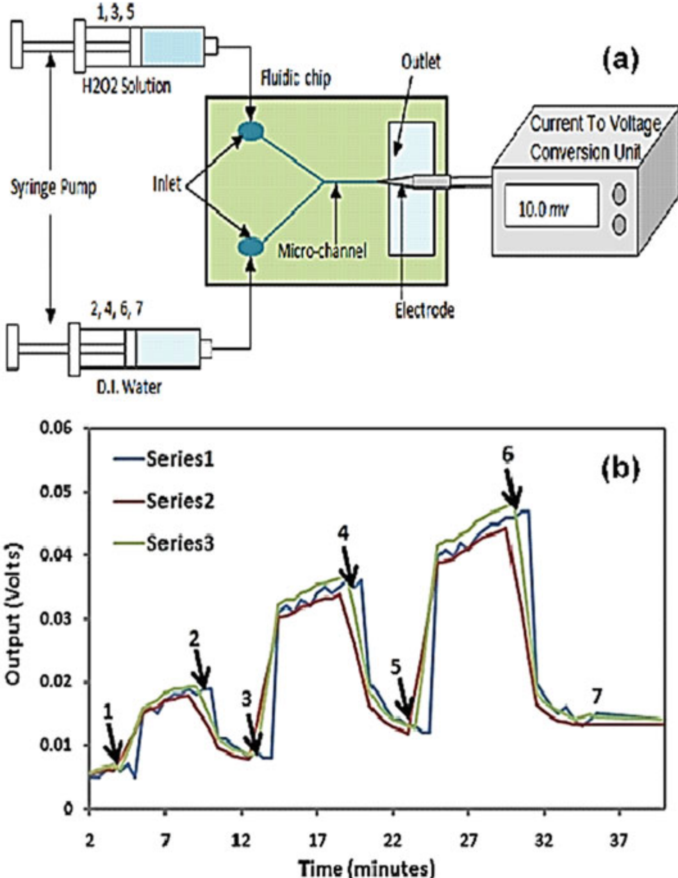

Fig. 8 **a** Schematic of the experimental setup for confirming electrode alignment with the microchannel. **b** The graph represents the change in output voltage (Vo) with time after the channel of microdevice presented in Fig. 4 (series 1), and Fig. 3 (series 2 & 3) is introduced with different hydrogen peroxide concentrations of (1) 0.003%, (3) 0.01% and (5) 0.03%. In between each of the concentration introductions, the channel was flushed with water (2, 4, 6, 7)

4.2 End-Channel Amperometric Detection for Microchip Electrophoresis

Sample injection and electrophoretic separation were performed through the application of negative potentials of −1500 V to the BGE-reservoirs, and −1000 V to the sample reservoirs, while BGE-waste or sample-waste reservoirs were kept at the ground.

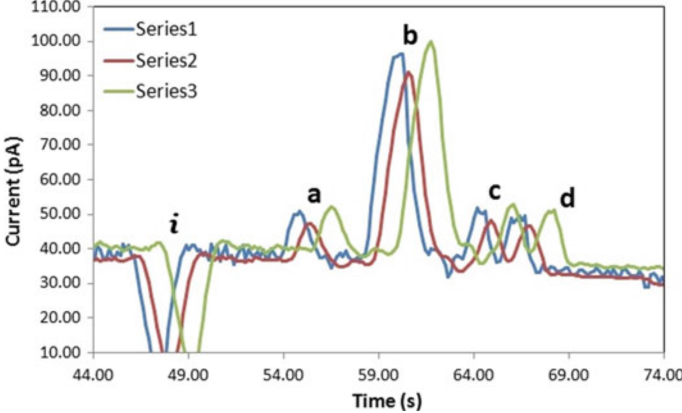

Fig. 9 Recorded electropherogram of an equimolar (5 μM) combination of **a** Sodium nitrite, **b** Tyrosine, **c** Hydrogen Peroxide, and **d** Ascorbic acid solution for device presented in figure-5 (series 1), figure-6 (series 2) and figure-2 (series 3). *i* Sample injection point, Conditions: BGE: 10 mM boric-acid with 2 mM TTAB attuned to pH 11 with 1 mM NaOH solution

Table 2 Approximate limit of detection for various analytes

Analyte	Limit of detection(μM)
1. Nitrile	~1.5
2. Hydrogen peroxide	~1.5
3. Tyrosine	~0.5
4. Ascorbic acid	~1.5

4.3 Separation Efficiency and Limit of Detection

The variations of baseline noise error were especially elevated (~35 nA), even with the superior resolution and sensitivity of end-channel detection in single-channel microchip electrophoresis (Fig. 9). The approximate limit of detection for various analytes at a signal to noise ratio of 4 is mentioned in Table 2.

5 Conclusion

The present study effectively demonstrates a cost-effective fabrication process for developing electrochemical-detection-based microfluidic devices of diverse geometries. The fabrication process may effectively be considered as cost-effective as it requires generally available fabrication-items, moderate semi-clean room facilities, lesser time, and minor skilled manpower. The proposed device fabrication process is single-step with competent repeatability in channel dimension, as well as working electrode placements at the microchannel endings.

Further, because of the cylindrical shape of the wire, the fabrication process provides a moderately circular microchannel geometry, which has certain other advantages over other generally microfabricated rectangular geometry. Additionally, as the proposed fabrication procedure is a one-step process, which does not require any oxygen plasma bonding step; hence, these channels may work at comparatively higher pressure without leakage. Also, as there is a uniformity of material in the microchannel, hence, increased dispersion phenomena between the bands can be avoided in electrophoresis processes. The inclusion of syringes as a substrate for casting the microchannel may be decisive for the field-portable filling of the microchannel with the requisite analyte/buffer solution in place of using the conventional bulky vacuum chamber coupled with the vacuum pump.

The alignment of microelectrode with the microchannel endings was validated by implementing a simple and efficient electrochemical detection circuit which revealed a change in its output voltage concerning a change in ionic concentration of the analyte in a region just adjacent to macrochannel endings. Further, the end-channel amperometric detection for microchip electrophoresis of sample mixture of nitrite, H_2O_2, Tyr, and AA was further experimentally validated for a few of the microchip designs.

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Morphological and Optical Analysis of GLAD Synthesize Vertically Oriented TiO_2 Nanowires on GaN Substrate for Optoelectronics Application

Rosy Kimneithem Haokip and Biraj Shougaijam

Abstract Highly efficient titanium oxide (TiO_2) nanowires (NWs) structures were synthesized from pressed and sintered titanium oxide (TiO_2) material on a gallium nitride (GaN) wafer inside e-beam evaporation chamber by employing glancing angle deposition (GLAD) technique. The morphological and chemical compositions were studied by the field emission scanning electron microscopy (FE-SEM) and energy dispersive X-ray spectroscopy (EDX). Our results indicated uniform growth and vertical nature of the NWs on GaN wafer. The average diameter of TiO_2 NWs is ~32 nm, and the length of the NWs is measured to be ~400 nm. The presence of titanium (Ti), nitrogen (N), gallium (Ga) and oxygen (O) was also evident from the analysis result. The growth mechanisms of TiO_2 nanowires (NWs) were also discussed in this work. The band gap of the deposited TiO_2 NWs obtained from photoluminescence analysis is ~3.3 eV. The peaks at 396.82 nm (~3.12 eV) and 450.83 nm (~2.75 eV) may be due to the presence of defects in the TiO_2. NWs. The deposited TiO_2 NWs on GaN substrate may be applicable for optoelectronics application.

Keywords FE-SEM · Glancing angle deposition technique (GLAD) · Nanowires (NWs) · Photoluminescence · TiO_2

1 Introduction

TiO_2 material has been widely used in photodetector applications [1–3] due to its low cost, riveting optical, electrical and chemical properties [4] such as large band gap of ~3.2 eV, high dielectric constant, high refractive index, high photosensitivity, high optical transmittance and transparency in visible region. Nanocrystalline structure of TiO_2 is highly stable at high temperatures and attracts great interest in gas sensor applications, light emitting diodes, solar cells and photocatalysis applications [5].

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Perpendicular TiO_2 NWs are highly photo-efficient attributed by its large surface-to-volume ratio [1] making it a potential tool in optoelectronic applications. TiO_2 NW-based devices restrict the accumulation of minority carriers at the electrode thereby reducing the overall noise [6]. Successful growth of high-density single crystalline structure of 1-D TiO_2 NWs on Ti/Glass substrate has been reported by Tsai et al. [7]. Many studies have been made to synthesize TiO_2 nanowires (NWs) using different deposition techniques such as thermal oxidation [8], hydrothermal [9], anodization method [10], sol gel [11], vapor liquid solid (VLS) [12], pulsed laser deposition [13] and electrospinning [14], in order to optimize the growth of TiO_2 NWs and nanorods. Al-Shabander et al. [15] observed uniform distribution and growth diameter of TiO_2 NWs and nanorods to be ~100 to ~200 nm in the presence of AAO template. However, the diameter of the TiO_2 nanorods was found to be ~100 nm after removal of AAO template. Santhi et al. [16] reported the growth of TiO_2 by hydrothermal process at pH 7 and pH 9 conditions. Rod-like TiO_2 structure was observed at pH 7 of length ~300–350 nm and diameter ~70–100 nm. At pH 9 condition, the morphology was reportedly suppressed to nanoplatelet structure. However, most of the reported TiO_2 nanostructure were not vertically aligned to the substrate. It is reported and accepted that the vertically grown nanowires have superior properties like large surface-to-volume ratio and fast electron transport. From the literature review, it is also evident that the deposition of vertically inclined TiO_2 NWs structure on p-GaN wafer is less studied due to limited number of low-cost fabrication techniques.

In this work, pressed and sintered TiO_2 pallets have been used for growing vertically inclined TiO_2 NWs on p-GaN substrate by the glancing angle deposition (GLAD) technique using e-beam evaporation chamber. The morphology and structure of p-GaN /TiO_2 TF/TiO_2 NWs have been investigated using field emission scanning electron microscope (FE-SEM), and chemical compositions were investigated using energy dispersive X-ray spectroscopy (EDX). The photocatalytic activities of TiO_2 NWs and TFs were measured using UV–Vis spectroscopy. Finally, the sample was characterized using photoluminescence analysis.

2 Experimental Procedure

TiO_2 pellets are obtained by compression of pure TiO_2 powder which is ~99.99% pure (MTI, USA) using a hydraulic press. To reduce porosity of the titanium oxide material, the pellets are further sintered in air at 500 °C which is lower than the melting point of TiO_2. This press and sintering of TiO_2 enhances the strength of the material as well as translucency, electrical and thermal conductivity. The *p*-type GaN substrate (1 cm × 1 cm) is properly cleaned with DI water for 30 s prior to deposition. The substrate is kept at a distance of 24 cm perpendicular from the TiO_2 evaporation source. TiO_2 thin film was deposited at a rate of 1.2 Å/s under the base pressure of ~2×10^{-5} mbar inside the e-beam evaporation chamber by physical vapor deposition method. The TiO_2 NWs were fabricated on top of the thin film at same deposition rate and base pressure by GLAD technique [17]. The substrate is rotated at azimuthal

rotation of 460 rpm, oriented at 85° with respect to perpendicular line between TiO_2 evaporation source and planar crucible [18].

The surface morphology and structure of TiO_2 thin film and NWs sample was investigated by FE-SEM (JOEL, JSM-6700F) characterization technique. The elemental composition of TiO_2 NWs was analyzed using EDX. The optical absorption intensity of the sample was investigated by UV–Vis near infrared spectrophotometer (Lambda 950, Perkin Elmer). The photoluminescence (PL) spectral intensity was investigated by xenon lamp (ELICO, SL 174) at 340 nm excitation.

3 Results and Discussion

3.1 FE-SEM Analysis

The images of top view and cross-sectional view of successfully deposited TiO_2 NWs on GaN substrate are shown in Fig. 1. The diameter of the NWs grown is ~32 nm, which is very less compared to the above results obtained using different deposition techniques. The larger diameter TiO_2 are due to the cluster formation during the deposition process [1]. The cross-sectional view of the FE-SEM also shows successful deposition of vertically oriented TiO_2 NWs of ~400 nm length. Some NWs are found shorter than the average size which may be due to the shadowing effect during deposition process. The increase in nucleation area of adjacent atoms may be due to diffusion over a long distance contributed by low deposition rate [19]. The overall FE-SEM image shows that the synthesized TiO_2 NWs have uniform structure and uniformly grown over the GaN substrate. This GLAD synthesize TiO_2 NWs may be a promising candidate for different optoelectronic applications due to surface-to-volume ratio and smaller dimension of the nanowire structure.

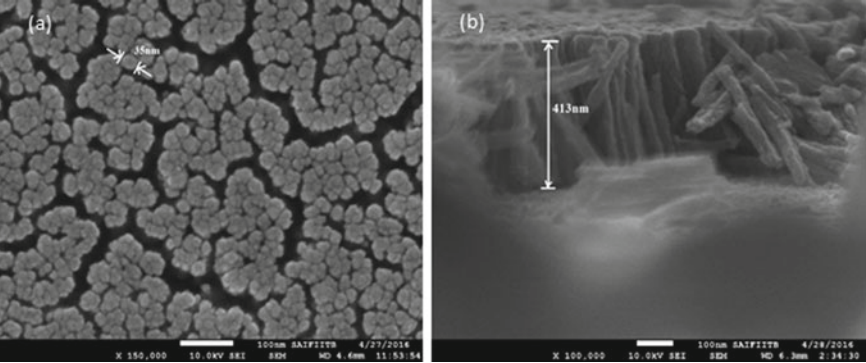


Fig. 1 **a** TiO_2 NWs top view. **b** Vertically aligned TiO_2 NWs cross-sectional view

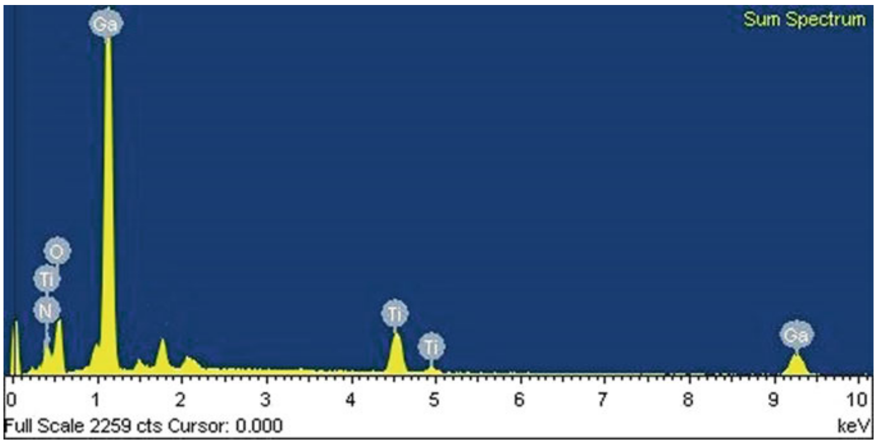


Fig. 2 EDX spectrum of TiO_2 NWs deposited on GaN substrate

In order to analyze the chemical composition, EDX analysis was done to identify the elements present in the synthesized TiO_2 NWs. The peaks from gallium (Ga), nitrogen (N), oxygen (O) and titanium (Ti) were investigated by EDX spectrum and observed as shown in Fig. 2. This also reveals that the TiO_2 is formed successfully on the GaN wafer.

3.2 *Absorption Analysis*

The optical absorption measurement done on the p-GaN/TiO_2 TF and p-GaN/TiO_2 TF/TiO_2 NWs is shown in Fig. 3. The image reported enhancement in absorption in the UV and extended to visible region as compared to the TiO_2 TF sample under the

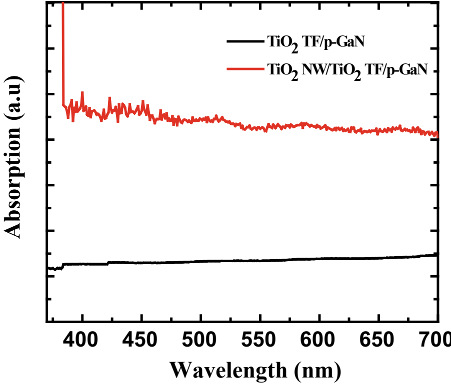
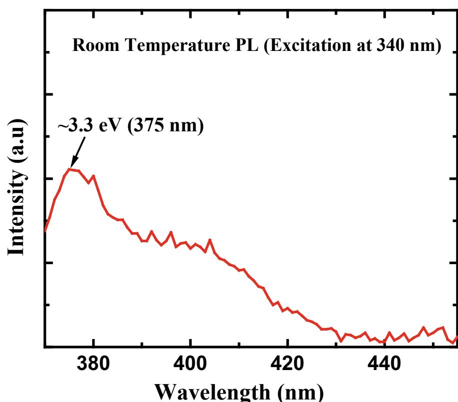


Fig. 3 Absorption spectral intensity of TiO_2 TF/p-GAN versus TiO_2 NWs/TiO_2 TF/p-GaN



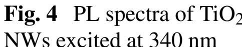


Fig. 4 PL spectra of TiO_2 NWs excited at 340 nm

irradiation of 370–700 nm at room temperature. This enhancement in the absorption of NWs may be contributed by the large surface-to-volume ratio of the vertically oriented NWs. Also, light scattering and trapping between the NWs increase due to the vertical nature of the TiO_2 NWs which is supported by the FE-SEM results. It can also be inferred that the photocatalytic activity of NWs is more due to larger availability of photons as compared to TF.

3.3 *Photoluminescence Analysis*

The PL spectrum of TiO_2 NWs is shown in Fig. 4. Excited at 340 nm indicates maximum peak at ~375 nm wavelength. The optical band gap calculated at this wavelength is observed to be ~3.3 eV. This emission peak may be the result of main band transition of the TiO_2 NWs. Similarly, the band gap of TiO_2 nanostructure was reported to be ~3.3 eV by Ashok Kumar et al. [20]. Again, Kernazhitsky et al. also obtained the band gap of TiO_2 NWs as ~3.3 eV using thermal hydrolysis technique [21]. This band gap energy implies the energy required to move a valence electron from valence band (VB) and conduction band (CB) [22]. It is noteworthy to mention that the band gap depends on the growth technique, size of the crystal grain, and types of TiO_2 (anatase or rutile). The smaller peaks in the UV and visible region at ~396 nm (~3.12 eV) and ~450 nm (~2.75 eV), respectively, may be due to defects in the TiO_2 interstitials [22, 23].

4 Conclusion

TiO_2 NWs were successfully fabricated on gallium nitride (GaN) wafer by GLAD method inside the e-beam evaporation system. Physical vapor deposition (PVD)

method was deployed to grow TiO_2 NWs over the substrate which is more advantageous compared to chemical process. Morphological investigation results confirmed the uniform growth of TiO_2 NWs. Homemade pressed and sintered TiO_2 material was employed to synthesize TiO_2 nanowires (NWs). The EDX analysis of the sample indicates the presence of gallium (Ga), nitrogen (N), titanium (Ti) and oxygen (O). The band gap obtained from PL spectra was found to be ~3.3 eV. The absorption spectra also complement the FE-SEM results indicating maximum absorption happening in the UV and visible area making it a favorable candidate for electronics application. Therefore, the proposed fabrication technique may be employed to fabricate TiO_2 NWs on GaN wafer for optoelectronics application.

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Analysis of a Proof mass Structure of a Capacitive Accelerometer as Wearable Sensor for Health Monitoring

M. Preeti, Koushik Guha, Krishna Lal Baishnab, ASCS Sastry, Kalyan Dusarlapudi, and K. Narsimha Raju

Abstract Design of a real-time device in the form of a MEMS wearable sensor poses challenge in diverse aspects. To model a device for any required ranges of the parameters, the finite element method helps efficiently as the performance of device, in terms of expected specifications like operating frequency, can be analysed with each changing parameter. Such modelling is described in the present paper throwing light on the performance of a proof mass designed for a capacitive accelerometer. The material used for the proof mass and the supporting beams is same and the frequency of operation of the proof mass in the required eigen mode is less than few tens of Hz. A proof mass designed with four support beams is modelled for low-frequency response. Optimising the geometry of the proof mass has given a frequency response between (2 and 12) Hz and a maximum displacement of 4405 μm. The material used is polycrystalline silicon.

Keywords MEMS · Wearable sensor · Accelerometer · Low frequency · Finite element method

1 Introduction

Wearable sensors can be instrumental in capturing fine movement data, gesture sensing and as a tool to capture sensory data to monitor and track diseases. The data collection process becomes easy and accessible to health care providers if they want to monitor over wireless and Internet communication. Health care over remote

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monitoring systems can be possible through wearable sensors and the specialists can reach the patients irrespective of their possibility of physical access to the patient directly. Medical reach into rural areas becomes more effective thereby. Early detection of diseases in certain chronic diseases is obligatory to maintain good health condition before it deteriorates. Recent development in microsystem technology has the paved way towards many portable, small sized devices out of which wearable sensors have gain much attention in the field of medical applications. Designing a medical wearable sensor could be advantageous over using commercial wearable devices in the aspect of gaining more control over the raw data as needed for further processing. Wearable devices assist in the field of rehabilitation, assessment of effectiveness of the treatment, home monitoring and detection of disorders in health by capturing physiological signals. Sensors can diagnose as well as assist continuous monitoring by biochemical sensing and motion sensing. There are various neurological diseases which show up symptoms in the form of reduced and abnormal motor activity. Parkinson's disease (PD) is one such neurodegenerative disorder which is seen is many elderly patients. The symptoms of PD are bradykinesia which is slowness of movement, tremors, rigidity in muscles and gait problems. The patient affected with PD looses their motor skills due to the fact that the brain looses the dopaminergic neurons. The transmission of signals from brain to the motor parts of the body becomes impaired. This leads to symptoms like unilateral and asymmetric tremor in hands and head, gait problems, cognitive impairment and problems with movement and gait. The early symptom of PD is involuntary shaking of hands known as pill-rolling effect. This shaking has a very low frequency in the order of (3–7) Hz. If this low-frequency tremor could be detected by a MEMS sensor, it would help in detecting that early sign of PD which could be a warning sign for the onset of the disease which left undetected or untreated would lead to serious problems for the patient later. Hand tremors being in very low-frequency and fixed-frequency range need a sensor that would detect them precisely and hence the sensor must operate in a range less than 10 Hz and have a gravity value less than 1 g with very less noise floor. The paper details different sensors from the literature that have added to the good achievements in medical field. The following describe the proposed device structure and the analytical equations that support their operation, proposing the optimised design and trade-offs in achieving the required specifications of the sensor.

2 Literature Survey

Gesture recognition using wearable sensors is one of the effective tools used to realise gesture-based information which can be further analysed using different programmes or algorithms. Zhiyuan et al. have developed an interaction prototype for gesture recognition which uses signals from accelerometer [1, 2]. Shahar Cohen et al. used wearable technology to collect data from a Parkinson's disease patient and analysed it with big data. This helped in designing strategies for patient care [3]. Wearable sensors are used in rehabilitation also where older adults and patients with chronic

diseases are continuously monitored for their movement data. Such data are analysed later for the assessment and treatment of the subjects [4]. The general way of assessing neurological disorders like Parkinsonism and movement disorders is visual examination and specific brain scanning techniques. But Rovini et al. proposed a system using inertial measurement unit to analyse the upper limbs movement keeping in view the non-invasiveness of the system and other factors like reducing the economic impact incurred by the disease [5]. There are a number of available commercial wearable devices that monitor the physiological signals like pulse rate, heart rate, blood pressure, number of steps, etc., but a wearable medical device is something which is autonomous and non-invasive performing a specific medical function. The technical challenges that the design of a wearable device faces are vast like biomedical sensors, data handling, decision support, feedback, telecommunication, physical design and autonomy. There are different technologies that support the devices. The technologies include sensors, clothing, computing hardware and communication support. The devices range from wearable monitoring devices, wearable rehabilitation devices, to wearable medical aids. Activity monitoring, motion monitoring and tracking motor skills could be done effectively using sensors like accelerometers designed particularly for such purposes. Identification and categorisation of different body movements and postures would help in identifying any unusual character in them and thereby detect the diseased condition [6, 7]. Tremor is one such motor inability seen in neurology patients which can be detected and quantified based on its frequency and amplitude, sometime the orientation also. If a specific tremor is to be detected, for example as the rest tremor in Parkinson's disease, that tremor has a fixed band frequency and needs to be investigated in that range only. The range falls in the order of (3–8) Hz according to [6]. From the literature, there have been trials made to monitor the movement activity, gait, sleep patterns and thereby monitor the progression of disease and give controlled medicine for the treatment [8]. Many medical studies, researches and case studies have also been done to understand the progression of Parkinson's disease [9]. Wearable and non-invasive sensors are becoming popular because of the advancement in technology giving scope for MEMS technology and micromachining in developing energy effective and highly comfortable sensors [10–14]. Manjiyani et al. have developed a MEMS-based three-axis accelerometer using ADXL335 interfacing it with NI DAQ and measured tilt and monitoring hand movement [15]. Grace Jency et al. have designed and analysed a quad beam MEMS accelerometer by adding mass to the top portion of the proof mass and analysed the damping of the same. Purposeful modification of certain geometries and structures of the device results in more stability and reliability of the device [12]. Bin Fang et al. have proposed a gesture capturing wearable device and models of inertia and magnetic sensors are analysed. The device designed includes accelerometer in it. The fingertip position is also measured here [16]. Madrid-Navarro et al. have conducted a cross-sectional study on PD patients and normal subjects and tested a wrist-worn wearable biosensor to detect continuous rhythms of sleep, motor disturbances and autonomic disruption. This data was taken as a measure to evaluate PD patients [17]. From the many researches that have been performed to monitor gestures and perform movement analysis, it could be identified that disease diagnosis could be

done with sensors by tracking the patient's physiological data. Parkinson's disease can be detected early by detecting the low-frequency involuntary hand tremors that fall in a band of frequency and are also rest tremors.

3 Device Structure and Principal of Operation

To measure the involuntary hand tremors that are of very low frequency, a device that is sensitive to that range of frequency has to be designed. MEMS sensors are of various types depending on the type of transduction principles it works on. The MEMS transducers include mechanical transducers, radiation transducers, thermal transducers, magnetic transducers, chemical and biological transducers. As MEMS is all about mechanical movement being represented in one or the other way of electrical signals, these transduction principles would become the basic principle of operation of that sensor. Each transduction principle can be used to either design a sensor or an actuator. A basic mechanical MEMS sensor essentially consists of a mechanical structure which receives the external stimulus which is the physical signal it is sensing. This external stimulus depending on the type of sensor undergoes change in dimension, displacement, strain, movement of plates or membranes or undergoes vibration and as a result produces an electrical signal.

3.1 Microstructure

MEMS design comprises of microstructures which are capable of moving according to their design and material used to build them. The basic MEMS structure is a microcantilever which is a beam fixed at one end but is free to move on the other end. The smallest dimension of the microstructure is in microns and can extend up to few millimetres which is why they are called as microelectromechanical systems. The materials used to build these structures depend on their field of application and required specifications to be met. As MEMS devices are popular in many fields of engineering and science, including medicine, materials like silicon, gallium arsenic, glass, silica, quartz, polymers and some metals like aluminium, gold, titanium and platinum are used in MEMS. Silicon is commonly used because of its ease of availability, its character of mechanical hardness, brittleness, elasticity and robustness. It also has high mechanical integrity up to 500 °C. To build a MEMS accelerometer, the transduction feature of the sensor has to be first selected. A capacitive MEMS accelerometer has excellent sensitivity and therefore helps to identify low frequencies with maximum resolution. The physical signal is sensed by a moving plate which is in parallel with a fixed plate. When the moving structure changes its geometry or its position with respect to the anchored plate, the change in distance between the plates is measured as the sensed signal. If fringing fields are neglected across the edges, the capacitance measured will be

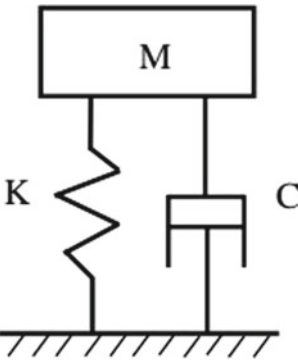

Fig. 1 Spring mass damper analogy of an accelerometer [18]

$$C_o = \in_o \in \frac{A}{d}$$

where A is the common area between the parallel plates or the electrodes and d is the distance between the plates. This moving plate of the parallel plate capacitor is called the proof mass of the capacitive accelerometer. The design of this proof mass plays the vital role in deciding the nature of operation of the accelerometer. The general MEMS accelerometer is equivalent to a spring mass damper as follows (Fig. 1).

The mass M represents the mass of the proof mass which receives the external stimulus of force, the spring constant (k) represents the flexibility of the spring and the factor (c) is the damping coefficient accounting to the damping that occurs in the system. When the mass experiences a displacement (x) because of the force applied on it, then an ideal spring with spring constant (k_s) will exhibit a restoring force (F_s) proportional to the displacement (x).

Therefore

$$F_s = k_s x$$

If the damping is neglected, then by Newton's second law

$$ma = m\frac{\mathrm{d}^2 x}{\mathrm{d}t^2} = k_s x$$

Acceleration (a) is given from the equation

$$a = \frac{k_s}{m} x$$

The equation of motion for the spring mass damper is given by the second-order equation as

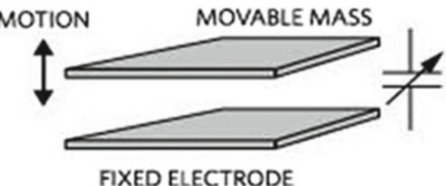

Fig. 2 Simple general structure of a capacitive accelerometer [19]

$$m\frac{\mathrm{d}^2x}{\mathrm{d}t^2} + c\frac{\mathrm{d}x}{\mathrm{d}t} + kx = ma$$

Figure 2 shows simple structure of a capacitive accelerometer having a moving proof mass and a fixed electrode. When the moving mass moves because of the physical signal it is sensing, it brings a corresponding change in the value of the capacitance measured between the plates. While this shows the simple form of the design, capacitive accelerometers are designed in more complex designs where the proof mass consists of moving capacitive fingers, each finger having at least one fixed finger parallel to it and each pair contributing to the change in capacitance. This makes the capacitive accelerometer have high sensitive readings.

3.2 Modelling of the Proof Mass for Optimum Design

A proof mass with support beams on four sides is designed so that it is movable under the external force applied on it. The other edges of the support beams are anchored and a load in the form of force is applied on the proof mass. The proof mass is modelled for its frequency response and displacement (Fig. 3).

A frequency response study is conducted over the proof mass using the finite element method and as per the required specifications, the response is analysed over a range of frequencies from (0 to 50) Hz.

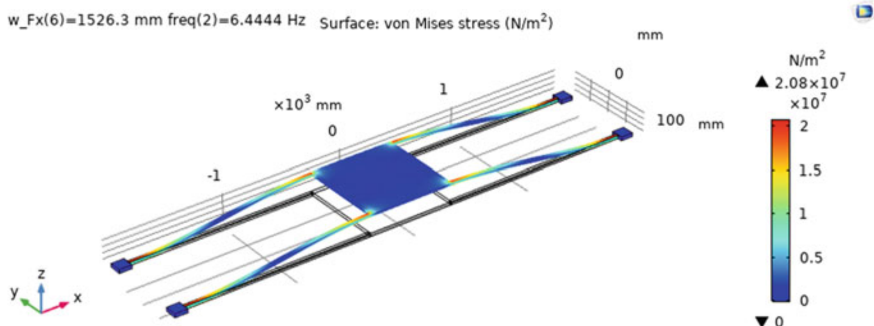

Fig. 3 proof mass supported with four supporting beams

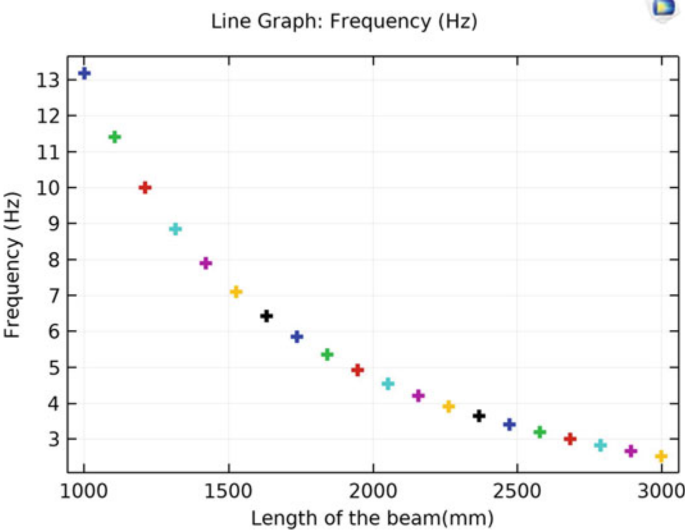

Fig. 4 Length of the beam versus frequency

The proof mass is expected to give a low-frequency response and resonate between the frequency range of (3–7) Hz. The length of the support beams is increased and frequency response is analysed. For a length of 1000–3000 mm of beam lengths, the operating frequency of the proof mass decreases from 13 to 2 Hz as shown in Fig. 4.

While it is evident that the increasing length of the proof mass has decreased its operating frequency, Fig. 5 shows the corresponding displacement experienced by the proof mass at each length. From a 0 Hz to around 25 Hz the displacement graphs have shown different values but over 25 Hz of frequency, the proof mass tended to have zero displacement.

The analysed displacement curves for a length of 1000–1526 mm is shown in Fig. 6, and at a length of 1631 mm, the graph experienced a severe dip as shown in Fig. 7.

For the length values of 1736–3000 mm, the displacement curves have followed similar patterns as shown in Figs. 8 and 9.

4 Results and Discussion

Figures 5, 6, 7 and 8 reveal that the displacement pattern is not uniform or proportional for a proportional increase in the lengths of the beams but have shown different patterns. Analysing the patterns, it can be noted that for a length of 1526 mm maximum displacement of 4405 µm is achieved resonating at 6.445 Hz (Fig. 10).

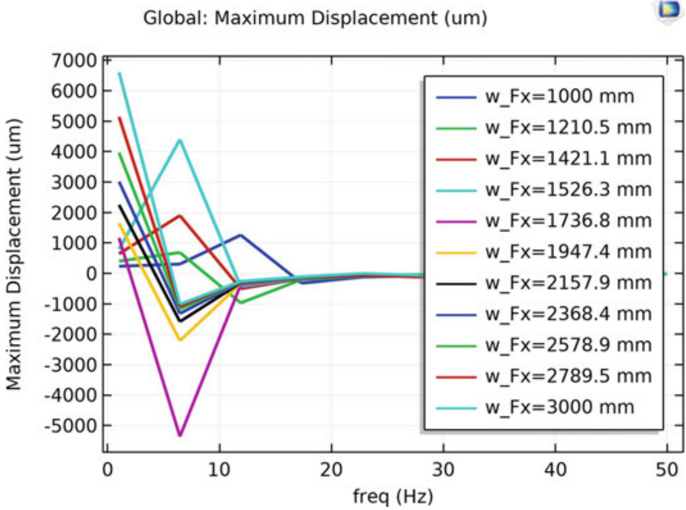

Fig. 5 Frequency versus maximum displacement of proof mass at different beam lengths

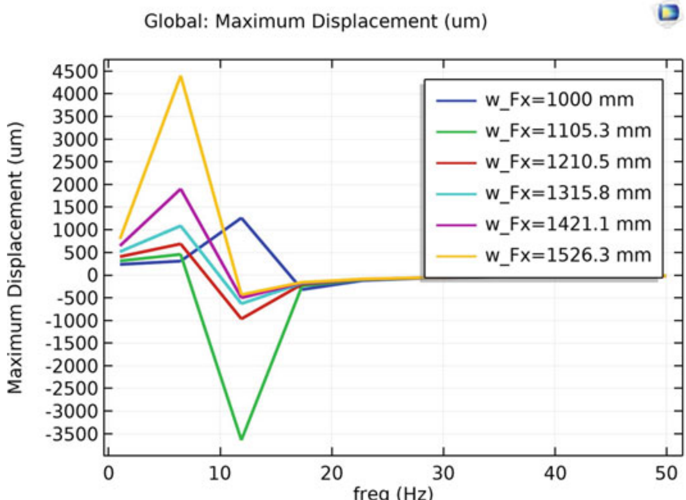

Fig. 6 Frequency versus maximum displacement of proof mass showing maximum displacement for lengths (1000–1526) mm

From Fig. 4, the graph showing length versus frequency also reveals the same result that at a length nearing 1526 mm, the frequency of operation falls nearer to 6.45 Hz. At this optimised value of the beam lengths, the proof mass vibrates in positive *z*-direction with a uniform displacement at all points over the proof mass as shown in Figs. 11 and 12.

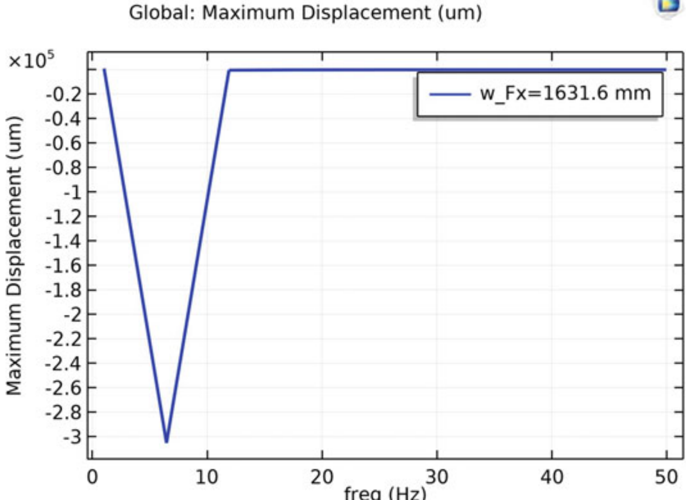

Fig. 7 Frequency versus maximum displacement of proof mass showing severe dip in displacement at a length of 1631 mm

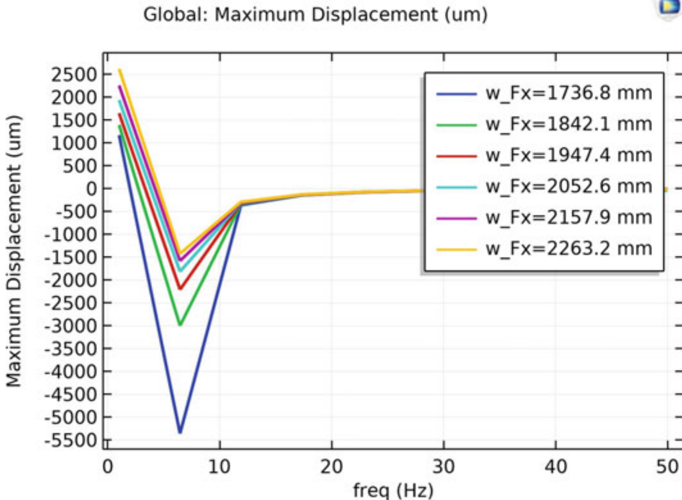

Fig. 8 Frequency versus maximum displacement of proof mass showing similar dip pattern for lengths (1736–2263) mm

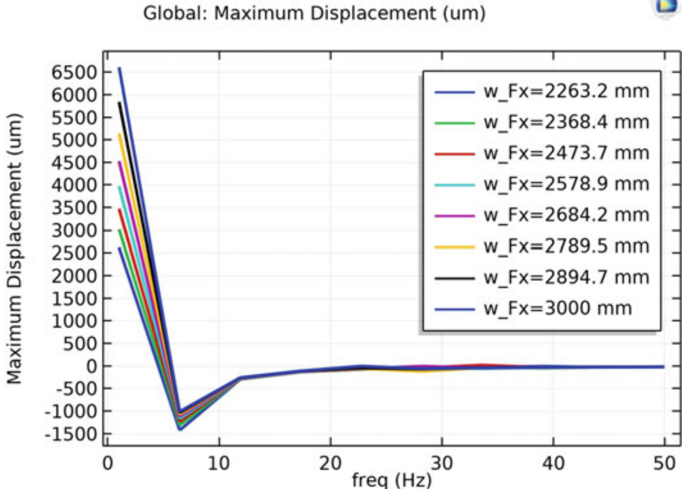

Fig. 9 Frequency versus maximum displacement of proof mass showing similar dip pattern for lengths from (2263–3000) mm

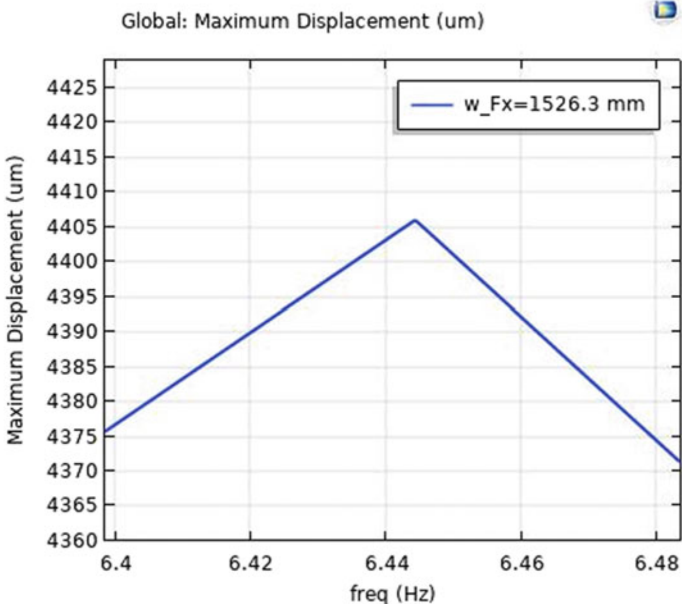

Fig. 10 Maximum displacement achieved for a frequency of 6.44 Hz

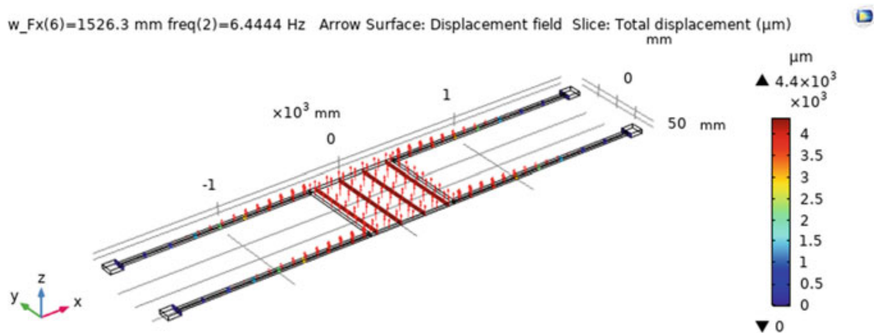

Fig. 11 Arrow surface plot showing direction of proof mass displacement

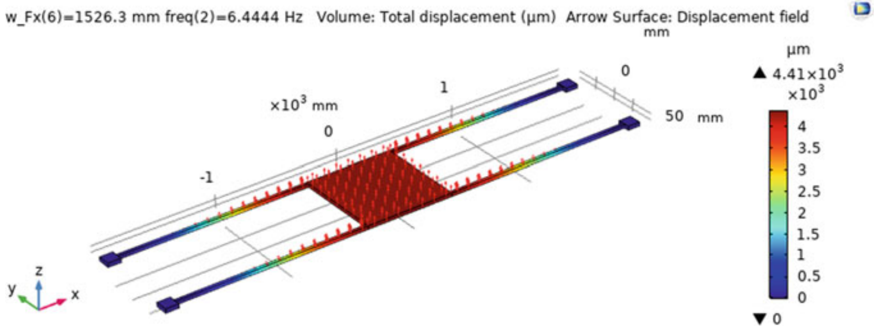

Fig. 12 Volume plot with arrow surface plot showing displacement fields and magnitude

Arrow surface plot in Fig. 11 shows arrows headed in the direction of the movement of the proof mass along with their magnitude specifying the amount of displacement to be 4405 µm. The volume plot in Fig. 12 marks the volume of the proof mass which underwent the same value of displacement indicating that there is no deformation of the proof mass while it is displaced.

5 Conclusion

A proof mass having four support beams is designed using polycrystalline silicon material. Finite element analysis is performed over the design to optimise its geometry. The length of the beams is varied and the displacement profiles of the proof mass at different frequencies is analysed. The required low-frequency response, in between the frequency (2–12) Hz, is obtained where the proof mass has shown displacement in positive z-direction at a maximum value of 4405 µm at a particular length of 1526 mm and a frequency of 6.44 Hz.

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SCAPS-1D Simulations for Comparative Study of Alternative Absorber Materials Cu_2XSnS_4 (X = Fe, Mg, Mn, Ni, Sr) in CZTS-Based Solar Cells

Ashutosh Srivastava, Trupti Ranjan Lenka, and Susanta Kumar Tripathy

Abstract In CZTS-based solar cells, finding an alternative absorber layer material to improve the device performance is ongoing research subject. In this paper, we have identified five alternative absorber layer materials, namely Cu_2XSnS_4 (X = Fe, Mg, Mn, Ni, Sr) and investigated the devices performance with architecture Al-ZnO/i-ZnO/CdS/Absorber/Mo in SCAPS-1D simulator individually of above said five different absorber materials which has not been reported in literature. All the solar cell devices are then optimized on device level by varying thickness of absorber layer, absorber doping and defect density and absorber/buffer interface defect density. We also observed their impact on solar cell characteristic parameters. A comparative study is also carried out to find applicability of these materials as an alternative absorber layer to CZTS in CZTS-based solar cells.

Keywords Solar cell · Absorber layer · Optimization · SCAPS-1D

1 Introduction

Thin film-based second generation solar cells still have the ongoing research prospects because of their low cost of production and easy fabrication process [1]. Solar cells based on Copper zinc tin sulfide (Cu_2ZnSnS_4, CZTS) are the second generation solar cells which have earth abundant and environment friendly constituent elements. Also the usage of CZTS as an absorber layer is justified by its band gap of 1.4–1.5 eV, which is appropriate for solar cell applications [2]. Power conversion efficiency of such cells has got stagnation for the past ten years [3–6]. Research is going on, to meet this issue by either improving the method of device fabrication, or doing some device engineering, or by improving the absorber material. Doping the absorber material with some similar elements is one such method in improving the performance of the cell. Various cationic replacements to zinc in CZTS have been done in literature, and the obtained material showed similar optical behavior to parent

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Table 1 Band gap and electron affinity of absorber layers

Absorber layer material	Band gap (eV)	Electron affinity (eV)
Cu_2FeSnS_4	1.42	4.40
Cu_2MgSnS_4	1.60	4.25
Cu_2MnSnS_4	1.62	4.58
Cu_2NiSnS_4	1.57	4.25
Cu_2SrSnS_4	1.78	4.00

CZTS material [7–13]. These zinc replacements are being studied because, due to similar atomic sizes of copper and zinc atoms, antisite defects are formed in CZTS. Such defects cause open circuit voltage deficits and eventually results in performance degradation of the cell. Recently, our group has studied $Ag_2MgSn(S/Se)_4$ quaternary chalcogenides and found more stable and better absorption coefficient as solar cell absorber layer [13]. Hence, we have identified five such zinc replacement in CZTS, namely Cu_2XSnS_4 where X = Fe, Mg, Mn, Ni, Sr, forming the absorber material Cu_2FeSnS_4, Cu_2MgSnS_4, Cu_2MnSnS_4 Cu_2NiSnS_4, and Cu_2SrSnS_4, respectively. These five materials have been studied in literature theoretically as well as experimentally from absorber layer perspective [7–11]. All these five materials have direct band gap as listed in Table 1.

In this work, we have studied these five materials as absorber material in CZTS-based solar cell, on an individual basis. The device structure of Al-ZnO/i-ZnO/CdS/Absorber/Mo is used in the simulation as shown in Fig. 1. Device optimization is done by varying various device parameters, such as absorber layer thickness, acceptor density of absorber layer, absorber layer defect density and absorber/buffer interface defect density. SCAPS-1D software has been used to study the performance of the cell [14]. A comparative study is done for device characteristic parameters open circuit voltage (V_{oc}), short circuit current (I_{sc}), power conversion efficiency (η), fill factor (FF), among all five solar cells with Cu_2XSnS_4 (X = Fe, Mg, Mn, Ni, Sr) as the absorber layers.

2 Material Parameters Used in Simulation with Device Architecture

Here we have studied thin film-based solar cell having Al-ZnO/i-ZnO/CdS/Absorber/Mo device architecture with well-studied CdS buffer layer. For absorber layer, we have used Cu_2XSnS_4 (where X = Fe, Mg, Mn, Ni, Sr). SCAPS-1D solar cell simulator has been used to study the solar cell device structure as shown in Fig. 1. This simulator solves one-dimensional charge transport equation, the relevant Poisson equation and electronic continuity equations meant for electronic charges electrons and holes and thus calculates the solar cell device parameters, in particular, open circuit voltage (V_{oc}), short circuit current (I_{sc}), fill factor (FF) and

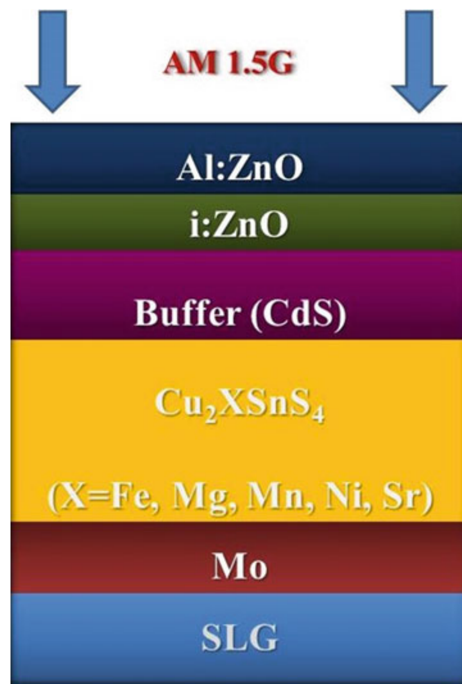

Fig. 1 Device architecture used in simulations

power conversion efficiency (η). Defect densities are considered as neutral, donor and acceptor type. All the material properties that are used in simulations have been collected from various literature relevant to study [2–6]. All these properties are listed in Tables 1 and 2.

Table 2 Various properties for all material used in simulation

Parameter	CdS	i-ZnO	Al-ZnO
Thickness (μm)	0.01	0.05	0.2
E_g (eV)	2.45	3.3	3.3
X	4.2	4.55	4.55
ε_r	8.9	8.12	8.12
N_c (cm^{-3})	2.52×10^{18}	4.1×10^{18}	4.1×10^{18}
N_v (cm^{-3})	2.01×10^{18}	8.2×10^{18}	8.2×10^{18}
μ_n	50	100	100
μ_p	20	20	20
N_D (cm^{-3})	1.0×10^{17}	1×10^{10}	1×10^{20}
N_A (cm^{-3})	0	0	0

3 Results and Discussion

3.1 Effect of Absorber Layer Thickness Variation

Absorber layer is known as the heart of the solar cell as it forms the *p–n* junction with the buffer layer and helps in forming the electron-hole (e^--h^+) pair. After the generation of e^--h^+ pair, it dissociates at the junction and electron travels through the absorber layer before reaching to the contacts. Width of solar cell plays very pivotal role in determining the device performance of solar cells. In this work, we have varied the width of Cu_2XSnS_4 (X = Fe, Mg, Mn, Ni, Sr) absorber layer from 1 to 3 μm and investigated the solar cell characteristics parameter variations. These variations are depicted in Fig. 2a–d.

Figure 2a represents the open circuit voltage (V_{oc}) for all the five absorber materials. V_{oc} is increased in the graph as the layer width increases from 1 to 3 μm. This can be clearly understood that as the width increases, the more number of e^--h^+ pair are generated near the junction and travel through the layer to get collected at the end contact. Also, the value of V_{oc} is almost similar for all the five absorber

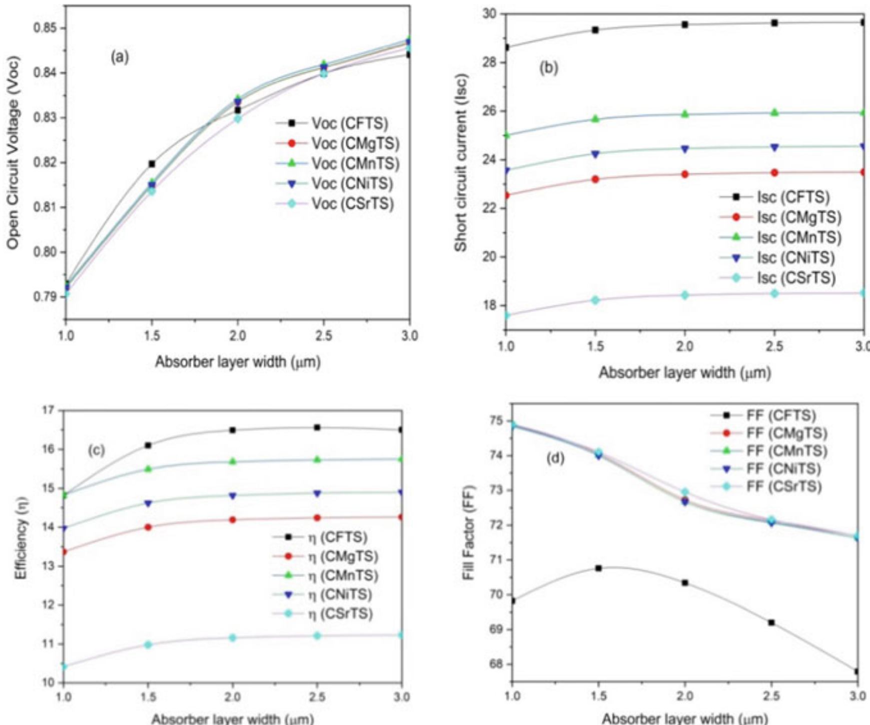

Fig. 2 Absorber layer width effect on V_{oc} (**a**), I_{sc} (**b**), fill factor (**c**), efficiency (**d**), respectively

materials. Figure 2b shows that the variation pattern of short circuit current (I_{SC}) for all five absorber materials is same with maximum current value at 1.5 μm width of absorber layer. Cu_2FeSnS_4 has higher current values as compared to other four materials with Cu_2SrSnS_4 having the least current values. Figure 2c shows that efficiency (η) also varies in the same way like V_{oc} varies with maximum efficiency value at 2 μm. Cu_2FeSnS_4 has the highest efficiency among all five materials, and Cu_2SrSnS_4 has the lowest. Fill factor (FF) variations can be seen in Fig. 2d where excluding Cu_2FeSnS_4 all the other materials follows same trend in the plot. Also, the fill factor value is minimum for Cu_2FeSnS_4 among all and rest other four have almost same values.

3.2 Effect of Electron Affinity Variation of Absorber Layer

Electron affinity of a semiconductor material is defined as the energy difference between the conduction band minima and the vacuum or in other words the energy required by an electron to come out from conduction band minima to vacuum level. Electron affinity determines the conduction band offset present at the connecting interface of the two semiconductors (here absorber and buffer layer). This offset plays a vital role in open circuit voltage and short circuit current and eventually in the performance of the solar cell. It is found that the electron affinity value varies depending on the method of fabrication as well as the ambience of the fabrication chamber [3]. Though this variation is little, but it affects the performance of solar cell a lot. So its correct value is very much desirable. In this work, we have performed simulation by varying electron affinity values of all five absorber material and observed the resultant variations in efficiency of solar cell device. Figure 3 presents the spectra

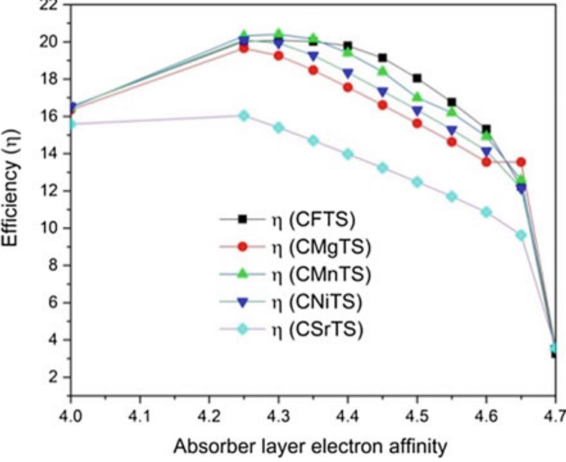

Fig. 3 Effect of electron affinity on efficiency of devices

of efficiency versus absorber layer electron affinity. The corresponding optimized values of electron affinity are given in Table 1.

3.3 Effect of Absorber Layer Acceptor Doping Density

For the betterment of the device performance, it is very much essential to optimize the doping density of absorber layer as it directly affects the open circuit voltage and short circuit current of the device and eventually the efficiency.

It is well known that the parent material Cu_2ZnSnS_4 is naturally a *p*-type material where approximately the acceptors density is equal to the hole density in the absorber layer.

The variation in performance (efficiency) can be categorized into three parts as shown in Fig. 4. In the range of 5×10^{10} to 5×10^{13} of doping density, efficiency does not vary at all. In the range of 5×10^{13} to 5×10^{15} of doping density, efficiency increases at a very fast rate and reaches a maximum value and gets decreased in range of absorber doping density of 5×10^{15} to 5×10^{17}. This pattern is followed in plots for every absorber material. The sudden high in efficiency in second range of acceptor density is attributed to increase in V_{oc} which can be understood by Shockley's equation given by Eq. (1):

$$V_{oc} = \frac{KT}{q} \ln\left(\frac{J_{ph}}{J_0} + 1\right) \quad (1)$$

where K is Boltzmann constant, T is the working temperature, q is the charge density, J_{ph} is the photogenerated current density and J_0 is the saturation current density. Short circuit current does not improve much due to acceptor doping density

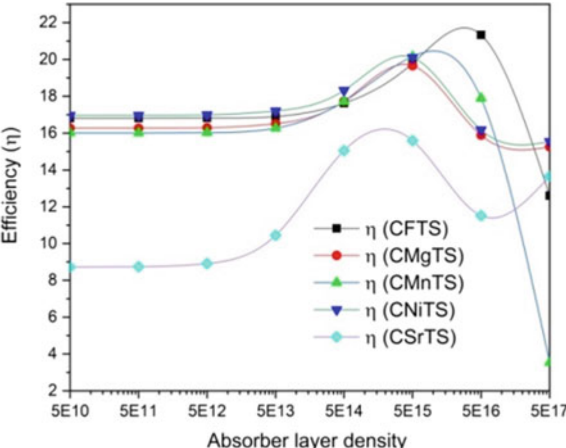

Fig. 4 Effect of absorber layer acceptor density on efficiency of devices

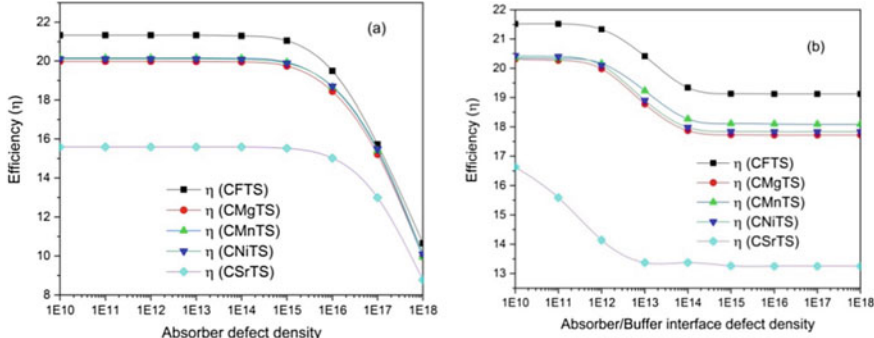

Fig. 5 **a** Efficiency variation with absorber layer defect density. **b** Efficiency variation with absorber/buffer interface defect density, respectively

variation. Cu_2SrSnS_4 gets its highest efficiency at doping density of 5×10^{15} and rest all four Cu_2XSnS_4 (X = Fe, Mg, Mn, Ni) has maximum efficiency at 5×10^{16} doping density.

3.4 Effect of Variation of Defect Density of Absorber Layer and at the Interface of Absorber and Buffer Layer

Defects are the major obstacle in the improvement of devices performance of CZTS-based solar cells. These are present either in point defect or in interstitial form. On the other hand, antisite defects are also present which are formed by interchanging of position of copper and zinc in CZTS. To overcome this issue, many cationic replacements of zinc in CZTS are done so far. Here, zinc has been replaced by five different elements, and the formed absorber materials are studied for solar cell applications. We have optimized the defect density for all these absorber layer materials. Figure 5a shows the plot where efficiency of the device is studied by defect density variation from 1×10^{10} to 1×10^{18}. It can be seen from the figure that efficiency does not vary up to defect density of 1×10^{15}. But as the defect density is increased beyond 1×10^{15}, efficiency of all devices with Cu_2XSnS_4 (X = Fe, Mg, Mn, Ni, Sr) decreased. This decrease in efficiency is due to Shockley read hall recombination in which these defects act as recombination centers in the forbidden energy gap.

Also, the presence of defects at the absorber layer and buffer layer interface affects the performance of the solar cell. Optimizing this interface defect helps in performance enhancement of the cell. In the current study, we have varied the interface defect density for all the five absorber layers with CdS buffer layer from 1×10^{10} to 1×10^{18}, and the plot is shown is Fig. 5b. It can be seen from the plot that the interface defect density up to 1×10^{12} does not affect much for Cu_2XSnS_4 (X =

Fe, Mg, Mn, Ni) except for Cu_2SrSnS_4 where defect density more than 1×10^{10} deteriorate the performance.

4 Conclusion

Effects of device parameter like absorber thickness, absorber doping density, absorber defect density and absorber/buffer interface defect density for the five absorber layer Cu_2XSnS_4 (X = Fe, Mg, Mn, Ni, Sr) have been studied, and in the simulations, CdS is studied as the buffer layer. Solar cell devices with these five absorber layer have been simulated, and the I-V characteristics of the studied solar cell devices are depicted in Fig. 6. The calculated solar cell characteristics parameters, namely V_{oc}, I_{sc}, η and FF are listed in Table 3. From Table 3, it is clear that all these five absorber layer material can be considered for CZTS replacements in CZTS-based solar cell. It can also be concluded that Cu_2FeSnS_4 is having best performance among all these five materials, and also, this study will give help during fabrication of solar cell.

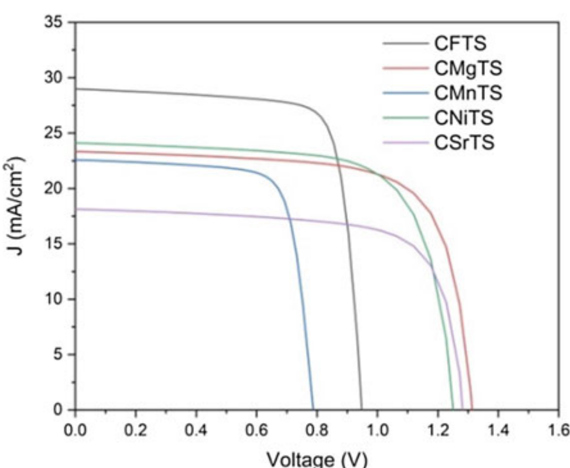

Fig. 6 Solar cell I-V characteristics

Table 3 Calculated solar cell characteristics parameters, namely efficiency (η), open circuit voltage (V_{oc}), short circuit current (I_{sc}), fill factor (FF) and for all five studied absorber layer

Absorber layer	η (%)	V_{oc} (V)	I_{sc} (mA/cm^2)	FF (%)
CFTS	21.52	0.95	28.98	78.19
CMgTS	20.30	1.10	23.34	78.82
CMnTS	13.63	0.81	22.59	74.07
CNiTS	20.43	1.07	24.11	79.08
CSrTS	15.59	1.09	18.15	79.04

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High-Performance Current Mirror-Based Voltage-Controlled Oscillator for Implantable Devices

Pritty and Mansi Jhamb

Abstract Wireless implantable medical devices (IMDs) offer immense possibilities in health care. Since IMDs survive on battery energy, they suffer from serious power constraints. While studying the power concerns of IMDs, it is depicted that voltage-controlled oscillator (VCO) is a fundamental component in the transceiver which consumes significant energy compared to other elements. The quality of performance offered by voltage-controlled oscillator (VCO) in turn depends on the characteristics of constituent current mirror circuit section. In this work, an extensive comparison of performance of VCO is carried out for different current mirror designs to ensure the high standards of quality at power supply as low as 1.8 V. All the circuits have been implemented using spice at 0.032 μm TSMC CMOS.

Keywords Voltage-controlled oscillator (VCOs) · Current mirror (CM) · Operational amplifier · Power · Gain · Bandwidth

1 Introduction

Medical implants are a critical research area owing to the potential applications in health. Batteries are widely adopted energy sources for bio-medical devices [1, 2].

Figure 1a, c depicts the implantable system's vital concept where a mouse is moving freely. Implantable systems/devices are designed using electronic equipment such as a regulator, rectifier, phase-locked loop system, voltage-controlled oscillator (VCO), amplifier, filter, etc., as shown in Fig. 1b. Phase-locked loop system is formed using VCO, filter and phase detector as shown in Fig. 1d. In this paper, VCOs have been designed using different current mirrors in delay cell [4–6]. CMs designed using

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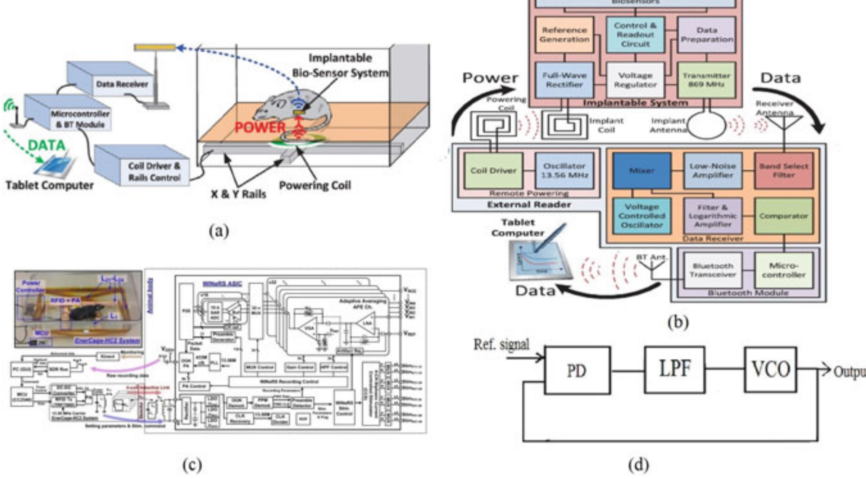

Fig. 1 **a** Block diagram of an implantable system [3]. **b** VCO in the implantable system [3]. **c** Bio-implantable system for nerve monitoring [3]. **d** Phase-locked loop system using VCO [3]

cascode [7–9], self-biased [10–12], variable gain technique [13], resistive compensation technique [14] and body/substrate driven of mirroring MOSFETs [15–17]. Several state-of-art current mirror designs have proposed to date [18, 19]. These designs targeted to enhance the characteristics/different parameters [3].

This work aims to present an empirical comparison of VCO designs using different current mirror circuits and all the existing current mirror designs on a common platform to compare their merits/demerits. The paper consists of the following sections: Sect. 2 depicts the state-of-art current mirror circuits; Sect. 3 described VCO designs using different current mirror topologies. Section 4 discusses the simulations, analyses and their respective characteristics. Section 5 presents the conclusion.

2 Current Mirror Topologies

The CM can design two fundamental ways: basic CM (BCM) in Fig. 2a and cascode CM (CCM) in Figs. 2d and 3. BCM use for designing different CM designs such as resistor-based current mirror (RBCM) in Fig. 2b and very low resistance CM (VLR-CM) in Fig. 2c. CM has designed using amplifiers (see Fig. 4). It can designed using bulk-driven CM (BDCM) in Fig. 5a, regulated bulk-driven CM (RBDCM) in Fig. 5b and variable gain CM (VGCM) in Fig. 5c, d.

Fig. 2 **a** Basic current mirror [5]. **b** Resistor-based current mirror [15]. **c** Very low resistance current mirror [6]. **d** Cascode current mirror [5]

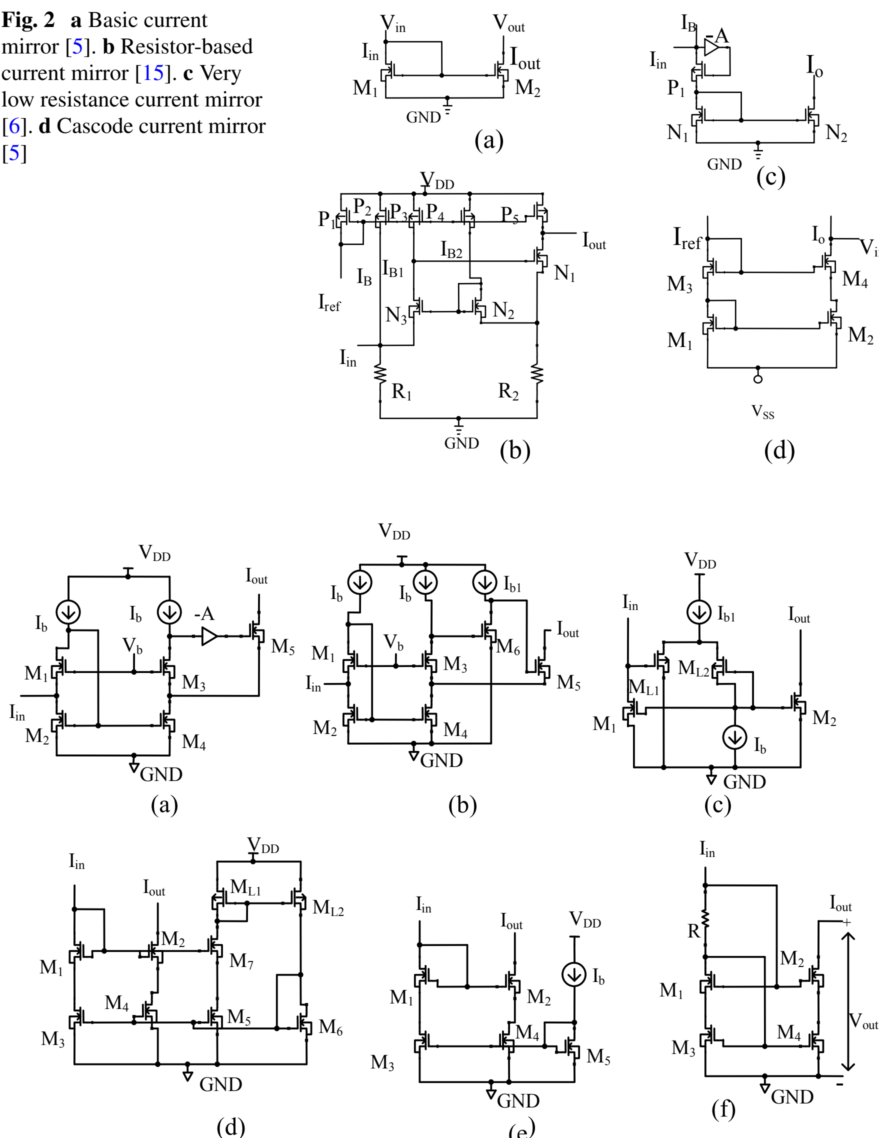

Fig. 3 Cascode CM designs **a** and **b** Regulated cascode CM with super-cascode transistor [11]. **c** Level-shifted CM [12]. **d** and **e** High swing CM [13]. **f** Self-biased cascode CM [9]

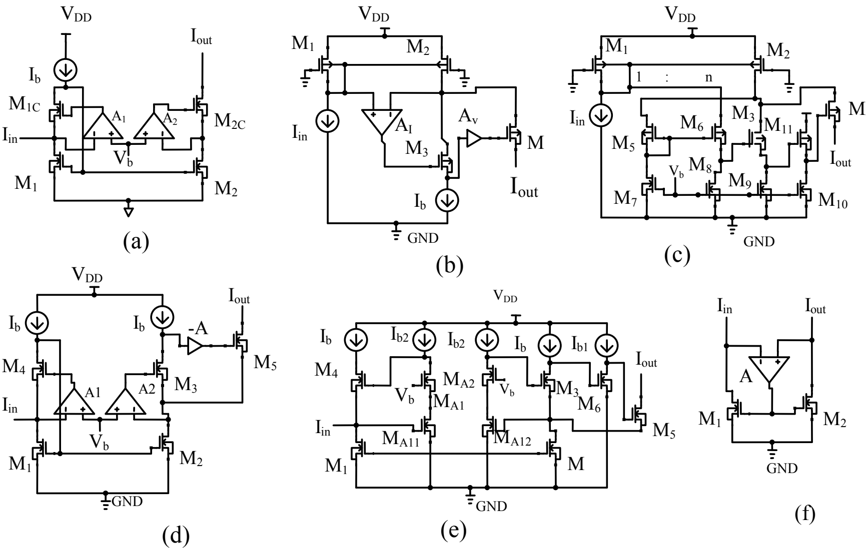

Fig. 4 Current mirror design using amplifiers. **a** Low-voltage, high-performance current mirror [6]. **b** and **c** Gain boosting current mirror [7]. **d** and **e** High-performance current mirror [17]. **f** Tail current source [8]

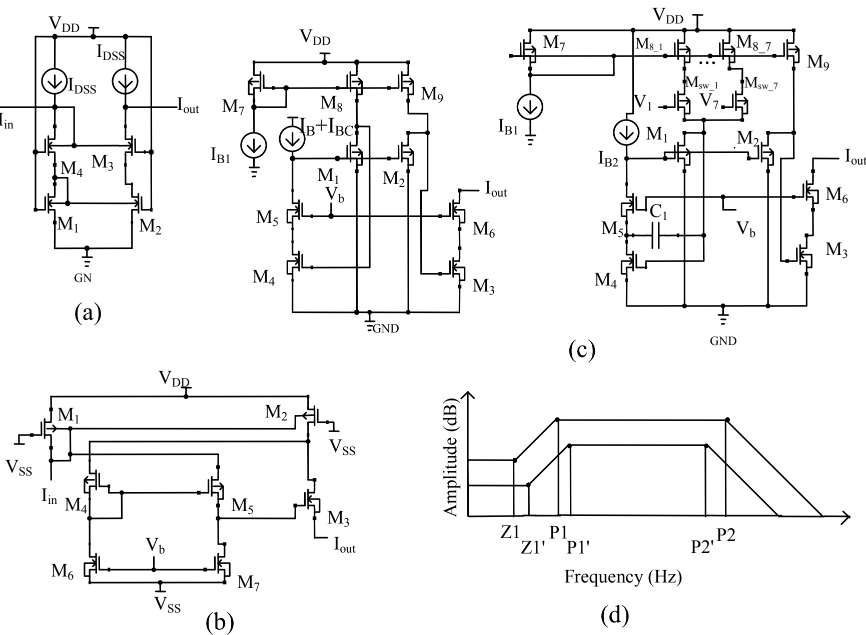

Fig. 5 **a** Bulk-driven CM [18]. **b** Regulated body-driven CM [16]. **c** Variable gain current mirror [14]. **d** Gain amplitude versus frequency bode plot [14]

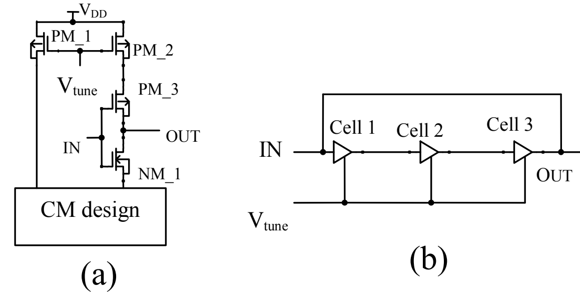

Fig. 6 Design for **a** Delay cell of different VCO. **b** Block diagram of VCO [3]

3 VCO Designs Using Current Mirror Topologies

A VCO works as an amplifier that presents its input using feedback. VCO's prime objective is to produce a waveform of fixed-magnitude output voltage at a particular frequency and a controlled output waveform within a specific range of voltage magnitude and frequency. Layouts for VCOs utilized *N* number of delay cells/stage. Figure 6b depicts a block diagram of a ring VCO using delay cells. The PM_3 and NM_1 transistors work as an inverter for input obtained using feedback. PM_2 transistor operates as the current source and limits the current in the inverter transistors.

The current in current mirror designs has matched to an inverting cell from the bias stage. The advantages in VCO design, such as the wide range of tuning range. VCO's cell has been designed using CM circuits. Different types of CM topologies are schematic with a complete delay cell of VCO. Schematics of delay cells have further converted into symbols for VCO design using spice CMOS technology (see Fig. 6a). VCO has been formed using 3-delay cells and a feedback loop.

4 Result and Discussion

The literature's current mirror designs have simulated in a 32 nm technology at a voltage of 0.8 V. (0.64/0.032) nm is aspect ratios (W/L) of several transistors for the current mirror. The W/L ratios of (M_1, M_2), (M_6, M_7) and (M_3, M_4, M_5) transistors are (0.48/0.032) nm, (0.048/0.032) nm ratio, (0.64/0.032) ratio for the body-driven current mirror. The layouts of all current mirror designs have shown in Fig. 7. Figure 8 shows the output waveform for VCO designs. The current mirror designs have implemented power variation with the switching in the supply voltage V_{DD} in Fig. 9f. Fixed power consumption has obtained in the CM design of the regulated cascode current mirror (RCCM) with a super-cascode transistor, level-shifted current mirror (LS-CM), high swing current mirror (HSCM) and high-performance current mirror (HPCM) (see Table 1). There is a variation from 0.521 * 10–6 μW

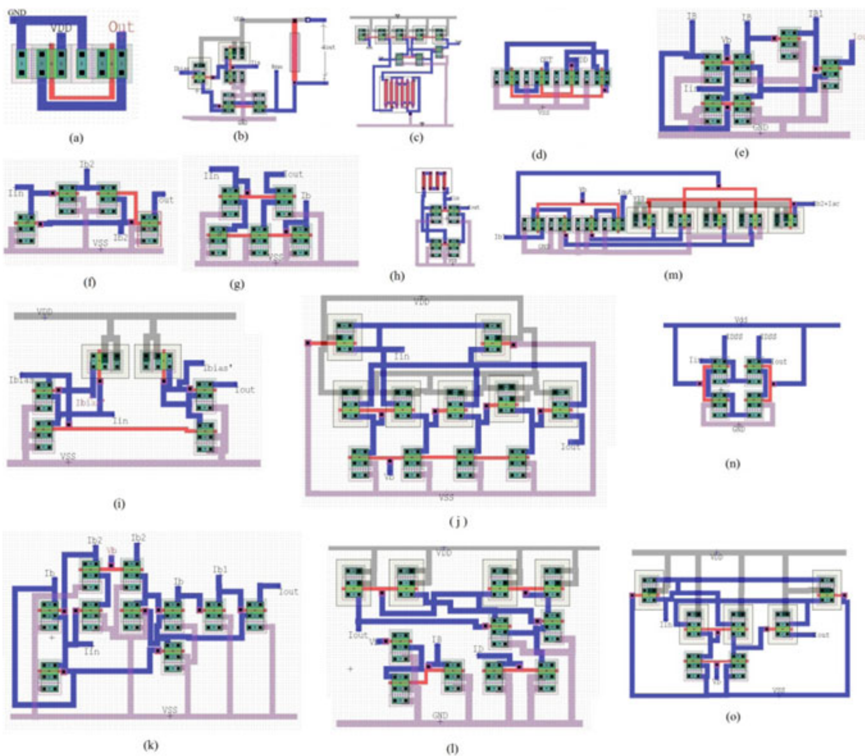

Fig. 7 Layouts **a** basic CM **b** VLR-CM **c** RBCM **d** Cascode CM **e** RSCM **f** LS-CM **g** HSCM **h** SB-CCM. **i** LV-HPCM **j** GBCM **k** HPCM **l** TCS **m** VGCM **n** BDCM **o** RBDCM

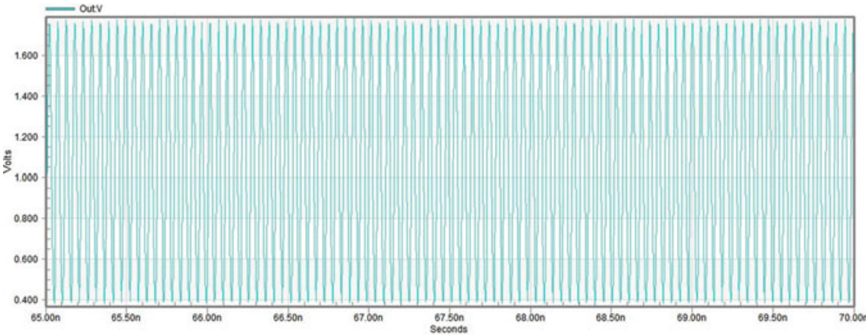

Fig. 8 General output waveform for various VCO designs

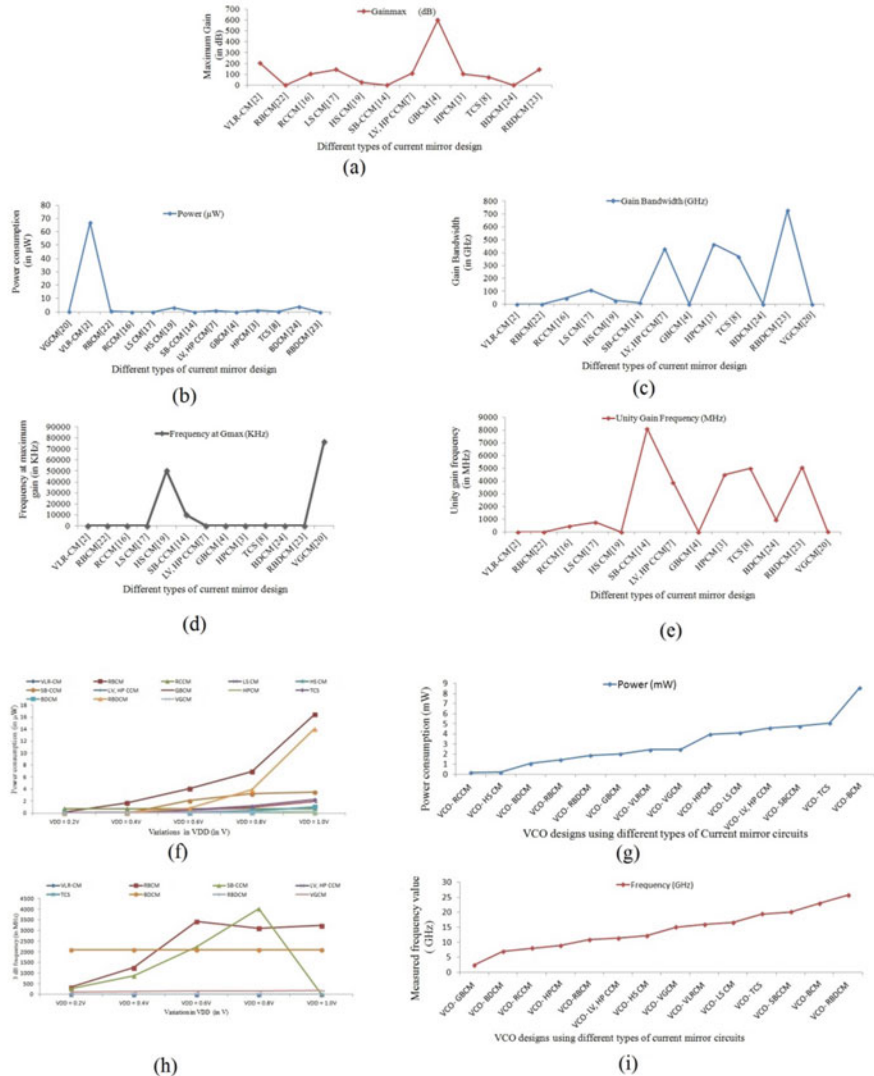

Fig. 9 Graph for different types of current mirror designs versus **a** maximum gain **b** power **c** gain-bandwidth **d** frequency at maximum gain **e** unity gain frequency **f** power **g** power consumption for different VCO designs at 1.8 V **h** 3 dB frequency/bandwidth at different V_{DD} values for current mirror designs **i** frequency for different VCO designs at 1.8 V

to 3.498 µW or 99.96% increment in power values for self-biased cascode current mirror (SB-CCM) in Table 2.

Resistor-based current mirror (RBCM), very low resistance current mirror (VLR-CM) have a shift in values from 0.140 to 16.40 µW or 99.146% and from 0.0212 to 0.991 µW or 97.8% increment in power consumption with V_{DD} value transition from

Table 1 Comparison between different parameters for current mirror designs

	Power (μW)	$Gain_{max}$ (dB)	Frequency at G_{max} (KHz)	Phase margin	Unity gain frequency (MHz)	Gain-bandwidth (GHz)	V_{in} (mV)	V_{out} (mV)
VLR-CM	0.4019	204.656	0.010	167.00	0.086	$17.736 * 10^{-6}$	800	799
RBCM	6.910	1.286	0.010	−8.328	0.211	$271.879 * 10^{-6}$	20.966	20.852
RCCM	0.736	102.242	0.010	−83.090	459.744	47	767.238	767.207
LS-CM	$0.97 * 10^{-6}$	144.512	0.0316	58.830	763.886	110.390	12.0735	12.0939
HS CM	$0.58 * 10^{-6}$	27.263	50,118	−96.244	1.072	29.243	–	–
SB-CCM	3.221	1.3916	10,000	−51.505	8098	11.267	650.525	650.526
LV-HPCM	$2.54 * 10^{-6}$	110.904	0.010	78.641	3899	431.667	7.403	7.402
GBCM	0.965	600	0.010	–	–	–	799.837	–
HPCM	$0.24 * 10^{-6}$	103.908	0.010	−82.064	4485	466.050	5.7769	1.8291
TCS	1.177	74.450	251.188	−6.713	4990	371.541	800	397.707
BDCM	0.280	604.422	$10 * 10^{6}$	−72.715	959.194	0.579	0.075	0.075
RBDCM	3.930	143.348	0.199	15.017	5091	729.415	551.203	551.203
VGCM	0.016	10.123	76,432	70.360	10.786	0.109	–	0.0091

Table 2 Power comparison at different V_{DD} values for current mirror circuits

V_{DD}	0.2 V	0.4 V	0.6 V	0.8 V	1.0 V
	Power (μW)	Power (μW)	Power (μW)	Power (μW)	Power (μW)
VLR-CM	0.0212	0.0680	0.168	0.4019	0.991
RBCM	0.140	1.700	4.066	6.910	16.40
RCCM	0.736	0.736	0.736	0.736	0.736
LS-CM	$0.97 * 10^{-6}$	$0.97 * 10^{-6}$	$0.97 * 10^{-6}$	$0.97 * 10^{-6}$	$0.97 * 10^{-6}$
HS CM	$0.58 * 10^{-6}$	$0.58 * 10^{-6}$	$0.58 * 10^{-6}$	$0.58 * 10^{-6}$	$0.58 * 10^{-6}$
SB-CCM	$0.521 * 10^{-6}$	0.00096	2.064	3.221	3.498
LV-HPCM	$0.158 * 10^{-6}$	$0.635 * 10^{-6}$	$1.42 * 10^{-6}$	$2.541 * 10^{-6}$	$3.970 * 10^{-6}$
GBCM	0.047	0.1783	0.448	0.965	1.90
HPCM	$0.24 * 10^{-6}$	$0.24 * 10^{-6}$	$0.24 * 10^{-6}$	$0.24 * 10^{-6}$	$0.24 * 10^{-6}$
TCS	0.029	0.173	0.572	1.177	2.247
BDCM	0.00047	0.0071	0.0568	0.280	1.057
RBDCM	0.0108	0.122	0.815	3.930	14.003
VGCM	0.0127	0.0392	0.0854	0.162	0.287

0.2 to 1.0 V. The power variations or increments are 0.158 * 10–6 μW to 3.970*10–6 μW or 96.02%, 0.047 to 1.90 μW or 97.526% and 0.029–2.247 or 98.709% for low-voltage high-performance cascode current mirror (LV, HPCM), gain boosting current mirror (GBCM) and tail current source (TCS), respectively. Variable gain current mirror (VGCM), bulk-driven current mirror (BDCM) and regulated body-driven current mirror (RBDCM) have power variation or increments from 0.00047 to 1.057 μW or 99.95%, 0.0108 to 14.003 μW or 99.92% and 0.0127 to 0.287 μW or 95.574% in Fig. 9b. The comparison between current mirror designs in terms of power has led from 43.125 to 99.98% change as compared to 6.910 μW maximum power value at supply voltage 0.8 V in Table 1. The maximum and minimum power has been consumed 8.556 mW and 0.196 mW by VCO-BCM and VCO-RCCM, respectively.

There are 97.709% powers saving in VCO-RCCM as compared to that of other VCO designs. The gain-bandwidth product has reached from 17.736 MHz to 729.415 GHz for different design of current mirror circuits. For RBCM and VLR-CM, there is a 99.999%, 99.987% less gain-bandwidth values as compared to the maximal gain-bandwidth product. RCCM, LS-CM, HSCM and SB-CCM have 93.552%, 84.865%, 95.990% and 98.45% decrease gain-bandwidth product values as compared to maximum 729.465 GHz gain-bandwidth as shown in Fig. 9c. For LV-HPCM, HPCM and TCS, the percentage of minimal gain-bandwidth is 40.820%, 36.106% and 48.926%, respectively, compared to the maximum gain-bandwidth value. For BDCM and VGCM, there is a 99.92% and 99.885% least gain-bandwidth values compared to that maximum value. At supply voltage variation from 0.2 to 1.0 V, the 3 dB frequency/Bandwidth is varied 89.50%, 77.285%, 93.124% and 66.857% for RBCM, VLR-CM, SB-CCM and LV-HPCM designs in Table 3.

Table 3 3 dB frequency comparison at different V_{DD} values for current mirror designs

V_{DD}	0.2 V	0.4 V	0.6 V	0.8 V	1.0 V
	3 dB frequency (in MHz)	3 dB frequency (in MHz)	3 dB frequency (in MHz)	3 dB frequency (in MHz)	3 dB frequency (in MHz)
VLR-CM	1.9538	0.3234	0.3509	0.3963	0.4438
RBCM	339.9898	1255.7	3429.2	3110.7	3239.4
SB-CCM	275.8331	878.327	2228.3	4012	-
LV-HPCM	0.00875	0.00768	0.00643	0.0049	0.0029
TCS	0.00796	0.0283	0.265	1.4066	5.0588
BDCM	2092.5	2092.5	2092.5	2092.5	2092.5
RBDCM	$206.9517 * 10^{-6}$	$219.3150 * 10^{-6}$	$269.848 * 10^{-6}$	$461.898 * 10^{-6}$	$807.763 * 10^{-6}$
VGCM	102.794	124.932	146.819	166.888	184.057

For TCS, RBDCM, VGCM, it's extend 99.84%, 74.379%, 44.150%, respectively, at V_{DD} range from 0.2 to 1.0 V and constant 2092.5 MHz 3 dB frequency value for BDCM in Fig. 9h. Figure 9i describes the different values of the oscillating frequency of VCO designs using different current mirror designs. The maximal 25.709 GHz and minimal 2.374 GHz oscillating frequency has been obtained in VCO-RBDCM and VCO-GBCM, respectively, in Fig. 9g. Oscillation frequency has saved 90.765% as compared to that of VCO-GBCM as shown in Table 4. Gain value for different types of CMs has 1.286 dB minimum and 602.422 dB maximum values. Compared with maximum gain value, RBCM and VLR-CM have 99.786%, 66.207% least gain values in Fig. 9a. The RCCM, LS-CM, HSCM and SB-CCM circuits have obtained 83.028, 76.01, 95.474 and 99.768% least gain values sequentially to maximum gain

Table 4 Power and frequency values at 1.8 V for different VCO designs

	Power (in mW)	Frequency (in GHz)
VCO-BCM	8.556	22.949
VCO-VLR-CM	2.4401	15.968
VCO-RBCM	1.428	10.894
VCO-RCCM	0.196	7.98
VCO-LS-CM	4.102	16.535
VCO-HS CM	0.1997	12.199
VCO-SB-CCM	4.761	20.114
VCO-LV, HP CCM	4.604	11.329
VCO-GBCM	2.018	2.374
VCO-HPCM	3.977	8.895
VCO-TCS	5.092	19.463
VCO-BDCM	1.0719	6.935
VCO-RBDCM	1.881	25.709
VCO-VGCM	2.450	15.011

value as shown in Table 1. Compared with maximum gain value, LV-HPCM, GBCM, HPCM and TCS have 81.590, 0.402, 82.751 and 87.641% least gain values. There is 76.204%, 98.319% minimal gain values of RBDCM and VGCM individually obtained when compared with the maximum gain value of BDCM. The maximum and minimal gains have reached at 10 GHz and 10 Hz frequencies in Fig. 9d. 167.006° and −96.244° have maximum positive phase margin for VLR-CM and minimum negative phase margin for HSCM in Table 1. The maximum positive phase margin and minimal negative margin have obtained at 86 kHz and 1.074 MHz in Fig. 9e.

5 Conclusion

The VCO designs and current mirror circuits have been simulated at spice 32 nm CMOS technologies. As performances of state-of-art current mirrors have evaluated, cascode CM gives minimum power consumption and minimum value of voltage transfer error and maximum unity gain frequency. Several CMs using op-amplifier have maximal bandwidth, less power consumption and high/ moderate gain values but high voltage transfer error. In comparison, VGCM provides less power, least unity gain frequency, moderate 3 dB frequency, positive phase margin, minimal gain and low gain-bandwidth. The comparison between different types of CMs reveals that 99.99% maximum gain-bandwidth for RBDCM compared to that minimum value for RBCM, a 99.99% increment in power value of RBCM as compared to the minimum power value of HPCM. The VLR-CM has offered the highest positive (167.006°) phase margin. The BDCM has offered a 99.786% higher gain compared to the minimum that value of RBCM. For BDCM, the frequency at maximum gain has obtained higher compared to that of basic CMs, LV-HPCM, GBCM and RCCM. The unity gain frequency of SB-CCM has a 99.98% higher value than the minimum that value of LR-CM.

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Power Efficient Analysis of MOS Current Mode Logic Based Delay Flip Flop

Ramsha Suhail, Pragya Srivastava, Richa Yadav, and Richa Srivastava

Abstract Prompt escalation of technology in the realm of electronics is beyond comparison. Pronounced digital circuits like registers, buffers, counters and sequential state machines make large scale utilization of Delay Flipflop (D flipflop). Subsequently, this work propounds several design facets of a D flipflop. Consequently, a CMOS based conventional NAND circuit is considered and examined for four design parameters namely, delay(t_p), power (pwr), Power Delay Product (PDP) and Energy Delay Product (EDP). Moreover, MOS current mode logic (MCML) based implementation is investigated for NAND circuit. In addition to that, this paper also presents a smart logic design of MCML NAND based D flipflop. The broached design results as a competent candidate for countless D flipflop based digital logic designs as it relents exclusive results in contrast to the conventional counterpart. Thus, the proposed enactment broaches as ideal circuit for recent digital logic style applications.

Keywords MOS Current Mode Logic (MCML) · Low Power · CMOS · D Flip Flop · NAND · PDP · EDP · HSPICE · Proteus

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1 Introduction

The rising sophistication of applications are impelling designs and manufacturing of IC to new levels of intricacy. The continuous decrease in the chip size and relative rise in the microchip density have made power consumption an emerging concern in VLSI industry. With the rise in the transistor density, there will be a relative need for CMOS scaling technology [1]. Also, the integration of digital and analog system circuitry can contribute in lowering the chip area [2]. Innumerable number of methodologies are introduced to lower down the power consumption in digital systems. Device geometries, device characteristics like threshold voltage and interconnect properties are remarkable factors that brings out reduction in the overall power consumption.

Several researchers today are evolving in this advanced technology in order to design and simulate efficient logic circuits using the state of art for improvising the performance. Consequently, there is a logic style that looks inspiring in this regard. It subsides the overall power consumption of a compact system in an analog friendly environment and is popularly known as MCML [3]. MCML has surfaced as fast, differential logic style which stands out with excellent power profile along with high operating speed [4]. Moreover, MCML is generating considerable interest in terms of its minimal switching noise and reduced sensitivity in process and thus it acts as an alternative for static CMOS design circuits[5].These enlightening features of MCML produces fruitful outcomes in mixed signal environments and perceive an extensive area of applications especially high-speed ring oscillators and optical communication transceivers [6].

The technology empowering these consumer products are critically subjected to several electronic components that have the ability to store information. Digital circuits that take this aspect into account is popularly known as sequential circuits or cyclic logic circuits. The output of sequential circuit mainly depends on present input along with the past input [7]. Flipflops are well known memory storage elements that can store up to one bit of information. It has two stable states that is 0 and 1 and thus is called as bi-stable multivibrator. One of the fundamental elements used for designing a circuit with sequential logic is D flipflop where d stands for delay. It is by far the most salient clocked flipflop with the ability to latch, store and memorize the data. It apprehends the value of D input at a defined section of the clock cycle. Moreover, this apprehended value represents the output. D flipflops are conventionally used as frequency dividers and data latches. In fact, they are a subset of communication transceivers as they introduce delay in the process by one clock pulse. The circuit symbol of D flipflop is shown in Fig. 1. It is a single input device which transfers input

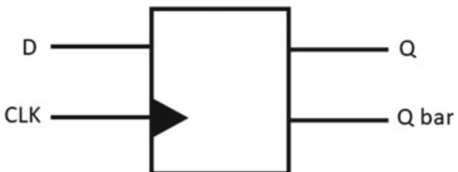

Fig. 1 Circuit symbol of Dflipflop

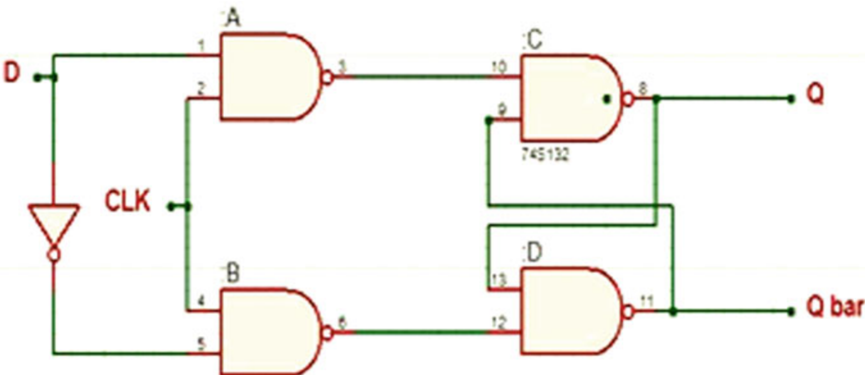

Fig. 2 D flipflop using NAND gate

data (D) to one of the outputs on clock falling or rising edge. This edge triggered device is a modified version of Set-Reset flipflop with an inverter connected between S and R inputs as shown in Fig. 2. It ensures that the S and R inputs of the SR.

flipflop are never equal to one at the very same time. The truth table and characteristic table of the corresponding flipflop is given in Tables 1 and 2.

The characteristic equation of D flipflop is stated in Eq. 1 as

$$Q_{n+1} = D \tag{1}$$

When we apply high clock input, the D input is duplicated as output. Thus, the D flipflop stores and produces an output no matter what logic value is applied at D input as long as clock input is high. However, if low clock signal is applied on D flipflop then the output depicts the previous output value.

This paper carries out the following analysis:

Table 1 Truth table of D flipflop

D	Q_n	State
0	Q_n	No change
1	1	Same value

Table 2 Characteristic table of D flipflop

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

- It examines a standard CMOS based NAND. The circuit is outlined for several design metrics, for instance, Power (PWR), delay (t_p), Power delay product (PDP), Energy delay product (EDP).
- NAND gate circuit is then executed with MCML design topology.
- A peculiar MOS based MCML *D* flipflop is put forward and examined for the specified design metrics.

To uphold the proposed peculiar design, this research work outlines massive simulations with the help of HSPICE for 16-nm PTM (developed by the Nanoscale Integration and Modeling (NIMO) Group at Arizona State University (ASU) [8].

This work is organized and garnered into five sections. Section 2 introduces the conventional CMOS implementation of NAND gate along with the overall power dissipation CMOS design circuits. Section 3 outlines the unique MCML implementation of NAND. Further, this section also covers the evaluation of the proposed circuit for several design metrics, for instance, Power (PWR), delay (t_p), Power delay product (PDP), Energy delay product (EDP). These parameters are contrasted with their counter parts(as explored in Sect. 2). Section 4 manifests the proposed circuit of MCML based D flipflop and summarizes the work with the comparative analysis between the two designs. Finally, Sect. 5 illustrates the conclusion of the critique.

2 Implementation of CMOS Based NAND

With the advancement in the technology, reliability of VLSI circuit has been an emerging concern of the semiconductor industry. Moreover, low power has become a prime issue in the VLSI circuit realization. Power consumption is a function of supply voltage, load capacitance and load capacitance. CMOS implementation techniques have acquired heed due to its low power delivering proficiency [9]. CMOS design circuits have two prime constituents of power dissipation namely Static power dissipation and dynamic power consumption. Hence, the overall power dissipation of CMOS circuit design is stated in the Eq. (2)

$$P_{\text{total}} = P_{\text{static}} + P_{\text{dynamic}} \tag{2}$$

CMOS devices have apparently very low static power consumption which is basically due to the leakage current. The static dissipation arises when each input is held at some sound logic level and the circuit is not at its charging state otherwise in case of some switching activity at nodes, dynamic power is generated in the CMOS device [10]. Today, almost every VLSI circuit has a predominant tradeoff between the two most concerned design metrics namely delay and power. These design metrics needs to be stabilized such that an enhanced operation speed and corresponding power and this is given by the power delay product (PDP) and it is stated in Eq. (3).

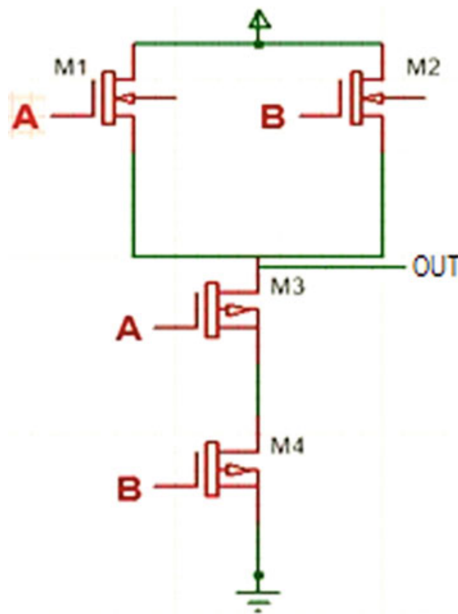

Fig. 3 Schematic of CMOS based NAND

$$\mathrm{PDP} = \mathrm{PWR} \times t_p \tag{3}$$

But it has been observed that on changing the input power supply, the relative PDP reduces significantly. To avoid this deviation, superior parameter named as energy product delay is derived. It is defined in Eq. (4) as

$$\mathrm{EDP} = \mathrm{PDP} \times t_p \tag{4}$$

Figure 3 depicts the schematic of CMOS based NAND. The author has grasped this opportunity to justify the above stated circuit and evaluated the same for four design metrics. Figure 4 demonstrates the simulation analysis for conventional CMOS based NAND circuit. The CMOS based NAND circuit is observed and explored on four parameters including delay, power dissipation, PDP and EDP at supply voltage of 700 mV. The conclusion drawn are shown in the Table 3.

3 Implementation of MCML Based NAND

The coherent performance of the CMOS based NAND considered in the previous section gives us an overview to realize a preferable configuration for the circuit. The circuit logic style that provides high speed with low power profile can thwart the peer style in case of fabrication requirements of the circuit designs in the VLSI industry.

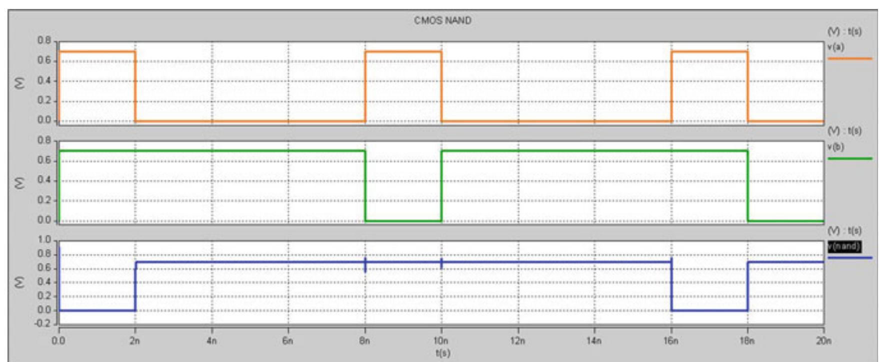

Fig. 4 Simulation results for CMOS based NAND

Table 3 Design metrics of CMOS based NAND

Device parameter (supply = 700 mV)	CMOS based NAND
t_p (ns)	0.14
PWR (pW)	34.49
PDP (ZJ)	4.97
EDP (ZJ-ns)	0.718

This section outlines the MCML based NAND gate. The schematic of MCML based NAND is evinced in Fig. 5.

MCML has surfaced as fast, differential logic style which stands out with excellent power profile along with high operating speed. Moreover, minimal switching noise and reduced sensitivity in process variations is observed in MCML designed circuit systems and thus it has gathered contemporary interest as an alternative for static CMOS design circuits.MCML based implementations are familiar for their outstanding performances as discussed in Sect. 1. Figure 6 depicts the simulation analysis of the MCML based NAND circuit.

Both forms of NAND are simulated for 16 nm Technology node at 0.7 V supply (V_{DD}). HSPICE based simulated results are tabulated in Table 4.

The MCML based NAND circuit is observed and explored on four parameters including delay, power dissipation, PDP and EDP at supply voltage of 700 mV. Table 4. brings comparative study between the conventional circuit design and the proposed circuit design. MCML based implementation shows 15.55 × improvement in delay, 30.20 × improvement in power, 451.81 × improvement in PDP and 7180 × improvement in EDP.

The MCML based NAND has emerged with remarkable results in comparison to CMOS based NAND. The former serves reduced delay and yields analog friendly environment, when compared to the latter one. The weak dependence of propagation

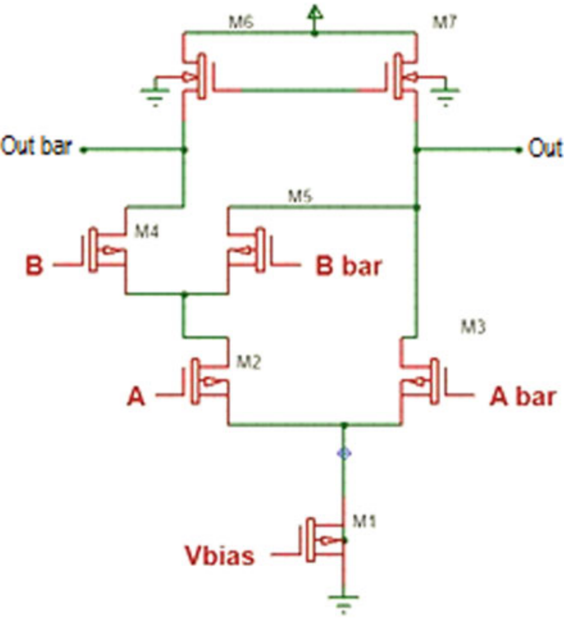

Fig. 5 Schematic of MCML based NAND

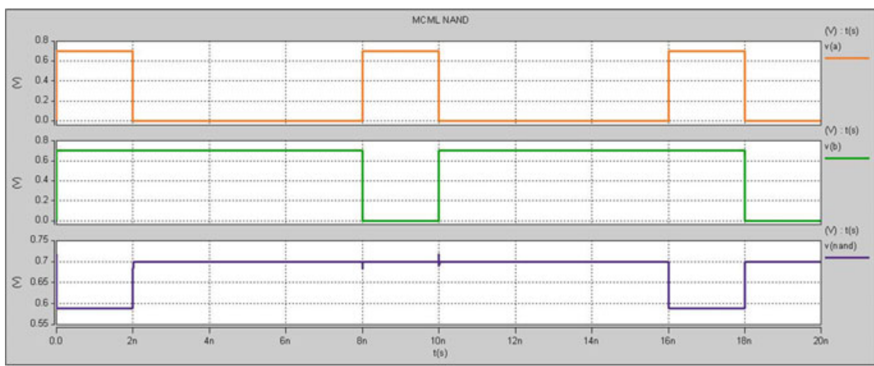

Fig. 6 Simulation results for MCML based NAND

delay on fan out capacitance is an added advantage to MCML topology over conventional CMOS. These results have further strengthened our confidence in the MCML based NAND circuit due to the significant reduction in the overall power consumption at much higher frequencies. Furthermore, both PDP and EDP has reduced remarkably. Thus, the MCML technique clearly has an advantage over the conventional techniques. This paper thus, validates the usefulness of MCML techniques. These

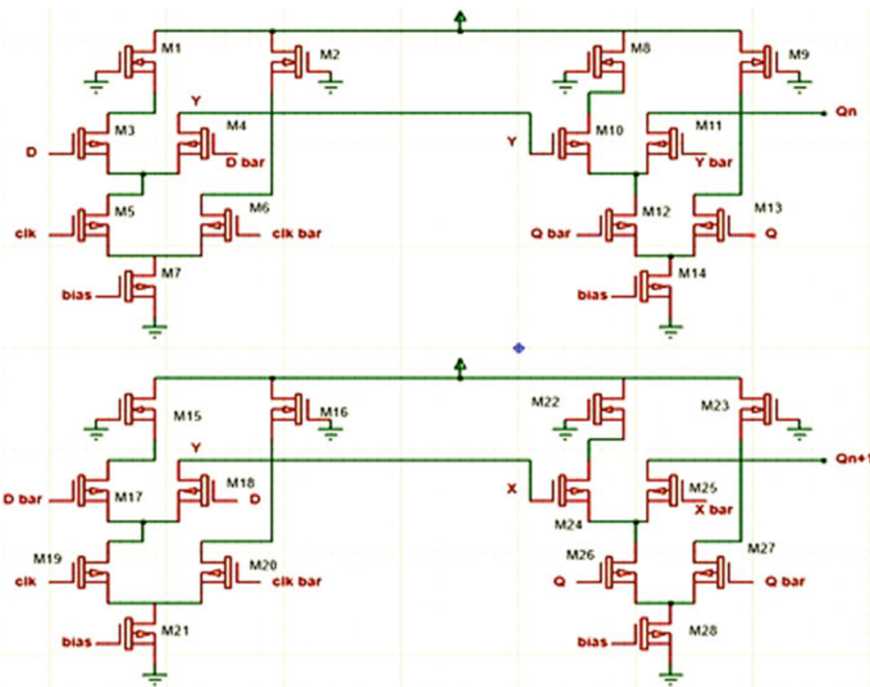

Fig. 7 Schematic of D flipflop using MCML NAND

Table 4 Design metrics of MCML based NAND

Device parameter (supply = 700 mV)	CMOS based NAND	MCML based NAND
t_p (ns)	0.14	0.009 (15.55)
PWR (pW)	34.49	1.142 (30.20)
PDP (ZJ)	4.97	0.011 (451.81)
EDP (ZJ-ns)	0.718	0.0001 (7180)

tabulated results offer powerful evidence for the superior performance of MCML based NAND.

Voltage swing is a crucial function of the input supply voltage. It defines a voltage range that impart an amplified and modified output without any deformation. In this treatise, it can be observed (from Figs. 4 and 6) that the proposed MCML based NAND has impressive low voltage swing in contrast to the CMOS based NAND and thus it becomes suitable for high-speed operations. MCML topology can enhance the performance of low power digital circuit by altering the voltage swing.This work provides additional support for the considerable insight at the D flipflop using MCML based NAND which will be discussed in the upcoming section.

Table 5 Design metrics of CMOS based D flipflop using MCML NAND

Device parameter (supply = 700 mV)	CMOS based D flipflop using MCML NAND
t_p (ns)	0.04
PWR (μW)	9.9
PDP (fJ)	0.47
EDP (fJ-ns)	0.02

4 Proposed Circuit: MCML Based D Flipflop

A streamlined implementation of MCML based NAND considered in the previous section offers a quick realization for designing more complex configuration for the logical circuits.According to [11], while designing D flipflops, each transistor is warily sized in order to attain the prime trade-off relative to power and delay. As most of the transistors drive internal nodes, they are scaled to reduce the overall power dissipation. But a compact transistor is prone to random variation, and thus the performance variation of a D flipflop becomes massive [12].

A recent review on literature focused on the cause of the metastability of the D flipflops and edged out a large hold time but enjoy zero setup time [13]. The literature in [14] draws our attention towards the comparative analysis between the CML based D flipflop and conventional D flipflop corresponding to delay and power profile. Several studies for instance [15] have conducted a research on dynamic CML to construct a power efficient delay flipflop.Major contribution and insightful study on CNFET based MCML 3-bit parity checker circuit has been reported in [16].

This section of the treatise focuses on designing a MCML based delay flipflop. The schematic for MCML based D flipflop is illustrated in Fig. 7. It is carried out with the help of four NAND gates where each NAND gate in turn is enacted by employing MCML topology. Furthermore, this section estimates four design metrics, specifically delay, power, PDP and EDP for the proposed MCML circuit. Additionally, H-spice based simulated results are listed in Table 5.

5 Conclusion

Intuitive discovery and research advancement in the most modern electronic chips make a headway to optimize speed and power. The two-design metrics determine the survival of any electronic circuit in today's competitive scenario of miniaturized dimensions. The cut-throat demand for high speed and low power has insinuated the research idea to optimize the electronic circuits for the same. Bountiful applications and appropriate use of Delay flipflop in latest electronic modules has provided impetus to this treatise. This paper, examines CMOS and MCML based NAND for delay and speed. Simulation results establishes superior performance of MCML based NAND implementation. Further this article proposes a MCML NAND based

D flipflop and successfully implements the circuit at 700 mV supply. The proposed circuit shows 0.04 ns delay, an 9.9 μW power. This article provides horizon for future research on low power. Low power circuit realization along with high input current range and high output impedance may be practiced as in [17]. Similarly, the proposed work may be implemented for high bandwidth requirement as demonstrated in [18]. Also, researchers can employ n/p-type oxides to implement D flipflop as in [19]. The schematics depicted in Figs. 2, 3, 5, and 7 are designed and mapped on the well-known circuit simulator named Proteus.

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Design and Analysis RF-MEMS Capacitive SPDT Switch for Wireless Applications

Ch.Gopi Chand, Reshmi Maity, K. Srinivasa Rao, N. P. Maity, and K. Girija Sravani

Abstract This paper introduces the design and simulation of SPDT-switch having less pull-in voltage and better isolation at 1–25 GHz range. The exhibition of the intended SPDT configuration is such that the signal can be routed within two ports utilizing barely one single-bias. Here, we have designed a non-uniform meander-type shunt switch and these two switches are incorporated on the same single line, which helps to decrease the pull-in voltage, also maintained good isolation and enhance the performance of the switch. The simulation of Electromechanical and Electromagnetic analysis is done in FEM and HFSS tools. However, the switch is obtained a small operating voltage of 2.3 V. The radio frequency characteristics of return (S_{11}) and insertion loss (S_{12}) are measured −32.44 dB, –0.108 dB, and the switch achieves good isolation as −59.94 dB and −42.25 dB at 1–25 GHz. Here, the proposed device is command signals and reduces opposed uniting two shifting components. The overall proposed device is kept better results at 1–25 GHz frequency.

Keywords Shunt type switch · SPDT switch · Actuation voltage · S-Parameters

1 Introduction

MEMS devices are widely used in a variety of forms and contain high-frequency apparatus namely RF switches, variable capacitors, and inductors. RF MEMS and microwave switches should be the subject of much investigation because of their superior achievements in particular small insertion loss, excessive isolation, very low power consumption, and good linearity [1–4]. By associated with PIN diodes, the

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MEMS switches are very minute, below density not sensitive to acceleration, and good switching time and high isolation. RF Electronics RF and Microwave Electronics have always needed switches that have low on-loss losses and high off-state isolation with high signal strength and low control power [5]. The linear connection MEMS switches have generally used for applications where the operating frequency is restricted to numerous gigahertz. An RF switch is a crucial segment for processing RF signals. They mainly utilize electrostatic triggering because power consumption is low and small switching times, as suitable compatibility by electrical components moreover accessories. Reliability remains a primary benefit of RF MEMS switches [6–9]. The Appearances such as dielectric charging, auto-commutation, and low-temperature processing decrease the potential of MEMS technology. A new SPDT switches are using a new geometric approach which ensures more reliability offered [10] Nowadays, in wireless and mobile communication systems, which produced an atomic hike in developing user demands as a military destination [11]. In particular, the SPDT device is a broadly used switching component in the importance of radio transmission operations and a measuring machine with multiple high data repetition signals needs to be attached to any random outputs [12, 13].

An SPDT switch switching circuit is analyzed that uses micro-machined switches with metal side contacts. The insertion of 0.08 dB and a reflection loss is 32 dB at 5 GHz, the isolation is 32 dB at 5 GHz, and return loss (S_{11}) is more than 19 dB at 5 GHz, and the actuation voltage of 23.3 [13].

The SPDT switch is presented versus a series capacitive circuit, and the total bandwidth is 20 GHz by more reliable isolation than –20 dB and insertion loss in the –0.1 to –0.5 dB range. Preliminary results are confirmed by COMSOL-Simulations, and a combined-circuit design with a pull-in voltage of 22.4 V among a resonant frequency is 10.94 kHz. [14].

Hybrid SPDT Design Approach switch isolation is better across a broad frequency range. The isolation of 55 dB, is achieved at 12.5 GHz with an insertion loss of 0.22 dB. The operating voltage and resonant frequency of the ohmic switches are 5.0 V and 6.79 kHz, in series [15].

The paper is systematic, as develops, in Sect. 2 expressed the purpose of the proposed RF-MEMS SPDT switch and its characteristics. Sect. 3 gives out the outcomes and its analysis of the device, and eventually, Sect. 4 concludes that entire article.

2 Structure of the Proposed Device

Usually, the beam is attached within the ground, signal line, and a fixed block is placed on the coplanar wave guide (CPW). While some DC voltage is employed among the membrane and the transmission line, the outcome steady force creates the beam and it slightly touches downward [16–18]. The thickness of CPW is 2 μm, and also silicon substrate is 30 μm. In a CPW transmission line, the dielectric thickness (td) is 0.5 μm and this gap is considering as 1 um from the dielectric layer and beam.

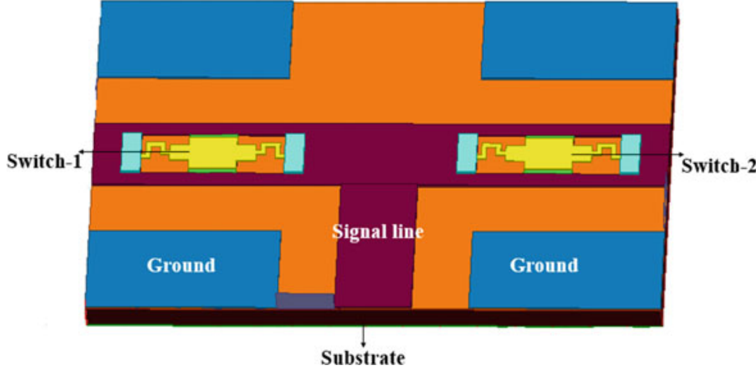

Fig. 1 Top view of meander type proposed SPDT switch

The device is made up of T-shaped transmission, beside a mounted switch with metal contacts, it is designed by using the ANSYS-HFSS simulation tool. The schematic diagram of the implemented SPDT is given in Fig. 1. The high resistance Si slice is operating as single substrate material, and SiO2 is adopted as the oxide layer, the Si_3N_4 is used as a signal dielectric and Au is utilizing as a switch membrane due to its good metal conductivity. This is followed by an increase in device performance.

The capacitive type shunt switches are placed on the signal line. One of these output channels has come together into the input port, without the primary position, the membrane and electrodes to maximize actuation force, which as a result, has a huge decrease in response voltage. The gap between the signal dielectric and membrane is having 1.6 μm and indicates deep on-state capacitance, which extra boundaries that device bandwidth by removing the more under operating frequency duration to a greater value. However, a smaller signal line gap results in degraded isolation in the off state.

The switch has been obtained to be performed by employing two identical switches driven through electrostatic force. Accordingly, they require a couple of paired signals that necessary to be organized to ensure an association path within one of the inputs to output ports. Consequently, several inconsistencies intervening switch designs can give asymmetrical switching properties when seen at the output terminal. This switching path can act efficiently simulated by connecting mechanical transportation lines upon the switch segment at proper ways of the junction. The proposed device measurements are reported in Table 1.

Table 1 Measurements of the proposed device

Sl. No	Structural elements	Length (μm)	Breadth (μm)	Height (μm)	Material
1	Substrate	600	400	30	Silicon
2	Ground	200	100	2	Gold
3	Oxide layer	600	400	2	SiO_2
4	Beam	50	40	1.5	Gold
5	Signal dielectric	50	40	0.5	Si_3N_4
6	Signal line	150	80	1.5	Gold
7	Meander-1	5	5	1.5	Gold
8	Meander-2	5	10	1.5	Gold
9	Meander-3	5	12	1.5	Gold

3 Results and Its Discussions

3.1 Spring Constant and Pull-In Voltage

We can reach a high ability to manage power from great restorative power and desirable insensitivity to fluctuation because of the immense spring rate. The operating voltage can be kept below 2.3 V,

Since an electrostatic force does involve in the confinement stage, a little gap has previously created amid the lower electrode and the beam. The spring rate can be determined by the equation, [19]

$$K = \frac{16EWt^3}{l^3} \tag{1}$$

Here, 'E'—Young's modulus, 'W'—width, 'l'—length, 't'—thickness

$$V_P = \sqrt{\frac{8Kg_0^3}{27\varepsilon_0 A}} \tag{2}$$

The deformation of a beam of the switch that can be operating at low voltage is nothing but a pull-in voltage. It depends upon the gap actuated area and spring constant (K). Theoretically, it is calculated by using the formula as, [20].

Where, 'K'—spring constant, 'g_0'—gap, 'A'—actuation area, 'ε_0'—free space permittivity. The actuation voltage (Vp) of proposed switch concerned as 2.3 V, the simulation voltage versus displacement of switch is shown in Fig. 2, and it is done by FEM tool.

Figure 3 shows that voltage versus displacement with gold material having the beam thickness is 1.5 μm.

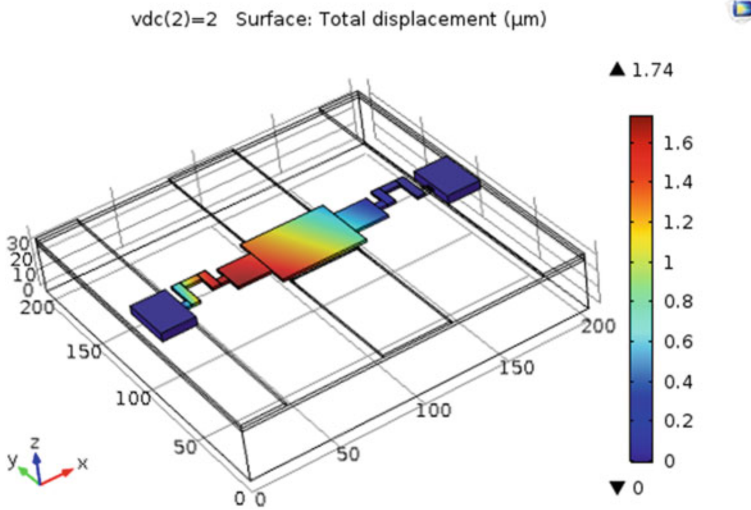

Fig. 2 Displacement of switch by pull-in voltage

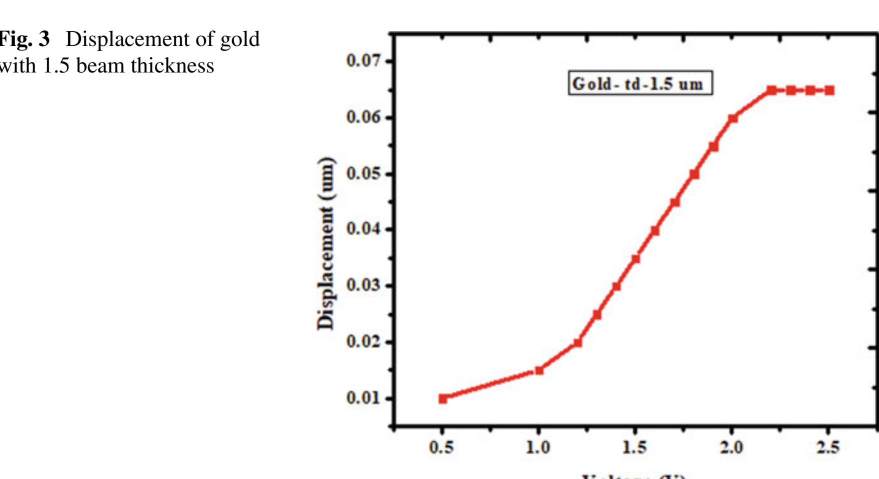

Fig. 3 Displacement of gold with 1.5 beam thickness

3.2 RF-Performance Analysis

We have estimated S-parameters of the SPDT switch that are analyzed in the simulator of high-frequency structures (HFSS) tools. The switch is occurred in two states such as ON and OFF conditions, in these we have measured return, insertion losses (S_{11}, S_{12}) and isolation (S_{21}), respectively. The dielectric material and thickness are key factor for getting good S-parameters [21–24]. The isolation level depends on the

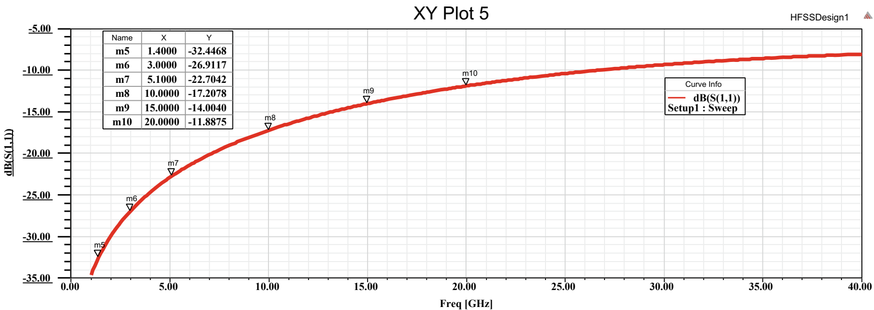

Fig.4 Return loss measured in on state

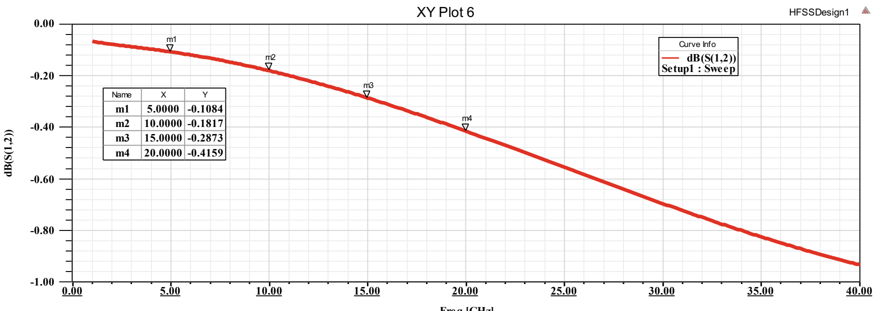

Fig.5 Insertion (S_{12}) of the switch

corresponding value of the shunt impedance to the specific impedance of the signal line [25–27].

The measured return loss in the upstate as −32.44 dB and −11.88 dB at 1–25 GHz is as displayed in Fig. 4. The minimum insertion was analyzed of −0.108 dB and 0.415 dB, at 5 to 20 GHz frequency as shown in Fig. 5.

Better isolation of the SPDT device in a extensive frequency scale, higher than Isolation −59.94 and −42.25 dB from 1 to 25 GHz is shown in Fig. 6.

4 Conclusion

In this paper, the SPDT switch was designed and simulated. The operating frequency of the proposed switch can be carried out from 1 to 25 GHz frequencies. The main focus of the paper is to design SPDT switch with low actuation voltage and good isolation, by using non-uniform meanders switch owning an actuation voltage are 2.3 V. The return (S_{11}) and insertion (S_{12}) are measured at −32.44 dB, −0.108 dB, the switch maintained good isolation as −59.94 dB, −42 dB at 1–25 GHz frequency.

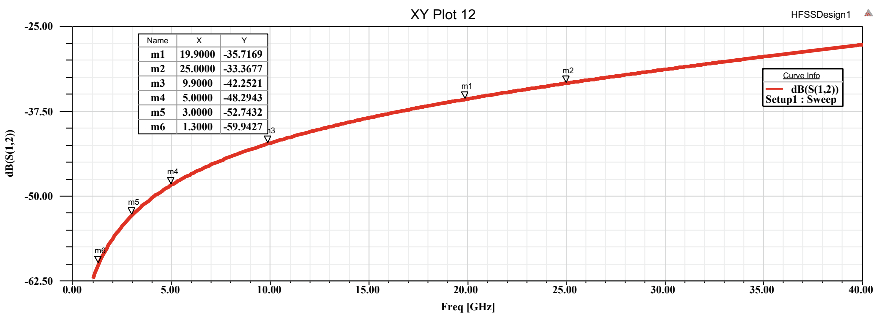

Fig. 6 Isolation of proposed switch

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Design of Piezoresistive-Based Microcantilever for MEMS Pressure Sensor in Continuous Glucose Monitoring System

G. Sai Lakshmi, K. Srinivasa Rao, Koushik Guha, and K. Girija Sravani

Abstract In this paper, design and simulation of three kinds of microcantilevers are done with the use of COMSOL Multiphysics FEM software. The physical behaviour of the 3 microcantilevers and its corresponding response is calculated using three materials zinc oxide, lead zirconate titanate and barium titanate and with three electrodes aluminium, gold and platinum. At most proposed microcantilever is an integrated with electro-osmosis pressure sensor to detect the blood glucose levels in continuous glucose monitoring system in terms of change in resistance and in voltage form.

Keywords Diabetes · Microcantilever · Piezoresistive · Capacitive · Piezoelectric · BIO-MEMS · Electro-osmosis

1 Introduction

A portable non-invasive device is introduced to monitor the patients suffered for blood insulin and glucose concentration. A separate PCB board was introduced which connects the finger chip and acquires the NIR wavelengths [1]. They designed a MEMS-capacitive sensor for CGM for diabetic patients. Two charged parallel plates which are driven electrically are separated by dielectric medium inside a microchamber and separated by an external environment [2]. A bio-compatible affinity MEMS glucose sensor is designed; in this, two devices are fabricated and characterized; it consists of a membrane or microcantilever which is placed inside the microchambers and separated by a sensing environment and driven by a controlled by the remote sensing field [3]. They proposed the affinity sensor for the CGM system. In the microchamber, two magnetically driven vibrating diaphragms are placed; by

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using different solutions, viscosity is calculated [4]. Interdigital electrodes ate taken to determine the blood glucose level in non-invasive way in several test objects [5]. They introduced the MEMS device for continuous glucose monitoring system which consists of semi-permeable membrane and a microcantilever, both are integrated with the microchannels to create the miniature device with a volume of 0.4 µl [6]. [7–10] shows the different structures of the pressure sensors by using various mechanisms to detect the blood glucose in the continuous glucose monitoring system. They introduced a multichannel nano-cavity photonic coupled crystal bio-sensor having waveguides and nano-cavities, and those nano-cavity coupled photonic bio-sensor is able to detect the glucose concentration in blood [11]. They designed a affinity glucose sensor, and it measures the glucose concentration through the changes induced by the glucose in the dielectric properties in a synthetic polymer [12]. Piezoelectric cantilever sensor through MEMS technology detects the glucose blood levels in the glucose monitoring system [13]. The signal processing unit, display unit and probe are mounted in a sensor for NI GMS and based on the principle of beers and lamberts law to detect glucose molecules in blood [14]. A approach of microwave spectrograph by using interdigital electrodes sensor is used to estimate the glucose levels in blood [15]. The device consists of a microcantilever or membrane and is controlled by remote magnetic induced in microchamber and isolated by a sensing environment by a semi-permeable membrane [16]. The CGM system for human body is proposed to monitor glucose levels at regular intervals; the main advantage of this is to give instant reports when the blood glucose is fallen or risen [17]. They introduced a multi-electrode sensor consists of four electrodes, that is, two platinum electrodes in that one is counter platinum electrode and another is reference electrode to measure the glucose concentration and background current [18]. A non-invasive bio-sensor is introduced to detect the blood glucose levels in glucose monitoring system by varying different voltage that sensor shows the effect in the blood [19]. To determine the performance analysis of the capacitive pressure sensor, two plates are separated by a dielectric medium [20]. Design of microbridges for pressure sensor for continuous glucose monitoring is done using the three principles piezoresistive, piezoelectric and capacitive [21]. They introduced the different capacitive pressure sensor to determine the capacitance when pressure is applied as input [22]. The capacitive pressure sensor is introduced for the harsh environment [23]. They proposed the Electro-Osmotic pressure sensor to detect blood glucose levels in the CGM system [24]. A multichannel nano-cavity coupled bio-sensor is introduced in the hexagonal lattice structure in air slab to determine the glucose concentration in blood [25]. Type 1 diabetes were made possible by the development that measures glucose levels in the blood, but the results taken for continuous glucose measurement may not come exactly [26]. The continuous glucose monitoring system used in this paper is minimally invasive method [27]. The structure which is constructed for a chip-less tag sensor may be embedded in a smart watch which can read the patients skin [28]. Till now two types of approaches are presented that is non-invasive and minimally invasive. In this paper, we proposed a sensor with chemical free nature, to improve sensitivity and for better response time.

The rest of the sections are as follows: proposed method and working principle are discussed in Sect. 2, performance analysis is discussed in Sect. 3, and finally conclusions are provided in Sect. 4.

2 Methodology

2.1 Proposed Device

A pressure sensor is used to measure stress induced in membrane which is caused by the pressure. Pressure sensor has test chamber and inner square cavity which is filled with the reference solution concentration 100 mg/dl. In the bottom of the test chamber, a semi-permeable membrane is placed and it is used to seal the square cavity. In the test chamber, the concentration 50–450 mg/dl of solution changes with reference to the solution in square cavity. When the fluid is brought into contact with outside solution if the solution is same but having the different concentration then the osmotic pressure difference is created in membrane and fluids moves towards the output. The deflections caused by the stress are calculated in the form of change in resistance and voltage.

2.2 Working Principle

In this paper, the sensor uses the Osmosis principle to detect the changes in glucose concentration levels. Osmosis is defined as the solvent flow across the semi-permeable membrane driven by a difference in concentration levels, and then the osmotic pressure develops and molecules move from lower concentration to higher concentration. In this pressure sensor, we are using three types of principles like piezoelectric, capacitive and piezoresistive as shown in Fig. 1.

3 Results and Discussion

3.1 Microcantilever by Capacitive Principle

From Fig. 2, we have observed that when we applying the pressure as input then the nonlinearity and sensitivity also increase, here we are used three electrodes such aluminium, gold and platinum. Among all the three electrodes, aluminium has better nonlinearity. Figure 3 shows the sensitivity of the sensor when the pressure is applied from the range of 500–3000pa.

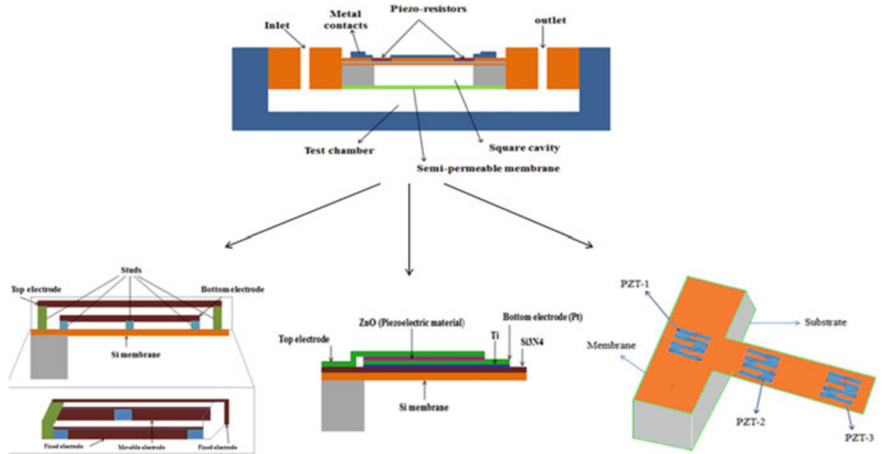

Fig. 1 Schematic view of glucose sensor **a** Capacitive microcantilever. **b** Piezoelectric Microcantilever. **c** Piezoresistive Microcantilever

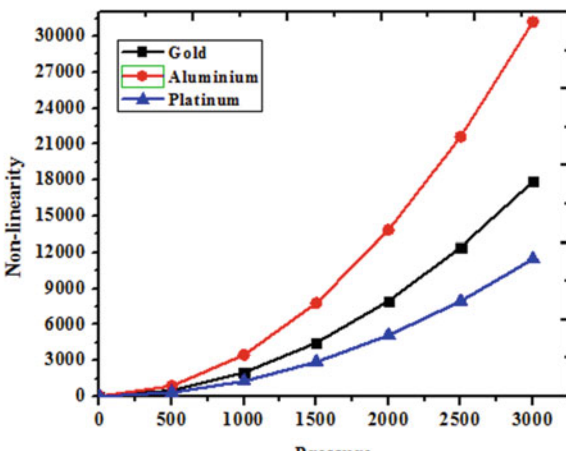

Fig. 2 Pressure versus nonlinearity for different materials

3.2 *Microcantilever by Piezoelectric Principle*

Figures 4, 5 and 6 show that when the pressure is applied, nonlinearity of the sensor increases. In this case, we have observed three materials zinc oxide (ZNO), barium titanate ($BaTiO_3$) and lead zirconate titanate (PZT) acting as piezoelectric materials, and three electrodes aluminium, gold and platinum. Figures 7, 8 and 9 show the sensitivity of the sensor when pressure is applied as input. Based on the both parameters nonlinearity and sensitivity, zinc oxide is the best material for the piezoelectric pressure sensor.

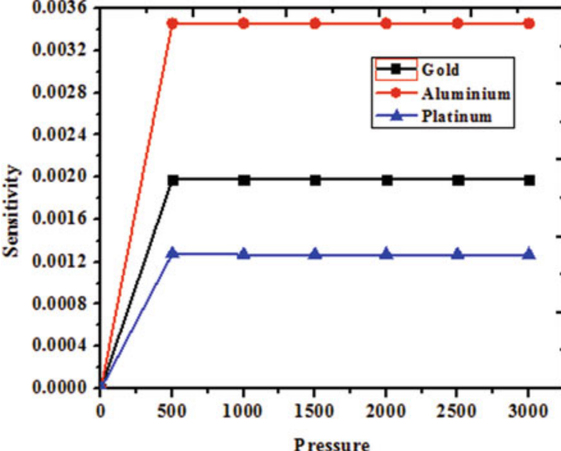

Fig. 3 Pressure versus sensitivity for different materials

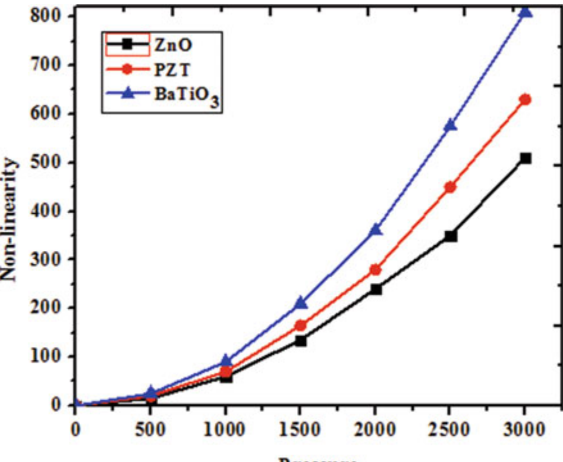

Fig. 4 Pressure versus nonlinearity for aluminium electrode with various materials

4 Conclusion

The microcantilever is designed and optimized with the use of FEM Tool. Three piezoresistors are placed on the top of the microcantilever, by integrating this microcantilever with the pressure sensor, and then we could calculate the change in resistance in the form of output voltage.

Different principles that are capacitive, piezoelectric and piezoresistive are used in microcantilever; among them, the piezoresistive microcantilever offers the best nonlinearity and sensitivity parameters of the pressure sensor as shown in Table 1.

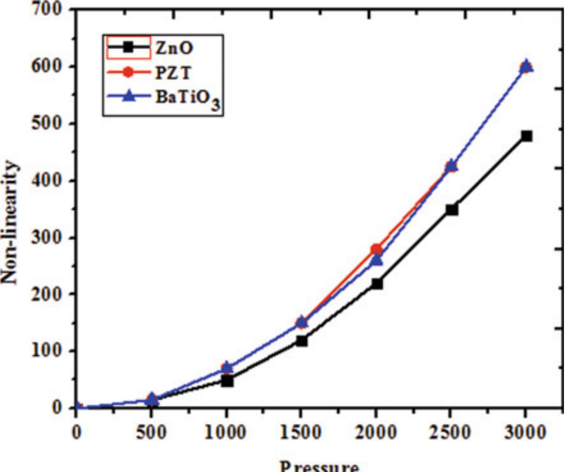

Fig. 5 Pressure versus Nonlinearity for gold electrode with various materials

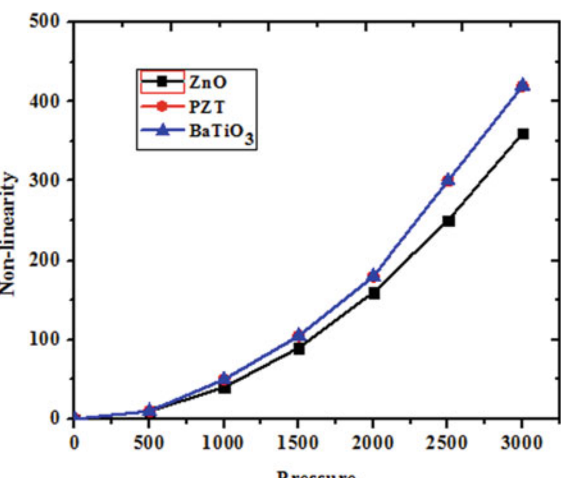

Fig. 6 Pressure versus nonlinearity for platinum electrode with various materials

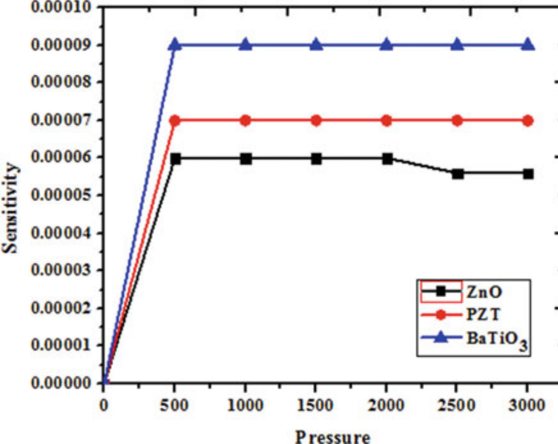

Fig. 7 Pressure versus sensitivity for aluminium electrode with various materials

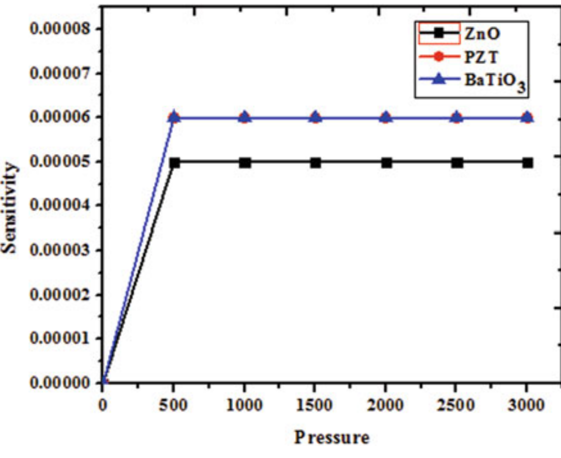

Fig. 8 Pressure versus sensitivity for gold electrode with various materials

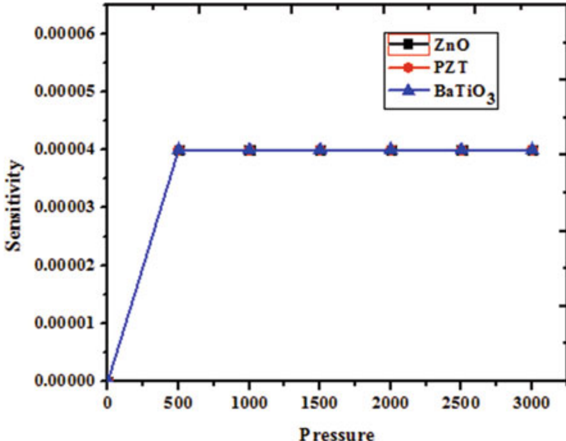

Fig. 9 Pressure versus sensitivity for platinum electrode with various materials

Table 1 Parameters comparison

Principles	Nonlinearity (%)	Sensitivity
Capacitive	50	$3.46e^{-5}$
Piezoelectric	47	$6e^{-5}$
Piezoresistive	30	$5.03e^{-9}$

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Impact of Quantum Wells on the Open-Circuit Voltage of the Kesterite Solar Cells

P. Chandrasekar, P. Sandeep Kumar, and Soumyaranjan Routray

Abstract The aim of this analysis was to investigate the quantum control of Cu2ZnSn(Sx,Se1-x)4, in which the S and Se propositions vary from 0 to 1. The spectral response of solar cells with recombination rate, energy band diagram, quantum efficiency with respect to absorption properties has been studied, resulting in a remarkable efficiency of 42% with a composition value of $x = 0.8$. The influence was investigated and evaluated mainly by the quantity of wells with a thickness of 10 nm and the different composition values of S/(S + Se). Barrier material CZTS has a wider bandwidth, whereas CZTSxSe1-x material also has a smaller bandwidth than the surrounding material to absorb photons at both lower frequency and higher frequency. With 45.702 (mA/cm2) Jsc and 1.03 V Voc, this analytic approach achieves optimum efficiency at 38%.

Keywords CZTSSe · Solar Cells · Kesterite · Multiple Quantum Well

1 Introduction

The conversion of photovoltaic energy from the Sun generates light energy. Light consists of energy packets called photons, the energy of which is solely dependent on frequency or colour [10]. Because of their direct band gap capabilities, Cu2ZnSn(S,Se)4 (CZTSSe)-based solar cells get more coverage. However, material (CZTSSe) efficiency is less than that of CIGS [3]. The efficiency reported as of now for CIGS is 23.35%, whereas CZTSSe was 12.6% [8]. A few logical works are in progress to help the nature of CZTSSe products around the globe. Particularly, the fuse of nanostructures in the material draws further interest [1]. The existence

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of a quantum well structure allows for the assimilation of both higher- and lower-frequency photons. The key issue depicted in CZTSSe was terrible showing because of high open-circuit voltage (Voc) and lower short-circuit current (Jsc). The execution of multiple quantum wells (MQW) in the CZTSSe expands the Jsc by limiting Voc[12]. *p—n* (barrier material) the solar cell is enclosed with a intrinsic territory that encloses electrons in 3D to 2D that tend to shift the useful state of electricity. The barrier material band gap will be higher than the well material band gap [2].

In this paper, we study the QW aspects of Courel [5] and Sravani's [12] previou work. In [5], CZTSSe was considered with the composition ratio *S* and Se and evaluated data until 50QW had been applied, whereas in [12], the authors performed 100QW numerical tests, in which CZTS and CZTSe were the barrier/well material with 5 nm/10 nm thick, respectively. We introduce QW structure with separate *S* and Se compositions of 100QWs. Atlas TCAD has been used to simulate the QW structure.

2 Device Structure

The CZTSxSe1− x material, which provides the p-i-n QW structure, is added between this barrier material. The planned structure consists of ZnO 200 nm, CdS 50 nm, an underlying well of up to 100 CZTS/CZTSSe well layers of 5 nm/10 nm, and CZTS 500 nm in bulk. For the different compositions, the band distance and affinity values (Table. 1) were calculated using Eqs. 1 and 2, where the bowing parameter b is labelled with 0.1 eV [4, 6].

$$E_g(\text{CZT}S_xSe_{1-x}) = (1-x)E_g\{\text{CZTSe}\} + xE_g\{\text{CZT}S\} - bx(1-x) \quad (1)$$

$$\chi(\text{CZT}S_x\text{Se}_{1-x}) = x\chi(\text{CZT}S) + (1-x)\chi(\text{CZTSe}) \quad (2)$$

The composition *S* and Se of the well is the '*x*' value that is obtained from the expression $x = S/(S + Se)$. Solar cell materials are mainly dependent on their absorption properties with respect to the spectrum. Any composition of CZTSxSe1-x has its own absorption properties. The absorption properties have been developed

Table 1 Band gap and affinity values

x	Material	Eg	Affinity
0	CZTSe	1.05	4.46
0.2	$CZTS_{0.2}Se_{0.8}$	1.124	4.388
0.4	$CZTS_{0.4}Se_{0.6}$	1.206	4.316
0.6	$CZTS_{0.6}Se_{0.4}$	1.296	4.244
0.8	$CZTS_{0.8}Se_{0.2}$	1.394	4.172
1	CZTS	1.5	4.1

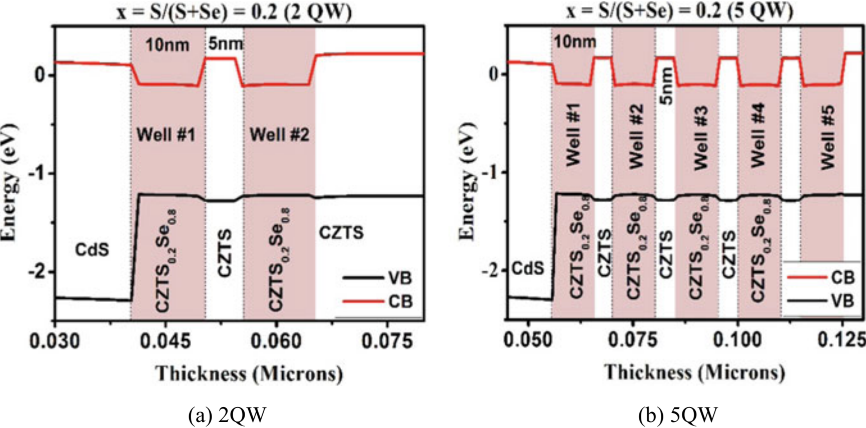
using Tauc Laurentz model for different composites S & Se [7]. Tauc density of states with Lorentz oscillations is given by Eq. 3 [9]

$$\varepsilon_{2TL}(E) = \begin{cases} \frac{(E-E_g)^2 A E_0 C}{(E^2-E_g^2)^2+C^2E^2} \cdot \frac{1}{E}, & E > E_g \\ 0, & E \le E_g \end{cases}, \tag{3}$$

where E_0, C, E_g and A—four fitting parameter.

3 Preliminary Results/Discussion

Within the electric field wave equation of Schrödinger, the quantum limits of the system have been studied and the eigenvalues of quantum wells are calculated [11]. Figure 1a and b displays the 2QW and 5QW energy band diagrams for $x = 0.2$ composition. This quantum energy levels make electrons generate and recombine. A solar spectrum of AM1.5 has been assumed with a frequency of 300–1300 nm wavelength in order to further explain solar cell emissions. The depth research was carried out using parameters such as recombination rate, photon generation rate, internal quantum efficiency (IQE), external quantum efficiency (EQE), short-circuit current (Jsc) and open-circuit voltage (Voc). Implementing QW increases electron–hole pair (EHP), resulting in a rise in electrical current in the barrier region, or nearby, as the thermionic emission escapes internally. Because of the strong electrical field at the well, the carrier exits more easily. Carriers that are not recombined in any structure can add further to the current density. Figures 2 and 3 indicate 2,3,4 and 5 QWs J-V for 0.2 and 0.4 composition, respectively.



(a) 2QW (b) 5QW

Fig. 1 Energy band diagram of CZTS0.2Se0.8 structure

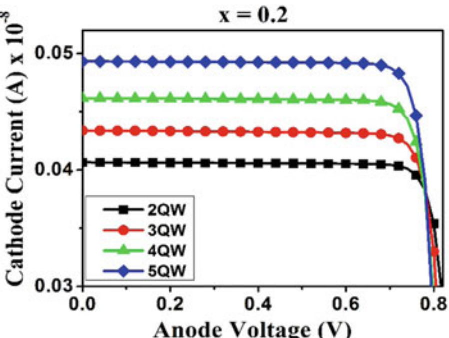


Fig. 2 JV curve of 2,3,4, and 5 QW of CZTS0.2Se0.8 structures

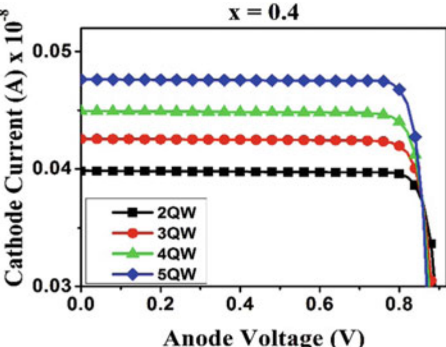


Fig. 3 JV curve of 2,3,4, and 5 QW of CZTS0.4Se0.6 structures

The graph (Figs. 2 and 3) shows that the rise in EHP generation results in more current density and a decrease in Voc as the number of wells increases. Table 2 lists the peak Jsc, Voc and efficiency of all four compositions.

On the other hand, Voc versus efficiency output graph comparisons were also drawn with respect to the QW number (Figs. 4 and 5). From Table 2, it is noted that for the composition value of $x = 0.8$ the QW solar cell achieves an efficiency of $\sim$38%, as described in [5]. The graph (Fig. 5) reveals that performance is saturated in 0.8 compositions after 50 QWs. It shows that according to the composite material, the rise in QW results in saturated performance.

Table 2 Maximum attained CZTSSe parameters

Parameters	0.2	0.4	0.6	0.8
Jsc(mA/cm2)	46.007	44.43	43.39	42.55
Voc(V)	0.748	0.823	0.907	1.02
Efficiency(%)	29.123	31.63	34.52	38.3

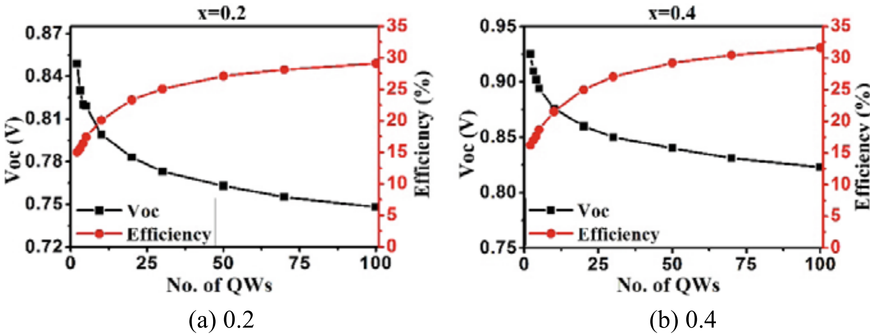


Fig. 4 Voc and efficiency of solar cell w.r.t. No. of QWs for **a** CZTS0.2Se0.8 and **b** CZTS0.4Se0.6

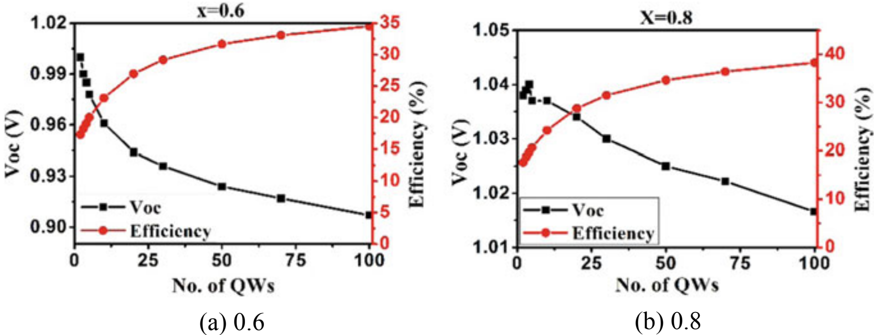


Fig. 5 Voc and efficiency of solar cell w.r.t. No. of QWs for **a** CZTS0.6Se0.4 and **b** CZTS0.8Se0.2

4 Conclusion

Including quantum wells, this research offers a theoretical examination of the different composition of S/(S + Se) data. The alignment of the composition of *S* and Se with their absorption results in the different values of Jsc and Voc, which in turn influences the overall performance of the solar cell. Findings have shown that the rise in quantum sources guarantees that EHP is produced or that photons are absorbed effectively by lower- or higher-frequency beams. The average output levels for all four CZTSxSe1-x formulations range from a minimum of 15.03 to a maximum of 38.3% in different quantum well quantity. This leads to further work on kesterite compounds in order to obtain greater potency in this substance due to structural variations.

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A 0.7 V 0.144 μW Frequency Divider Design with CNTFET-Based Master Slave D-Flip Flop

Uma Sharma and Mansi Jhamb

Abstract In this paper, flip flop-based frequency divider is proposed which is suitable for low voltage and low power design. Frequency divider is implemented using CNTFET-based master slave D-FF. For the design of frequency divider, various design parameters as delay in propagation (*tp*), power dissipation (pwr), Power Delay Product (PDP) and Energy Delay Product (EDP) are studied for a conventional master slave D-FF. These metrics are compared with design metrics of CNTFET (Carbon Nano-Tube Field Effect Transistor)-based master slave D-FF. Simulation results show that the CNTFET-based master slave D-FF offers high speed and less power dissipation. This research work proposes a power efficient frequency divider design that has total power consumption as low as 0.144 μW for 0.7 V supply. All the simulations are performed on HSPICE simulator at 22 nm technology.

Keywords Master Slave D-flip flop · Carbon Nano-Tube Field Effect Transistor · Frequency Divider

1 Introduction

In modern electronics, the domain of low voltage and low power encompass a tremendous share [1]. In digital integrated circuit design, designing of memory cell which comprises flip flop as basic element demands low power design. Almost in every digital integrated circuit design, use of flip flops is trending due to its distinctive characteristics. The speed of the circuit depends upon the latency of the flip flops, whereas power consumption depends upon the switching circuitry. Keeping this in mind, a low voltage low power CNTFET-based D-FF design helps in minimizing the overall power consumption and delay of the conventional CMOS-based D-FF design. CNTFET technology is becoming an emerging trend for power efficient applications.

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Downscaling of CMOS technology toward nano-technology effectuates design and reliability challenges and so greatly lessens the potential of CMOS technology for low voltage and low power applications. And also due to the additional scalability and less scale of CNTFET in comparison with MOSFET transistors makes it lucrative and suitable for low power applications [2].

In the communication system design, frequency dividers play a very important role in the field of different communication blocks such as PLLs, Frequency synthesizers and modulators. The speed of these blocks depends upon the circuitry of frequency divider. Various topologies such as LC-tank frequency dividers, Current Mode Logic frequency dividers, and flip flop-based frequency dividers are reported in the literature [3]. A wide range of topologies are used to optimize the design of D-FF such as POWERPC 603, DDFF, C2MOS, CPLSDFF, HLFF [4], etc. The use of CNTFET shows a great reduction in propagation delay and power consumption.

Flip flop is the basic memory element which stores two stable states 1 or 0, and therefore is known as a bistable element. D-FF is one of the important bi-stable elements for the designing of memory cells. The extended version of D-FF is known as master slave D-FF(MSD-FF). Actually, a D-FF operates only at single input, the D (data) input. The MSD-FF is edge-triggered, that implies, output toggles only when the clock makes a transition from high to low. The circuit symbol of MSD-FF is shown in Fig. 1. It consists of two D-FF one as master and another as slave. MSD-FF is implemented using CMOS inverter latch and pass transistor [5]. The circuit of MSD-FF using CMOS Inverter is shown in Fig. 2. D-FF is used to transfer the input to the output without any change, due to this fact it is also known as data flip flop [5]. Table 1 depicts the truth table of D-FF. In MSD-FF output of the first latch is saved in the second latch, when the clock is low, but there is no change in the state of the first latch. Therefore, output is taken only when there is a transition from high to low.

The characteristic equation of D-FF is given by

$$Q_{n+1} = D_n \tag{1}$$

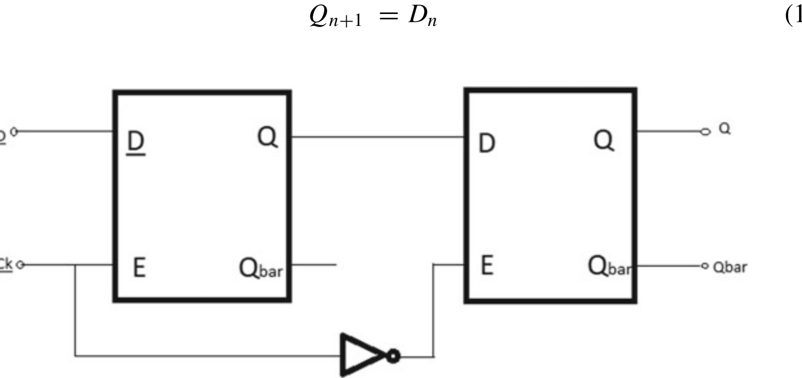

Fig. 1 Circuit symbol of MSD-FF

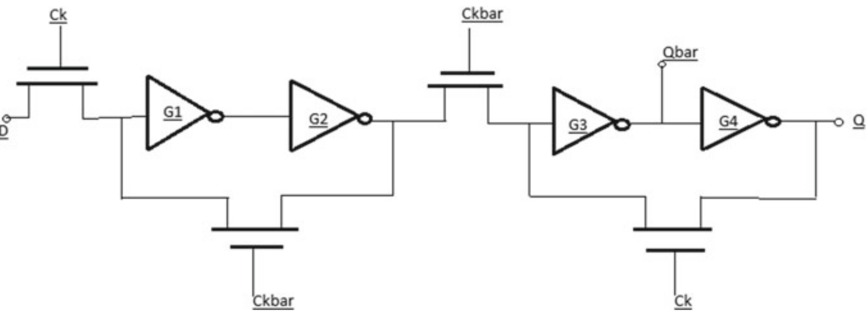

Fig. 2 MSD-FF using CMOS Inverter

Table 1 Truth table of D-FF

CK	*Dn*	*Qn* + 1
0	0	*Qn*
0	1	*Qn*
1	0	0
1	1	1

In this research work CMOS implementation of MSD-FF is presented; simulations are performed using HSPICE for 22-nm PTM [6]. Further, this conventional MSD-FF is implemented through a promising technology, CNTFET. The roadmap for this research paper is discussed hereafter. Section 2 describes the implementation of MSD-FF using CMOS and CNTFET technologies. In Sect. 3 simulations are presented for both the designs. In this section comparative analysis has been performed for CMOS- and CNTFET-based MSD-FF. Section 4 proposes a new CNTFET frequency divider as an application of MSD-FF as. In the same section simulation results are given for CNTFET frequency divider. Results and discussion appear in Sect. 5. Based on the comparative analysis finally this research work is concluded in Sect. 6.

2 CMOS Implementation of MSD-FF

MSD-FF is implemented using the most common synchronization element pass transistor at the input terminal and the CMOS inverter latch to store the data [7]. CMOS implementation of master slave flip flop is described in Fig. 3. In the integrated circuit design delay of the circuit depends upon the number of transistors used in the design and in the maximum circuit designs there is a bargain between power and delay. Therefore, for the design optimization it is required to have knowledge about power and delay. This research work presents the computation of two important low

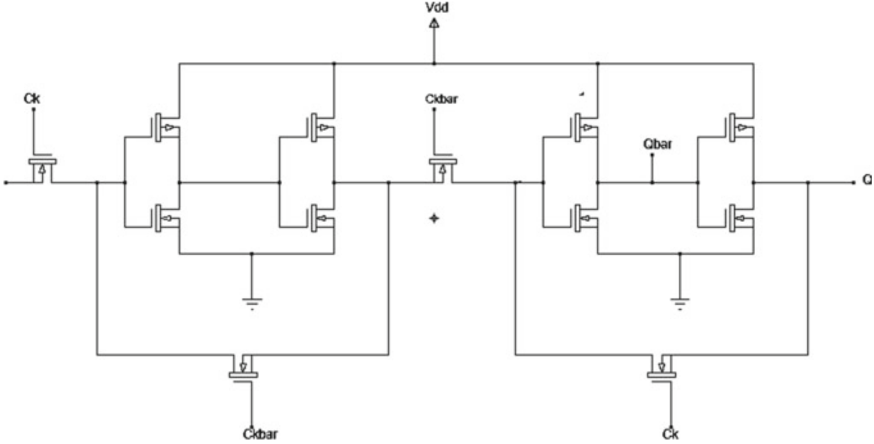

Fig. 3 CMOS-based MSD-FF

Table 2 Design metric of MOS-based MSD-FF

Device parameter supply = 0.7 V	CMOS-based MSDFF
tp (ns)	31.650
PWR (μW)	0.398
PDP (aJ)	12,596.7
EDP (aJ-ns)	398,685.55

power design parameters, EDP and PDP. These parameters are calculated at supply voltage of 0.7 V and the details are given in Table 2.

For the efficient low power design CNTFET technology is used to implement MSD-FF, as the emergence of nanotechnology started in the 21st century [8]. But miniaturization of device dimension after a certain limit may cause many problems in CMOS circuit design. After that the technology like CNTFET fulfills the demand of low voltage low power circuit design [8]. This CNTFET-based design is simulated using HSPICE by replacing MOSFET with CNTFET.

3 Simulation Results

Efficient implementation of CNTFET-based MSD-FF is implemented in the previous section that provides momentum to realize even better configuration for the same circuit. Extensive HSPICE-based simulation results are shown in Figs. 4 and 5. Calculations of delay, power, *PDP* and *EDP* have been performed with the help of these simulation results.

In this section, evaluation of the various design parameters, such as delay (*tp*), power (*pwr*), Power Delay Product and Energy Delay Product is performed. These

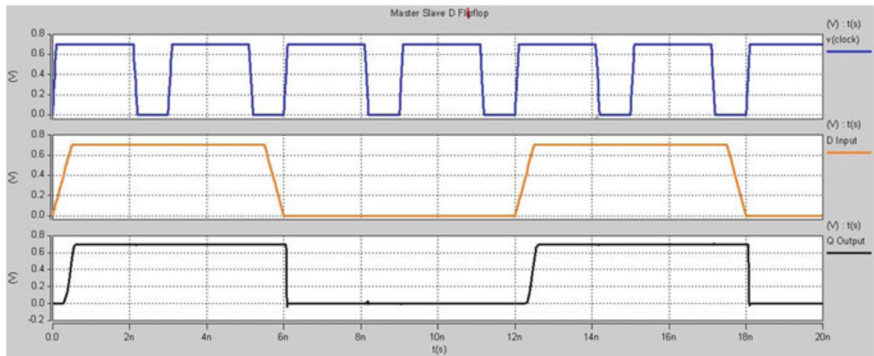

Fig. 4 Simulation result for MSD-FF using CMOS

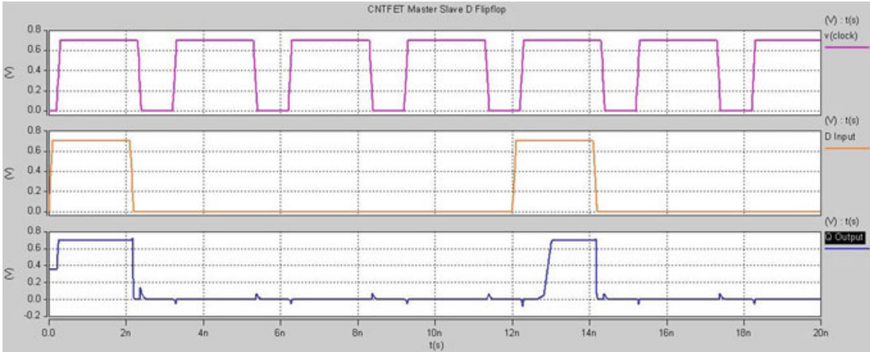

Fig. 5 Simulation result for MSD-FF using CNTFET

design metrics are also compared with the conventional MSD-FF. Both the circuits are simulated for 22 nm Technology node at 0.7 V supply (VDD). HSPICE-based simulated results are presented in Table 3. 3D stacked bar chart is also presented in Figs. 6 and 7 to make better understanding of the simulation results.

A comparative analysis of CNTFET-based MSD-FF with other existing designs has been carried out with help of the literature. Table 4 illustrates the comparison between CNTFET-based MSD-FF and other existing models. It is apparent from the

Table 3 Design metrics of CNFET-based MSDFF

Device parameter supply = 0.7 V	CMOS-based MSD-FF	CNFET-based MSD-FF
tp (*ns*)	31.650	0.0029
PWR (μW)	0.398	0.3943
PDP (aJ)	12,596.7	1.143
EDP (aJ-ns)	398,685.55	0.00319

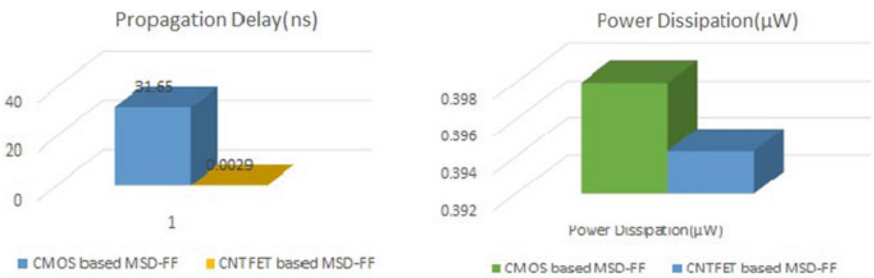

Fig. 6 Delay and power comparison between CMOS- and CNTFET-based MSD-FF

Fig. 7 PDP and EDP comparison between CMOS- and CNTFET-based MSD-FF

Table 4 Performance comparison of CNTFET MSD-FF

Methods	POWERPC603 [4]	C2MOS [4]	CPLSD FF [4]	MSD-FF	CNTFET MSD-FF
Technology (nm)	130	130	130	22	22
Power(μW)	4.89×10^3	2.794×10^3	2.17	0.398	0.394
PDP (aJ)	171.1×10^9	32.8×10^9	40.5	12.59×10^3	1.143
Transistor count	22	22	16	14	14

comparison table that the CNTFET technique provides very least values of PDP and power. In the next section CNTFET-based frequency divider is proposed that has least values of delay and PDP.

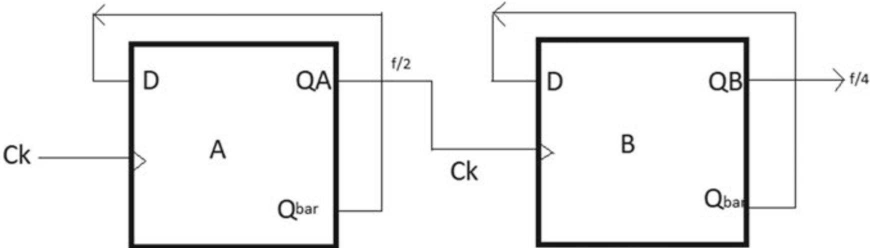

Fig. 8 Circuit symbol for MSD-FF-based frequency divider

Table 5 Design metric of proposed frequency divider

Device parameter supply = 0.7 V	CNFET-based frequency divider
tp (*ps*)	43.103
PWR (μW)	0.1444
PDP (attoJ)	6.182
EDP (attoJ-ps)	266.4

4 Proposed Design: Frequency Divider Using CNTFET MSD-FF

From the comparison table it is clearly observable that the CNTFET-based design provides very good results in terms of all the design metrics but especially CNTFET design offers very less delay as compared to CMOS-based design and this results in effective reduction in PDP. This magnificent CNTFET design is the superior alternative for the high-speed circuits like frequency dividers. Here, in this research work CNTFET-based frequency divider design is proposed. Circuit symbol for MSD-FF-based frequency divider is shown in Fig. 8. This design is implemented using CNTFET technology and simulation is performed with HSPICE simulator at 0.7V supply. For this outstanding design different design parameters are calculated and tabulated in Table 5.

The simulation results depicted in Fig. 9 and the design metrics of CNTFET-based Frequency divider which are drawn from the HSPICE simulation performed at 0.7 V supply shows the effectiveness of the proposed CNTFET-based frequency divider.

5 Results and Discussion

In this research work CNTFET-based low voltage low power design is proposed for Frequency divider. The proposed frequency divider design offers 0.144 μW power consumption and very less value of PDP as low as 6.182 attoJ. To evaluate the

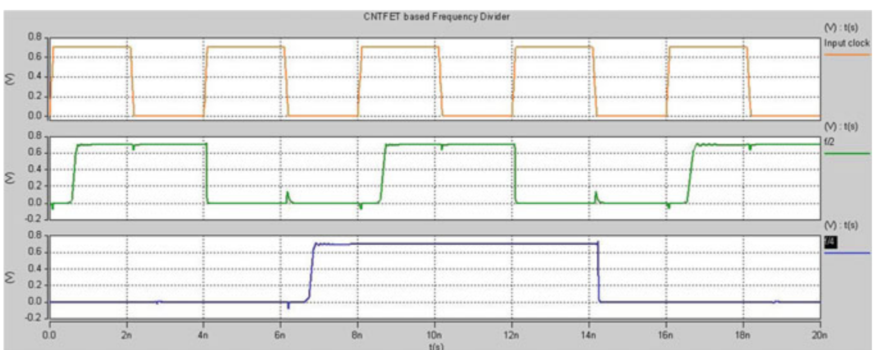

Fig. 9 Simulation results of CNTFET-based frequency divider

performance of different circuits discussed in this paper, design metrics such as *tp*, pwr, *PDP* and *EDP* are considered as important measures. This paper focuses on the efficient use of low power devices like CNTFET for the high-speed low power applications.

6 Conclusion

In this research work MSD-FF- and CNTFET-based MSD-FF are analyzed at 0.7 V nominal *V*DD using HSPICE simulator. The CNTFET MSD-FF shows better results, specifically 0.0029 ns delay and 1.143 aJ power delay product. These simulation results of CNTFET-based MSD-FF are extended to implement a new design of frequency divider. A flip flop-based frequency divider is proposed which results in 43.103 ps delay and 6.182 aJ power delay product. The proposed frequency divider design is a competent candidate for the high-speed communication circuits. The results of proposed frequency divider can be extended for the implementation of different sequential circuits such as counters and registers [9]. As sequential circuits are very essential part for the designing of memories and timers. In the near future we are planning to employ the proposed design in the sequential circuits.

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Radix-10 Multiplier Implementation with Carry Skip Adder Using Verilog

M. Shashikumar, Bhaskar Jyoti Das, Jagritee Talukdar, and Kavicharan Mummaneni

Abstract Multiplier plays a vital role in different applications hence more number of multiplier applications are available, as there is a high requirement of multipliers in the various applications, it is required to develop a high speed and area efficient multiplier. This article explains the design and development of high speed and area efficient multiplier using Verilog. In this work, a new 16 bit multiplication unit has been designed and implemented. The proposed multiplier will incorporate for developing the multiplier and it will be using a binary coded decimal adder and carry skip adder, and CSKA has a higher speed and lower energy consumption. For calculating multiples of multiplicand BCD Adder will be used and for calculating sum of partial products CSKA Adder will be used. Parallel path is used for carry propagation in the carry skip adder. Hence, time taken for propagation delay can be reduced in the adder. 16-bit Multipliers is designed, implemented and explained in this paper. The important factors need to improve for designing multiplier is less area, high speed and low power.

Keywords Radix-10 · BCD Adder · CSKA adder

1 Introduction

Multipliers play an important role in different systems such as microprocessor, FIR filters, digital processors, etc. Multipliers are part of electronic world. Multipliers are used in different electronic systems which performs various calculations such are micro controllers, microprocessors and digital signal processing processors [1]. Multipliers are also used in different algorithms like discrete fourier transform, fast fourier transform etc. Multiplication is an important arithmetic operation, and multipliers are developing from long back time. Multiplications were performing using the arithmetic logic unit's adder. Array multipliers were introduced because of increasing

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the clock rates and time limitation became important [1]. Low power and area efficient adder circuits have become very important in VLSI industry. Multiplication is regular and important operation in the mathematical calculation of decimal numbers. Multipliers are the important component in the microprocessor arithmetic units, DSP processors and multimedia etc. and also multipliers are used in many various applications. Hence, the design and implementation of low power, high speed and area efficient multiplier are very essential.

The implemented multiplier is a multiplication unit which performs multiplication using binary coded decimal adder and carry skip adder. Partial products can be reduced by using higher value number. Multiplication is done by using no. of additions, when performing multiplication initially we will get partial products, and then we have to add those partial products to get the final sum. Multiplier and multiple digits have to select to calculate the partial product. Using the modification of addition process, we can improve the multiplication process, generation and addition of partial product complexity can be decreased or reduced by modifying addition process. For multiplication, implementation multiplicand is multiplied by the each multiplier digit after multiplying, we get the partial product then every multiplier is multiplied to multiplicand so that we can get all the partial products then all the partial products are added to get the implemented multiplication. Here, three basic constituents are used to implement the multiplication of the given numbers. Multiples are calculated first in the multiple evaluation unit, second multiplier digits are calculated in multiplier decoding unit, and finally partial products are calculated in multiple accumulation unit.

Multiplication of decimal numbers is very important in many applications. In 2003, first multiplier was implemented and which performs decimal multiplication. In this multiplier, partial products are calculated using tree of carry save adder [2]. To achieve moderate area and high-speed carry save adder and counters were used in the multiplier [2]. Various methods and measurements have taken to enhance the generation and accumulation of partial products. In the revised class of parallel multipliers, the multipliers was implemented by using binary coded decimal adder and by utilizing carry propagation addition will be calculated and pre-correction of sum has to be performed [2, 3]. As there is an increasing in computational complexity, it is important to improve the operation of multiplication. We will try to implement the efficient multiplier in this project.

Partial product calculation process is simplified in each multiplier digit because binary addition is easier than the decimal addition [4]. Parallel multipliers are the fast one when compared to sequential multipliers, but in the parallel multipliers multiplicand multiple generations are involved.

The paper is classified into following divisions: Sect. 1 explains the highlights of an introduction part, Sect. 2 explains the work proposed, Sect. 3 explains the implementation and results, Sect. 4 explains the simulation results obtained through Xilinx ISE, and Sect. 5 concludes the work.

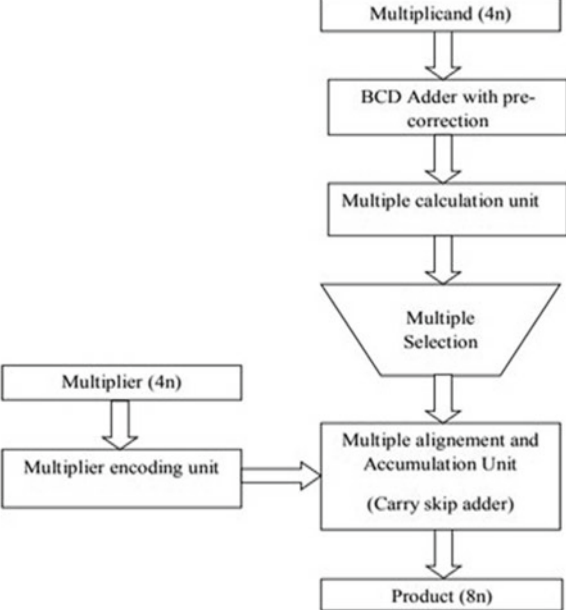


Fig. 1 Flow chart of multiplier

2 Proposed Work

The proposed and implemented multiplier uses carry skip adder for calculating the partial products and in this multiplier, we are not using extra recoding logic. To get the accurate addition of the multiples, pre-correction step is used in the BCD Adder [1]. Carry skip adder is used for the improvement of the multiplier, the carry skip adder is used when calculating the partial products, which makes the multiplier area efficient. The proposed and implemented multiplier is easy to calculate the multiples of multiplicand and the calculation of final sum (Fig. 1).

3 Implementation and Results

Algorithm for proposed multiplier is explained in this paper. For multiplication, we have considered a 4-digit number A (1234) and B (3456) as a multiplicand and multiplier, respectively. First, the multiplicand multiples are evaluated then recoding of multiplier digits have to be done, and then the partial products are calculated using the encoded multiplier bits. The final product is calculated using the partial products. The algorithms are explained below.

3.1 Multiple Calculation

Calculation of multiples is the first step in the multiplier here we use BEC-1 binary coded decimal adder is used to generate multiplicand multiples, {A, 2A, 3A, 4A, 5A} are the generated multiples.

2A is calculated by addition of A and A using BEC-1 BCD Adder [5]. Using BEC-1 BCD Adder 3A is calculated by adding A and 2A, similarly all multiples are calculated, we can observe the multiple calculation steps and multiples in Fig. 2.

We can observe binary coded decimal addition with pre-correction using BEC-1 BCD Adder, pre-correction is performed when the addition of two numbers is greater than or equal to nine, if addition of two digits is less than nine then we do not perform pre-correction step if addition of two digits is greater than nine or carry occurs then pre-correction has to be performed. To perform the pre-correction, we have to add

i. A+A=2A

		Cb=1	Cb=1	Cb=1	
A	3456	0011	0100	0101	0110
A	3456	0011	0100	0101	0110
A+6 For Cb=1		0011	1010	1011	1100
A	3456	0011	0100	0101	0110
2A		0110	1111	0001	0010
		0110	1001	0001	0010
				Correction	

ii. A+A=2A

A		0011	0100	0101	0110
2A		0110	1001	0001	0010
A+6 For Cb=1		1001	1010	0101	1100
2A		0110	1001	0001	0010
3A	0001	0000	0011	0110	1110
	0001	0000	0011	0110	1000
					Correction

(iii). A+3A = 4A

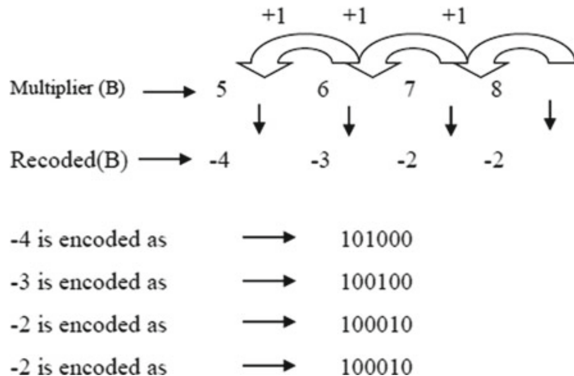
A		0011	0100	0101	0110
3A	0001	0000	0011	0110	1000
A+6 For Cb=1		0011	0100	1011	1100
3A	0001	0011	1001	0101	1000
4A	0001	0011	1000	0010	0100

(iv). A+4A

A		0011	0100	0101	0110
4A	0001	0011	1000	0010	0100
A+6 For Cb=1		0011	1010	0101	1100
4A	0001	0011	1000	0010	0100
5A	0001	0111	0010	1000	0000

Fig. 2 Calculation of multiples using BEC-1 binary coded decimal adder

Fig. 3 Multiplier decoding



correction factor (0110 is the correction factor), to get the final sum we should add 0110 (correction factor) with first digit and then we should add 0110 with the second digit then we get the final sum. 1110 and 1111 are the unused combinations, and this combinations are pre-corrected after pre-correction these combinations are taken as 1000 and 1001.

3.2 Accumulated Multiple and Multiplier Encoding

Partial products are obtained. If the multiplier digit is greater than five then it has to be recoded. If the sign bit occurs for a digit greater than or equal to five then the adjacent digit is increased by one bit. The numbers which are present between 6 to 9 are encoded as −4––1. Hence, the encoded digits are dissembled between −5 to + 5. Each number or digit is encoded into one signed bit and five selection bits. Now, let us consider the recoding of a digit less than or equal to five and the recoding of the digit greater than five. The partial product generation and the final sum (final product) are shown in Fig. 3.

3.3 For Multiplier Digits Greater Than or Equal to 5

Figure 3 shows the obtained partial products from the multiples using multiplier encoded selection bits [6]. The partial products are added and left shifted to get the final sum.

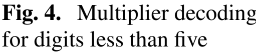
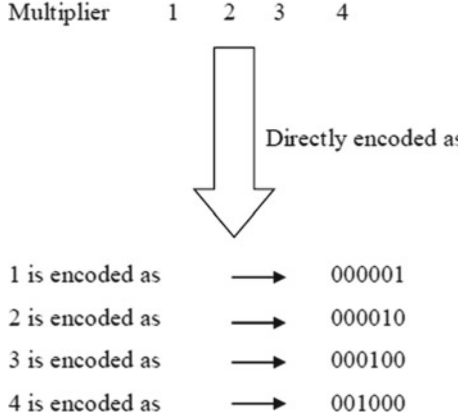


Fig. 4. Multiplier decoding for digits less than five



3.4 For Multiplier Digits Less Than Five

Not need to recode the digits of multiplier if the digits are less than five, we can use those values directly as it is for calculation. For example, if 1234 is a multiplier digit then it is encoded as follows.

According to the encoded multiplier [7] bits partial products are calculated by selecting multiples that can be seen from Fig. 4. The partial products are added and left shifted to get the final sum.

3.5 Partial Product Addition Using Carry Skip Adder

For getting final sum of the multiplier, we should add the partial products which are obtained in the previous stage using carry skip adder [8]. RCA (Ripple carry adder) is used in the implementation of carry skip adder and also carry skip adder is belong to the category of by-pass adder. The carry skip adder has a critical path. The carry skip adder starts at full adder passes through all the adders and stops at the final bit of the sum. Carry skip adder is efficient adder because of its low-power consumption and the less area. The structure of 4 bit carry skip adder is shown in Fig. 5 [9].

4 Simulation Results

Verilog HDL is used for multiplier design, and ISIM simulator is used for the simulation of multiplier. The simulated waveform of multiplier and carry skip adder and BCD Adder are shown in Figs. 6 and 7, respectively. In Fig. 6, a is 16 bit 4 digit multiplier number 1234, b is 20 bit 4 digit multiplicand number 3456, and fsumh &

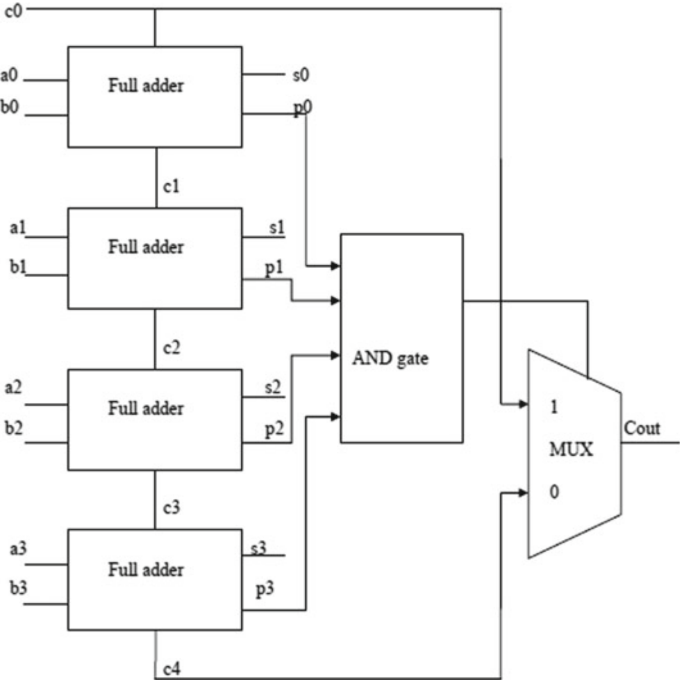


Fig. 5 Carry skip adder

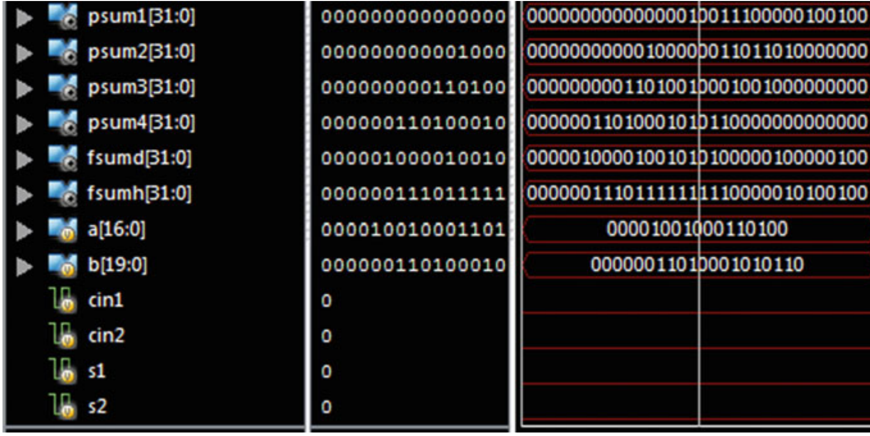


Fig. 6 Multiplier and carry skip adder results

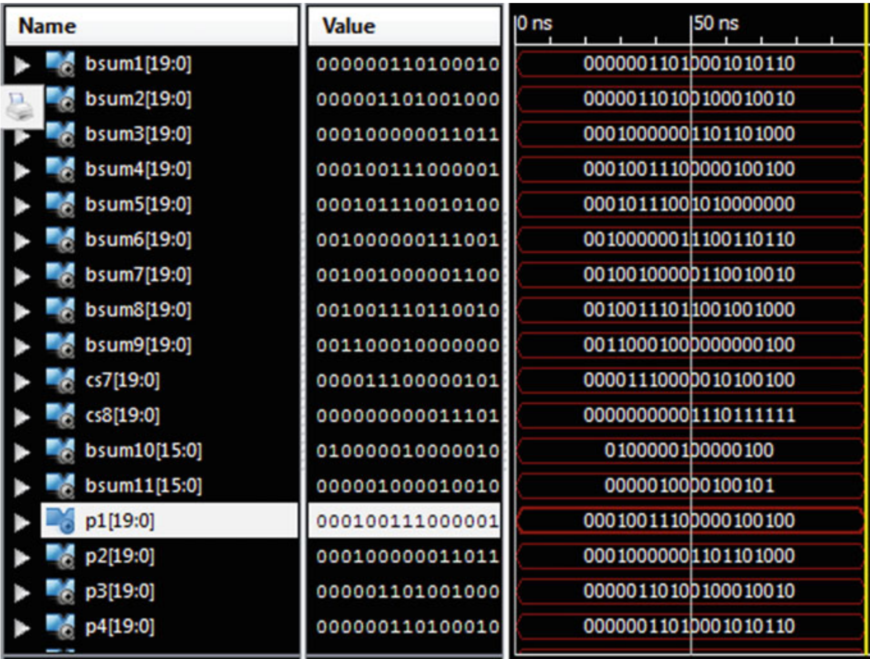


Fig. 7 Multiples of multiplicand calculation using BCD adder

fsumd 32 bit 8 digit number of final sum of multiplier is 04264704. In Fig. 7, bsum0 to bsum12 are the multiples of multiplicand, psum1 to psum4 are partial products, and cs1 to cs8 are the carry select adder outputs.

5 Conclusion

The algorithm for implemented multiplier is explained in this paper. Addition of partial products is calculated by using carry skip adder. Partial products are calculated using this algorithm from the multiples available using encoding multiplier bit. The implemented multiplier decreases the no. of gates used. Decreases the delay, as decreased no. of gates used the area will be decreased and power consumption also will be decreased. The circuit design become easy. Speed will be increased.

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Design and Analysis of FEM Novel X-Shaped Broadband Linear Piezoelectric Energy Harvester

M. Krishnasamy, J. R. Shinde, H. P. Mohammad, G. Amarnath, and Trupti Ranjan Lenka

Abstract This paper presents a novel simulation model of an X-shaped linear piezoelectric energy harvester for wideband applications. Moreover, the physical dimensions and material properties are taken as same as used in nonlinear H-shaped multimodal, which is experimentally analyzed in the literature. The designed FEM harvester model is analyzed for wideband applications in terms of displacement, optimum load resistance, maximum electrical and mechanical output powers, and efficiency. Furthermore, the results show that the novel X-shaped linear piezoelectric energy harvester produces more electrical response and efficiency. Finally, this work can be extended for the development of a numerical model with practical implementation in wideband applications.

Keywords Broadband energy harvester · COMSOL · Piezoelectric · Optimum load resistance

1 Introduction

Current research statistics have resulted that the carbon dioxide levels are increased by 134 parts per million in the last 150 years, and the temperature of the earth's surface has also increased by 1.73 °F [1]. However, the greenhouse effect combined with burning fossil fuel will increase the sea levels due to the continuous increment

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of carbon dioxide levels [2]. Hence, these effects are giving the alarm of the negative impact of usage of fossil fuels as a primary energy source. And also, it promotes the researchers to move in direction of the renewable energy sources.

There are many renewable energy sources are available such as wind, water, solar and kinetic motion, or mechanical vibrations. Moreover, a few energy sources are used in large-scale applications, but these sources are limited with dependent on nature like wind, water, and solar. Finally, kinetic motions or vibrations are considered very useful and also easily available in our human day-to-day life. Thus, vibration-based energy harvesting techniques play a vital role to replace the other techniques in renewable energy harvesting systems.

In a vibration-based energy harvester, the basic concept is that the mechanical vibration signal can be converted to an electrical signal. There are five main catteries: piezoelectric, electrostatic, electromagnetic, piezo-magneto-elastic, and triboelectric. In piezoelectric [3], the mechanical strains can be converted into electrical energy using the specific materials of a crystalline structure. Similarly, the variable capacitance between two dielectric materials can be used to generate electrical energy in the electrostatic method [4]. However, the magnetic field by the stationary magnet can be interacted by the moving coil due to external mechanical force. Thus, the changes in the electromagnetic field can induce electrical energy in electromagnetic energy harvesters [5]. The combinations of electromagnetic and piezoelectric techniques are utilized in piezo-magneto-elastic energy harvesters [6]. Recently, the theoretical and simulation models of triboelectric energy harvesters [7] are developed with two dielectric materials of opposite polarities.

Naturally, the vibration sources produce the mechanical signal in a wide band at a single frequency. Further, the linear piezoelectric energy harvester will give the maximum response at a single frequency as a resonator and it is not practically feasible for applications. In the recent scenario, the researchers are more interested to design and develop energy harvesters for wideband applications through linear and nonlinear methods. Also, the reliability and lifetime of nonlinear methods are limited due to nonlinear effects. Hence, the wideband linear piezoelectric energy harvesters can become more popular in recent research societies.

To achieve the wideband, Liu et al. [8] arranged the array of various lengths of the parallel cantilevers with tip mass. Here, the electrical outputs each are serially connected concerning a single drive circuit. The electrical responses are obtained from 19.4 to 51.3 mW for the bandwidth of 17 Hz (30–47 Hz) at the acceleration of 1.0 g. Similarly, R. Guillemet et al. [9] developed the novel concept of combining the electrostatic spring softening and mechanical spring shifting for harvesting the electrical power of 2 μW, bandwidth 22 Hz (140–162 Hz) at an external acceleration of 0.25 g with the load resistance of 5.4 MΩ. In this case, the polarization voltage is used for the electrostatic effects up to 30 V.

The parameters of parallel cantilevers with tip mass are analyzed through simulation models using COMSOL software for achieving the wide bandwidth response at a low-frequency range [10]. This work is reported that the bandwidth is increased

by 460% as compared to traditional devices. Also, the simulated results are experimentally validated at load resistance of 600 kΩ and acceleration of 1 g. The silicon-based S-shaped piezoelectric energy harvester [11] was designed and fabricated for harvesting the electrical voltage of 7.5 mV at a lower frequency (<11 Hz) with acceleration less than 0.2 g. Here, the developed device is limited to a single resonant frequency.

The aluminum nitride (AIN)-based piezoelectric energy harvester prototype [12] is developed for the bandwidth of 10 Hz with output voltage at 2.4–4 mW at an external acceleration of 0.1–0.6 g. H-shaped piezoelectric energy harvester [13] has been designed, and the three disk-shaped tip mass are attached with sandwiched spring flexures and a cantilever beam. Here, the two maximum peak voltages are separately harvested at 110 and 118 Hz through the main beam and sub-beam, respectively. Similarly, the hybrid multimodal [14] of H-shaped piezoelectric energy harvester is developed for wideband in lower frequency. In this work, the four consecutive resonant modes are used to improve the bandwidth. The simulation model of the designed device is presented using COSOL software for finding the eigenfrquencies and the mode shapes. Finally, the developed model is fabricated and the obtained results are as follows: the bandwidth 10 Hz and maximum power of 250.23 μW at a load of 90 kΩ under 0.4 g. Thus, we consider the physical dimensions and material properties of this designed model for further enhancement in linear response.

We designed herein a special structure of the X-shaped linear piezoelectric energy harvester for wideband applications. However, the consecutive four numbers of modes shapes can be taken into account which can produce only by the lateral displacement. In Sect. 2, the proposed linear piezoelectric energy harvester models with working principles are explained. In Sect. 3, the finite element method (FEM) of the designed model is utilized to obtain the mode shape with eigenfrquencies. The simulated results of the FEM model are discussed and evaluated in Sect. 4. Finally, the conclusions and future work are mentioned in Sect. 5.

2 Design and Working Principle

We proposed the model for harvesting the electrical energy from mechanical vibration of different frequencies. In this model design, the two symmetrical cantilever beams with cylindrical tip mass are connected in an X-shape with exact diagonal direction as shown in Fig. 1. The tip masses are added at end of the each cantilever beam to increase the average mechanical strain and stress levels and also to reduce the resonant frequency of the designed device. The center area of the X-shape is fixed with a cylindrical beam. It is used to allow the device to vibrate at its resonant frequency. The size of the base beam is 5 mm radius and length of 20 mm. Moreover, the unimorph piezoelectric layers are placed at the top of each cantilever beam which is covered by very thin electrodes. The mechanical effects and mass of these electrodes are not considered for the theoretical calculations due to the thickness of it.

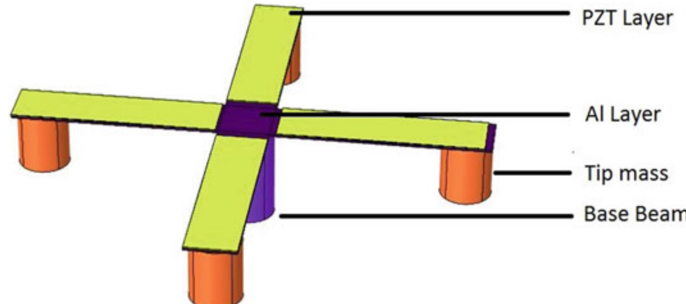

Fig. 1 Schematic diagram of designed X-shaped broadband linear piezoelectric energy harvester

Table 1 Physical dimensions and material properties of designed harvester [14]

Parameters	Value
X-shape cantilever beam	$93 \times 10 \times 0.4$ mm^3
PZT layer	$40 \times 10 \times 0.267$ mm^3
Young's modules Al beam	69 GPa
Young's modules PZT beam	62 GPa
Piezoelectric strain coefficient of PZT ($-d_{31}$)	320×10^{-12} C/N
PZT voltage coefficient of PZT ($-g_{31}$)	9×10^{-3} m^2/C
Relative dielectric constant of PZT	3800
Mass of tip mass	1.27 g

Here, the physical dimensions and material properties are considered as same as in [14] which are presented in Table 1. Also, the external sinusoidal accelerations can be given in z-direction as a lateral movement to the model. The harvester can harvest the electrical energy in the d_{31} mode of vibration.

In this designed model, the first four resonant frequencies are nearby to each other for providing the broadband energy harvesting systems. However, the initial six mode shapes are obtained and the 4th and 5th modes have produced the displacement in lateral with longitudinal directions which are shown in Fig. 2. Thus, the 4-Degree-Of-Freedom (4-DOF) model can be used for analyzing its operation. The simulation model of the designed device can be developed using a FEM tool in COMSOL multi-physics.

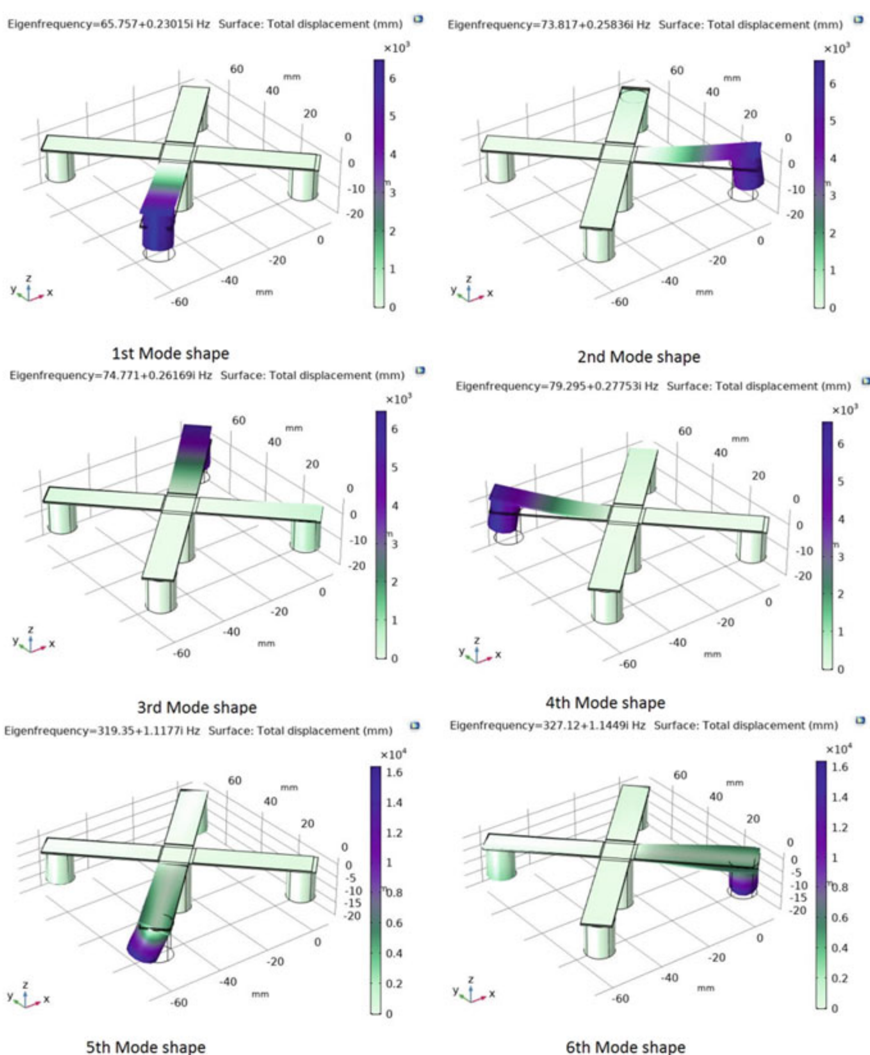

Fig. 2 Simulated mode shapes of the designed energy harvester

3 Simulation Model Using Finite Element Methods (FEMs)

In the research, the simulation model of the designed harvester can be developed using COMSOL software in 3D elements [15]. However, the generalized formulation of Hamilton's principle can be used in this model for developing the beam elements. These 3D beam elements have the capabilities to generate the basic block element for many smart structures, particularly in Micro-Electro-Mechanical

Systems (MEMS). Furthermore, these elements are considered inactive substructures that can be connected with the PZT layer. Firstly, the finite numbers of inactive elements are formulated. Secondly, the mechanical properties (strain, stress, and displacement) and the electrical properties (potential and fields) are generated to physical dimensions and input acceleration. Following that, the discretization is evaluated through FEM, and then, these terms are obtained for the active beam element. Similarly, the mechanical DOFs are used to separate the mechanical parameters like strain, stress, weight, and electromechanical coupling matrices in static and dynamic analyzes. Generally, the following process is followed for the transformation of element matrices as like as from secondary to primary local coordinate systems and from primary to global coordinate system. In this way, the designed simulation model can be analyzed through the proposed formulation.

In this FEM model, the PZT-5A and aluminum materials are used as piezoelectric layer and substructure, tip mass base beam, respectively. The physics of solid mechanics, electrostatics, electrical circuits, and piezoelectric effects are applied to generate the performance of the harvester. Additionally, the isotropic damping effect of concerning materials is also used. Moreover, the meshing, boundary, and edge elements are 172,058, 70,640, and 3671. Eigenfrequencies analysis is used to find the natural frequency at no-load conditions. Natural frequencies of the first six modes are obtained as 65.76, 73.82, 74.77, 79.30, 319.35, and 327.12 Hz. The frequency-domain analysis with parametric studies is used to obtain the electrical output parameters like voltage, current, Root-Mean-Square power, optimum load resistance, and mechanical power. Finally, these results are analyzed as per the standard producers which are mentioned in the literature.

4 Results and Discussion

The simulation FEM model can be used to characterize the mechanical and electrical energy harvesting performance of the X-shaped broadband linear piezoelectric energy harvester. Here, the harmonic input mechanical vibration is given to the designed model at the frequency range of 65–85 Hz. However, this FEM model has produced the lateral displacement only in the first four mode shapes. Thus, the d_{31} polarization PZT layers are sufficient to harvest the electrical energy for broadband applications [16].

Figure 3 shows the tip displacement amplitude of each cantilever beam in the z-direction; these obtained displacements are considered by the total harmonic body load at different frequencies in frequency-domain studies. The body load can be analytically calculated by the FEM model by multiplying the total density of the device with acceleration. However, the displacement of the 4th beam is more than other beams at primary mode. Also, the broadband displacement is achieved by 1st and 2nd beam in 2nd and 3rd mode shapes, respectively. Hence, the electrical energy harvesting performance is directly proportional to the displacement of beams which is justified in Fig. 4.

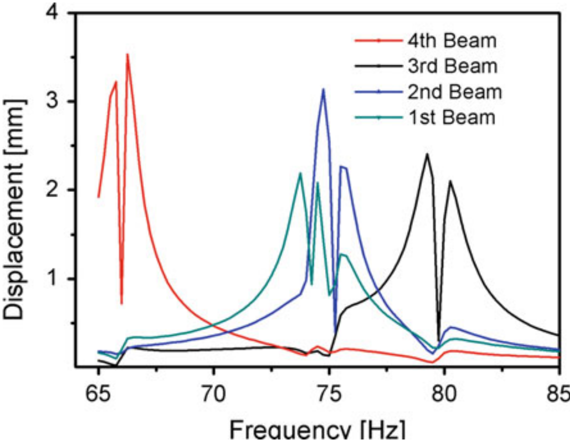

Fig. 3 Simulated tip mass displacement of each beam in z-direction using FEM model

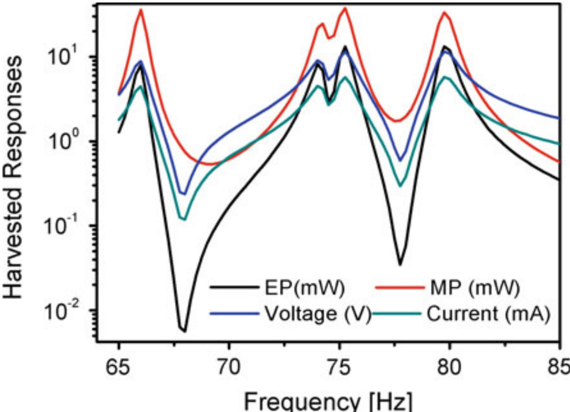

Fig. 4 Simulated electrical and mechanical responses FEM model under $R_L =$ 20 kΩ, acceleration = 1 g.(EP—electrical power—and MP—mechanical power)

In Fig. 4, the electrical and mechanical responses are symmetrical in all modes due to linear symmetric piezoelectric elements. Even though, the quantities of the harvested response are different in each mode because of the variations in stress levels on the piezoelectric elements. Here, the maximum total electrical power of 13.3 mW is obtained at 79.75 Hz in the 4th mode due to more displacement of all beams as shown in Fig. 3. Similarly, the maximum displacement is given by the 4th beam at primary mode, but the total displacement is less than the 4th mode. Hence, the maximum output electrical power is 5.4 mW less in primary mode. It concludes that the electrical responses are dependent on the total displacement of each beam. The output responses of mechanical and electrical power are 36 and 7.9 mW in the first mode, 24.67 and 8.19 mW in the second mode, 37.48 and 13.27 mW in the third mode, and 33.58 and 13.3 mW in the fourth mode, respectively. Thus, the harvesting efficiencies are 21.94, 33.2, 35.54, and 39.4% for the concerning modes. It is observed that the efficiency of the designed harvester is more in the 4th mode as

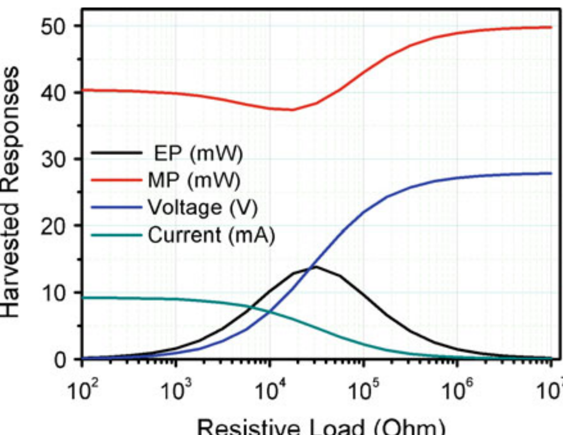

Fig. 5 Simulated electrical and mechanical responses as a function of external load resistance at acceleration 1 g at frequency 75 Hz

compared to other modes due to a higher value of the electrical response as shown in Fig. 4. It results in the anti-resonant frequencies and responses in between the two successive modes. To improve the broadband frequency responses, the anti-resonant responses can be removed by including the nonlinear effects.

The output electrical and mechanical response is analyzed as a function of external resistive load under the acceleration of 1 g at a single frequency of 75 Hz as shown in Fig. 5. Moreover, the mechanical power approximately becomes constant in minimal and maximum resistive load resistances; the transient response has occurred from 3 to 17 MΩ. Similarly, the harvested electrical power is also obtained for the peak value of 13.86 mW at 31.6 kΩ. Hence, the external resistive load is optimized, whereas the efficiency of the harvesting system will be maximized at 31. 6 kΩ. Also, the harvested electrical voltage and current are obtained and analyzed as a function of the resistive load. Here, the harvested current responses are maximum at the lower side and the voltage responses are maximum at the higher side of total resistance.

5 Conclusions

This research paper presents the simulation model of a novel X-shaped linear piezoelectric energy harvester for broadband applications using the COMSOL software. Moreover, the mechanical and electrical responses are obtained and analyzed as a function of vibrational frequency and external resistive load. Also, the eigenfrequencies and optimum load resistance are identified to harvest maximum power. Furthermore, this research work can be extended toward developing the numerical model using MATLAB software with fabrication for validating the FEM model results. Also, the FEM-designed model results may be individually analyzed in each beam

for the first four modes through different load resistance. Finally, the physical dimensions of the designed model may change for implementing the harvester in practical applications like a source of the running Inverter power supply and AC machine.

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Efficient Full Adder Design Based on New Reversible Tuned Fredkin Gate (TFG)

Makumsibou R. Zeliang, Malvika, and Kavicharan Mummaneni

Abstract Reversible logic is becoming one of the highlights of innovative research trends in recent times. It has proved to be a promising candidate for the applications in nanotechnology, quantum computations, and low-power CMOS devices. The need for miniaturization and low power electronics is an ever-emerging research area in lowering power consumption and heat dissipation. In this paper, we are introducing an efficient design approach for a reversible full-adder. This is achieved by introducing a new universal gate called Tuned Fredkin Gate (TFG), which is able to synthesize any Boolean function. Quantum realization of Feynman, Fredkin, and also TFG gate is presented here. The proposed full-adder design outperforms various existing designs based on quantum measures like quantum cost (QC), ancilla inputs (Constant inputs), garbage outputs (GO), and delay. It has shown a reduction in quantum cost by 1 unit, in constant input by 100%, in garbage output by 50%, and in delay by two gate counts. The performance analysis was carried out in Xilinx Vivado 2016.1 environment using Verilog. Moreover, the simplicity in the design structure compared with the existing counterparts makes it a viable choice over other existing ones.

Keywords Reversible gate · Quantum cost · Garbage output · Tuned Fredkin Gate (TFG)

1 Introduction

Current computers in the market are much compact, quicker and more efficient than older generations. The major cause for this advancement comes from the rising number of transistors embedded onto a chip. For any digital computer, logic levels are defined as either 0 or 1, known as bit. Every operation on a computer is relative to manipulating these bits, i.e., flipping of 1–0 s and vice versa. Classical computation

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is irreversible by its nature, basically meaning that input cannot be restored from its output.

According to R. Landauer [1], any logical reversibility is closely linked with its physical attributes. Additionally, it requires a minimum heat generation for each cycle of logical computations that are irreversible. For a single bit of lost information, it yields energy of KT × ln2 joules, where K equals 1.3807×10^{-23} J/K denotes "Boltzmann's constant" while T denotes temperature. At 300 K, for a single bit, the quantity of heat dissipated seems minimum but non-negligible at 2.9×10^{-21} J. G. E. Moore [2] forecasted that the rate of increase in transistors on a chip would double about every two years, which is popularly known as the "Moore's law." In line with this effect, the growth of elements onto a chip would also be leading to more power dissipation. Bennett stated that zero power dissipation for any operation can be achieved when executed in a logically reversible manner. The reason being that the quantity of energy released in the system forms a direct relation with the number of lost bits in the course of its operation [3].

In a reversible system, circuits do not erase information and so the information is not lost. These circuits are capable of producing unique o/p (output) vectors from their i/p (input) vectors means that there exists a one-to-one mapping between them and vice versa. Correspondingly, heat dissipation is reduced and hence allows higher transistor densities with incredible speeds. Additionally, through reversible computing, there is also a minimal impact on physical entropy. But there are certain crucial design constraints of reversible circuits enlisted as follows:

1. Reversible gates do not permit fan-outs.
2. It should use a minimal number of reversible gates.
3. It should keep quantum cost minimal.
4. It should produce the least possible garbage outputs.
5. It should use a minimal number of ancilla inputs.
6. It should have optimized gate levels or logical depth.
7. It should have a low power requirement.

2 Basic Definitions Associated with Reversible Logic Gate

There are several quantum measures like constant input, garbage output, quantum cost, delay, and gate count that are essential metrics to look at while designing any reversible logic circuit.

2.1 Constant Input/Ancilla Input

Ancilla input is the number of i/ps maintained constant either at 1 or 0 for the logical function to synthesize to keep the circuit reversible. Constant inputs are also called ancilla inputs.

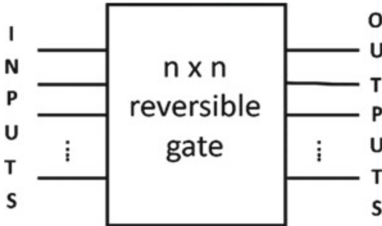

Fig. 1 Schematic of n × n reversible gate

2.2 Garbage Output (GO)

GO is the number of o/ps that are not utilized in its circuitry. The number of i/ps and o/ps should be the same in order to preserve reversibility. So, the outputs required to ensure reversibility through the one-to-one mapping between the i/ps and o/ps are called GOs. A relation can be drawn between the ancilla input and GO as [1].

$$\text{inputs} + \text{ancilla inputs} = \text{outputs} + \text{garbage outputs} \tag{1}$$

2.3 Quantum Cost (QC)

QC is considered as the cost associated with its primitive logic gates to realize the circuit [4]. So, the QC for any circuit is simply the number of either 1 × 1 or 2 × 2 primitive gates needed to realize that reversible logic circuit. The two primitive gates are namely NOT (1 × 1) and Controlled-NOT (2 × 2) gates with a QC of zero and one, respectively [5].

NOT gate. It is the simplest quantum gate (1 × 1) with QC as zero and unity delay as depicted in Fig. 2a.

Controlled-V and Controlled-V + gates. These two primitive gates are described in Fig. 2b, c. They share some properties, as shown in Eqs. 2, 3, and 4 [6].

$$V * V = \text{NOT} \tag{2}$$

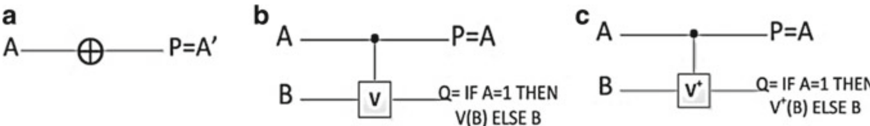

Fig. 2 **a** 1 × 1 NOT. **b** 2 × 2 Controlled-V. **c** 2 × 2 Controlled-V^+ gates

$$V^{+} * V^{+} = \text{NOT} \tag{3}$$

$$V * V^{+} = V^{+} * V = I \tag{4}$$

2.4 Delay

Delay can be defined as the "unit time" taken by each gate to compute the output from its given input. A unit time is taken as 1Δ. Considering *logical depth* is the shortest pathway from an input to an output having minimum reversible gates. This correlates to the total count of reversible gates coming on its track [6], i.e., it can be taken as a measure of delay as suggested in [7]. Delay of both 1×1 and 2×2 primitive gates is equal to 1.

3 Fundamental Reversible Gates

Basic reversible logic gates used in quantum computing are also called qubit gates. At present, we can find numerous existing reversible gates throughout the literature [8]. Some essential qubit gates discussed in this paper are the Feynman gate, Fredkin gate, and our proposed TFG gate.

3.1 CNOT / Feynman Gate (F)

CNOT or F gate is a 2×2 reversible gate, having one input variable directly going as one output variable. The i/ps are A and B while the o/ps are P and Q, which is shown in Eq. 5. CNOT gate has a QC of 1. It is mostly used as a copying gate and also as an inverter. Figure 3b demonstrates the quantum representation of F gate. Delay, according to [7, 9], is 1Δ.

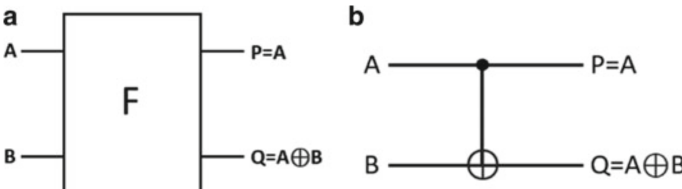

Fig. 3 **a** CNOT/Feynman gate. **b** Quantum equivalent of Feynman gate

$$P = A;\ Q = A \oplus B \tag{5}$$

3.2 Fredkin Gate (FG)

FG is a 3 × 3 universal gate, as represented in Fig. 4a. Let us consider A, B and C as our i/ps and P, Q and R as our o/ps. Individually, the o/ps are given as shown in Eq. 6. For i/p $A = 0$, we get $Q = B$ and $R = C$. For i/p $A = 1$, we get $Q = C$ and $R = B$. In Fig. 4b, each dotted rectangular box has a QC of 1. Therefore, the design for an FG gate involves a QC of 5. Figure 4b demonstrates the quantum equivalent of FG gate. Delay obtained according to [7, 9] is 5Δ.

$$P = A;\ Q = \bar{A}B \oplus AC;\ R = AB \oplus \bar{A}C \tag{6}$$

4 Proposed 3 × 3 TFG Gate

The proposed 3 × 3 reversible gate, TFG (Tuned Fredkin Gate) is shown in Fig. 5a. The i/ps are "A, B, C" while the o/ps are "P, Q, R", which is shown in Eqs. 7, 8, and 9. TFG gate has a QC of 6, i.e., one cost more than the FG gate. However, this consideration highly minimizes the overall quantum parameters, as shown later in

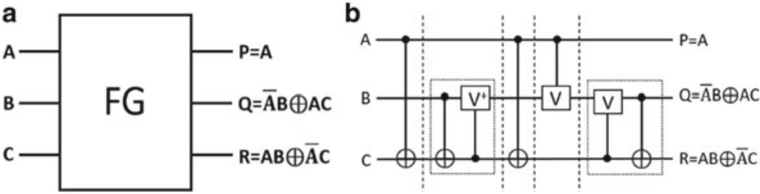

Fig. 4 **a** Fredkin gate. **b** Quantum equivalent of Fredkin gate

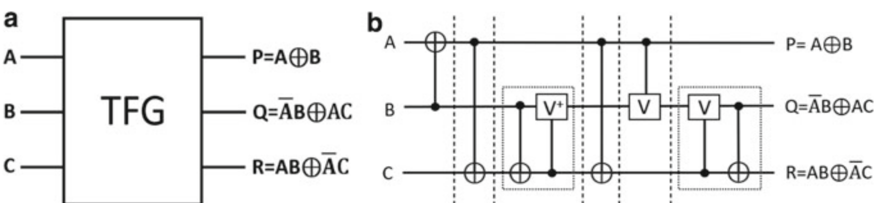

Fig. 5 **a** TFG gate. **b** Quantum equivalent of TFG gate

Table 1 Truth table of 3 × 3 TFG gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	1	1	0
0	1	1	1	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	0	1	1

our proposed design.

$$P = A \oplus B \tag{7}$$

$$Q = \bar{A}B \oplus AC \tag{8}$$

$$R = AB \oplus \bar{A}C \tag{9}$$

The quantum representation for a TFG gate is represented in Fig. 5b. TFG is itself a universal gate capable of implementing other logic gates. The implementation of the TFG gate involves a QC of 6. Its truth table can verify the TFG gate to see whether the i/ps and o/ps have a one-to-one mapping between them. We can observe from Table 1 that all eight different i/p and o/p vectors are uniquely mapped, and thus the TFG gate fulfills the condition of reversibility.

4.1 Realization of Basic Logic Gates

Since TFG is a universal gate, we can "program" it to virtually function like any conventional logic gates as desired for our circuit, as shown in Fig. 6.

NOT gate/FAN-OUT. For i/ps $B = 0$ & $C = 1$; we get $P = A$, $Q = A$ and $R = \bar{A}$.

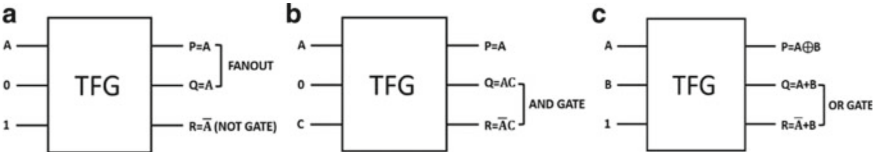

Fig. 6 TFG as **a** NOT, **b** AND and **c** OR gates

AND gate. For i/p $B = 0$; we get $P = A, Q = AC$ and $R = \bar{A}\ C$.
OR gate. For i/p $C = 1$; we get $P = A \oplus B, Q = A + B$ and $R = \bar{A} + B$.

5 Reversible Adder Designs

full-adder forms a foundational building block for numerous computational designs. We have the outputs in a full-adder block, namely as "Sum and Carry," which is expressed as follows:

$$\text{Sum} = A \oplus B \oplus C\text{in}; \quad \text{Carry} = C\text{in}\,(A \oplus B) + AB \tag{10}$$

Several reversible logic designs are discussed in [10–15], which compute both Sum and Carry. The literature in [10–18] has shown various quantum cost-efficient full-adder designs which have been realized using Fredkin gate, New gate, Peres gate, HNG gate, MHNG + TKS gate. Reversible adder based on a new single gate called TSG having one constant input, 2 GOs and a QC of 13 with a delay of 13Δ was represented in [14].

5.1 Existing Adder Design 1

The adder design 1 in [16] is shown in Fig. 7a, which involves 5 Feynman gates and 1 Fredkin gate. The first two F gates are used to set up fan-out signals, while the other three are used for generating *Sum*. Here, FG gate is utilized to generate *Cout* based on Xi or Yi. The adder design 1 comes with two ancilla inputs, 3 GOs, and a QC of 10 with delay as 3F for *Sum* signal and 2F + 1FG for *Cout* signal generations. Also, in adder design 1, *Sum* and *Cout* signals are produced simultaneously.

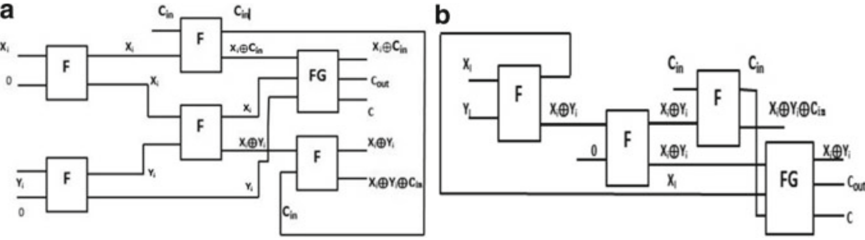

Fig. 7 **a** Existing adder design 1. **b** Existing adder design 2

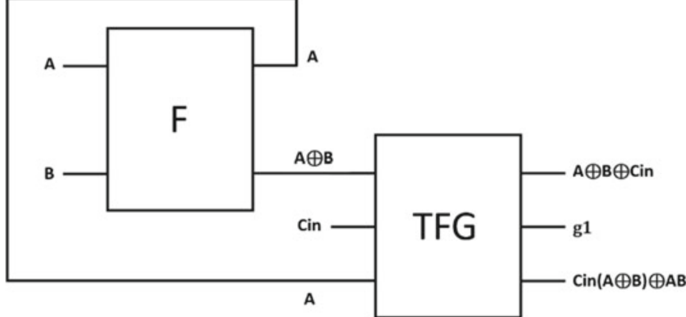

Fig. 8 Proposed full-adder design using Feynman (F) and tuned Fredkin (TFG) gates

5.2 Existing Adder Design 2

The adder design 2 is considered the improved one in [16], as depicted in Fig. 7b. It involves 3 Feynman gates with 1 Fredkin gate. The first F gate is used to set up the fan-out signal, while the remaining two are used for generating *Sum*. The Fredkin gate is used for generating *Cout* based on either Xi or Cin. The adder design 2 consists of 1 constant input, two garbage outputs, and a QC of 8 with associated delays as 3F for *Sum* signal and 2F + 1FG for *Cout* signal generation. In adder design 2, the *Sum* signal is generated before the *Cout* signal.

5.3 Proposed Work

Analyzing both the above designs, an efficient design method is proposed as depicted in Fig. 8. The proposed circuit requires only one 2×2 Feynman gate and one 3×3 TFG gate. It has two gates less than the improved design discussed in [16] and has a minimized quantum cost of 7. It produces only one garbage output with the constant input completely reduced to Zero. In this design, the *Cout* signal and *Sum* signal are generated simultaneously in 1F + 1TFG. The proposed reversible gate TFG is better suited for Adder operation than the regular Fredkin Gate. Therefore, it is observed that our presented approach is outperforming those two methods discussed in [16].

6 Simulation Results and Analysis

The proposed design was prepared using Verilog, and the Simulation was carried out in Xilinx Vivado 2016.1 platform. The functionality of the entire design was tested and verified using a test-bench. The output simulation waveform for every i/p combination corresponding to the proposed adder approach is depicted in Fig. 9. The

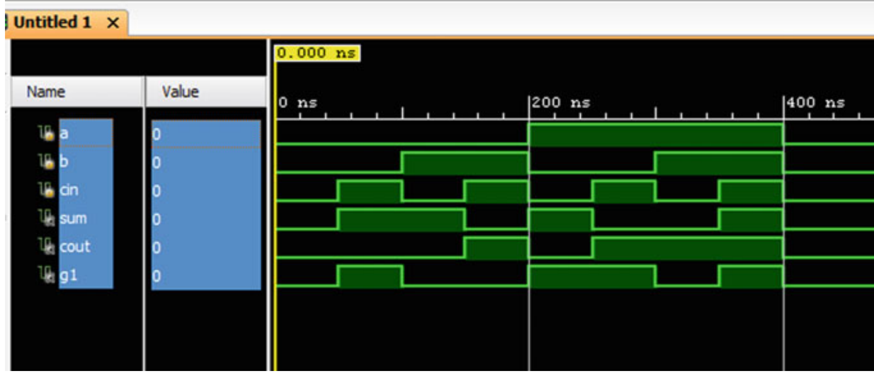

Fig. 9 Simulation waveform of full-adder

three i/ps are named as a, b and cin, while the three o/ps are named as *sum*, *cout*, and *g1*. Sum and Cout signals are available simultaneously. *g*1 is the only unwanted output, as shown, which could be utilized in future designs (Table 2 and 3).

Table 2 Comparison of various parameters of different adder designs

Circuit design names	Parameters			
	Quantum cost	Garbage output	Ancilla input	Number of gates used
Full-adder using DKG gate [12]	11	2	Unspecified	Unspecified
Feynman gate- and Fredkin gate-based full-adder 1 [16]	10	3	2	6
Feynman gate- and Fredkin gate-based full-adder 2 [16]	8	2	1	4
Proposed TFG gate-based full-adder	7	1	0	2

Table 3 Comparison of delays of various adder designs

Name of the circuit design	Delay	
	Sum	Carry out
Feynman gate- and Fredkin gate-based full-adder 1 [16]	3F	1FG + 2F
Feynman gate- and Fredkin gate-based full-adder 2 [16]	3F	1FG + 2F
Proposed TFG gate-based full-adder	1F + 1TFG	1F + 1TFG

7 Conclusion

The proposed design is implemented with a minimal QC of 7, while GO has also been reduced to half of the best performing designs. Constant input has been completely reduced to zero, a remarkable observation among all other existing designs. When we consider a delay in logical depth, it is 1 and 6Δ for Feynman and TFG gates, respectively. The proposed design offers the best balance in trade-offs considering constant input, GO, QC and delay. The proposed design is compared with existing structures, particularly with those designs based on Feynman and Fredkin gates. Additionally, this adder design has reduced ancilla inputs by 100%, the number of gates used by 50%, and GOs by 50%. QC has been minimized to 7. Moreover, this design is faster in output signal generations compared to those discussed in the literature. A new full-adder implementation using TFG gate is introduced through this work, which is better suited for the full-adder operation. Our proposed adder approach shows a better minimization of quantum parameters like constant input, GO, QC, gate count and also delay over various existing designs, making it a viable choice over its counterparts.

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Design of High-Speed 32-Bit Vedic Multiplier Using Verilog HDL

Hariprasad Ganji, Ravindra Kumar Maurya, and Kavicharan Mummaneni

Abstract With the advancement of technology, there is a need for high-speed multipliers in every processor. Since multiplication is nothing but a series of addition and shifting operations, the multiplier's speed also depends on its adder. Vedic multiplication is an interesting research topic that gives faster multiplication results, and carry save adder is one of the advanced and fastest adders. In this paper, we are integrating the Vedic multiplication technique, namely Urdhya Thiryagbhyam and carry save adder, to get faster results. Using the proposed 32-bit Vedic multiplier (VM), delay and area are reduced by 39 and 44% in that order compared to the existing 32-bit Vedic multiplier (VM).

Keywords Carry save adder · Urdhya Thiryagbhyam · Vedic multiplication

1 Introduction

Multipliers are the most important and necessary building blocks of the arithmetic logic unit. Most of the signal processing applications like DFT, FFT, and convolution need high-speed multipliers. The Vedic approach is proven to be the fastest algorithm [1, 2], giving quicker results than conventional array multipliers [3] and Booth multipliers [4]. So, here we are applying the Vedic approach to our digital circuits. Speed and area are the essential parameters of any digital system. To get these, many researchers are working on different multiplication techniques. Urdhya thiryagbhyam is one of the methods which reduce computational delay. T. Guptha et al. [1], in their work "A CSA-Based Architecture of Vedic Multiplier for Complex Multiplication," presented a comparative analysis between array multiplier, booth multiplier, and Vedic multipliers in which Vedic multipliers have a less computational delay. [5] S. Lad and V. S. Bendre, in their work "Design and Comparison of Multiplier using Vedic Sutras" presented the novel approach, Urdhya thiryagbhyam sutra, which means row-wise and cross-wise multiplication.

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There are several [4, 6, 7] architectures based on Urdhya thiryagbhyam that has been proposed by using different adders like ripple carry adder, kogge stone adder, carry look-ahead adder, carry save adder and carry select adder. B. Koyada et al. [8] presented "A comparative study on adders" in which a comparison between several adders is made and among those carry save adder is the most widely used adder for multiplication applications. [9] M. B. Murugesh et al. proposed "Modified High-Speed 32-bit Vedic Multiplier Design and Implementation", which using two carry save adders and consuming more area. This paper has presented to decrease the area and delay of the existing work [9]. This paper presents the Vedic method Urdhya thiryagbhyam in Sect. 2and 3 gives a brief idea about the carry save adder. Section 4 and 5 shows the existing and proposed architectures of Vedic multipliers, respectively. Section 6 provides the simulation and comparison results of the proposed Vedic multiplier. Finally, Sect. 7 presents the conclusions of this work, followed by references.

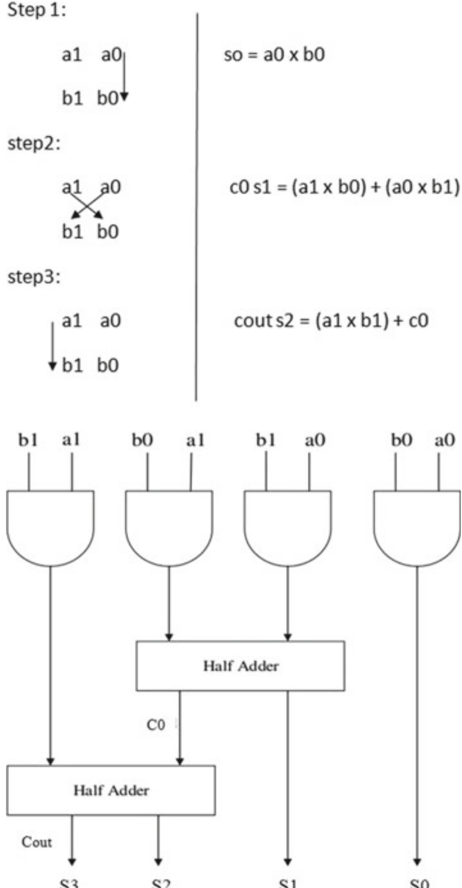
2 Urdhya Thiryagbhyam

Urdhya thiryagbhyam is a Vedic approach developed by Sri Bharathi Rama Krishna Thirtha after his comprehensive research on Vedas. Urdhya thiryagbhyam multiplication technique is different from the conventional multiplication approach [10]. This approach also applies to any number system [5, 11]. Figure 1 shows the logic implementation of the 2×2 Vedic multiplier in which half adders are used to shift the carries to the corresponding next stages. For the multiplication of two 2-bit numbers, the following steps from step 1 to step 3 are performed.

3 Carry Save Adder

Full adders can add three bits, and the third bit is taken as carry. To add three n-bit size numbers, we typically use a ripple carry adder to add two numbers, and the third number will be added later to the result by using another ripple carry adder. [12] Ripple-carry adder is nothing but a cascaded connection of full adders; full adders perform their operation after getting a carry from their previous full adder; likewise, there is a dependency between full adders. Figure 2 shows the 4-bit carry save adder architecture.

Carry save adder [13] uses two stages; in the first stage, three numbers are added, and generated carries given to the next step. In the early stage, full adders work independently without waiting for the input carry. In the next stage, two half adders and two full adders are used to add carries generated in the first stage. The 4-bit carry save adder [8] consists of five output bits and one carry.



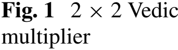


Fig. 1 2 × 2 Vedic multiplier

4 Vedic Multiplier

Figure 3 shows the architecture of the 4-bit existing Vedic multiplier [9]. If A3A2A1A0, B3B2B1B0 are two 4-bit numbers multiplied, then the result is from S7 to S0.

By splitting 4-bits into 2-bits (A3A2 & A1A0), (B3B2& B1B0), and considering two bits as one bit, we can apply Urdhya thiryagbhyam algorithm [14] in which row-wise multiplication, cross-wise multiplications are performed and carries shifted to the next immediate stages. For this purpose, it requires four 2 × 2 Vedic multipliers and produces four partial products [15]. As we are using the urdhya thiryagbhyam algorithm, the first two LSB bits of the initial partial product directly give the final result's S1, S0 values. The intermediate two partial products are added by using the first carry save adder. To this result, two MSB bits from the first partial product, two LSB bits from the final partial product are added by using another carry save adder,

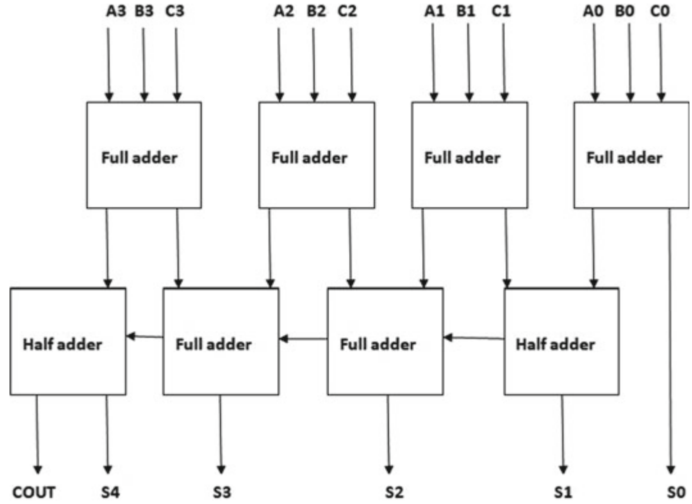


Fig. 2 Carry save adder

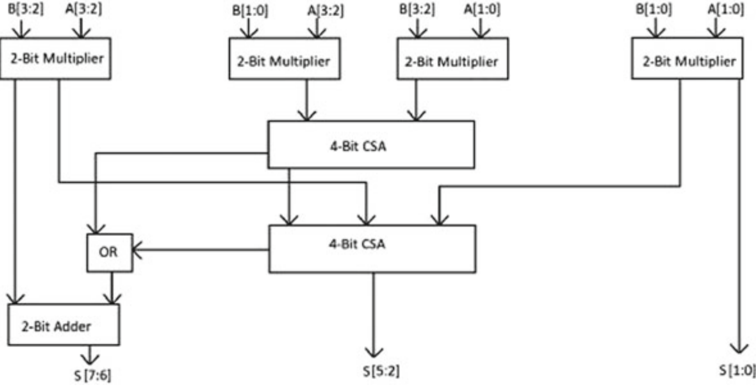


Fig. 3 Existing 4-bit Vedic multiplier

and it gives S5-S2 in the final result. In 4-bit multiplication, the carries generated from the two carry save adders are always equal to zero, and the MSB bits of these carry save adders are given to the OR gate. Using two-bit adder output of the OR gate and first 2-MSB bits of the final partial product are added, which gives S7, S6 values of the final result.

The drawbacks of the existing architecture [9] are, here, the carry save adder is not used efficiently. Also, suppose we use the same analogy to the higher-order bits; it gives the wrong results for particular cases where the MSB bits of two carry save adders are high at a time, for which OR gate did not produce any carry (example—multiplication of 63,999 and 40,949).

5 Proposed Vedic Multiplier

The design of the proposed VM is shown in Fig. 4. In this proposed work, we considered two LSB bits of the final partial product and two MSB bits of the initial partial product as a single 4-bit number. So, we will have three numbers that can be added by using only one carry save adder. Also, we are using a 2-bit adder, which is a cascaded connection of 2 half adders. In 4-bit multiplication, carry generated from the carry save adder is always equivalent to zero, and MSB of carry save adder connected to the 2-bit adder (LSB). Other inputs to the 2-bit adder are taken from the MSB bits of the final partial product. Since we are multiplying two four-bit numbers, the final result is bound to be only in 8-bits so that the carry from the 2-bit adder is always equal to zero. We can apply the same analogy to the higher-order bits in these cases; carry from carry save adder cannot be ignored. For example, in 8-bit Vedic multiplication, we require a 4-bit adder, consisting of 4 half adders in cascade. In this case, the second half adder must be replaced by one full adder to which the carry output of the carry save adder is connected.

Figure 5 shows the proposed 32-bit VM, where the 16-bit adder uses 15 half adders and one full adder. The full adder must add carry from the carry save adder, carry from the previous half adder, and another bit from the final partial product. The full adder's generated sum is given to the final result and carry connected to the next half adder. Here carry generated from this 16-bit adder is always equal to zero. After multiplying two 32 bits in decimal format, the maximum possible product is 18446744065119617025, represented in 64-bits of the binary form. Hence last half adder of the 16-bit adder can be replaced by an OR gate depending upon the designer's interest.

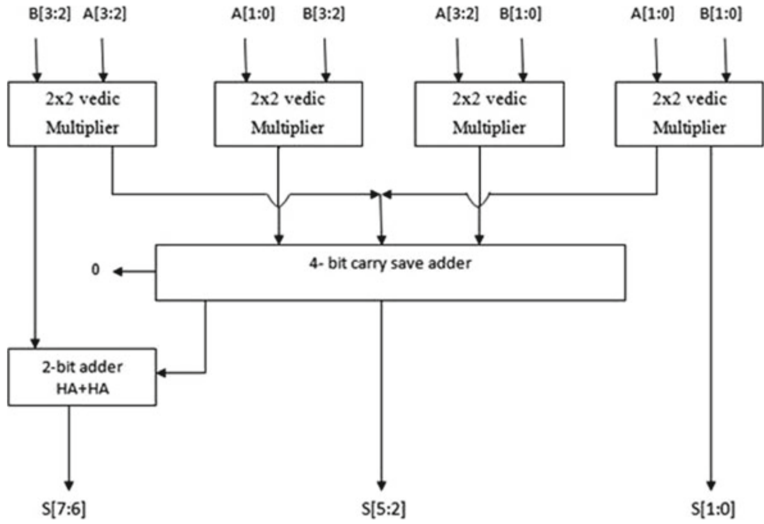


Fig. 4 Proposed 4-bit VM

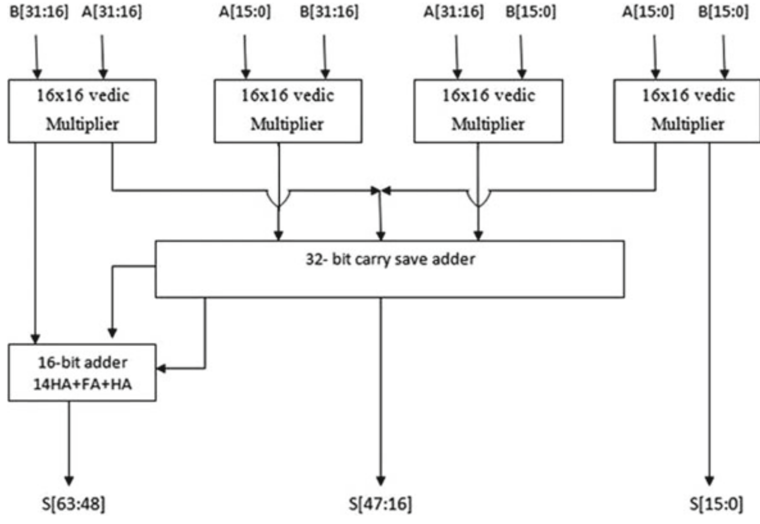


Fig. 5 Proposed 32-bit VM

6 Results

The proposed Vedic multiplier simulated in Xilinx vivado 2019.2, and synthesis carried out in Xilinx ISE 14.7. The comparison results of the existing Vedic multiplier[9] and the proposed VM are shown in Tables 1 and 2, and Figs. 6, 7. Figures 8, 9, 10 and 11 presents the 4-bit, 8-bit, 16-bit, and 32-bit proposed VM simulation results, respectively.

Table 1 Existing multiplier delay and area

S No.	Existing Vedic multiplier [9]	Delay (ns)	LUT utilization
a	4-bit multiplier	14.215	38
b	8-bit multiplier	24.186	201
c	16-bit multiplier	43.714	903
d	32-bit multiplier	68.859	3802

Table 2 Proposed multiplier delay and area

S No.	Proposed Vedic multiplier	Delay (ns)	LUT utilization
a	4-bit multiplier	10.875	22
b	8-bit multiplier	21.335	112
c	16-bit multiplier	36.524	503
d	32-bit multiplier	41.887	2126

Fig. 6 Delay comparisons

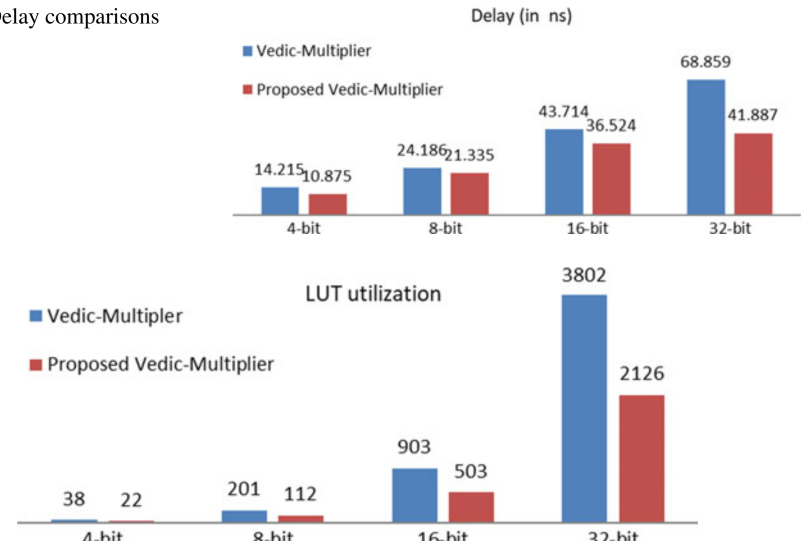


Fig. 7 Area comparisons

Fig. 8 4-bit proposed VM model result

Name	Value						
a[7:0]	205	255	249	255	159	205	206
b[7:0]	183	245		159	249	183	135
s[15:0]	37515	62475	61005	40545	39591	37515	27810

Fig. 9 8-bit proposed VM model result

Name	Value			
a[15:0]	59287	33567	65432	59287
b[15:0]	19456	56789	55555	19456
s[31:0]	1153487872	1906236363	3635074760	1153487872

Fig. 10 16-bit proposed VM model result

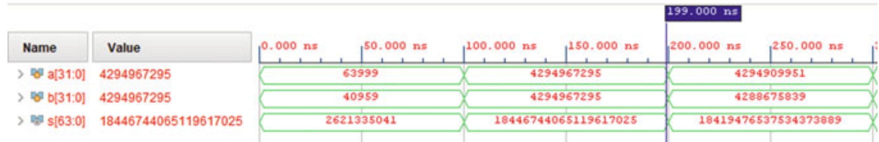


Fig. 11 32-bit proposed VM model result

7 Conclusion

To get accurate results, the OR gate needs to be avoided. Digital signal processing applications require very high-speed multipliers, and this paper has presented a high-speed multiplier design without using an OR gate. There is a decrement of 39% in the delay, 44% in the area than the existing 32-bit Vedic multiplier. Similarly, we can design higher-order 64-bit, 128-bit multipliers for various applications.

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Designing of RF-MEMS Capacitive Contact Shunt Switch and Its Simulation for S-band Application

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Abstract This paper presents design and simulation of RF-MEMS capacitive type shunt switch. The main parameters of electromagnetic and electromechanical analysis are performed by utilizing COMSOL and HFSS tools. The performance of the switch is enhanced by including perforation and non-uniform meandering technique. Here, to design an RF-MEMS switch with a change in dimensions and different air gaps, and thickness of the beam for low frequency applications. The actuation voltage of the proposed switch having 10.6 V, the upstate capacitance is 6 × 10ˆ−15. The stress of the beam was obtained as 41.7 MPa. The switch has shown higher isolation and lower insertion loss while implementing the microwave and mm-wave circuits. The S-parameters like return and insertion losses are having −22.37 dB, −0.11 dB, the isolation is obtained −21.89 dB at 2 GHz frequency.

Keywords RF-shunt switch · Pull-in voltage · S-Parameters

1 Introduction

Micro-electromechanical systems or MEMS technologies are defined as micro mechanical and electromechanical components with a micromachining processed devices used in our daily life. These can be done using materials such as ferroelectric, magnetic, ceramic, and semiconductor materials. The physical size of the MEMS is 1–100 μm and MEMS devices can vary from micrometer to millimeter. Unlike the other technologies like transistor devices which are also minute devices, these

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MEMS have a moving element in it that can be moved with the help of different types of physics like electrostatic, electrothermal [1–4]. The basic MEMS have a moving element of one and for the complex ones, it can have multiple moving elements.

MEMS technology is coming into the picture over the last few decades. The researchers and developers have invented a large number of MEMS devices for every possible sensing modality for temperature, pressure, chemical, magnetic fields, radiation, etc.

MEMS can be used in a different type of application like biological MEMS, radiofrequency MEMS. RF-MEMS has switches, phase shifters, and resonators. RF-MEMS switch has two basic types which are capacitive and ohmic type. The capacitive switches have a moving plate which changes the capacitance. The ohmic switches have cantilevers that are controlled by electrostatic force. While implementing the RF-MEMS switch we can use the two types of modes, i.e., parallel and series modes.

Compared to electrothermal, electrostatic actuation is preferred [5, 6] the phase-change and phase-transition materials [7] there is no necessity for external heating sources and high resistivity of silicon due to low power consumption [8–11], and no use of heat for glass substrates and also fused-silica [12–15], or technology of CMOS [16–19]. RF-MEMS switches of electrical and mechanical designs excellent performance at the microwave to mm-wave frequencies compared to other types of switches such as GaAs-based FET [20].

The steps followed in this paper are, in the first part, an introduction of MEMS with brief details of RF-MEMS switch and, in second part, description of the proposed design and its theoretical parameters and specifications. In part three, results and discussions after that final section concludes the paper.

2 Proposed Design

The switch has a substrate and CPW line. The CPW is a combination of a two ground plane on either side with a signal line in middle. The dielectric layer is located above the signal line of CPW to oppose the additional deficiency of signal. In this process, the electric signal flow is controlled and RF signal becomes transmitted [21, 22]. The proposed switch is having silicon substrate and the dielectric layer is silicon nitride. The planar beam consists of perforations and meanders, it is taken as gold material, and the diagrammatic illustration of the proposed switch is as shown Fig. 1. The switch specifications are also mentioned in Table 1.

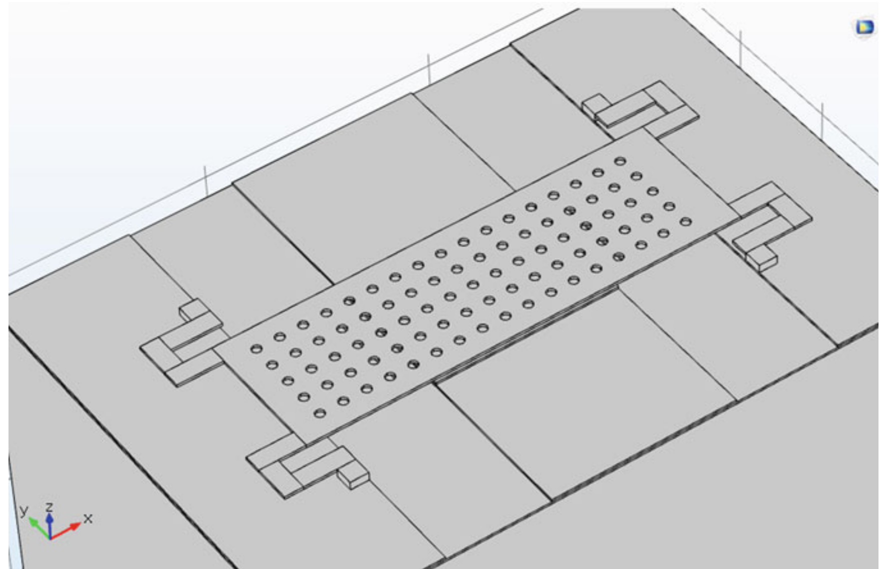

Fig. 1 The diagrammatic illustration of the capacitive contact switch

Table 1 Dimensions of various parameters in the switch

Parameters	Materials	Width	Depth	Height
Substrate	Silicon	290	200	200
Oxide	Silicon nitride	290	200	1
Ground	Gold	60	200	1
Signal	Gold	80	200	1
Dielectric	Silicon nitride	80	60	1
Electrode	Gold	25	40	1
Beam	Gold	190	160	1.2

All dimensions mentioned are in µm

2.1 Electromechanical Analysis

2.1.1 Spring Constant

A nonlinear mechanical behavior, in other terms force needed to pull the beam divided by the distance beam, gets longer. It is denoted as ‘k’ [23],

$$k = \frac{EWt^3}{l^3} \quad (1)$$

Here 'E,' 'W,' 't,' 'l' are the young's modulus, width, thickness, and length of the beam, respectively.

2.1.2 Pull-in Voltage

The minimum voltage is required to actuate the switch. It is denoted as V. The pull-in-voltage mainly depends on spring constant K.

$$V_P = \sqrt{\frac{8Kg_0^3}{27\varepsilon_0 A}} \tag{2}$$

Here, 'K,' 'g_0,' 'ε_0,' 'A' are the spring coefficient, length of the gap between the beam and dielectric, permittivity and contact area, respectively.

2.1.3 Capacitance

The capacitance of an operation is calculated at two stages, upstate capacitance and downstate capacitance. The upstate capacitance means the value of capacitance when switch is in ON state mode. The downstate capacitance means the capacitance value of switch in OFF state mode.

$$C_u = \frac{\varepsilon_0 A}{g_0 + \frac{t_d}{\varepsilon_r}} \tag{3}$$

The calculation of downstate capacitance C_d[24],

$$C_d = \frac{\varepsilon_0 \varepsilon_r A}{t_d} \tag{4}$$

Here, 'A,' 'g_0,' 'ε_o,' 'ε_r,' 't_d' are addition of area of overlapping and area of two electrodes, length of the gap between the beam and dielectric, relative permittivity of free space, dielectric permittivity, and thickness of beam, respectively.

2.1.4 Stress

The analysis of stress helps to understand the unnecessary deformation in the beam.

$$\sigma_{cr} = \frac{\pi^2 \mathrm{E} t^2}{3l^2(1 - v)} \tag{5}$$

Table 2 Dimensions of various meanders in the switch

Meander	Length (um)	Width (um)	Thickness (um)
$K1$	20	8	1.2
$K2$	16	8	1.2
$K3$	22	8	1.2
Fixed block	22	8	3.7

All dimensions mentioned are in μm

where 'E,' 't,' 'l' are young's modulus, thickness, and length of the beam, respectively.

2.2 *Electromagnetic Analysis*

Electromagnetic analysis means analyzing the behavior of the device under electric field and magnetic field. In this analysis, we analyze the S-parameters (S_{11} (return loss), S_{12} (insertion loss), and S_{21} (isolation)).

The capacitive contact parallel switch is also called a fixed–fixed capacitive shunt switch. This type of switch is the most used RF-MEMS switch. This is a composition of a movable beam, fixed supports, dielectric, electrodes, signal, ground, oxide layer, and substrate [25]. The meanders support movable beam are attached to fixed supports. The dimensions of meanders are mentioned in Table2.

3 Results and Discussion

The simulation part is done in two parts, electromechanical analysis and electromagnetic analysis. The electromechanical analysis is done in COMSOL software and the electromagnetic analysis is done in High-Frequency Structure Software (HFSS). The displacement, upstate capacitance, downstate capacitance, and stress analysis are done in COMSOL software. The S_{11}(return loss), S_{12}(insertion loss) and S_{22}(isolation) are calculated using the HFSS software. The total displacement of the beam is observed as in Fig. 2, the upstate capacitance is $6.03 \times 10\hat{}-15$ shown in Fig. 3, it is depending on the dielectric thickness and material.

The return loss, insertion loss, and isolation are calculated in High-Frequency Structure Software. Figure 5 shows the return loss as −22.37 dB, Fig. 6 shows the insertion loss as −0.11 dB. Figure 7 shows the isolation which obtained as −21.89 dB at 2 GHz frequency. The overall S-parameter values are measured in the frequency range of 1–4 GHz. During the upstate return and insertion loss are calculated while the isolation is in the downstate.

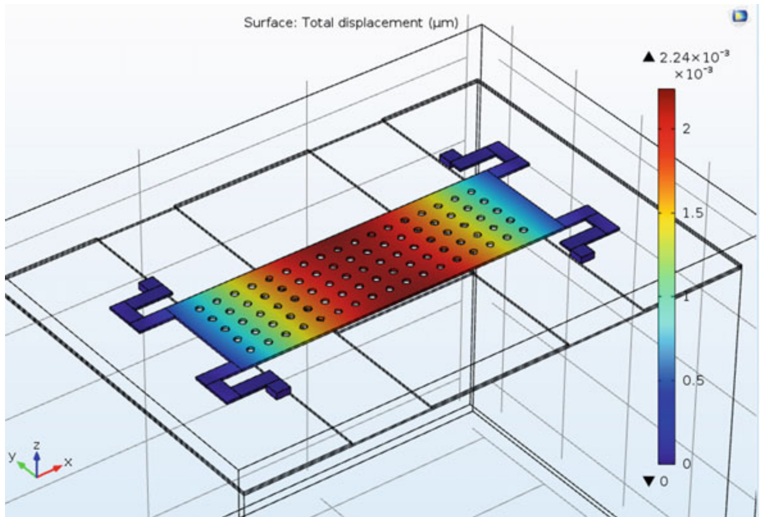

Fig. 2 Displacement of the beam observed at 10.6 V

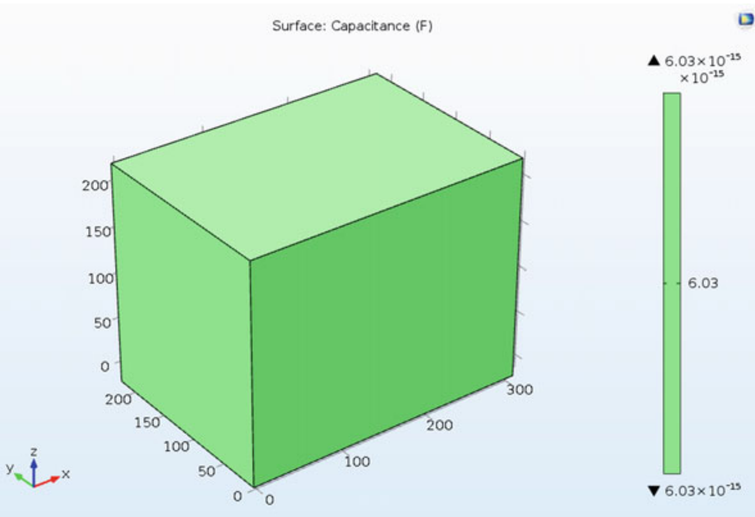

Fig. 3 Upstate capacitance of switch

The stress analysis of the proposed switch is observed that the switch can resist by having stress which is 41.7 MPa as shown in Fig. 4.

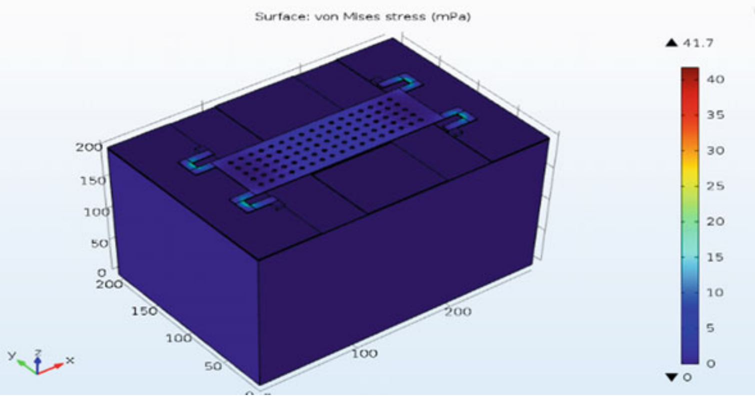

Fig. 4 Stress analysis of switch

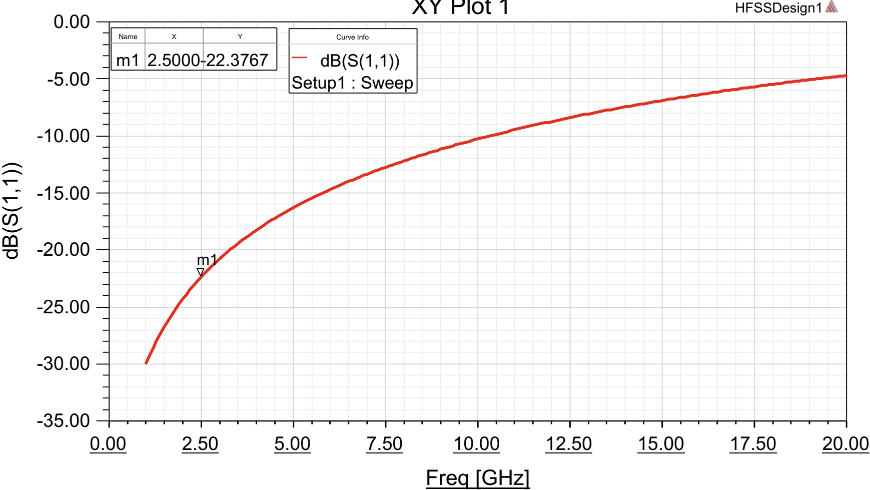

Fig. 5 Return loss measured at 2.5 GHz

4 Conclusions

In this paper, the designing and simulation of capacitive type shunt switch is done. The switch analysis of pull-in voltage (V_P), capacitance (C_u, C_d), stress, and S-parameters are analyzed and simulated with the help of COMSOL and HFSS tools. The focus of the switch is tried to reduce the pull-in voltage (V_P) and improved the isolation. Here, the meanders and perforations are utilized to reduce the pull-in voltage (V_P), the obtained actuation voltage is 10.6 V and upstate capacitance analysis is 60.4 fF, and the stress is maintained as 41.7 MPa. The electromagnetic

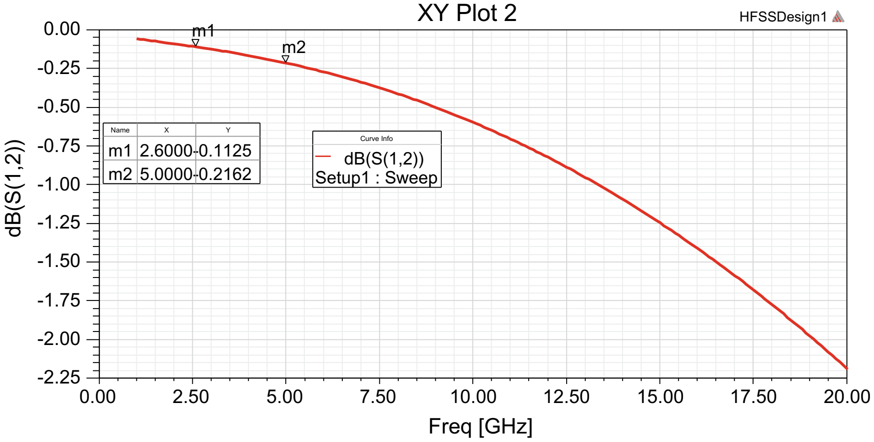

Fig. 6 Insertion loss measured at 2.5 GHz

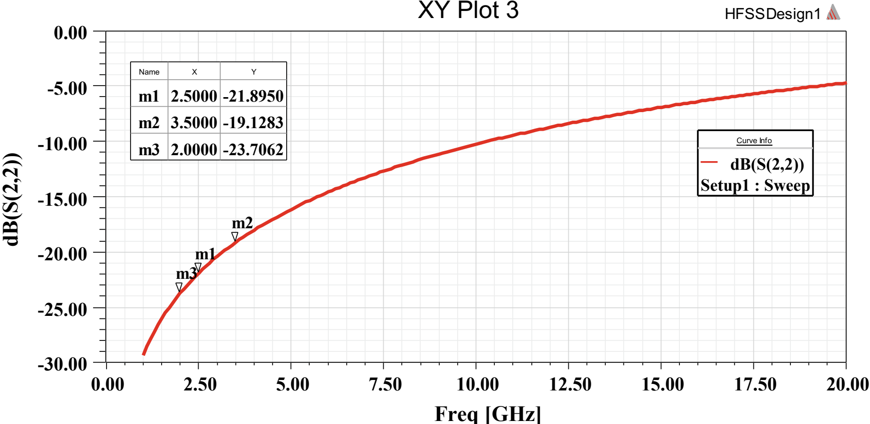

Fig. 7 Isolation measured at 2.5 GHz

analysis of S-parameters such as S_{11}(return loss) and S_{12}(insertion loss) is having $-$22.37 dB, $-$0.11 dB and the S_{21}(isolation) is $-$21.89 dB observed at 2 GHz frequency. The proposed switch is obtained better results at 2 GHz, so it is utilized for the S-band frequency (2–4 GHz) applications.

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Study and Analysis of Retention Time and Refresh Frequency in 1T1C DRAM at Nanometer Regime

Amol S. Sankpal and D. J. Pethe

Abstract A evolution in VLSI technology takes place, aspect of electronic devices scales down gradually. Scaling in electronic device offers improvement in speed, cell density and storage capacity in DRAM arrays. Leakages in MOS transistor surge as the MOS transistor scales down. The performance analysis of 1T1C DRAM cell is affected due to various leakage sources in MOS transistor. The intention of this paper is to present variation in capacitor value effects on behavior of leakage current, leakage power, retention time and refresh frequency (Frefresh) in 1T1C DRAM cell. This paper investigates the performance of DRAM cell in terms of leakage parameters, retention time (Th) and refresh frequency (Frefresh) with variation of capacitor values (Cs). While capacitor value increases, leakage parameter minimizes; correspondingly, retention time improvement is possible. Design and simulation of DRAM cell for variable values of capacitor were performed with the assistance of cadence tool at 180 nm technology.

Keywords DRAM cell · Retention time · Refresh frequency

1 Introduction

Owing to the innovation in VLSI technology, size of the electronic appliances continuously dropped down with an improvement in storage or cell density within a lesser silicon area and perfection in electrical and physical characteristic of MOS device. For small size and high-density memories, scaling is good option but electronic device scaling has some merit and demerits too. Scaling in MOS transistor increases the chip densities on silicon wafer, but correspondingly sources of leakage increase in semiconductor devices. Due to leakage sources in semiconductor memories, there

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is a leeway of loss of data; therefore, the performance of the system is affected very severely. Several sources in MOS transistor contributing leakage and static power dissipation are also increasing. Retention time (Th) is most substantial parameter in dynamic random access memory. As the source of leakages goes on increasing in MOS transistor, correspondingly retention time reduces due to which performance of the system is affected abruptly. In this paper, simulation is carried out for leakage parameters, retention time and refreshes frequency. As leakage parameter increases, it affects retention time (Th) and refresh frequency (Frefresh) is examined.

The paper is structured into the following segments: Part 2 focuses on specific sources of leakage in MOS transistor-related literature reviews. Part 3 is the implementation and experiments of DRAM memory for leakage parameters. Part 4 highlights our results and discussion, while part 5 showcases our conclusion of leakage parameters.

2 Related Work

DRAM is used as main or central memory in computer system. In large database, application DRAM is preferred for its low peripheral circuitry. The main part of DRAM is NMOS transistor and capacitor (CS). Word line and bit line are controlling nodes. Leakage is crucial issue in DRAM due to which probability of data loss from storage capacitor increases. In the mentioned literature, sources of leakage in MOS transistor are lessened with circuit level leakage minimizing techniques.

In this paper, retention time (Th) is most prestigious factor in DRAM. Retention time (Th) characteristic is changing with junction leakage, and gate induces drain leakage. Reduction in substrate doping minimized the junction leakage with a corresponding increase in lightly doped drain implantation energy (LDD) and thickness of gate oxide (t_{ox}); gate-induced drain leakage minimized [1]. In this paper, for SOC applications gain cell memories are more preferred. Here comparison of 2T1D and 3T1D gain cell memories is done, and it is preferred in low-power application. Standby leakage power is minimized with the proposed gain cell memory [2]. Symmetric gate oxide structure influences off-state leakage current (I_{off}), and in SOI MOSFET, gate-induced drain leakage plays an important role. MOSFET having asymmetric gate oxide structure is used for reducing off-state current (I_{off}) and gate-induced drain leakage [3]. In this paper, 3 T DRAM and 4 T DRAM are executed with several nanometer technology for comparative study of leakage current and power [4]. In this paper as the device is scaled down to accumulate more number of transistors on single silicon wafer, it causes leakage. Self-controllable voltage level (SCVL) leakage reduction technique is used for minimizing leakage current in DRAM arrays as compared to traditional DRAM [5]. Highly dense memories may increase leakage in DRAM cell; here, self-controllable voltage level (SCVL) technique is used to minimize leakage [6]. In this paper for optimization of leakage power and noise in DRAM sleep transistor technique is used [7]. In this paper to

minimize GIDL, work function modulation technique (WFMT) for NMOS transistor is proposed. Concentrations of doping impact on gate-induced drain leakage in transistor. Reduction of GIDL is proposed with dual work function metal (W_f) gate without affecting threshold voltage (V_{th}) [8]. In this paper, embedded DRAM 3T1D is considered for power dissipation analysis [9]. In this paper, FinFET technology is used for implementation of three transistor DRAM cell. 3 T DRAM with FinFET technology contributes lowest leakages as compared to basic DRAM [10].

Nowadays, one-transistor DRAM cells with poly-Si substrate have involved concentration as responding to the shortcoming of the silicon one-transistor DRAM cell [11]. With annealing deposited amorphous silicon, a poly-Si one-transistor DRAM cell is simple to design and less expensive than a silicon one-transistor DRAM cell as its configuration can be implemented. In accumulation, the poly-silicon SOI design permits a three-dimensional load structural design that extremely enhances absorption concentration. The logical range of semiconductor material silicon one-transistor DRAM is extensively decreased in a thin-substrate design, whereas in a poly-Si one-transistor DRAM cell here a small device thickness is achieved [12]. Slightly high VTH is suitable to the asymmetrical barrier potential improved by the GBs at random scattered along the channel area [13]. As drain source voltage (V_{DS}) value enhances, drain leakage obtains superior through thermionic ground emission and lead retain tunneling [14].

3 Implementation and Experiments

3.1 DRAM Cell Memory

For one-bit data storage operation DRAM is used. Active element is transistor (NMOS) and capacitor (CS) is used for stored charge over it. Word line is used to make transistor ON and OFF and bit line (BL) control I/O bit. The schematic representation of DRAM cell is shown in figure (Fig. 1).

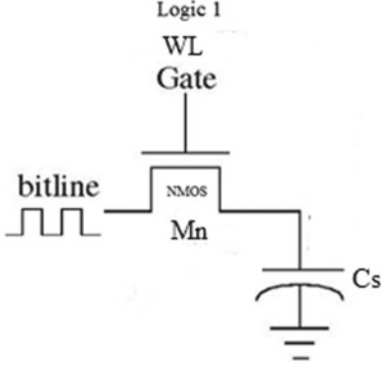


Fig.1 1T1C DRAM memory cell

Fig.2 1T1C DRAM cell schematic

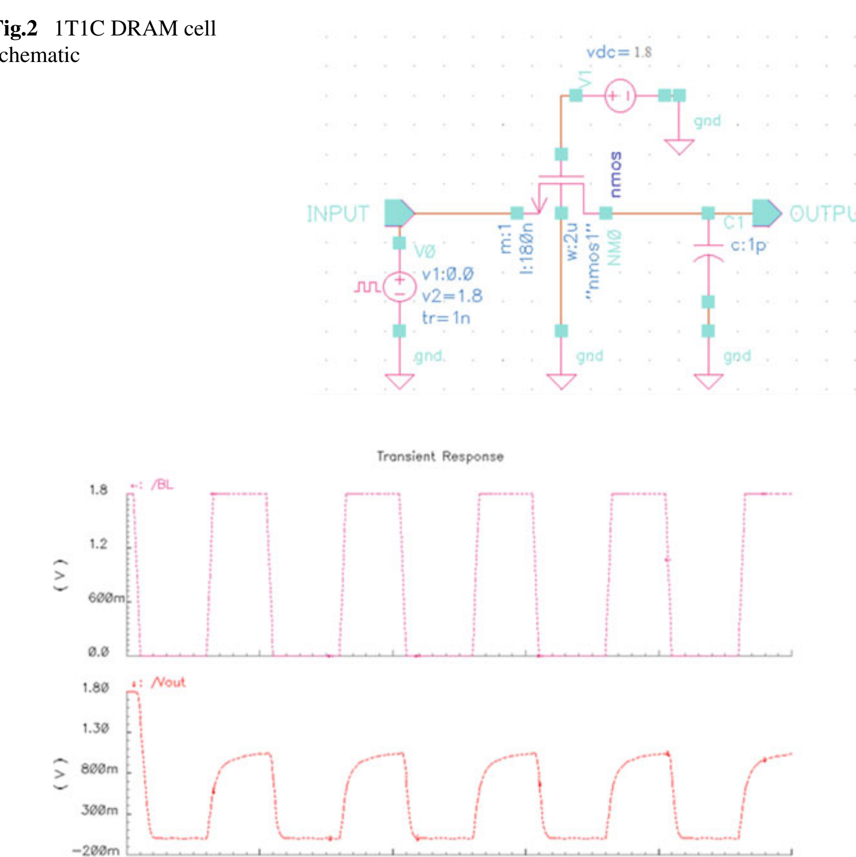


Fig.3 1T1C DRAM cell transient response

3.2 Schematic and Simulation of DRAM Cell

The DRAM schematic is shown in Fig. 2, Fig. 3 represents transient response, and Fig. 4 represents leakage current waveform, respectively.

3.3 Simulation Result

DRAM simulation is carried out in cadence tool using 180 nm technology having supply voltage Vdd of 1.8 V. The peripheral circuitry for DRAM cell is minimum for reduction of power consumption and maintaining the performance of 1T1C DRAM circuit. It is comparative analysis of 1T1C DRAM circuit; the parameters like leakage

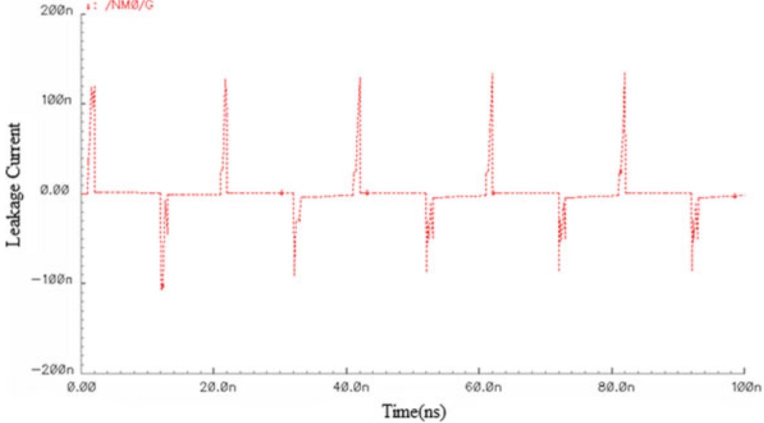


Fig.4 1T1C DRAM cell leakage current

Table 1 Simulation results

Sr. No	Storage cap (pF)	Leakage current (nA)	Leakage power (nW)	Retention time (ms)	Refresh frequency (Hz)
	Cs	IL	PL	Th	Frefresh
1	1	4.22	7.92	0.421	1190.47
2	2	0.32	0.62	12.1	41.66
3	3	0.12	0.19	49.10	10.18

Table 2 Comparison of DRAM with conventional DRAM results

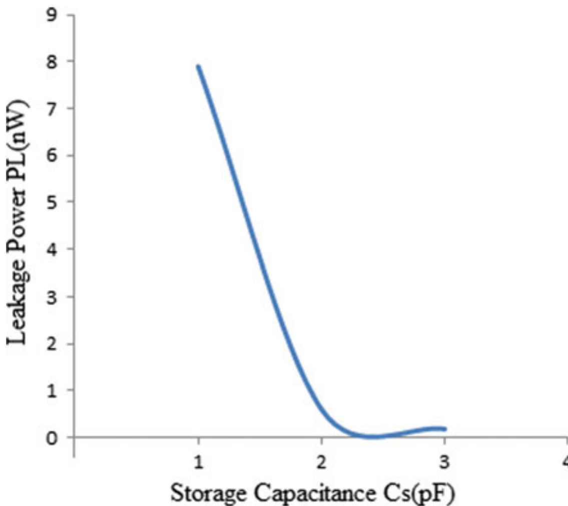
Sr. No	Performance parameters	Reference [6]	1T1C DRAM
1	Technology	250 nm	180 nm
2	Supply voltage	3 V	1.8 V
3	Leakage current	0.713 mA	4.22 nA
4	Leakage power	16.85 μW	7.92 nW

current, leakage power, retention time and refresh frequency are shown in Table 1 (Table 2).

3.3.1 Leakage Power

Reduction in channel length in MOS devices by scaling leakage current plays vital role in degradation of device performance. Leakage current arises due to substrate injection effect and sub-threshold voltage. In MOS device, leakage power of 1T1C

Fig.5 Capacitor (pF) versus leakage power (nW)



DRAM is given by

$$P_{\text{Leak}} = I_{\text{Leak}} \times V_{\text{dd}} \tag{1}$$

where

P_{Leak} is the leakage power of 1T1C DRAM,

I_{Leak} is the leakage current,

V_{dd} is the power supply.

The graph indicates variation in capacitor value; correspondingly, leakage power reduction is shown in Fig. 5.

3.3.2 Sub-threshold Leakage Current

Sub-threshold current arises when V_{gs} voltage is below V_{th} voltage of transistor. When V_{gs} is less than V_{th}, transistor operates in weak inversion region and current is flowing between drain and source. The leakage sub-threshold current in MOS transistor can be expressed as:

$$I_{\text{subthreshold}} = I_0 e^{\frac{(V_{gs}-V_{th})}{nV_T}}\left[1 - e^{-\left(\frac{V_{ds}}{V_T}\right)}\right] \tag{2}$$

where

$I_0 = \frac{W\ \mu_0\ C_{OX}\ V_T^2\ e^{1.8}}{L}$,

$V_T = \frac{KT}{q}$ =thermal voltage,

V_{th} = threshold voltage,

V_{ds} = drain to source voltage,
V_{gs} = gate-to-source voltage,
C_{ox} = gate oxide capacitance,
μ_0 = carrier mobility,
n = sub-threshold swing coefficient.
L and W are the transistor length and width, respectively.

The graphs indicate variation in capacitor value; correspondingly, leakage current reduction is shown in Fig. 6.

The graph indicates variation in capacitor value which gives improvement in retention time shown in Fig. 7.

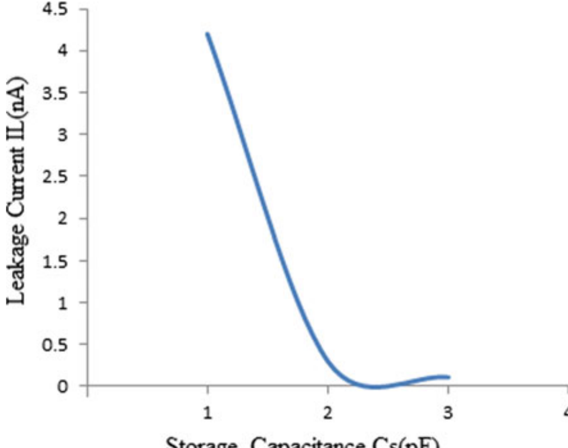


Fig.6 Capacitor (pF) versus leakage current (nA)

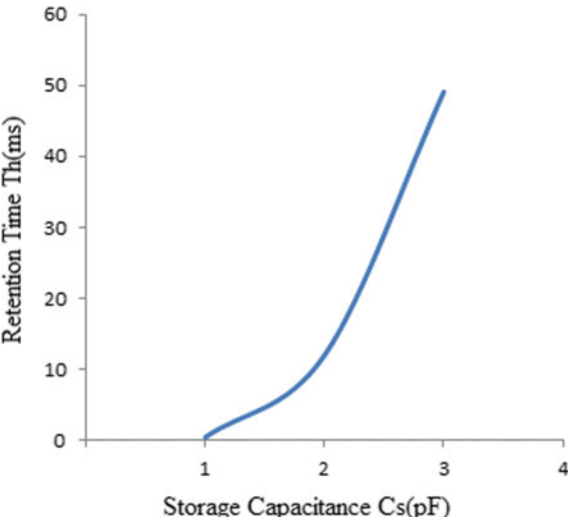


Fig.7 Capacitor (pF) versus retention time (ms)

The graph indicates that as leakage current increases, retention time decreases as shown in Fig. 8.

The graph indicates that as leakage power increases, retention time decreases as shown in Fig. 9.

The graph indicates that as retention time increases, refresh frequency reduces as shown in Fig. 10.

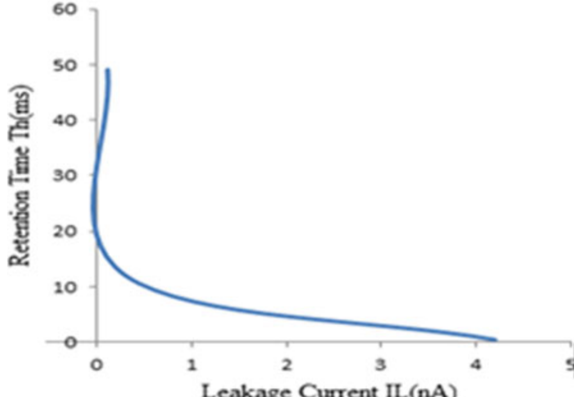


Fig.8 Leakage current (nA) versus retention time (ms)

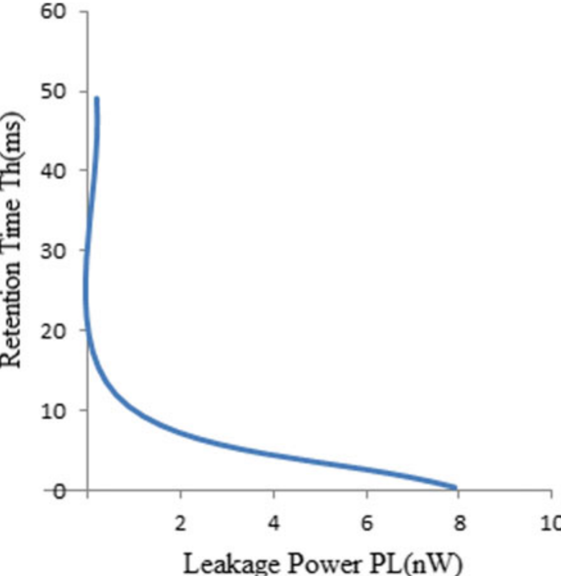


Fig.9 Leakage power (nW) versus retention time (ms)

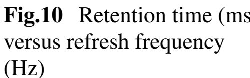
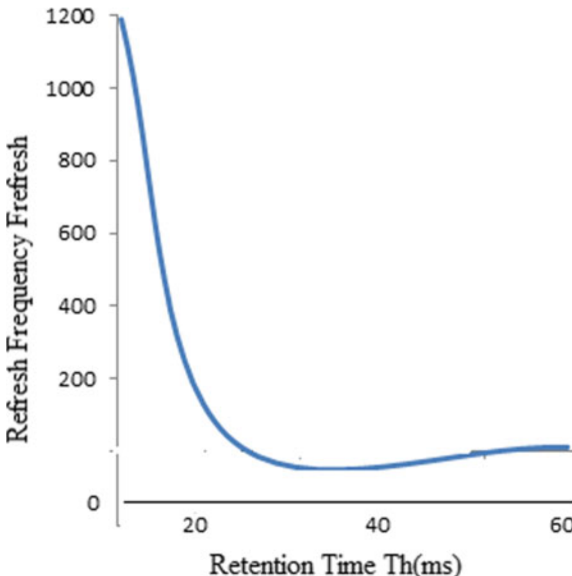


Fig.10 Retention time (ms) versus refresh frequency (Hz)



4 Results and Discussion

1T1C DRAM simulation is carried out in 180 nm technology using cadence tool. During experiments word line and bit line kept at 1.8 V, the values of storage capacitor kept varying. Simulation results state that as the storage capacitor (Cs) is varied from minimum to maximum value, leakage parameters, i.e., current (IL) and power (PL), can be reduced, and retention time (Th) can be increased; correspondingly, refresh operation frequency also decreases. There is a direct relation between retention time (Th) and storage capacitor (Cs). In simulations, the value of storage capacitor increases; correspondingly, retention time increases and refresh frequency goes down. Due to improvement in retention time, the possibility of loss of information is minimized. Access time of 1T1C DRAM cell is 22.1 ns and aspect ratio of DRAM cell is 1.11, respectively.

5 Conclusion

In this paper, leakage issues in MOS transistor of 1T1C DRAM cell memory were examined. As the devices are scaled down to keep dynamic power under control, threshold voltage v_{th} scaling results in increasing leakages current. Leakage current is the most prominent factor in CMOS circuit; we have analyzed a compressive quantitative study of leakage behavior on retention time and refresh frequency (Frefresh) in 1T1C DRAM cell. In this analysis, leakage power and leakage current reduced to

excessive level using variations of capacitor value (Cs) and improvement in retention time is proposed. Improvement in retention time also decreases the refresh frequencies, and possibilities of information loss are minimized.

In the future work, in DRAM memory cell, we will apply various leakage reduction techniques for reducing leakage parameters and it will be compared with conventional parameters.

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Self-Automated Parking with FPGA-Based Robot

G. Divya Vani, K. Srnivasa Rao, and M. C. Chinnaiah

Abstract This paper proposes a framework of intelligent approach for autonomous parking of the robot. It addresses the challenges of service robots parking in real-time indoor environment. A versatile automatic parking system is developed based on two key approaches, which can able to perform in real-time conditions, 1. Self-exploration of indoor environment for recognition of parking space by autonomous robot and 2. Road map for parking of autonomous robot using intelligent methods. Hardware schemes have been developed for self-exploration by a robot, and it is executed based on the tree-based algorithm and road map for parking of robot is performed by intelligent traversing methods. The FPGA-based robot is used for the validation of self-autonomous parking methods. Xilinx tools have been used for simulation, synthesis and implemented autonomous parking using ZedBoard Zynq-7000 FPGA.

Keywords Autonomous parking · Indoor environment · FPGA · Robot · Self-exploration

1 Introduction

The rapid evolution of autonomous parking from the past decade is very much essential because expert drivers are also facing challenges in parking of vehicles. The urban population is gradually attracted for vehicle usage for their itinerary, and this is impacted more on parking slots in an urban environment. The traffic is affected due to unavailability of parking and smart methods to resolve the challenges in parking.

The researchers suggest parking techniques for dissolving the parking challenges with smart approaches. Chinrungrueng et al. [1] addressed analysis about parking availability space versus required parking. The smart parking is essential for both

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open parking and indoor parking. In parking, the major constraints are estimation of parking space availability, navigation towards parking and parking approaches. An estimation of parking space has addressed by researchers with smart technologies: 1. Early identification of parking with sensor methods, 2. Reservation methods has followed as per the requirements to decrease the traffic issues, 3. Dynamic parking as per instant availability. Jhang et al. [2] are mentioned in their review about the importance of navigation methods towards parking space, few of navigation algorithms like Markova models, RRT has used. Bischoff et al. [3] have mention autonomous vehicles, impact at parking situation. Parking constraints about kinematics for both parallel parking and perpendicular parking have been reviewed and addressed by researchers [2–4].

The open parking lots conceptual discussion has been reviewed by Paidi et al. [5]. An open parking system impacts with challenges as per environmental conditions like rainy season, fog environment [6], lighting impacts on parking at day and night conditions. Open parking constraints are essential for different sizes of vehicles. Parking in unauthorized spaces creates traffic issues and accidents, and it is one of the major issues. In this regard, parking lots are mentioned separately at different spaces as per the size of vehicles. The parking is extended for truck-trailer type vehicles also, and it is addressed by Manivannan [7]. The autonomous parking of truck-trailer has addressed by Kusumakar et al. [8].

The urban civilization in the developing countries is more impacted with parking due to less size of individual house/home. Few solutions are mentioned by researchers as multi-storied parking with smart techniques using CNN methods by Usman et al. [9]. The Han et al. [10] mentioned mapping techniques for the parking of the car type robot at indoor environment. The authors in [11–14] have developed various methods based on vision and map estimation for parking.

The smart parking depended on sensors, technologies with computational devices. Sensors are mostly considered are infrared, ultrasonic, inductive loop detectors, RFID tags, magnetometer, microwave radar, GPS and machine vision. The sensors like active/passive infrared sensors, ultrasonic sensors and thermal image/image visions are suitable for certain parking conditions and also highly preferred in the indoor parking. The other sensors along with machine vision are appropriate for the open parking lot. The technologies have been used such as parking guidance systems, vehicular ad hoc networks, multi-agent systems, neural network and fuzzy logic. Along with these computational devices like microprocessors, microcontrollers, FPGAs are preferred for computing the sensor information and to communicate with other systems. Among computational devices, FPGAs are highly opted one for parking; it computes multi-sensor information parallelly, less power consumption, and it is also compatible device.

The recent challenge in an indoor environment, especially at homes, restaurants and industrial service robots are playing vital role in assisting human beings. These mobile robots are known as a part of the family. At the same time, they required certain parking space in the environment, if not children, elderly at home and workers at industry colliding chances are more. In this regard, parking of mobile robots at home/industry/work space is very much essential. The proposed algorithm is a

novel approach for parking of mobile robots in the indoor environment. In this research work, an FPGA device is used for computing the sensor information at fusion conditions and proposed algorithms.

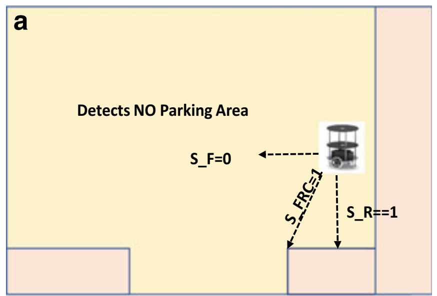
The key contributions of this paper are:

1. An adaptation of exploration for parking search in real-time indoor environment.
2. A novel approach algorithm has been developed for parking of robot with parallel model.
3. The hardware scheme for evaluation and validation of parking algorithm in indoor environment.

This section provides the overview of parking and the importance of mobile robot parking in indoor environments. The sect. 2 is addressed about the indoor parking methodology, and sect. 3 deals with hardware schemes for mobile robot parallel parking. The sect. 4 describes the evaluation of algorithm with simulation, synthesis results. The sect. 5 elaborates the novelty of the proposed research work with the conclusion.

2 Mobile Robot Parking Algorithm for Indoor Environment

The proposed algorithm is regarding mobile robot parking in an indoor environment, and it is represented in the Fig. 1. The proposed algorithm is confined with two major objects, self-exploration of indoor environments for recognition of parking space and trajectories for parking of autonomous robot using hardware-based algorithm. The Table. 1 gives the different nomenclatures used in the proposed work.



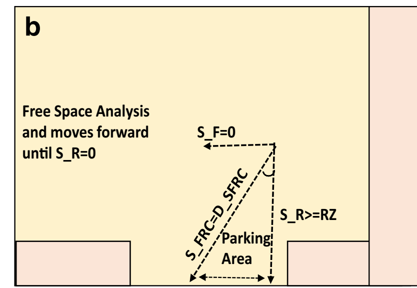


Fig. 1 **a** No space for parking. **b** Estimation of parking space

Table 1 Nomenclatures with expansion of their symbols

Nomenclature	Expansion of symbol
S_F	Sensor at front side of robot
S_{FR}	Sensor placed between front and right sides
S_R	Sensor at right side
S_{BR}	Sensor placed between the back and right sides
S_B	Sensor at back side
S_{BL}	Sensor between the back and left sides
S_{FL}	Sensor placed between front and left sides
S_{x_D}	Sensor distance from objects
R_z	Size of the robot
d_{Min}	Minimum distance from robot
d_{Max}	Maximum distance from robot
d_{Min_D}	Minimum distance of diagonal sensor
d_{Min_d}	Minimum distance of parking depth
θ_m	Angular movement of robot
θ_{90°	Right angle movement
D_{R2z}	Distance is equal to double the size of the robot

2.1 Self-Exploration of Mobile Robot for Parking

The first aspect of the proposed algorithm is self-exploration to achieve parking space. It executes this aspect with localization of the robot, mapping towards parking and avoiding obstacles with proper robot alignment. The localization of the robot has been performed with sensory information, from current location estimation of all sensor's distances (S_{x_D}). Among them, minimum distance sensor is considered and traverse to that direction. Then it traverses as per condition along with the side plane, and it takes appropriate direction at obstacle avoidance situations.

Algorithm 1a: Self-exploration of robot for parking

Input : S_{x_D}, $\{Sx = S_F, S_{FR}, S_{FL}, S_B, S_{BL}, S_{BR}, S_L, S_R\}$
Output: Exploration of parking space by mobile robot.

Step 1: Estimation of robot localization in indoor environment.
1. *If* $f_{min_dist}(S_F, S_B, S_L, S_R)$ //Eg: S_F sensor with minimum distance than other sensors
2. Robot will drive towards minimum distance direction //S_F sensor direction.
   go to step 2
3. *Else* $f_{min_dist}(S_{FR}, S_{FL}, S_{BL}, S_{BR})$
   //S_{FR} sensor with minimum distance than other sensors
4. Robot will rotate $\theta_{45°}$ towards respective lead position direction
   // Robot rotates towards S_F sensor direction
   go to step 1
5. *End*

Step 2 : Traversing towards Parking with map
6. *If* (S_F =0)
7. *If* (S_L=0, S_R=1)
   //Robot following the right plane of the environment
8. Forward action performed
9. *Else* (S_L=1, S_R=0)
   // Robot following the left plane of the environment
10. Forward action performed
11. *Else*
    // Robot following both the planes
12. Forward action performed
13. *Else*
14. *If* (S_L=0, S_R=1)
    //Obstacles are nn front of right and front planes
15. Left turn with $\theta_{90°}$.
16. *Else* (S_L=1, S_R=0)
    // Obstacles are in front of left and front planes
17. Right turn with $\theta_{90°}$.
18. *Else*
    // Deadlock condition
19. Backward action is performed, when any of sensors bit information is zero.
20. *End*

2.2 Parallel Parking Algorithm of Robot

The other aspect of the proposed algorithm is regarding parallel parking of the robot. It consists of three concern points (a) prior parking search (b) estimation of parking space and (c) parking execution for both forward and backward trajectories. This aspect is estimated in parallel to the self-exploration approach.

$$d_{min_D} = \sqrt{(y_2 - y_1)^2 + (x_2 - x_1)^2} \quad (1)$$

$$\mathrm{d}x = (x_2 - x_1) = \mathrm{d}\min + 2Rz \tag{2}$$

$$\mathrm{d}y = (y_2 - y_1) = \tan 45^\circ \times \mathrm{d}x \tag{3}$$

As per Euler's principal, the computation is performed for d_{Min_D}. As per right angle triangle, dx and dy are evaluated.

Algorithm 1b: parallel parking of the robot

Input : {S*x*= S_F , S_{FR} , S_{FL}, S_B, S_{BL}, S_{BR}, S_L, S_R }, $d_{Min,}$ d_{Max}
Output : Exploration of parking space by mobile robot.

Step 1: Prior parking space estimation
1. *If* ((S_F =0)
2. *If* (S_L=0, S_R=1))
3. *If* ($S_{FR_D} \geq d_{Min_D}$) // parking space sufficient
4. *go to step 2 of 2b*
5. *Else*
6. Robot forward, go to step1 of 1b
7. *End*
8. *Else If* (S_L=1, S_R=0))
9. *If* ($S_{FL_D} \geq d_{Min_D}$) // parking space sufficient
10. *go to step 2 of 2b*
11. *Else*
12. Robot forward, go to step1 of 1b
13. *End*
14. *Else*
15. go to step 2 of 1a
16. *End*

Step 2 : Estimation of Parking space
17. *If* ((S_F =0)
18. *If* (S_L=0) && ($S_{R_D} \geq D_{R2z}$)
19. *If* ($S_{FR_D} \geq d_{Min_D}$) // parking space sufficient as per depth
20. *go back until half distance of Rz.*
21. *If* ($S_{FR_D} \geq d_{Min_D}$)
22. go to step 3 of 1b // parking space sufficient as per length
23 *Else*
24. Robot forward, go to step1 of 1b
25. *End*
26. *Else If* (S_R=0) && ($S_{L_D} \geq D_{R2z}$)
27. *If* ($S_{FL_D} \geq d_{Min_D}$) // parking space sufficient as per depth
28. *go back until half distance of Rz.*
29. *If* ($S_{FL_D} \geq d_{Min_D}$)
30. go to step 3 of 1b // parking space sufficient as per length
31. *Else*
32. Robot forward, go to step1 of 1b
33. *End*
34. *Else*
35. go to step 2 of 1a
36. *End*

Step 3 : Parking execution with forward trajectory

```
37. If ((S_F =0) &&  (S_F_D ≥ d_Min_d)
38.        Rotate robot for θ_15° & forward up to  half of the robot size
39.        If (S_F_D ≥ d_Min_d)
40.                Rotate robot for θ_15° & forward up to  half of the robot size
41.                If (S_F_D ≥ d_Min_d)
40.                        Rotate robot for θ_15° & forward up to half of the robot size
42.                        Execute robot rotation with θ_45° for revert angle of previous
43.                        Reached Destination
44.                        Want to come out of parking, go to step 4 of 1b
45                 Else
46.                        go back for half robot size and θ_15° invert to previous angle
47.        Else
48.                go back for half robot size and θ_15° invert to previous angle
49. Else
50         go to step1 of 1b
51 End
```

3 Hardware Scheme of Parallel Parking

The novelty of the proposed algorithm is a hardware scheme for parallel parking of mobile robots in indoor environments. This hardware scheme consists of sensor fusion module, parking search module, parallel parking module and processing module are parallel executing modules as per control unit with respect to the algorithm.

The sensor module is interfaced with 2 bit information which is fed from the control to trigger signal after the time interval of echo signals, which received by the same module. The received sensor information is in the analogue format, and it is converted into distance with the support of pulse width to distance converter module. This sensor output data with 20 bit information has driven to the sensor fusion module. It synchronizes total sensor data, and it drives information to the control unit and other modules. The control unit plays vital role in performing of the algorithm. The self-exploration in-search of parking space is performed by parking search module. The modules consist of internal architectures for estimation of robot localization, traversing mapping for parking and obstacle avoidance in the environment. The parking module has been integrated with four internal architectures such as Self-exploration of indoor environment, estimation of parking space, parking trajectories for both forward and backward approaches. The processing module will process the algorithm and feeds the motor controls to perform motor operations. The FPGA-based robot used for validation of the proposed algorithm, Zynq board XC7Z020 type FPGA used for implementing and for synthesis report. The ultrasonic sensors are preferred, and it is appropriate for indoor environment. The stepper motors are used to drive the robot. The total algorithm has deployed into the FPGA, and it acts as processing device for execution of parking.

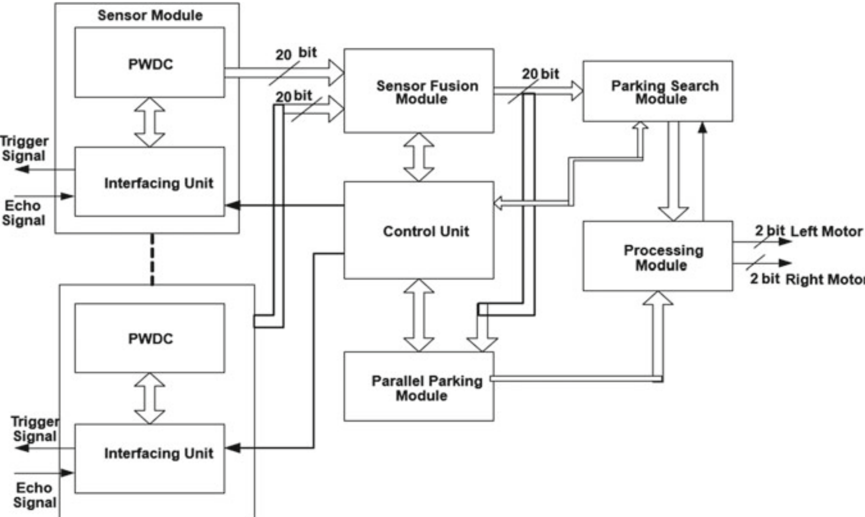


Fig. 2 VLSI architecture for parallel parking of mobile robot in indoor environment

4 Results

The proposed algorithm is validated using an FPGA-based robot. The proposed system executed experimentally for self-exploration and parallel parking algorithms in Fig. 3.

In the Fig. 4, the robot receives the signals from all the sensors and navigates towards the parking area. The robot detects no obstacle from the front sensor (S_F) and navigates up to one metre and to check for the free space. At 9,001,000 ns S_F = 0, S_R = 1, S_L = 1 indicates, no free space on either sides of the robot and it navigates in the forward direction. State_reg gives all the transitions required for parking, Stae_reg = 2'b001 indicates no free space for parking.

In the Fig. 5, the robot confines the parking space. The path planning to park the robot in parallel method is shown. Robot takes 15° right turn followed by navigation in forward with the step size until it rotates 45°.

4.1 Comparison

The parking approaches have classified into parallel and perpendicular methods. The authors [2–4] mentioned about parking of car type robot modelling, but it is not executed inside the service industry/home. The state of the art of proposed research work is hardware-based parallel parking, and it is first of its kind mentioned about inside the home/service industry in real-time conditions using parallel parking

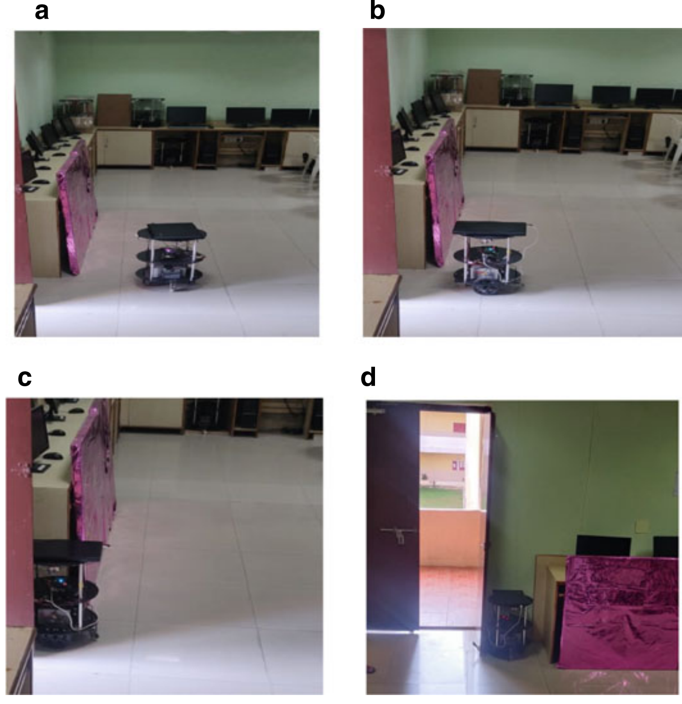


Fig. 3 **a**-**d**: Snap shots of FPGA-based mobile robot parallel parking

Fig. 4 Simulation results of parking search

method. It consumed less logical area space in a computational device, and also it consumed less power at 1.6 mAmp.

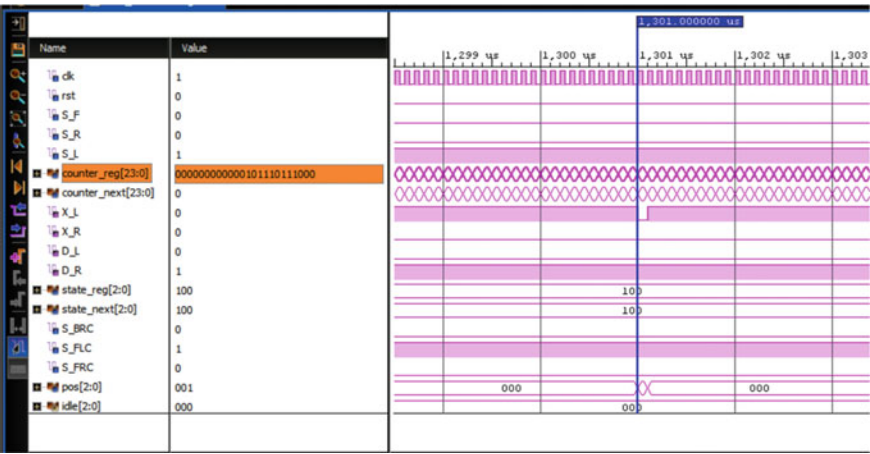


Fig. 5 Parking the robot in parallel mode

5 Conclusion

The proposed research work has been developed for autonomous parking of FPGA based robot. The novelty of the proposed algorithm is a state of art to develop the parallel parking algorithm for mobile robot in indoor environments. The other novelty of research work is hardware scheme for proposed algorithm. The area consumed for this is 23% of the device, and static power consumed is 1.6 mA; it is recorded using Xilinx power tools. This execution is done by coding the robotic modelling in Verilog HDL, and same is simulated and synthesized. The experimental validation is conducted for self-exploration and parallel parking trajectories. This result impacts the next future mobile robot parking methods in indoor environment.

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Validation and Implementation of a Smart Flood Surveillance System Based on Wireless Sensor Network

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Abstract This article presents a real-time early flood monitoring cum warning system in flood-prone areas. The proposed system comprises of three chief constituents, namely sensor network, computing/transmission unit, and database/application server. The real-time information of water conditions is supervised remotely via a wireless sensor network. The data obtained from the hardware system are stored in the cloud and compared with the real-time data of rainfall, emergency flood level, etc. from state meteorological center. The network system decides whether there is an emergency and sends warnings in the form of text messages to the people nearby flood-prone areas.

Keywords Flood monitoring · Wireless sensor networks · Assam flood · Arduino UNO · Probability

1 Introduction

Flood is one of the major natural disasters in India. Of all the Indian states, the northeastern state of Assam is one of the hotspots for this annual disaster. Geographically, the state of Assam has a humid tropical monsoon climate. The river drainage in the state is exorbitantly rich, channeled by the Brahmaputra River and the Barak River. The Brahmaputra is one of the largest rivers in the world, comprising of a relatively complex network of tributaries. The river flows through Tibet, Arunachal Pradesh, Assam and finally drains out through Bangladesh into the Bay of Bengal. The Brahmaputra basin covers an area of around 1,94,413 km^2 in India [1].

Flood in the state of Assam is caused by the Brahmaputra and its tributaries. There are several factors responsible for floods in the state, and they may be attributed to natural, hydrometeorological, and anthropogenic reasons. Floods have been devastating for agriculture and socioeconomic stability. The loss of lives and food during floods have always remained a challenge to the country. Floodwaters also result in

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hazards in the electrical power grid by inundating heavy duty equipment and thus causing short circuits, internal discharge damage, and moisture-inflicted damages [2, 2].

Therefore, it has become extremely important to warn the people who live nearby rivers and are vulnerable to floods, so that the after-effects of the disaster are decreased, and natural habitat stays protected [4]. Current work in sensor networks highlights the growing applicability of networks to everyday problems [5]. Monitoring of water conditions in and around agricultural regions is utmost essential for food security and socioeconomic sustainability [6]. The main aim of flood prediction and warning is to inform people before flood occurrence. Again, flood detection is dependent on primitive manual observation and remote surveillance, and manual observation is not reliable and real time [7]. But, an intelligent flood alert system supports data acquisition, assessment, monitoring, and transmission of warning to the concerned people. Wireless sensor nodes fetch the data from the active sites, whereas a controller analyzes the collected data and generates flood warnings.

To reduce the cost of transmission, we propose to use a smart sensing system that can communicate to the server constituent during critical conditions [8], and inform the people so that they have enough time to prepare for emptying their place. A flood sensing algorithm which is capable of presenting a real-time summary of critical parameters, and deployed throughout twenty four hours a day can be immensely useful for flood management operations, and forecasting [9].

Real-time flood surveillance through wireless sensor networks can detect, timely monitor, and transmit the site's status to the control unit. It is a wireless sensor network which can monitor the real-time data of water condition remotely. The data obtained from the sensor network are stored in the cloud, and the stored data are compared with the real-time data of temperature, humidity, rainfall, water level, etc. collected from Sonitpur District meteorological center. Then, the system decides whether there is an emergency or not. To fetch relevant information, a person is required to visit a web site and to get the information, the person requires to use a mobile phone with internet connectivity, and most people find it difficult to afford one [10]. But text messages can be sent to any mobile without an internet connection. So, if there is an emergency, the system can send a text message to every registered person in that affected zone for further action.

Section 2 of this article briefly presents the block diagram of the setup. Section 3 mentions the mathematical fundamentals of the system. The results obtained from the sensors and the measure of probabilities are presented in Sect. 4. Section 5 concludes the work.

2 Working Principle

The flood detection system shown in Fig. 1 consists of a microcontroller, ultrasonic sensor, water flow sensor, raindrop sensor, temperature and humidity sensor, transmitter, and receiver. The hardware collects the data of rainfall measurement, level of

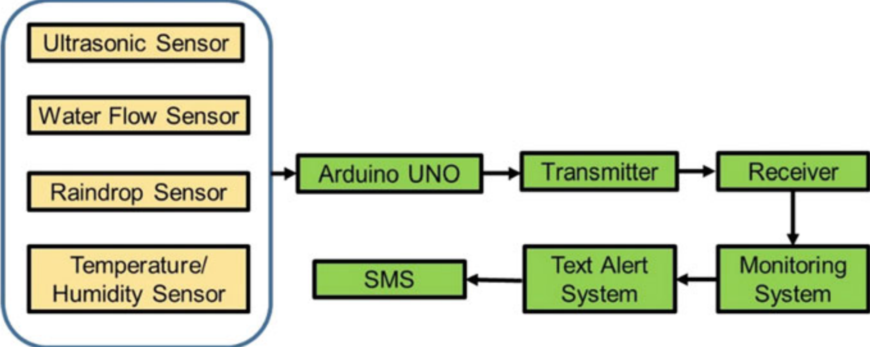

Fig. 1 Block diagram of a smart flood surveillance system

water, pressure of water, and speed of water to determine the flood. In real time, a 230 V AC supply is used; however, in this work, we have converted this AC power supply to a DC power supply [11].

- **Microcontroller (via Arduino UNO)**: The controlling with processing is done by the microcontroller. At first, the microcontroller takes all the information from the sensors. Then, this information is sent to the receiver through the transmitter.
- **Water flow sensor**: This sensor is used to measure the speed of the water. It consists of a valve (plastic) through which the water can pass. A water rotor is present which contains a Hall effect sensor. The sensor sense and measure the water flow.
- **Ultrasonic Sensor**: This sensor is used to measure the height of the water level from the ground. If the ultrasonic waves of high frequency emitted by it are obstructed by an object, they are reflected and received as signals by the sensors. The distance between transmit time and receive time is a representation of the distance of the object [12].
- **Raindrop Sensor**: This sensor is used to measure the average rainfall in a region of interest. This sensor module is a convenient component for detection of rain. It can act as a switch when a raindrop falls on the raining board and measure the rainfall intensity.
- **Temperature and Humidity Sensor**: This sensor is used to detect changes in atmospheric temperature and humidity in a region of interest. So, we use a DHT11 sensor that operates by single wire protocol and offers a digital output. The sensor can measure the temperature from 0 °C to 50 °C and the humidity from 20 to 90% with an accuracy of $\pm$ 1 °C and $\pm$ 1%, respectively.

After collecting the data, it is transmitted serially via the transmitter, which is received by the tuned receiver. The transmitter and the receiver are correctly interfaced with an Arduino kit or microcontroller each for communication. The data obtained from the hardware system are stored in the cloud and compared with the real-time data of rainfall, daily water level, temperature, and danger flood level. The

system takes a decision whether there is an emergency or not, and if the system finds an emergency, it sends a text to each registered person in the area. This article focusses on the integration of sensors to receive the results and modeling them before storing in cloud servers.

3 Mathematical Analyses

The mathematics of the system is based on the probability of rainfall, and its relationship to variables like occurrence times, and year of occurrence. This section describes the mathematics behind the prediction-based system proposed in this work.

Frequency of Rainfall and Probability

The probability of heavy rainfalls varies with locality as aforementioned. To determine the probability of return period or reoccurrence interval for such heavy rainfall, mathematical analysis is required. Assam is a state in Northeast India where heavy rainfall happens in the month of May–August almost every year. The calculation of the probability of reoccurrence interval of such type of rainfall is required to arrive a sustainable model for early detection of flood. Frequently occurred rainfall in Assam is equal to 187 mm [13]. Every year this type of rainfall occurs one to three times in Assam. Since every year this type of rainfall occurs, we have taken 12 months as a return period and this type of rainfall occurs between June and July months. The probability of rainfall occurring in each month $(P) = (1/T)$ has a chance of 8.3%. The probability of rainfall not occurring in each month $(Q)= (1-P)$ has a higher chance of 91.67%. The probability of rainfall occurring 'r' times in 'n' successive months [4] is given by

$$P_{r,\,n} = {}^{n}C_{r} \cdot P^{r} \cdot Q^{n-r}$$

where ${}^{n}C_{r} = \frac{n!}{(n-r)!r!}$. By using the above equation, we can calculate the probability of rainfall occurring a different number of times in a year or 12 successive months. For $P_{r=0,n=12} = Q^{n}$, reliability $= (1-P)^{\mathrm{nv}} = 35.2\%$ which is the probability of rainfall not occurring at all in '12' successive months. Similarly, for $P_{r=1,\,n=12} = 1-Q^{n}$, risk = 1–0.352 = 64.8%, which is the probability of rainfall occurring at least once in '12' successive months (Table 1).

From the plot in Fig. 2 and the mathematical analysis, it is seen that as the value of 'r' increases the percentage of probability of rainfall decreases. Here, for 5 times occurring rainfall, the probability is 0.17%, but in real life, the probability of 5 times occurring rainfall may be 0.1–10%. Since rainfall is a natural process, we cannot calculate the exact value. The theoretical value calculated is near to the practical values.

Flood Reoccurrence intervals

Table 1 Probability of rainfall occurring ‘r’ times in ‘12’ successive months

Rainfall occurring (r times)	Probability (%)
r = 0	35.2
r = 1	64.8
r = 2	19.1
r = 3	5.74
r = 4	1.19
r = 5	0.17

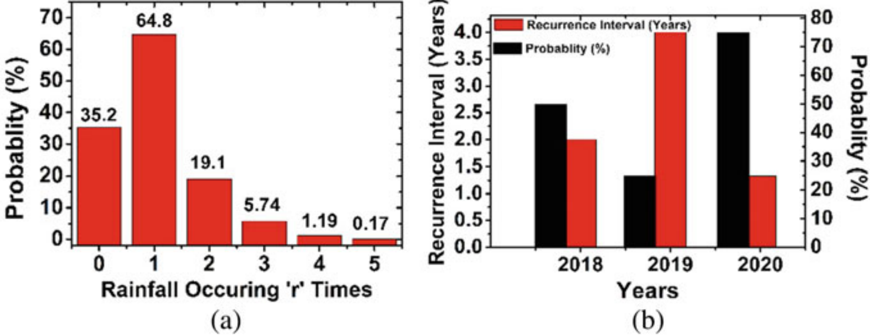

Fig. 2 **a** Plot probability versus rainfall occurring ‘r’ times. **b** Plot of probability/recurrence interval versus year

A parameter defined as the average time duration or predicted average time duration between natural events like earthquakes, floods, landslides, or river discharge flows is known as return period.

By using mathematical analysis, the probability and recurrence interval of floods can be calculated [6]. To calculate probability and recurrence interval, a few parameters have been used as defined here, and they appear in Table 2. The rank is defined as the number or order of a flood when all floods are arranged according to their size. The largest flood is allotted a rank of 1, followed by the second largest which is allotted a rank of 2, and so on. The total number of years is designated as “n.” In Table 2, n = 3. There are data from three years (2018–2020). Probability is calculated as $= \frac{\text{Rank}}{n+1} \times 100$, recurrence interval (R.I.) is defined as the average time between

Table 2 Probability and recurrence interval for three years

Year	Stage (Feet)	Rank	Probability	Recurrence interval (Years)
2018	214.37	2	50	2
2019	217.65	1	25	4
2020	213.52	3	75	1.33

re-occurrences. For example, R.I of two years means that the flood happens once in any given 2-year period. Recurrence interval is calculated as $\frac{n+1}{Rank}$.

From Table 2, it is seen that as the stage or feet increases the Recurrence interval also increases. But the probability of a flood occurring decreases as the recurrence interval increases as evident from Fig. 2b. Here we use the data of dangerous water levels for the district Sonitpur of Assam only [13]. For the other districts or other states, the probability or the recurrence interval will be different.

4 Results and Discussion

To carry out the analyses, and build a predictive framework, data from previous years were used to predict the parameters for 2020.

From the data for 2019, it is seen that the daily water level varies for different days. The minimum level of daily water level was 61.26 M, and the maximum level of daily water level was 66.34 M. The water level of Assam reaches the highest during July. So, the flood is recurring annually in this month. In Assam, for a good number of days, the water level remains at the maximum level which is above the fixed danger level of water. Owing to the geographical variation in different districts of Assam, the daily water level varies accordingly. Here the data of daily water level are taken for the area of Tezpur, Sonitpur District, only. The daily danger level remains constant at 65.23 M.

Here, in Fig. 3a, the markers represent the past value of daily water level [13] and the solid line represents the present value of daily water level measured by the sensor in the year 2020. From the above plot, it is seen that the past value of the daily water level is almost the same as the present value of the daily water level measured by the ultrasonic sensor. Here for 2020, the data of daily water level are measured by the ultrasonic sensor. The daily water level is measured by the water level sensor

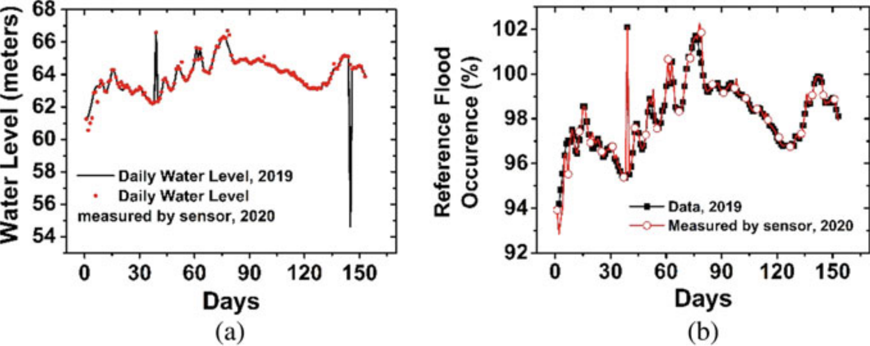

Fig. 3 **a** Plot of daily water level measured by the sensor w.r.t days. **b** Plot of reference flood occurrence percentage w.r.t days (153)

which varies for different days. The minimum daily water level is 60.56 M, and the maximum daily water level is 66.71 M. The minimum and the maximum values of the water level measured by the sensor are almost the same as the past values of the water level.

Figure 3b plots the reference flood occurrence in percentage by comparing the water level data from 2019 with that of the data measured by the sensor in 2020. From the observation, it is seen that the percentage for water level measured by the sensor is almost the same as that of the past value of the daily water level. Having validated the predictability of the sensor, it can be stated that if the value of the daily water level measured by the sensor is greater than the fixed danger level of the river of that area, an alert message will be sent to the mobile phone numbers by the server at which all data related to water levels and rainfall related variables are stored. However, the data of temperature, humidity, the measure of rainfall, and present speed of water measured by the sensor are also stored at the server so that from ~~all~~ the data, we can predict the probability of a flood of that area in advance.

Figure 4a shows the plots for daily water level and rainfall. Again, the temperature is also related to the daily water level. From Fig. 4b, it is observed that around every 10–12 days, there is a spike in the temperature sensed. But it may vary in some cases. However, the exact analysis and simulation of the mutual distribution of rainfall and temperature are very difficult due to the possible interdependence between them. It is generally said that the correlation between the rainfall [13] and the temperature [14] changes for different months. Since temperature [13], daily rainfalls [14], daily water level [14] all are related to each other, the probability of floods can be predicted in more advance before the flood occurs. But flash floods may not be predicted in advance due to high degree of their randomness of occurrence.

A comparison of this work with the existing methods is tabulated in Table 3. A quantitative comparison cannot be made among the works as the percentage of accuracy of prediction has not been cited in the compared works. However, a qualitative comparison among the works [15–17] can be made as mentioned in Table 3, which can project a status of the proposed work.

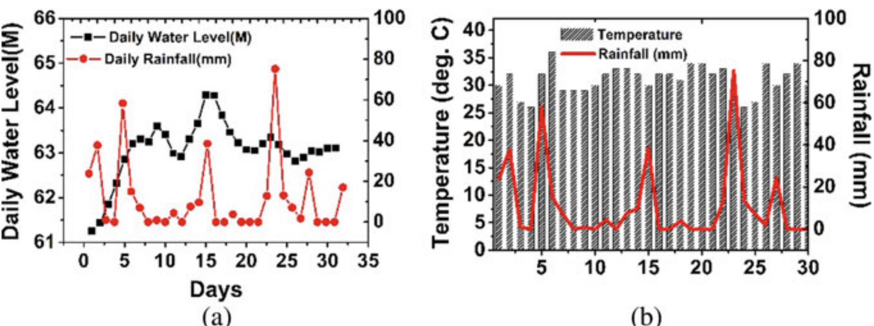

Fig. 4 **a** Plot of daily water level and daily rainfall w.r.t days (31). **b** Temperature and daily rainfall w.r.t. days (31)

Table 3 Comparison of this work with existing schemes

Work	Nature of data/connectivity	Cost effectiveness	Method	Predictability	Alert system
[15]	Real time (5 min)/internet	Yes	Artificial neural network	High	Server data
[16]	Real time/IoT	Yes	–	–	Mobile application
[17]	One to three days/satellite	No	Water surface fraction method	Extremely high	Monitoring station
This work	Real time and past year/wireless network	Yes	Probabilistic modeling	High	SMS (Short Message Service)

5 Conclusion

This article presented a strategy and a pilot prototype of a model that can predict floods, concerning a special case of Tezpur, Sonitpur District, India. Through mathematical backgrounds, the model sets the backdrop for the assimilation of sensors and utilizing them to collect data from the site. The method further depicts the communication between the instrumentation on-site to the cloud storage, from where they can be retrieved, and appropriate action may be taken. To cover rural areas where the internet may not be accessible and to make the information dissemination convenient, the message of warning is programmed in the proposed model to be sent in the form of text messages on mobile phones. The wireless transmission of data, computational methods, and validation show that the model can be used for flood prediction in the country, and abroad. Also, the developed system will help to build an intelligent flood prediction system by using an artificial neural network or other types of AI system in future.

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Hybrid Nonlinear Vibration Energy Harvester Due to Combined Effect of Stretching and Magnetic-Induced Nonlinearity

Osor Pertin and Koushik Guha

Abstract Vibration energy harvesting (VEH) is viable solution for battery free and self-powered micro-/nano-systems. The ambient vibration available for harvesting is low, random and broad. Hybrid energy harvester provides an alternative to narrow bandwidth, high operational frequency and low-power density VEH. In this paper, nonlinear hybrid vibration energy is developed by integrating both piezoelectric and electromagnetic VEH. The piezoelectric energy harvester and electromagnetic harvester is optimized for low frequency and maximum power generation configuration. The device is designed for maximum stretching-induced nonlinearity and repulsive magnetic nonlinearity to achieve bistable-quartic (BQT) potential. The potential profile and restoring force is studied to show enhanced performance of the device. When excited at the natural frequency of 59 Hz and acceleration amplitude of 0.5 g, a total voltage generation of 2.6 V (Piezoelectric voltage = 1.8 V and induced electromagnetic voltage = 0.8 V) is reported. The hybrid design enhances the frequency bandwidth, power generation and off-resonance operation making it efficient to be used in broadband random vibration environments.

Keywords Microelectromechanical system (MEMS) · Vibration energy harvester · Nonlinear · Wideband · Bistable · Stretching

1 Introduction

Microelectromechanical system (MEMS)-based vibration energy harvester (VEH) has been very popular among the micro-energy harvesting methods for their easy miniaturization, implementation and high power density [1]. VEH devices usually harvest the ambient mechanical vibration into usable electrical by electrostatic, piezoelectric and electromagnetic transduction mechanisms. Piezoelectric harvester (PEH) and electromagnetic harvester (EMH) are popular among researchers because of their high electromechanical coupling effect and they do not require external bias

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source like electrostatic harvester. The generated electrical output can be used to realize self-powered microelectronics circuits like wireless sensor nodes (WSN), implantable and wearable devices. Conventional linear VEHs based on resonance of the structure have the drawback of high frequency, narrow bandwidth and low output generation**.** Also, the environmental vibration is low, broad and varying with time and therefore the VEHs perform inefficiently in real-time practical use. Significant researchers have been resolute on reducing the operational frequency, widening the bandwidth and enhancing the output power density of the VEHs [2, 3].

Nonlinear vibration energy harvester has become a recent popular choice owing to its lower resonant frequency and broad bandwidth. It is proved that introduction of nonlinearity in energy harvesting will broaden the operational bandwidth and show superior power generation [4]. Marzencki M et al. introduced nonlinearity into a clamped–clamped PEH device with a central located seismic mass by redesigning the interlayer stresses of beam [5]. In 2009, Erturk et al. [6] and Cottone et al. [7] reported the bistable PEH configurations based on magnetic attraction and repulsion arrangements, respectively, that shows the potential energy profile with a potential barrier between two potential wells. Navabi S et al. proposed a MEMS PEH, whose operational bandwidth is improved taking the advantage of both the multimodal and stretching-induced nonlinearity [8]. But the three proof masses used increases the size and device complexity. In a similar design concept, Liu et al. achieved a wide band electromagnetic harvester using an array of harvester unit covering different designated frequencies [9]. Saibal R et al. reported that magnetic-induced bistable nonlinear structure reduced the frequency while restricting the bandwidth widening [10]. Therefore, Pranay P et al. of same team developed and demonstrated that magnetic-induced bistability and stretching-induced quartic potential profile in a single design enhances the performance across the vibration spectrum of an electromagnetic VEH device [11]. But usually output performance is reduced for broadband harvester.

Hybrid energy harvesters have been developed by many researchers in order to enhance the generated power. It is reported that Hybrid VEH configuration integrated with piezoelectric and electromagnetic mechanism shows improved performance compared to the single mechanism in widening the bandwidth and enhancing the output power [12, 13]. In 2019, Guangyi Z et al. proposed a hybrid energy harvester composed of a piezoelectric portion contained with a double-clamped trapezoidal beam and an electromagnetic portion featured with a plane coils and a magnet sleeve [14]. They experimentally found that output power shows 52.4% improvement generating 0.637 mW power. Haipeng L et al. reported a hybrid harvester based on fixed–fixed beam with deposited PZT layers and magnetic attraction-induced nonlinearity which reduced the stiffness and operational frequency [15]. Similar nonlinear hybrid harvester is designed by Ping L et al. which benefits from the advantages of nonlinear magnetic repulsion technique and frequency up conversion simultaneously [16].

In this paper, a hybridization of nonlinear PEH and nonlinear EMH approach is developed for harvesting vibration energy. We have used the novel idea of nonlinear segmented trapezoidal PEH that will also introduce stretching into the

hybrid system. Trapezoidal FR4 material cantilever beam with segmented piezoelectric (PZT) layers, NdFeB permanent magnet and a circular copper coil are used to make the hybrid energy harvester design. The harvester induces bistability through repulsive magnetic arrangement at tip of the FR4 spring structure and administers quartic potential profile with very low potential barrier between two wells due to stretching of thin and hollow fixed guided trapezoidal beam. It is already proved that segmented trapezoidal PEH at strain nodes shows improved performance compared to the conventional non-segmented PEH [17]. Tapered hollow structure demonstrates stretching in high order which enhances the frequency bandwidth and power density of the VEH [18]. For maximum electromagnetic-induced voltage, already reported four pole arrangement of NdFeB permanent magnets and circular wound coil are employed [10, 11]. The model of the hybrid harvester is developed and simulated across range of frequencies for performance analysis.

This paper is organized as follows: Sect. 2 describes the development of the hybrid VEH design and simulation. Section 3 discusses the simulation obtained results. The concluding comments are given in Sect. 4.

2 Structural Design and Simulation of the Nonlinear Hybrid Vibration Energy Harvester

2.1 Structural Design

The harvester design consists of FR4 material spring structure, segments of PZT layers, NdFeB magnets, and copper wound coil. Figure 1(a) shows the proposed hybrid design where the stretchable segmented trapezoidal PEH employs the piezoelectric transduction and the copper coil and NdFeB magnets arrangement employs electromagnetic transduction for harvesting electrical energy from mechanical energy. For the electromagnetic part, Fig. 1(b) shows the distribution of magnetic-field of the four magnets arrangement around the coil responsible for maximum flux distribution and a soft magnet sleeve that will bind magnetic-field lines in a narrow region to make the coil cut more induction magnetic lines which will in turn improve the electromagnetic output. Figure 1(c) shows the schematic diagram of the nonlinear PEH portion. The trapezoidal beam design produces more uniform strain distribution and therefore makes efficient use of the beam volume compared to the conventional rectangular beam. The rectangular holes at the wider end of the trapezoidal piezoelectric harvester will reduce the stiffness and increase the order of stretching. Figure 1(d) shows the piezoelectric polarization direction of the PZT beam which can be used to locate the strain node for segmentation. The magnetic repulsive pair at guided end of FR4 spring structure introduces bistable nonlinearity into the system.

The generalized Duffing potential energy equation $U(y)$ and the consequent spring reaction force which is derivative of the potential, $F(y) = -\frac{\partial \mathrm{U(y)}}{\partial y}$ is given by [11],

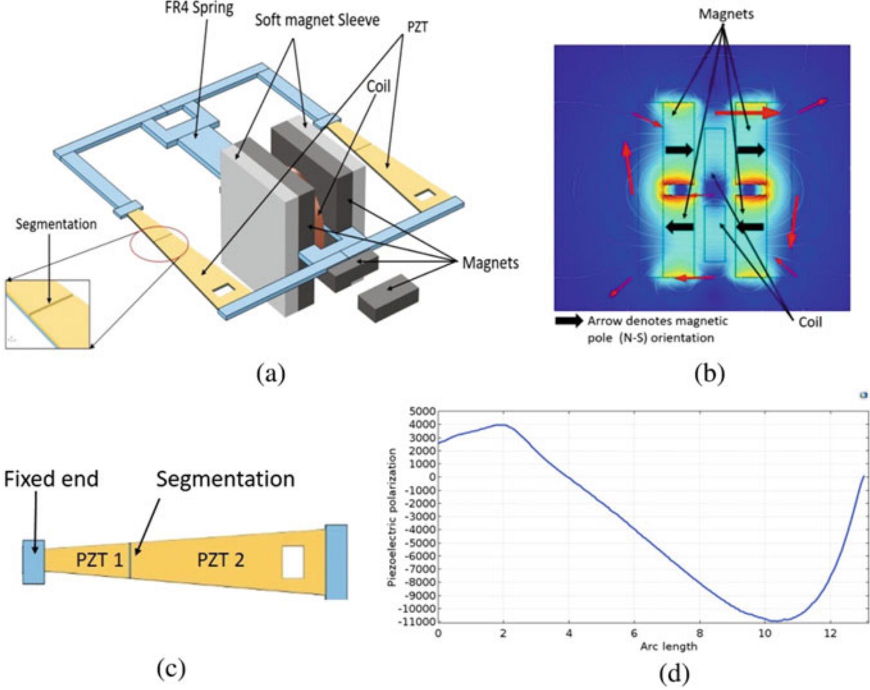

Fig. 1 **a** Proposed nonlinear hybrid piezoelectric-electromagnetic VEH. **b** Magnetic flux lines in electromagnetic assemble. **c** Schematic of segmented nonlinear trapezoidal PEH. **d** Piezoelectric polarization curve along the piezoelectric beam length

$$U(y) = \frac{1}{2}Ay^2 + \frac{1}{4}By^4 \tag{1}$$

$$F(y) = -Ay - By^3 \tag{2}$$

where y represents the deflection of the oscillator, A and B are independent nonlinear parameters.The final generated power of the designed nonlinear hybrid energy harvester is the sum of piezoelectric power output P_p and electromagnetic power output P_{em}.

$$P_{\text{output}} = P_p + P_{\text{em}} \tag{3}$$

Table 1 Geometric dimension and material properties

Description (Geometry)	Value	Description (Material)	Value
Total length of device	35 mm	Density of PZT	7500 (kg/m^3)
Piezoelectric stretching beam length	12 mm	Density of FR4	1900 (kg/m^3)
Beam Width at clamped end (x = 0)	1 mm	Density of NdFeB	7500 (kg/m^3)
Beam width at guided end (x = l)	3 mm	Young modulus, PZT	64(GPa)
Thickness of PZT	0.1 mm	Young modulus, FR4	22(GPa)
Thickness of FR4 substrate	(0.1–0.4) mm	Young modulus, NdFeB	160(GPa)
Distance between two PZTs	0.1 mm	Piezoelectric constant	−16.6(C/m^2)
Distance between two repulsive magnets Magnet size Mass of magnets	3.5 mm 8 × 4 × 1.5 mm 3.6 kg$\times 10^{-3}$	Permittivity constant	25.55 (nF/m)

2.2 Finite Element Analysis

The hybrid VEH design model is created using FEM software COMSOL MULTIPHYSICS 5. Body load of 0.5 g acceleration is applied as mechanical input on the device. The FR4 spring is fixed at the one end and the other end is guided by the applied excitation. The structure is meshed before performing any simulations analysis. Complete mesh consists of 21,610 domain elements, 12,347 boundary elements, and 2292 edge elements.Geometry and material properties of the structure is given in Table 1.

3 Result and Discussion

The force vs. displacement curve shows nonlinear behavior of the system (Fig. 2(b)) while the potential energy profile shows a bistable-quartic curve with two wells having a very shallow potential barrier between the potential wells (Fig. 2(c)) as compared to single well profile of a mono-stable quartic configuration without repulsive magnetic pair. The obtained nonlinear stiffness constant of the BQT is 4.83 $\text{N}\times 10^7/m^3$ while mono-stable configuration shows a stiffness value of 6.26 $\text{N}\times 10^6/m^3$.

Figure 3 compares the generated voltage of hybrid harvester to single-energy harvesters. The combined effects of stretching nonlinearity and repulsive magnetic bistable nonlinearity improve the frequency bandwidth of both the generated piezoelectric voltage and induced electromagnetic voltage in the coil. The generated

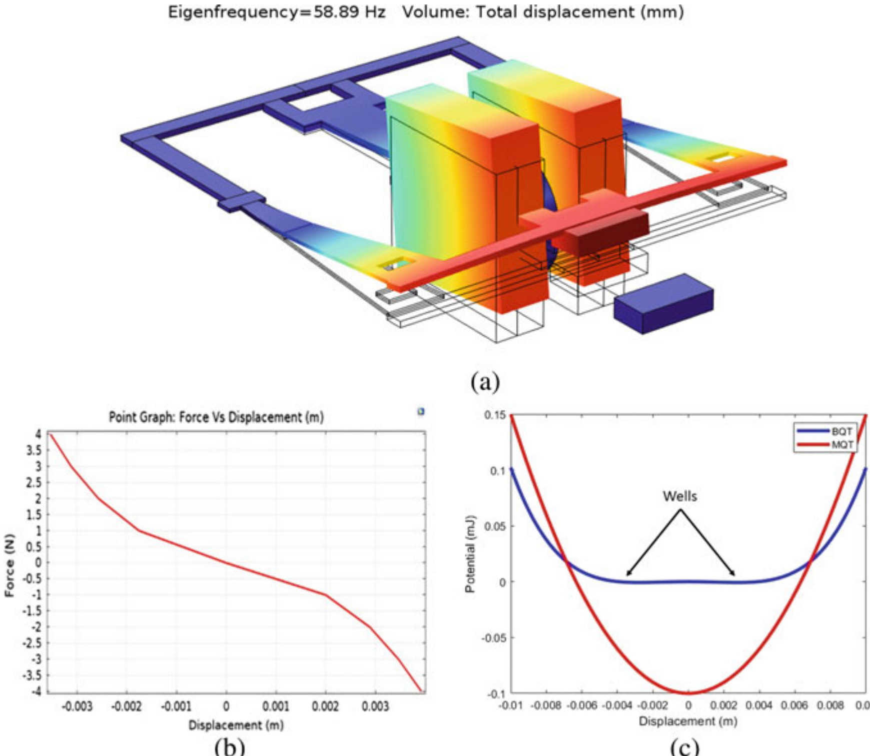

Fig. 2 **a** Proposed design in the fudamental mode of vibration with 58.89 Hz eigen frequency. **b** Nonlinear restoring force. **c** Comparison of potential energy profile of bistable-quartic (BQT) configuration having a distance of 3.5 mm between the two repulsive magnet pair and mono-stable qartic (MQT) configuration without the magnetic pair

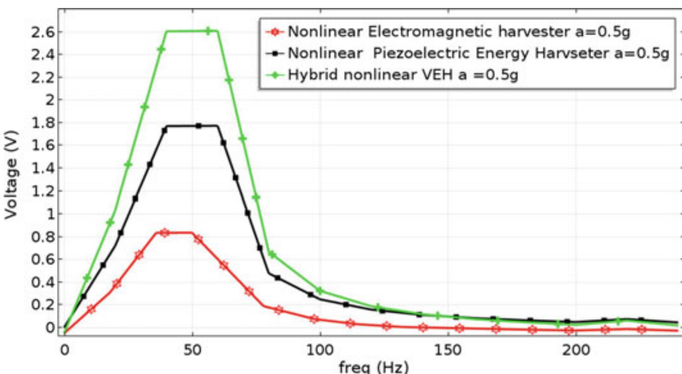

Fig. 3 Output voltage comparison of nonlinear piezoelectric energy harvester, nonlinear electromagnetic energy harvester and hybrid nonlinear energy harvester across a frequency sweep of (10–250 Hz)

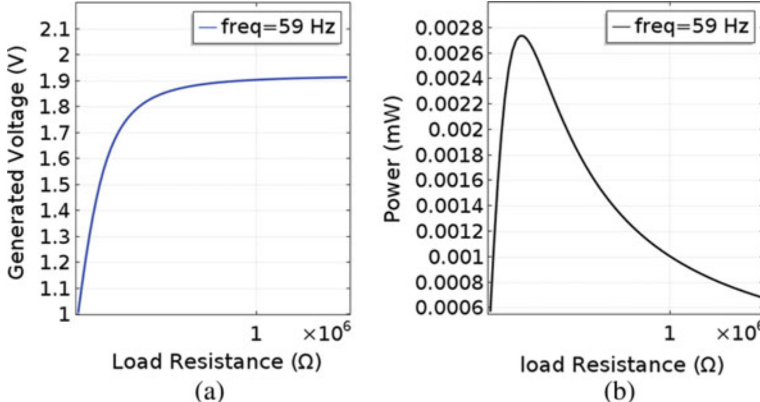

Fig. 4 **a** The varying output voltage for varying piezoelectric load resistance, **b** varying output power for varying load at mechanical excitation of 59 Hz and 0.5 g

voltage of PEH portion is 1.8 V and of EMH portion is 0.8 V for 0.5 g input acceleration and optimal load value of 200kΩ. The generated piezoelectric voltage depends on the size of piezoelectric PZT layers and therefore the generated voltage is lesser compared to state-of-art piezoelectric harvesters because the proposed model also include the concept of nonlinearity due to stretching reducing the size of PZTs. The output of the hybrid nonlinear VEH is the sum of piezoelectric voltage and electromagnetic voltage, and hence, hybrid design shows increase in power generation capability compared to single harvesters.

The peak operating frequency of the proposed harvester will change with different mechanical acceleration input; therefore, the optimal load of the harvester too changes. The load resistance of the electromagnetic harvester does not vary greatly and is kept constant at 1000 Ω. The change in piezoelectric voltage at the peak resonant frequency of 58.88 Hz and mechanical excitation of 0.5 g for varying load resistance is as seen in Fig. 4. The optimal piezoelectric load resistance is reported to be 200kΩ.

4 Conclusion

A low-frequency hybrid nonlinear VEH using both piezoelectric and electromagnetic transduction mechanism is proposed and studied. The choice of FR4 material and optimized shape of the spring structure for maximum stretching results in lower oscillating frequency. The introduction of nonlinearity using stretching and bistable repulsive magnet shows improvement in frequency bandwidth, output generation capability and off-resonance performance making it efficient to be used in broadband random vibration environments. The reported generated voltage is quite enough to operate the WSNs and nano-/microsystems.

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Design and Performance Evaluation of 1 KB SRAM in SCL 180 nm Technology

Abhishek Kumar, Abhishek Sahu, and Shree Prakash Tiwari

Abstract A 1 KB static random access memory (SRAM) and its control circuit are designed to be implemented in 180 nm technology. Designed SRAM is working on 200 MHz and exhibited good memory cell stability. Overall SRAM architecture was implemented using 6 transistors (6 T) memory cells accessed by row and column decoders. Control logic architecture was also implemented to perform read and write operations using sense amplifier and write driver circuits, respectively. The circuit achieved memory access time of 2.7 ns, which is among the lower values from many earlier published reports for similar technologies, while consuming 5.2 mW power for one byte.

Keywords Static random access memory (SRAM) · SRAM control circuit · Sense amplifier · Write driver · Row and column decoders

1 Introduction

Memory arrays are important part of any digital integrated system [1]. Over the years, due to the dawn of low power and high-integrated density electronic gadgets such as mobiles, computers, etc., there was a great necessity of technology progression in memory chip design [2]. Static random access memory (SRAM) has also gone through these technology advancement phases. SRAM is generally used in microprocessors as a cache memory because of its high processing speed. Many topologies of SRAM cell and other peripherals, which are used in memory block, have been proposed over the years to reduce the power consumption as well as area of system on chip (SoC) [3]. In memories, there is always a trade-off between power consumption and speed of operation [4]. Hence, it is always a challenging task in memory designing to keep both these parameters, i.e., power consumption and speed balanced, while keeping minimum area of SoC [5, 6].

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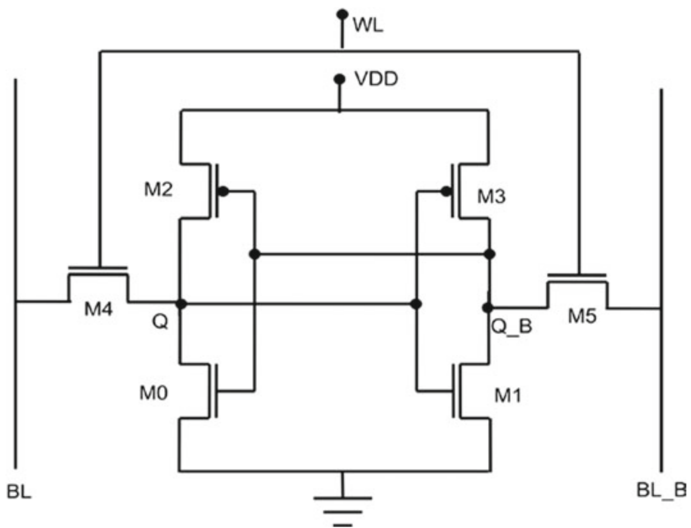


Fig. 1 Schematic of basic 6 T SRAM cell

SRAM is a volatile memory, which means data stored in it retained till the power is ON. A conventional 6 T SRAM cell dominates among various other topologies such as 8 T, 5 T, 4 T, and load-less 4 T SRAM cell because of its advantages such as higher cell stability at lower supply voltages and lower process complexity [7–10]. 6 T SRAM cell constitute two NMOS driver transistors (M0 and M1), two PMOS pull-up transistors (M2 and M3), and two NMOS access transistors (M4 and

M5) as depicted in Fig. 1. 6 T SRAM cell utilizes two cross coupled inverters to form a bi-stable latch making it capable of storing 1 bit at a time during data retention mode. Access transistors in cell are coupled with bit lines BL and BL_B (where BL_B is inverted BL) on opposite sides and can be triggered with a word line (WL) control signal, which provides isolation between bi-stable latch and bit lines during hold mode [1, 11, 12].

2 SRAM Operation

2.1 Hold Mode

Bi-stable latch is disconnected from both the bit lines because access transistors (M1 and M2) are inactive preventing any charge flow. Hence, latch retains the data which is already stored in it till any change in access transistors and power is ON. This mode of operation consumes less power because of less leakage current of 6 T SRAM cell.

2.2 Read Operation

For a bit stored in cell prior to retrieving the data, precharge circuit is activated which charges both the bit lines (BL and BL_B) capacitors to supply voltage (VDD), and then by accessing word line (WL) signal, data can be retrieved from cell by enabling sense amplifier.

For stable read, driving capability of driver transistor must be greater than driving capability of access transistor [1]. To satisfy this condition, cell ratio must be greater than 1 as given in Eq. (1), which usually comes around 1.5–3.

$$\text{cell ratio} = \frac{(W/L)_{\text{driver}}}{(W/L)_{\text{access}}} > 1 \tag{1}$$

2.3 Write Operation

Prior to writing a bit into a cell, precharge circuit charges the bit lines capacitors to desired values. When WL is turned ON, bit lines overpower cell with new values using write driver circuit, which grounds the bit line corresponding to bit '0.'

For stable write, driving capability of access transistor must be greater than driving capability of pull-up transistor [1]. To satisfy this condition,

$$\text{pull-up ratio} = \frac{(W/L)_{\text{pull-up}}}{(W/L)_{\text{access}}} < 1 \tag{2}$$

2.4 SRAM Read Write Control

This was designed using a decoder circuit with WRITE/$\overline{\text{READ}}$ and Mem_en (memory enable) inputs and to be storing the bits at moderate frequency of 200 MHz. It accommodates 10 bits address and 8 bits data line which is activated when write and read operations are initiated on Mem_en = 1, otherwise remains idle.

When Mem_en = 1, it activates precharge circuit (PRE) and word line enable (WLE), which then activates the word line according to address from address bus. Enabling the address line, enables the word line WL in SRAM, making it ready to be accessed for write or read using WRITE/$\overline{\text{READ}}$ control line. Both the read and write operations are activated alternatively as.

$$\text{WRITE}/\overline{\text{READ}} = \begin{cases} if 1, activates WRITE \\ if 0, activates READ \end{cases} \tag{3}$$

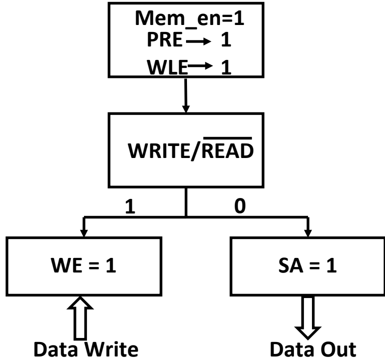


Fig. 2 Logic flow diagram of SRAM control circuit

Activating WRITE, load bits from data bus and simultaneously turns writer driver circuit ON, leading to data write in respective cells. On activating read, sense amplifier is turned ON, and hence, bits are loaded to data bus, leading to data read operation. The control circuit logic flow diagram is given in Fig. 2.

3 Design of Blocks and Their Integration

SRAM memory comprises of memory cell array, word line driver, row decoder, column decoder, sense amplifier, write driver circuit, precharge circuit, and all of them are controlled by a control circuitry, as shown in Fig. 3.

3.1 Memory Cell Array

1 KB (1024×8 bit) SRAM memory requires 10 address lines to access 1024 location of memory in which each location has 8 bits long data accessed by 8 data lines. In linear memory organization, cells are organized in the form of a two-dimensional array with rows and columns using address (word line) and data lines, respectively. This organization created scaling problem by forming a long and narrow memory cell causing few word lines to be smaller in size, and the end lines get very long causing uneven read or write delays. To overcome this problem, the cell matrix created has the array of 128×64 created by 7 row address lines ($2^7 = 128$ combinations) and 3 column address lines ($2^3 = 8$ combinations) coupled with 8 bit lines making a total of $8 \times 8 = 64$ data lines in row [13].

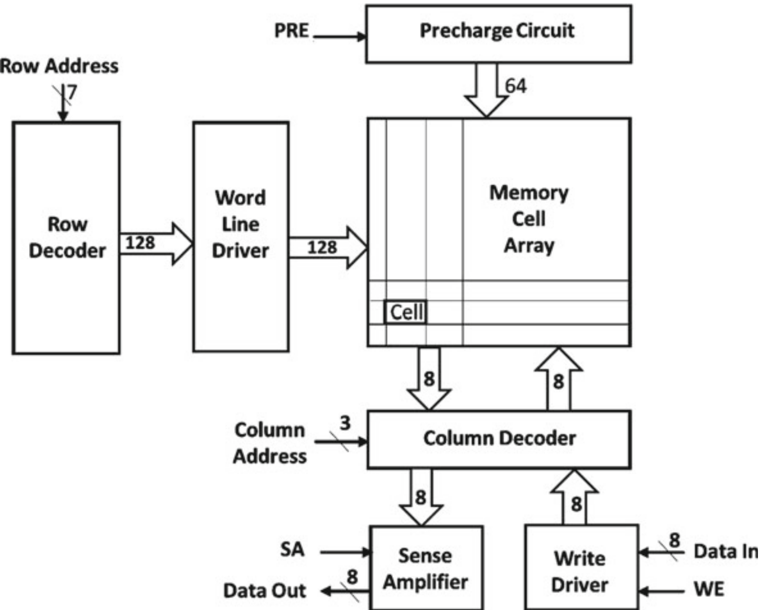


Fig. 3 SRAM block architecture

3.2 *Word Line Driver*

Even on shrinking the memory cell, the row decoder output was unable to drive efficiently till 64th bit on a word line. To overcome this, a word line driver was needed with every decoded lines. The driver circuit consists of even number of inverters arranged in increasing order of their transistor sizes, which are following the decoder output controlled by word line enable signal.

3.3 *Row and Column Decoders*

The decoder circuits provide 2n outputs for given n inputs. Here row decoder creates 128 word lines from 7 of the 10 address lines, and column decoder creates 8 bit lines (BL) from remaining 3 address lines. In addition, the column decoders create BL_B from BL by using inverters.

Using the column decoder, apart from selecting a byte, a bit or a set of bits can also be selected by providing bit select lines. For 8 bits, three (23) such select lines can be provided.

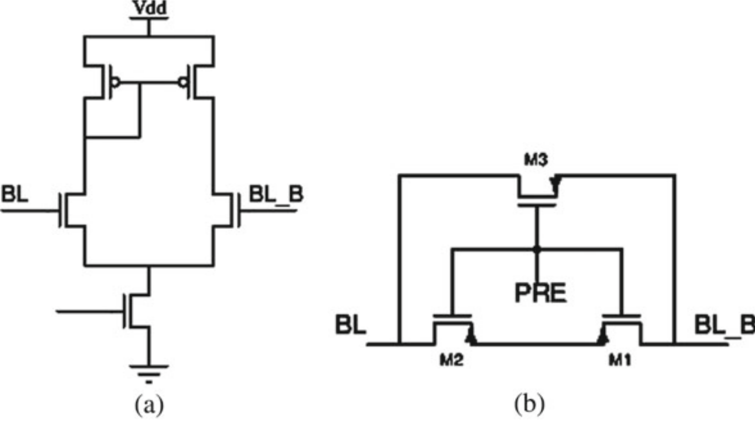


Fig. 4 Schematic of, **a** differential sense amplifier, **b** 3-transistors precharge circuit

3.4 Write Driver Circuit

It pulls down one of bit lines to ground (0 V) depending on input bit, which is going to be written in selected cell during write operation. Since both the bit lines are inverse of each other, '1' will be followed on the other line. After which, the new bits are loaded from bit lines BL and BL_B to *Q* and QB when word line is ON.

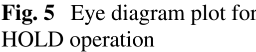
The write driver circuit is controlled by write enable (WE) signal and when turned ON, loads the bits from Data_in to memory cells. These cells are addressed by word line decoder.

3.5 Sense Amplifier

It is an important circuit (Fig. 4a), which regenerates the bit line signals in a memory design [14]. It perceives the information stored in selected cell by detecting the small voltage variation between the bit lines (BL and BL_B) during read operation. The differential sense amplifier used here is a basic differential amplifier comparing the bit lines BL and BL_B when sense amplifier control signal SA is accessed.

3.6 Precharge Circuit

It is also known as bit line conditioning circuit which has the task to charge both bit lines to supply voltage VDD before read and write operations. The circuit comprises of three PMOS transistors of which M1 and M2 are used for precharging and M3 for equalizing voltages on bit lines as shown in Fig. 4b.



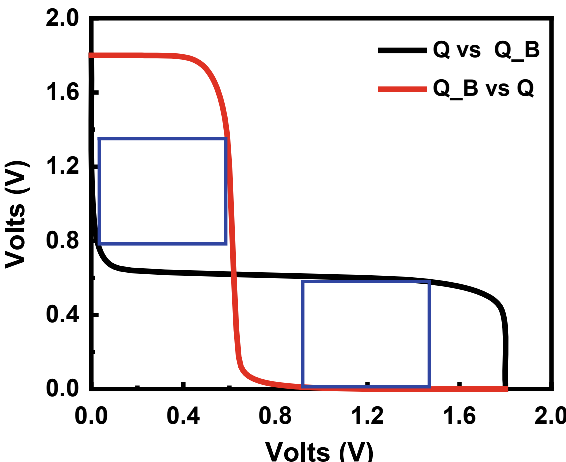


Fig. 5 Eye diagram plot for HOLD operation

4 Results and Discussion

The circuit was designed and simulated using Cadence Schematic Design Suite, and the layout was simulated in caliber using 180 nm process design kit (PDK) from semi-conductors laboratory (SCL). For all three SRAM modes, noise margins were calculated, and SRAM read and write operations were performed.

4.1 Static Noise Margin (SNM)

It is defined as minimal voltage that can be employed at storing terminal of cell such that alteration in stored information take place. Static noise margin characterizes noise margin of SRAM cell in data retention (hold) mode, which quantifies the cell stability in the presence of noise. The SNM of SRAM cell is measured by analyzing voltage transfer characteristics (VTC) of each half-cell of SRAM (one inverter at a time) creating an eye (or butterfly) diagram [9].

Noise margin (NM) of a memory cell for any operation can be determined as minimum of both halves of cell which is given as [1, 12]:

$$N = \min\left(NM_{\text{high}},\ NM_{\text{low}}\right) \tag{4}$$

From Fig. 5, the SNM for HOLD operation was evaluated to be 560 mV, as the smallest fitting square.

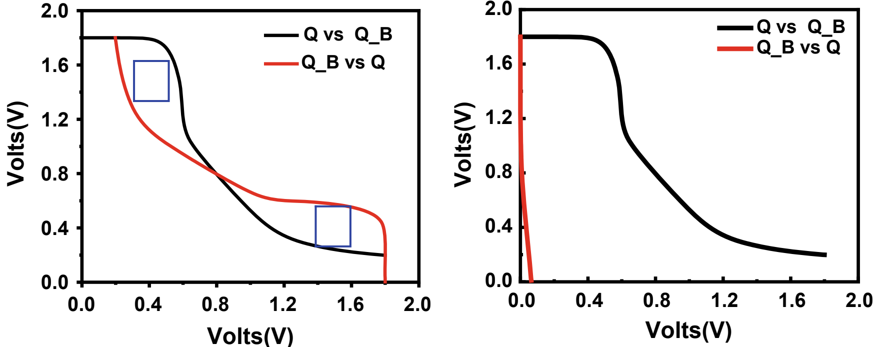


Fig. 6 Eye diagram plot for (a) READ operation (b) WRITE operation

Table 1 Cell ratio versus read noise margin

Cell ratio	RNM (mV)
4.0	390
3.0	360
2.5	320
2.0	290
1.5	270

4.2 Read Noise Margin (RNM)

The SRAM cell has to render an unaltered and stable read. Since cell is more susceptible to noise during read operation therefore for stable read, cell must possess high read noise margin. The RNM of SRAM cell is defined as capability of cell to avoid alteration of stored data during read operation.

From Fig. 6a, it is clearly seen as smaller the noise margin square, more are the chances for it to flip data during read operation [9]. Read noise margin is directly proportional to cell ratio. Keeping high cell ratio, better cell stability can be attained during read operation as shown in Table 1.

4.3 Write Noise Margin (WNM)

Write noise margin is defined as maximum noise voltage tolerated at bit lines for stable and successful write operation. This quantity indicates the cell stability during write operation. In 6T SRAM cell, the write noise margin is always greater than static noise margin as well as read noise margin, since the other inverter in memory cell latch has its output grounded during write operation [9].

Here from Fig. 6b, the measured SNM is 590 mV, measured as largest fitting square above 0.9 V on vertical axis, while writing ‘0.’ In 6T SRAM cell, WNM varies directly with pull-up ratio, i.e., WNM increases with increase in pull-up ratio (Table 2).

4.4 SRAM Read and Write Operations

The output plot in Fig. 7 shows bit ‘1’ stored in a cell. BL changes from ‘1’ to ‘0’ when IN being ‘0’ is transferred to BL. This change in cell bit can be observed at OUT when SA is made ‘1,’ where OUT changes from ‘1’ to ‘0.’

From the results, the comparison from features of our work with few similar work previously published is given in Table 3. A better access time was achieved in our

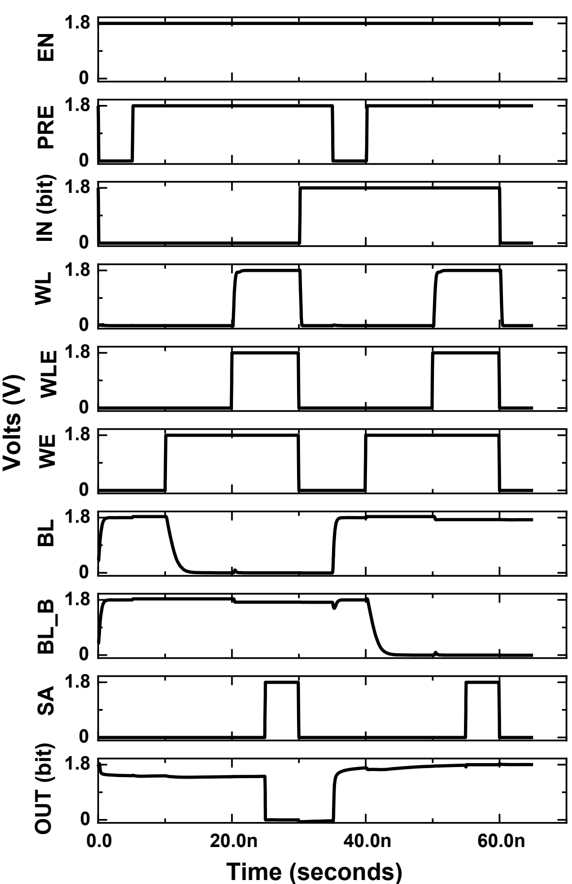


Fig. 7 SRAM read and write operations

Table 2 Cell ratio versus write noise margin

Cell ratio	WNM (mV)
1.2	600
0.9	595
0.7	590
0.6	580
0.5	570

Table 3 Comparison of results with similar reports

SRAM	[15]	[17]	[16]	This work
Technology	350 nm (0.8V)	250 nm(1.8V)	180 nm(0.65V)	180 nm(1.8V)
Size	$1M \times 1$ bits	$4.5M \times 1$ bits	$32K \times 8$ bits	$1K \times 8$ bits
Access time	10 ns	1.8 ns	8.33 ns	2.7 ns
Power consumption	5 mW	2.8 mW	1.7 mW	5.2 mW

design than that for [15] and [16]. However, the consumed power reported in this work is higher, due to the higher supply voltage.

5 Conclusion

A 1 KB SRAM was designed to work on 200 MHz clock speed using basic 6 T cell architecture. To control its read and write operations, a control circuit was also designed. This design was implemented on 180 nm PDK provided by SCL, which allows the power supply up to 1.8 V.

Arranging memory cells by dividing address lines in two parts (7 and 3) created a compact cell array with lower number of select lines and smaller row and column decoders. The uniformity of cell arrangement ensured equal read, write, and access times throughout the memory block. The cell stability analysis of 6 T SRAM cell for different cell ratio and pull-up ratio was also analyzed. Higher cell ratio achieved better cell stability during read operations by providing higher read noise margins. Increase in pull-up ratio leads to rise in write noise margin, but the ratio should not increase above 1 for successful write operation. While matching the results with similar reports, it can be concluded that our results were comparable to them.

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Comprehensive Analysis of **α**- and **β**-form of Copper (II) Phthalocyanine for Organic Field-Effect Transistors

Ajay Kumar Mahato, Deepak Bharti, Vivek Raghuwanshi, Ishan Varun, and Shree Prakash Tiwari

Abstract In this work, α-form and β-form of copper (II) phthalocyanine (CuPc) were used for fabrication of OFET devices and the corresponding electrical performance was studied. OFETs with α-form CuPc were found to exhibit better device performance with an average mobility of $4.7(\pm 1.0) \times 10^{-3}$ cm^{2}V^{-1} s^{-1} compared with β-form with an average mobility of $0.9(\pm 0.2) \times 10^{-3}$ cm^2 V^{-1} s^{-1}. The better device performance of α-form CuPc OFETs was attributed jointly due to thinner active semiconductor and better film uniformity in α-form CuPc OFETs over β-form devices.

Keywords OFETs · CuPc · α-form CuPc · β-form CuPc

1 Introduction

Over the past few years, several groups across the globe have significantly explored organic field-effect transistors (OFETs) technology for different applications because of several benefits which include cost-effectiveness, low-temperature deposition, mechanical flexibility, and compatibility for large-area fabrication [1]. To utilize these devices applications, including high yield, higher reliability, and good electrical performance, is desirable. Though, solution process able organic semiconductor materials endow the advantages of cost-effectiveness [2, 3]; however, film uniformity is a matter of concern. But, thermally evaporated organic semiconductor provides higher uniformity and crystallinity of deposited films [4], which eventually leads to high yield and stable electrical performance in devices. Among various

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thermally evaporated organic semiconductor materials, metal-substituted phthalocyanines (MPcs) have been studied with great interest due to their exclusive physical, chemical, and optoelectronic properties and have been demonstrated for numerous applications which include solar cell, OFETs, gas and humidity sensor, nonvolatile memory, organic rectifiers, etc. [5–8]. For OFETs, copper (II) phthalocyanine (CuPc) is preferred over other MPcs, because of its decent field-effect mobility. Commercially, CuPc exists mainly in two crystalline forms, commonly called as α-form and β-form. However, reports for exclusive comparison of electrical performance of α- and β-form of CuPc OFETs are scarce.

In this work, OFETs were fabricated using α- and β-form of CuPc as an active semiconductor layer on a heavily doped (n^+) silicon (Si) substrate with a bilayer gate dielectric (spin-coated polystyrene (PS) on thermally grown 300 nm SiO_2) to explore their electrical performance. Bilayer gate dielectrics are known to offer various advantages in terms of device performance over single layer [4, 9]. OFETs with α-form CuPc were operated at lower voltage than with β-form and also showed better electrical performance. To investigate the underlying reasons, both the forms of CuPc were characterized for their material properties using techniques such as UV–Vis spectroscopy, Raman spectroscopy, XRD, and atomic force microscopy (AFM). Both forms of CuPc exhibited similar characteristics in UV–Vis spectroscopy. Moreover, in UV–Vis spectroscopy the deposition of α-phase of CuPc at room temperature using both α- and β-forms of CuPc was revealed. In AFM spectroscopy, α-form of CuPc exhibited lower surface roughness compared with β-form, which in turn attributed to the better device performance in OFET based on α-form of CuPc. Though diffused Raman peak was obtained for powder β-form CuPc, nearly identical degree of crystallinity of α- and β-form CuPc was indicated by XRD.

2 Experimentation

OFETs were fabricated using both forms of CuPc on a heavily doped (n^+) silicon substrate with a bilayer gate dielectric (spin-coated PS on thermally grown 300 nm SiO_2). Cleaning of samples was done using ultrasonication in 2-propanol, trichloroethylene (TCE), and methanol at 80 ºC, followed by drying in N_2 flow. A 0.5wt. % solution of PS was prepared in toluene at 70 ºC under constant magnetic stirring for a duration of 2 h. Spin-coating of PS solution on a Si/SiO_2 substrate was performed at 2000 rpm for a period of 30 s, followed by annealing at 60 ºC for a duration of 30 min. α- and β-form CuPc (Mw ~ 576.08) was purchased from TCI Chemicals and used it for OFET fabrication without any purification. A thin layer of CuPc (α- and β-form) was deposited through thermal evaporation on a PS-coated Si/SiO_2 substrate at a pressure level of 2×10^{-5} Torr. The thickness of the deposited CuPc layer was measured to be 43.4 ± 2.2 nm and 53.5 ± 1.3 nm for α- and β-form of CuPc, respectively. Further, thermal evaporation of gold (Au) was performed at a pressure of 1.8×10^{-6} Torr for source/drain contact deposition with various aspect (*W/L*) ratios using a shadow mask, which acts as a top-gate electrode, while a heavily doped (n^+)

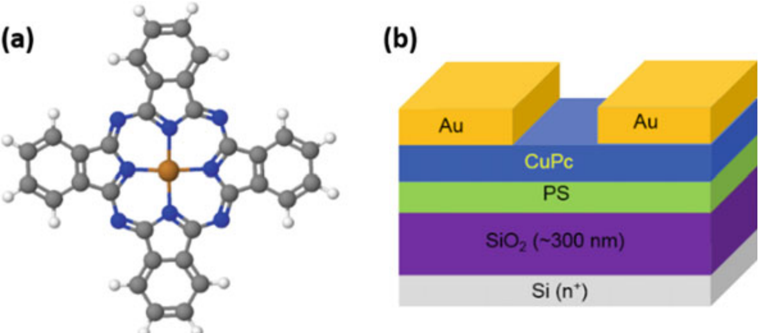

Fig. 1 **a** Chemical structure of CuPc, **b** device structure of CuPc OFETs

silicon substrate acts as a bottom-gate electrode. Procedures of extraction of various OFET's electrical parameters such as maximum field-effect mobility (μ_{max}), average field-effect mobility (μ_{avg}), average threshold voltage ($V_{\text{TH,avg}}$), average subthreshold swing (SS_{avg}), and average interface trapped densities ($D_{\text{it,avg}}$) were discussed in our earlier report [10]. The gate capacitance density (C_{i}) for SiO_2/PS bilayer was evaluated to be ~4.9 nF/cm^2 at a frequency of 1 kHz. To explore the distinct features of α- and β-form CuPc, material characterizations such as UV–Vis spectroscopy, Raman spectroscopy, XRD, and AFM spectroscopy were performed. A Lambda 750 UV–Vis spectrophotometer from Perkin Elmer was used to perform UV–Vis spectroscopy for the wavelength ranges from 270 to 1000 nm. A STR-500 conformal micro-Raman spectrometer from AIRIX Corporation was used to perform Raman spectroscopy of CuPc samples. CuPc powder samples were exposed to green-colored laser having a wavelength of 532 nm with an input power of 25 mW for a spectral range of 450–1650 cm^{-1} for Raman spectroscopy. XRD measurement of powder samples of CuPc was taken using X'Pert Pro from PANalytical Ltd. The percentage crystallinity was measured as the ratio of area of crystalline peaks to the area of the whole diffractogram. Thickness measurement of the deposited semiconductor layer was taken using a Dektak XT surface profiler from Bruker. SPM XE-70 from Park Systems was used to capture the surface morphology of the deposited CuPc thin film using AFM spectroscopy. Chemical structure of CuPc and OFET device structure are shown in Fig. 1.

3 Results and Discussion

3.1 Transistor Performance

Figure 2 summarizes the comparison of transfer and output characteristics of both types of CuPc OFETs with an aspect ratio of 2000 µm/100 µm.

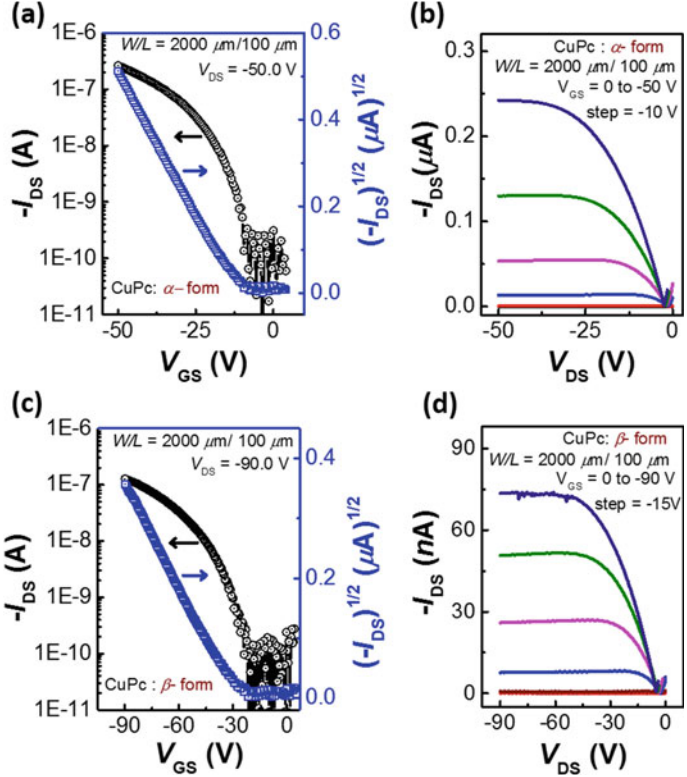

Fig. 2 **a** Transfer and **b** output characteristics of a particular α-form CuPc OFET. **c** Transfer and **d** output characteristics of a representative β-form CuPc OFET. Both devices have *W/L* ratio of 2000/100 μm

In Fig. 2a, the particular α-form CuPc OFET showed μ and V_{TH} values of 3.7 $\times$ 10^{-3} cm^2V^{-1} s^{-1} and -12.1 V, respectively. These devices showed an excellent saturation behavior in output characteristics (Fig. 2b) with an average mobility of 4.7($\pm$1.0) $\times$ 10^{-3} cm^2V^{-1} s^{-1} obtained from 29 such OFETs. From the transfer characteristics shown in Fig. 2c, the particular β-form CuPc device exhibited μ and V_{TH} values of 0.8 $\times$ 10^{-3} cm^2V^{-1} s^{-1} and -30.1 V, respectively. An average mobility of 0.9($\pm$0.2) $\times$ 10^{-3} cm^2V^{-1} s^{-1} was obtained for these devices from 19 such OFETs (lesser than α-form). In this case also, an excellent saturation behavior was obtained in output characteristics (Fig. 2d). Table 1 summarizes the extracted electrical parameters of α- and β-form CuPc OFETs. One significant difference in transistor performance can be seen here, with a mobility of α-form five times higher than that of β-form, even at a lower operating voltage. Other OFETs parameters were also inferior in β-form compared with α-form. The relative better electrical performance of α-form-based CuPc OFETS over β-form devices may be due to the

Table 1 Summary of various OFETs electrical properties of both forms of CuPc

CuPc type	$\mu_{max} \times 10^{-3}(cm^2V^{-1} s^{-1})$	$\mu_{avg} \times 10^{-3}(cm^2V^{-1} s^{-1})$	$V_{TH,avg}(V)$	$SS_{avg}(V/dec.)$	$D_{it,avg} \times 10^{12}(cm^{-2} eV^{-1})$
α-form	6.9	4.7 ± 1.0	-14.1 ± 1.7	5.2 ± 1.3	2.7 ± 0.7
β-form	1.3	0.9 ± 0.2	-31.6 ± 3.5	10.9 ± 1.8	5.5 ± 1.0

thinner active semiconductor layer. Moreover, the material characterization of α- and β-form of CuPc was also performed to investigate the physical origin.

3.2 Material Properties

Figure 3 represents the Raman spectra and XRD characterization of the powder samples of α- and β-form CuPc.

Raman spectra of powder samples of α- and β-form CuPc are shown in Fig. 3a, b, respectively. Both forms of CuPc show a Raman peak at wavenumber (WN) values nearly around 1521, 1448, 1336, 1142, 1035, 952, 832, 747, 679, and 595 cm^{-1}. Raman peaks present at WN values of 1336, 1448, and 1521 cm^{-1}correspond to

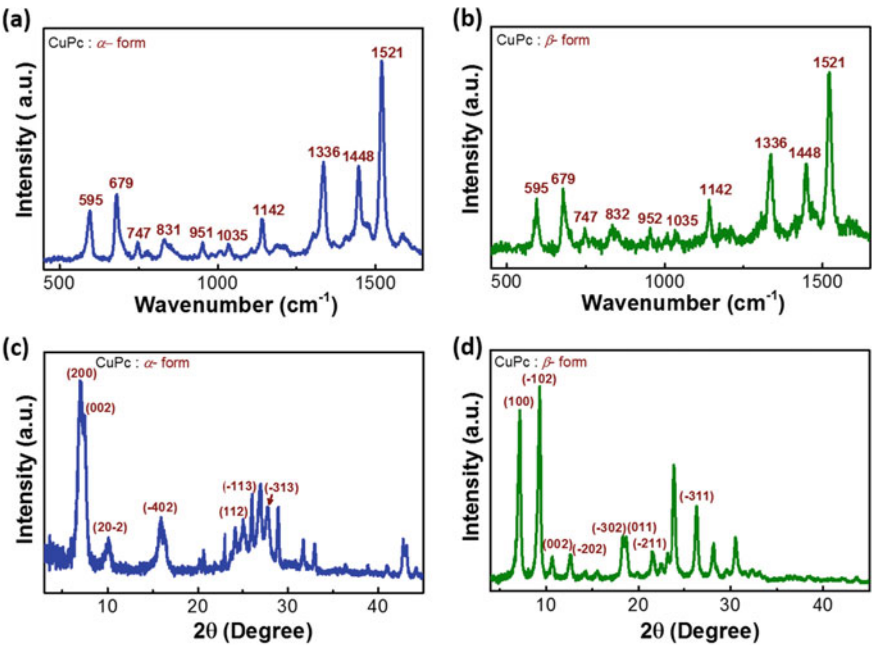

Fig. 3 Raman spectra of powder samples of **a** α-form and **b** β-form of CuPc. XRD characterization of powder samples of **c** α-form and **d** β-form of CuPc

pyrrole stretching, isoindole ring stretching, and displacement of C–N–C bridge bond related to central copper metal ion of phthalocyanine molecule, whereas Raman peaks present at WN values of 595, 679, 832, and 1035 correspond to A_{1g} of benzene ring deformation, B_{1g} macrocycle breathing, C–N stretching, and C–H bending, respectively [11]. For the Raman peaks corresponding to the WN values of 747, 832, 951, and 1035 cm^{-1}, β-form CuPc exhibits diffused Raman peaks compared with α-form CuPc. Diffused Raman peaks in β-form compared to α-form represent the variation in crystallinity of CuPc for different forms. Figure 3c and d represents the XRD results of powder samples of α- and β-form of CuPc at 2θ values from 4º to 45º, respectively. α-form of CuPc showed major significant peaks at 2θ values of 7.01º and 7.51º representing the crystalline plane of < 200 > and < 002 >, respectively [12], whereas β-form of CuPc showed peaks at 7.21º and 9.31º representing the crystalline plane of < 100 > and < −102 >, respectively [13, 14], showing the differences in crystalline behavior in different forms of CuPc. However, powder samples of both forms of CuPc exhibited nearly identical (~95%) degree of crystallinity. Figure 4 represents the UV–Vis spectroscopy characteristics of the deposited α- and β-form CuPc thin films.

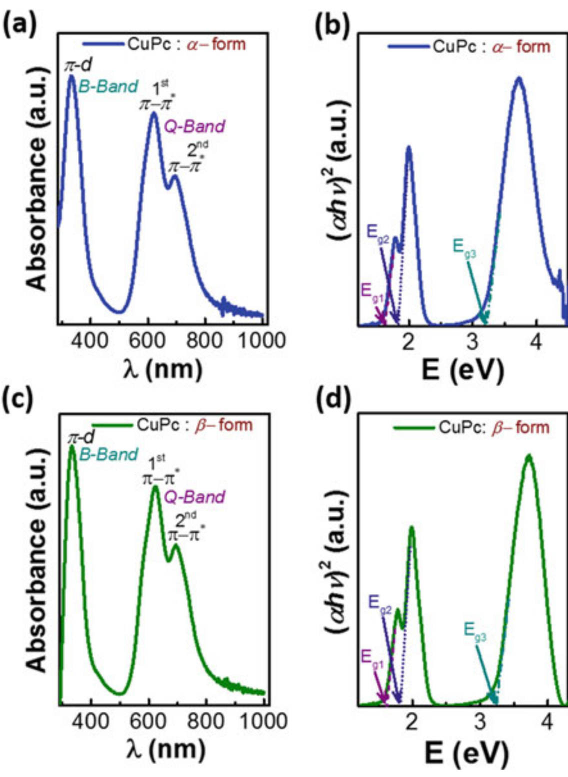

Fig. 4 **a** UV–Vis absorption spectra and **b** $(\alpha h\nu)^2$ versus energy plot for α-form CuPc. **c** UV–Vis absorption spectra and **d** $(\alpha h\nu)^2$ versus energy for β-form CuPc

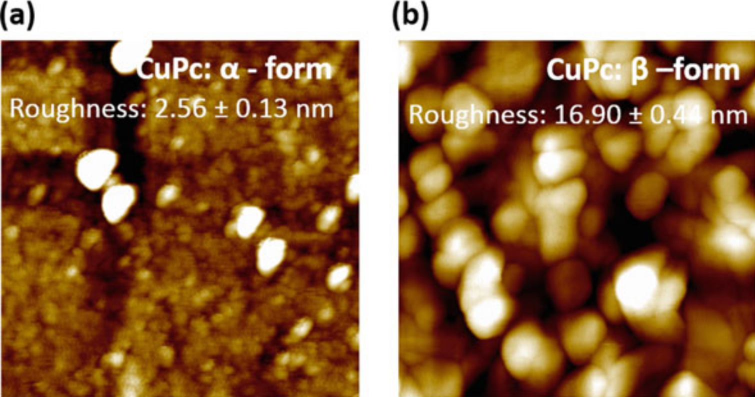

Fig. 5 AFM characterization of **(a)** α-form and **(b)** β-form of the deposited CuPc thin film

UV–Vis absorption spectra and $(\alpha h\nu)^2$ versus energy (eV) plots for α and β-form of CuPc are given in Fig. 4a, b–c, d, respectively. Both forms of CuPc showed nearly identical UV–Vis characteristics. UV–Vis peaks in Q-band are raised due to π–π* excitation between bonding and antibonding orbitals, whereas a peak in B-band is raised due to π–d transition [15]. In Q-band, absorption peaks at 621 nm and 696 nm represent the first π–π* transition and second π–π* transition, respectively. Similar absorption peaks in Q-band in UV–Vis spectroscopy represent the deposition of α-phase of CuPc in thin films at room temperature [5] using both α-form and β-form of CuPc. Figure 4b and d shows that both forms of CuPc are having nearly identical band gap values of $E_{g1} = 1.6$ eV and $E_{g2} = 1.8$ eV due to the first and second π–π* interaction, respectively, in Q-band and $E_{g3} = 3.2$ eV in B-band due to π–d transition. Thus, both forms of CuPc have an identical optical band gap value of 1.6 eV, representing identical charge transfer mechanism in both forms. Figure 5 represents the 1×1 µm AFM images of the deposited α- and β-form CuPc thin films.

The obtained average surface roughness of the deposited α-form CuPc (2.56 ± 0.13 nm) thin film was found to be lower than that of β-form CuPc (16.90 ± 0.44 nm), which in turn deteriorates corresponding device performance in β-form CuPc OFETs compared with α-form CuPc devices.

4 Conclusion

OFETs were fabricated with α- and β-form of CuPc. α-form CuPc OFETs exhibited superior electrical performance over β-form. The relatively better performance of α-form CuPc OFETs can be attributed due to the thinner active semiconductor layer compared with β-form devices. Moreover, material characterizations were done using UV–Vis spectroscopy, Raman spectroscopy, XRD, and AFM spectroscopy to

investigate the physical origin of difference in electrical characteristics. Diffused Raman peak was obtained for powder β-form CuPc; however, nearly identical degree of crystallinity of α- and β-form CuPc was indicated by XRD. UV–Vis spectroscopy reveals the deposition of α-phase of CuPc using both α- and β-form of CuPc in thin-film deposition. In AFM spectroscopy, the thin-film deposition using α-form of CuPc exhibited lower surface roughness compared with β-form of CuPc. Thus, the relatively better electrical performance in α-form CuPc OFETs over β-form devices was attributed due to the thinner active semiconductor and the better film uniformity.

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