Research on a Low-Latency Communication Module for the Reactor Protection System

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Abstract. The response time of shutdown of a nuclear reactor is an important parameter of reactor protection systems in nuclear power plants. Furthermore, as a part of a reactor protection system, the point to point communications system mostly influence the response time of shutdown of a nuclear reactor. A new solution to optimizing the response time is introduced, where a point to point communication system is implemented by FPGA technologies. The new designed system could extremely improve the efficiency of communications, which contributes to shortening the response time of shutdown. This paper delivers not only analysis of the response time of shutdown in current systems, but also the design scheme of the FPGA-based system. In addition, the communication system based on FPGA optimizing the response time of shutdown of a nuclear reactor is proved which is applied in reactor protect systems of VVER.

Keywords: Point to point communication · Reactor Protect System · Nuclear plant

1 Introduction

The Reactor Protection System (RPS), a component of the safety Instrument and Control (I&C) system, is recognized as the most important safety assurance system for nuclear power plants. When its operating parameters reach the nuclear safety protection threshold, the reactor should be shut down in an emergency to void nuclear safety accidents. Since the handling of the shutdown response involves the safety of personnel, equipment, and the environment in nuclear power plants, the response time of shutdown of a nuclear reactor is required strictly [1].

The response time of shutdown of a nuclear reactor is recommended in both Standard Review Plan for the Review of Safety Analysis Reports for Nuclear Power Plants (NUREG-0800) published by the U.S. Nuclear Regulatory Commission (NRC) and Computer-based Software Important to Safety in Nuclear Power Plants (HAD102/16) published by Ministry of Ecology and Environment of China, which should usually be less than 0.2 s [2, 3]. In this case, how to reduce response time shutdown of a nuclear reactor is an important factor that should be considered in the design of a safety I&C system.

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In RPS, the response time of showdown a nuclear reactor refers to the time required from the signal collected by the sensor to the output signal of the RPS made by the showdown circuit devices, which means the signal travels through Analog Output (AI), I/O bus processing, point-to-point network communication, main processor central processing unit (CPU) calculation, Digital Output (DO). Most institutions and manufacturers reduce the response time by optimizing the selection of AI and DO modules, I/O bus ports, and CPU application algorithms [4]. However, there are few studies on improving the efficiency of network communication to optimize the response time.

In this research, a FPGA-based low-latency communication module is proposed, which greatly improves the processing efficiency of multi-channel, large data capacity point-to-point communication, in order to optimise the response time. The architecture of the RPS and the calculation method of the response time are firstly introduced, followed by analysing the factors affecting the response time. Furthermore, the point-to-point communication is optimised by FPGA-based system which is verified by experiment contributing to optimising the response time of of showdown a nuclear reactor and applied in VVER further.

2 Response Time of Showdown a Nuclear Reactor

2.1 Architecture of Reactor Protection System

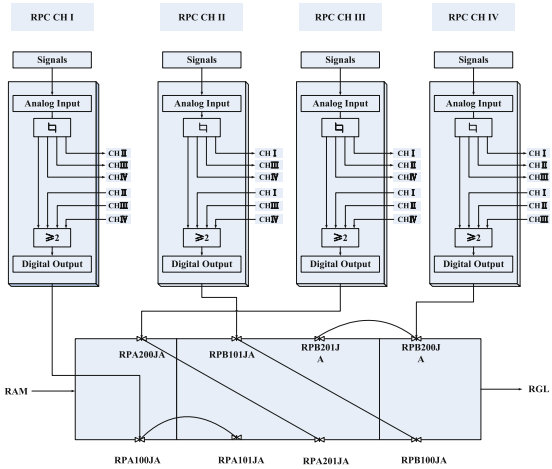

Fig. 1. Illustration of a typical RPS

A typical digital reactor protection system is shown in Fig. 1, which is designed with four redundancy channels. In this case, every channel works independently of other channels. The working condition signal of the reactor is collected through the analog input board, followed by the signal input into the CPU processing unit to participate in the voting logic processing of this channel after threshold comparison. The result of

threshold comparison is transmitted to other channels via point to point communication to participate in the voting logic processing of other channels. The judgment result of the receiving threshold of each protection channel is output to the coil of the circuit breaker of the channel through the 2oo4 voting logic [5].

2.2 Signal Process of RPS

The trip signal flow of the emergency shutdown in RPS is shown in Fig. 2. Sensor signals are collected by analog input board (AI) and sent to CPU for processing, followed by the result output by the local CPU transmitting to the remoted CPU by point to point communication module achieved by the communication module [6]. After that, the data processed by remoted CPU is sent to digital output board (DO), followed the digital signal output by DO.

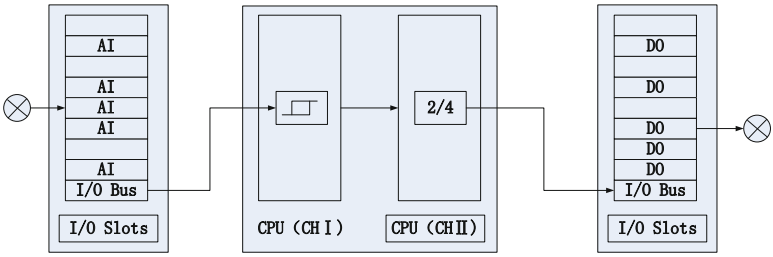

Fig. 2. Diagram of trip signal flow of the RPS

a) **Calculation of the Response Time**

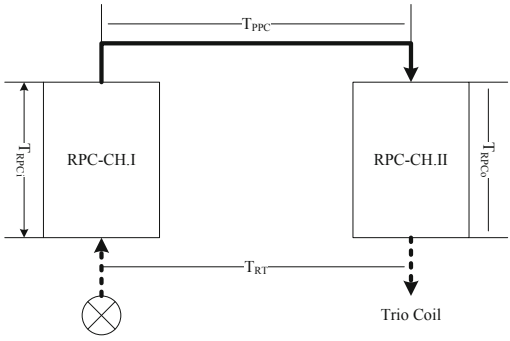

Fig. 3. Calculation of response time of shutdown of a nuclear reactor

As illustrated above, three factors should be considered for the calculation of the response time of shutdown of a nuclear reactor, shown in Fig. 3, which are the input

time of the RPS (T_{RPCi}), the communication time of point to point communication (T_{PPC}), and the output time of RPS (T_{RPCo}). The equation is listed as below.

$$T_{RT} = T_{\mathrm{RPCi}} + T_{\mathrm{PPC}} + T_{\mathrm{RPCo}} \tag{1}$$

b) **Analysis of the Response Time of the FirmSys**

In the FirmSys, the input time and output time of the RPS, mainly related to external devices such as conditioning device, relay and coil, is difficult to optimise. In this case, the point to point is firstly considered to improve the response time in the system, and is also mainly stated in this paper.

The FirmSys, the first DCS with safety class 1E produced by China with proprietary intellectual property, is taken as an example to describe how the response time to be calculated. In the FirmSys, the point to point communication is achieved by Main Process Units (MPU) and Network Communication Units (NCU), which is shown in Fig. 4. In this case, the calculation equation of the response time could be update as below where the process time of MPU and NCU and transmission time of the network are considered.

$$T_{RT} = T_{\mathrm{RPCi}} + 1.7T_{\mathrm{MPU1}} + 2T_{\mathrm{NCU1}} + T_{\mathrm{Trans}} + 1.7T_{\mathrm{MPU2}} + 2T_{\mathrm{NCU2}} + T_{\mathrm{RPCo}} \tag{2}$$

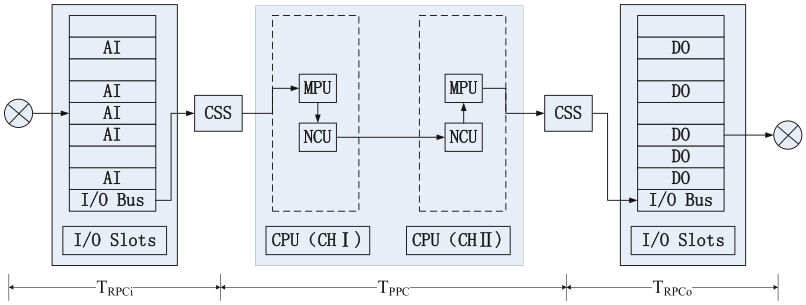

Fig. 4. Calculation of response time of shutdown of a nuclear reactor

In specific project where FirmSys is applied, the operating cycle of MPU, NCU are set to 15 ms, 8 ms respectively. In general cases, the cycle of T_{RPCi} and T_{RPCo} to 32 and the RTSNR could be calculated, which is,

$$\begin{aligned} T_{RT} &= T_{\mathrm{RPCi}} + 1.7T_{\mathrm{MPU1}} + 2T_{\mathrm{NCU1}} + T_{\mathrm{Trans}} + 1.7T_{\mathrm{MPU2}} + 2T_{\mathrm{NCU2}} + T_{\mathrm{RPCo}} \\ &= 32 + 1.7 \times 15 + 2 \times 8 + 1.7 \times 15 + 2 \times 8 + 32 = 149(ms) \end{aligned} \tag{3}$$

c) **Requirement of Optimising the Response Time of the FirmSys**

It can be seen from the above calculation that the cycle of MPU and HNU greatly affects the response time of Shutdown of a Nuclear Reactor. With the increase in the scale of nuclear I&C system, especially after the application of the Russian VVER

reactor, the number of data processed by MPU has greatly increased, which lead to the rising embedded-based MPU. Due to the increase of the MPU cycle, the response time also increases, which could lead to not meeting the requirement of the system. In this case, steps should be taken to reduce the operating cycle of the MPU or NCU, in order to improve the response time. Due to algorithm implemented in MPU, which is not suitable to be modified, the NCU is selected for redesign.

3 A FPGA-Based Low-Latency Communication Module

3.1 Analysis of Current Communication Modules (NCU)

Based on FirmSys, NCU is designed to provide the MPU to send and receive network data, which is shown in Fig. 5. When sending, the MPU places the data to be sent in the DPRAM, followed by the NCU reading the information in the DPRAM. Data validity verification is performed, and the verified data is sent to other nodes through the NCU. When receiving, the data validity check is performed, after the NCU receives the information. As check passed, the data is stored in the DPRAM, before reading by the MPU.

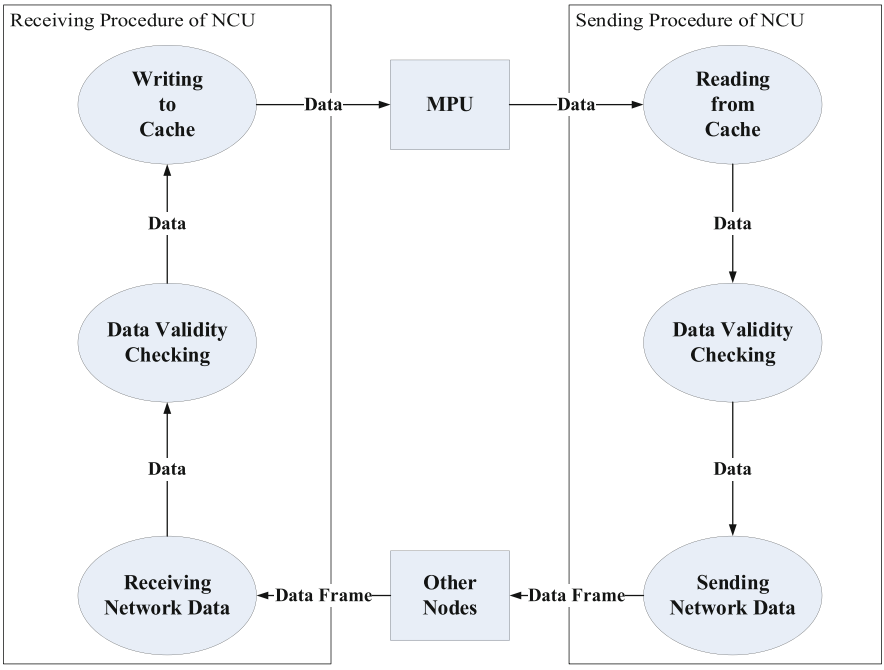

Fig. 5. Data processing of NCU

Based on the characteristics of the microprocessor, the functions of the NCU operate periodically. The tasks executed in the execution cycle of each microprocessor shown in Fig. 6 where each subtask is executed sequentially. In this case, the minimum execution period of the network communication module is the sum of the periods of each subtask that is 8 ms currently.

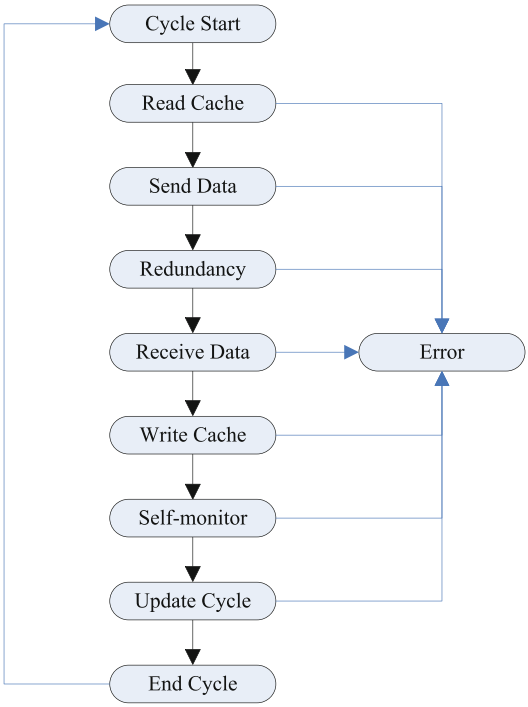

Fig. 6. Flowchart in the microprocessor-based system

Access to DPRAM is the second major factor affecting NCU based on microprocessor architecture. When the NCU receives data from other stations, it stores the data received by the NCU in the designated memory area, and check the validity of the data. After the check is passed, the data would be put in the corresponding memory, followed by data written to the DPRAM.

When performing data sending tasks, the data written to the top area of DPRAM from the MPU, followed data validity verification performed. After the verification is passed, the data would be put into the designated network sending data area. When the sending task is to be executed, the data would be sent. Due to the characteristics of the microprocessor, the verification could not be executed, when data being receive.

3.2 A FPGA-Based Low-Latency Communication Module

On the basis of the original microprocessor-based solution, the FPGA-based communication module is designed, which contributes to improvement of the processing cycle of point-to-point communication. Due to the parallel processing capability of FPGA, each subtask in Fig. 6 can be executed simultaneously in FPGA. The processing diagram of the new designed communication module based on FPGA architecture is shown in Fig. 7.

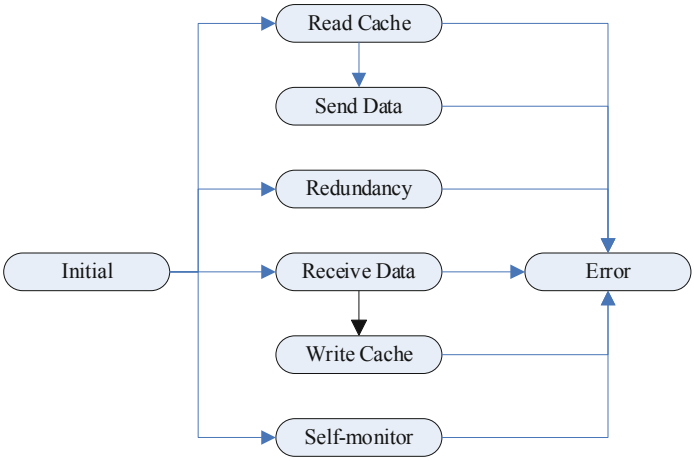

Fig. 7. Flowchart in the FPGA-based system

A FPGA-based communication module is implemented, shown in Fig. 8. When the MPU sends data to other nodes, the data is first written to DPRAM and sent to other nodes via PHY after MAC processing immediately. When receiving the data, the received data via PHY is stored in DPRAM for the MPU reading.

Due to the parallel processing mechanism of FPGA, all registers could be processed synchronously, which means all subtasks could be processed at the same time [7]. According to the characteristics of FPGA, the logic judgment of related registers could be completed within a single FPGA clock cycle. No concept of cycle exists in FPGA-based communication module and all data is updated in real time, which means the overall response time of the point to point communication depends on the operation cycle of the MPU.

The DPRAM interacted with the MPU is shown in Fig. 9. When the FPGA reads the data in the DPRAM, it also performs data buffering, data splicing, data verification, and data state analysis. When reading the data from the MPU, the data is directly obtained from DPRAM to the FPGA internal register, and the obtained data is read into the relevant status register and data validity check module at the same time. It is equivalent to completing three subtasks achieved by microprocessor-based system, which extremely increases the efficiency of the point to point commutation.

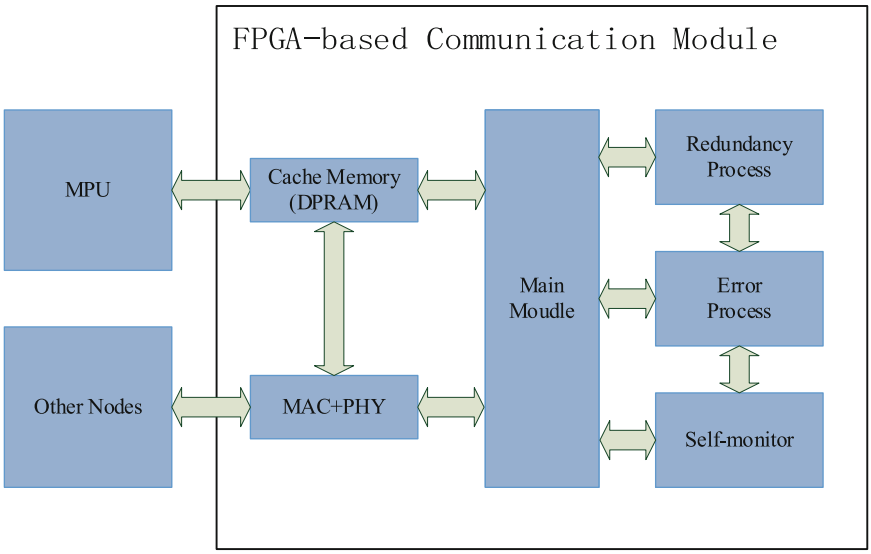

Fig. 8. Block diagram of a FPGA-based communication module

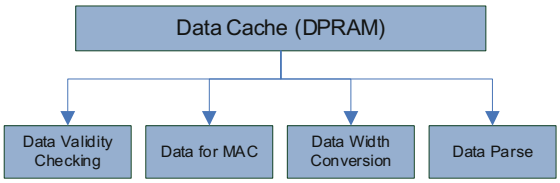

Fig. 9. Processing in parallel for accessing to memory

4 Verification and Analysis

4.1 Verification

A validation model is establish based on FirmSys, which is shown in Fig. 10. The interface of the model is no difference between microprocessor-based and FPGA-based communication module, which allows the news designed product be validated in the old system [8]. The operational condition of FPGAs and data in FPGA could be monitored by logic analyser.

4.2 Analysis of Result

For measure the cycle time of a FPGA-Based NCU, test points are applied in every state of the main FSM, which could be monitored by SignalTap, an on-chip logic analyser produced by Altera. A group of register value monitored by SignalTap is shown in Fig. 11.

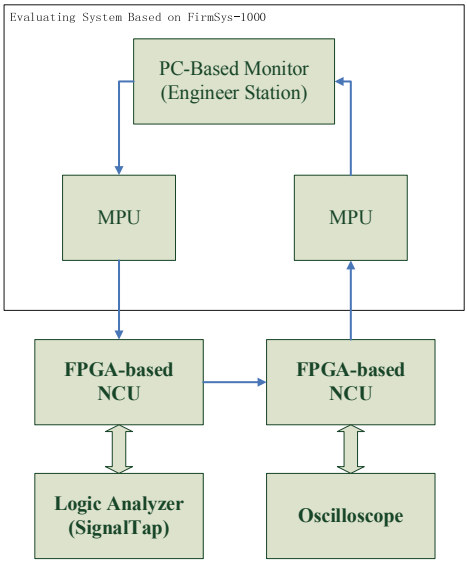

Fig. 10. Verification platform

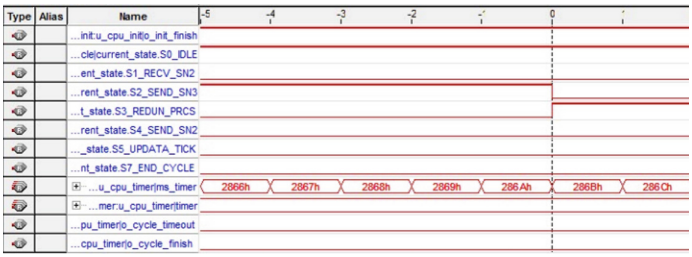

Fig. 11. Result observed from SignalTap

After 100 times repeated experiment, the time of data transmit from sender to receiver lies between 750 us and 850 us, which is shown in Fig. 12. In this case, the processing time of point to point communication achieve by FPGA-based communication module could be considered as 0.8 ms, and used for further calculation.

4.3 Analysis of the Response Time

After the FPGA-based communication module applied, the Response Time could be calculated again, which is,

$$\begin{aligned} T_{RT} &= T_{\mathrm{RPCi}} + 1.7T_{\mathrm{MPU1}} + T_{\mathrm{PPC}} + 1.7T_{\mathrm{MPU2}} + 2T_{\mathrm{NCU2}} + T_{\mathrm{RPCo}} \\ &= 32 + 1.7 \times 15 + 0.8 + 1.7 \times 15 + 32 = 117.8(ms) \end{aligned} \tag{4}$$

As a result, the response time of shutdown of the nuclear reactor by 31.2 ms based on FirmSys.

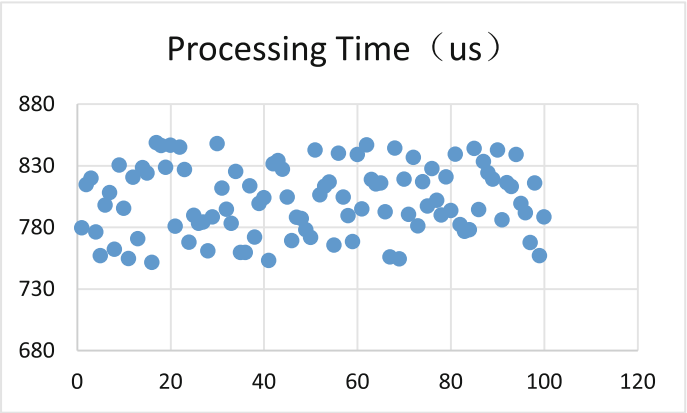

Fig. 12. Verification result

5 Conclusion

A new solution to optimizing the response time of shutdown of the nuclear reactor is introduced, where a low-latency communication module implemented by FPGA technologies in this paper. Analysis of the response time of shutdown in current systems is delivered in this paper, followed by the design scheme of FPGA-based systems. In addition, the experimental result shows that communications system based on FPGA optimizing the response time of shutdown of a nuclear reactor is proved which enhances advanced technologies applied in reactor protect systems. In the future research, the use of FGPA to achieve other equipment and functions of the safety I&C system is the research objective.

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