Physical Design and Implementation of Multibit Multilayer 3D Reversible Ripple Carry Adder Using "QCA-ES" Nanotechnique

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Abstract Quantum dot cellular automata with electro-spin ("QCA-ES") nanotechnology is an effective alternative to today's popularly used "CMOS" technique. Owing to the advancement of the proposed "QCA-ES" which is a more effective transistor-less nanotechnology, the optimization of area occupation, delay, energy dissipation and device complexity becomes easier. In this work, the "QCA-ES" nanotechnology is proposed for the design of an advanced 4-bit reversible adder, which is also known as ripple-carry-adder ("RCA"). Here, the proposed advanced adder is designed with multilayer 3D platform using multilayer inverter gate. A comparative study among the different other methods of full-adder design is shown in the paper, which shows that the delay, cell complexity and area occupation of multibit advanced full-adder structure can be minimized more by forming a multilayer 3D reversible "RCA" design, where multilayer inverter gates are used. Further, a comparative study is also presented between the proposed advanced multibit multilayer "RCA" design and other advanced multibit adder designs using the selected "QCA-ES" technology by varying the quantum cell size (18–16 nm). A brief discussion of high-temperature tolerance with proper output strength of the proposed advanced multibit multilayer "QCA-ES"-based design is also presented in this paper.

Keywords CSA · CLA · Multilayer · QCA-ES · RCA · Reversible

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1 Introduction

Arithmetic and logic unit or ALU is the key component of any processor in today's digital world and full-adder circuit is an important part of this key component, which can be used to represent the addition-result of digital numbers. "CMOS" technology is widely used to design this important component till now because this technology supports Moore's law [1–3] to optimize device area and delay with time. But, the increment of device number in a single chip with time creates trouble to properly maintain the device size and speed with the proper fault-free operation. When the component size is scaled down, it increases the design complexity as well as power consumption and dissipation. So, a low-power, high-speed, less-complex, nano-sized and effective replacement of the above technology is required to design the components of ALU in this modern era. This paper chooses an advanced "QCA-ES" nanotechnology to design a multibit advanced full-adder circuit ("RCA") using a novel reversible logic in multilayer 3D platform.

In this work, a novel full-adder structure is designed at first, where a three-input majority gate with only four quantum cells are used and then this design is compared with the other previously published designs of 2019–2020 to represent the advancement of our proposed structure to optimize the occupied area, cell complexity and delay. After proving the betterment of the proposed "QCA-ES"-based full-adder design, it is compared with the previously published full-adder designs, and this paper focuses on the optimization of the occupied area, power, delay, complexity and cost of the proposed multibit adder design by using reversible gate in multilayer 3D platform. Modified "3:3 TSG Gate" is applied over here to avoid the energy dissipation per single bit and to compensate for the high-temperature effect due to layer number increment by using adiabatic logic [4].

The rest of the paper is presented as follows. After introducing the main focus, the proposed component, technology, logic of this presented paper, and the background of the proposed technology with proposed logic are discussed in the Sect. 2. After that, the Sect. 3 of this paper presents the literature review of the proposed circuitry and the Sect. 4 shows the presented work of this paper. Section 5 shows the simulated outcomes with required comparisons and proper discussion. After all the above stages, a brief conclusion about this proposed paperwork is presented with proper future-scope discussion in the sixth section.

2 Theoretical View of the Proposed Technique and Logical Expression

2.1 "QCA-ES" Cell Configuration, Gate Structure and Clocking Scheme

The proposed "QCA-ES" nanotechnology is mainly utilized to configure the physical-level structural design of any digital component in this nanotechnical era, and these components become an effective replacement of "CMOS"-based components in this recent nanoelectronic era, which is already discussed in the introduction section of this paper. This proposed advanced technology "QCA-ES" is a four-quantum dot-based technology, where the quantum cells are placed one after another to form a quantum wire and the information flow from input to output can be possible by the interaction of neighboring quantum cells. The discussed four-quantum dots are placed in each quantum cell, where two diagonally placed dots are occupied by the electron. When the electrons become excited they start to move through the tunnel in a spintronic direction and this electron-spin concept helps to move information from one cell to another cell. The polarization of quantum cells is another important factor of this technology, which depends on the above concept. When electrons start to move in the clockwise direction it shows positive polarization, meaning binary "1", and when the movement is in the anti-clockwise direction, the cell polarization becomes negative, meaning the cells act as binary "0".

Figure 1a, b represent the binary 0 and binary 1 cell design (Fig. 1 is "90°" cell design and Fig. 2 is "45°" cell design), where the two electrons are placed in
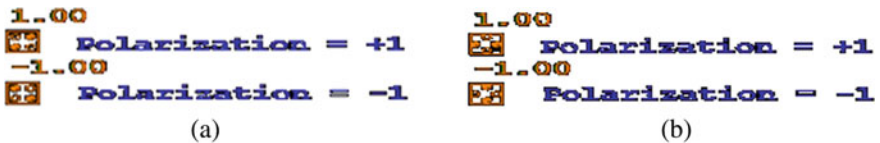

Fig. 1 **a** The "90°" binary 0 cell design and binary 1 cell design in QCA. **b** The "45°" binary 0 cell design and binary 1 cell design in QCA
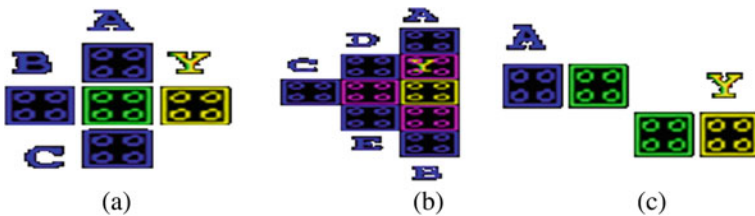

Fig. 2 **a** Three-input majority gate by using quantum dot cells. **b** Five-input majority gate by using quantum dot cells. **c** A basic inverter gate structure of QCA technology

two separate diagonal positions due to the electrostatic repulsion between the same charged carriers (electrons).

In this portion, some important gates in QCA electro-spin technique are properly discussed which are rapidly used to form any binary expression in the digital field. "90°" quantum cells are used in these presented gate designs due to less energy consumption [5] and higher output amplitude level compared to "45°" rotated quantum cells. Three-input majority gate, five-input majority gate and inverter gate are some of the most effective and rapidly used logic gates in this selected advanced nanotechnique. The input polarity of three-input majority gate is the same as the output polarity. Let a, b and c are the three inputs of this above gate structure, then the output looks like Eq. (1). This gate also can be used to design "AND" gate and "OR" gate by changing the polarity (−1 and +1) of one of the used three inputs in three-input majority gate, which are also given in Eqs. (2) and (3), respectively. The three-input majority gate is presented in Fig. 2a. In the introduction part, it is clearly revealed that this proposed technology is more advanced than the "CMOS" technology. If in this part, the "CMOS" designs of these above gates are compared with "QCA-ES" design, then it can be said that the number of used cells is less than the number of used transistors to form all those above gate structures, such as more than 25 transistors are required to design a three-input majority gate (MG) and six transistors are required to design each "AND" gate and "OR" gate.

$$M (A, B, C) = AB + BC + CA \tag{1}$$

$$M (A, B, 1) = AB + B.1 + A.1 = A + B \tag{2}$$

$$M (A, B, 0) = AB + B.0 + A.0 = A.B \tag{3}$$

The five-input majority gate with the proper truth table is also represented in this part in Fig. 2b and Table 1. As it is known that for any binary representation the "NOT" gate plays an important component role, it can be easily designed in QCA technology as an inverter gate. Fig. 2c presents an inverter gate in single-layer form, but when it is converted into multilayer form the number of used cells is 50% reduced with high output strength. This acts as another advantage of the proposed technology to form low-sized and low-power digital logic gates.

Table 1 Truth table of the five-input majority voter gate

Sum of (A, B, C, D, E)	Majority of (A, B, C, D, E)
0	0
1	0
2	0
3	1
4	1
5	1

Fig. 3 "QCA-ES" clocking scheme
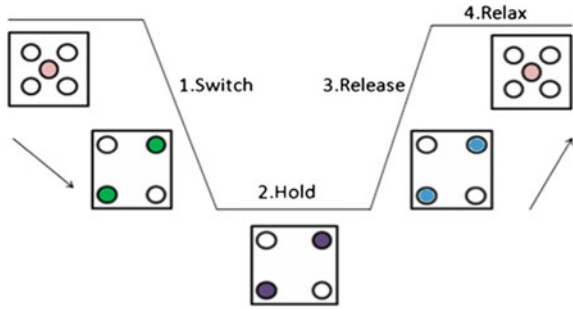
The "QCA-ES" technology-based design can be performed in two ways by clocking phenomenon, such as zone clocking and continuous clocking. In zone clocking the change of the clock zone in a quantum path is required to change the potential barrier between the quantum dots to get the propagation delay of output [4, 6]. Thus, the change in the clock zones needs to be controlled, because the rapid change in clock zones means a continuous change of barrier potential, which can increase the power consumption and power dissipation also. An advanced clocking scheme, named "Bennett Clocking Scheme" is already introduced [7], where the information can be saved before erase, which reduced the amount of dissipated power per bit without compromising the delay reduction of the proposed design.

If we discuss the basics of the clock zones, then it is important to discuss the fort clock phases of each clock zone. The four clock phases are switch, hold, release and relax, which are clearly shown in Fig. 3. In the switch phase, the cells are switched to work. Then the hold phase helps to flow the information by electron localization in the quantum dots based on the polarization of neighbor cells. In the release phase, the relocation of electrons takes place and complete relocation is possible in the relax phase. The phase difference between the two clock phases is 90°.

2.2 Basics of Reversible Gate and Used Multilayer Structure

Previously discussed "Bennet Clocking Scheme" is mainly used in reversible logic, which follows adiabaticity to maintain the extra heat generation with layer increment. This reversible logic gate is used in this work to design an arithmetic unit and logic unit combination (an important part of the core component, named "Arithmetic and Logic Unit" or "ALU", of any digital processor). In a conventional gate only input-based outputs are achieved, but in the reversible gate (presented in Fig. 4) inputs can also be represented by outputs and vice versa [8]. It can reduce the area, delay and complexity of the design. Briefly, it can be said that the advancement of selected "QCA-ES"-based design can be explored by applying reversible logic [9–12].

In our proposed structure an advanced wire crossing is used to achieve power-efficient, high-dense and high-speed circuit easily and this is multilayer wire crossing,

Fig. 4 Block diagram of reversible gate
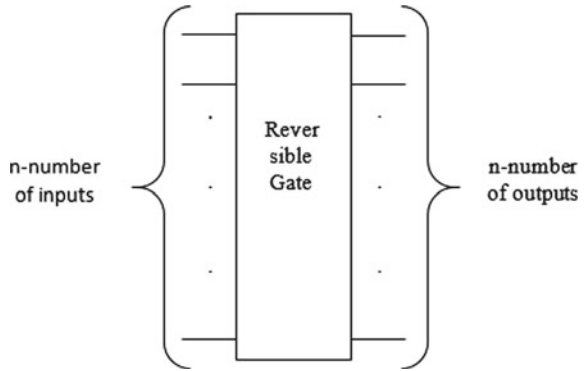
which can form a 3D design by specifying different cells in different layers. A connecter layer between two different layers is also required in this type of design.

The multilayer structural improvement of quantum cell automata technique with electron-spin phenomenon is utilized in this paper, where a three-dimensional structure (presented in this paper in Fig. 5) can be formed from a two-dimensional structure for a unit area and delay reduction, and multilayer 3D inverter gates are used to form the proposed components with 16 nm quantum cell. Another advantage of this multilayer structure is an increase in the output strength. When a single-layer structure needs a huge number of quantum cells, at the same time, the design complexity is also maximized. But, it can be reduced by using this multiyear crossover technique [13].

Fig. 5 " 3D" structure using multiple layers in QCA design
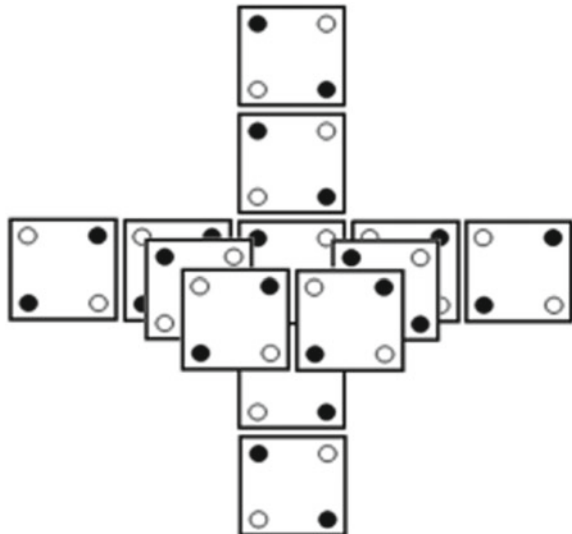
3   Literature Review

A QCA-based novel full-adder structure is designed in this paper before the "RCA" formation. This proposed adder design is used to form a 4-bit "RCA" in this work, which is discussed in the next section. In this section, some recently published QCA-based full-adder designs are shown one after another, which helps to make a comparison between the published works and our proposed work. In 2019, Fahimeh Danedaran et al. designed a fault-tolerant full-adder with 0.02 μm^2 area, 0.5 clock phases, 32 quantum cell complexity and 0.07305 eV dissipated energy for 1 E_k using five-input majority gate [14]. In this year also, a reversible full-adder subtractor design is formed by Moein Sarvaghad Moghaddam [15] with 58 quantum cells, 2 clock zones and 0.04 μm^2 to add another subtraction operation with reversibility. Next year, Nuriddin Safoev et al. designed a QCA-based 8-bit full-adder subtractor circuitry using a novel structure of coplanar full-adder with 49 quantum cells, 0.04 μm^2 area and 4 clock phases delay [16]. An incrementer/decrementer design is also formed this year by using the full-adder structure with 56 cells and the output strength calculation is also given in that paper [17].

Marshal Raj et al. presented a novel adder design where the clock pulse, area and cell number are increased, but this design presents an extra operation (subtraction) with adder operation [18]. A novel "Arithmetic and logic Unit" using QCA technology is designed in 2020 by Seyed-Sajad Ahmadpour, and as we know the full-adder is an important component in "Arithmetic and logic unit". This paper [5] presented a novel fault-tolerant design of full-adder circuitry by QCA. But in that, if a fault-tolerant full-adder design is used, the number of cells increased and the area is also increased, which creates a limitation of that presented circuitry. The above limitations of that previously published paper are already reduced in the same year by Behrooz Parhami et al. [19], where new majority-voter gate-based QCA-full-adder with 55 cells, 0.037 μm^2 area and 0.75 clock-cycle delay is used to form different types of 8-bit carry generator. Another novel full-adder structure is presented in the same year by M.M Abutaleb, where 38 quantum cells are used with 0.03 μm^2 area and 0.75 clock-cycle delay to form and compare two different types of "RCA" circuitry [20]. The used cell complexity of full-adder design is reduced (4 cells are decreased) in a published paper of Nuriddin Safoev et al., with less delay and the same area is compared with the previous one, by making the proposed component's formation in multilayer QCA platform [21]. The cell-reduction technique of QCA-based full-adder design is continued by Subhanjan Subhasis Das et al., where the delay is the same as the previously discussed paper but the area is reduced down to 0.02 μm^2. This paper also calculates the energy dissipation, which is 2.39e^{-003} eV for 1 E_K [22].

The 13 number of cells to design a QCA-based full-adder circuit is designed with the same clock phase delay in a published work of Jeyalakshmi Maharaj et al. [23], which is utilized to design a multibit "RCA" circuit. The discussed designs are compared with our proposed circuit which is presented in the next part of this paper through a parametric comparison table. There are various types of advanced multibit

full-adder designs already discussed in the paper [24], such as ripple-carry-adder or "RCA", carry-save-adder or "CSA" and carry-look-ahead-adder "CLA". The various types of "QCA-ES"-based designs of these above-advanced adder circuits are presented in previously published papers. In this research work, the parameters of some previously published multibit advance adder designs are summarized, which helps to make a clear comparison of different types of proposed advanced adder designs of different papers with our presented reversible multibit design. In [25], V. Pudi et al.'s advance multilayer 4-bit adder design took 698 quantum cells with $0.618\,\mu m^2$ area occupation, 4 clock-cycle delay and 9.888 quantum cost, which were reduced by a multilayer 4-bit "CSA" design of paper [13] written by D. De and J. C. Das, where cell complexity, area occupation, delay and quantum cost were 525, $0.55\,\mu m^2$, 2.5 clock-cycle and 3.44, respectively. Then Sarvarbek Erniyazov et al. presented a paper [26] where the advancement of quantum cell-based 4-bit "CSA" over the fastest advanced 4-bit adder "CLA" using quantum cell was discussed after reducing the quantum cell size. The advancement of the presented "CSA" was discussed in the above paper, where the occupied area, complexity, delay and cost reduction can be possible compared to the proposed "CLA" design in a single-layer platform. But, an advanced adder design compared to the above published "CSA" design is presented in this work, where the previously discussed parameters of proposed circuitry are optimized more by using reversible logic in a multilayer 3D "QCA-ES" platform with comparatively small cell size and proper output strength.

4 Proposed Design

As we know, a novel reversible "QCA-ES"-based "RCA" design is ultimately presented in this paper in multilayer platform, but 1-bit full-adder structure is also represented in this part of this paper, where a clear parametric comparison with other previously published (discussed in the previous part of this paper) QCA-based full-adder circuit is represented in this portion through Table 2. This proposed full-adder structure is shown in Fig. 6.

Table 2 proves the advancement of our "QCA-ES"-based full-adder compared with other discussed designs. This structure is mainly utilized to form the reversible multilayer 4-bit "RCA", which is discussed below (see Table 3).

A novel seventh-layer reversible 4-bit "RCA" design using quantum cells are presented in Fig. 7, where the used full-adder designs with extra "XOR" operations are shown in layers 1, 3, 5 and 7, and layers 2, 4 and 6 present the communication line between every two layers. In Fig. 7, a new four-cell three-input majority gate [5, 23] with multilayer inverter gates is used by specifying one layer above another layer to reduce the unit area and delay, and the reversible logic reduces power dissipation of the proposed multilayer 3D design. "3:3 TSG Gate" is used over here as a reversible gate where three inputs are used (let A, B and C) and the three outputs are (1) direct output of input A, (2) "XOR" of A, B and C and (3) "XOR" of A and B. The truth table of the used reversible gate is also presented in the following sections.

Table 2 Parametric comparison among different adder designs

Referred papers	Cell complexity	Occupied area (μm^2)	Latency (ps)
[5]	32	0.02	0.5
[27]	58	0.04	0.5
[16]	49	0.04	1
[17]	56	0.047	1
[18]	75	0.09	0.75
[2]	85	0.082	2
[19]	55	0.037	0.75
[20]	38	0.03	0.75
[21]	34	0.03	0.5
[22]	32	0.02	0.5
[28]	26	0.02	0.5
[29]	16	0.006	0.5
[15]	13	0.009	2
Proposed (18 nm)	12	0.008	0.5
Proposed (16 nm)	12	0.006	0.4
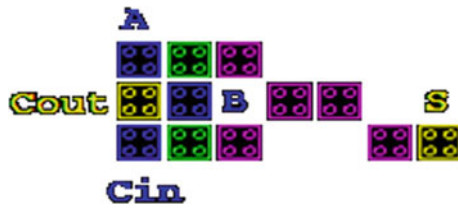
Fig. 6 Physical-level design of the proposed 1-bit full-adder design

Table 3 Truth table of "3:3 TSG Gate"

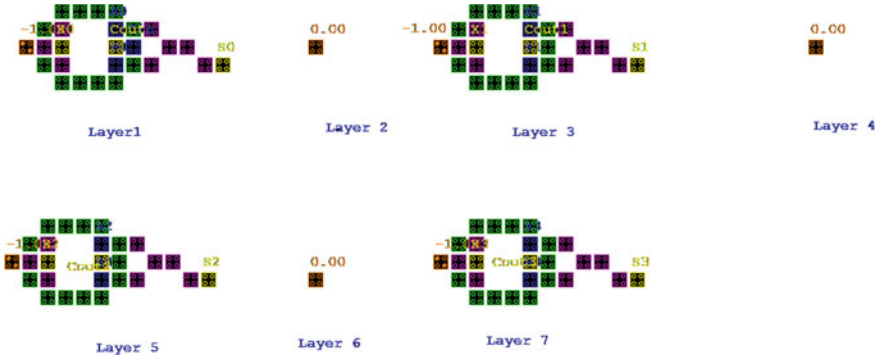| Input			Output		
A	B	C	A'	P = A XOR B XOR C	Y = A XOR B
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	0	0	1
1	0	0	1	1	1
1	0	1	1	0	1
1	1	0	1	0	0
1	1	1	1	1	0

Fig. 7 Physical-level design of reversible multilayer 4-bit "RCA"

5 Simulated Outputs and Discussion

In this portion, the direct output of reversible full-adder structure is given, where the previously discussed proposed 1-bit full-adder circuit is used. After the design-simulation, the used "Full-Adder" design to form the proposed reversible multibit multilayer "RCA" is simulated in advanced "QCA-ES" platform and the simulated result is presented below in Fig. 8 separately. These "Full-Adder" designs are used in this work to form the proposed structure of 16 nm quantum cell-based multilayer 3D 4-bit reversible "RCA" design and the simulated output of this proposed circuitry is presented in this paper in Fig. 9.

In the above outcomes, A0 to A3 and B0 to B3 are the inputs of 4-bit "RCA" and the carry-out of the previous "Full-Adder" acts as the carry-input of next "Full-Adder". S0 to S3 are the sum-output of the proposed design and output X0 to X3 are
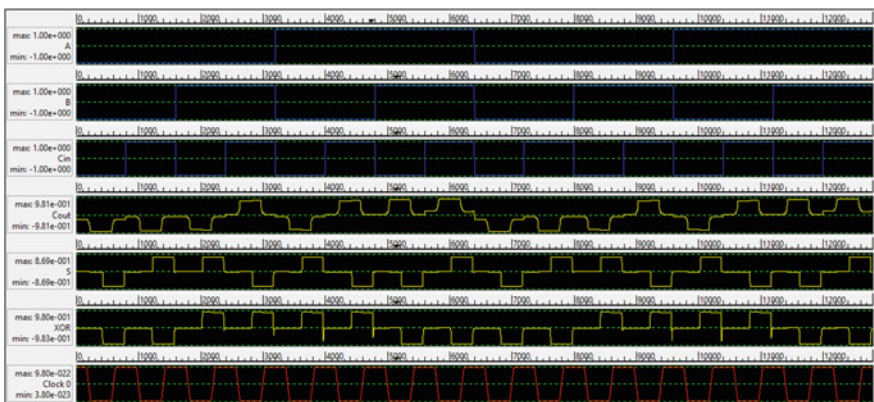

Fig. 8 QCA output of reversible "full-adder" design with "XOR" operation
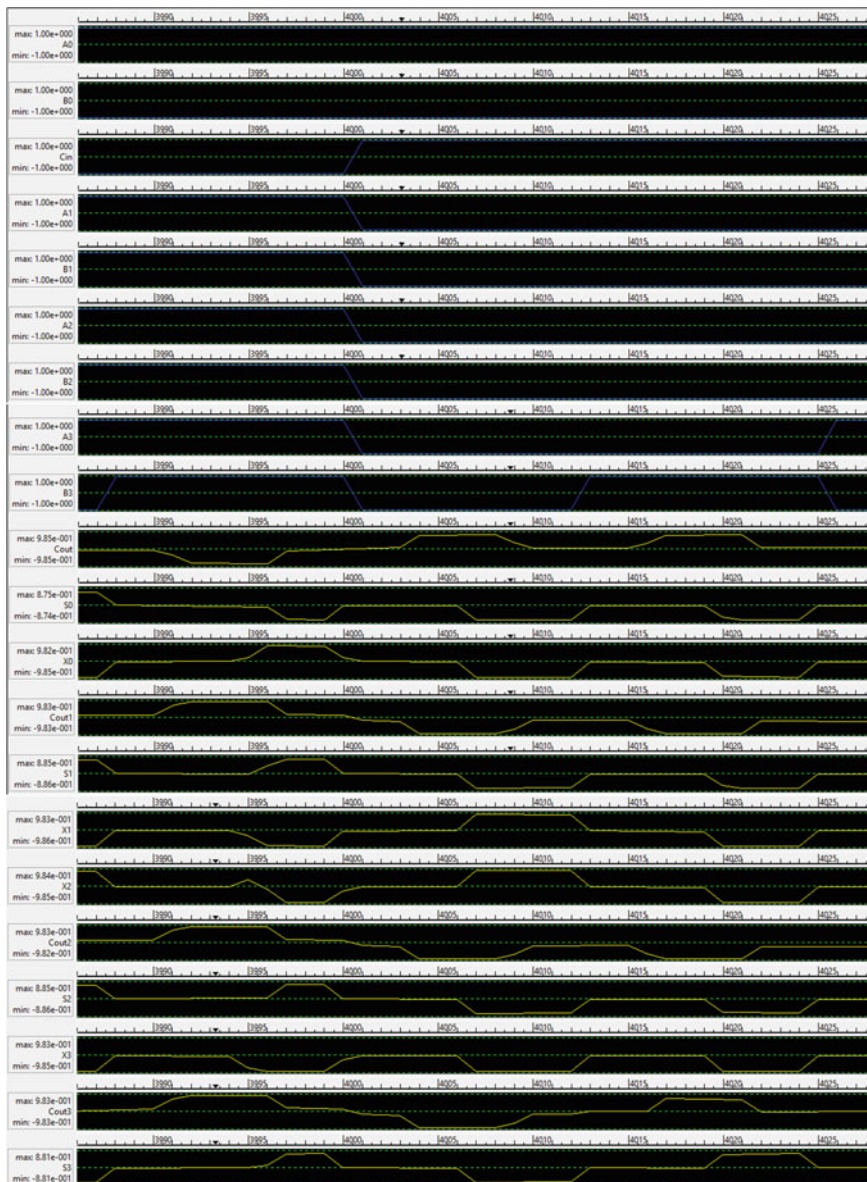
Fig. 9 Output of four-bit reversible multilayer "RCA" design with "XOR" operation

the "XOR" outputs which are another logical expression of the proposed reversible 4-bit "RCA".

This proposed more advanced nanotechnology than "CMOS" is used in this work in multilayer 3D platform with reversible logic, which is discussed previously and this proposed multilayer "RCA" design is better than the "QCA-ES"-based "CLA" and "CSA" configuration, published in the previous year [26]. The proposed design of our paper can reduce the area occupation, area utilization factor (AUF) [27] (ratio of area occupation of the proposed design and area occupied by used quantum cells), delay, complexity and cost with proper output strength (9.3 at 3 K temperature, which is graphically presented in Fig. 10) and low power dissipation. Another comparison table, Table 4, is presented to show the advancement of multilayer 3D reversible "RCA" compared to previously published "QCA-ES"-based "CSA" and "CLA" structure.

Basically, if the advancement of adder-circuitry based on the given parameters in this paper is discussed, then it can be said that "CSA" is the fastest advanced adder among other advanced adder structures, which are formed in a single-layer platform. But, Table 4 clearly shows that in a multilayer 3D platform with the help of a selected reversible gate the proposed "RCA" circuitry can optimize the required area, delay,
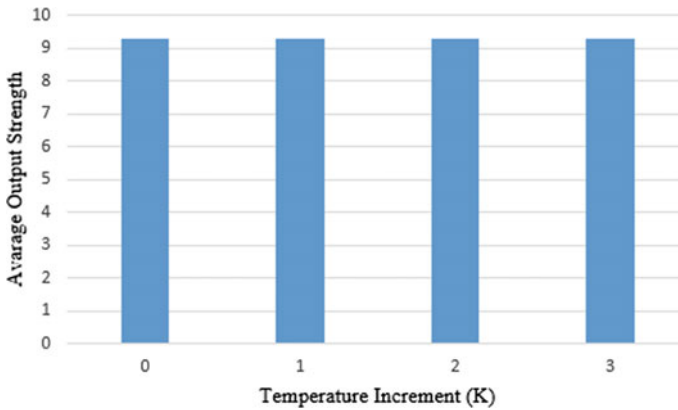

Fig. 10 Graphical representation of average output strength changes versus temperature increment

Table 4 Comparison between "QCA-ES"-based "CLA", "CSA" and reversible "RCA" design with different layer types [26]

Adder type	Area occupation (μm^2)	AUF	Complexity	Delay (ps)	Layer type	Quantum cost (area × latency^2)
"CLA"	0.92	11.5	777	2.75	Multilayer	6.95
"CSA"	0.66	9.42	696	2.25	Coplanar	3.34
Reversible "RCA"	0.03	1.5	111	1.75	Multilayer	0.091

AUF, complexity and cost of the design more than previously published single-layer "CSA" circuitry.

The output strength is reduced at the time of cell diameter reduction due to the electron-scattering problem, but the multilayer design can reduce this problem by reducing the chance of quantum wire crossing. Thus, multilayer design can maintain the output strength of "QCA-ES"-based digital designs at the time of cell diameter reduction. Owing to the above discussion, our proposed design can also give proper output with better output strength (up to 9.94) at the time of layer separation gap reduction up to 5 nm.

6 Conclusion

A low-power, cost-effective, nano-sized, less complex, high-speed and temperature-tolerant advanced multibit-adder design is the primary objective of this work. The proposed design leads to a better arithmetic component of ALU compared to the current CMOS transistor-based components, since the CMOS technology suffers from scalability problems and high interlapping complexities at the time of inte-grated circuit formation. Extending our previous work [25], further optimization of "CSA" and "CLA" has been achieved in this work by using QCA-ES technology in addition to multilayer reversible "RCA" formation. In our previous work [25], the advancement of "CSA" compared to "CLA" has been proved, and in this work, it is shown that the use of multilayer reversible "RCA" is capable of optimizing the area occupation up to 95.4%, AUF up to 84%, complexity 84%, delay 22.22% and quantum-cost 97.3% with proper output strength. As a future scope of this work, the proposed design may be used as a combination of the arithmetic unit and the logic unit in ALU with proper fabrication and proper validity checking (checked by "FPGA Spartan 3E" board).

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