Analysing the Behaviour of 14 nm, 10 nm, 7 nm FinFET and Predicting the Superiority Among the Lot

Soumya Sen and Mandeep Singh

Abstract The advancement of technology leads to the discovering of fresh avenues. Things took to bit challenging after the regular planar MOSFET dished out various shortcomings when they were subjected to downscaling. Few issues such as velocity saturation, drain-induced barrier lowering (DIBL), surface scattering, impact ionization etc. came into the picture. These are known as the short channel effects [1]. With the introduction of FinFET in the semiconductor market, it had brought with it a lot of advantages such as a notable improvement in the switching speed to the power consumption on one side to better controlling of leakage current also with significant switching speed. Also, with more added advantages an appreciable I_{ON}/I_{OFF} ratio is maintained. FinFET had given significant control of the channel by the devices for the usage of more than one gate. As a result, the short channel effects can be controlled without shooting high the carrier concentration. For all these, the researchers have dared to scale down the devices more to a significant extent. As the size gets lower there is a much healthier performance with very high efficiency. This very paper not only digs deep into the FinFET technology but also discusses the evolution of 14 nm, 10 nm, 7 nm technology for FinFETs and their features which takes the edge over their counterpart.

Keywords FinFET · Short channel effects · 14 nm · 10 nm · 7 nm · NanoHub

1 Introduction

MOSFET or the metal-oxide semiconductor field-effect transistor is a four-terminal device having the source, gate, drain and the body as the fourth terminal. The role of the gate is like a controlling tap that controls the flow of electrons. The distance between the source and the drain is the channel. The driving force of the I_d is the V_g.

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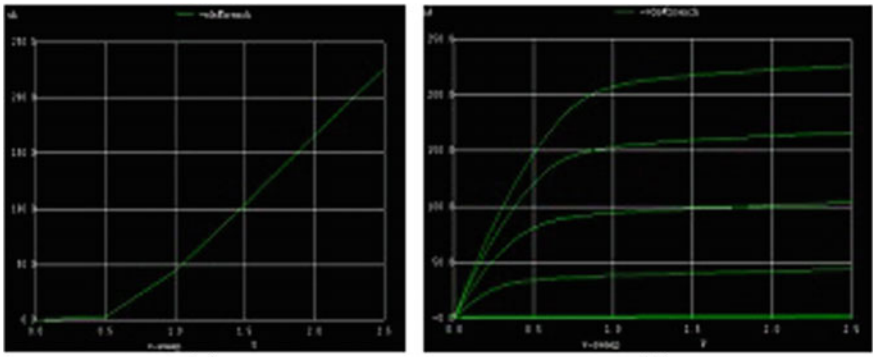
S. Dhar et al. (eds.), *Advances in Communication, Devices and Networking*,
Lecture Notes in Electrical Engineering 776,
https://doi.org/10.1007/978-981-16-2911-2_2

The lowering of the channel length leads to downscaling of the device size and the diminishing of the gate voltage. This in turn makes the control of the gate low over the channel, which in turn invites the short channel effects [1, 2]. The device in turn becomes smaller to denser and the complexity of the circuit increases. The various short channel effects lead to leakage current to high power consumption issues which in turn damages the device. So in order for better gate control, the MugFETs have come into the picture. The FinFET falls into this category; the multiple-gate of the FinFET [3, 4] has been controlled by a single electrode and can be considered as one single gate. A major catch of the dual gate of the FinFET is that as the doping concentration is made to remain constant, the I_{ON} is two times that of the planar MOSFET which in turn is much beneficial according to the electrical integrity of the devices. The devices will have much improved carrier mobility and a lowered leakage current issues. If we explore deeper into the short channel effects of the devices, which include the *drain induced barrier lowering (DIBL), velocity saturation, hot electron effects, impact ionization*, the DIBL occurs due to the increase of the potential of the drain where the increase of the drain potential leads to the lowering of the barrier. The depletion region of the drain moves into the bulk. As a result, what happens is a huge rush of current flows through the subthreshold region. The major master of the device was the gate whose responsibility has been taken down by the drain. Now, as the barrier is lowered there is a current flow which is known as *leakage current* which would be very high and cannot be controlled by the gate [1]. Therefore, the device could not be turned off. It is seen that the entire depletion region from the drain would be entirely *punched through* to the source. So, there would be no depletion region around and the drain current would not be controlled by the gate, thus concluding that the gate loses its control over the device. Like this, many more like *velocity saturation* when the electric field will have no effect on the increased velocity. Figure 1a, b shows the simulated graphs in *NgSPICE* [5] of I_d versus V_{gs} and I_d versus V_{ds}, where in the aspect ratio W/L, the L is kept minimum. The aspect ratio is kept the same as 1.5. For the smallest value of L, the current is minimum



(a) (b)

Fig. 1 **a** The Id versus Vgs of 0.25 um MOSFET; **b** Simulation results for Id versus Vds

due to velocity saturation condition in short channel device where the velocity gets saturated early before it reaches the pinch off point.

The next effect we can highlight is the *hot electron effect* where the electrons get ionized and upon entering into the oxide they increase the temperature of the oxide, hence the VT also shoots up degrading the overall performance of the device. Including all, we are having the *impact ionization effect* where one charge carrier will have sufficient energy to knock on another creating an e-h pair. With the short channel effects, the other problems which arise are the stray and parasitic capacitances and resistances. The major reason is the downscaling of the transistor. As much as the transistor sizes are shrinking down, the more the issues arise.

1.1 FinFET

The FinFET [3, 4] was designed to answer the hindrances of leakage current by wrapping the gate electrodes around the channel. Now, in the traditional transistor, we have it on the top of the channel. Here, the silicon fins act as the channel. The uncovered regions of the fins(gate) are the source and the drain. The source and the drain are surrounded by the silicon fin which has an undoped nature. This is further surrounded by an extension implant and poly oxide. There is also a high-K dielectric and metal gate. Energizing the gate electrode will lead to excellent control over the channels and the channel surrounds the gate. After the gate electrode, the region of the fin located beneath the electrode is inverted. It forms a path that will conduct between the source and the drain. FinFET is a fully depleted device and the conduction happens in the outermost edges of the fin. The double gate of the FinFET reduces the I_{OFF} (see Fig. 2).

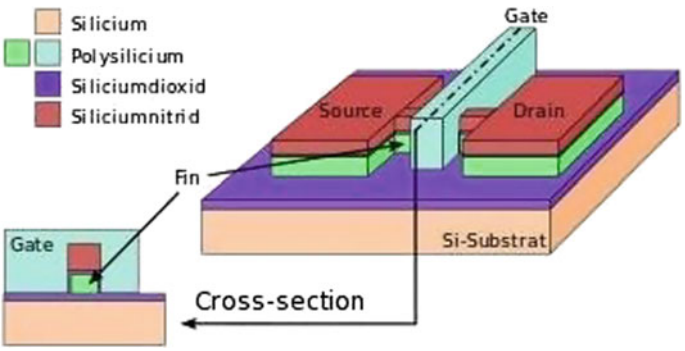


Fig. 2 FinFET device schematic [4]

1.2 FinFET Characteristics

- In order to improve the current drive, the source and the drain are raised, leading to the reduction of parasitic resistance and capacitance.
- The short channel effects are being suppressed by the development of silicon fin.
- FinFET is a type of MugFET [6]; it can achieve larger channel width by the usage of multiple fins. The number of fins is directly proportional to the increase in current.
- High performance can be achieved for symmetric gates, and asymmetric gates can also be built which focus on V_T.

The major foe of the semiconductor devices, short channel effects could be easily dealt with. FinFET is actually from the MuGFET [6] family which can be any fin-oriented multiple-gate transistors. The very law of Gordon Moore is very much satisfied when we see the fabrication technology revolution of *14 nm to 10 nm to 7 nm.* The theory of nanometres is the very story of processors which are used and the memories.

2 The FinFET Technology Nodes (14 nm, 10 nm, 7 nm)

The 14 nm was released in the year 2015, keeping in mind the battery lifetime of the cell phones. The switching speed was also high from the counterparts of SOI MOSFETs. The density of the Intel 14 nm FinFET is about 44 MTr/mm^2. Miniature the size, the cost explosion is also high. This will also be explored further as the paper explores more into the 10 nm and then to 7 nm FinFET technologies. The major usage is in the Intel's 5th to 9th generation processors. The 14 nm technology outsmarts the 12 nm as well as the 16 nm FinFET technology [7, 8].

10 nm came into the picture nearly about in the year 2017 with a density of about 99.00 MTr/mm^2 for Intel, and as for TSMC, it is about 60 MTr/mm^2. The 10 nm FinFET technology is nearly about three times denser than the 14 nm process. The major parameter under the scanner is their clock speed, and for this very reason, it is not been considered for the processor for desktops. The power reduction is nearly 60% and its 20% is faster than the TSMC's 12 nm/16 nm.

7 nm is the most highlighted technologies of modern times having a density of about 1.6 times that of 10 nm of TSMC, even a dominating power reduction over 45% over the 10 nm technology of FinFET. The density of the 7 nm process as depicted by Samsung is about 95.00 MTr/mm^2 (approx.) having an ability to present a much lightweight and slimmer version of smart phones; adding to that, there is a significant high switching speed in the 7 nm FinFET technology for the increased drive current and leakage current reduction. The thinner gate oxides lead to the requirement of lesser input voltage supply and finally lesser voltage swings. The FinFET technology outsmarts the normal planar MOSFET by their gate around approach around the

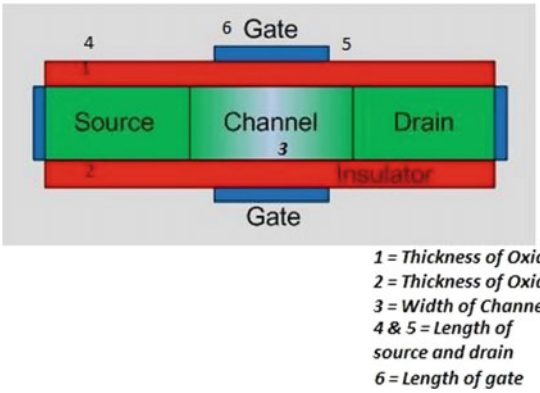


Fig. 3 Cross-section of FinFET simulated in NanoHub

channel, which in turn gives a better gate control, and as we shrink the size much more gate control is needed.

Despite all of these, we have a major challenge under the scanner, that is, the quantum tunnelling. This comes into the picture when the size shrinks and the transistors are in a fully turned on mode and cannot be turned down (see Fig. 3).

3 Results and Discussion

For the simulation purpose, we have used the *NgSPICE* as well as the *Nanohub.org* [8] in order to simulate the MOSFET as well as the FinFET in accordance to their dimension. In order to simulate the FinFETs, we have used the dimensions in accordance to Table 1. Here, the different technology nodes which are 14 nm, 10 nm and 7 nm, respectively, are shown. The default dielectric constant used in the insulator

Table 1 Parameters and technology nodes

Parameter	Technology nodes and testing conditions		
L_g	14 nm	10 nm	7 nm
L_s	8 nm	6 nm	4 nm
L_d	8 nm	6 nm	4 nm
O_s	2 nm	2 nm	2 nm
O_d	2 nm	2 nm	2 nm
W_{ch}	5 nm	4.5 nm	3.5 nm
T_{ox1}	1 nm	0.8 nm	0.65 nm
T_{ox2}	1 nm	0.8 nm	0.65 nm

L_g: Length of gate, L_s: Length of source, L_d: Length of drain, O_s: Gate overlap to source, O_d: Gate overlap to drain, W_{ch}: Width of channel, T_{ox1}: Thickness of oxide1, T_{ox2}: Thickness of oxide2

is 3.9, which is because of SiO_2, *silicon dioxide*. The given bias points are 3, to get the values for the DIBL, *drain-induced barrier lowering*, which will be discussed later in the paper. The thickness of the oxide or Tox is decided on the value of the dielectric constant. The gate type is used as the metal. The *MuGFET* [6] technology is used for testing conditions. The parameters are taken as such in consideration with the current technology nodes. For the simulation purpose, Geometry—X and Geometry—Y were considered, as the analysis is done on the 2-D device. The simulator used is *Padre*. The critical current for the threshold voltage is 1e−4. This is done for the logarithmic scale for the calibration of the drain current.

It is observed from Fig. 4a that the 14 nm FinFET [9] has good short channel controlling abilities. When compared with Fig. 4b and c, it can be observed clearly that the V_T is decreasing from 14 nm > 10 nm > 7 nm. The leakage current also is getting decreased. Lesser leakage current will also lead to low power consumption and high device efficiency (see Figs. 5 and 6).

As it is known that the current starts driving forward when it crosses the V_T, in the ideal case $I_D = 0$. But if we see practically, there is some current in the zone where there is a negligible gate voltage. This part is the subthreshold region, and the steeper

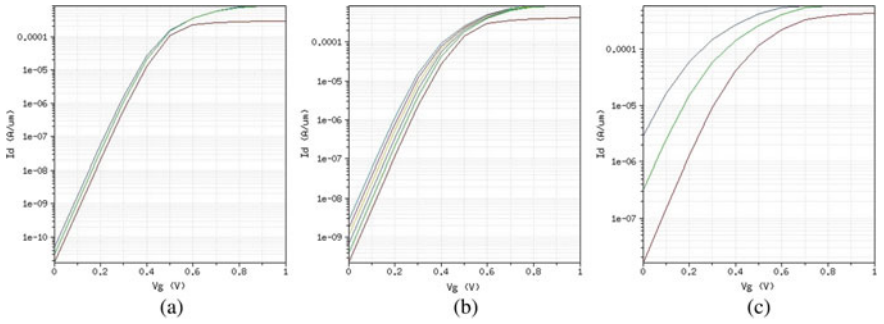


Fig. 4 **a** The log I_d versus V_{gs} of 14 nm FinFET; **b** Simulation results for log I_d versus V_{gs} of 10 nm FinFET. **c** Transfer characteristics for 7 nm FinFET

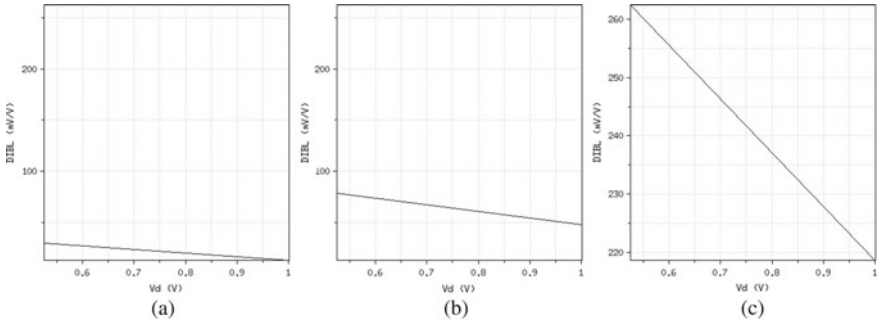


Fig. 5 **a** Drain-induced barrier lowering of 14 nm FinFET; **b** Simulation results for DIBL of 10 nm FinFET. **c** DIBL for 7 nm FinFET

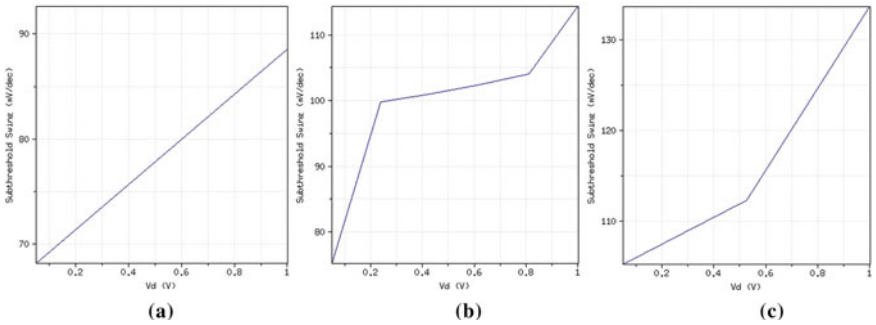


Fig. 6 **a** Simulation in nanohub.org for subthreshold swing for 14 nm FinFET; **b** Simulation results for subthreshold swing of 10 nm FinFET. **c** Subthreshold swing simulation for 7 nm FinFET

the *subthreshold swing* the lesser is the I_{OFF} and the more is the I_{ON}/I_{OFF}. The drastic decrease of the drain-induced barrier lowering can be seen clearly as the devices get shrunk down, and finally being used for cell phones or desktop processors for their longer battery lifetime and significant low V_T, to provide the same encouraging circuit designs with low power circuits.

4 Conclusion

This paper uses the 2-D models for examining the characteristics of the 14 nm, 10 nm and 7 nm technology nodes. It can be well enough concluded that though the 7 nm of Intel is under the development mode the TSMC has launched its 7 nm, and the current technology node of 7 nm is quite superior in terms of density. As examined from the overall characteristics though even after a bit of leakage current, there are abundant superior characteristics for the 7 nm FinFET technology to outsmart the others. The blessing is that the advance of research is such that the 5 nm and 3 nm technologies are not very far away from commercial use.

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