Performance Analysis of Gate-Stack Nanoscaled Recessed-S/D SOI-MOSFET for Analog Applications

Nilesh Anand Srivastava, Anjali Priya, and Ram Awadh Mishra

1 Introduction

Nowadays, semiconductor devices have become the backbone of modern communication systems with the development of low-power and high-performance integrated-circuits (ICs). Further, these ICs are advancing day by day with the continuous growth of complementary-metal–oxide–semiconductor (CMOS) technology for low power analog applications [1, 2]. Moreover, the heart of these high-density ICs is a MOSFET, as each IC is accommodated with billions of MOS-devices [3, 4]. So, this is a prime concern that the MOS-transistors should exhibit significant characteristics for successful integration with an IC. To attain high-density and high-speed ICs, the miniaturization of CMOS transistors is taking place from the past two decades [4, 5]. However, the hyper scaling tends in MOS-transistors beyond 100 nm node have deteriorated the performance of the device and results in various short-channel-effects (SCEs), such as mobility-degradation; hot-carrier-effects (HCE); gate-induced-drain-leakage (GIDL); drain-induced-barrier-lowering (DIBL); etc. [5, 6]. These detrimental changes in nanoscaled MOS-devices may lead to threshold-voltage roll-off and hence leakage in the subthreshold-regime [7].

Various suggestions have been reported in earlier researches' to overcome these unwanted effects in short-dimension MOSFETs. Like, multi-metal-gate (MMG: dual-/triple-metal) [8, 10] and multi-gate (MG: double-/triple-/gate-all-around

N. A. Srivastava (✉) · R. A. Mishra
Motilal Nehru National Institute of Technology Allahabad, Prayagraj 211004, India
e-mail: rel1702@mnnit.ac.in

R. A. Mishra
e-mail: ramishra@mnnit.ac.in

A. Priya
CASEST, School of Physics, University of Hyderabad, Hyderabad 500046, India
e-mail: anjalipriya@uohyd.ac.in

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(GAA)) [11] FETs have been suggested to enhance the gate controllability over channel. However, the gate-all-around structures suffer from various misalignment issues and have higher fabrication complexity. Further, the silicon-on-insulator (SOI) technology [12] (FinFET-SOI [13], Fully-/Partially-Depleted SOI [14–16], Junction-less-transistors [17]) has replaced bulk Si-substrates and results in very low off-state leakage with improved short-channel behavior. Similarly, different performance enhancement techniques, like, source/drain engineering [18]; high-k/low-k gate-stack (GS) [19]; hetero-dielectric (HD) [20] have also been suggested in earlier state-of-the-art to improve the device immunity in nanoscale regime.

Moreover, as per the recent reports, FD SOI MOSFETs offer significant immunity over SCEs with lesser process complexity than Fin-shaped FETs [21–23]. Also, FD SOI technology exhibits un-doped channel concept due to its thinness and follows the Moore's law altogether [24, 25]. The first theoretical potential model of FD SOI-MOSFET was proposed by Young [21]. Further, Suzuki et al. had modified with the inclusive effects of SOI-thickness [22]. Next, Cheng et al. had concluded that dynamic threshold and back-bias technique could be two alternatives to improve the analog and radiofrequency (RF) performance of nanoscaled-SOI MOSFETs [23].

Further-more to overcome the issue of DIBL significantly, the multi-metal-gate technique has been employed in FD SOI-MOSFETs [24, 25]. In which, multi-metal gates of different work-functions are arranged side-by-side to reduce the DIBL effects in a much-controlled manner. The dual work-function metal gates offer a step-like potential profile [24]. Kumar et al. had theoretically investigated FD SOI performance with dual-metal-gates (DMG) [24]. In continuation, Srivastava et al. has extensively studied the concept of separated metal-gates with dielectric modulation and source-engineering [10, 25].

However, FD SOI-MOSFETs with ultra-thin-body (UTB) may lead to the larger series-resistance due to ultra-thin regions of S/D. Moreover, Zhang et al. had suggested that this could be further overcome by the use of recessed-S/D (Re-S/D) technology [26] and Sivilicic et al. had given the theoretical justifications for the same [27]. In next, the methodology of Re-S/D technique also employed with multi-metal-based SOI-MOSFETs [28, 29]. However, technology scaling in the nanometres regime also reduces the oxide thickness, which increases the current and speed. Also, the thin oxides may lead to the carriers-tunnelling through gate-oxide and hence cause of gate-oxide leakage current. This leakage may further be reduced by using high-k oxide-material such as HfO_2 (Hafnium Dioxide) stacked with SiO_2 (silicon-dioxide) [19]. However, less attention has been made to utilize the technique of gate-stack in the design of triple-metal gate-engineered Re-S/D SOI-MOSFET.

This paper presents the performance investigation of short-channel GS-TMG: Re-S/D FD SOI MOSFET for the first time. The results assure that the concept of gate-stack can further improve the performance of triple-metal gate-engineered Re-S/D FD SOI MOSFET. This paper has been organized in the following sections. The device structure and process flow are discussed in Sect. 2, and the simulation platform and model definition has been described in Sect. 3. Next, the numerical simulation results of the proposed FD SOI MOSFET have been extensively analyzed in Sect. 4. Finally, the overall work is concluded in Sect. 5.

2 Device Design Strategies and Process Flow

The studied device structure of GS-TMG: Re-S/D FD SOI n-MOSFET is shown in Fig. 1, and the device parameters and their specifications are listed in Table 1. The device is initially designed at 45 nm technology node with three different work-function metal gates (L_{M1}: $\phi_{M1\text{-Aurum}} = 4.8$ eV; L_{M2}: $\phi_{M2\text{-Molybdenum}} = 4.6$ eV; L_{M3}: $\phi_{M3\text{-Titanium}} = 4.4$ eV) of length 15 nm each ($L_g = L_{M1} + L_{M2} + L_{M3}$). This arrangement is suitable to enhance the gate control over the channel and screen-off the changes due to higher drain-bias. Next, the high-k spacer is placed to overcome the fringing-field effects at gate edge. Also, the device is composed of high-k (HfO_2)/low-k (SiO_2) dielectric-gate-stack ($\varepsilon_{r:high\text{-}k} = 32$ and $\varepsilon_{r:low\text{-}k} = 3.9$), such that a thin layer of low-k dielectric is deposited prior to the high-k. Gate-stack engineering will help to overcome the issues of off-state and gate-oxide leakage. All other design parameters and doping levels are mentioned in Table 1.

The process flow of the device mentioned above is also feasible with less complex fabrication steps as compared to Fin-shaped FETs. The process feasibility can be discussed in the following steps. Step 1: Pattering of Silicon-wafer [10]; Step 2: Formation of UNI-BOND technique based SOI substrate [15]; Step 3: Preparation of Re-S/D junctions [18]; Step 4: Implantation of source/drain regions [15, 18]; Step 5: Stacked-oxide growth [10]; Step 6: Metal-Gates ($M_1/M_2/M_3$) deposition [18]; Step 7: Side-spacer growth/Etch/Contact Formation; Step 8: Lift-off/Device Test.

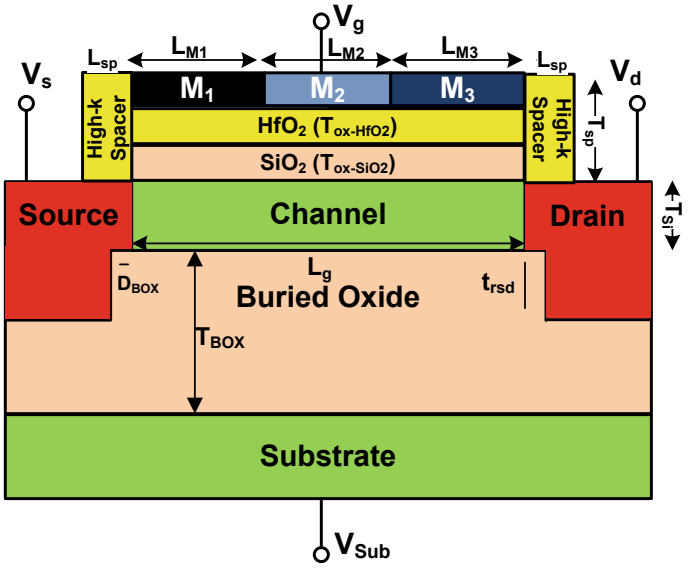

Fig. 1 Studied and simulated design of gate-stack TMG: Recessed-S/D FD SOI-MOSFET

Table 1 Device design parameters and specifications

Parameter	Symbol	Value	Unit
Channel length	L_g	45	nm
High-k oxide-thickness	$T_{ox\text{-}HfO_2}$	1	nm
Low-k oxide-thickness	$T_{ox\text{-}SiO_2}$	1	nm
High-k spacer length	L_{sp}	10	nm
High-k spacer-thickness	T_{sp}	3	nm
BOX-thickness	T_{BOX}	50	nm
Si-film thickness	T_{si}	12	nm
Re-S/D thickness	T_{rsd}	20	nm
BOX overlap Re-S/D thickness	D_{BOX}	3	nm
Metal-gates length-ratio	–	1:1:1	–
Doping (source/drain)	$N_{S/D}$	1×10^{20}	cm^{-3}
Doping (substrate)	P_{Sub}	1×10^{16}	cm^{-3}

3 Simulation Methodology

The design and simulation of studied FD SOI n-MOSFET have been performed using Silvaco-TCAD (ATLAS™) [30]. For the accurate analysis, different numerical models have been included at the simulation platform [28]. As SRH (Shockley–Read–Hall) model is taken to access the life-time of majority-carriers (generation/recombination). Next, to add the effects of mobility degradation due to temperature, Lombardi-mobility, and CVT (constant-voltage-and-temperature) models are considered. Also, the FLDMOB model (field-dependent-mobility) has been utilized to monitor the impact of transversal-field in nanoscaled-MOS design. To investigate thermal behaviour lat.temp (lattice-temperature) model has also been considered here. Further, the Gummel-Newton model and drift–diffusion are taken for the study of switching (on/off) behavior of the device. Furthermore, this is necessary to adopt the quantum-potential models at 45 nm node. So, for the analysis, QME (Quantum–Mechanical-effect) and BQP (Bohm-Quantum-Potential) models has also been taken into consideration. The analyzed simulation results are discussed in Sect. 4.

4 Performance Investigation of Gate-Stack TMG: SOI-MOSFET in Re-S/D Technology

This section represents the short-channel electrical performance of the proposed SOI-MOSFET. Figure 2 represents the drain-current versus gate-voltage (I_d vs. V_{gs}) characteristics of the proposed MOSFET and referenced state-of-the-art [28] at $T = 300$ K. It is observed that the proposed GS technique in TMG: SOI MOSFET helps to reduce off-state-leakage significantly in comparison to SOI-MOSFET [28].

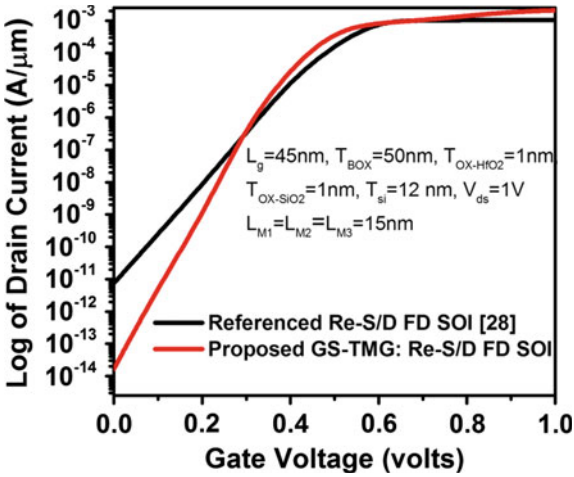

Fig. 2 The plot of drain-current (I_d) with variation in gate-voltage (V_{gs}) for proposed and reference FD SOI-MOSFET [28]

The suggested and referenced FD SOI offers off-state (I_{off}) of 0.169 fA and 7.5 pA and on-current (I_{on}) of 2.13 mA and 1.12 mA, respectively. This corresponds to the higher switching performance ($I_{on}/I_{off} = 10^{11}$) in the case of proposed GS: TMG SOI MOSFET than the referenced device ($I_{on}/I_{off} = 10^{9}$) at $L_g = 45$ nm. This is due to the reduced off-state gate tunneling in gate-stack FD SOI-MOSFET.

Also, the metal-gate-engineering will offer step-like potential-profile, which helps to increase the control of gate over the channel and the considerable reduction in drain-electric-field penetrations at higher V_{DS}, i.e., lesser DIBL effect. Similarly, the output drain characteristic (I_d vs. V_{ds}) of the devices is shown in Fig. 3. It is inferred from the plot that the proposed MOSFET results in improved current behavior than reference FD SOI MOSFET [28]. Also, the variation of subthreshold-slope (SS) at different BOX oxide thickness and $L = 45$ nm is shown in Fig. 4. It is found

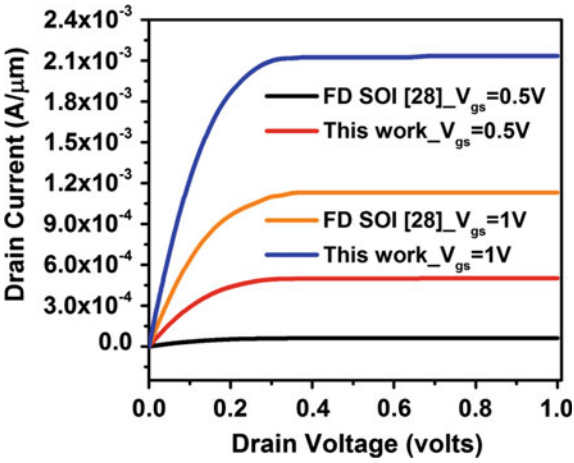

Fig. 3 The plot of drain-current (I_d) with variation drain voltage (V_{ds}) at different V_{gs} for proposed and reference FD SOI-MOSFET [28]

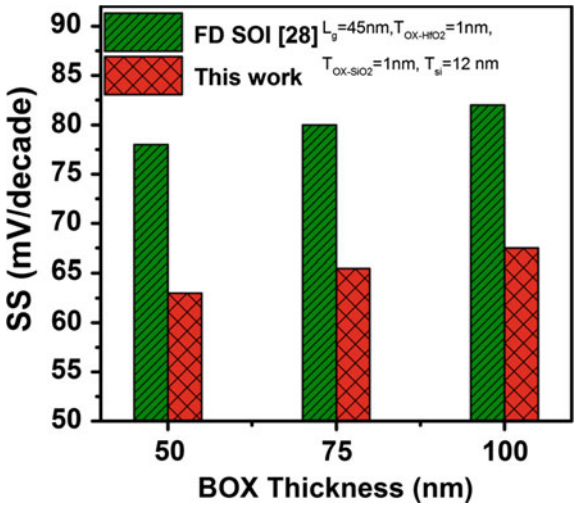

Fig. 4 The plot of subthreshold-slope at different BOX thickness (50–100 nm) at $L = 45$ nm for proposed and reference FD SOI-MOSFET [28]

that the proposed device offers a lesser value of subthreshold-slope as compared to referenced device [28]. This is due to the lesser off-state leakage in case of proposed FD SOI as compare to referenced device.

Next, the DIBL effect due to change in T_{BOX} (50–100 nm) and channel-length (30–60 nm) is monitored on the basis of TCAD-simulations for the proposed device. The result of TCAD simulation for the analysis of DIBL with variation in drain bias from $V_{ds} = 0.5$ V to $V_{ds} = 1$ V is drawn in Fig. 5. A noticeable reduction is seen, as the proposed MOSFET exhibits very less value of DIBL even at $L_g = 30$ nm. This

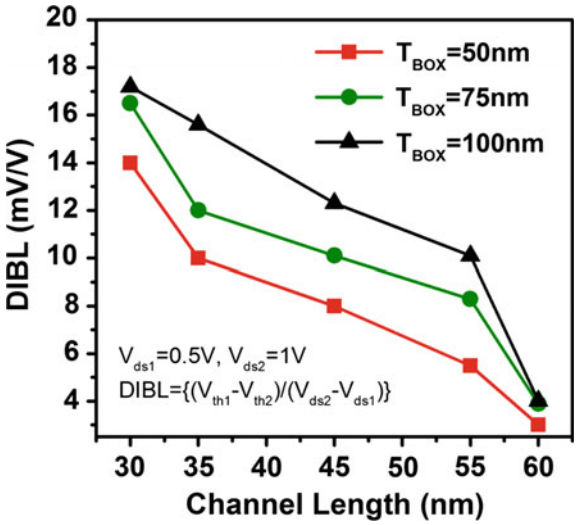

Fig. 5 The plot of DIBL at different channel length for proposed SOI-MOSFET

performance is due to the suggested technique of high-k stack in Re-S/D; gate/spacer engineered nanoscaled SOI-MOSFET.

4.1 Impact of Temperature on Gate-Stack TMG: SOI-MOSFET in Re-S/D Technology

This section discusses the impact of temperature variation on DC and analog behaviour of studied nanoscaled gate-stack SOI-MOSFET. Here, firstly the effect of change in operating temperature on drain-current performance is taken under study. Figure 6 shows the I_d versus V_{gs} plot of the studied device with change in device temperature over the range 200–400 K. It is clear from the analysis that the off-current and on-current both take a shift when the operating temperature increases. The increment in I_{off} at higher temperature is due to the effect of thermal generation/ionization and reduction in I_{on} may be due to the scattering phenomenon [23]. However, these changes are minimal in the case of the studied device, and the resulting current behavior is acceptable even at $T = 400$ K.

Next, the exact analysis of I_{off} with variation in device temperature and T_{BOX} is shown in Fig. 7. The device represents better off-state behavior and optimum drain current even at 400 K. Similarly, the calculated switching ratio (I_{on}/I_{off}) ratio at different operating temperature dictates that I_{on}/I_{off} ratio of the device has been reduced from 10^{12} to 10^{9} with the increase in temperature from 200 to 400 K. So, the analysis itself explains that the MOSFET could be further analyzed for low-power circuit applications.

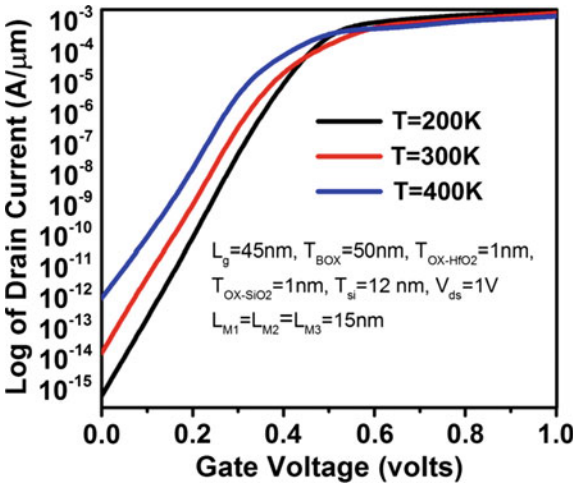

Fig. 6 Impact of temperature on drain current (I_d vs. V_{gs} characteristics) for the proposed SOI-MOSFET at $T =$ 200–400 K and $L_g = 45$ nm

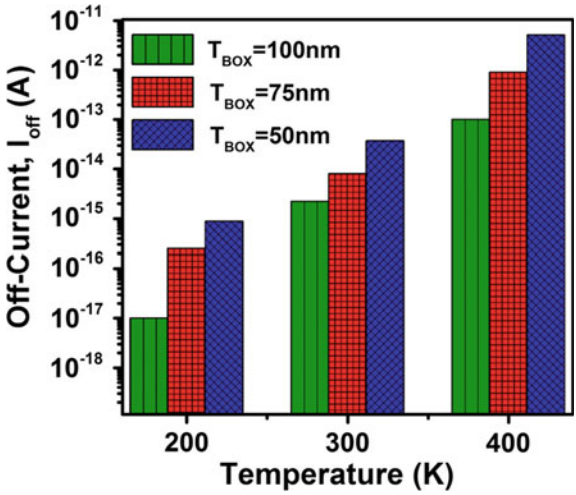

Fig. 7 Impact of temperature on sub-threshold leakage-current (I_{off}) for the proposed SOI-MOSFET with variation in T_{BOX} = 50–100 nm at $L_g = 45$ nm

4.2 Impact of Temperature on Analog Performance

The analog performance study of proposed nanoscaled SOI-MOSFET at different temperatures is discussed here. Here, TCAD simulations have been performed for the analysis of transconductance, $g_m = \partial I_d/\partial V_{gs}$, output-conductance, $g_d = \partial I_d/\partial V_{ds}$, and transconductance-efficiency-factor, TEF $= g_m/I_d$. Figure 8 represents the analysis of transconductance versus gate voltage with variation in temperature from 200 to 400 K at $L_g = 45$ nm. One can observe from the plot that the device exhibits better transconductance behavior. As, the device offers transconductance of 4.07 mS at $T = 300$ K and approximately increases (decreases) by 11% (21%) at $T = 200$ K (400 K). So, the device will offer higher gain even at $T = 400$ K.

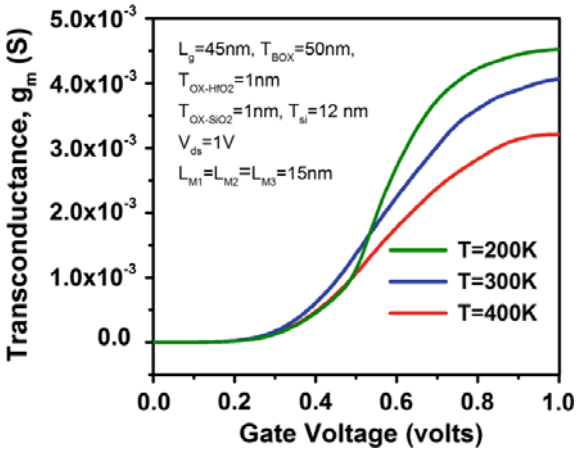

Fig. 8 Temperature-dependent transconductance analysis of studied SOI-MOSFET with variation in V_{gs} at T = 200–400 K and $L_g = 45$ nm

Similarly, the plot of *TEF* versus V_{gs} is drawn in Fig. 9. *TEF* value represents the effectiveness of drain-current and transconductance with the thermal behavior of device-to-circuit co-designs. The ratio of transconductance and drain-current defines TEF. Also, the value of *TEF* must be lower in the strong-inversion regime and higher in weak-inversion. A similar trend is seen in the case of the proposed device. Moreover, less deterioration is recorded when temperature varied from 200 to 400 K. So, the device can also be suggested for high-gain analog applications in highly linear and thermal stable mode. In continuation, the analysis of output conductance versus V_{ds} at $T = 200$–400 K and $L_g = 45$ nm is drawn in Fig. 10. In order to achieve the higher gain in analog ICs, g_d must be as low as possible. One can find from the plot that as the drain-voltage is applied, g_d starts decreasing after $V_{ds} = 0.2$ V, 0.24 V

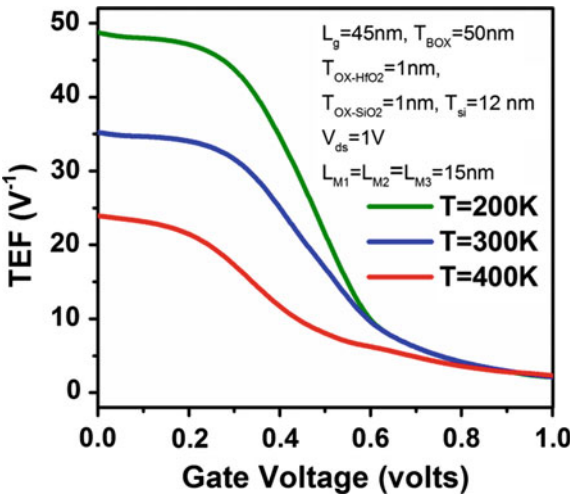

Fig. 9 Temperature-dependent analysis of transconductance-efficiency-factor (TEF) with variation in V_{gs} at $T = 200$–400 K and $L_g = 45$ nm

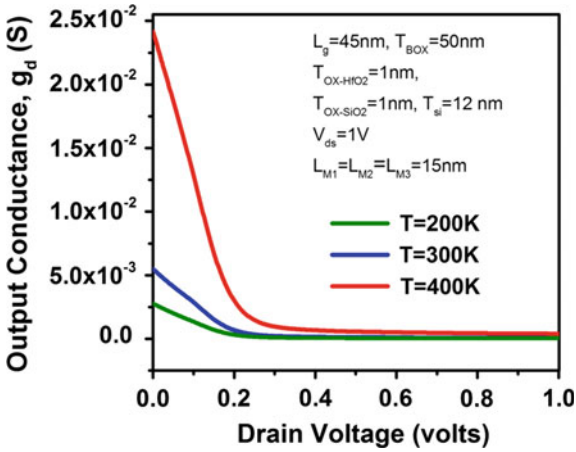

Fig. 10 Impact of temperature on output conductance with variation in V_{ds} at $T = 200$–400 K and $L_g = 45$ nm

Table 2 Performance parameters of GS-TMG: Re-S/D FD SOI FDSOI MOSFET at $L = 45$ nm, $T_{BOX} = 50$ nm and $T =$ 200–400 K

Parameters	Temperature		
	$T = 200$ K	$T = 300$ K	$T = 400$ K
I_{off} (A)	6.67×10^{-16}	1.69×10^{-14}	1.05×10^{-12}
I_{on} (A)	2.33×10^{-3}	2.13×10^{-3}	1.7×10^{-3}
Switching ratio (I_{on}/I_{off})	3.49×10^{12}	1.26×10^{11}	1.61×10^{9}
DIBL (mV/V)	8.2	8.9	15.5
g_m (mS)	4.53	4.07	3.21
TEF (V^{-1})	48.74	35.21	23.95
g_d (mS)	0.004	0.007	0.041

and 0.28 V at $T = 200$ K, 300 K and 400 K respectively. Moreover, the increase in g_d is considerable even at $T = 400$ K.

The overall analysis of the aforementioned SOI-MOSFET with variation in temperature is listed in Table 2. It is worth to mention that the high-k oxide-stack multi-metal-gate engineering technique is advantageous in recessed-S/D technology-based SOI-MOSFETs. Hence, this analysis itself dictates the device applicability in low-power thermally-stable analog-circuit and systems.

5 Conclusion

This paper investigates the impact of high-k gate-stack and metal-gate engineering on the performance of recessed-S/D technology-based FD SOI-MOSFET. The studied device exhibits enhanced short-channel immunity with improved temperature sensitivity at $L_g = 45$ nm. As the device offers $I_{off} = 0.169$ fA (1.05 pA) and $I_{on} = 2.13$ mA (1.7 mA) at $T = 300$ K (400 K) and $L = 45$ nm. This results in I_{on}/I_{off}-ratio of 10^{11} (10^{10}) at $T = 300$ K (400 K), which is significant to off-flow the subthreshold-leakage in nanoscaled-MOS devices. Next, the higher value of transconductance enables the device application in high gain analog amplifiers. Similarly, the device signifies the better *TEF* value of 35.21 V^{-1} at $T = 300$ K and decreases (increases) at $T = 400$ K (200 K) in weak-inversion regime. The resulting value of *TEF* dictates the device applicability in highly-linear ICs with improved thermal stability. Further, the device also offers the lower value of output-conductance at $T = 300$ K and $L = 45$ nm, which is desired for higher intrinsic-gain. So, the studied MOS-device could be suggested as an alternative for low- power analog circuits in the near future.

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