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Amit Dhawan
Vijay Shanker Tripathi
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Kshirasagar Naik *Editors*

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Contents

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Design and Comparison of Low-Power, High-Speed T Flip Flop, and 4-Bit Asynchronous Counter Using Various Design Techniques

Sunny Mavani and Anuja Askhedkar

1 Introduction

Nowadays, the use of portable devices is rapidly increasing which forces us to use a battery which is a limited power source. Although battery technology is improving very slowly in comparison with the microelectronics technology, the demand for the design of logic circuits which consumes less power and better performance is increasing. Power, area, and delay are the key parameters to measure the quality of VLSI circuits. But there is always a trade-off among these parameters. The design of sequential circuits has two basic parts: flip flops and some combinational logic. This flip flop allows us to store a 1-bit data, so it is used as a memory cell, which can be designed using combinational logic gates like NOR, NAND, AND, OR, XOR, NOT, CMOS latches, feedback, and transmission gates [1].

In industries, CMOS is the most widely used technology in logic design. CMOS has two different families: (1) Static and (2) Dynamic logic. From these two, static is the commonly used, and it has two networks (1) NMOS network known as pull-down network, and (2) PMOS network known as pull-up network. But the disadvantages of static logic are that a greater number of transistors are required, so delay and area increase. To overcome these disadvantages of CMOS, one of the methods introduced is PTL (pass transistor logic). The benefits of PTL are (1) low-power consumption due to a smaller number of transistors and (2) less delay due to lower area. There are also some problems with PTL, firstly it supplies the output voltage which is less than the input voltage level V_{dd}, and secondly, the reduced voltage level at input leads to a situation where the PMOS device is not completely turned off and due to this static power dissipation might be critical. There are various PTL based

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methods are proposed to overcome these problems like double-pass transistor logic (DPL), complementary pass transistor logic (CPL), and transmission gate (TG). Transmission gate is one of the finest implementations of the PTL, and it overcomes the issue of output voltage level swing degradation by using NMOS and PMOS parallel to each other [2]. In recent trends, gate diffusion input (GDI) is used to design logic circuits with low-power, high-speed, and less transistor count.

One of the flip flops that are designed in this paper is T flip flop (TFF). TFF is the primary sequential logic circuit used in designing binary counters, frequency dividers, shift registers, demultiplexers, and 2-bit parallel load registers [3]. In this paper, schematic and layout design of master–slave TFF is implemented using three different technologies CMOS, GDI, and TGB. And using these implemented T flip flop, 4-bit asynchronous counter is also designed. The counter is implemented for all the above technologies, and results are compared in terms of power, area, delay, and PDP.

The paper is organized as follows: a brief GDI introduction is illustrated in Sect. 2. Implementation of master–slave T flip flop, its simulation waveform, and layout design are shown in Sect. 3. Implementation of the 4-bit asynchronous counter and its simulation waveforms are shown in Sect. 4. The different technologies are compared in terms of power, delay, area, and PDP, and the results are discussed in Sect. 5. In the last Sect. 6, whole work is concluded.

2 Gate Diffusion Input Logic

In Fig. 1, the basic GDI cell is presented. The GDI cell looks like to the CMOS inverter, but functionality wise entirely differs from standard CMOS inverter. Unlike

Fig. 1 Basic GDI cell

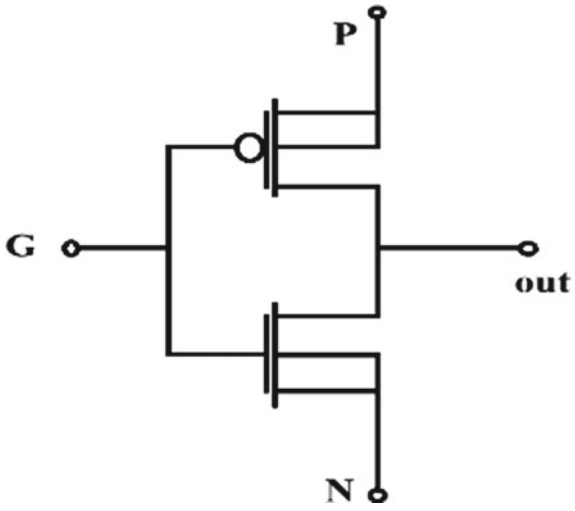

Table 1 Various input configuration of GDI cell for different Boolean functions

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A} + B$	F2
'1'	B	A	$A + B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B + AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

the CMOS inverter, the standard GDI cell is made up of three inputs nodes: (1) G (common gate input of both the PMOS and NMOS), (2) N (drain or source input of the NMOS), (3) P (drain or source input of the PMOS). Bulk or body terminal of NMOS is connected to N, and bulk terminal of PMOS is connected to the P. GDI technique offers a greater advantage compared to other technologies which are low-power dissipation and less transistor count. In Table 1, GDI cell input configuration for different logic functions using only using two transistors is shown. In CMOS, most of these logic functions are complex and require more than six transistors. If there are N input CMOS logic structure, then it could be extended to $N + 2$ input GDI cell by using Shannon expression.

Like other technologies, GDI is also suffering from some drawbacks first one is the low output voltage swing problem due to the poor high-to-low switching characteristics of PMOS. The second drawback is that is in the standard p-well CMOS fabrication process, it is not possible to implement all the functions mentioned in Table 1. For the successful implementation of these functions, SOI (silicon on insulator) or twin-well CMOS technologies are required. By using standard p-well CMOS process, only $F1$ function can be implemented because any NMOS bulk is continuously and equally biased [2].

The bulk node of both PMOS and NMOS is not biased properly which leads to the variations in threshold voltage. To overcome this drawback, the modified GDI cell is introduced in which the body terminal of both PMOS and NMOS are, respectively, connected to V_{dd} and ground. Apart from that threshold variations in m-GDI cell also improves the logic swing degradation [4]. The modified GDI basic cell is presented in Fig. 2. In this paper, all the logic circuit designs for GDI were based on the $F1$ and $F2$ functions only.

3 T Flip Flop

The flip flops are the primary building block of any sequential design. Flip flops are used to store 1-bit data. The flip flop is clocked, non-clocked flip flops are known as latches. These flip flops have many different types, in this paper, we are focusing on T flip flop. In toggle flip flop whenever the clock is triggered, it inverts the state

Fig. 2 Modified GDI cell

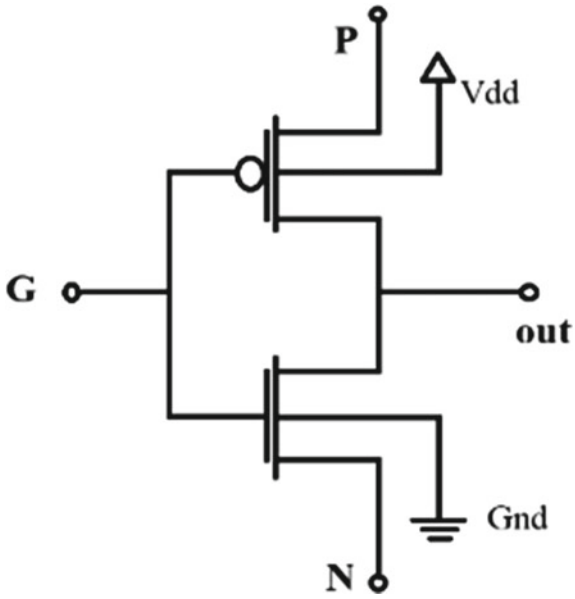

Table 2 Characteristics of TFF

	T	Q(t + 1)
No change	0	Q(t)
Toggle	1	Q′(t)

of flip flops. TFF is mostly used for designing of the counter. The characteristics of TFF is shown in Table 2 [5].

3.1 CMOS Based TFF

Figure 3 presents the master–slave TFF using CMOS technology. In this schematic, each NAND gate is based on CMOS logic. Schematic design consists of 6 two-input NAND gates and 2 three-input NAND gates. The circuit contains 38 transistors. Figure 4 shows the layout implementation of CMOS TFF.

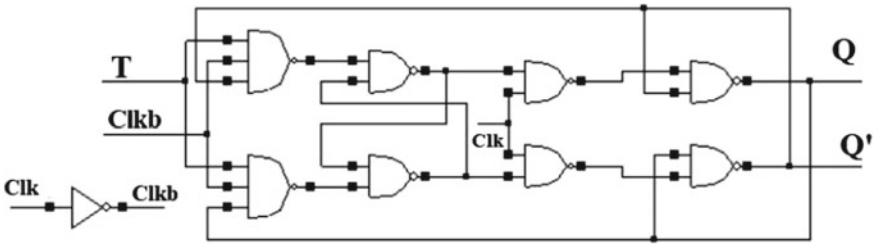

Fig. 3 TFF using CMOS logic

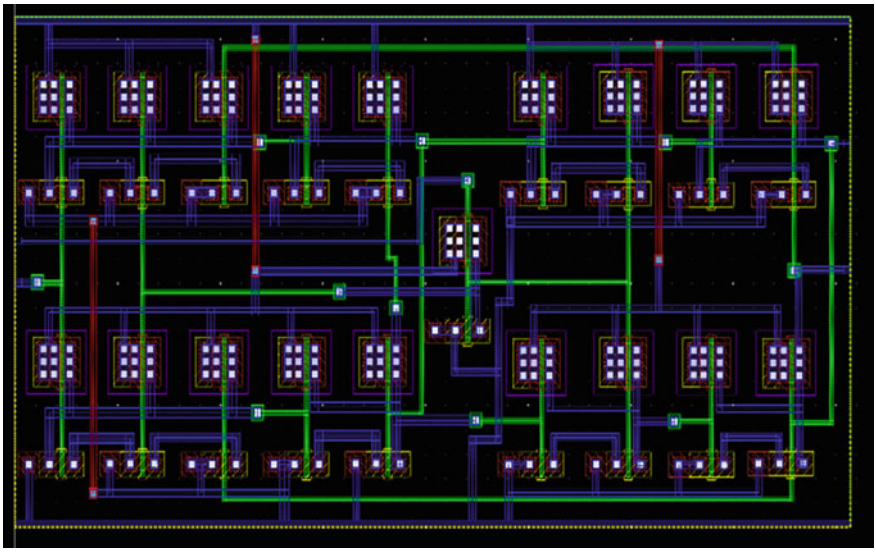

Fig. 4 Layout of CMOS master–slave TFF

3.2 TGB Based T Flip Flop

The transmission gate-based realization of the TFF is shown in Fig. 5. It consists of six transmission gates and six inverters and a total of 24 transistors. The layout of the transmission gate based TFF is presented in Fig. 6.

3.3 GDI Based TFF

The GDI implementation of T flip flop is presented in Fig. 7. This GDI T flip flop is based on only GDI F1 and F2 function. The total number of transistors used are 36. The Layout design of GDI TFF is presented in Fig. 8.

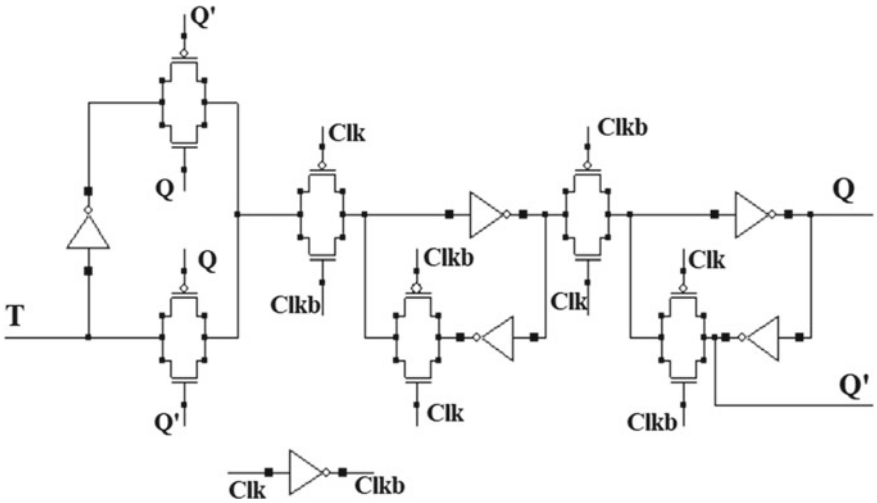

Fig. 5 Schematic of TGB T flip flop

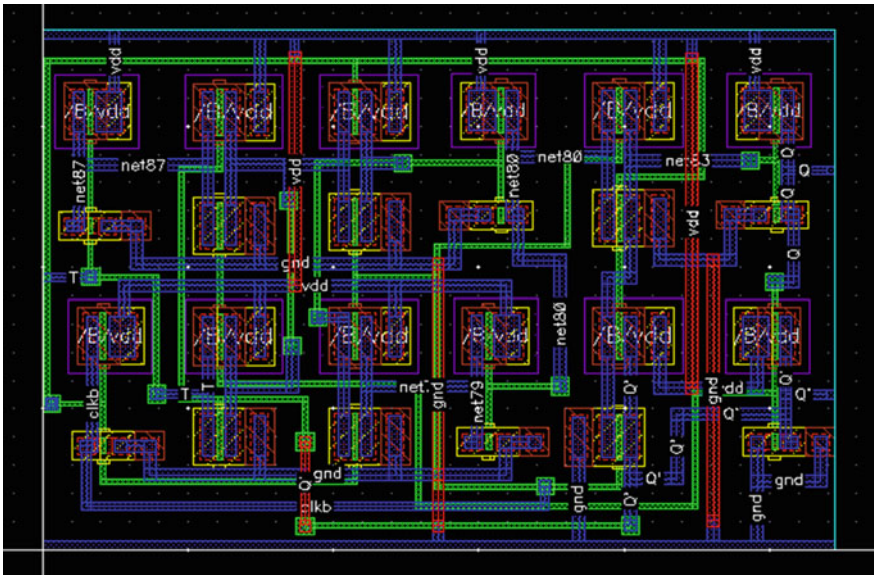

Fig. 6 Layout of TGB T flip flop

The simulation waveform of the GDI TFF is presented in Fig. 9. In that, the first waveform is input signal T, the second waveform is the clock signal. Then, the third waveform is output signal Q, and the last fourth waveform is output signal Q′. Outputs are changing their states when T is a high and positive edge of the clock occurs.

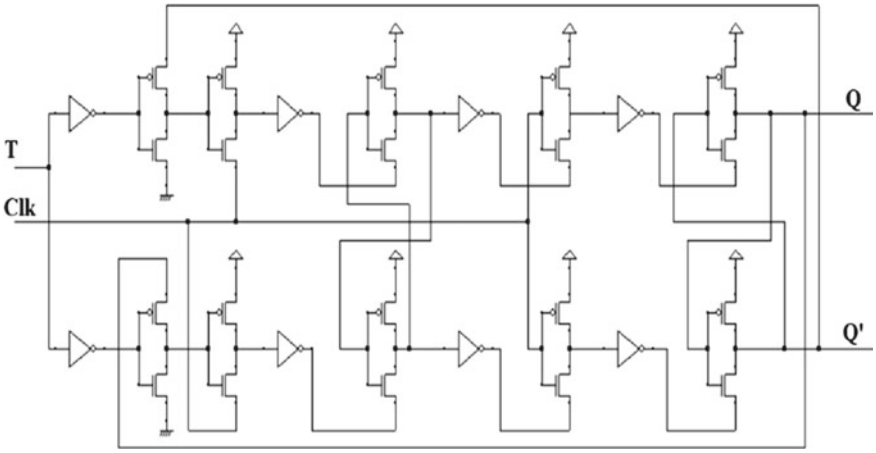

Fig. 7 GDI realization of TFF

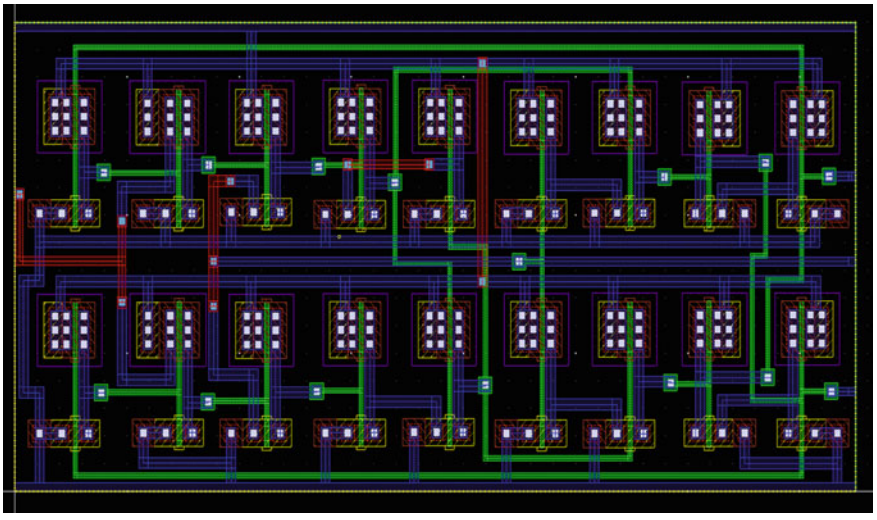

Fig. 8 Layout of GDI based master–slave TFF

4 Asynchronous Counter

Counters are designed with the use of flip flops. Counters are normally used in real-time digital processing applications. In the design of the N bit counter, N number of flip flops are used. For example, for a design of a 4-bit counter, 4 flip flops are required. The count range of N bit counter is from 0 to $2^n - 1$ for up counter and from $2^n - 1$ to 0 for the down counter. Counters are mainly two types synchronous and asynchronous. In the synchronous counter, for all the circuit, common clock pulse

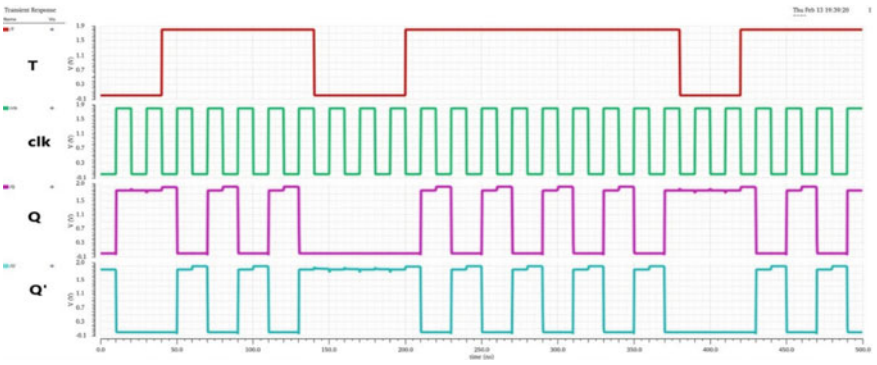

Fig. 9 Simulation waveform of GDI TFF

is used, wherein the asynchronous counter only one clock is used, the output of the previous logic circuit is taking to the next logic circuit as a clock [5]. In this paper, by using the T flip flop designed, a 4-bit asynchronous counter is designed.

The 4-bit asynchronous counter design using GDI is presented in Fig. 10. The four conventional GDI mater-slave TFFs are used, which resulted in a total of 144 transistors. Similarly, the 4-bit counter is also implemented using TGB and CMOS based master–slave T flip flops which resulted in a total of 96 and 152 transistors respectively. The simulation waveform of the counter is shown in Fig. 11. In that, first waveform is input signal T common to all flip flop, and it is always high. The second waveform is the clock signal. Then, all remaining eight waveforms are output signals Q1, Q2, Q3, Q4, Q1′, Q2′, Q3′, and Q4′, respectively. In Fig. 11, since T is always high, every change in output occurs at the positive edge of the clock.

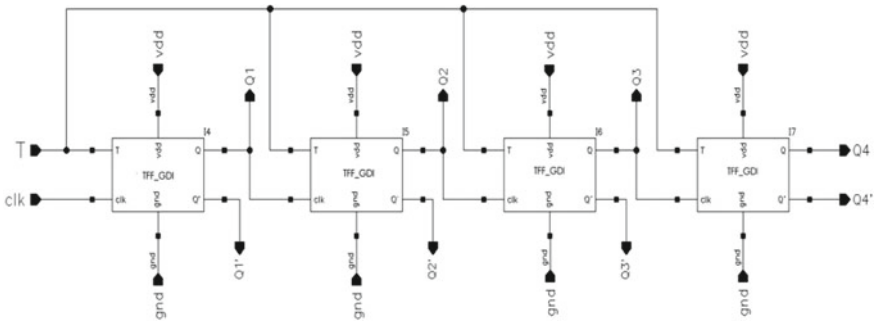

Fig. 10 GDI based 4-bit asynchronous counter

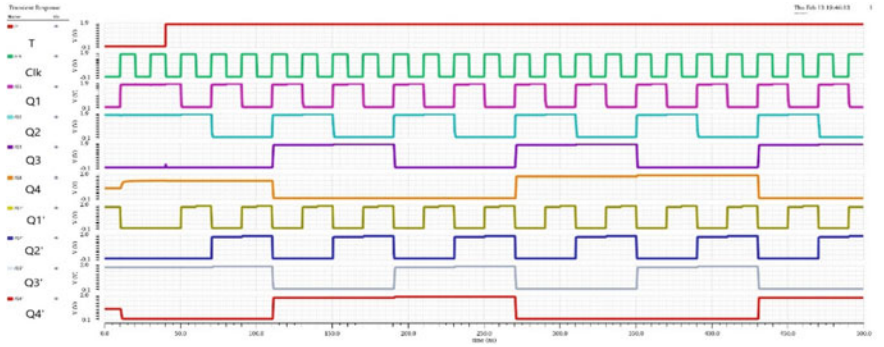

Fig. 11 Simulation waveform of GDI 4-bit asynchronous counter

5 Simulation and Performance Analysis

All the circuits and layouts are designed using the Cadence virtuoso tool for 180 nm technology, and circuits are simulated with a supply voltage as 1.8 V. All the results in a simulation are considered after the designing of the layout and all the parasitic and other capacitive parameters are taken into account. Each logic circuit is implemented using three different technologies: CMOS, GDI, and transmission gate. For all the circuits W/L of the PMOS transistor is taken three times the W/L of NMOS transistors, to achieve the best performance. Total width of each circuits including width of both NMOS and PMOS are specified in Tables 3 and 4. All the results are given in Tables 3 and 4 which are post-layout simulation results.

Table 3 shows the performance analysis of T flip flop for all the three design methodologies. GDI shows a comparatively good result for all parameters than

Table 3 Simulation results of CMOS, TGB, and GDI for master–slave T flip flop

Logic style	Number of transistors	Total width (μm)	Power (μW)	Area (μm^2)	Delay (ps)	PDP (fJ)
CMOS	38	41.04	24.42	851.75	215.63	5.265
TGB	24	33.48	21.62	501.72	242.51	5.243
GDI	36	38.88	19.92	635.84	212.17	4.226

Table 4 Simulation results of CMOS, TGB, and GDI for 4-bit asynchronous counter

Logic style	Number of transistors	Total width (μm)	Power (μW)	Area (μm^2)	Delay (ps)	PDP (fJ)
CMOS	152	164.16	70.70	4165.04	0.976	68.9
TGB	96	133.92	70.50	2567.49	1.440	101.5
GDI	144	155.52	37.61	3066.14	1.277	48.0

CMOS. Also, GDI shows better results than TGB for all parameters except the area. The number of transistors is less in TGB, and hence, area of TGB T flip flop is less than CMOS and GDI. Minimum power consumption and minimum delay are observed in GDI which is 19.92 μW and 212.17 ps, respectively. GDI T flip flop has the lowest PDP of 4.226 fJ.

In Table 4, the 4-bit asynchronous counter simulation results are presented. Lowest power consumption is in GDI which is 37.61 μW, while in CMOS and TGB, it is nearly double power consumption than the GDI. While the lowest delay is observed in the CMOS which is 0.97 ns, delay of GDI is 1.277 ns which is slightly higher than the CMOS. The number of transistors is less in TGB, so the area is less in TGB, but PDP of the TGB is more than double compared to GDI. Overall PDP for GDI, CMOS, and TGB are 48 fJ, 68.9 fJ, and 101.5 fJ, respectively.

6 Conclusion

In this paper, the cross-coupled NAND gate-based high-performance power and delay efficient T flip flop and 4-bit asynchronous counter are implemented with some popular designing methodologies like CMOS, TGB, and GDI. GDI counter which gives the most efficient power and PDP result because of the GDI master–slave T flip flop that has better performance than standard CMOS and TGB T flip flop.

All the logic circuits are implemented in 180 nm standard p-well CMOS technology. All the schematic and layout are designed and simulated using the Cadence virtuoso tool. The performance analysis is made for all the three designing methods for the major VLSI aspects like area, power, delay, and power–delay product. Simulation results with 1.8 V as a supply voltage for 180 nm technology show that the GDI counter has the least power consumption of 37.61 μW which is 46.8% less than the power consumption of CMOS and TGB counters. And also, the least PDP in GDI counter 48 fJ which is 30.3% less than the PDP of CMOS counter and 52.7% less than the PDP of the TGB counter.

So overall GDI gives the lowest power and PDP results for both the T flip flop and 4-bit asynchronous counter. The standard p-well CMOS process has some limitations for GDI implementation. In this paper, all the GDI circuits are implemented using only $F1$ and $F2$ functions. considering this limitation, it still gives the low power and PDP in comparison with CMOS and TGB.

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Performance Evaluation of Bimetallic Surface Plasmon Resonance Sensor Based on $Ti_3C_2T_x$ (MXene)

Rajeev Kumar, Sarika Pal, Narendra Pal, J. P. Saini, and Y. K. Prajapati

1 Introduction

The role of surface plasmon resonance (SPR) sensor has been seen in various sensing application of chemicals, physical and biological analytes [1, 2]. Surface plasmons (SPs) are free charge oscillations of electron at interface of metal–dielectric owning opposite sign permittivity and lead to generate in surface plasmon wave (SPW) at interface. SPW is transverse nature wave that decay exponentially in both dielectric medium and metal. Resonance condition occurs when the momentum of SPW and incident light matches with each other. This matching condition is obstructed by very little changes in the interface condition. SPR sensors are mostly realized by Kretschmann configuration because of its simple and realizable geometry [1]. Since last three decades, SPR sensors were utilized for their label-free, real-time and highly sensitive detection of bimolecular interaction monitored with modification in refractive index (RI) of sensing layer [2, 3]. The experimental realization of

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surface plasmon resonance sensor as biacore system found numerous applications such as in medical diagnostics, organic chemical detection, drug evolution in the pharmaceutical industry [4, 5] and other biomedical areas [6]. SP generation capability is dependent on exceptional optical properties of the metals like as silver (Ag), copper (Cu), gold (Au) and nickel (Ni) [7]. These metals possess best SPR characteristics in visible range while in infrared range their utilization is limited due to higher losses [7]. Currently researchers in near-infrared range have used nanostructure transparent conducting oxide, e.g., Ga-doped zinc oxide instead of metals for SP generation [8]. Such SPR sensors have been utilized for figure of merit enhancement as they show low sensitivity in near-infrared region. So, for SPR sensor operating in visible range, metals are best choice for SP generation to get higher sensitivities. Au is commonly used metal for SP generation due to its sensitivity, non-toxicity and stability for biomolecular interaction. But, they compromise accuracy of detection due to larger imaginary part of permittivity responsibly for SP damping effect [9]. The utilization of Ag metal is capable of giving accurate detection with trade-off in sensitivity, if protected from oxidation by using some other material over it [10]. Ag is easily oxidized in the ambient environment and is potentially toxic to the living cell as well [10, 11]. Therefore, many researchers used bimetallic layers in SPR sensor to deal with trade-offs between sensitivity and accuracy. Bimetallic combination of Ag and Au has been used for chemical sensing and bimolecular detection [12–14]. Researchers tried not only bimetallic configurations for specific sensing but also utilized different materials possessing unique optical sensing properties. Some examples of such materials are graphene [15], antimonene [16], black phosphorus [17], transition metal di-chalcogenides [18] and metamaterials [19]. In past few years, MXene ($Ti_3C_2T_x$) is newly introduced material in 2D materials family useful for SPR sensing [20–28]. It consists of transition metal carbides and nitrides with attractive electrochemical properties. Its excellent physical, electronic and electrochemical properties have been used in sensor, energy conservation devices and electrochemical capacitor [20–22]. The use of 2D material MXene (Ti_3C_2Tx) as bio-recognition element (BRE) layer helps to capture the biochemical molecules present in an aqueous solution. The unique properties of Ti_3C_2Tx (MXene), i.e., high metallic conductivity, hydrophilic surface terminations, larger surface area and higher binding energies provides enhanced sensing performance of SPR sensor [23–27]. Its excellent hydrophilic, functionalized surface terminations (–OH, =O and –F) help to capture biochemical molecules present in sensing medium to increase the sensitivity. Larger surface and higher binding energy of MXene provide larger contact area and efficient binding of biochemical molecules on its surface [23–27]. Wu et al. [25] recently demonstrated an Au-based SPR sensor with Ti_3C_2Tx (MXene), which exhibited the higher sensitivity 160°/RIU at 633 nm wavelength. Xu et al. [26] theoretically investigated an Au-based SPR sensor with TMD and $Ti_3C_2T_x$. They calculated highest sensitivity 198°/RIU with five-layer WS_2. Srivastava et al. [27] theoretically investigated the $Ti_3C_2T_x$ (MXene)-based SPR sensor. Group obtained the maximum sensitivity 190.2°/RIU for their proposed work. Pal et al. [28] remarkably increases the sensitivity of SPR sensor using heterostructure of $Ti_3C_2T_x$ (MXene) and BlueP/MoS_2 for biochemical sensing. Their work exhibited

the highest sensitivity of 204°/RIU for three layers of BlueP/MoS_2 and monolayer $Ti_3C_2T_x$ (MXene) using Ag metal and CaF_2 prism. Bimetallic layers are not tried yet for $Ti_3C_2T_x$ (MXene)-based SPR sensor for sensing of analytes.

So, this work presents a new $Ti_3C_2T_x$ (MXene)-based SPR biosensor configuration using bimetallic layers of Ag and Ni. Ni is chemically inactive metal, and it shows poor plasmonic properties due to high Joule losses [11, 29, 30]. Ni possesses remarkable magnetic and magneto optical merits useful for sensing [11, 29, 30]. On combining these ferromagnetic and noble metals provides a high sensitivity as compared to conventional SPR sensor by localizing electromagnetic field associated with plasmonic response [29, 30]. The cost of Ni is less than that of other metals. This bimetallic combination is used to get significantly enhanced sensitivity after including the nickel (Ni) layer. The selective performance factors such as sensitivity (S), minimum reflectance (R_{min}), detection accuracy (DA) and quality factor (QF) are evaluated by characterizing the reflectance curve of the proposed design.

This work is demonstrated in various sections. Section 2 clarifies the numerical modeling; Sect. 3 expresses the results and discussion; and finally, Sect. 4 concludes this work.

2 Sensor Design, Theoretical Model and Performance Factors

The proposed $Ti_3C_2T_x$ (MXene)-based bimetallic configuration is shown in Fig. 1. The first layer is BK7 prism with refractive index 1.5151 at 633 nm wavelength [31–33].

The second and third layers are of Ag (optimized thickness) and Ni metal (5 nm, 10 nm and 15 nm thickness) grown on top of BK7 prism, respectively. The refractive indices of Ag and Ni are calculated using Drude–Lorentz model [29].

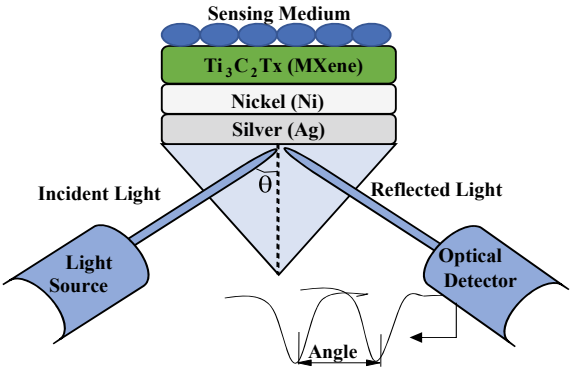

Fig. 1 Proposed SPR biosensor

$$n_m(\lambda) = \sqrt{1 - \frac{\boldsymbol{\lambda}^2 \boldsymbol{\lambda}_c}{\boldsymbol{\lambda}_p^2(\boldsymbol{\lambda}_c + i\boldsymbol{\lambda})}} \tag{1}$$

where $\boldsymbol{\lambda}_c$ is collision wavelength (1.7614×10^{-5} for Ag and 2.84092×10^{-5} for Ni), $\boldsymbol{\lambda}_p$ is plasma wavelength (1.4541×10^{-7} for Ag and 2.5381×10^{-7} for Ni) and $\boldsymbol{\lambda}$ is 0.633 μm wavelength. The use of fourth layer is $Ti_3C_2T_x$ (MXene) as BRE layer for biochemical sensing with RI 2.38 + 1.33i [32–34]. The last layer is sensing layer for analyte detection. The RI of the sensing medium is changed from $n_s = 1.330$ to 1.335 [32–34].

The transfer matrix method (TMM) is applied to get reflectivity of the p-polarized incident light [31–34]. The tangential E and H fields between first and last boundaries are related by:

$$\begin{bmatrix} E_1 \\ H_1 \end{bmatrix} = U \begin{bmatrix} E_{N-1} \\ H_{N-1} \end{bmatrix} \tag{2}$$

where E_1, H_1 and E_{N-1}, H_{N-1} shows the tangential field component at the 1st and Nth layer, respectively, where U denotes final matrix of the combined five-layer configuration as [27].

$$U = \begin{bmatrix} U_{11} & U_{12} \\ U_{21} & U_{22} \end{bmatrix} = \prod_{k=2}^{N-1} U_k, \tag{3}$$

where U_k corresponding to Kth layer is

$$U_k = \begin{bmatrix} \cos\beta_k & -i(\sin\beta_k)/q_k \\ -i q_k \sin\beta_k & \cos\beta_k \end{bmatrix} \tag{4}$$

And k lies from 1 to N
where

$$q_k = \left(\frac{\mu_k}{\varepsilon_k}\right)^{\frac{1}{2}} \cos\theta_k = \frac{(\varepsilon_k - n_1^2 \sin^2\theta_1)^{\frac{1}{2}}}{\varepsilon_k} \tag{5}$$

Here,

$$\beta_k = \frac{2\pi}{\lambda} n_k \cos\theta_k (z_k - z_{k-1}) = \frac{2\pi d_k}{\lambda} \left(\varepsilon_k - n_1^2 \sin^2\theta_1\right)^{\frac{1}{2}} \tag{6}$$

and

$$q_k = \frac{\left(n_k^2 - n_1^2 \sin^2\theta_1\right)^{\frac{1}{2}}}{n_k^2} \tag{7}$$

The wavelength is λ and incident angle is θ_1.

Reflection coefficient (r_p) is given as follows:

$$r_p = \frac{(U_{11} + U_{12}q_N)q_1 - (U_{21} + U_{22}q_N)}{(U_{11} + U_{12}q_N)q_1 + (U_{21} + U_{22}q_N)} \tag{8}$$

where q_1 and q_N calculated from Eq. (5) are related terms for the 1st and Nth layer, respectively.

The reflectance is given as:

$$R = \left|r_p\right|^2 \tag{9}$$

2.1 Sensor Performance Factor

Performance factors calculated from reflectance curve must be high for a good sensor. Sensitivity, accuracy and quality of detection are used to measure sensor performance [31]. The resonance angle shift w.r.t variation in RI of sensing layer is known as sensitivity (S).

$$S = \frac{\Delta\theta_{\text{res}}}{\Delta n_{\text{s}}} \tag{10}$$

Detection accuracy (DA) measures resolution of SPR sensor, which is calculated from spectral width of reflectance curve. It is inversely proportional to full width at half maximum, FWHM, and it is difference of resonance angle at 50% reflectivity of reflectance curve. DA and quality factor (QF) may be given as:

$$\text{DA} = \frac{1}{\text{FWHM}} \tag{11}$$

$$\text{QF} = \frac{S}{\text{FWHM}} \tag{12}$$

3 Results and Analysis

The objective is to see the effect of the bimetallic layer of Ag and Ni with 2D material $Ti_3C_2T_x$ (MXene) on sensor performance. To compare the effect of nickel in proposed bimetallic design, the simulated results are evaluated with and without Ni. First Ag and Ni thicknesses are optimized for the proposed design, and then,

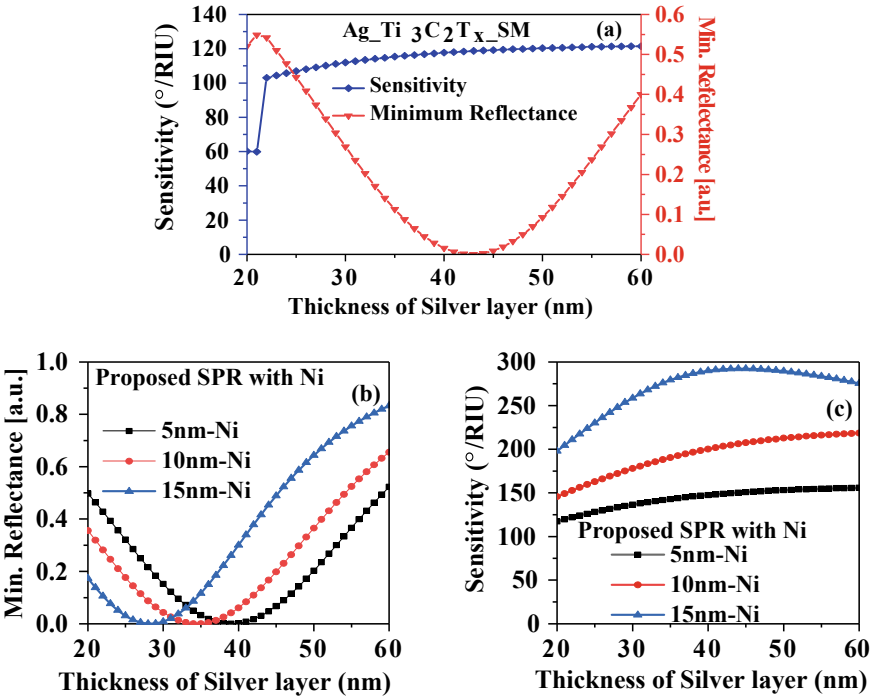

Fig. 2 **a** Variation of R_{min} and sensitivity for Ag thickness for proposed SPR without Ni. **b** Variation of R_{min}. **c** Sensitivity for Ag thickness for proposed sensor

their performances is evaluated in terms of sensitivity, DA and QF curves. Figure 2a shows Ag thickness optimization by plotting variation of minimum reflectance (R_{min}) and sensitivity versus Ag thickness (20–60 nm) for proposed sensor without Ni. The R_{min} first decreases from 0.52 a.u., becomes minimum to 0.0004 a.u. at 43 nm and then increases to 0.40 a.u. for Ag thickness change from 20 to 60 nm. The sensitivity increases from 60°/RIU to 121°/RIU for Ag thickness variation from 20 to 60 nm. So, Ag thickness of 43 nm may be chosen as optimized thickness at which minimum R_{min} and larger sensitivity is achieved for proposed sensor without Ni. After adding the Ni layer (5 nm, 10 nm and 15 nm), variation of the minimum reflectance and resonance angle shift ($\Delta\theta_{res}$) is shown in Fig. 2b, c, respectively, to optimize thickness of Ag and Ni. Minimum reflectance (R_{min}) shifts to smaller Ag thickness for higher values of Ni thickness as observed in Fig. 2b [31]. It demonstrates minimum reflectance (R_{min}) of 0.0003 a.u. obtained at 28 nm Ag thickness for 15 nm thickness of Ni layer. On analyzing Fig. 2c, it gives higher shift of resonance angle ($\Delta\theta_{res}$) for 15 nm Ni [31]. Higher resonance angle shift and minimum reflectance (R_{min}) are necessary to achieve large sensitivity and accuracy. On calculating sensitivity from Eq. (10) for Fig. 2c, it increases from 117°/RIU to 156°/RIU and 146°/RIU to 218°/RIU at optimized Ag thickness for 5 nm and 10 nm thickness of Ni layer, respectively. Figure 2c suggests

sensitivity increases from 198°/RIU to 292.32°/RIU for the Ag thickness from 20 to 45 nm, and thereafter, it decreases from 292.09°/RIU to 275°/RIU for the Ag thickness from 46 to 60 nm for 15 nm Ni thickness. This shows the highest sensitivity of 292.32°/RIU is attained at 45 nm Ag and 15 nm Ni thickness. Thus, after analyzing Fig. 2b, c optimized Ag and Ni thicknesses are 28 nm and 15 nm, respectively. At these optimized thicknesses, higher resonance angle shift and minimum reflectivity is obtained for proposed design.

Figure 3a–c shows the reflectance curve for proposed design without Ni, proposed SPR without $Ti_3C_2T_x$ (MXene) and proposed SPR, respectively. Figure 3a indicates

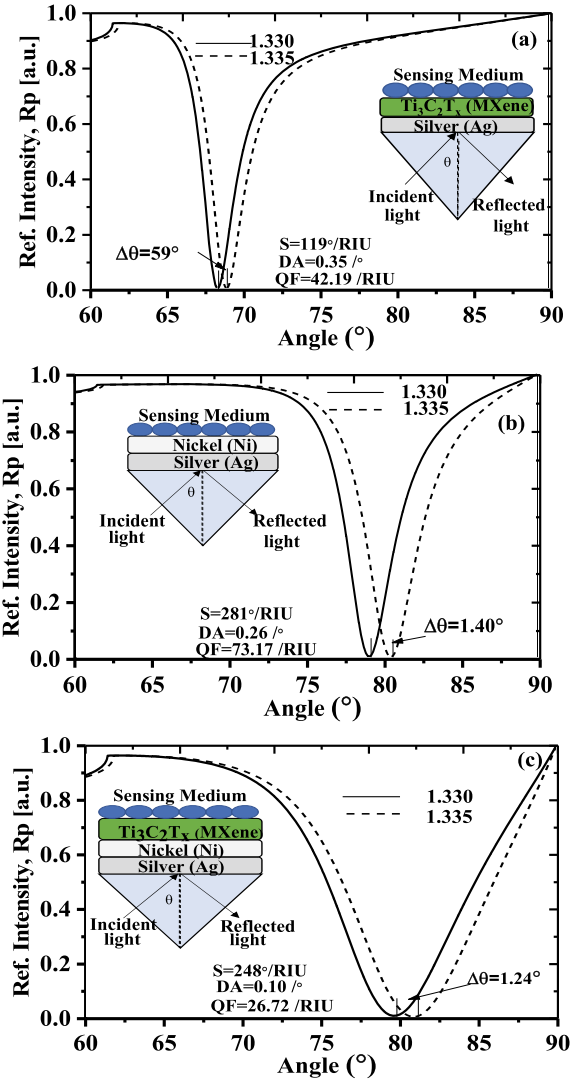

Fig. 3 Reflectance curve for: **a** proposed SPR sensor without nickel, **b** proposed SPR sensor without $Ti_3C_2T_x$ (MXene), **c** proposed SPR sensor

resonance angle shift ($\Delta\theta_{res.}$) of 0.59° for $\Delta n_s = 0.005$ for proposed SPR without Ni. Sensitivity, DA and QF calculated from reflectance curve shown in Fig. 3a are 119°/RIU, 0.35/degree and 42.19/RIU. Figure 3b shows the reflectance curve of proposed SPR sensor without MXene at 15 nm Ni and 41 nm Ag thickness, for $\Delta n_s = 0.005$. The larger resonance angle shift ($\Delta\theta_{res.} = 1.40°$) is obtained. This indicates use of Ni enhance SP field by localizing it in sensing region [30]. Figure 3b indicates the sensitivity, detection accuracy and quality factor for proposed design without MXene are 281°/RIU, 0.26/degree and 73.17/RIU, respectively. Figure 3c shows the reflectance curve of proposed SPR sensor using 15 nm Ni at 28 nm Ag thickness for $\Delta n_s = 0.005$. The larger resonance angle shift ($\Delta\theta_{res.} = 1.24°$) is obtained for proposed design than without using Ni. Figure 3c indicates the sensitivity, detection accuracy and quality factor for proposed design are 248°/RIU, 0.10/degree and 26.72/RIU, respectively. Thus, we can conclude bimetallic configuration in $Ti_3C_2T_x$ (MXene)-based SPR sensor show much better performance for sensing of analytes. This is due to use of Ni responsible for sensitivity improvement and better adsorption properties of $Ti_3C_2T_x$ [23, 24].

Parameters obtained from reflectance curve plotted for proposed SPR without Ni, proposed SPR without $Ti_3C_2T_x$ and proposed SPR shown in Fig. 3a–c are also provided in Table 1 for easier analysis. The data entered in Table 1 show clear comparison of all performance factors calculated for proposed SPR without Ni, proposed SPR without $Ti_3C_2T_x$ and proposed SPR. The comparison of both Fig. 3b, c and Table 1 indicates that sensitivity for proposed SPR sensor without MXene is much higher than on using MXene. However, the proposed SPR sensor without MXene indicating Ni at top layer will not be able to bind analytes efficiently on it. So, in spite of highest sensitivity attained for proposed SPR sensor without MXene, the

Table 1 Performance parameter at optimized silver and Ni (15 nm) thickness with monolayer $Ti_3C_2T_x$

Parameters		Proposed SPR without Ni	SPR without MXene	Proposed SPR with Ni
Resonance angle before adsorption ($n_s = 1.330$)		68.27	79.06	79.6720
Resonance angle after adsorption ($n_s = 1.335$)		68.86	80.47	80.9119
Resonance angle shift ($\Delta\theta$), $\Delta n_s = 0.005$ (degree)		0.59	1.40	1.239
Sensitivity (°/RIU)		119	281	248
FWHM (degree) n_s	1.330	2.82	3.84	9.28
	1.335	2.90	4.15	9.70
DA (/degree) n_s	1.330	0.35	0.26	0.107
	1.335	0.34	0.24	0.103
Quality factor (/RIU)	1.330	42.19	73.17	26.72
	1.335	41.03	67.10	25.56

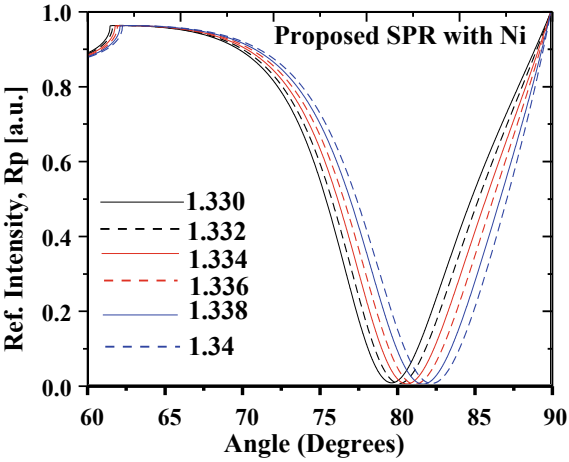

Fig. 4 Variation of the reflectance curve for different sensing medium RI, n_s

proposed SPR sensor shows efficient analyte sensing due to higher binding energies, larger surface area and hydrophilic surface terminations of MXene ($Ti_3C_2T_x$).

We plotted reflectance curve for proposed SPR, for wide range of sensing medium RI (1.33–1.34), as shown in Fig. 4. There is right shifting of resonance angle to higher value with slow increase in the angular beam width for higher sensing layer RI up to 1.340. Thus, nature of the reflectance curve suggests that proposed SPR can operate for wider range with good sensitivity and detection accuracy. Figure 5a–c indicates the variation in performance factors such as sensitivity, FWHM, DA and QF with increasing RI of the sensing medium at optimized Ag and Ni thicknesses in visible range. The variation of sensitivity increases with change in RI of sensing layer from [116°/RIU to 119°/RIU], [261°/RIU to 303°/RIU] and [236°/RIU to 259°/RIU] for Ag-Ti_3C_2Tx-SM, Ag-Ni-SM and Ag-Ni-Ti_3C_2Tx-SM structures, respectively, as shown in Fig. 5a. Similarly, the FWHM increases with change in RI of sensing layer from [3.17° to 3.37°], [3.82° to 4.54°] and [9.48° to 9.79°] for Ag-Ti_3C_2Tx-SM, Ag-Ni-SM and Ag-Ni-Ti_3C_2Tx-SM structures, respectively. Figure 5a shows that the sensitivity obtained for Ag-Ni-SM structure is much higher than that of other two proposed structure. But, Ni does not possess unique attachment properties like of Ti_3C_2Tx for attachment of biochemical molecules, so it cannot be used as BRE layer in spite of achieving high sensitivity. Figure 5b indicates the variation in detection accuracy and quality factor for change in sensing layer RI of Ag-Ti_3C_2Tx, Ag-Ni and proposed SPR sensor. The detection accuracy decreases from [0.315/° to 0.296/°], [0.1054/° to 0.1021/°] and [0.261/° to 0.220/°] of Ag-Ti_3C_2Tx-SM, Ag-Ni-SM and Ag-Ni-Ti_3C_2Tx-SM, respectively, as shown in Fig. 5b. Detection accuracy decreases for higher sensing layer RI because it is reciprocal to FWHM, and FWHM has shown increasing trend for Ag-Ti_3C_2Tx-SM, Ag-Ni-SM and Ag-Ni-Ti_3C_2Tx-SM structures in Fig. 5a. Now, the quality factor variation with sensing layer RI is from [36.460/RIU to 35.363/RIU], [68.39/RIU to 66.66/RIU] and [24.90/RIU to 26.464/RIU] for Ag-Ti_3C_2Tx-SM, Ag-Ni-SM and Ag-Ni-Ti_3C_2Tx-SM structures.

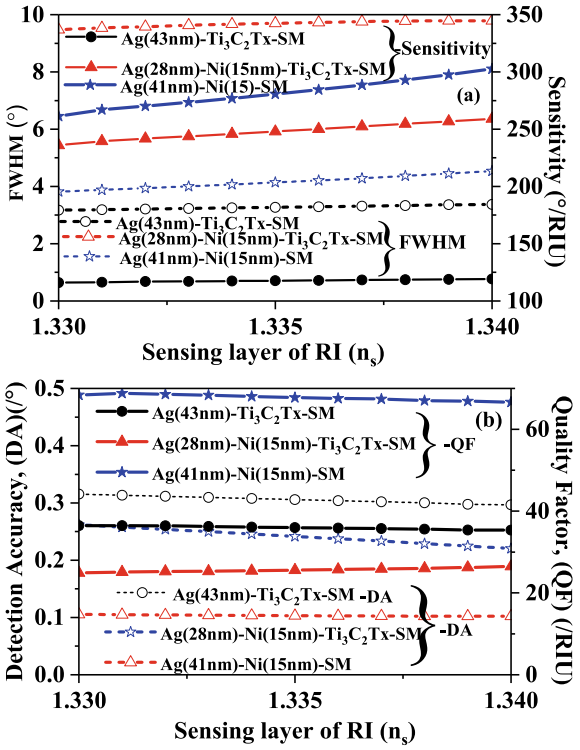

Fig. 5 Variation of **a** sensitivity and FWHM, **b** detection accuracy and quality factor as a function of sensing layer RI for proposed SPR sensor without nickel, proposed SPR sensor without Ti3C2Tx (MXene) and proposed SPR sensor

In proposed bimetallic SPR sensor, silver first layer provides the sharp SPR dip and high detection accuracy, while Ni as second layer provides chemical stability and high sensitivity. The resonance angle for all thicknesses of Ni layer enhances with increase in RI of sensing medium with MXene [30]. The detection accuracy (DA) and the quality factor (QF) decreased with the addition of $Ti_3C_2T_x$ (MXene) layer due to higher imaginary part of MXene which increases the damping losses. Thus, the rise in MXene layers increases damping in SPs which increases the FWHM, which is a linear function of damping and as a result, the detection accuracy and quality factor decrease. The use of Ni enhances the electromagnetic field in sensing layer interface by localizing the electromagnetic field at sensing layer interface [30].

Lastly, a comparison of the proposed work with recently investigated $Ti_3C_2T_x$-based SPR sensor is presented in Table 2.

4 Conclusion

In this work, $Ti_3C_2T_x$ (MXene)-based SPR sensor with bimetallic layers of Ag-Ni has been theoretically analyzed for improving the sensitivity. The top Ni layer protects

Table 2 Sensitivity comparison of the proposed work with recently investigated $Ti_3C_2T_x$-based SPR sensor

Structure and references	Sensitivity (°/RIU)
Prism/gold layer/$Ti_3C_2T_x$/sensing medium [26]	160
Prism/WS_2/$Ti_3C_2T_x$ [27]	198
Prism/gold layer/$Ti_3C_2T_x$/WS_2/black phosphorus/sensing medium [28]	190.2
Prism/silver layer/$Ti_3C_2T_x$/blueP-MoS_2/black phosphorus/sensing medium [29]	204
Proposed—prism/silver layer/nickel layer/$Ti_3C_2T_x$/sensing medium	292

the Ag layer from oxidation and also increases the sensitivity of proposed SPR sensor. Thicknesses of Ag and Ni layer are optimized before evaluating the sensitivity, which obtained the sensitivity 248°/RIU at Ag thickness (28) with Ni layer (15) with 3×10^{-4} a.u. minimum reflectance. The sensitivity is increased for higher Ni thickness. The result shows that when the monolayer Ti_3C_2Tx is deposited on the Ag-Ni layers, the sensitivity reaches up to 292°/RIU at optimized Ag thickness (45 nm) with Ni layer (15 nm) with changing RI of sensing medium from 1.330 to 1.335. Also, detection accuracy and quality factor decrease because of increased damping of surface plasmons due to higher imaginary part of RI of MXene. Sensitivity of Ag-Ni bimetallic layer-based proposed SPR sensor is maximum than that of Ag-$Ti_3C_2T_x$ layers.

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Optimized FPGA Implementation of 64-Point FFT Using Folding Transformation

Nafzia and L. Lijesh

1 Introduction

The rapidly advancing communications and computing industry handles digital signal processors (DSPs). The consistency of DSP results with limited performance and high power dissipation includes mathematical calculations and analysis, i.e., spectrum analysis, correlation analysis, and filtering of low DSP applications [1]. When understanding complex mathematical operations, the tools circuit must evaluate and analyze its operating parameters such as area, time, and power. Among those parameters and the increase in circuit complexity including more functionality, speed optimization is the crucial parameter that demands to be addressed. One of the main reasons for speed optimization is the demand in the new generation of portable devices including laptops, palmtops, and mobile phones.

With the growth of VLSI, FFT indicates that it is working on an extensive area of DSP and communication system applications. Although there are many DSPs that can perform an FFT fast sufficient to maintain several real-time applications, some systems demand additional computation or speed requirements that exceed the abilities of a DSP [2]. Under those circumstances, that dedicated logic has been proven to be useful for an FFT computing. Moreover, FFT remains extensively utilized within communication systems, particularly orthogonal frequency division multiplexing (OFDM) systems, wireless LAN, ADSL, VDSL systems, and Wi-MAX. Besides usage, the system requires high performance, low power consumption, and also low chip area. And it should enhance nearly ubiquitous in high-speed signal processing.

The FFT leads to efficient algorithm optimization for determining the discrete Fourier transform (DFT). There are many techniques and algorithms for FFT in the survey, and recent developments that increase performance and power [3]. Most of the FFT processors are memory-based architectures that contain the main processing

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component and several memory units. Those architectures are cost-effective and cannot be parallelized. Consequently, low-power techniques need to be used to optimize the power distribution in complex circuits. So the pipeline architectures are especially suitable for real-time employment because they can efficiently merge among the sequential nature of sampling.

FPGA devices are frequently utilized for hardware implementations in communications purposes; FPGAs in high-level technologies can obtain excellent execution while they must have high flexibility, fast design time, and also cheaper cost [4]. Similarly, FPGAs become frequently attractive toward FFT processing purposes; moreover, it is the objective principle of this paper. In the VLSI device, less area usage, low power consumption, and high speed are some of the important parameters. Therefore, the main purpose of the proposed architecture is designed to enhance the execution speed and also reduce the hardware complexity.

In this paper, we focus on the speed-optimized 64-point pipelined FFT architecture, which uses the concept of folding transformation technique to balance the trade-off between flexibility and performance. Folding transformation is a method that decreases the area of the silicon chip by joining different arithmetical operations into one operation utilizing time scheduling techniques [5]. The proposed work is focused on the design of the efficient architecture for 64-point FFT using the radix-2^2 Single path delay feedback (SDF) algorithm which aims at efficient butterfly computation which results in high-speed processing with less power consumption and hardware complexity. The design is implemented for analyzing numerous parameters such as power, area, and time. It combines the benefits of pipeline architecture with the capability to reduce the operations and generalizable for any point of FFT's, which is the power of 2. This design is coded using VHSIC-HDL and also simulated under Xilinx ISE 14.2.

The paper organization is as follows: In Sect. 2, the FFT algorithm is discussed. The folding technique is discussed in Sect. 3. Pipeline FFT implementation architecture is explained in Sect. 4. Section 5 has results and discussion. Finally, Sect. 6 represents a brief conclusion.

2 FFT Algorithm

The FFT processor refers to the hardware implementation of the FFT algorithm for the DFT that calculates all of those signals in the time domain towards the frequency domain. FFT is an efficient algorithm, which uses periodic and symmetric properties DFT twiddle factors compute the DFT with minimal computations. Until the 1960s, this algorithm was software-based. However, as technology such as system-on-chip develops, FFT algorithms can no longer be implemented in hardware forms [6]. Nowadays, most DSP and wireless applications are designed to run on a portable system, and the FFT processor has low power requirements. By dividing the DFT into smaller DFTs, it provides several technologies that reduce the computational complexity from (N^2) to ($\log_2 N$). The DFT of the N series of complex numbers X_0,

…, X_{N-1}can be expressed as Eq. 1.

$$X(k) = \sum_{n=0}^{N-1} W_N^{kn}; \quad 0 \le k \le N-1,\ 0 \le n \le N-1 \tag{1}$$

where

$$W_N^{kn} = \mathrm{e}^{-2\pi j/N}$$

The term W^{kn} is the DFT coefficient also called the twiddle factor; N is the DFT length, (n) is the time sequence and $X(K)$ is a frequency sequence.

Implementation of DFT Eq. 1 results in larger hardware and higher complexity. Therefore, FFT was developed to overcome its computational complexity and reduce hardware costs. FFT algorithms follow the specific process of partitioning and conquering, which implies redundancy in the structure. The FFT can efficiently decompose and estimate a DFT by using the symmetric and periodical property of the complex sequence W_N. The FFT property can be explained in Eqs. 2 and 3 they are highly beneficial to simplify the rotatable calculation:

$$\text{Symmetry property} \quad W_N^{k+\frac{N}{2}} = W_N^{N/2} \times W_N^k = -W_N^K \tag{2}$$

$$\text{Periodicity property} \quad W_N^{k+N} = W_N^k \times W_N^N = W_N^K \tag{3}$$

Hence, FFT with two parameters n and k; they are the time index and frequency index, respectively. Therefore, it decreases the complex arithmetic operations from N^2 to $(N/2)$ and $N\log_2 N$, respectively. Commonly, it works by decomposing the input signals into smaller steps. The analysis can be achieved by adopting either decimation-in-frequency (DIF) or decimation-in-time (DIT) decomposition for efficient computation [6].

If the length of the sequence N is taken as $N = r^m$ here, r is called the radix size of the FFT algorithm. The most effectively realized choice for $r = 2$ leads to radix-2 FFT algorithms. Therefore, with $N = 2^m$, the effective computation is performed by dividing the N-point DFT to $\frac{N}{2}$-point DFTs, then each $\frac{N}{2}$-point DFT divided to $\frac{N}{4}$-point DFTs and continuing this process until 2-point butterflies are obtained [7]. The total computational cost can be considerably reduced with the aid of the shorter FFTs, their outputs again used to calculate numerous outputs.

Equation 1 can be expanded as:

$$X(k) = \underbrace{\sum_{n=0}^{N-2} x(n) W_N^{nk}}_{\text{even}} + \underbrace{\sum_{n=1}^{N-1} x(n) W_N^{nk}}_{\text{odd}} \tag{4}$$

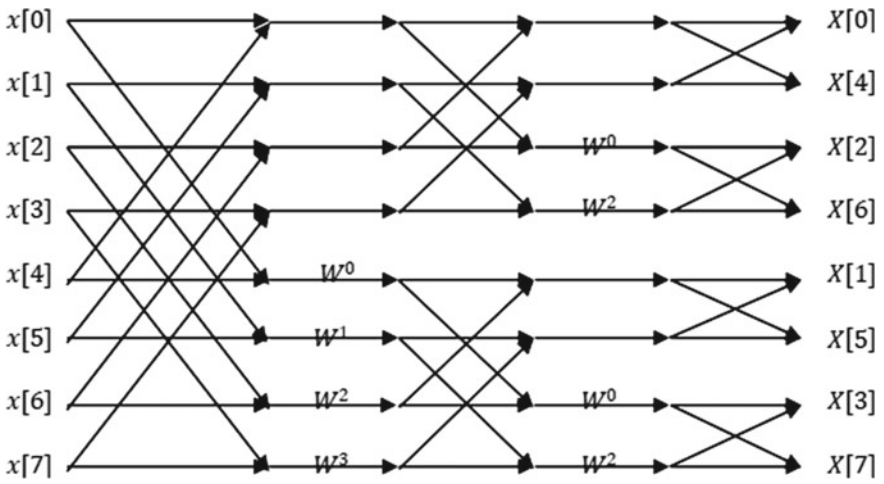


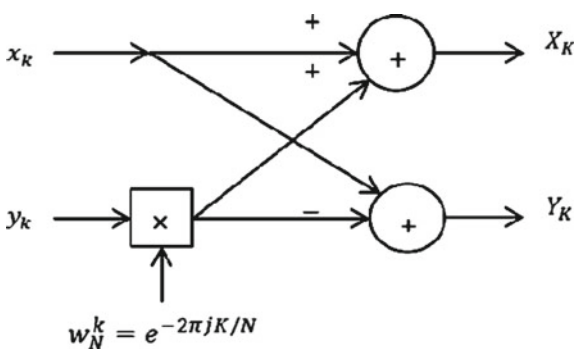
Fig. 1 Decomposition of 8-point DIT FFT

The radix-2 FFT reconfigures the Eq. 1 toward two sections: a sum of even digits $n = 0, 2, 4, \ldots, N - 2$ and sum over the odd digits $n = 1, 3, 5, \ldots, N - 1$ explained in Eq. 4. The DIT algorithm decomposition for $N = 8$ would be shown in Fig. 1.

2.1 Radix-2 Point Butterfly Structure of FFT

In every FFT processors, the fundamental building block is the butterfly computation unit (BCU), which is used to perform mathematical operations. Each butterfly has its controller independent of each other. The decomposition of each N-point FFT can cause micro-operations to be repeated, hence the so-called butterfly operation. Here, $N = 2n$ is usually called radix-2 FFT, and the calculation will be done with twiddle factor, hence a 2-point form of DFT is called "butterfly" [8] is shown in Fig. 2.

Fig. 2 2-point FFT butterfly and its operation



The butterfly unit consists of two inputs denoted by x_k and y_k with their respective outputs X_k and Y_k. This algorithm destroys the frequency samples at each step of the FFT. Functions are identified in each pair of input signals. Note that the multiplications by j are performed by the following:

$$X_K = x_k + y_k W_N^K \tag{5}$$

$$Y_K = x_k - y_k W_N^K \tag{6}$$

Equations 5 and 6 represent the relationship between real and imaginary data. Furthermore, in addition, the BCU determines the expense and properties of the FFT processor. It consists of complex multipliers and adders, and this multiplier remains the speed control of an FFT processor implementation [9]. If those complex multiples are performed by utilizing, shift, and add operation that will occur into high-priced hardware and limit the realization of FFT.

The FFT uses only a single BCU in most cases to repeat all the calculations and required the least amount of memory due to the "in-place" memory access approach. With the "in-place" approach, the butterfly computational outputs are put into the corresponding memory location of input; hence half of the memory utilization can be reduced. The research provides an effective address system for parallel and pipelined "in-place" memory access. It delivers an output value for each clock period; besides, the memory and butterfly block use 100% performance in every pipeline.

3 Folding Transformation Technique

It is the method of reducing the silicon area of an IC through multiplexing various processes towards an individual signal operative unit, such as multipliers, adders, registers, multiplexers, and interconnection wires [10]. Folded structures are therefore designed using a limited number of butterfly units. The folding transformation method is illustrated in Fig. 3. This explains that edge e produces some delay content $D(c)$ among the weight W from origin end A to target end B.

The equivalent folding effect is shown in the Fig. 4. The operational unit of the origin end A is S_A to be pipelined through the P_A stage which is required to reach the delay of Eq. 7.

$$G_N(A \rightarrow B) = FD(C) - P_A + b - a \tag{7}$$

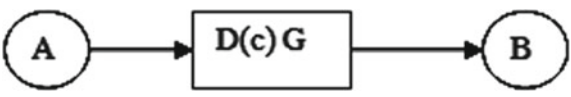


Fig. 3 The folding transformation technique

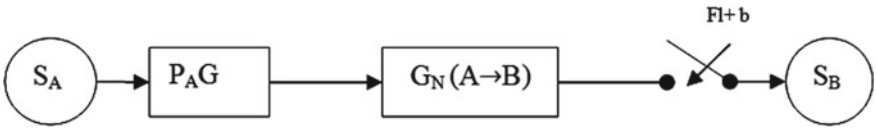


Fig. 4 Folded edge

The edge is switched to the target end B, whose functional unit is S_B exists on the state $Fl + v$, where the term F is a folding factor. The folding factor describes the amount regarding algorithmic processes that can be performed or completed through any individual operational unit upon the hardware, where u and v denote the folding orders of the U and V ends. The folding order is the period in which a point is listed to perform in hardware. The arranged operation set that executes the identical operational unit is known as folding set T. Every folding set holds F listings, some may concern as invalid [11]. To have a fully folded system, all edges of the data flow graph (DFG) must be taken.

For example, the process can be described using 8-point DIF FFT corresponding DFG as shown in Fig. 5. The graph is divided into three stages; every stage includes a set of butterflies and multiplier.

Consider the folding sets for $T = 8$ with the folding order 4.

$$A = \{\phi, \phi, \phi, \phi, A_0, A_1, A_2, A_3\}$$

$$B = \{B_2, B_3, \phi, \phi, \phi, \phi, B_0, B_1\}$$

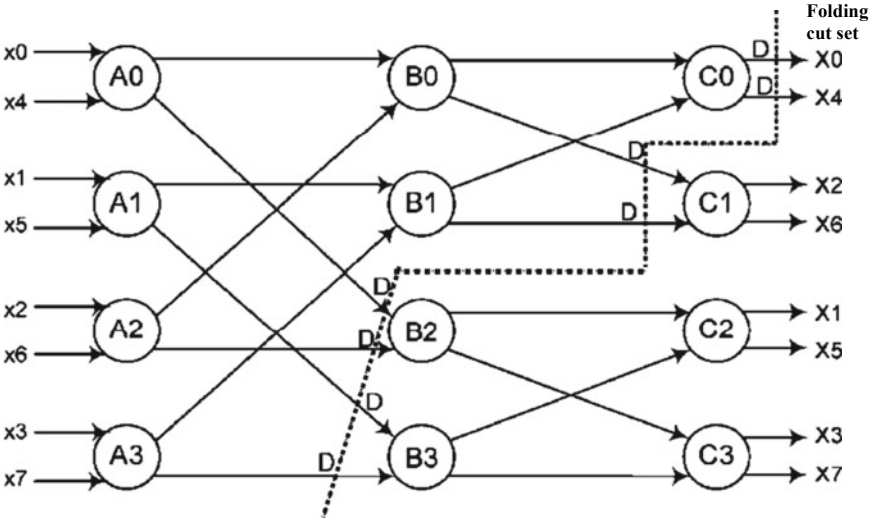


Fig. 5 8-point DFG for folding

$$C = \{C_1, C_2, C_3, \phi, \phi, \phi, \phi, C_0\}$$

The operational unit performs $A0, A1, A2$, and $A3$ functions at the appropriate time and is idle at null operations. Folding equations are obtained by folding sets with negative delays and non-negative delays. Assume that there are no pipeline stages for butterfly operations, i.e., PA = 0, PB = 0, PC = 0. All the edges of the DFG will get the folded architecture by writing the folding equation in (8).

$$\begin{array}{ll} G_N(A_0 \rightarrow B_0) = 2 & G_N(B_0 \rightarrow C_0) = 1 \\ G_N(A_0 \rightarrow B_2) = -4 & G_N(B_0 \rightarrow C_1) = -6 \\ G_N(A_1 \rightarrow B_1) = 2 & G_N(B_1 \rightarrow C_0) = 0 \\ G_N(A_1 \rightarrow B_3) = -4 & G_N(B_1 \rightarrow C_1) = -7 \\ G_N(A_2 \rightarrow B_0) = 0 & G_N(B_2 \rightarrow C_2) = 1 \\ G_N(A_2 \rightarrow B_2) = -6 & G_N(B_2 \rightarrow C_3) = 2 \\ G_N(A_3 \rightarrow B_1) = 0 & G_N(B_3 \rightarrow C_2) = 0 \\ G_N(A_3 \rightarrow B_3) = -6 & G_N(B_3 \rightarrow C_3) = 1 \end{array} \tag{8}$$

DFG can be piped to ensure that the returned hardware has a non-negative delay. $G_N(A_0 \rightarrow B_0) = 2$, that means there exists an edge from the butterfly node toward node against the folded DFG by two delays. For the folded system to be realistic, $G_N(A \rightarrow B) \geq 0$ must satisfied on all edges of the DFG. Retiming and/or pipelining can be used to perform this property or to determine if the folding sets are impractical [12]. We can recognize a negative delay on some of the edges in Eq. (8). DFG can be pipelined as shown in figure to assure that folded hardware produces a non-negative delay. The pipeline folded delay for DFG is given by displayed equations are centered and set on a separate line.

$$\begin{array}{ll} G_N(A_0 \rightarrow B_0) = 2 & G_N(B_0 \rightarrow C_0) = 1 \\ G_N(A_0 \rightarrow B_2) = 4 & G_N(B_0 \rightarrow C_1) = 2 \\ G_N(A_1 \rightarrow B_1) = 2 & G_N(B_1 \rightarrow C_0) = 0 \\ G_N(A_1 \rightarrow B_3) = 4 & G_N(B_1 \rightarrow C_1) = 1 \\ G_N(A_2 \rightarrow B_0) = 0 & G_N(B_2 \rightarrow C_2) = 1 \\ G_N(A_2 \rightarrow B_2) = 2 & G_N(B_2 \rightarrow C_3) = 2 \\ G_N(A_3 \rightarrow B_1) = 0 & G_N(B_3 \rightarrow C_2) = 0 \\ G_N(A_3 \rightarrow B_3) = 2 & G_N(B_3 \rightarrow C_3) = 1 \end{array} \tag{9}$$

It requires16 registers to integrate these edges into the folded architecture. When true folding sets were determined once, then retiming operation used to perform the function or to decide whether these folding sets remain impractical. The folding of the butterfly networks can be extended over any length of N-points utilized by the FFT to create a more efficient architecture.

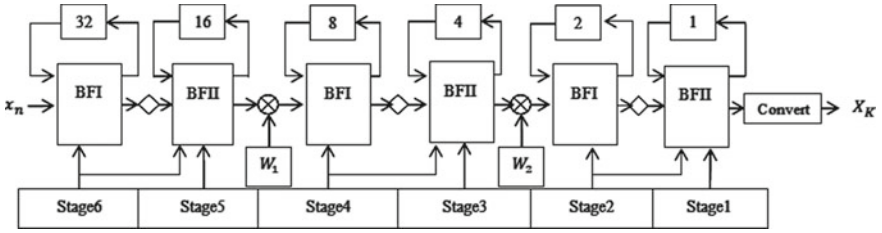


Fig. 6 64-point pipeline architecture

4 Pipeline Implementation

4.1 Architecture Selection

In recent studies, several pipeline architectures are explained [13]. Each pipeline FFT architecture required different features and sources. The resource usage rate provides the computational capability. Pipelined FFT architectures appear to be the primary solution for low latency, high throughput, low power consumption, and small area designs [14, 15]. For decreasing the use of multiplication and addition functions and simplifying the hardware design radix-2^2, FFT algorithm is adopted for implementation. The radix-2^2 algorithm has a similar multiplicative complexity as radix-4, but it retains the radix-2 butterfly structures. Butterflies outputs are connected into first-in-first-out (FIFO) buffers in a feedback loop that provides single-path input and processing of a sample toward every clock cycle [16]. This spatial regularity is a significant architectural advantage over different algorithms if regarding pipeline architecture toward VLSI implementation. The radix-2^2 FFT algorithm not only maintains the simple hardware structure of radix-2 but also uses low calculation. In conjunction with pipelining technology, FPGA implementation makes FFT processors compatible with high speed and efficiency. From the studies, radix-2^2 single path delay feedback (R2^2SDF) architecture is adopted for implementation because it generates high computational efficiency. SDF architecture remains the most attractive and generally accepted architecture because it provides high throughput and requires a less small number of hardware resources [17].

The decomposition of the twiddle factor occurs by using the common factor algorithm; hence, FFT can be reproduced to obtain complete radix-2^2 FFT.

$$X(K_1 + 2K_2 + 4K_3) = \sum_{n_3=0}^{\frac{N}{4}-1} \left(H(K_1, K_2, n_3) W_N^{n_3(K_1+2K_2)} \right) W_{\frac{N}{4}}^{k_3 n_3} \tag{10}$$

(K_1, K_2, K_3) can be expressed as:

$$H(K_1, K_2, n_3) = \underbrace{\left[x(n_3) + (-1)^{k_1} x\left(n_3 + \left(\frac{N}{2}\right)\right)\right]}_{\text{BFI}} + (-j)^{(k_1+2k_2)} \underbrace{\left[x\left(n_3 + \left(\frac{N}{4}\right)\right) + (-1)^{k_1} x\left(n_3 + \left(\frac{3}{4}\right)N\right)\right]}_{\text{BFI}} \quad \text{BFII} \tag{11}$$

BFI and BFII in Eq. 11 are the two butterflies of the first and second columns of the radix-2^2 algorithm that have trivial multiplication in the signal flow graph (SFG) [18].

To achieve trivial multiplication function, it demands constant multipliers and the logic operation provides control signals. The architecture comprises a commutator, butterfly, and complex multiplier in every stage, and a decrease in multiplicative complexity is one of the benefits. In each stage, the pipelined registers are added as part of the design to avoid long critical path delays. Clock input is provided to all the stages at the same time. Figure 6 shows the 64-point pipeline architecture. The symbol $\otimes$ represents nontrivial multiplication and trivial multiplication depicted in a diamond shape where the twiddle factor component comprises only real-imaginary data transferring and sign conversion.

4.2 Architecture via Folding

The 64-point FFT consists of four stages with a feedback structure based on SDF architecture. The power consumption of an FFT occurs in two significant areas; in the BCU and the register for internal data storage. In this design, the power consumption in those two areas can overcome by applying the folding technique by reducing the usage of butterfly operation. The folding transformation method is applied to DFG by deriving the pipeline architecture of the FFT. Folding can be applied in between each node and the folding set is determined manually based on simple observations described in Sect. 3. In our design folding technique is applied in between each node of DFG only in the last three stages of 64-point FFT. A set of ordered operations which is the same functional unit is needed for modifying the DFG, i.e., folding set. Every set comprises F approaches; few sets exist as invalid. Therefore, the number of folded sections is taken as a single operational section. The execution of the operational unit performs the process at the jth point [which belongs to $0 - (F - 1)$] of the folding set at the time of partition. This term folding order implies the time occurrences were each point is listed to execute on the hardware.

Using folding techniques, multiple butterflies within a similar column are usually mapped to an individual butterfly unit. That results in the effective usage of the chip area because the identical hardware is utilized for various butterfly operations. Folding sets are produced instinctively to overcome computing time and the usage of storage components also decreased. The DFG has real and imaginary data paths.

The folding approach is used to optimize the data path through identify the exact butterflies in the flow graph. The flow graph of the 64-point FFT using the folding technique is shown in Fig. 7.

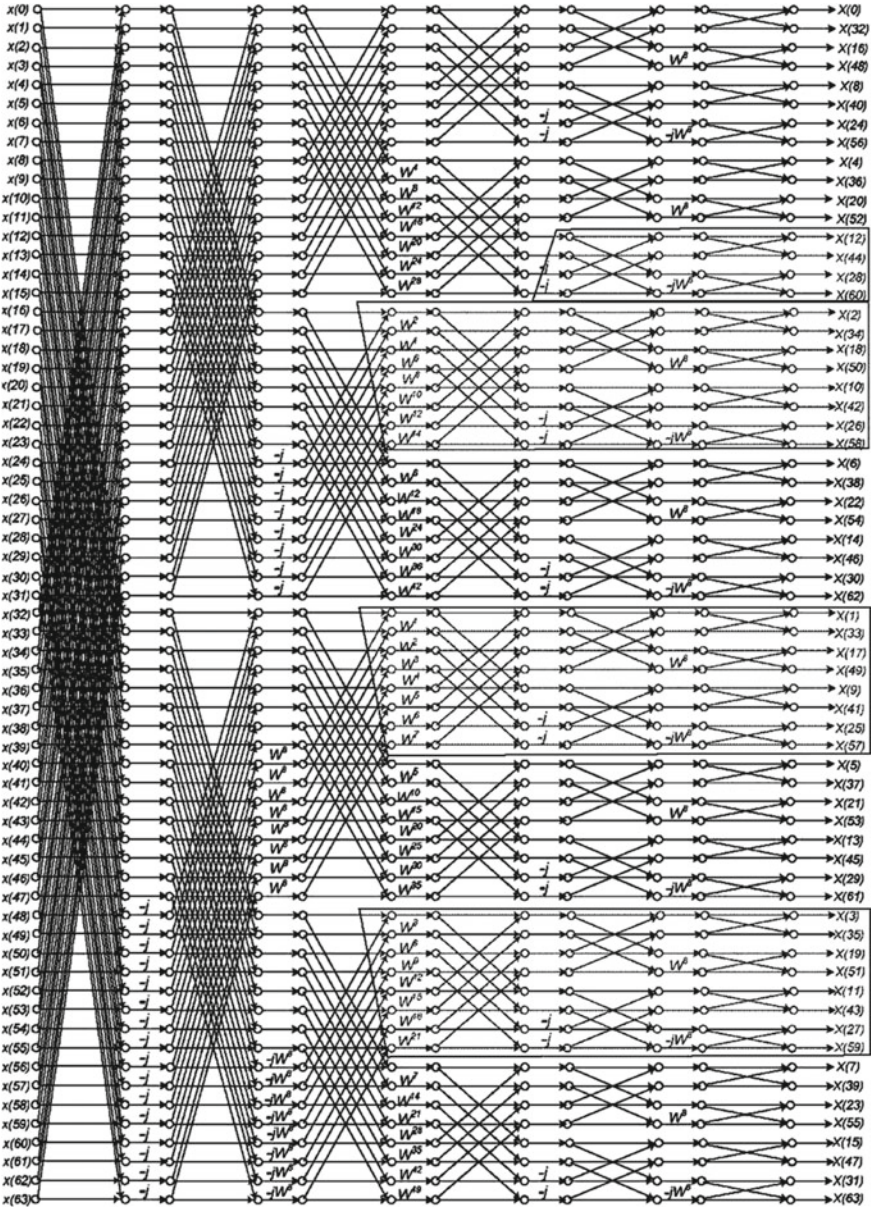


Fig. 7 Flow graph of 64-point folding FFT

5 Result and Discussion

This project design is usually based on design and testing. The 64-point optimized pipeline FFT is implemented using a folding transformation technique is proposed. The pipelined FFT modules and sub-modules were designed based on the VHDL description. VHDL stands as VHSIC (very-high-speed integrated circuit) hardware description language, does usually applied as a design approach language toward FPGA and ASIC devices. The ISE software is used for synthesizing and simulation of VHDL codes. The implementation of the design is recognized by Xilinx Vertex 6 FPGA, and the simulation is performed on ISE Design Suite 14.7 simulator. FPGA has the processing power for handling high-speed DSP.

Every FFT algorithms commonly share the same memory architecture for the design. Pre-computed twiddle factors and the following features are stored in ROM; FFT size, Fixed-point arithmetic, memory size and addressing, twiddle factors length, and word length. A read-only memory (ROM) is connected to the FFT module which is stored by input data $X(n)$ in .txt or .dat file. ROM provides signal input data to FFT modules within the period clock cycle that depends upon the number of FFT points. The computation of the FFT can occur in four stages. Each stage is pipelined to the next stage. After completing one stage, the output of the previous stage is used as an input to the next stage by swapping the memory address. The architecture is analyzed for its power, area, and timing.

If errors occur, the FFT modifies the modules or their sub-modules on by synthesis. Once the simulation result has been confirmed, these Verilog coding will be download into the FPGA for further testing and performance analysis. In every FFT, butterfly operation is the main unit on which to determine the speed of the whole process. From the simulation, the inputs and outputs are usually displayed in waves. Using the test bench code, simulations were carried out for the design to validate the behavioral description. The simulation waveform is depicted in Fig. 8.

The RTL of the proposed distributed algorithm based radix-22 64 point FFT processor is shown in Fig. 9. The device utilization while simulated at Virtex 6 FPGA, it is recognized that it outlines the FFT structure to LUTs, multipliers, registers, clock buffers, IO buffers, flip-flops/latches, adder/Subtractor as well as IO bounds. The utilization parameters are tabulated in Table 1. The memory usage of the device is about 468 Mb.

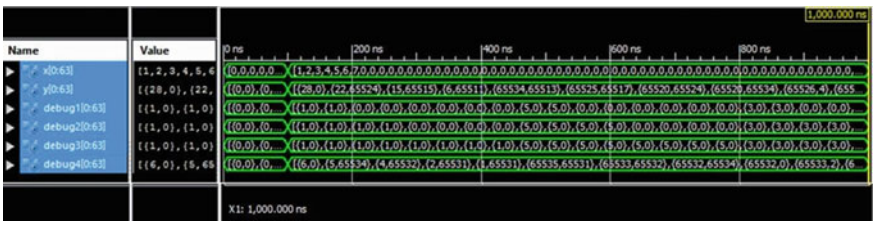


Fig. 8 Simulated output waveform

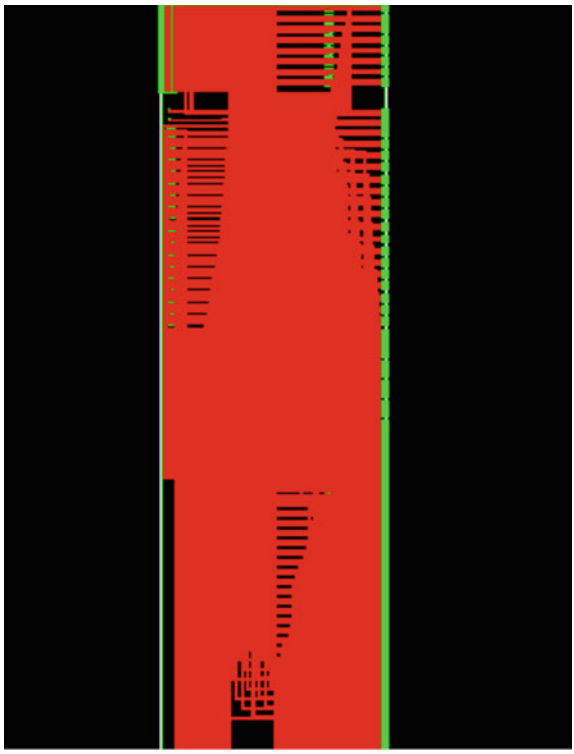


Fig. 9 RTL diagram of 64-point FFT

Table 1 Device utilization of 64-point FFT

Logic utilization	Quantity used	Utilization (%)
LUT-FF pair	3683	41
Clock buffers	1	6
IO buffers	57	14
Flip-flops/latches	4183	4
Multipliers	234	
Adders/subtractors	182	
Selected device	6slx75fgg676-3	

The delay analysis is obtained from timing summary. The proposed 64-point FFT algorithm achieves a time period required is about 12.509 ns with maximum frequency of 79.940 MHz. From the timing report, there is no delay path in this design. Moreover, the power analysis of this design is achieved by using the Xpower analyzer. The power namely the clock, signal, IO, logic and dynamic power obtained from the Xpower analyzer is shown in Fig. 10. The dynamic power dissipation of the system is 0.001 W, and leakage power is about 0.064 W.

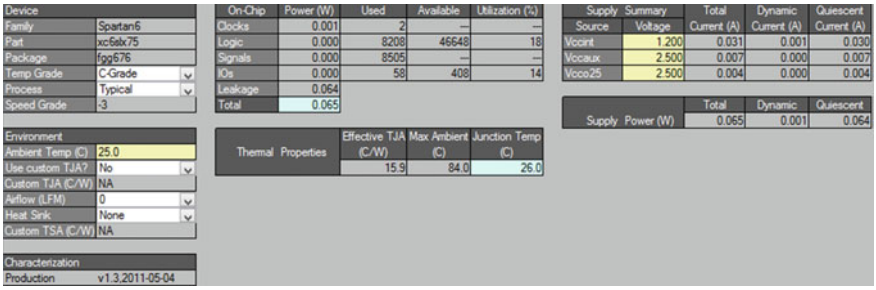


Fig. 10 Power analysis result

Table 2 Performance analysis of 64-point fft design using different algorithm

Processor	Power (mW)	Frequency (MHz)	Delay (ns)
Suganya [19]	852	53.143	25.538
Malashri [20]	121	–	13.762
Dali [21]	243	52.72	–
Proposed	65	79.940	12.509

The proposed implementation compares with the existing FFT architecture is tabulated in Table 2. The maximum speed can be obtained by maximizing the frequency, i.e., speed is directly proportional to frequency. The proposed system can perform at a very high frequency compared to other systems. The frequency of the proposed system is 79.940 MHz which is the maximum. Hence, the speed of the system is increased.

Power consumption depends on the architecture design and number of factors such as clock frequency, switching activity rates, etc. By comparing with other systems, the proposed system consumes less power.

6 Conclusion

This paper makes an effort of implementing the folding transformation technique to the pipelined FFT architecture for a 64-point FFT. Efficient speed optimized architecture for the computation of FFT has been proposed for a given algorithm in this paper. The design is coded toward VHDL and the implementation of the architecture was achieved in Virtex 6 FPGA, and its simulation is performed by the Xilinx ISE Design Suite 14.7 simulator. The design results in high speed and optimized delay. Those folding structures remain ideal applications on implantable or portable devices due to their high speed and low space. Therefore, our architecture represents the best solution for applications implemented by FPGAs.

As a future scope to this, the design can be implemented with other technologies and can be implemented for larger point FFT with full hardware utilization.

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Optimization of Antenna Parameters Using Neural Network Technique for Terahertz Band Applications

Anurag K. Kumar, Medhavi Kirti, Shuchishmita Pani, and Sanjeev Saxena

1 Introduction

As the world is going wireless at a really fast pace, new technology and systems are in place to make the communication viable and efficient. A device is said to be an antenna if it is capable of radiating electromagnetic waves in a desired direction. It is said to be the basic unit of the wireless communication system. Microstrip patch antenna (MPA) is an antenna type which is very commonly used. MPA is designed such that it contains a patch etched on a dielectric substrate which is grounded [1]. The patch can be etched in many shapes such as square, circular, rectangular and triangular. MPA exhibits various characteristics, such as lightweight, cost-effective, low profile, low radiation loss and compact in size, has a large bandwidth and has no complex fabrication processes [2]. These properties allow MPA to be used in portable devices, satellite receivers, sensors, mobile communication systems, detectors etc. There are various bands in which MPA can operate in, but we will be studying its operation in the THF band. According to International Telecommunications Union (ITU), frequencies from 0.3 to 3 THz are considered to be in the range of tremendously high frequency (THF) band [3]. The wavelength of this band is in the range of 1–0.1 mm. Terahertz band lies between the microwave and infrared bands according to the

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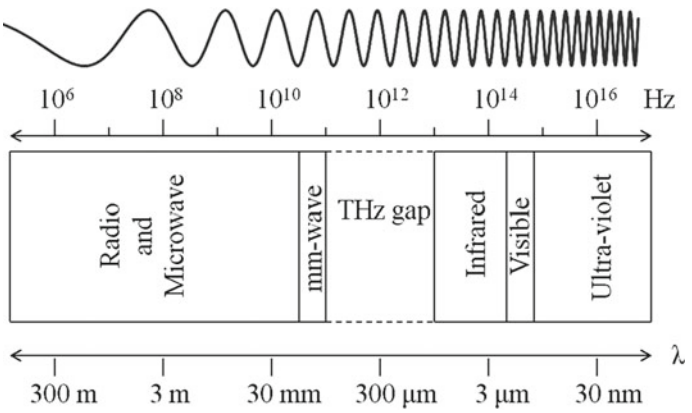

Fig. 1 Electromagnetic spectrum

electromagnetic spectrum. Imaging, spectroscopy and communication are various applications that utilizes terahertz radiation [4].

- Imaging: Terahertz radiation is used in biomedical imaging. The human tissues can be penetrated up to a few millimeters using these radiations. As a result, these radiations are used for medical imaging where diagnoses take place on the surface of the body such as skin, mouth, detection of breast cancer and imaging in dental care.
- Spectroscopy: It is a technique to find the properties of materials and understand their characteristics in the electromagnetic spectrum. Study of properties of absorption of various materials such as single crystal, microcrystal and other organic molecules is done using terahertz spectroscopy.
- Communication: In future, the wireless communication may use T-rays as bandwidth for data transmission. The other applications in communication world related to terahertz radiation exist in high altitudes such as aircraft to satellite or satellite to satellite (Fig. 1).

The effects of these radiations on human body are reported in various papers by various researchers [5–7]. This paper tries to reduce these effects by reducing the SAR value of the MPA. Specific absorption rate (SAR) measures the amount of transmitted energy absorbed by human tissue. International Commission on Non-Ionizing Radiation Protection (ICNIRP) has recommended an SAR value of 0.4 W/kg for occupational exposure and 0.08 W/kg for exposure on the public in general for the frequency range of (0.006–0.3 THz) [8]. Not much research has been done beyond this range on recommending the limits of SAR value, but this paper will make an effort to reduce the SAR value as low as possible. Many researchers have already published their work on terahertz applications, but they have discovered many design constraints which are to be focused upon. Since the resonant frequency is inversely proportional to the length of patch, i.e., antennas smaller in size operate in higher frequency and vice versa, for the antenna to radiate in THz region, the antenna

dimensions are in the nanometer range which requires very precise and complex fabrication process which leads to high cost of the designed antenna [9–11].

Communication devices are getting smaller and smaller in size without compromising on its performance. Antennas play a very important role as they can occupy less space and are able to radiate at various frequency bands. The shape and size of the antenna can be optimized which can further optimize its parameters such as gain, directivity and efficiency. A dataset was created containing input parameters as resonant frequency of the antenna (f), dielectric constant of the substrate in which the patch is etched (ε) and height of the dielectric substrate (h) and output parameters as dimensions of the patch, i.e., length of the patch (l) and width of the patch (w) which can be calculated [12]. Artificial neural network (ANN) is used for optimization. It is very fast and requires lesser efforts as compared to other data processing models. Using ANN, a particular algorithm can resolve a dataset which is big in size in a short duration of time by applying minimum efforts. Levenberg–Marquardt back-propagation algorithm was used to train dataset containing the antenna dimensions as it is fast in convergence and gives accurate predictions of the outputs, but it takes a lot of memory space [13]. Neural network was created using nn-tool in MATLAB R2018a software.

1.1 Rectangular Microstrip Patch Antenna

It is the most basic patch antenna with a patch on one side which radiates electromagnetic waves and a ground plane on the other side [14]. Dielectric material is used for substrate while the patch and ground are conductors (Fig. 2).

The width of the patch is calculated as:

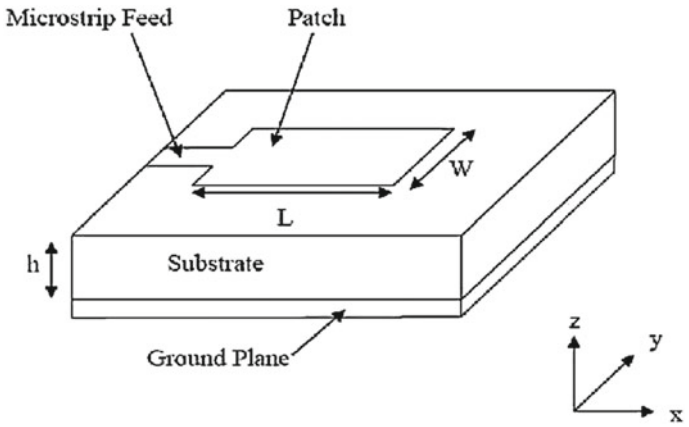

Fig. 2 Basic diagram of a rectangular microstrip patch antenna

$$w = c/\left(2f_{\mathrm{r}} * \left(\sqrt{(\varepsilon_{\mathrm{r}} + 1)/2}\right)\right) \tag{1}$$

where w is width of patch, f_{r} is the resonant frequency, c is the speed of light, ε_{r} is dielectric constant.

Effective dielectric constant ($\varepsilon_{\mathrm{eff}}$) is the ratio of the width to the height of a patch (w/h) in a microstrip patch antenna, as well as the dielectric constant of the substrate (ε_{r}) material. It can be calculated as:

$$\varepsilon_{\mathrm{eff}} = ((\varepsilon_{\mathrm{r}} + 1)/2) + ((\varepsilon_{\mathrm{r}} - 1)/2[1 + 12(h/w)]^{(-1/2)}) \tag{2}$$

Effective length (L_{eff}) is numerically identical in transmission and reception and is calculated as:

$$L_{\mathrm{eff}} = c/\left(2f_{\mathrm{r}} * \left(\sqrt{(\varepsilon_{\mathrm{eff}} + 1)/2}\right)\right) \tag{3}$$

Length extension (ΔL) is calculated as:

$$\Delta L = 0.412h((\varepsilon_{\mathrm{eff}} + 0.3) * (w/h + 0.264))/((\varepsilon_{\mathrm{eff}} - 0.258) * (w/h + 0.8)) \tag{4}$$

Length of antenna can be calculated from the above two equations as:

$$L = L_{\mathrm{eff}} - 2\Delta L \tag{5}$$

1.2 Artificial Neural Network (ANN)

In our human body, all the activities that are performed by our body from sleeping to exercising heavily involves the use of the biological neural network where all the instructions are provided from the brain and executed by the neurons which passes on information from one neuron to the other creating a network of neurons called the neural network. Artificial neural network (ANN) works in quite a similar way in which the biological neural network works. Neuron is the elementary unit of any neural network. Like synapses in a brain, all the neurons are interconnected with each other. The mapping of inputs to the outputs that are desired (also called target outputs) in the neural network is called 'training' of neural networks [15]. A particular algorithm is used by the network to fit in a neural network to obtain the desired outputs.

$$Y = \sum(\text{weight} * \text{input}) + \text{bias} \tag{6}$$

- Input: The values that are given by the user who is operating the neural network is used as input.
- Weight: All the input values are not treated equally in ANN. It is the weight associated with each input that decides if the input value is important enough to alter the output. Each input has a weight value.
- Bias: The neural network requires an activation neuron to kick start its process. This activation neuron is called bias. The value of bias is always 1 and is an extra neuron in the input.

Working of a Single Neuron. An input value and a bias constitute basic structure of a neuron. An input signal received is assigned a weight value which is multiplied together. The product of input signal and the weight is summed up together and added to the bias value [16]. For example, if x is input value and w is weight, output is z and targeted output is y then (Fig. 3),

$$z = x_1 * w_1 + x_2 * w_2 + x_3 * w_3 + \cdots + x_n * w_n + b * 1 \tag{7}$$

$$y = \text{sigmiod}(z) \tag{8}$$

$$\text{sigmoid}(z) = 1/\left(1 + e^{(-z)}\right) \tag{9}$$

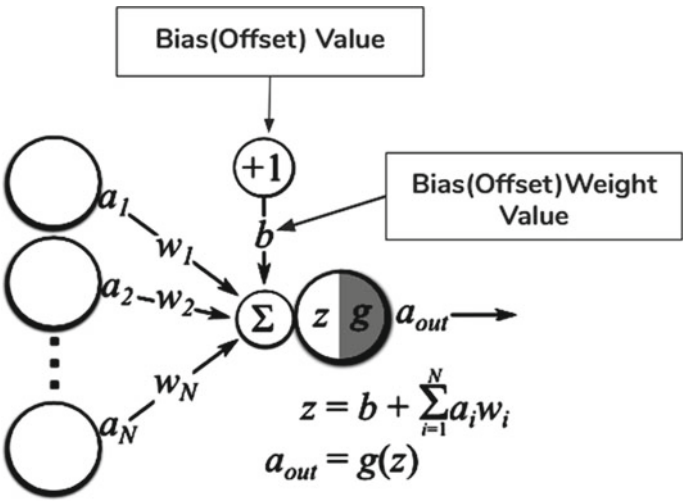

Fig. 3 Working a single neuron

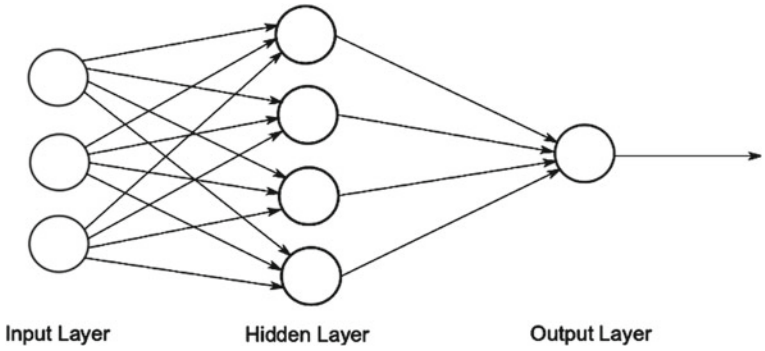

Fig. 4 Structure of an artificial neural network

Connection of Neurons. All the neurons in layer are interconnected to the neurons in the other layer. Values of the weights are updated continuously to reduce error values (Fig. 4).

Input Layer. This layer consists of all the input values and is the first layer in a neural network. Bias and weights are not applied in this layer. No operations take place in this layer. The only function of this layer is to provide input to the next layer.

Hidden Layer. There are various layers in this layer. As the number of hidden layers increases, the result of the training process improves. Each neuron in one layer is connected to every neuron in another layer.

Output Layer. This is the final layer in a neural network which gets input from the hidden layer. All the actual outputs are received from this layer.

Neural Network Tool (nntool) in MATLAB. This tool is widely used by researchers to create and train artificial neural network. Selection of dataset, creation of neural network and its training in MATLAB are done by the neural network tool (nntool). This tool provides with the actual outputs and compares it with the target output to find error values. To ensure that the deviation between actual outputs and target outputs is not large and the performance of the neural network is efficient, data fitting techniques such as mean squared error and regression analysis are used, respectively. The difference between the actual outputs and target outputs is squared. The average of these squared differences is said to the mean squared error (MSE). The lower the MSE, the better. There is no error if the MSE is zero. Regression value gives the extent to which the actual outputs and target outputs are correlated. The actual and the target outputs have a close relationship if the regression value is 1. The actual and the target outputs have a random relationship if the value is closer to 0.

Algorithms that are available in nftool to train ANN In MATLAB:

Levenberg–Marquardt Algorithm. It is formulated for loss function which are in the form of sum of squared errors. This solves the problem that may arise in curve fitting. It is more accurate and precise than Gauss–Newton and gradient descent method. Therefore, it is preferred over the other algorithms. It is an iterative process and minimizes deviation between the actual and target outputs.

Bayesian Regularization. This algorithm is quite similar to Levenberg–Marquardt algorithm as it uses Jacobian matrix in its computations, with the only difference that it provides better results than Levenberg–Marquardt algorithm for larger datasets.

Scaled Conjugate Gradient. For a very large dataset, it is expected that the algorithm does not consume a lot of space and provides good results as well. This situation can be handled well by the scaled conjugate gradient which uses gradient calculations rather than Jacobian calculations to save memory space.

2 Creating Dataset

For microstrip patch antenna, resonant frequency of the antenna (f), dielectric constant of the substrate in which the patch is etched (ε) and height of the dielectric substrate (h) were assumed to be in the range of (0.3 THz $\leq f \leq$ 3 THz), ($\varepsilon_r =$ 10.2, 12.9) and (0.005 mm $\leq h \leq$ 0.3 mm), respectively. A lot of variations were made using the ranges given above to compute the dimensions of the patch, i.e., patch length (l) and patch width (w). Table 1 gives a sample of how the dataset was created. A total of 144 samples were recorded in the dataset.

3 Results and Discussions

3.1 Training Neural Network in MATLAB

The dataset, containing the input and targeted output values, was imported in nntool in MATLAB. This dataset needs to be trained using the neural network. As discussed earlier, data fitting techniques, such as mean squared error and regression analysis, were used to evaluate performance of the neural network. Inputs having the least error between its actual output and target outputs were taken into consideration for simulating an antenna in HFSS. Figure 5 shows the neural network which was created to train the dataset.

Table 1 A sample of the dataset created

Input			Output	
Resonant frequency in THz (f_r)	Dielectric constant (ε_r)	Height in mm (h)	Length in mm (L)	Width in mm (W)
0.3	10.2	0.005	0.158118819	0.213200716
0.3	12.9	0.01	0.13835854	0.18966081
0.3	10.2	0.025	0.150243383	0.211288564
0.3	12.9	0.05	0.120787044	0.18966081
0.3	10.2	0.075	0.124862913	0.211288564
0.3	12.9	0.1	0.095483098	0.18966081
0.3	10.2	0.125	0.099268465	0.211288564
0.3	12.9	0.15	0.071788966	0.18966081
0.3	10.2	0.175	0.075386828	0.211288564
0.3	12.9	0.2	0.049838768	0.18966081
0.3	10.2	0.225	0.039407737	0.18966081
0.3	12.9	0.25	0.042440173	0.211288564
0.3	10.2	0.275	0.032071997	0.211288564
0.3	12.9	0.3	0.009794842	0.18966081

The subsequent data were made in a similar manner

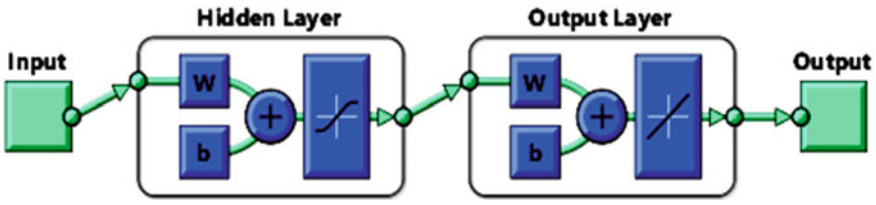

Fig. 5 Neural network in MATLAB

Best Validation Performance. The best validation performance of the neural network is where the iteration of the algorithm stops training the inputs further and gives the least error value, and was found to be at epoch 19 at 2.1207×10^{-5} which is shown in Fig. 6.

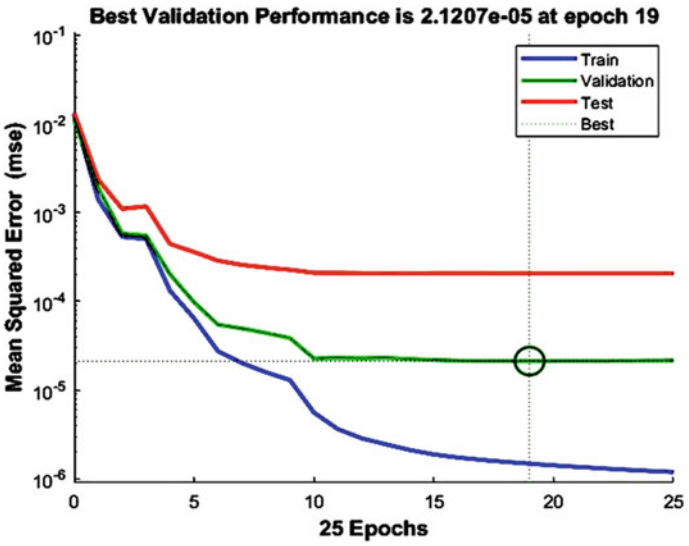

Fig. 6 Training performance of the neural network created in nntool in MATLAB

Performance Regression. The network performance is validated by plotting the regression curve. All the output values including the training, validation and testing sets are plotted. It is said to fit perfectly if the data fall along 45° line where all the targets and outputs are equal. The regression in Fig. 7 is a very good fit where values of R are greater or equal to 0.9627.

Error Histogram. Training data are shown by the blue bar, validation data are shown by green bar, and the testing data are shown by the red bar. An indication of data points which does not fit properly, in fact, the fit is worse with most of the data called outliers, is given by the error histogram. Figure 8 showcases the error histogram after the training of the dataset.

3.2 Results of Antenna Simulation

The simulation of the MPA in HFSS 15 includes a patch etched on a dielectric substrate which is grounded. The aim to design and simulate an MPA radiates in terahertz band and has a high antenna gain and reduced SAR value with optimized dimensions. Table 2 shows the dimensions which gave us the best antenna parameter results.

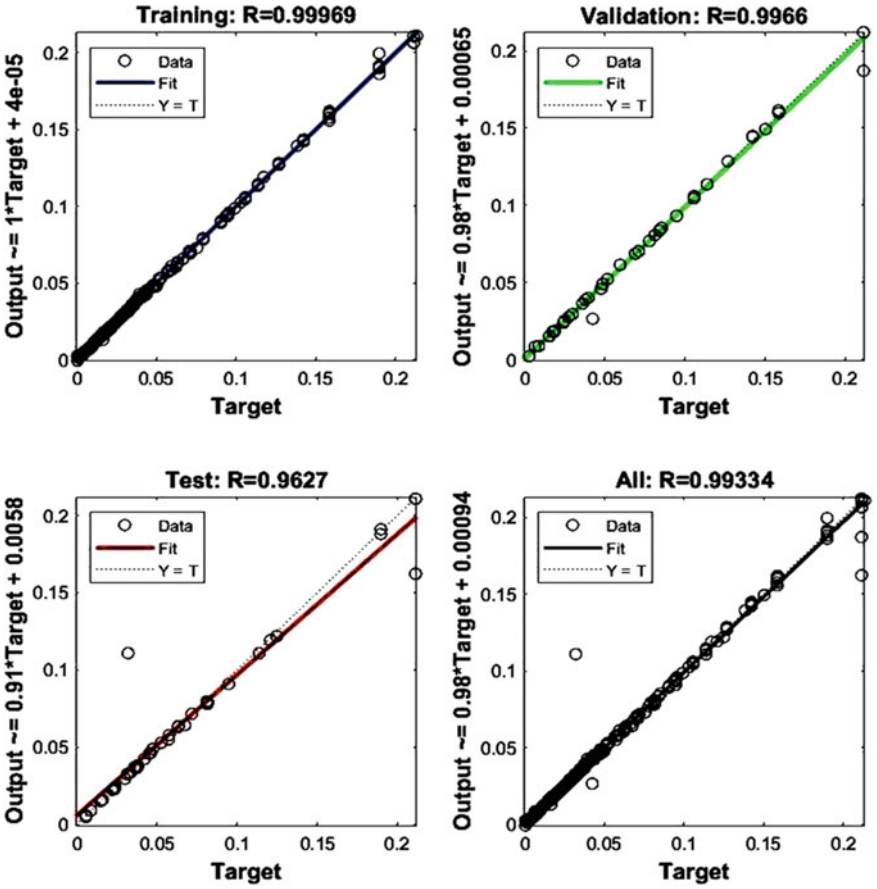

Fig. 7 Performance regression of the neural network created in nntool in MATLAB

Antenna design. Figure 9 shows the design of the antenna. The given designed antenna has the dimensions that are given in Table 3. For better impedance matching and return loss, inset feed was used to design the antenna.

Return loss graph. The return loss S_{11} parameter of the antenna after simulation was discovered to be −23.8963 dB, and bandwidth was calculated to be 0.0793 THz. As shown in Fig. 10, the antenna radiates at 1.7075 THz.

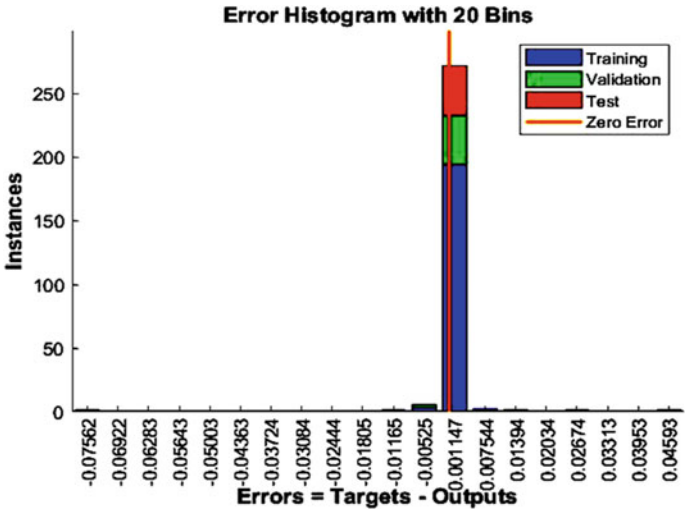

Fig. 8 Error histogram of the neural network created in nntool in MATLAB

Table 2 Parameters with least errors through training the dataset in the nntool in MATLAB

Input parameters	*Values*
Frequency	1.7 THz
Dielectric constant	12.9
Height of substrate	0.01 mm
Output parameters	*Values*
Width of patch	0.020714961 mm
Length of patch	0.033469555 mm

SAR field. Specific absorption rate (SAR) measures the amount of transmitted RF energy absorbed by human tissue. It is a function of mass density of tissue (kg/m^3), electric field induced by radiated energy (V/m) and electrical conductivity (S/m). SAR Field obtained was 0.13264 (W/kg) which is shown in Fig. 11.

Radiation pattern. It is a depiction of the energy distribution that is radiated from the antenna as a function of direction in the form of a diagram. It can be depicted in the form of field pattern or power pattern. Usually radiation pattern is shown in a 3D polar plot as shown in Fig. 12. The radiation pattern shown in Fig. 13 is the 2D version and is obtained by simply dividing the 3D plot in vertical and horizontal pattern. As it can be observed, the antenna gain has the highest value of 5.6202. The pattern can be called an omnidirectional pattern as it radiates in almost every direction, i.e., 0°, 90°, 180° and 270°.

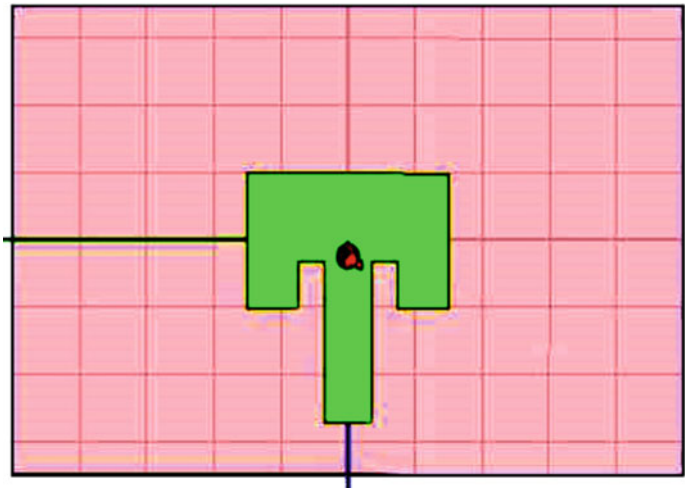

Fig. 9 Antenna designed by applying the most optimized dimensions

Table 3 Antenna dimensions of the proposed design that is to be simulated in HFSS 15.0

Patch dimensions	
Length	0.03 mm
Width	0.02 mm
Substrate dimensions	
Length	0.01 mm
Width	0.07 mm
Height	0.01 mm
Feed dimensions	
Inset distance	0.007 mm
Inset gap	0.004 mm
Feed width	0.007 mm
Feed length	0.024 mm

4 Conclusion

In neural network, actual outputs and targeted outputs are compared after its computation using Levenberg–Marquardt algorithm to find error values for each dataset where the output comprises of the patch dimensions. Antenna patch dimensions with the least error value were chosen as the dimensions of the patch in the antenna in order to optimize it and improve gain as well as reduce the SAR value of the antenna for it to be used in healthcare applications where wireless communication is involved. The antenna designed can radiate at 1.7075 THz with a bandwidth of

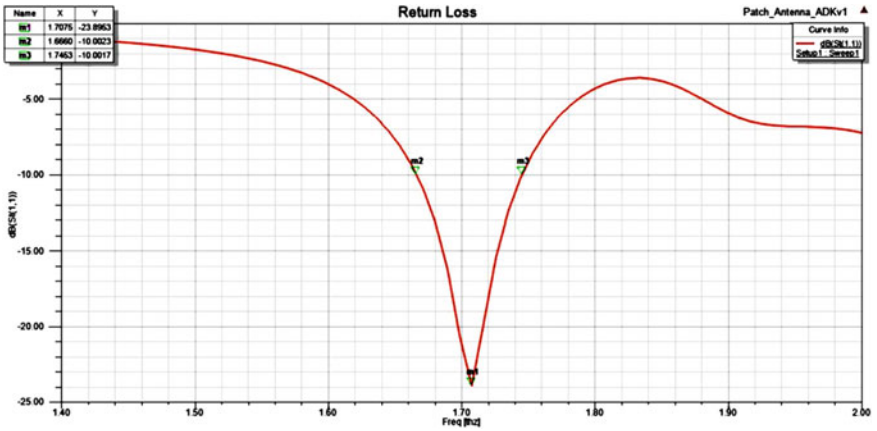

Fig. 10 Return loss graph of the antenna after being simulated

0.0793 THz. The results of the research conducted were compared with the research work of other publishers that is given in the references. Though the constraints in the design proposed in the paper persist, the results in the paper brought it closer to implement cost-effective and less cumbersome fabrication process for antenna to radiate in the terahertz range.

The results can be further improved by using other algorithms to train dataset in the ANN and by designing an antenna that can radiate in terahertz range and can be fabricated using easier processes and lesser cost.

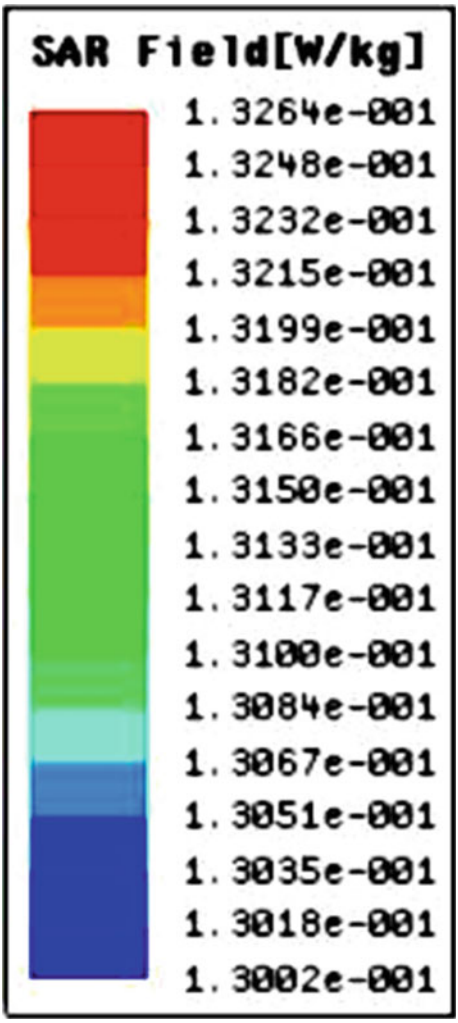

Fig. 11 SAR field of the antenna in HFSS after analysis

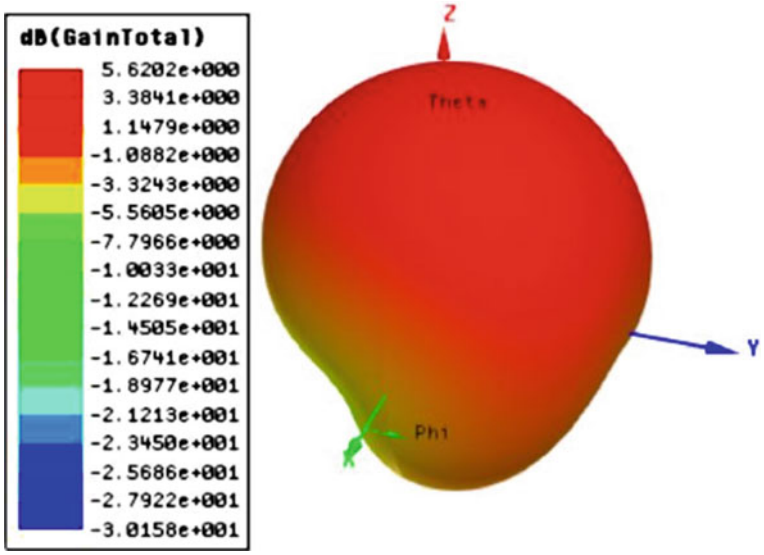

Fig. 12 3-D polar gain plot given by the simulated antenna

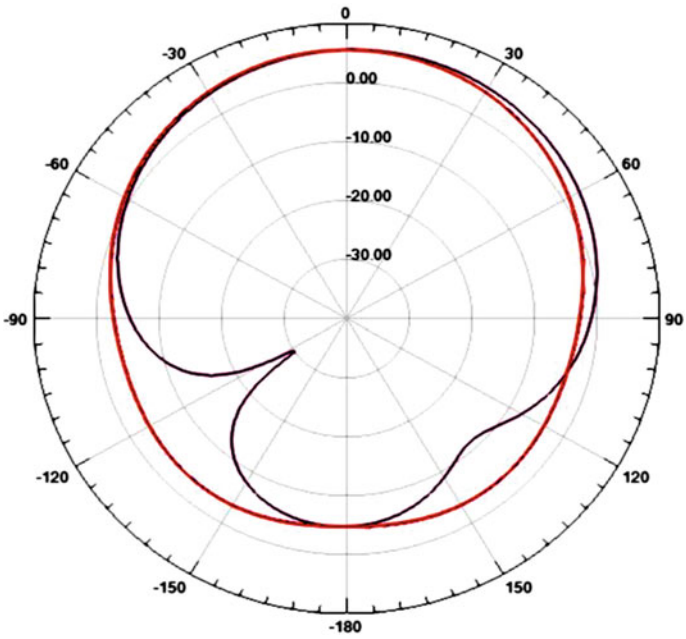

Fig. 13 Radiation pattern in 2D format of the antenna simulated

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BE-Sync: A Bandwidth Efficient Time Synchronization for Underwater Wireless Sensor Networks

Amrita Datta and Mou Dasgupta

1 Introduction

Time synchronization is an essential part of a distributed network for efficient collaboration of sensor nodes and information exchange. It is a well-studied area in terrestrial sensor networks. Unfortunately, time synchronization algorithms that work for terrestrial networks cannot be ported to an underwater environment. When sensor nodes shift around due to waves and water current, delay estimation during two-way message exchange becomes difficult. Also, underwater sensor networks must work with limited bandwidth for information exchange. Network traffic can lead to congestion and packet loss. During instances when a sensor node seeks to synchronize its local time with the network time, the information exchange can lead to congestion in the network in which multiple nodes are exchanging different types of information with each other or with the reference nodes. Coupled with high propagation delay and node mobility, any effort to synchronize the sensor node can face the risk of packet collision and further delays in estimation. This paper proposes a novel time synchronization protocol that uses non-homogenous Poisson process (NHPP)-based back-off technique to synchronize an unsynchronized sensor node by ensuring that available bandwidth is used efficiently. This bandwidth efficient synchronization (BE-Sync) employs NHPP that determines the probability of packet collision in the network and holds off sending the reference time stamps by a reference node to an unsynchronized node if the probability of packet collision is high. This ensures that packets are sent when there is low probability of collision and, therefore, low chance of reference time stamps getting lost. The method further employs outlier removal of reference time stamps received from reference nodes using Mahalanobis distances. Finally, linear regression is employed over the received time stamps to synchronize the local clock with network time.

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The contribution of this paper is twofold. First is the use of NHPP to determine instances of high probability of packet collisions in the network, in which reference time stamps are sent to unsynchronized nodes only when probability of packet collision is low. And second is the use of Mahalanobis distances measure to remove outlier time stamps from the reference nodes leading to higher accuracy in regression estimates.

The rest of the paper is arranged as follows. Section 2 gives a brief overview of the extant literature in time synchronization in underwater, Sect. 3 explains the system model that contains the clock model, network architecture, mobility model the back-off model that employs NHPP, and Mahalanobis distance measure. Section 4 outlines the proposed BE-Sync methodology, and Sect. 5 provides simulation and results. Section 6 concludes the paper.

2 Related Work in Time Synchronization

Time synchronization is an important concern that we need to consider especially for sensor networks. This section provides brief overview of some of the important synchronization protocols.

TSHL is the first time synchronization technique introduced for networks that demonstrate high latency. The time synchronization process is split into two phases for mobile UWSNs in TSHL [1]. The clock skew is estimated in the first phase by nodes. Then skew compensated synchronized messages are swapped in the second phase by the nodes to determine offsets. In the second phase in order to determine the offset, they swap skew compensated synchronization messages within the network. THSL has been designed to handle long propagation delays and energy efficiency at the same time and, hence, ideal for networks with high latency. MU-Sync [2], which is a cluster-based algorithm for UWSNs, avoids frequent resynchronization by estimating both offset and the clock skew. Two linear regressions are performed using local time information. The first regression enables the cluster head to determine the effect of the long duration of propagation delay and the estimate of offset, and skew is obtained from the second regression. The cluster-based nature of MU-sync enables it to be applied to mobile UWSNs employing multi-hop architecture. In MC-Sync [3], two mobile reference nodes are used to estimate node mobility. The MC-Sync is not energy efficient when compared to MU-Sync as it does not allow the reference nodes to broadcast the synchronization messages. Mobi-Sync estimates long dynamic propagation delay by considering the spatial correlation in patterns in the movements of mobile nodes. The time synchronization in Mobi-Sync [4, 5] is achieved in three stages starting with delay estimation, then linear regression, and, finally, terminating with calibration. The application of Doppler shift enabled time synchronization protocol for UWSNs first appeared in D-Sync. D-Sync [6] improves upon propagation delay and synchronization by estimating and compensating for the Doppler shift. A pairwise time synchronization approach across layers for UWSNs is proposed in DA-Sync [7] that stands Doppler assisted time synchronization. The

DA-Sync takes into account the skew while estimating mobility led Doppler shift in UWSNs. Kalman filter is employed to refine the estimate of relative velocity and enhance accuracy of time synchronization. E^2DTS [8] is a time synchronization algorithm proposed for UWSNs which is energy efficient and based on a distributed architecture. E^2DTS algorithm is applicable for time synchronization under conditions of node mobility. RSUN [9] or robust synchronization for underwater networks takes packet collision into account which is mostly ignored in time synchronization protocols. Low bandwidth and high network traffic in UWSNs could lead to packet collisions and data loss, and hence, proper back-off technique needs to be applied before the time synchronization process begins. DE-Sync [10] ensures time synchronization with high degree of accuracy by considering clock skew while determining Doppler scaling factor and not considering sound speed which is determined by many physical and chemical properties of underwater environment.

3 System Model

3.1 Clock Model

Consider a set of nodes whose clocks have a certain skew and drift as compared to the reference clock.

$$N(t) = \alpha_n(t) + \beta_n \tag{1}$$

where $N(t)$ is a vector of local times with respect to the reference time t and α_n and β_n are the skew and offset for a set of n nodes in a cuboids' of dimensions $a \times b \times c$. The rate at which a clock runs relative to a reference frequency is known as clock skew. The time difference between the local and reference clock is called clock offset.

3.2 Network Architecture

Consider a UWSN deployment with a certain number of ordinary nodes and anchor nodes (reference nodes). The anchor nodes are self-synchronized and perform multiple tasks of information communication, localization, time synchronization, maintaining routing tables, acting as reference clocks, etc. They have high computation power and are much fewer in number as compared to normal nodes. These anchor nodes are in regular communication with the sink nodes that float on water surface. The sink nodes are equipped with GPS, acoustic, and radio transceivers. The normal nodes are numerous and spread out to detect events of interest. They generally remain passive to conserve energy and become active when something happens in their vicinity. Also, water currents make them mobile and their positions changes frequently in the XY plane. The local times in these nodes become unsynchronized over a period.

3.3 Mobility Model

Our protocol assumes that all nodes move around due to water currents. Hence to model the node mobility, we employ a cointegrated random motion-based technique drawn from a normal distribution. We assume that reference nodes and unsynchronized nodes both move in the same underwater environment, and hence, even if they do not move in lock step with each other, their movements are cointegrated. For example, a water current or a wave would tend to move both unsynchronized nodes and reference nodes in the same relative direction even though the magnitude and direction of movement may not be an exact match. Figure 1 shows one such instance as an example.

Here we have purposefully generated two separate cointegrated random motion, one each for the anchor node and unsynchronized node, whose randomness is centered around a standard normal distribution defined by mean 0 and variance 1. The trajectories of freely moving reference nodes and unsynchronized nodes are obtained over a period of time.

3.4 Back-Off Model

Underwater sensor network communication faces bandwidth constraints. The method proposed in this paper uses a time synchronization method that uses two-way communication between reference node and unsynchronized node. Whenever such two-way communication is initiated, there is a probability that available bandwidth might get clogged as many types of communication takes place in the underwater environment among sensor nodes apart from time synchronization-related communication.

The proposed algorithm ensures that message communication between reference nodes and unsynchronized nodes occur only when there is minimum probability of packet collision due to constrained bandwidth, and their packets do not get lost or dropped. The nodes in the proposed protocol employ a back-off method using

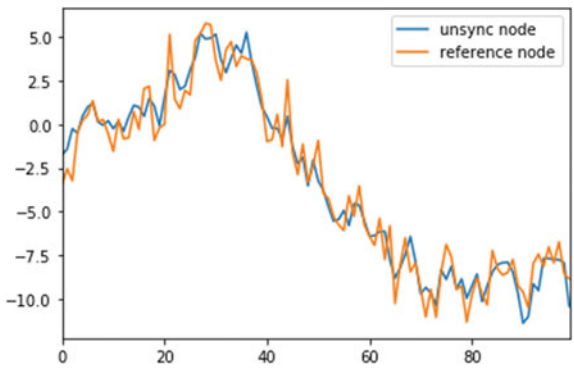

Fig. 1 Gaussian distribution-based mobility model

non-homogenous Poisson process to model this period of wait before resending the reference packet.

A Poisson process is a model for a series of discrete events where the average time between events is exponentially distributed and is known, but the exact occurrence time of the event is not known. A non-homogenous Poisson process (NHPP) is one where even the average time between the events is not known.

A NHPP, $N(\cdot)$ has the following properties -

- The occurrence of a collision event is independent of any occurrence before it. The number of collision events in a given time interval $(t, t + \Delta t)$ depends on the current time and the length of the time interval Δt.
- The rate of collision events is given by Eq. 2

$$P[\text{ exactly one event in}(t, t + \Delta t)] = P[N(t, t + \Delta t) - N(t) = 1] = \lambda(t)\Delta t + \varrho(\Delta t) \tag{2}$$

  where $\lambda(t)$ is the rate function or the intensity function.
- For a very small Δt, such that $\Delta t \to 0$, the probability of more than one packet collision is negligible.
- $N(0) = 0$ at $t = 0$. At $t = 0$, there are no packet collision events.

On the basis of above assumptions, the probability of n packet collision in a given duration of time is given by Eq. 3

$$P[\ N(t) = n] = \frac{\int_0^t \lambda(t)\mathrm{d}t}{n!} * e^{-\int_0^t \lambda(t)\mathrm{d}t} \tag{3}$$

In a UWSN, it is quite possible that it is not known when packet collision might occur and the frequency with which packet collision might occur. We may have a scenario where incidences of packet collision are spaced far apart or spaced close to one another. Thus, average time between collisions is not deterministic and better approximates the real conditions in a UWSN.

We begin with a homogenous Poisson process assuming the average time between two collision is known and follows an exponential distribution. Then we use Lewis and Shedler 1979s "thinning" algorithm [11] to approximate a non-homogenous Poisson process as follows

- Take a NHPP $N(t)$ and generate points within time interval $[0, 1]$ with a rate function $\lambda(t)$.
  - This rate function (also known as intensity function) denotes the rate at which the packet collision happens is assumed to be exponential, and its functional form is decided by the network architect.
  - In the proposed algorithm, the rate function is of the form $\lambda(t) = 100 * e^{-(x^2+y^2)}$

    The abscissa (x-axis) denotes the occurrence of the event at any time within the interval, and ordinate (y-axis) denotes the probability of occurrence and has a density function.
    The unit of time is set by the network architect in advance.

The unit can range from a nanosecond to a second. The paper assumes a unit of microseconds (10^{-6} s).

- Let n be the number of packet collision events that can happen between $t = 0$ to $t = 1$ and $S(n)$ be the time of most recent packet collision event.
- At $t = 0$, the NHPP process is initialized and generates points in the time interval $[0, 1]$ such that $U_1 \sim Uniform(0, 1)$.
- Set $t = t - \frac{lnU_1}{\bar{\lambda}}$.
  - $\bar{\lambda}$ is such that $\bar{\lambda} \geq \lambda t$.
  - Calculate thinning probability $p(t) = \frac{\lambda t}{\bar{\lambda}}$.
    - In thinning, packet collision and no packet collision are two separate Poisson processes. The algorithm rejects no packet collision and, hence, "thins" the distribution to only packet collision events.
  - Generate $U_2 \sim Uniform(0, 1)$ independent of U_1.
  - If $U_2 < p(t)$, set $n = n + 1$ and $S(n) = t$.
  - Continue generating till $t = 1$.

Once the probability of packet collision events is determined within the next set time duration, the reference node chooses to broadcast the reference time packets when probability of packet collision is minimum.

3.5 Mahalanobis Distances

A strong local transient current can affect some nodes for a short duration of time making them move in a particular direction. In such a scenario, subsequent time stamps would be affected due to large errors creeping in due to propagation delay. Also since only a subset of nodes might get affected, errors might have a correlation structure. This needs to be rectified.

Once all time stamps are received, the anchor nodes calculate Mahalanobis distances to identify leveraged and influential outliers in the data that might affect regression output. This ensures that any outliers that might affect the fit of a regression are removed. In Mahalanobis distance measure, the distance of a point from a distribution is calculated. From a computation standpoint, the columns are transformed into uncorrelated variables followed by variance scaling to 1. Finally, Euclidean distance is calculated between a point and the distribution. The formula for Mahalanobis distance [12] is given by Eq. 4-

$$D^2 = (x - m)^T * C^{-1} * (x - m) \tag{4}$$

where D^2 is the square of the Mahalanobis distance, x represents the rows (observations) in a dataset, m is the mean of each column, and C^{-1} is the inverse covariance matrix. Here, on the right hand side, the first term $(x - m)$ gives the distance of

the observation x from the mean m and multiplied by the inverse of the covariance matrix C. If the observations are highly correlated, then covariance would be high, and $(x - m)$ term would be divided by a higher number; if the correlation is low, then covariance would be low and the $(x - m)$ term would be divided by a smaller number. Thus, the covariance matrix acts as a scaling factor.

3.6 Linear Regression

Ordinary least squares (OLS) is a widely used technique in underwater time synchronization protocols. OLS is run over the data points that are received and corrected using Mahalanobis distances to estimate the clock skew and clock offset. OLS fits a line through the datapoints in a way to minimize the sum of squared errors.

4 Details of Proposed Methodology

4.1 Overview of BE-Sync

BE-Sync follows pairwise synchronization approach for estimating the clock offset and clock skew. BE-Sync consists of three main steps: first, there is message exchange between reference node and unsynchronized (ordinary) node with proper back-off model in place to reduce the probability of packet collision, second, where it is ensured that received timestamps are analyzed to identify and eliminate inconsistent timestamps and, finally, estimate the clock skew and offset.

4.2 Impact of Collision and Message Exchange of BE-Sync

In BE-Sync, we assume that the propagation delays for each information exchange are the same. Consider a reference node $\mathcal{R}$ with standard time is fixed, and node $\mathcal{S}$ is a sensor node to be synchronized. In underwater sensor network, bandwidth comes at a premium. Any given node whether a reference node or otherwise must perform several activities and communicate information within the limited bandwidth allocated to them. If the network is experiencing high traffic, it is prudent that nodes in the network employ a back-off protocol so that packets are not lost, and they do not have to resend again and again.

The proposed protocol uses a back-off model based on NHPP. Consider a scenario when it is time for the reference node to start broadcasting the sync-req message. It could be a time when probability of packet collision is high in the network or it could also be a time that probability is low. The reference node employs back-off

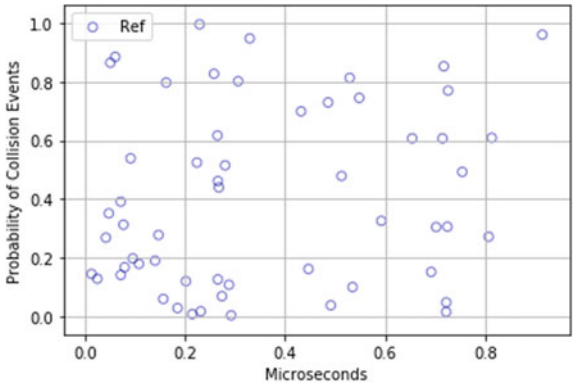

Fig. 2 Probability scatter plot of packet collisions in the next 1 ms for node $\mathcal{R}$

technique to hold off the transmission of reference time packets till probability of packet collision is low.

As evident from the scatter plot Fig. 2, the probability of packet collision is almost 0 at 0.2 and 0.3 ms. Hence, the reference node does not broadcast immediately but waits for atleast 0.2 ms before broadcasting. One point to be noted is that the threshold probability can be set dynamically based on information of past collision events. Also, the choice of time unit is also be changed by the network architect based on application and other preferences. A threshold of 0% packet collision although is most effective, but it gives fewer chances to the reference node to broadcast. If the computation times are high, then this chance that comes after 0.2 ms can be missed, and reference node must recalculate leading to power usage and delay. A threshold set at 20% probability affords about 22 chances to the reference node to broadcast. These instances of low packet collision are spread apart so even if the first instance is missed, the reference node has many more chances. There is always a tradeoff between faster packet transmission and packet collision which must be managed judiciously. In time synchronization algorithms, reference node broadcasts multiple times within a given a time frame. Thus, if it can transmit more within a given window, the unsynchronized node can synchronize its clock earlier too.

Once the appropriate window for packet transmission is estimated, information is transmitted between the reference nodes ($\mathcal{R}$) and the ordinary (unsynchronized) nodes ($\mathcal{S}$). This packet called sync-req message contains time $\mathcal{T}_{\mathcal{R}}^1$, the time stamp, and actual reference time at the time of sending. The ordinary node $\mathcal{S}$ receives the sync-req message and notes the time it received it as $\mathcal{T}_{\mathcal{S}}^1$. Then anchor (reference) node again sends the sync-req message $\mathcal{T}_{\mathcal{R}}^2$, and the ordinary node ($\mathcal{S}$) receives them and notes down the time of receipt $\mathcal{T}_{\mathcal{S}}^2$. This message receipt continues till node ($\mathcal{S}$) has received enough data points (sync-req messages), as shown in Fig. 3.

As Fig. 4 shows, four time stamps are required to calculate the clock offset. The ordinary node ($\mathcal{S}$) sends out a skew synchronized REQ message to the reference node ($\mathcal{R}$) at $\mathcal{T}_1$. The node R receives the message at $\mathcal{T}_2$ and notes it. At $\mathcal{T}_3$, the reference node sends out the REP message which node $\mathcal{S}$ receives at $\mathcal{T}_4$. Multiple

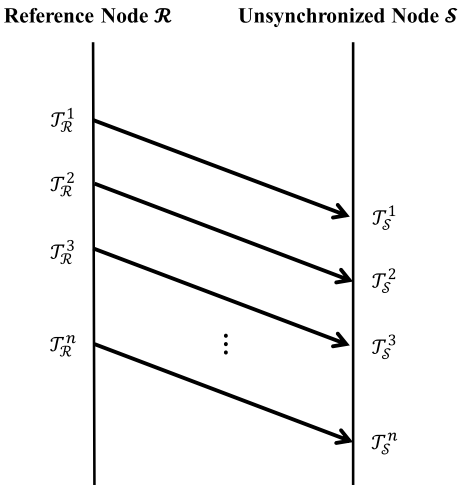

Fig. 3 Set of clock sync request messages

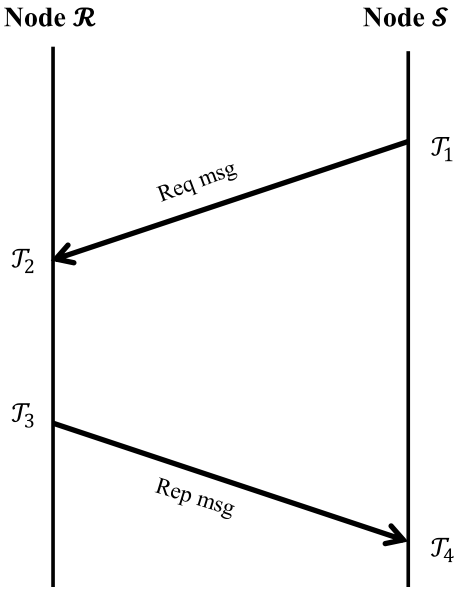

Fig. 4 Two-way message exchange

exchanges like this occur between $\mathcal{R}$ and $\mathcal{S}$, which node $\mathcal{S}$ uses to calculate clock offset. Ideally each exchange cycle described above should generate 4 time stamps for node S. Due to packet collision, it is possible that one or more packets get lost during this bi-directional exchange. Due to packet collision, it is possible that one or more packets get lost during this bi-directional data exchange.

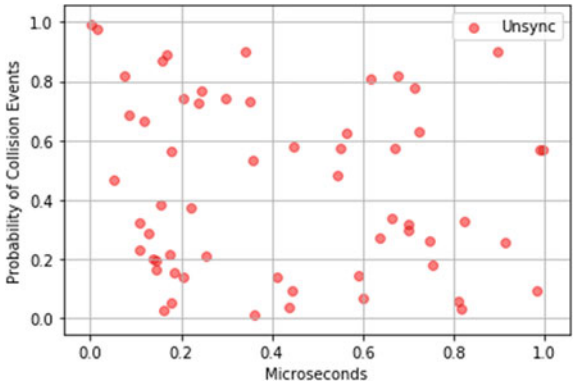

Fig. 5 Probability scatter plot of packet collisions in the next 1 ms for node $\mathcal{S}$

Hence, node $\mathcal{S}$ employs same NHPP-based back-off technique as explained in Sect. 3.4. The least probability for packet collision arises at 0.18 microsecond, 0.38 microsecond, and 0.81 ms. Hence, $\mathcal{S}$ can choose any of these windows to send out the REQ messages.

The node ($\mathcal{S}$) sends out its messages based on lowest probability of packet collision shown in Fig. 5. This ensures that packets are not lost, and offset calculations are accurate. After all packet exchanges are completed, the proposed protocol uses Mahalanobis distance as mentioned in Sect. 3.5 and regression techniques (Sect. 3.6) to synchronize the time of unsynchronized nodes.

5 Performance Evaluation

5.1 Simulation Setup

We assume a cuboidal region of 1000m $\times$ 1000m $\times$ 1000m where several ordinary nodes and anchor (reference) nodes are distributed. They can move as explained earlier under the effect of water currents or waves explained earlier. The speed of sound underwater is assumed to be 1500 m/s. The NHPP calculations to determine the probability of packet collision in the network are made considering a time period of 1 μs described in Sect. 3.4. The reference nodes send the sync-req messages at intervals when the probability of packet collision is lowest, and the same back-off technique is followed by ordinary node when they send the REQ messages. Once the skew and offset adjusted time stamps are received, Mahalanobis distances are calculated and outliers removed before regressions are run.

5.2 Simulation Result

The simulations run 10,000 times in Python Jupyter Notebook on a machine running Intel i7 2 GHz processor and 16 GB RAM. Root mean square error (RMSE) is estimated for determining the rate at which error grows for RSUN [9] and BE-Sync. As evident from Fig. 6, RMSE increases for BE-Sync at a rate lower the RSUN. RMSEs are comparable till 10^3 ms following which the error for RSUN rises rapidly as compared to BE-Sync. While error in BE-Sync rises too, the slope for RSUN is steeper than BE-Sync. Even after 10^7 ms (equivalent to 10 s), the RMSE of BE-Sync is about an order of magnitude lower than the RMSE of RSUN.

We also show how packet collision can affect error after synchronization if not properly factored in. NHPP-based BE-Sync method has superior performance as compared to RSUN and MU-Sync. As probability of packet collision increases in the network shown in Fig. 7, NHPP adjusts for it, and packets are sent only when collision probability is low. Hence, error after synchronization is lower as compared to RSUN [9] and MU-Sync [2]. The error in BE-Sync is at least an order of magnitude lower than RSUN when probability of packet collision is low and three orders of magnitude lower than MU-Sync. As the probability of packet collision increases, the error rate in BE-Sync also increases but remains much lower than either of RSUN or MU-Sync. When we go into scenarios where probability of packet collision is high (0.4 and above), the error rate of BE-Sync does not increase as much, something we do not see in RSUN, and Mu-Sync is anyway has a much higher error rate from the beginning.

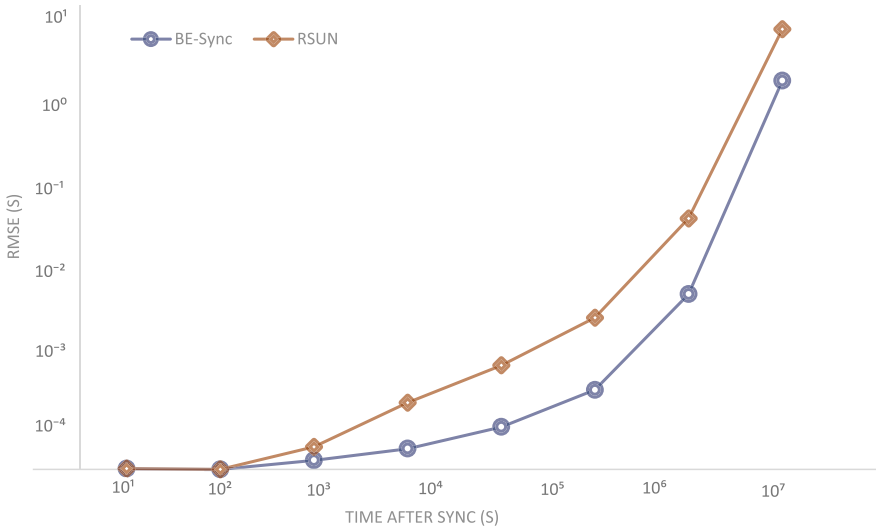

Fig. 6 Root mean square error versus the time elapsed since synchronization

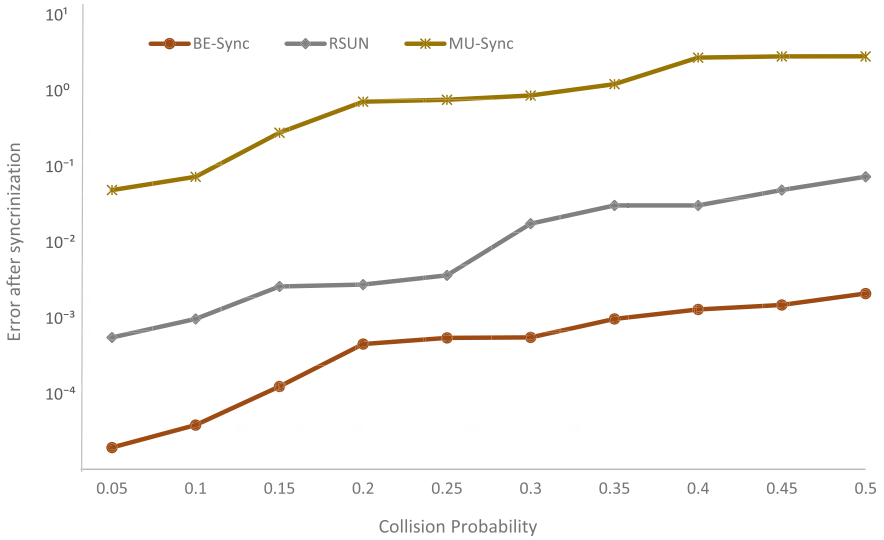

Fig. 7 Effect of collision probability on synchronization accuracy

6 Conclusion and Future Work

In this paper, we have demonstrated that factoring in the probability of packet collision can lead to more efficient time synchronization in underwater sensor networks. We proposed a novel approach to back off using non-homogenous Poisson process. This paper also points out as to why observations can be correlated and propose the use Mahalanobis distance measure to remove time stamps that are outliers and adjust for correlation. The results demonstrate that BE-Sync performs better when compared to RSUN and MU-Sync protocols.

While BE-Sync provides more efficient time synchronization, it does not consider energy efficiency issues. Research in time synchronization algorithms that are also energy optimized is the way forward.

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An Analysis of Analog Performance for High-K Gate Stack Dielectric Pocket Double-Gate-All-Around (DP-DGAA) MOSFET

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1 Introduction

As the world is moving toward smaller and advanced feature gadgets, where ultra large-scale integration ($ULSI$) technology is being extensively used to manufacture them. This technology requires high-performing nano-scale multi-gate (MG) MOSFETs [1–4] as these offer multi-directional control on the channel. Among these MG MOSFETs, gate-all-around (GAA) MOSFET exhibits drastically improved electrostatic controllability over the channel and high immunity toward short channel effects ($SCEs$), offers high packing density, and shows steep subthreshold characteristic [4]. Despite these attractive features, GAA has low drive current and suffered from low computational speed [5]. However, by horizontal/vertical stacking, drive current capability could be improved, but this will decrease the number of devices over the same chip area. To maintain the high drive current and device density, Fahad et al. [6] introduced double-gate-all-around MOS ($DGAA$). The outer ($shell$) gate makes it similar to the GAA, and the inner ($core$) gate provides additional control. These two gates of $DGAA$ control the channel independently and provide superior $SCEs$ immunity and boost the drive current for better speed [6, 7]. In $DGAA$, improved electron mobility can be achieved by decreasing the gap between two gates when the difference between two gates goes down by 4 nm, the volume inversion takes place, and electron mobility gets improved [8]. However, a further boost in the device performance can be achieved by incorporating dielectric pockets (DP) inside the channel region form the source and drain side. This modified MOS structure is

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also known as an insulated-shallow extension (ISE) version of MOS [9]. Incorporation of DP is used to prevent the $SCEs$ and reduce the leakage or OFF-current (I_{OFF}) [9–12]. DP is also termed as a diffusion stopper incorporated in the channel from the source and drain side [13]. Trivedi et al. [9] had worked on ISE technology with a high-K gate stack to enhance the ON-current (I_{ON}) and analog/RF performance. As the extract of the works mentioned above, it can be concluded that the use of DP and high-K insulating material may be beneficial to enhance the $DGAA$ performance.

This work covers the comparative study of two MOSFET structures, $DGAA$ and high-K insulating material DP-$DGAA$. They are evaluated for I_{OFF}, I_{ON}/I_{OFF} ratio, subthreshold swing (SS), drain-induced barrier lowering ($DIBL$), transconductance (g_m), TGF, and other analog characteristics on the $ATLAS$ device simulator.

2 Device Structure and Simulation Details

The three-dimensional ($3D$) structure of the DP-$DGAA$ MOS device for simulation-based investigation is shown in Fig. 1. The cut-plane view of the DP-$DGAA$ MOS device is displayed in Fig. 2. A thin SiO_2 layer wraps the cylindrical channel region with a high-K dielectric (Hfo_2). For the dielectric pocket, SiO_2 has been introduced in the channel region from the source and drain sides. Table 1 represents the DP-$DGAA$ and $DGAA$ devices parameters used for simulation. The following models of $3D$ $ATLAS$ device simulator have been employed to perform the simulation of the proposed DP-$DGAA$ device and $DGAA$ devices [14], such as the drift–diffusion model, field-dependent mobility model, concentration-dependent mobility model, and Shockley-Read-Hall (SRH) model.

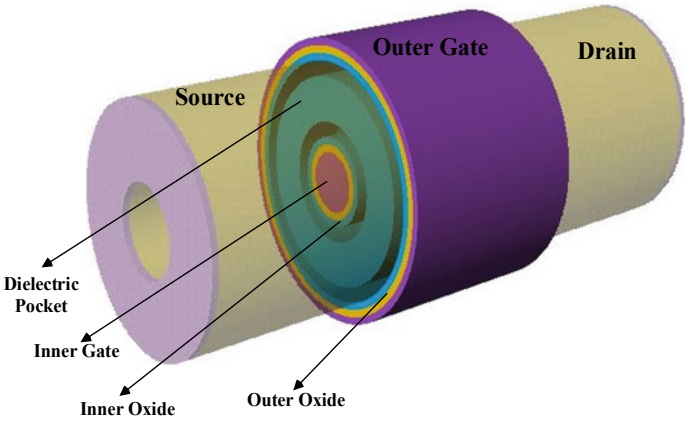

Fig. 1. 3-D structure view of DP-$DGAA$ MOSFET

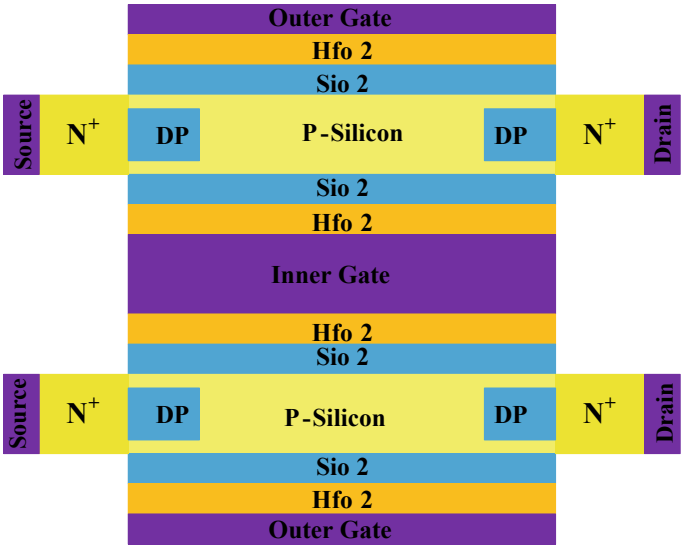

Fig. 2 Cut-plane view of $DP\text{-}DGAA$ MOSFET

Table 1 Physical device parameters used for $DP\text{-}DGAA$ and $DGAA$ MOSFET simulations

Parameters	*DGAA*	*DP-DGAA*
Channel length (L)	20 nm	20 nm
Source/drain doping (N_D)	10^{20} cm^{-3}	10^{20} cm^{-3}
Channel doping (N_A)	10^{15} cm^{-3}	10^{15} cm^{-3}
Oxide (SiO_2) thickness (t_{ox})	2 nm	1 nm
Hafnium oxide (HfO_2) thickness ($t_{high\text{-}K}$)	–	1 nm
Channel thickness (t_{si})	8 nm	8 nm
Inner core metal radius	4 nm	4 nm
Metal work-function (ϕ_M)	4.99 eV	4.8 eV
Dielectric pocket length (DP_L)	–	4 nm
Dielectric pocket thickness (DP_D)	–	4 nm

3 Results and Discussion

Figure 3 displays the contour plot of the electric field for high-K gate stack $DP\text{-}DGAA$ MOSFET at $V_{DS} = 0.5$ V and $V_{GS} = 0$ V. The plot reveals that the electric field is higher at the interface of drain and channel, but it is not strong enough to influence gate leakage current. It is almost dependent on V_{GS}. Figure 4 presents the comparison of drain current of high-K gate stack $DP\text{-}DGAA$ and $DGAA$ MOSFET versus gate-to-source voltage (V_{GS}) at a drain-to-source voltage (V_{DS}) = 1 V. The improvement of I_{ON} and I_{OFF} is found in high-K gate stack $DP\text{-}DGAA$ MOSFET, as presented in

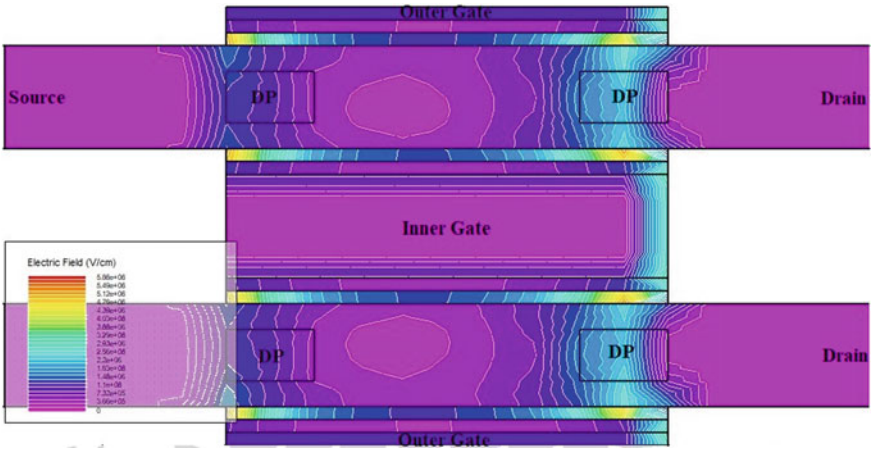

Fig. 3 Horizontal cut-plane view of electric field for $DP\text{-}DGAA$ MOSFET at $V_{GS} = 0$ V and $V_{DS} = 0.5$ V

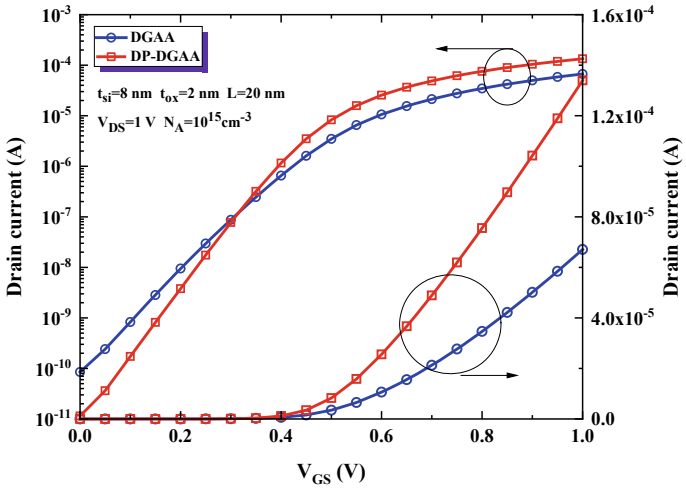

Fig. 4 Comparison of drain current (I_D) of $DP\text{-}DGAA$ and $DGAA$ MOSFET versus V_{GS} at $V_{DS} = 1$ V

Fig. 4. The reduction of OFF-current occurs because of the presence of dielectric pockets (DPs) at the drain-channel and source-channel interfaces as they diminish the charge sharing at both interfaces. The ON-current is enhanced due to high-K dielectric, which increases the electron velocity at the source boundary consequence of enhanced carrier transport capability. The I_{ON}/I_{OFF} ratio is better for the high-K gate insulator material-based $DP\text{-}DGAA$ MOS device than the $DGAA$ device due to the steeper subthreshold slope. Therefore, the high-K gate insulator material-based

$DP\text{-}DGAA$ device is more appropriate for high-speed switching applications. The comparison of drain current of high-K gate insulator material-based $DP\text{-}DGAA$ and $DGAA$ MOSFET versus V_{DS} at $V_{GS} = 1$ V is presented in Fig. 5. It exposes that the drain current of high-K gate insulator material-based $DP\text{-}DGAA$ MOSFET is more beneficial than the $DGAA$ device. Figure 6 demonstrates the comparison of trans-conductance (g_m) of high-K gate insulator material-based $DP\text{-}DGAA$ and $DGAA$ MOSFET against V_{GS} at $V_{DS} = 1$ V. The g_m is a crucial fundamental agent for analog and RF applications, and it is necessary to determine a maximum bias point.

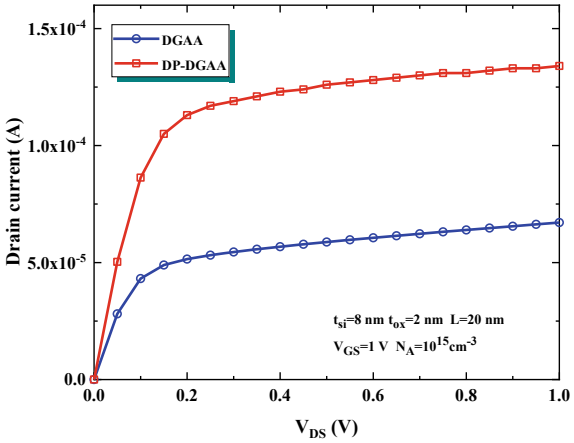

Fig. 5 Comparison of drain current (I_D) of $DGAA$ and $DP\text{-}DGAA$ MOSFET versus V_{DS} at $V_{GS} = 1$ V

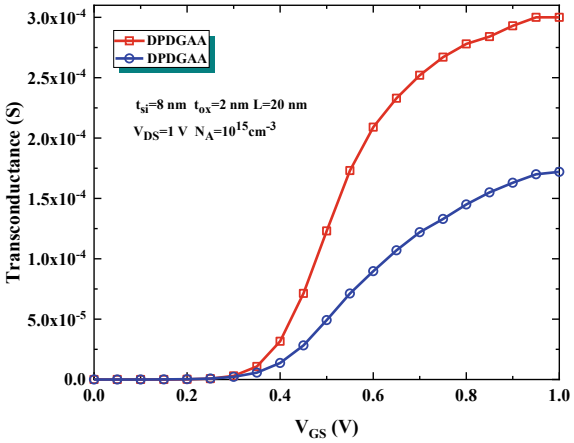

Fig. 6 Comparison of Trans-conductance (g_m) of $DGAA$ and $DP\text{-}DGAA$ MOSFET against V_{GS} at $V_{DS} = 1$ V

The figure reveals that the $DP\text{-}DGAA$ MOSFET shows a leading g_m compared to the $DGAA$ device.

The comparison of TGF (g_m/I_D) of high-K gate insulator material-based $DP\text{-}DGAA$ and $DGAA$ MOSFET against V_{GS} at $V_{DS} = 1$ V is shown in Fig. 7. The trans-conductance generation factor (TGF) is defined as the ratio of g_m and I_D. The TGF is more crucial for the high-K $DP\text{-}DGAA$ device than the $DGAA$ device in the subthreshold region, and the most distinguished TGF value is near the principal utility of subthreshold swing (60 mV/decade). The more vital utility of TGF symbolizes the steady performance of the analog circuit still for low power supply.

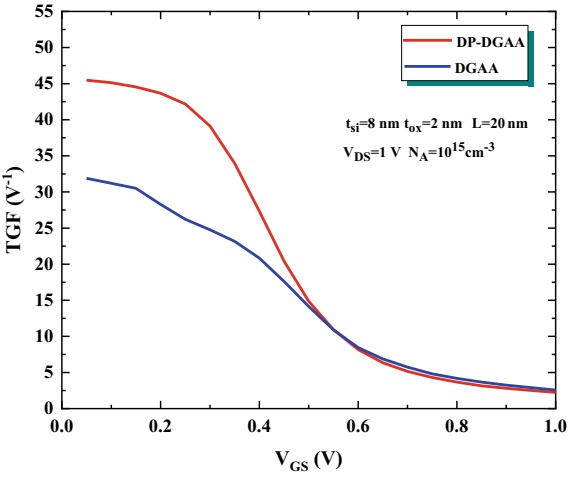

Fig. 7 Comparison of TGF (g_m/I_D) of high-K gate insulator material-based $DP\text{-}DGAA$ and $DGAA$ MOSFET against V_{GS} at $V_{DS} = 1$ V

Table 2 Analog FOMs of $DGAA$ and high-K $DP\text{-}DGAA$ MOSFET at $V_{DS} = 1.0$ at constant threshold voltage

Parameters	*DP-DGAA*	*DGAA*
I_{ON} (A)	1.34×10^{-04}	6.70×10^{-05}
I_{OFF} (A)	1.14×10^{-11}	8.51×10^{-11}
I_{ON}/I_{OFF}	$1.17 \times 10^{+07}$	$7.8 \times 10^{+05}$
SS (mV/decade)	73.64	93.15
DIBL (mV/V)	59.06	172.9
g_m (S)	2.99×10^{-04}	1.72×10^{-04}
TGF (g_m/I_D)	45.48	31.89
g_m/g_d	29.3	11.15

Table 2 shows the analog FOMs of $DGAA$ and high-K DP-$DGAA$ MOSFET at $V_{DS} = 1.0$ at a constant threshold voltage. According to Table 2, the high-K DP-$DGAA$ MOS device is found more superior for analog performance than the $DGAA$ MOSFET. The high-K DP-$DGAA$ ON-current, I_{ON}/I_{OFF} ratio, g_m, TGF, and intrinsic gain are found higher than the $DGAA$, but the OFF-current, subthreshold swing and $DIBL$ are diminishing in comparison to $DGAA$ MOSFET.

4 Conclusion

The impact of dielectric pockets (DPs) introduced in high-K gate insulator material-based $DGAA$ MOSFET on analog performance is investigated and compared with the $DGAA$ device in this paper. The high-K gate insulator material-based DP-$DGAA$ MOSFET has exhibited much-improved performance than $DGAA$ MOSFET. The high-K gate insulator material-based DP-$DGAA$ MOSFET has shown better $SCEs$ immunity compared to $DGAA$. The ON-current of the high-K DP-$DGAA$ device is enhanced than the $DGAA$. The OFF-current of high-K DP-$DGAA$ is effectively suppressed compared to $DGAA$, which results in a much-improved I_{ON}/I_{OFF} current ratio in distinction to $DGAA$ MOSFET. The high-K gate insulator material-based DP-$DGAA$ MOSFET reflects much better analog performance as compared to the $DGAA$ device. Therefore, it is more superior for high-speed analog and switching applications.

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Novel Design of Cylindrical DRA Built MIMO Antenna for 5G Future Prospective Covering (n78/n79) Bands

Ajay Kumar Dwivedi, Anand Sharma, Ashutosh Kumar Singh, and Vivek Singh

1 Introduction

The new face of the world is changed drastically with the resurgence of the latest technology in the domain of wireless communication, especially in mobile communication working on 5G and 6G frequency bands. Various services and advanced features have been developed and offered to the end-users; hence, their exigency in terms of speed forces the researchers to work and develop 5G/6G enabled devices and rollout the services by 2021 [1]. The main objective behind 5G communication is the superior speed it offers, wider bandwidth with very low latency. The whole 5G band has been split up into three different groups (i) <2 GHz (i.e., coverage band) (ii) between 2 and 6 GHz (coverage and capacity layer) (iii) >6 GHz known as the super data layer. In the initial phase, the work is underway to provide the services in the sub-6 GHz frequency range, i.e., (3.3 GHz/3.8 GHz/4.2 GHz) for (n78/n77) and (4.4–5 GHz) for (n79). Working in the frequency, as mentioned above, the band offers the best tradeoff between the wider bandwidth and the rate of transfer of data

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[2]. So, to deliver uninterrupted services to the devices operating at the 5G frequency band, the researchers are needed to be more focused on switching the designing of the SISO antenna to the MIMO antenna so that the requirement of a high rate of data transmission can be achieved. The MIMO antenna geometrical layout consists of multiple inputs and multiple output antennas to mitigate the fading effect and improves the quality of services (QoS), but at the same time, it is tough to accommodate a large number of identical antenna elements in the single unit which leads to the rise of mutual coupling among the antenna elements, and therefore deteriorate the antenna performance and data transmission speed [3]. The value of isolation in the case of MIMO antenna above 10 dB is considered to be in the acceptable range for antenna operating in the Sub-6 GHz spectrum [4]. There is myriad research article has been reported in the past in the domain of planar antennas [5] and dielectric based MIMO antennas [6, 7]. Dielectric resonator-based compact MIMO antenna was first implemented in [8]. Various techniques have been incorporated to enhance the isolation by inserting slits in the ground plane [9], by introducing neutralization lines [10], a high value of separation is achieved when the arrangements of the elements are orthogonal to one another [11]. Limited research work has been done to cover up the entire Sub-6 GHz spectrum. In the present scenario, there is a massive demand to design a MIMO antenna system, which will cover the whole 5G bands, i.e., n77 (3.3–4.2 GHz) and n79 (4.4–5 GHz).

In the presented work, a 2 × 1 dual-polarized DR based MIMO antenna is modeled and investigated by using computer simulation tool HFSS 18. A cylindrical dielectric resonator is rest upon the reshaped triangular-shaped aperture with the conformal strip line is drawn on the sidewalls of the dielectric resonator. The designed antenna operates at three resonating frequencies, i.e., at 3.41 GHz, 5 GHz, and 5.51 GHz covering the frequency spectrum of Sub-6 GHz with satisfactory isolation of <-20 dB. The modified lines on the patch, are responsible to create the CP waves in the lower frequency band and linear polarization characteristics in the upper-frequency band with a considerable gain of (>6 dB) over the whole band. The geometrical layout, mathematical verification of the generated modes, and other results have been discussed in the next section of the article.

2 3D Geometrical Arrangement of the Proposed Antenna

Figure 1 depicts the 3D view as well as the dimensional look of the proposed MIMO antenna. The present article composes of two similar CDRAs made up of alumina-based material ($\varepsilon_{rDRA} = 9.8$; $\tan\delta = 0.002$) of height and radius = 13 mm, which is kept over the FR-4 substrate of height = 1.6 mm having the property ($\varepsilon_{sub} = 4.4$ and $\tan\delta = 0.02$). A modified triangular shape patch is settled on the top of the substrate. The conformal microstrip feed line is employed to feed the power to the radiating patch, and a modified ground plane at the bottom is used to excite the antenna. Table 1 indicates the finalized parametric values of the propounded radiator.

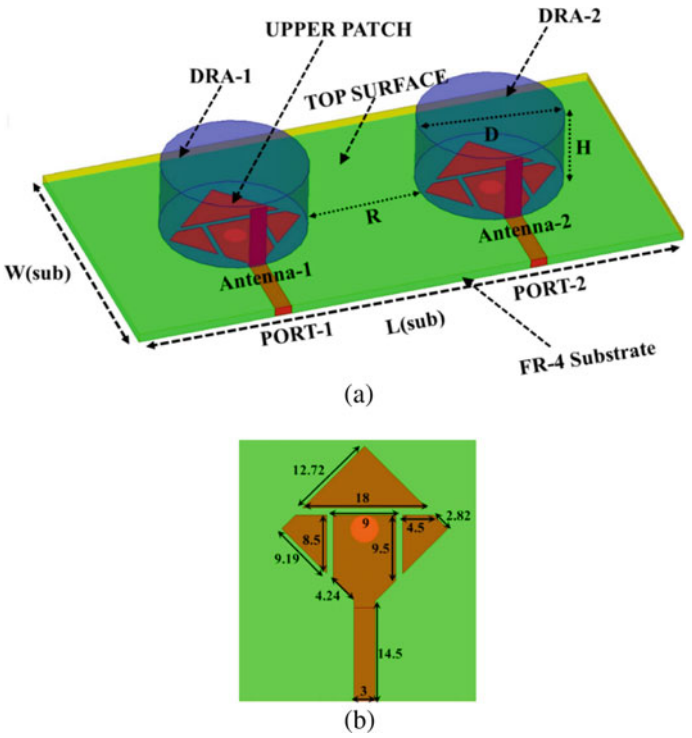

Fig. 1 Schematic layout of the modeled MIMO antenna. **a** 3D view, **b** dimensional look of the patch

Table 1 Optimized dimensions of the presented MIMO antenna

Parameters	Dimension (mm)	Symbol	Dimension (mm)
L (sub)	100	L_1	12.72
W (sub)	50	L_2	18
W_F	3	L_3	9
D and H	13	L_4	6
R	47	L_5	8.5
L_6	9.19	L_8	2.82
L_7	4.5	L_9 and L_{10}	4.24 and 14.5

3 Antenna Analysis and Mathematical Validation

The modeling and the study of the suggested MIMO antenna have been done by using the computer software ansys HFSS 18. Figure 2 shows the variation in the $|S_{11}|$ parameters for two different cases, i.e., by placing the DRA on top of the patch and without using it, three important observations are observed (i) the proposed antenna

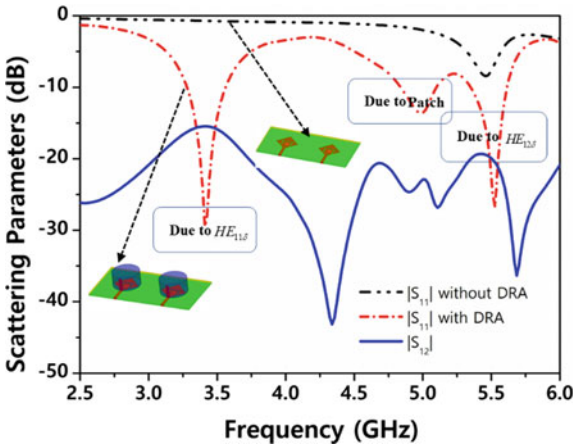

Fig. 2 Comparison in terms of scattering parameters of the presented MIMO antenna with and without using the DRA and the mutual coupling

operates at three different resonating frequencies with magnitude (>−10 dB) (ii) generation of two dissimilar hybrid modes, i.e., $HE_{11\delta}$ and $HE_{12\delta}$ at two different resonating frequencies (iii) capable to generate the circular polarization features at the lower resonating frequency. From the perusal of Fig. 2, it can be seen that out of the three resonating frequencies, two are the radiating modes, and one resonating band generated because of the radiating patch. The mode field lines also verify the generation of modes c.f. Fig. 3.

The resonant frequency for $HE_{11\delta}$ in the case of cylindrical DRA can be computed mathematically firstly calculated the value of effective permittivity and the effective Height of the CDRA from Eqs. 2 and 3 and then substitute the value in the first equation [12].

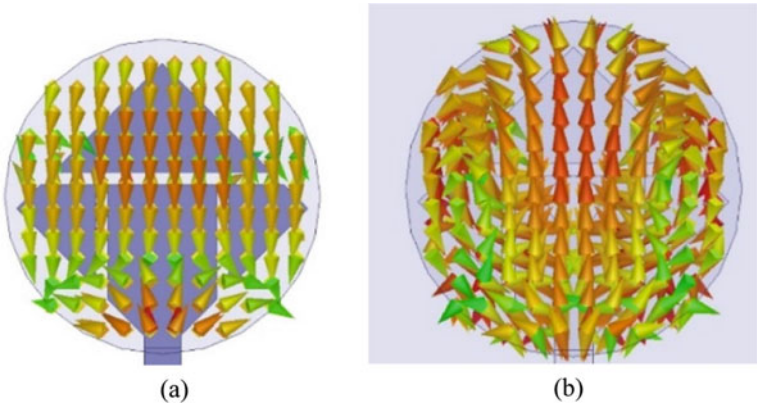

Fig. 3 Electric field lines distribution in the DRA. **a** At 3.41 GHz (top view), **b** at 5.5 GHz (top view)

$$f_{r,\mathrm{HE}_{11\delta}} = \frac{6.321c}{2\pi D\sqrt{\varepsilon_{\mathrm{dra,eff}}+2}}\left\{0.27+0.36\left(\frac{D}{2H_{\mathrm{eff}}}\right)+0.02\left(\frac{D}{2H_{\mathrm{eff}}}\right)^2\right\} \quad (1)$$

$$\varepsilon_{\mathrm{dra,eff}} = \frac{H_{\mathrm{eff}}}{\frac{H}{\varepsilon_{\mathrm{Al_2O_3}}}+\frac{H_{\mathrm{sub}}}{\varepsilon_{\mathrm{sub(FR-4)}}}} \quad (2)$$

and

$$H_{\mathrm{eff}} = H + H_{\mathrm{sub}} \quad (3)$$

By exercising the above calculation, the resonant frequency so obtained as 3.38 GHz from Eq. 1. However, no known formula exists to calculate the resonant frequency of $\mathrm{HE}_{12\delta}$ mode, yet it can be anticipated by using the resonant frequency of $\mathrm{HE}_{11\delta}$ mode, as shown below [13]:

$$f_{r,\mathrm{HE}_{12\delta}} \geq 1.85\, f_{r,\mathrm{HE}_{11\delta}} \quad (4)$$

Using Eq. 4, the resonating frequency of 5.45 GHz is obtained for $\mathrm{HE}_{12\delta}$ mode. Which is in close agreement with the simulated value.

4 Results and Discussion

With the reference of Figs. 2 and 4, two necessary conditions are fulfilled (i) Isolation exceeds by 20 dB between the different antenna elements (ii) the curve of $|S_{11}|$ and $|S_{22}|$ matches precisely the same. A CP wave characteristic is obtained and shown in Fig. 5, any shape of aperture always behaves as a magnetic dipole and exhibits weak

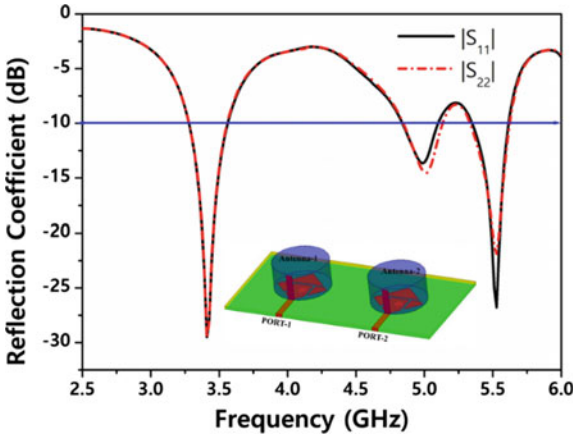

Fig. 4 Plot of the reflection coefficient in terms of ($|S_{11}|$ and $|S_{22}|$) of 2 port MIMO antenna

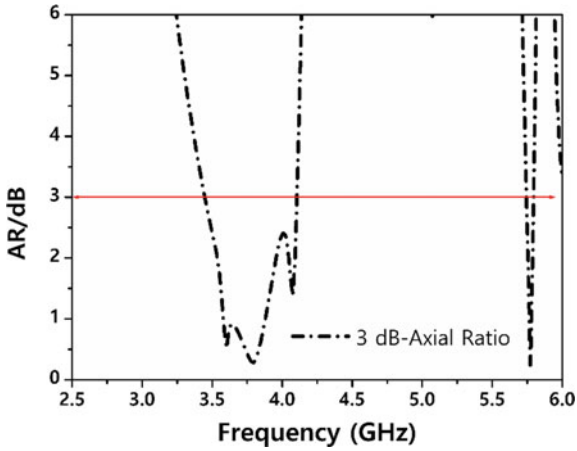

Fig. 5 A 3 dB axial ratio at the lower frequency (3.41 GHz) of the presented MIMO radiator

coupling. The vertical and horizontal strips lines on the patch, able to create a 90° phase shift, and hence the CP wave is obtained at the lower frequency band.

Figures 6 and 7 displays the 2D far-field radiation pattern of the two antennas at the different resonating frequencies, the patterns are achieved when port 1 is excited, keeping the port 2 ended with 50 Ω resistance and vice versa. Figure 6 shows that the radiation pattern of the antenna when port 1 and port 2 is used at 3.41 GHz is right-handed circularly polarized with a sufficient difference of 20 dB. The value of co and cross-polarization is almost the same for both the antennas. Which satisfies one of the conditions of the MIMO antenna. The reduction of 8–10 dB in the co and cross-polarization can be seen (c.f. Fig. 7c, d). At 5.5 GHz, the $HE_{12\delta}$ mode is radiating at the broadside direction.

The peak gain and antenna radiation efficiency versus frequency have been plotted and shown in Fig. 8; it is clearly seen that the proposed MIMO antenna has a positive value of gain over all the three resonating frequencies and the value increases in

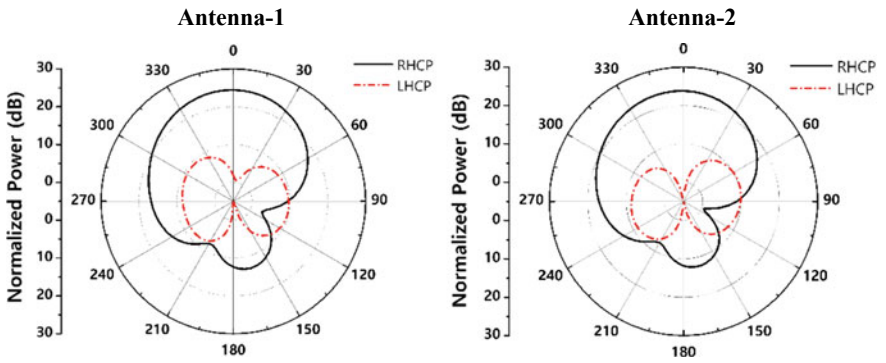

Fig. 6 2D far-field (LHCP and RHCP) radiation pattern of antenna-1 and antenna-2 at 3.41 GHz

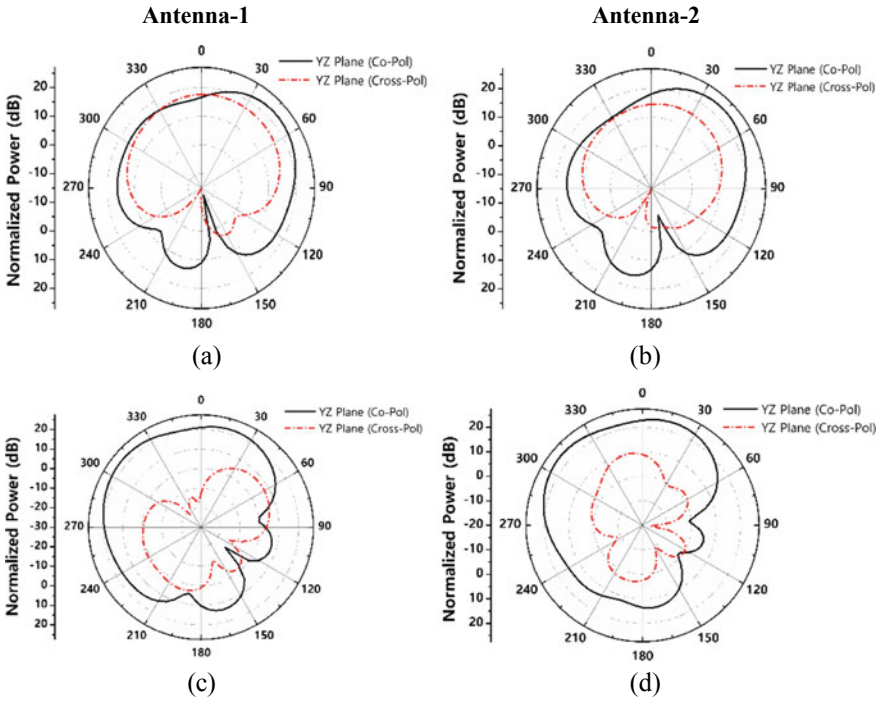

Fig. 7 2D far-field pattern in *YZ* plane for antenna 1 and antenna 2 at 5 GHz shown in figs. (**a**) and (**b**) and for antenna-1 and antenna-2 at 5.51 GHz shown in figs. (**c**) and (**d**)

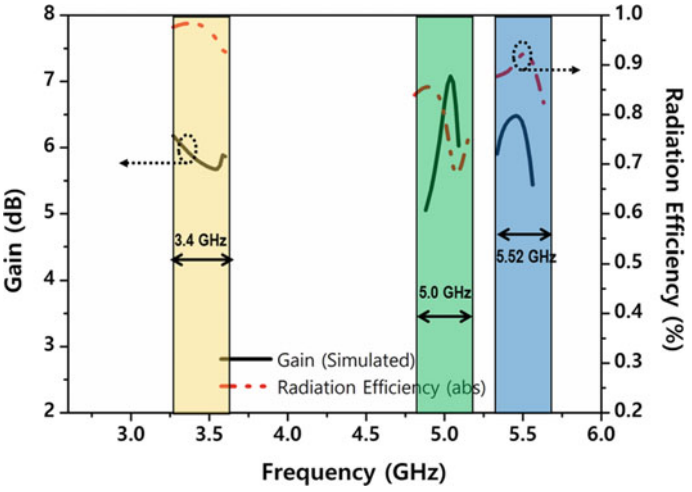

Fig. 8 Simulated gain and radiation efficiency versus frequency plot of the proposed MIMO antenna

the higher frequency due to the use of cylindrical DRA. It is also make out that the antenna has radiation efficiency > 90% over the whole operating band.

5 Diversity Representation of the Present MIMO Antenna

The envelope channel coefficient and diversity gain are two essential diversity parameters in MIMO applications. In practical MIMO antenna applications, ECC plays a very vital role in determining the effect of the radiation pattern of one antenna on to others. When placed in the same unit cell, for better performance ECC (<0.5) is considered to be in the acceptable range. From Fig. 9, it is noticed that ECC is very close to zero, which proves that it has a good radiation pattern in MIMO wireless applications. ECC can be calculated by the scattering parameter by the use of a given equation [14].

$$\rho_{\text{enm}} = \left| \frac{\left| S_{\text{nn}}^{*} S_{\text{nm}} + S_{\text{mn}}^{*} S_{\text{mm}} \right|}{\left| \left(1 - |S_{\text{nn}}|^2 - |S_{\text{mn}}|^2\right)\left(1 - |S_{\text{mm}}|^2 - |S_{\text{nm}}|^2\right) \right|^{1/2}} \right| \tag{5}$$

The value diversity gain (DG) should ~10, in Fig. 9, it is observed distinguish that the value of DG is closer to 10 at the operating frequency, and also it can be found by the given formula [15].

$$\text{DG} = \sqrt{1 - \text{ECC}} \tag{6}$$

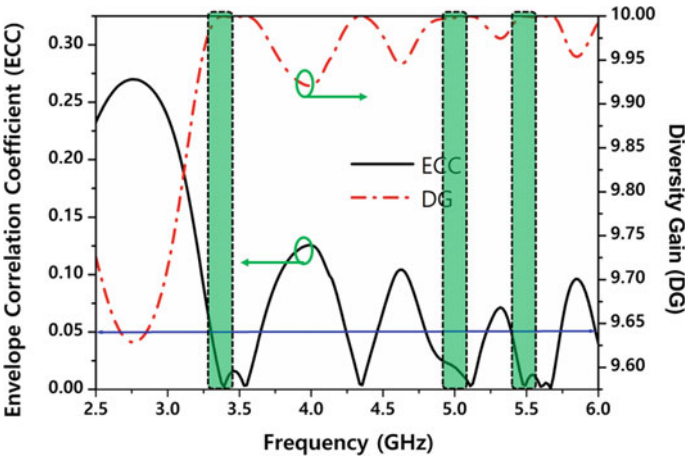

Fig. 9 Graph of simulated ECC and DG versus frequency of the suggested MIMO antenna

6 Conclusion

In this manuscript, a triband, dual-polarized 2 × 1 dielectric resonator-based MIMO antenna has been modeled and discussed. The proposed antenna is designed to cover up the two crucial frequency bands n77 (3.3–4.2 GHz) and n79 (4.4–5 GHz) of Sub-6 GHz applications. The placement of antenna elements able to provide decent isolation (>20 dB) and nearly a constant gain of about (~5 to 6 dB) with almost (>90%) antenna efficiency. The simulated value of ECC and DG revels that the antenna has better diversity performance. All the simulated results are shown and explained to make the proposed DR based MIMO antenna an appropriate module for 5G applications.

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Investigation of Analog Performance of $In_{0.53}Ga_{0.47}As$-Based Nanotube Double-Gate-All-Around (DGAA) MOSFET

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1 Introduction

In the last two decades, the MOSFET Technology node shifted from micro-meter to nano-meter to improve Gadget performance, computational speed, and its features. With the shrinking device dimensions, short channel effects (SCEs) become indispensable. The adverse effect produced by SCEs can be overcome through modifications in device design. Few designs are FinFET, Omega FET, and Multigate (MG) MOSFET. Due to better SCE immunity in an aggressive scaling environment, MG-MOSFET is a better choice [1–4]. Among all Multigate (MG) structures, Gate-All-Around (GAA) MOSFET achieved efficient gate control to dissuade short channel effects for the future technology nodes, and become the first choice of researchers [4]. GAA MOSFET provides reasonable electrostatic control over the channel, drastically suppresses the SCEs, and improves subthreshold characteristics that make it highly attractive for low power applications [4]. However, due to the small drive current, it suffers from low computational speed [5]. Horizontal/vertical stacking of GAA improves the drive current but at the cost of the useful chip area. Without compromising the chip area, drive current can be enhanced through the incorporation of one additional gate in GAA. Now Double-Gate-All-Around (DGAA) [6–8] with inner (Core) and outer (shell) gates provides high drive current as well as superior short-channel immunity in comparison with GAA. Further improvement in drive

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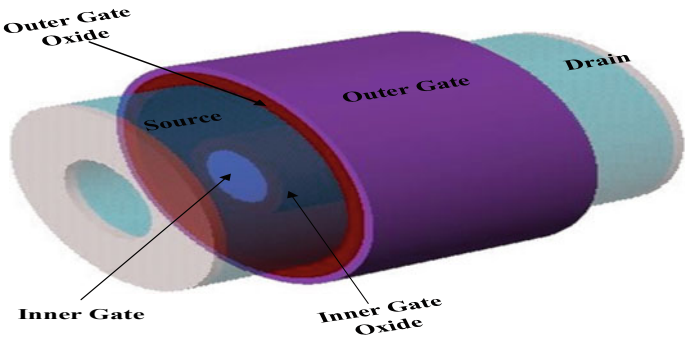

Fig. 1 3D schematics structure of $In_{0.53}Ga_{0.47}As$-based DGAA MOSFET

current at reduced supply voltage can be achieved through fabricating it with high mobility material $In_{0.53}Ga_{0.47}As$ [9, 10]. It also diminishes the leakage current and provides superior computational speed. In light of the works mentioned above, it can be concluded that with shrinking dimensions, $In_{0.53}Ga_{0.47}As$ DGAA MOSFETs are a promising solution for excellent computational speed.

In this work, a comparative study of Silicon-Based DGAA and $In_{0.53}Ga_{0.47}As$-Based DGAA has been done. The performance analysis of Silicon-Based DGAA and $In_{0.53}Ga_{0.47}As$-Based DGAA devices have been done in terms of variation in ON-state current (I_{ON}), OFF-state current (I_{OFF}), ON–OFF current ratio (I_{ON}/I_{OFF}), subthreshold swing (SS), Drain induced barrier lowering (DIBL), trans-conductance (g_m), and trans-conductance generation factor (TGF) characteristics on ATLAS, a 3D device simulator from SILVACO.

2 Device Structure and Simulation Framework

The 3D schematics structure of $In_{0.53}Ga_{0.47}As$-Based DGAA MOSFET for simulation is shown in Fig. 1. The cross-sectional view of $In_{0.53}Ga_{0.47}As$-Based DGAA MOSFET is displayed in Fig. 2. A thin Al_2O_3 oxide layer wraps the tubular channel region. Table 1 represents the device parameters used for simulation. The following models of 3D ATLAS device simulator have been active to perform the simulation of the proposed $In_{0.53}Ga_{0.47}As$-Based DGAA device and Silicon-Based DGAA devices [11], such as DD charge transport model, Lombardi (CVT) model, concentration-dependent mobility model, and Shockley-Real-Hall (SRH) model.

3 Results and Discussion

Figure 3 shows the contour plot of Potential for $In_{0.53}Ga_{0.47}As$-Based DGAA

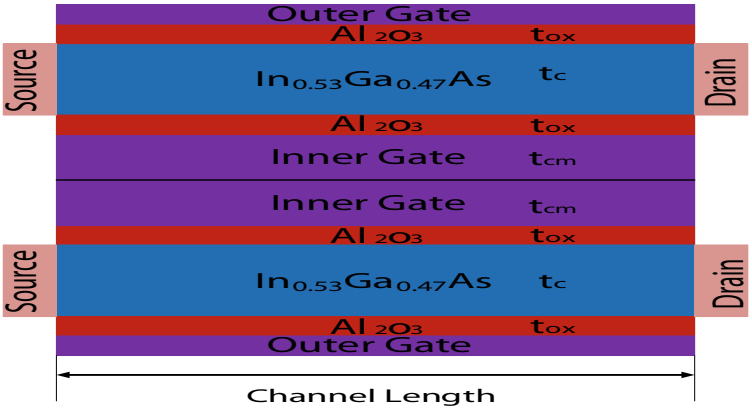

Fig. 2 The horizontal cross-sectional view of $In_{0.53}Ga_{0.47}As$-based DGAA MOSFET

Table 1 Silicon and $In_{0.53}Ga_{0.47}As$ based device parameters used for DGAA MOSFETs simulation

Parameters	Silicon	$In_{0.53}Ga_{0.47}As$
Channel length (L)	20 nm	20 nm
Source/drain doping (N_D)	10^{20} cm^{-3}	10^{20} cm^{-3}
Channel doping (N_A)	10^{15} cm^{-3}	10^{15} cm^{-3}
Oxide thickness (t_{ox})	1 nm	1 nm
Channel thickness (t_C)	8 nm	8 nm
Inner core metal radius	4 nm	4 nm
Metal work-function (ϕ_M)	4.64 eV	5.1 eV

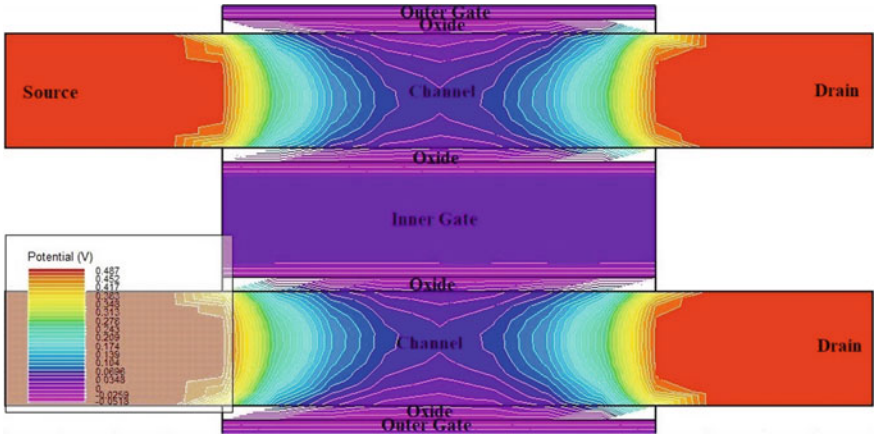

Fig. 3 The horizontal cross-sectional view of a contour plot of potential for $In_{0.53}Ga_{0.47}As$-based DGAA MOSFET at $V_{GS} = V_{DS} = 0$ V

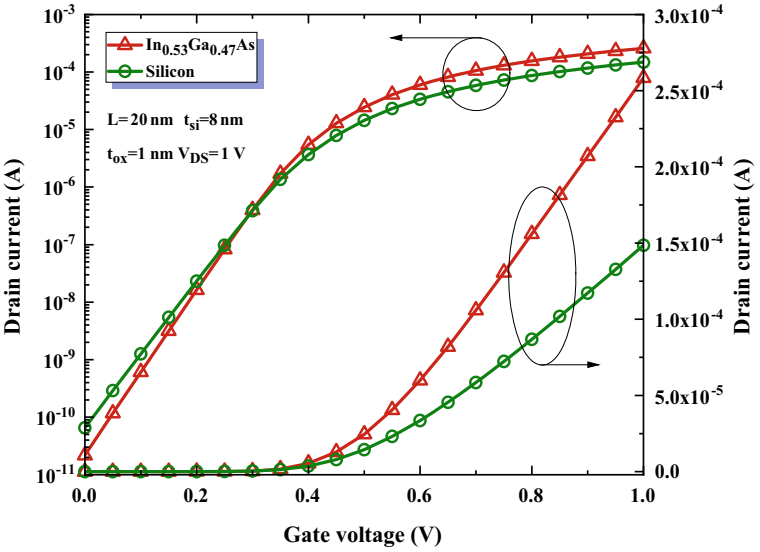

Fig. 4 Comparison of drain current (I_D) of silicon and $In_{0.53}Ga_{0.47}As$-based DGAA MOSFET versus V_{GS} at $V_{DS} = 1$ V

MOSFET at $V_{GS} = V_{DS} = 0$ V. The plot reveals that the minimum inner surface channel potential is higher than the minimum outer surface potential. It indicates the dominance of the inner gate over the outer gate in controlling the channel region. Figure 4 presents the comparison of Drain current (I_D) of Silicon and $In_{0.53}Ga_{0.47}As$-Based DGAA MOSFET versus gate-to-source voltage (V_{GS}) at a drain-to-source voltage (V_{DS}) = 1 V. The improvement of I_{ON} and I_{OFF} is observed in $In_{0.53}Ga_{0.47}As$-Based DGAA MOSFET, as shown in Fig. 4. The ON-current increases by 74.32%, but the OFF-current reduces by 66.66% of $In_{0.53}Ga_{0.47}As$-Based DGAA MOSFET compared to Silicon-Based DGAA MOSFET. Due to the device channel's high mobility material with high gate oxide consequence of insignificant phonon scattering in the channel region, it has occurred. The I_{ON}/I_{OFF} ratio is found better for the $In_{0.53}Ga_{0.47}As$-Based DGAA MOSFET in comparison to DGAA MOSFET owing to the steeper subthreshold slope. Hence, the $In_{0.53}Ga_{0.47}As$-Based DGAA MOSFET is more suitable for high-speed switching applications and low power consumption circuits. Figure 5 shows the comparison of Drain current of Silicon and $In_{0.53}Ga_{0.47}As$-Based DGAA MOSFET versus V_{DS} at $V_{GS} = 1$ V. It reveals that the drain current of $In_{0.53}Ga_{0.47}As$-Based DGAA MOSFET is higher by 74.32% compared to silicon-Based DGAA MOSFET. The comparison of Trans-conductance (g_m) of Silicon and $In_{0.53}Ga_{0.47}As$-Based DGAA MOSFET against V_{GS} at $V_{DS} =$ 1 V is shown in Fig. 6. The g_m is a crucial key factor for analog and RF applications, and it is also essential to define an optimum bias point. For any device, the cut-off frequency is the peak at an optimum bias point. The figure exhibits that the

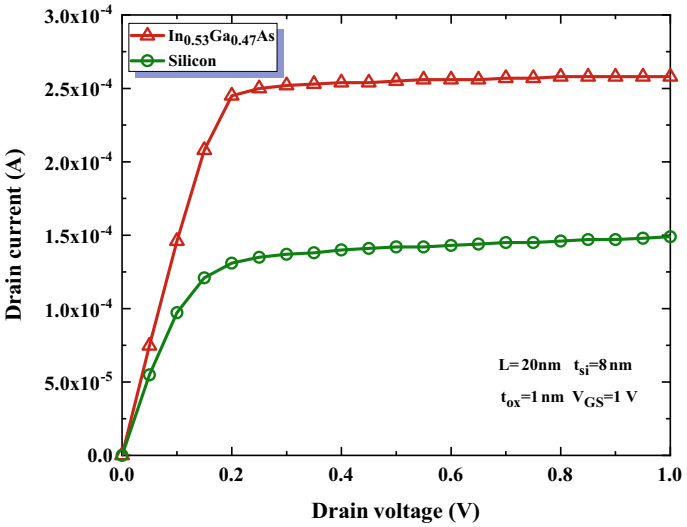

Fig. 5 Comparison of drain current of silicon and $In_{0.53}Ga_{0.47}As$-based DGAA MOSFET versus V_{DS} at $V_{GS} = 1$ V

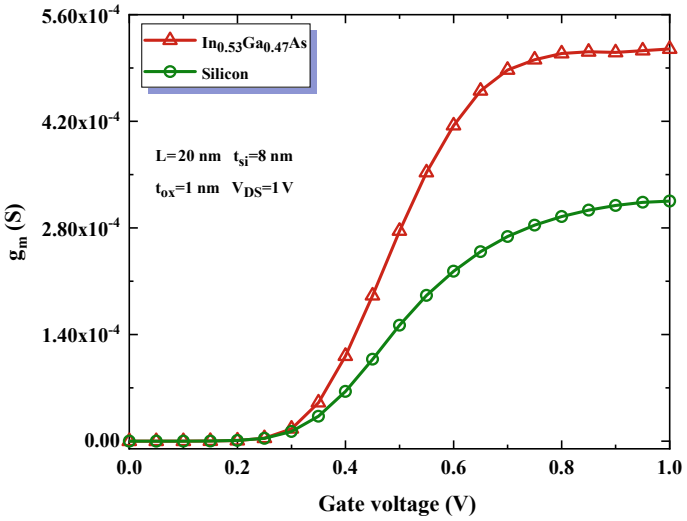

Fig. 6 Comparison of trans-conductance (g_m) of silicon and $In_{0.53}Ga_{0.47}As$-based DGAA MOSFET against V_{GS} at $V_{DS} = 1$ V

$In_{0.53}Ga_{0.47}As$-Based DGAA device exposes 63.5% more distinguished g_m than the Silicon-Based DGAA MOSFET.

Figure 7 demonstrates the comparison of TGF (g_m/I_D) of Silicon and $In_{0.53}Ga_{0.47}As$-Based DGAA MOSFET against V_{GS} at $V_{DS} = 1$ V. The ratio of g_m and I_D is known as the trans-conductance generation factor (TGF). The highest TGF value is near the Ideal amount of subthreshold swing 60 mV/decade. In the subthreshold region, TGF is more significant for $In_{0.53}Ga_{0.47}As$-Based DGAA MOSFET than the silicon-Based DGAA device. The more valuable value of TGF indicates the steady operation of the analog circuit even for low power supply.

Table 2 shows the Analog FOMs of Silicon and $In_{0.53}Ga_{0.47}As$-Based DGAA

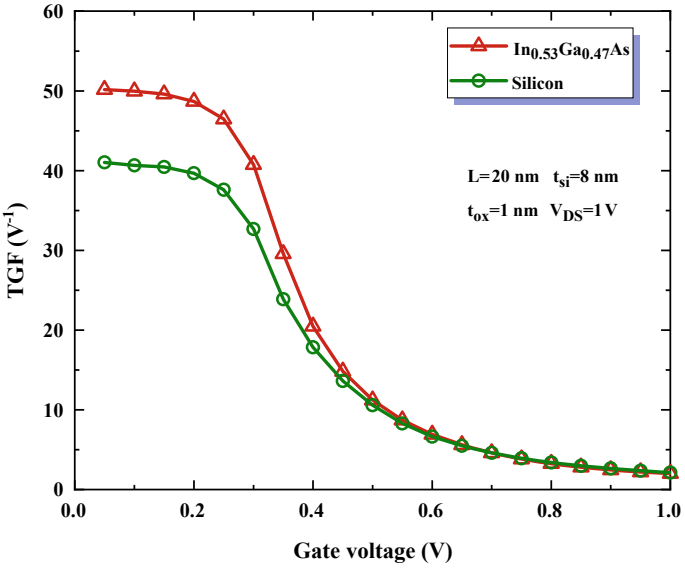

Fig. 7 Comparison of TGF (g_m/I_D) of silicon and $In_{0.53}Ga_{0.47}As$-based DGAA MOSFET against V_{GS} at $V_{DS} = 1$ V

Table 2 Analog FOMs of silicon and $In_{0.53}Ga_{0.47}As$-based DGAA MOSFET at $V_{DS} = 1.0$ at constant threshold voltage

Parameters	Silicon	$In_{0.53}Ga_{0.47}As$
I_{ON} (A)	1.48×10^{-04}	2.58×10^{-04}
I_{OFF} (A)	6.51×10^{-11}	2.17×10^{-11}
I_{ON}/I_{OFF}	$2.28 \times 10^{+06}$	$1.19 \times 10^{+07}$
SS (mV/decade)	77.13	68.42
DIBL (mV/V)	73.01	33.94
g_m (S)	3.15×10^{-04}	5.15×10^{-04}
g_m/I_D (V^{-1})	41.04	50.16

MOSFET at $V_{DS} = 1.0$ at constant threshold voltage. According to Table 2, the $In_{0.53}Ga_{0.47}As$-Based DGAA device is found better for analog performance compared to silicon-Based DGAA MOSFET. The ON-current, g_m, and TGF of $In_{0.53}Ga_{0.47}As$-Based DGAA devices are higher by 74.32%, 63.5%, and 22.22%, respectively, than the silicon-Based DGAA device. However, the $In_{0.53}Ga_{0.47}As$-Based DGAA MOSFET performance parameters such as OFF-current (I_{OFF}), subthreshold swing (SS), and DIBL are reduced by 66.66%, 11.3%, and 53.51%, respectively, compared to silicon-Based DGAA MOSFET.

4 Conclusion

The In0.53Ga0.47As-Based DGAA MOSFET has been proposed in this paper. It has been examined by a 3D ATLAS TCAD device simulator from SILVACO and compared with the silicon-Based DGAA MOSFET. The In0.53Ga0.47As-Based DGAA MOSFET has exhibited much-improved performance compared to silicon-Based DGAA MOSFET. The In0.53Ga0.47As-Based DGAA MOSFET has shown better SCEs immunity compared to silicon-Based DGAA. The ON-current, g_m, and TGF of In0.53Ga0.47As-Based DGAA devices have been found higher by 74.32%, 63.5%, and 22.22%, respectively, compared to the silicon-Based DGAA device. However, the In0.53Ga0.47As-Based DGAA MOSFET performance parameters such as OFF-current (I_{OFF}), subthreshold swing (SS), and DIBL have found reduce by 66.66%, 11.3%, and 53.51%, respectively, compared to silicon-Based DGAA MOSFET. The In0.53Ga0.47As-Based DGAA MOSFET reflects much better analog performance compared to the silicon-Based DGAA device. Therefore, it is more superior for high-speed analog and switching applications.

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Integrated Clock Gating Analysis of TG Based D Flip-Flop for Different Technology Nodes

Sunita Panda, Samiksha Sharma, and Abhijit R. Asati

1 Introduction

In the field of electronics, especially in battery operated digital devices that need faster operation keeping power consumption low, the low power dissipation is an important design constraint. The circuit power dissipations are of mainly two types, viz. static and dynamic. The switching activity of the circuit decides the dynamic power consumption of a circuit; whereas the circuit leakage currents decide the static power dissipation of a circuit. The proportional dependence of dynamic power with switching activity, load capacitance, frequency of operation and square of supply voltage of the circuit is well-known. Since with scaling the technology node both parasitic capacitance and supply voltage reduce therefore it also helps in reducing the dynamic power consumption of a circuit. Furthermore, static power consumption increases due to increased leakage currents. In most of the VLSI digital circuits a clock network remains an integral part and it consumes a 30–70% of total power dissipation [1].

In flip-flop the dynamic power requirement is reduced using clock gating technique. The clock gating can be achieved through (i) enable signal so as to control clock to a clock network when not in use or (ii) clock gating as applied to individual flip-flop when its input D and output Q are same. The D flip-flop (triggered in negative edge) is realized using TG based master-slave model as shown in Fig. 1 which is same in structure with positive edge triggered PowerPC 603 flip-flop [2–4]. In this paper clock gating technique restricts the clock signal to a clock network when it is not in use. The application of clock to the flip-flop will result in 0 to 1 and 1 to

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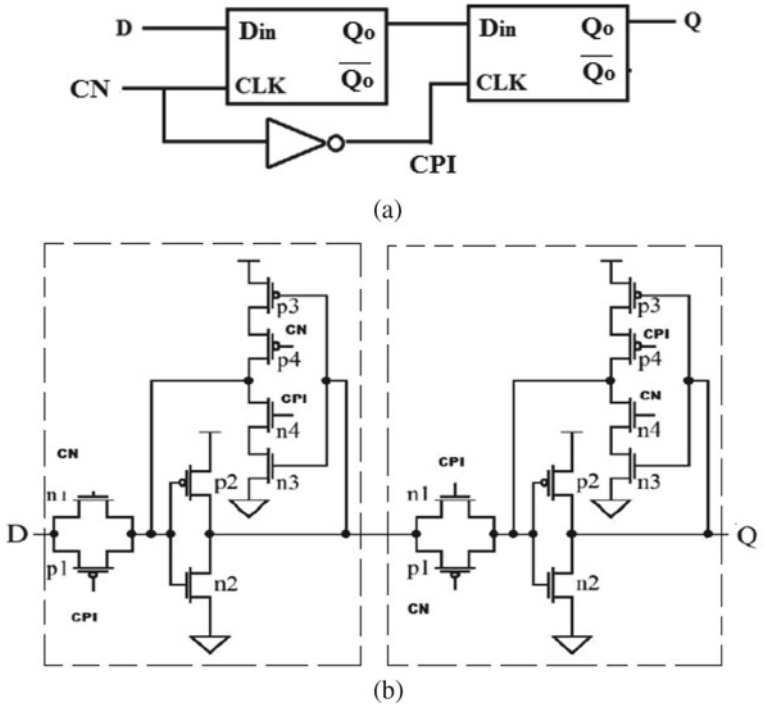

Fig. 1 **a** Block diagram of flip flop, **b** TG based D flip-flop

0 transitions with a change in data or clock which increases the switching activity hence consume more power [5, 6]. Further increase in switching activity is due to transition in applied input data 'D' of the flip-flop (termed as the data activity factor as explained later in Sect. 3). The flip-flop clock gating implementation in [5, 6] at 350 nm technology, also the implementation in [7] at 28 nm technology node show power results for clock gating for some benchmark circuits but do not consider data activity factor and frequency in analysis. The implementation in [8] 16 nm node where the work describes the low power and low dynamic leakage in 16-bit counter using ICG but in-depth analysis for individual flip flop on ICG considering the data activity factor and frequency is missing. In this paper we have simulated the average power dissipation of D flip-flop with and without ICG at different technology nodes at circuit level considering the data activity factor and frequency. The ICG approach has been implemented in the TG based D flip-flop. The power consumption with and without ICG at several frequencies of operation and several data activity factors are investigated as a comparative analysis study at 32 nm, 22 nm, 16 nm technology nodes, respectively (selected technology nodes). The comparative analysis performed by applying selected data activity factors at a particular random intermediate clock frequency so as to observe both positive and negative power savings. Further analysis is performed by changing the selected frequency of clock for a fixed data activity

factor so as to observe the effect of frequency. Section 2 discusses the TG based D Flip-Flop and ICG Method. Section 3 shows all simulation results and discussion and Sect. 4 concludes the paper.

2 Implementation of TG Based D Flip-Flop and ICG Technique

2.1 TG-Based D Flip-Flop

The TG based flip-flop in Fig. 1 is realized using TG in the forward path and clocked inverters in the feedback path. This is a negative edge triggered master-slave flip-flop with CN as clock pulse and CPI as inverted clock pulse. The master stage activates for positive clock and slave stage at negative clock. Feedback clocked inverters are used in order to overcome input noises. For sizing the transistors, all transistors in the forward path are given high driving capacity to lower the clock-to-Q delay of flip-flop and hence to improve its speed of operation. Feedback inverters are kept at minimal size to reduce the area of the overall circuit. The ratio from pmos to nmos taken are 1.5:1, 1:1, 1:1 for 32 nm, 22 nm and 16 nm technology nodes, respectively. The supply voltages chosen are 0.45 V, 0.45 V and 0.35 V for 32 nm, 22 nm, and 16 nm, respectively.

2.2 ICG Circuit

The ICG circuit is shown in Fig. 2 [5]. Latch-NOR ICG is basically used for negative edge triggered flip-flops. This clock gating circuitry consists of a positive D latch followed by a NOR gate. The gated clock (Gclk) signal is passed through an inverter to generate inverted gated clock (Gclk_bar). For clock gated TG based D flip-flop, the inputs CN and CPI of flip-flop circuit of Fig. 1 are replaced with Gclk and Gclk_bar, respectively. Instead of applying Enable directly to the NOR gate, firstly it is applied to the latch, as it removes any glitches present in enable signal.

This ICG also changes polarity of global clock [5] as shown in Fig. 4.

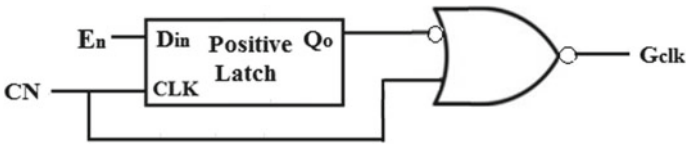

Fig. 2 Latch-NOR ICG cell for negative edge triggered flip-flops [5]

3 Simulation Results and Discussion

The TG based D flip-flop and shown in Fig. 1 and clock gated TG based D flip-flop as explained in Sect. 2.2 are simulated for three technology nodes, namely 32 nm, 22 nm, 16 nm. Figure 3 shows the transient responses of the TG based D flip-flop without ICG. The output Q follows the D at every negative edge of the clock pulse.

Figure 4 shows the transient responses of the TG based D flip-flop with ICG. The output Q follows the D at every negative edge of the gated clock pulse. The instantaneous power waveform of TG D flip-flop without ICG is shown in Fig. 5, while instantaneous power waveform of TG D flip-flop with ICG is shown in Fig. 6.

The analysis assumes following parameters:

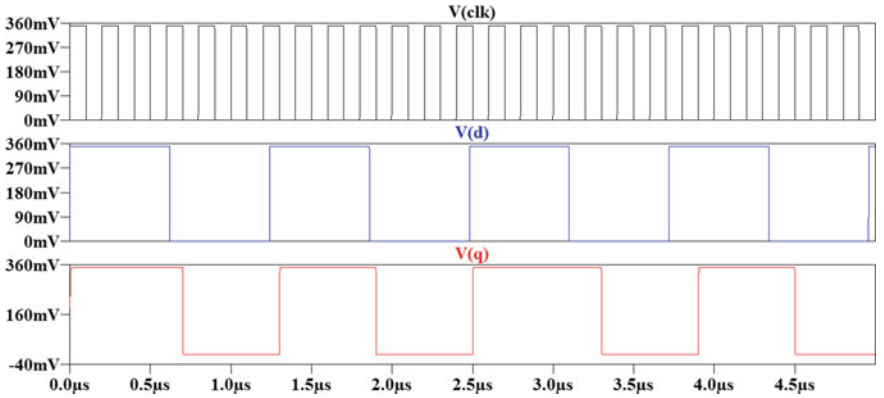

Fig. 3 Transient response of TG based D flip-flop without clock gating

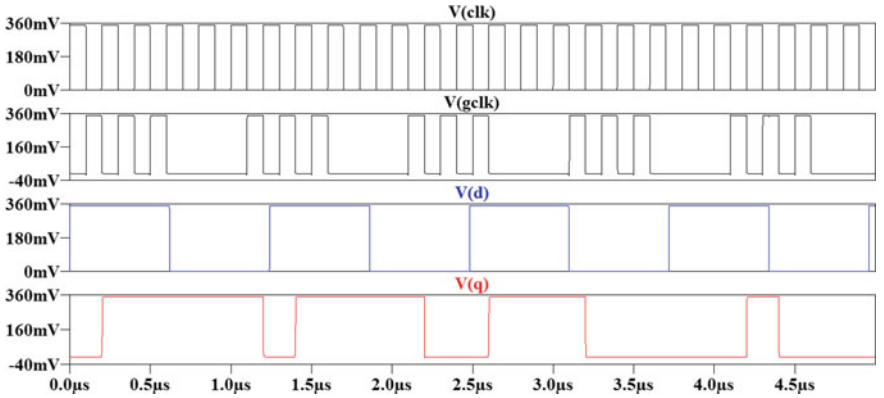

Fig. 4 Transient response of D flip-flop with ICG

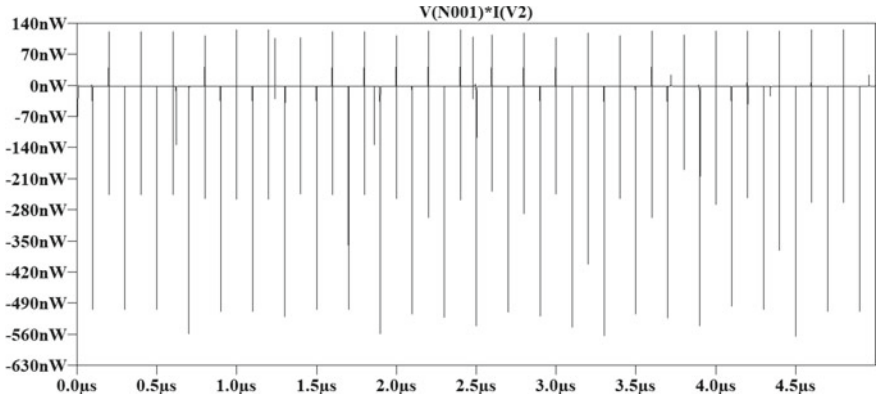

Fig. 5 Instantaneous power waveform without CG in TG D flip-flop

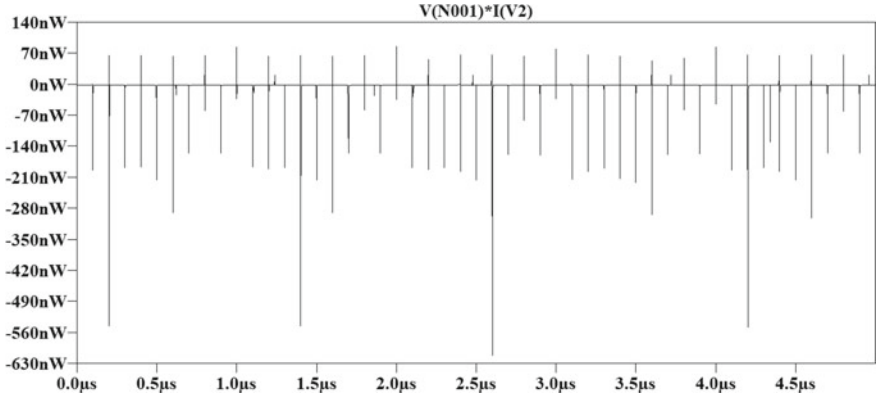

Fig. 6 Instantaneous power waveform with ICG in TG D flip-flop

f_{clk}: Frequency of clock signal. The clock periods are selected as 5 ns, 20 ns, 60 ns and 200 ns which gives f_{clk} as 200 MHz, 50 MHz, 16.67 MHz and 5 MHz, respectively.

Data activity factor: % change in data in every clock cycle [if data 'D' changes every clock cycle then data activity factor is 100%, if data changes every three clock cycle then data activity factor is 33.33% (~33%), if data changes every six clock cycle then data activity factor is 16.66% (~16%), if data changes every twelve clock cycle then data activity factor is 8.33% (~8%), if data do not changes then data activity factor is 0%, etc.]. The data activity factor reduces the switching at the internal nodes of the flip flop, i.e., if data 'D' does not change then switching at internal nodes of flip flop will reduce.

Rise and fall times: The rise and fall times kept equal value of 50 ps for data, clock and enable signal.

Table 1 Comparison of average power dissipation for different of technology nodes

Technology nodes (f_{clk} = 16.67 MHz, Data activity factor = 33%)	P_{avg} Unit: nW	
	W/O ICG	With ICG
32 nm	6.6904	5.2457
22 nm	5.5186	4.6214
16 nm	4.0103	4.1412

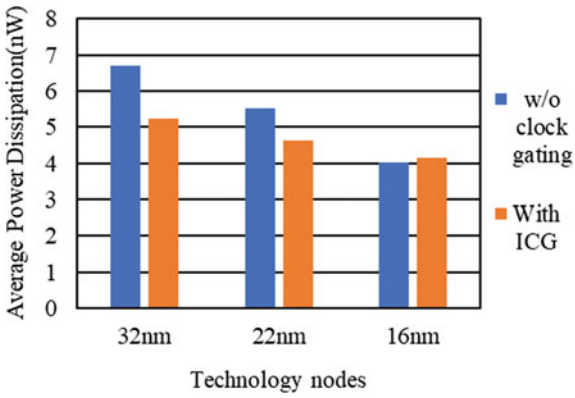

Fig. 7 Graphical representation of average power dissipation for different technology nodes (f_{clk} = 16.67 MHz, Data activity factor = 33%)

$\boldsymbol{P_{avg}}$: Average Power dissipation in watt.

% Power savings: Reduction in power after clock gating with respect to power without clock gating.

Firstly, the average power dissipation of TG based D flip-flop with and without ICG circuitry is compared for the different the technology nodes at 16.67 MHz clock frequency (60 ns clock period) and 33% data activity as shown in Table 1.

The graph in Fig. 7 indicates that average power dissipation of TG based D flip-flop with and without ICG. The average power dissipation increases with increase in technology node values as expected. Also clock gating appears to be ineffective at 16 nm technology node.

Further, the power consumption and power savings of TG based D flip-flop with and without ICG are studied for the different technology nodes by fixing the clock frequency at 16.67 MHz (random intermediate clock frequency so as to observe both positive and negative power savings, so that negative power saving can be further analyzed) and by varying the data activity factor as indicated in Table 2 (for 32 nm), Table 3 (for 22 nm) and Table 4 (for 16 nm). The '+' sign in % power savings column indicates that power can be saved using ICG and '−' sign indicates that average power increases.

The graph in Fig. 8 drawn for 16.67 MHz clock frequency shows that the power savings of TG based D flip-flop with ICG technique is significant at selected technology nodes (32 nm, 22 nm and 16 nm) and at higher data activity factor. It is also

Table 2 Average power dissipation and power savings for 32 nm technology for different activity factor ($f_{clk} = 16.67$ MHz)

Data activity factor (%)	P_{avg} (w/o ICG) Unit: nW	P_{avg} (with ICG) Unit: nW	% Power savings
100	13.853	7.763	43.95
33	6.690	5.245	21.59
16	4.760	4.151	12.79
8	3.876	3.829	1.21
0	3.041	2.995	1.49

Table 3 Average power dissipation and power savings for 22 nm technology for different activity factor ($f_{clk} = 16.67$ MHz)

Data activity factor (%)	P_{avg} (w/o ICG) Unit: nW	P_{avg} (with ICG) Unit: nW	% Power savings
100	12.057	6.239	48.25
33	5.518	4.621	16.26
16	3.800	3.264	14.10
8	3.021	2.992	0.976
0	1.483	2.424	−63.47

Table 4 Average power dissipation and power savings for 16 nm technology for different activity factor ($f_{clk} = 16.67$ MHz)

Data activity factor (%)	P_{avg} (w/o ICG) Unit: nW	P_{avg} (with ICG) Unit: nW	% Power savings
100	7.824	5.599	28.43
33	4.010	4.141	−3.26
16	2.982	3.584	−20.17
8	2.528	3.451	−36.5
0	2.082	2.999	−44.01

observed that the 22 nm and 16 nm technology node power saving become −ve (i.e., power consumption increases) at 33% and lower data activity factor. Thus, higher data activity factor is more suitable for ICG.

Further to analyze the effect of frequency at 33% data activity factor where for 16 nm technology node power saving became −ve, the power consumption and power savings of TG based D flip-flop with and without ICG circuitry are studied for all selected technology nodes by varying the clock frequency. The analysis for 32 nm (shown in Table 5), for 22 nm (shown in Table 6) and 16 nm (shown in Table 7).

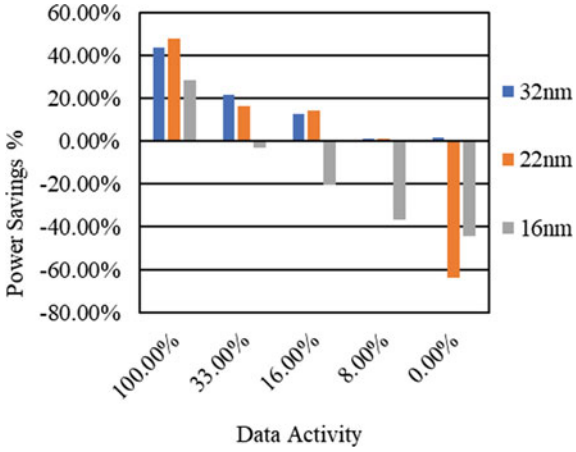

Fig. 8 Percentage of power savings at different technologies using ICG with varying data activity factor

Table 5 Average power dissipation and power savings for 32 nm technology at different clock frequency (data activity factor = 33%)

Clock frequency (f_{clk}) Unit: MHz	P_{avg} (w/o ICG) Unit: nW	P_{avg} (with ICG) Unit: nW	% Power savings
5	2.290	2.252	1.60
16.67	6.690	5.245	21.59
50	18.566	12.965	30.16
200	69.437	45.824	34.00

Table 6 Average power dissipation and power savings for 22 nm technology at different clock frequency (data activity factor = 33%)

Clock frequency (f_{clk}) Unit: MHz	P_{avg} (w/o ICG) Unit: nW	P_{avg} (with ICG) Unit: nW	% Power savings
5	2.301	2.144	6.81
16.67	5.518	4.621	16.25
50	14.370	9.259	35.56
200	52.269	30.590	41.47

The graph in Fig. 9 shows that even at moderate activity factor of 33%, the percentage of power savings with ICG of TG based D flip-flop is significant at its higher clock frequency of operation (50 and 200 MHz) and true for all the technology nodes, viz. 32 nm, 22 nm, 16 nm. The interesting observation is 16 nm technology which earlier showing −ve power saving (at lower data activity factor) at 16.67 MHz clock frequency now also shows significant power saving at 50 and 200 MHz Thus, such type of ICG in a TG based D flip-flop is suitable for saving power only for

Table 7 Average power dissipation and power savings for 16 nm technology at different clock frequency (data activity factor = 33%)

Clock frequency (f_{clk}) Unit: MHz	P_{avg} (w/o ICG) Unit: nW	P_{avg} (with ICG) Unit: nW	% Power savings
5	2.285	2.453	−7.35
16.67	4.010	4.141	−3.26
50	8.745	5.924	32.25
200	27.804	15.804	43.15

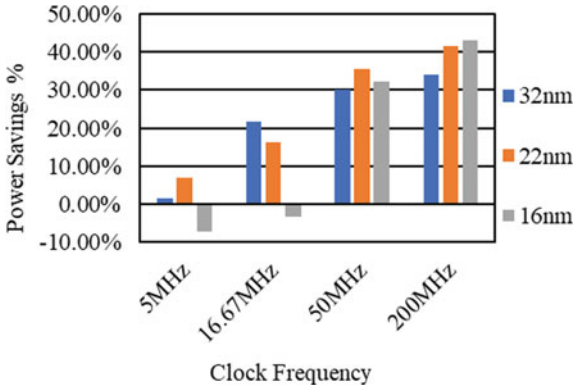

Fig. 9 Percentage of power savings at different technologies using ICG with varying clock frequency

higher clock frequency and/or high data activity factor. As technology node reduces, the effect of ICG at lower technology node reduces at either low clock frequency or lower data activity factor. Thus, high speed, high activity is suitable candidate for implementing suggested ICG technique in TG based D flip-flop. The comparative analysis of power in a flip-flop circuit with and without ICG considering data activity factors, clock frequency and technology node is not observed in literature.

4 Conclusion

The work presented an analysis of a TG based D flip-flop with and without ICG technique to study power dissipation and power saving considering the data activity factor and frequency. The results were also compared for 3 technology nodes (32 nm, 22 nm, 16 nm) to include the effect of technology scaling. It is observed that the ICG technique in a TG based D flip-flop is suitable for saving power for higher clock frequency and high data activity factor. The effect of ICG technique at lower technology node reduces either at the lower clock frequency or at the low data activity factor. The high speed and/or high activity circuits designed using higher technology nodes (where normal power dissipation is generally more) the ICG technique in a

TG based D flip-flop is advantageous for larger power saving. Similar analysis can be applied to other flip flops.

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Design of Ku Band HEMT-Based Class AB Amplifier

Manoj Kumar, Sukwinder Singh, and Deepti Kakkar

1 Introduction

Ku frequency band extends from 12 to 18 GHz and is mostly used for satellite communication. Because of the higher frequency, smaller dish antennas can be deployed to receive the signals, and antennas array can be used to increased directivity, power, gain, and to maximize the signal to interference plus noise ratio (SINR). Ku band also provides flexibility to the users as it has a smaller dish size, so it offers a cheaper and focused beam. As compared to Ka band operations, Ku band suffers less rain fade.

There are various active devices like MESFET, MOSFET, HEMT, etc., which are used for amplifier designing and each active device has some advantages and disadvantages. High electron mobility transistor (HEMTs) is one of the most preferred choices because these devices can operate over high frequencies. GaN HEMTs have high gain and high PAE. This reduces DC power consumption in the circuit, and hence, circuit size and designing cost are reduced because of the reduced heat dissipation circuit for the amplifier [1, 2].

GaN HEMTs have high operating voltage, so it helps to obtain the high power delivered in the load [1]. For designing an amplifier, it is very important to know the specification of the active device. There are many parameters like gain, power, PAE, operating voltages and frequencies which are dependent on the active device [3]. For linearity and efficiency, we can switch among various amplifier classes like A, B, AB, C, F and inverse class-F. Class A amplifier is linear, but efficiency is only 50%.

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In class B operation, the user can get a maximum theoretical efficiency of 78.5%, but it is somewhat nonlinear. Class C amplifier is highly nonlinear as compared to both class A and class B. Class AB amplifier provides a trade-off between linearity and efficiency [4, 5]. In this paper, a Ku band RF power amplifier is designed for satellite communication.

2 Literature Review

Ying Chen et al. discussed a Ku band RF power amplifier with 1 W of output power. The amplifier was designed and implemented in MMIC. This power amplifier used 16 active devices and then operated in phase to obtain a combined output RF power of 1 W. A 16 way output combiner was implemented in such a way that it transformed the 50 Ω standard load impedance into optimum load as seen by active devices. In this manner, the transmission line could have larger lengths, so to reduce it, the inductors were used. The MMIC for this design provided a power-added efficiency (PAE) of 37.5% [6].

G. Christopher Barisich et al. discussed a 3-stage C, X, Ku band GaN PA. The amplifier provided 5 W power output and power added efficiency (PAE) of 13% over frequencies 6–17 GHz. While comparing the performance, both frequency and bandwidth are important parameters since at higher frequencies, device parameters are lower and matching is quite complex. For the wideband power amplifier, the hybrid implementation is done in comparison with the MMICs. Distributed power amplifiers required a large chip to provide a similar performance [7].

Aliraza Yousefi et al. discussed a Ku band RFPA which was based on class AB pHEMT technology and design utilized a multistage architecture. A step by step procedure is explained which can be used to design a multistage amplifier for any frequency band and other specifications. This amplifier design provided an RF output power of 37 dBm along with the power added efficiency of 37% [8].

Hao et al. discussed a Volterra series-based power amplifier, for calculating the nonlinearity of a power amplifier circuit. This was used to calculate the best bias circuit for maintaining a balance between efficiency and linearity [9].

3 Circuit Description

3.1 DC Analysis

Before designing an amplifier, it is necessary to find out appropriate bias point, so a DC simulation was done using the GaN HEMT model while changing the default peak drain current by 2 A in the Keysight ADS program. The DC simulation circuit

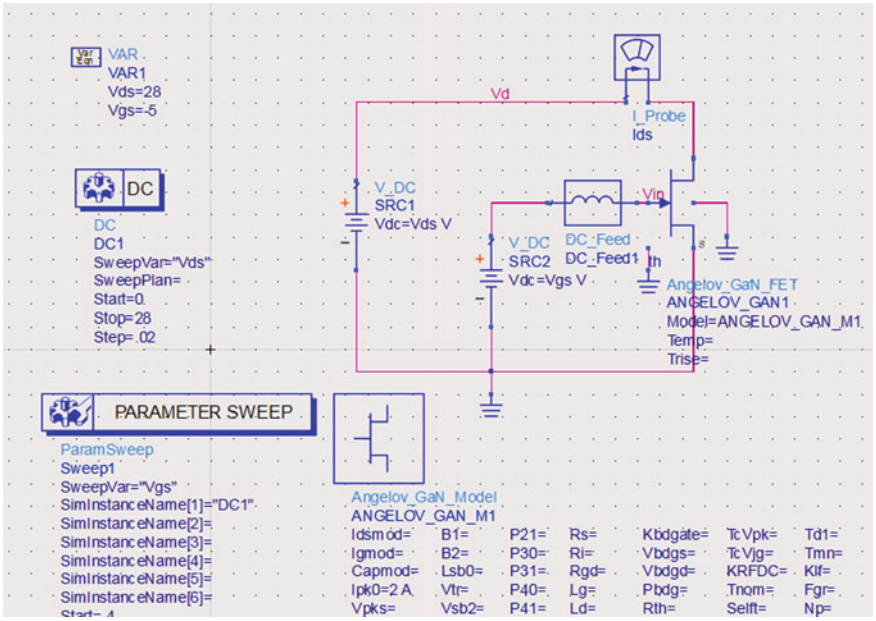

Fig. 1 DC bias circuit

consists of active device and variable drain and source voltages connected as shown in the figure in order to obtain the I–V characteristics.

After simulating the circuit (shown in Fig. 1), I–V characteristic of the HEMT device is calculated as shown in Fig. 2. Generally, the bias point for class A amplifier is taken as a voltage at which the drain current is half of the maximum value of it [3].

For class B amplifier, the bias point is at the threshold voltage. So the bias point for class AB amplifier can exist anywhere but in between the bias point of class A and class B amplifier [3, 4]. For our amplifier design, the bias point was taken at voltage $V_{gs} = -2.25$ V, $V_{ds} = 28$ V and $I_{ds} = 147$ mA.

3.2 Block Diagram for Class AB Amplifier

The proposed circuit for class AB amplifier was designed using Keysight advanced design system (ADS). The selection of the GaN HEMT is based on its specifications like power, gain, efficiency and operating frequency range. The block diagram for the class AB amplifier is shown in Fig. 3.

The source is the RF input power (dBm) with an input impedance of 50 Ω. The input matching network is used to deliver the maximum power from RF input source to the next stage for the desired range of frequency as the matching is frequency-dependent. Gate and drain bias network consist of DC source along with the DC feed

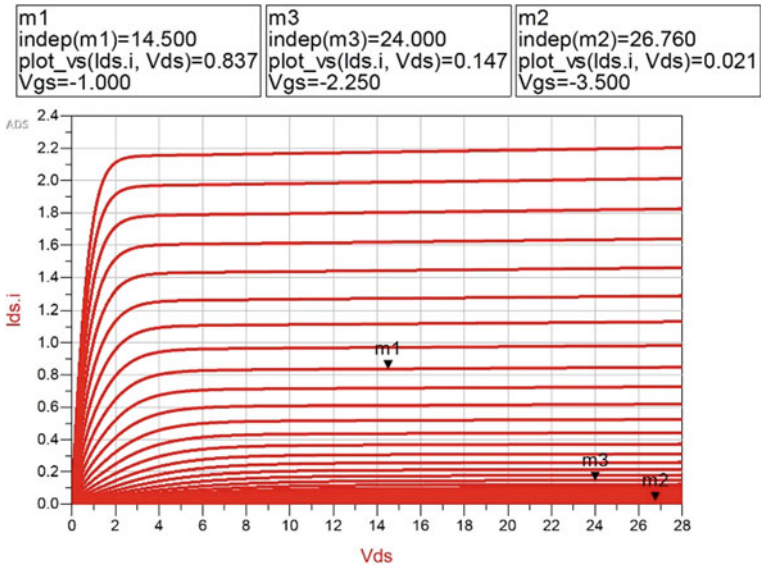

Fig. 2 *I*–*V* characteristics of GaN HEMT

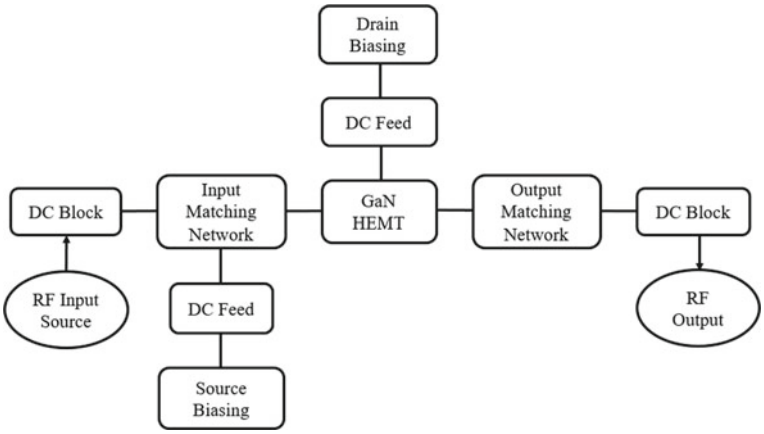

Fig. 3 Block diagram for class AB amplifier

component which can be realized by the stub of quarter wavelength and an open stub that provides a high impedance to be seen by the RF input path.

3.3 *Load Pull Analysis*

Load pull analysis is done to find out the optimum value of the load for which the power delivered to load is maximum or the efficiency is maximum or for maintaining a trade-off between the power and efficiency. The circuit for load pull analysis is shown in Fig. 4. In load pull analysis, different values of the load impedances are checked to find the optimum one which provides the maximum output power, gain and PAE.

In load pull analysis, the maximum power delivered was 40.253 dBm along with 15.253 dB; gain at input power of 25 dBm and maximum PAE was 48.078%. The values of load impedance for different parameters are shown in Table 1 (Fig. 5).

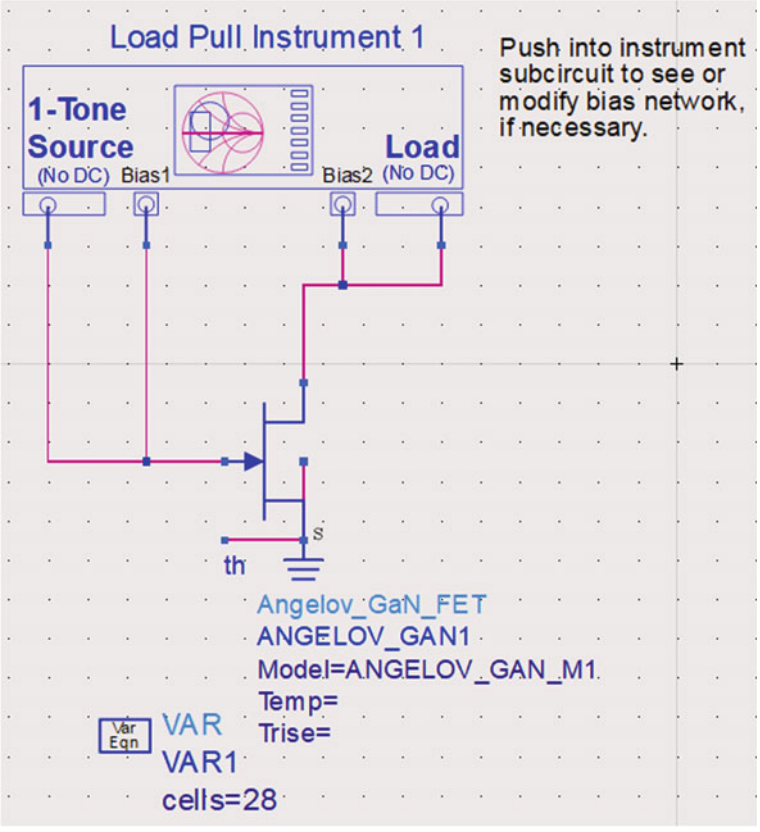

Fig. 4 Load pull simulation circuit

Table 1 Optimum values of load

Optimum value of load	For maximum power (and gain)	For maximum PAE
	12.534 + j3.926 Ω	14.249 + j4.145 Ω

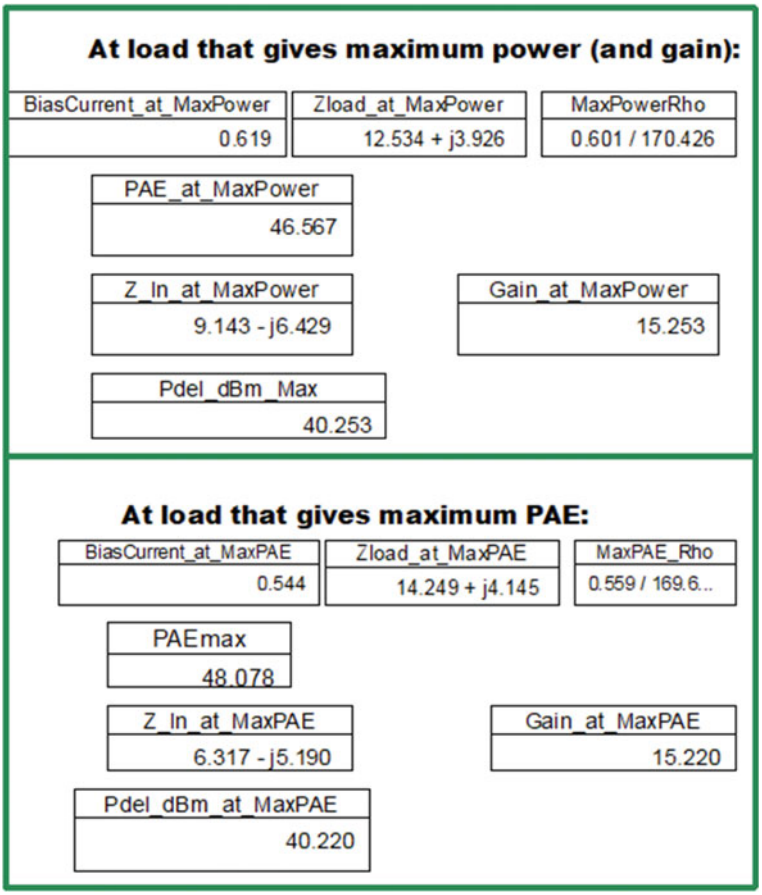

Fig. 5 Load pull simulation results

3.4 Impedance Matching

After load/source pull simulation, we get the optimum value of source and load impedances, but in our amplifier design, the values of standard source and load impedance are 50 Ω, so to operate the amplifier with these impedances, impedance matching is performed. The purpose of impedance matching is to maximize power transfer or minimize reflections between the two stages. In our design, the impedance matching will transform the effective impedance at input and output ports to 50 Ω.

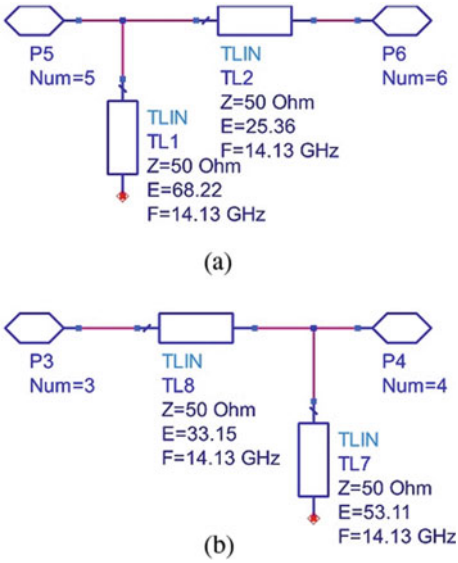

Fig. 6 **a** Input matching network, **b** Output matching network

Figure 6a, b are the input and output matching network, respectively. The impedance matching is done using distributed elements by using Smith chart utility in Keysight ADS.

In the input matching, standard 50 Ω impedance is matched with $6.317 - j5.190\ \Omega$, and the output impedance of $14.249 + j4.145\ \Omega$ is matched with 50 Ω.

4 Simulations and Results

4.1 Power Added Efficiency (PAE)

Maximum of 34.27% PAE was achieved (Fig. 7). Basically in class AB operation the efficiency ranges between 50 and 78.5% theoretically. For this design, the PAE could be achieved more than 34.27%, but this could result in degraded linearity.

4.2 Gain

Graph of gain while varying input drive P_{in} is shown in Fig. 8. Initially, the gain increases with the increase in the input power P_{in} up to 17.318 dB at 17 dBm and then decreases to 13.46 at 25 dBm input power. The amplifier delivers low output power for obtaining the high gain.

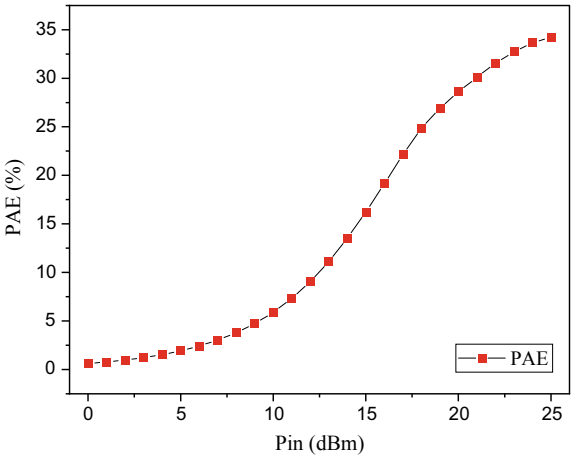

Fig. 7 PAE versus P_{in} curve

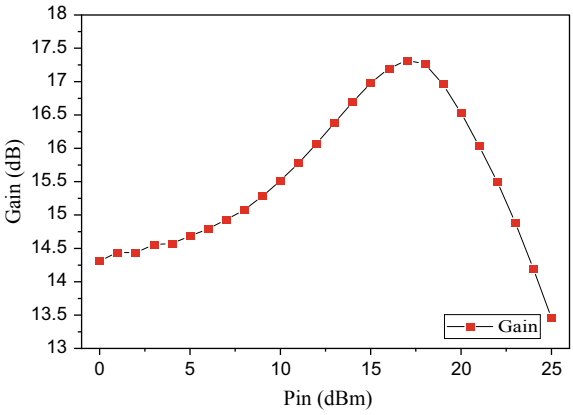

Fig. 8 Gain versus P_{in} curve

4.3 Power Delivered

P_{in} versus P_{out} curve is shown in Fig. 9, and the relation between the P_{in} and P_{out} is almost linear. To obtain the high PAE and high power, the drain bias voltage V_{ds} should be lowered. The maximum achieved power is 7.01 W (38.46 dBm).

4.4 Matching Network Responses

Figures 10 and 11 show the frequency response of input and output matching network, respectively, for the frequency range 13.75–14.5 GHz.

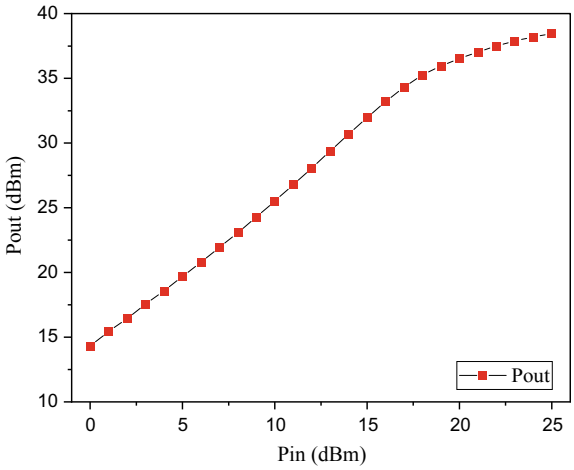

Fig. 9 P_{out} versus P_{in} curve

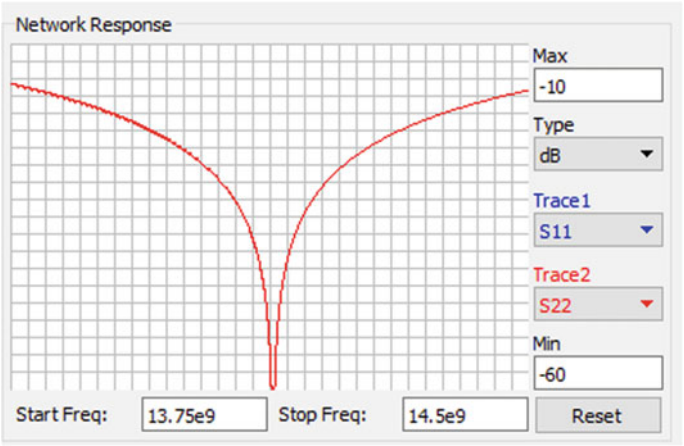

Fig. 10 Input matching curve (S_{11})

5 Conclusion

Ku band HEMT-based class AB amplifier has been completely designed and the maximum power achieved is 7.01 W. The maximum gain achieved is 17.318 dB at 17 dBm input drive along with the 34.27% PAE at centered frequency of 14.125 GHz. Our future work expansion is to design a multistage amplifier and fabrication of the complete design (Table 2).

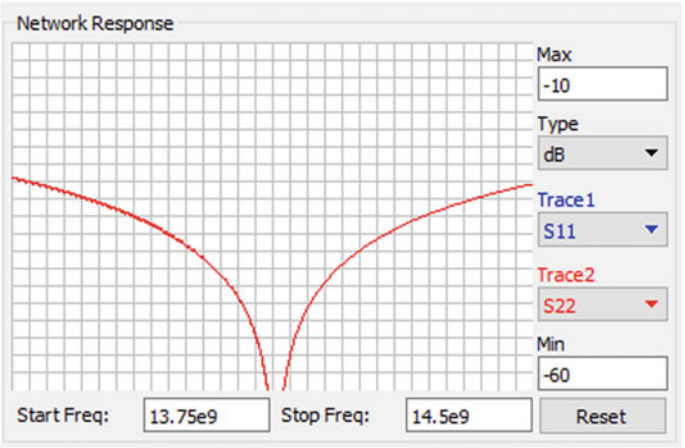

Fig. 11 Output matching curve (S_{22})

Table 2 Comparison between different works

Refs.	Author	Frequency (GHz)	PAE (%)	Gain (dB)	Power (dBm)
	This work	**13.75–14.5**	**34.27**	**17.318**	**38.46**
[6]	Chen et al.	13.5–14.5	37.5	10	30
[7]	Christopher Barisich et al.	6–17	18	18	38
[8]	Yousfi et al.	13–19	37	15	37
[10]	Maassen et al.	13.75–14.5	15	23	46.98

Bold refers to the work presented in this paper

Acknowledgements We thank the VLSI design group of NIT Jalandhar for their interest in this work and useful comments to draft the final form of the paper. The support of DST-SERB Project (ECR/2017/000922) is gratefully acknowledged. We would like to thank NIT Jalandhar for lab facilities and the research environment to carry out this work.

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X Band Class F Power Amplifier for Satellite Communication

Akash Gaikwad and Sukwinder Singh

1 Introduction

Next-generation satellite communication demands a high radio frequency power amplifier (PA) with high efficiency, output power and gain. There are different classes of PAs for achieving high output power and efficiency such as class E and F. There are some advantages and disadvantages for this PAs concerning difficulties in implementation, high output power, bandwidth limits, etc [1, 2].

Power amplifiers can be categorized on the basis of linearity (linear and nonlinear PAs). They can also be classified as biasing and switching class PAs. Minimum harmonic power is generated in linear PAs. Nonlinear PAs operate near to the saturation region, and hence, more harmonics are generated. PAs can be classified based on efficiency, conduction angle and quiescent point. Class A, Class AB, Class B and Class C are biasing PAs, and class E and F are the switching PAs which is classified based on connected network configuration to the active element. Class E and F are switching PAs which are highly nonlinear PAs [1–4].

Conceptually class F PAs can achieve 100% efficiency with harmonic power delivered to the load. Class F PA achieves high efficiency by the help of harmonic resonators. Class F PAs are based on proper termination of harmonics such as odd harmonics when it is open and even harmonics when it is short. Shaping circuits are used to shape the current and voltage waveform applying open and short termination at odd and even harmonics. With the help of shaping current and voltage waveform outcomes the half sinusoidal waveform for the current and the voltage, it is square waveform. For that reason, with decrease in overlapping between voltage and current waveform at the drain, the class F PA achieves maximum efficiency. Proficiency of

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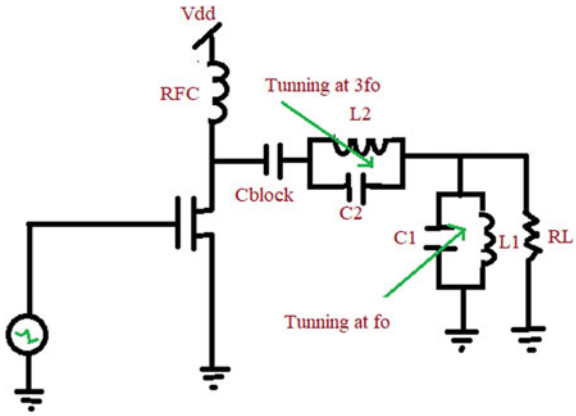


Fig. 1 Design of PA for 3rd harmonic [2]

Table 1 Comparison of different X band PA

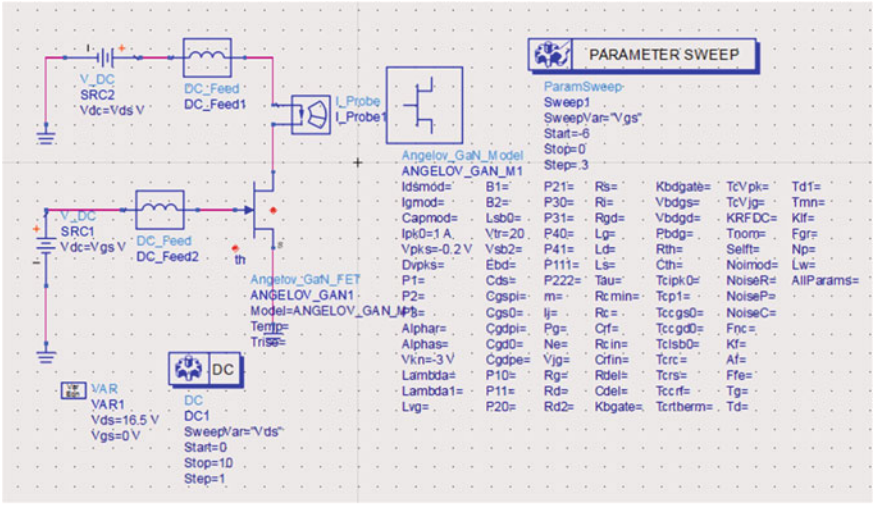
Refs.	Frequency (GHz)	PAE	Gain	Output power (dBm)
This work	11.75	52%	15 dB	30
[1]	7.9–8.25	55	16.2	36.5
[5]	8–8.3	48	12	37
[6]	8.2	33.62%	8.1 dB	31.25

high output power and excellent efficiency, engineers are more attentive toward class F PA [2, 4] (Fig. 1).

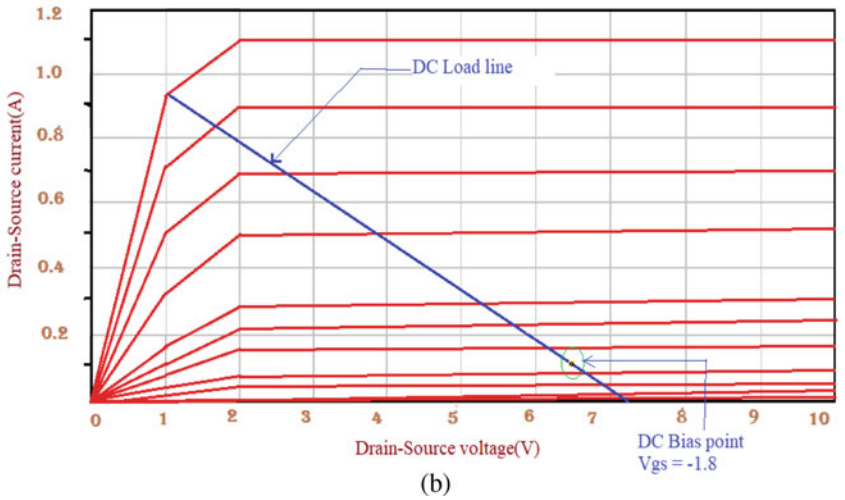
Based on frequency, output power and power added efficiency, performance of different X band power amplifiers is shown in Table 1.

2 DC Biasing

Quiescent point of the designed class F PA is in class AB PA. With the help of DC biasing, the device can operate in the desired mode. DC simulation is done by using GaN HEMT in ADS shown in Fig. 2a. Gate bias swept for V–I characteristics of the PA is 0 to − 6 V. The peak current is considered as 1 A, which is a typical value for GaN HEMT. Drain bias voltage is 16.5 V for class F PA, and the gate bias voltage is − 1.8 V which is chosen from the V–I characteristics of the device appeared in Fig. 2b [2].



(a)



(b)

Fig. 2 **a** DC bias simulation. **b** V–I characteristics of nonlinear transistor model

3 Simulation and Results

Simulation of class F PA is performed as shown in Fig. 3. Operating frequency of class F PA is 11.75 GHz which is useful for satellite applications. Drain voltage is 16.5 V, and gate voltage is − 1.8 V. In class F PA, control of harmonics is essential in the design. At the third harmonic frequency, $L1||C1$ is a parallel resonator that resonates third harmonic frequency; because of this for third harmonic is open.

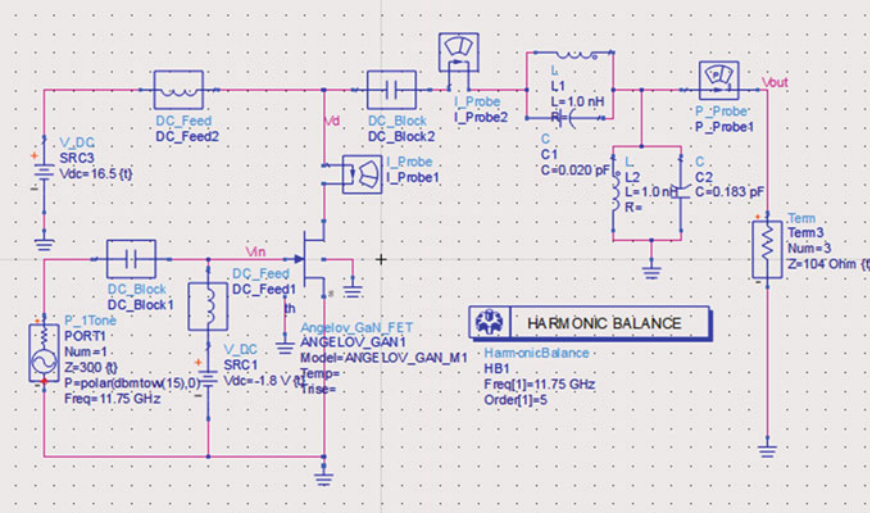


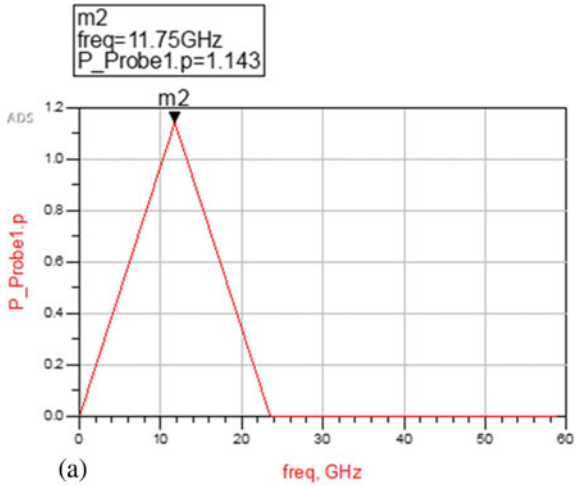
Fig. 3 Designed of class F power amplifier

Similarly, $L2 \| C2$ is shunt parallel resonator that resonates at fundamental frequency, so that other harmonics (excluding third) are short circuited to ground.

GaN can operate at a higher temperature and it can work at a higher voltage. Advantages of GaN HEMT are high breakdown voltage, wide bandgap and high operating frequency, etc [7]. Hole mobility and electron mobility are high in GaN which provides smaller knee voltage to device channel is turned on. Efficiency is one of the parameters that play a major role in power amplifier design. High efficiency in mobile systems means a longer battery life which further improves the mobility of such devices. High efficiency of fixed wireless devices will reduce the losses due to the high temperature and decrease maintenance costs. In this, we achieve 52% efficiency and 15 dB gain for class F PA [2].

Maximum output power of this design is shown in Fig. 4a. Output power of the class F PA is 1.143 W (30.58 dBm). Frequency domain analysis of drain voltage is shown in Fig. 4b. Proper termination of harmonics in the design of class F PA shows open for odd harmonics and short for even harmonics [3].

Drain current (I_D) and drain voltage (V_D) waveforms in the time domain for class F power amplifier are shown in Fig. 5. It satisfies the ideal case of class F PA which the output current forms even harmonics and produces a sinusoidal waveform which is half of its waveform, though the drain voltage generates odd harmonics and produces the square waveform. Decrease in overlapping between the voltage and the current waveforms at the drain leads to increase in efficiency of class F PA. Control of harmonics leads to waveform flattening which in turn reduces dissipated harmonic energy.



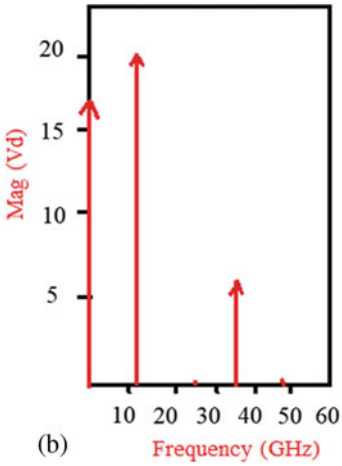


Fig. 4 **a** Output power of class F PA. **b** Harmonics of drain voltage in frequency domain

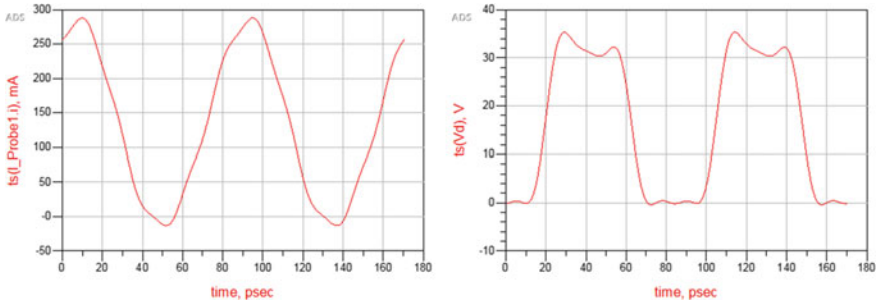


Fig. 5 Time domain waveforms of I_D and V_D for class F PA

4 Conclusion

Class F amplifier has been designed in X band with operating frequency of 11.75 GHz. The PA achieved 52% efficiency with output power of 30 dBm and gain of 15 dB. The efficiency was increased by controlling the harmonics generated. This single stage Class F will be extended to multistage PA for higher output power and gain.

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Investigation of GNR Based Meta-Material Antenna for Single and Dual Band THz Applications

Ritesh Kumar Kushwaha, P. Karuppanan, and Nand Kishore

1 Introduction

A terahertz (THz) band lies in-between the millimeter and visible frequency range in the spectrum. It has various distinctive properties such as larger bandwidth, high data rate (up to 100 Gbps), high resolution, noninvasive, and able to see through the wall [1, 2]. Hence, it is useful for high-speed wireless communication, imaging, medical industries, agriculture, etc. However, high attenuation loss is the THz band due to the absorption of high frequencies by water molecules present in the atmosphere [3]. Therefore, an efficient THz system is required to reduce the path loss issue. Initially, only photonics-based THz devices and systems have been evolved due to the unavailability of electronic devices and materials. However, from the last two-decade electronic devices and some novel materials are investigated; therefore, Frequency Multiplier Devices (FMD) and graphene materials [4, 5] have been explored. In the THz wireless systems, graphene-based devices and antennas are preferred due to its exceptional electrical and mechanical properties. Graphene is the only renowned two-dimensional material and defined by Kubo's surface conductivity formula in terms of temperature, chemical potential, frequency, and scattering rate. One of the most exciting features of this material is its capability to sustenance transverse magnetic (TM) surface plasmonic modes in the THz band that leads to low loss plasmonic devices and transceiver antennas [6]. In the similar literature, Aidi et al. [7] has reported graphene-Nano-ribbon (GNR) based dipole antenna in which widely explored the resonance characteristics and Surface Plasmon Polariton (SPP) of graphene in the THz band. A graphene patch antenna with metamaterial substrate

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has been reported in [8], in which radiation characteristics at 1.67 THz frequency. However, the authors achieved only 16.6% radiation efficiency from this antenna. The detailed theoretical and numerical analysis of graphene's SPP has been explored in the THz band [9]. Also, a graphene-based split-ring resonator (SRR) with the different prototype structures was reported and analyzed its performance characteristics in the THz regime [10, 11]. Nevertheless, most of the graphene antennas have not intended to improve the antenna gain.

In this article, a 1 × 2 graphene-based rectangular ring antenna array is structured on PBG substrate utilizing proximity feed methods to achieve high gain and radiation efficiency. Section 2 investigates the graphene formulation and GNR SRR. The design and analysis of a GNR antenna are demonstrated in Sect. 3. Further, Sect. 4 describes the result and discussion of a proposed GNR antenna. Finally, the conclusion of the entire work is discussed in Sect. 5.

2 Theoretical Formulation and Analysis of Graphene

Graphene has numerous applications in the microwave and THz frequency band due to its remarkable properties such as high conductivity (carrier mobility ~ 200,000 cm^2/Vs), high tensile strength (Young's modulus: 1.10 TPa), transparent nature (1 atom thin ~ 0.345 nm), mechanical flexible (elasticity ~ 20%) and high surface to volume ratio [12, 13]. Moreover, graphene conductivity can be controlled by applying the dynamic tunning and layers stacking method; this revolutionized phenomenon could be used to develop a reconfigurable antenna by tunning the external bias voltage [14].

2.1 Mathematical Analysis of Graphene Surface Conductivity

The graphene conductivity is evaluated from the Kubo's formula. It consists of two parts, namely intraband and interband conductivity [9]. In lower THz band, interband conductivity can be neglected, whereas intraband conductivity (σ) of graphene can be expressed by:

$$\sigma_{\text{intraband}}(\omega) = \frac{-iq^2 k_B T}{\pi \hbar^2 (\omega - 2i\Gamma)} \left[2\ln\left(1 + e^{-\mu_c / k_B T}\right) + \frac{\mu_c}{2k_B T} \right] \tag{1}$$

where k_B and $\hbar$ are the Boltzmann's and reduce plank's constant respectively, μ_c is the chemical potential, Γ = scattering rate, T = temperature and ω is the radian frequency.

Also, the chemical potential of a graphene sheet is expressed by:

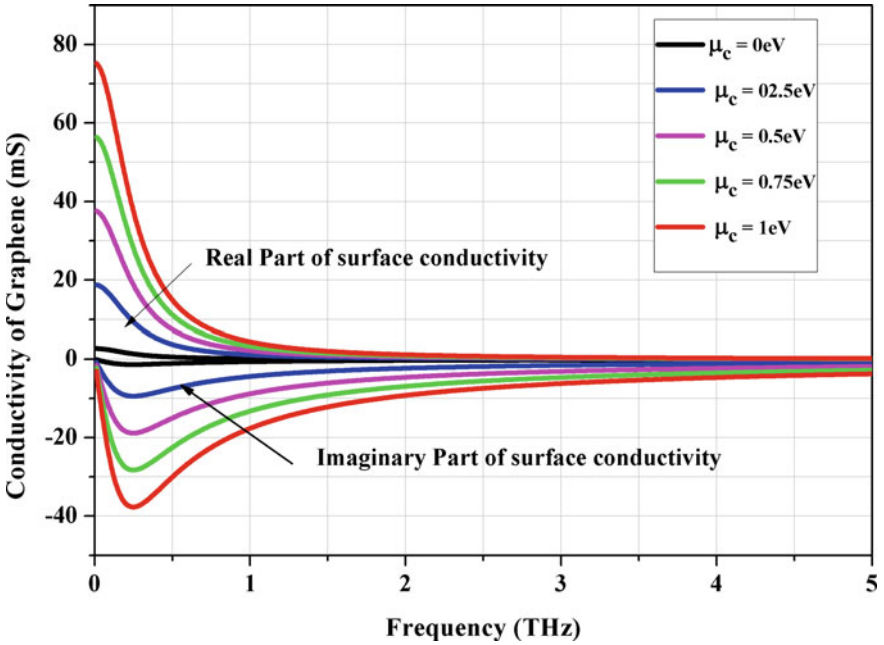

Fig. 1 Intra-band conductivity of graphene performance with different values of chemical potential

$$\mu_c = \hbar v_f \sqrt{\frac{\pi \varepsilon_0 \varepsilon_r}{ed} V_b} \tag{2}$$

where V_b = bias voltage, $v_f \approx 10^6$ m/s, $\hbar = 1.055 \times 10^{-34}$ J s and d is the thickness of substrate.

In Fig. 1, the real and imaginary values of intra-band conductivity is shown. It is clearly seen that the real part of conductivity is increased, but an imaginary part of conductivity is decreased while changing the chemical potential (μ_c) of graphene. We assume the graphene's relaxation time is 3 ps, the temperature is 300 K, and the thickness of 0.00335 μm throughout the manuscript.

2.2 Split Ring Resonator (SRR) Analysis

The behavior of SRR, such as transmission and reflection coefficients is analyzed in the THz frequency band. The unit cell concentric SRR is investigated by applying the wavefronts at either side with opposite directions. The mathematical formulation of the required values is given by [15]:

$$S_{11} = \frac{\Gamma_0^{-1}\left(1 - e^{-j2nk_0d}\right)}{1 - \Gamma_0^{-2}e^{-j2nk_0d}} \tag{2}$$

$$S_{21} = \frac{\left(1 - \Gamma_0^{-2}\right)}{1 - \Gamma_0^{-2}e^{-j2nk_0d}} \tag{3}$$

where S_{11} = reflection coefficient, S_{21} = transmission coefficient, d is max. dimension of the substrate, k_0 is the wave number. Γ_0 is represented by:

$$\Gamma_0 = (Z - 1)(Z + 1)^{-1} \tag{4}$$

where Z is the input impedance, represented by:

$$Z = \pm\left(\frac{S_{21}^2 - (1 + S_{11})^2}{S_{21}^2 - (1 - S_{11})^2}\right)^{-1/2} \tag{5}$$

The behavior of reflection coefficients (S_{11}) and transmission coefficient (S_{21}) in the operating frequency band is illustrated in Fig. 2. It is revealed that dual-band resonance occurs at 0.69 and 0.805 THz frequencies. Hence the proposed SRR can work dual-band frequencies.

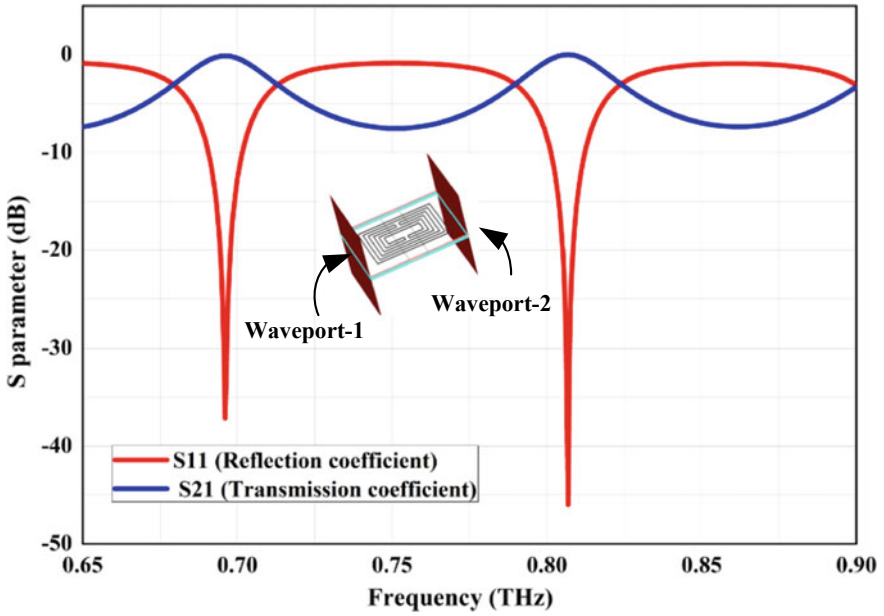

Fig. 2 *S*-parameter behaviour of SRR with frequency

3 Antenna Geometry

Firstly a rectangular patch is designed using the dimension extension technique [16]. Then the patch is miniaturized to form SRR. Finally, the antenna is placed at λ/2 distance to create an array. Figure 3 depicted the structure of the graphene-based

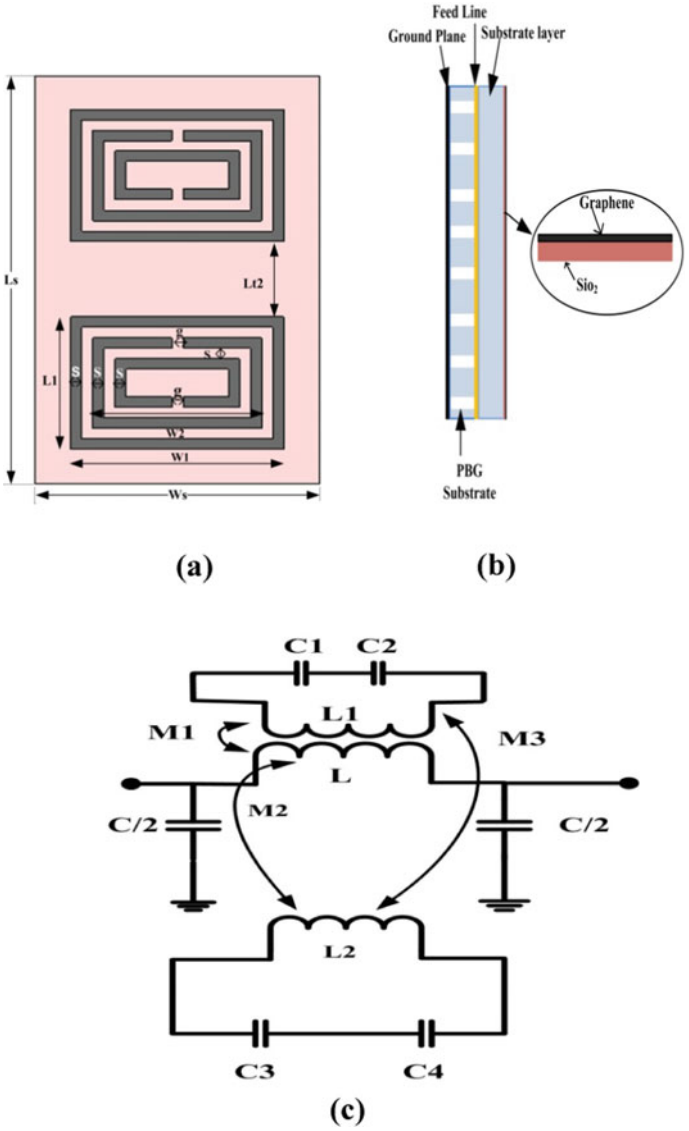

Fig. 3 Antenna geometry **a** top-down view, **b** left-side view, **c** equivalent circuit model

Table 1 Selected dimensions of projected antenna

parameters	Dimension
Outermost rectangular ring ($W1 \times L1$)	$520 \times 320\ \mu m^2$
Middle rectangular ring ($W2 \times L2$)	$460 \times 260\ \mu m^2$
Innermost slotted ring ($W3 \times L3$)	$400 \times 200\ \mu m^2$
Feed line ($W_f \times L_f$)	$150 \times 576\ \mu m^2$
Substrate and ground plane ($W_s \times L_s$)	$776 \times 576\ \mu m^2$
Separation distance and gap (g) between rings (S)	30 μm
Distance between Array (Lt2)	217 μm

rectangular SRR antenna array concentric with closed rectangular rings and mounted on the silicon dioxide (SiO_2) layer thickness of 0.285 μm, subsequent with the upper substrate layer. As a SiO_2 is a tremendous optical contrast, therefore these layers help to GNR visible. It is worth mentioning that a single layer graphene thickness (Δd) is only 0.335 nm; therefore, graphene stacking has been utilized here with ten layers that lead graphene to 3D structures. The lower dielectric subtracts a height of 12.5 μm, is the identical substrate with photonic bandgap structures. These PBG structures are the air cylindrical-circular holes and arranged in the periodic order to suppress the substrate's wave losses. The radius, height, and separation distance of the PBG structure is 30 μm, 12.50 μm, and 100 μm, respectively. The proximity microstrip feed line is the rectangular strip and sandwich between the upper and lower substrate material; its dimensions are 150 μm × 580 μm. The optimized dimensions of the proposed structure are illustrated in Table 1.

Also, the equivalent circuit model of proposed geometry can derive from the proposed design in terms of lumped inductance (L), capacitance (C). Figure 3c depicts the approximate frequency response models of the projected SRRs resonance circuit. The mutual inductance exhibits the magnetic coupling between the rectangular strip lines, and the stripline gap is in capacitance. Magnetic couplings of $M1$, $M2$ (self-coupling), and $M3$ (mutual-coupling). Henceforth, the proposed structure can be modeled as the tank resonant circuit with parameters i.e., $L1$, $C1$, $C2$, and $L2$, $C3$, $C4$.

Table 1 shows the optimum dimension values of projected geometry. The particle swarm optmization (PSO) technique has been adopted to get discrete values.

4 Simulated Results and Discussions

In this section, the radiation characteristics of the planned antenna are realized with its different simulation results.

Figure 4 illustrated the reflection coefficients (S_{11}) of a design antenna. The tunable properties can easily be analyzed by changing the chemical potential of graphene. The single band is observed at μ_c of 0 eV and obtained dual-band at 0.5 eV and

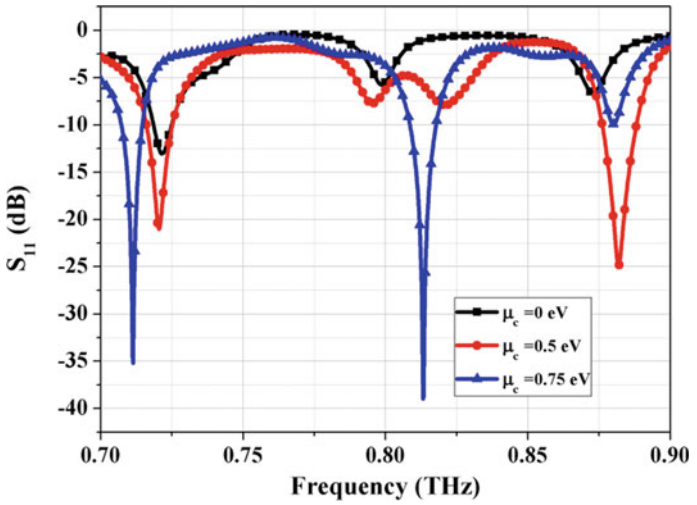

Fig. 4 Return loss versus frequency with different chemical potential

0.75 eV. The attained minimum S_{11} of − 38.99 dB with μ_c of 0.75 eV at resonance frequency at 0.8132 THz whereas the highest value of return loss is obtained at 0.7216 THz with 0 eV chemical potential. The corresponding fractional bandwidth (< − 10 dB) for a single and dual-band of operations is 6.35 and 15.9 GHz. Remarkably, these frequencies band showed various applications such as video-rate imaging, material characterization, wireless communications, explosive detection [15–18]. Therefore the design reconfigurable antenna would be satisfied with the single-band and dual-band necessity of the THz systems.

Figure 5 shows the VSWR performance in the THz frequency band. One may observe the least VSWR is 1.027 at 0.797 THz by applying 1 eV chemical potential. It is noticed that all VSWR values below 1.9; thus, the criteria of VSWR values 2:1 would be satisfied for optimum performance.

Figure 6 displays the gain of the designed GNR antenna in the operating frequency range. The antenna gain of 8.89 dB at 0.72 THz in single-band operation and the peak antenna gain is 10.16 dB observed at 0.882 THz in dual-band of operation. The corresponding –dB fractional bandwidth is around 160 GHz, with the lowest frequency at 0.74 THz. Moreover, μc at 0.5 eV, the excellent 3 dB gain bandwidth can be observed i.e., around 300 GHz. However, a peak antenna gain at the resonance frequency band is lower.

Figure 7 shows the radiation efficiency behavior with operating frequency and different μ_c of GNR. The realized minimum radiation efficiency is around 40.91% at 0.7216 THz with μ_c of 0 eV. Moreover, the maximum radiation efficiency is achieved around 91.45% at 0.879 THz with 1 eV chemical potential.

Figure 8 illustrated the proposed antenna's surface current distribution by applying chemical potential at 0.75 eV. It is observed that current density is more substantial at the SRR arms and feed line edges.

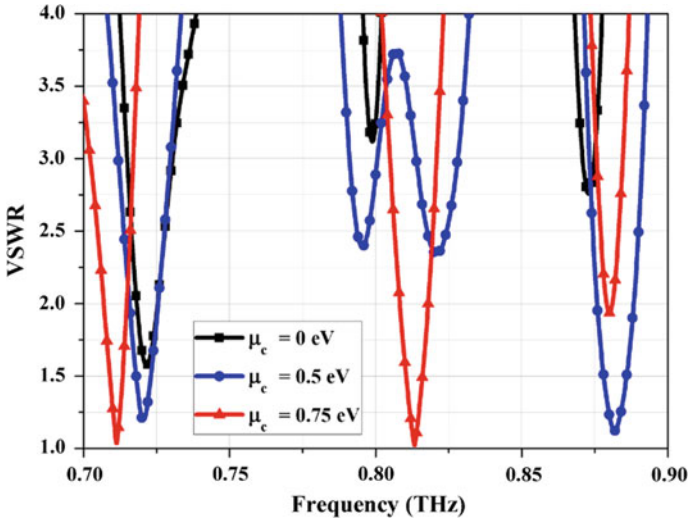

Fig. 5 VSWR (at chemical potentials of 0, 0.5 and 0.75 eV)

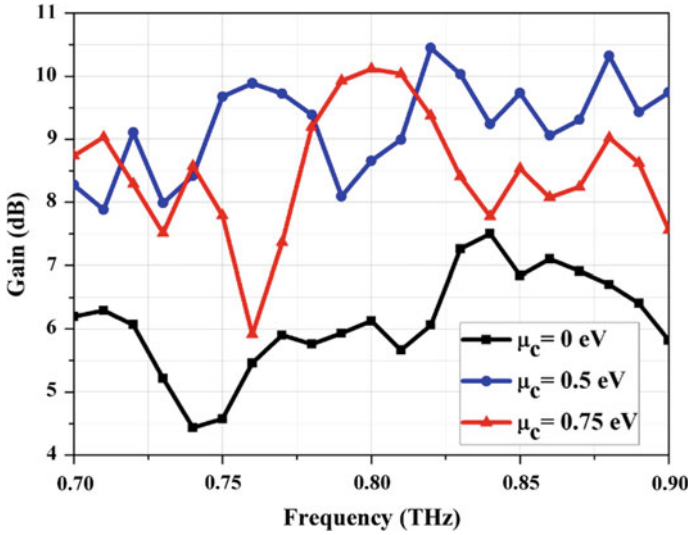

Fig. 6 Proposed antenna gain with different μ_c

The E-plane proposed GNR antenna's radiation performance is investigated with different μc of GNR, which are revealed in Fig. 9. It can be seen that with μ_c, the proposed antenna is more directive and minimum sidelobe level.

Figure 10 shows the 3D directivity pattern. The directivity of single-band resonance is achieved around 9.93 dB at 0.7216 THz by applying a chemical potential of

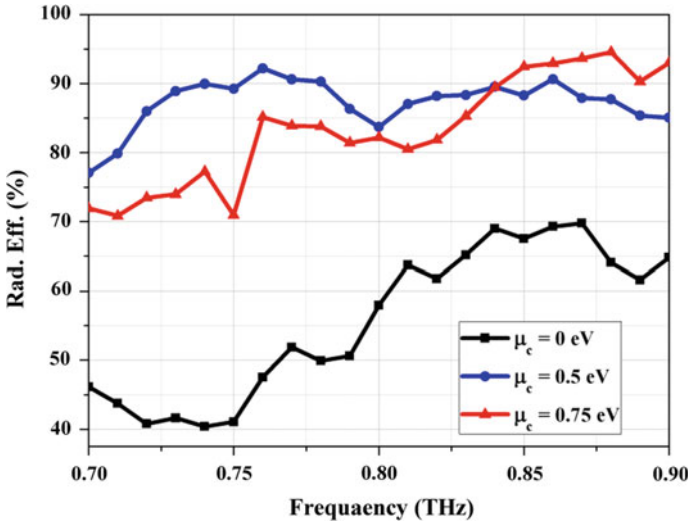

Fig. 7 Radiation efficiency performance with μ_c

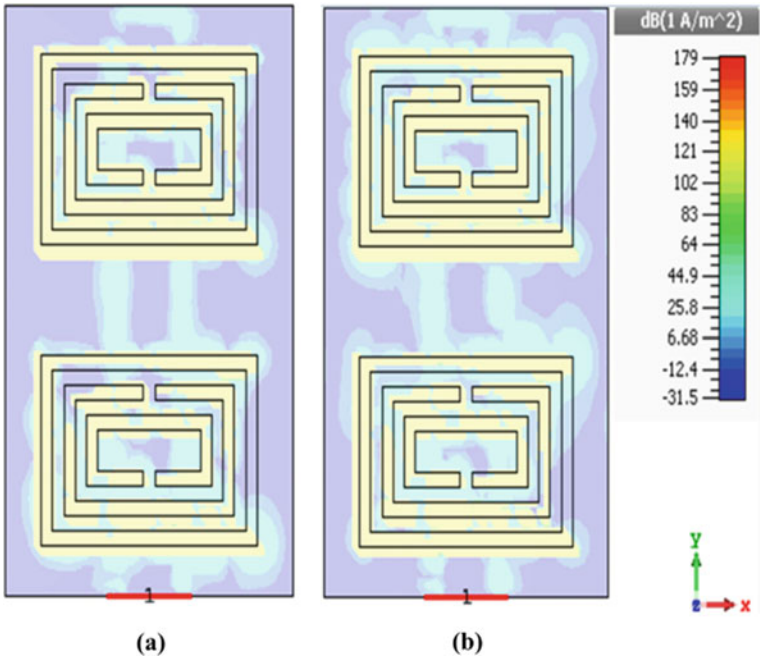

Fig. 8 Surface current distribution with μ_c of 0.75 eV **a** at 0.7114 THz (f31-single band), **b** at 0.8132 THz (f32-dual band)

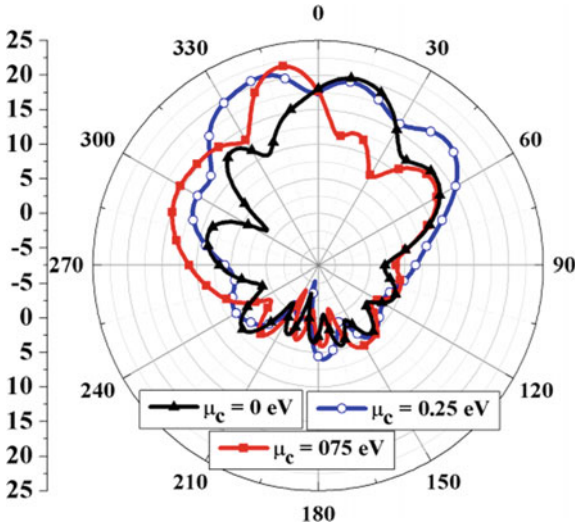

Fig. 9 E-plane radiation pattern (first bands) with different chemical potential

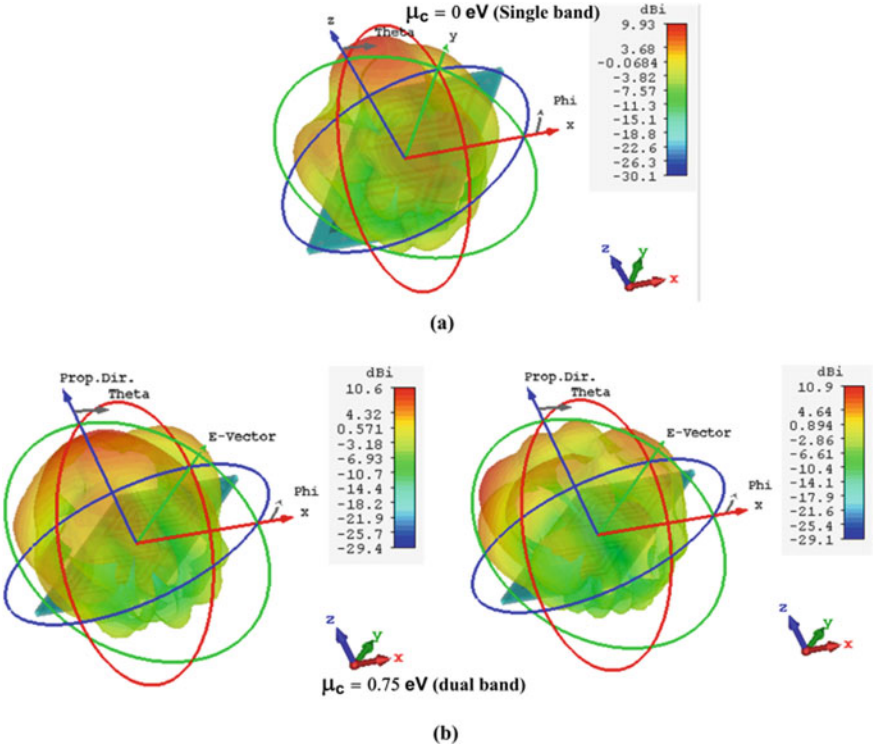

Fig. 10 Pattern directivity **a** at 0 eV first band **b** at 0.75 eV dual band

Table 2 Radiation performance of projected antenna compared to earlier work

	Chemical potential (eV)	Band	Resonance frequency (THz)	S_{11} (dB)	VSWR	Gain (dB)	Directivity (dBi)	Rad. efficiency (%)
Proposed work	0	Single	0.7216 (f0)	− 13.05	1.572	5.928	9.93	40.9
	0.5	Dual	0.7206 (f21)	− 21.01	1.21	9.045	9.802	86.18
			0.8819 (f22)	− 24.85	1.915	10.15	10.90	87.30
	0.75	Dual	0.7114 (f31)	− 35.20	1.071	8.91	10.5	71.26
			0.8132 (f32)	− 38.99	1.073	9.815	10.9	80.93
[19]	0.13, 0.19, 0.25, 0.36, and 0.5	Single	0.87, 1.03, 1.17, 1.34, and 1.6	− 12.5, − 28, − 27, − 14, and − 10.5	–	max. 1.8	–	–
[20]	0.1–1.2	Single	0.65–0.8	min. − 29	–	–	7.11	–
[21]	0.1–0.27	Dual	2.14–2.18	− 25.78	min. 1.03	max. 4.41	max. 6.1	67.7
			2.5–2.59	− 42.77	min. 1.02	max. 5.03	max. 7.06	60.8
[22]	0.16–0.26	Dual	3–9	min. − 42	–	–	max. 7.8	–

0 eV. Whereas, dual-band directivity of 10.6 and 10.9 dBi at 0.8132 THz by applying μc of 0.75 eV.

Finally, a proposed antenna's radiation characteristics are compared with other reported graphene antennas, listed in Table 2. On may be observed that targeted antennas are better radiation performance in comparison to earlier reported antennas.

5 Conclusion

The analysis and simulation of reconfigurable GNR antenna array have been accomplished in this article. Initially, the graphene conductivity behavior has been investigated and then developed a miniaturized patch GNR array with novel geometry of SRR. PBG substrate is employed in the bottom substrate to decrease the surface wave loss. The single and dual-band resonance is observed by varying the chemical potential that validates graphene's reconfigurable behavior. Single-band achieved with chemical potential of 0 eV and the dual-band achieved with 0.5 and 0.75 eV chemical potentials. The suggested frequency band of operation is appropriate for

numerous terahertz applications such as homeland, video imaging, and material characterization, security system using spectroscopy.

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Comparative Study of Silicon and $In_{0.53}Ga_{0.47}As$-Based Gate-All-Around (GAA) MOSFETs

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1 Introduction

In the modern society, there has been always demand for uninterrupted communication, fast computation, and high-quality entertainment with smaller electronic gadgets. MOSFETs are the backbone of these gadgets. Shrinking dimensions of MOS help to incorporate more features in a single chip, but at the same time due to shrinking in MOS dimensions the phenomena of short channel effects (SCEs) such as subthreshold characteristic, reduction in carrier's mobility, and gate tunneling currents come in the picture. However, the SCEs can be decimated through modification in MOS design.

Multigate devices [1–6] designs like FinFET, Omega FET, and gate-all-around (GAA) are analyzed over different parameters. The GAA MOSFET [6, 7] is becoming a cornerstone due to multidirectional electrostatic control over the gate, superior SCE immunity, and high packing density. In smaller-scaled devices, if the voltage at the drain is expanded, the potential barrier in the channel minimizes, which indicates that the gate loses its control over the channel, overseeing drain-induced barrier lowering (DIBL). This impact is due to the potential distribution from the source/drain region. However, GAA suffers from the low drive current [8]. To overcome the low drive current, the high mobility material $In_{0.53}Ga_{0.47}As$ is used to fabricate the GAA [9], which enhances the working speed at a reduced supply voltage. $In_{0.53}Ga_{0.47}As$-based

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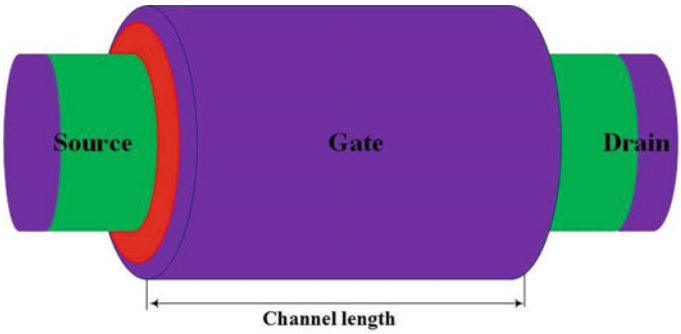

Fig. 1 3D schematics structure design of $In_{0.53}Ga_{0.47}As$-GAA MOSFET

gate GAA MOSFET provides a boost in drive current, excellent immunity to SCEs, enhanced gate-channel electrostatic, and high carrier mobility [10, 11]. Various materials appeared into consideration, among which indium–gallium–arsenide (InGaAs) is one of the considerably focused materials. In conclusion to the works mentioned above, it can be summarized that with reducing dimensions, $In_{0.53}Ga_{0.47}As$-GAA MOS is a fruitful solution for superior computational speed.

In this work, the performance of Si-GAA and $In_{0.53}Ga_{0.47}As$-GAA has been compared. Comparison of Si-GAA and $In_{0.53}Ga_{0.47}As$-GAA devices has been made in terms of variation in OFF-state current (I_{OFF}), ON–OFF-current ratio (I_{ON}/I_{OFF}), subthreshold swing (SS), drain-induced barrier lowering (DIBL), trans-conductance (g_m), and trans-conductance generation factor (TGF) characteristics on ATLAS, a three-dimensional (3D) device simulator from SILVACO.

2 Device Structure and Simulation Approach

The 3D schematics structure of $In_{0.53}Ga_{0.47}As$-GAA MOSFET for simulation is shown in Fig. 1. The cross-sectional view of $In_{0.53}Ga_{0.47}As$-GAA MOSFET is shown in Fig. 2. A thin Al_2O_3 oxide layer wraps over the nanowire channel region. Table 1 shows the device parameters used for simulation. The following models of 3D ATLAS device simulator from SILVACO have been included to perform the simulation of the proposed $In_{0.53}Ga_{0.47}As$-GAA device and Si-GAA devices [12], like drift diffusion charge transport model, Lombardi (CVT) model, concentration-dependent mobility model, and Shockley–Real–Hall (SRH) model.

3 Results and Discussion

Figure 3 presents the potential of $In_{0.53}Ga_{0.47}As$-GAA MOSFET at $V_{GS} = 0$ V and

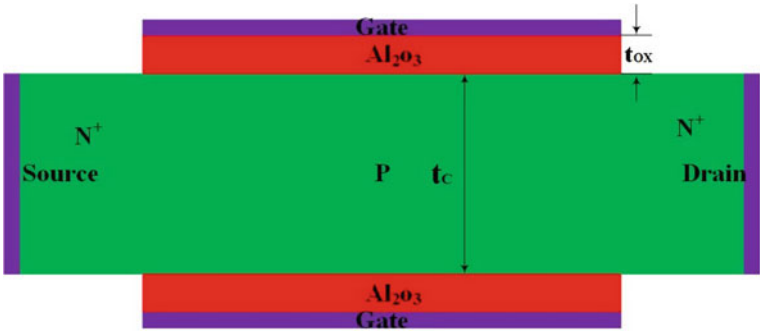

Fig. 2. 2D cross-sectional view of $In_{0.53}Ga_{0.47}As$-GAA MOSFET

Table 1 Silicon and $In_{0.53}Ga_{0.47}As$-based device parameters used for GAA MOSFETs simulation

Parameters	Si-GAA	$In_{0.53}Ga_{0.47}As$-GAA
Channel length (L_C) (nm)	20	20
Source/drain doping (N_D) (cm^{-3})	10^{20}	10^{20}
Channel doping (N_A) (cm^{-3})	10^{15}	10^{15}
Oxide thickness (t_{ox}) (nm)	1	1
Channel thickness (t_C) (nm)	10	10
Metal work-function (ϕ_M) (eV)	4.6	5.1

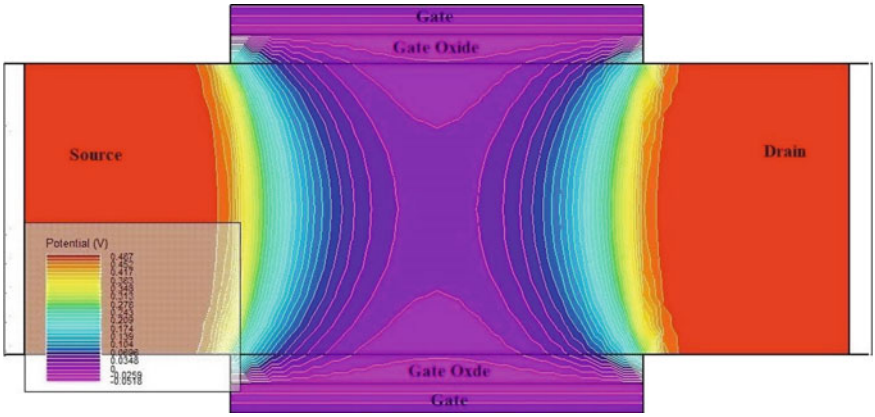

Fig. 3 The cross-sectional contour plot of potential for $In_{0.53}Ga_{0.47}As$-GAA MOSFET at $V_{GS} = V_{DS} = 0$ V

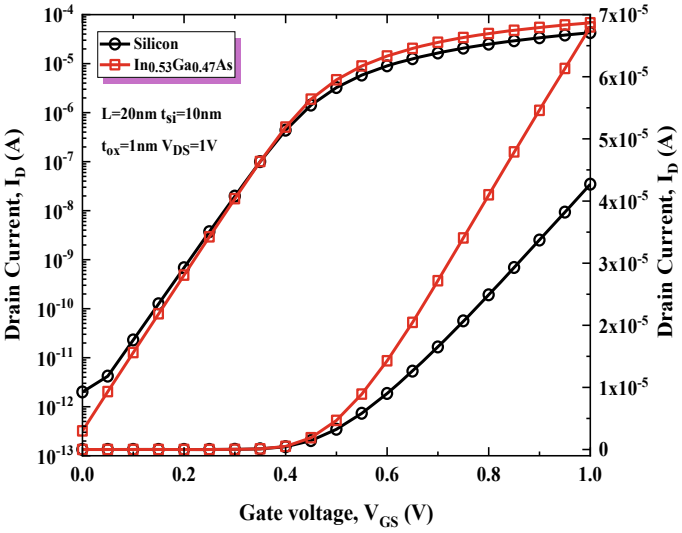

Fig. 4 Variation of drain current (I_D) of Si-GAA and $In_{0.53}Ga_{0.47}As$-GAA MOSFET versus V_{GS} at $V_{DS} = 1$ V

$V_{DS} = 0$ V. The plot indicates the lowest central surface potential, and it demonstrates the gate controllability over the channel region. Figure 4 shows the comparison of drain current (ID) of $In_{0.53}Ga_{0.47}As$-GAA and Si-GAA MOSFET as a function of gate-to-source voltage (V_{GS}) at a drain-to-source voltage (V_{DS}) = 1 V. The improvement of I_{ON} and I_{OFF} is analyzed in $In_{0.53}Ga_{0.47}As$-GAA MOSFET, as shown in Fig. 4. The ON-current is enhanced by 59.62%, but the OFF-current reduces by 84% of $In_{0.53}Ga_{0.47}As$-GAA MOSFET compared to Si-GAA MOSFET. It has occurred due to the high mobility material $In_{0.53}Ga_{0.47}As$ of the device channel with high gate oxide Al_2O_3. Hence, the $In_{0.53}Ga_{0.47}As$-GAA MOSFET is more satisfactory for high-speed switching applications and also low power consumption.

Figure 5 shows the comparison of drain current of $In_{0.53}Ga_{0.47}As$-GAA and Si-GAA MOSFET with V_{DS} at $V_{GS} = 1$ V. The improvement of drain current in $In_{0.53}Ga_{0.47}As$-GAA MOSFET from characteristics of the InGaAs is because the $In_{0.53}Ga_{0.47}As$ has higher mobility than silicon. The comparison between trans-conductance (g_m) of $In_{0.53}Ga_{0.47}As$-GAA and Si-GAA MOSFET against V_{GS} at $V_{DS} = 1$ V is illustrated in Fig. 6. The g_m is a crucial factor for analog and RF applications, and it is moreover essential to define an optimum bias point. For any device, the cut-off frequency is the peak at an optimum bias point. The graph displays that the $In_{0.53}Ga_{0.47}As$-GAA device discloses 53.33% more distinguished g_m than the Si-GAA MOSFET.

Figure 7 illustrates the comparison of TGF (g_m/I_D) of $In_{0.53}Ga_{0.47}As$-GAA and Si-GAA MOSFET against V_{GS} at $V_{DS} = 1$ V. The measurement of g_m and I_D is recognized as the trans-conductance generation factor (TGF). The highest TGF value is near the ideal amount of subthreshold swing 60 mV/decade. In the subthreshold

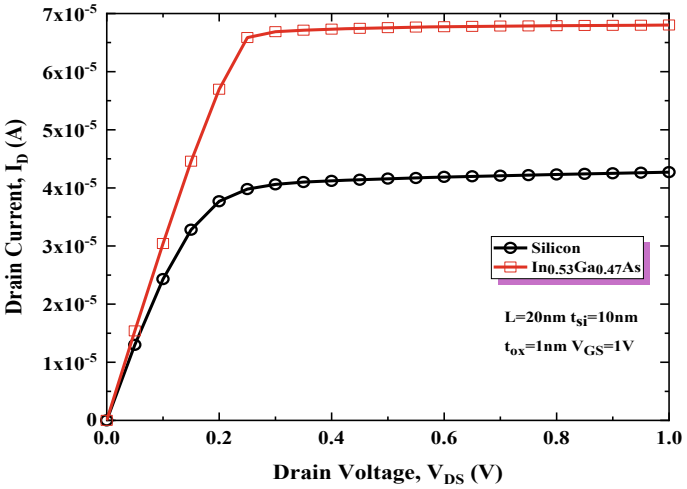

Fig. 5 Variation of drain current of Si-GAA and $In_{0.53}Ga_{0.47}As$-GAA MOSFET versus V_{DS} at $V_{GS} = 1$ V

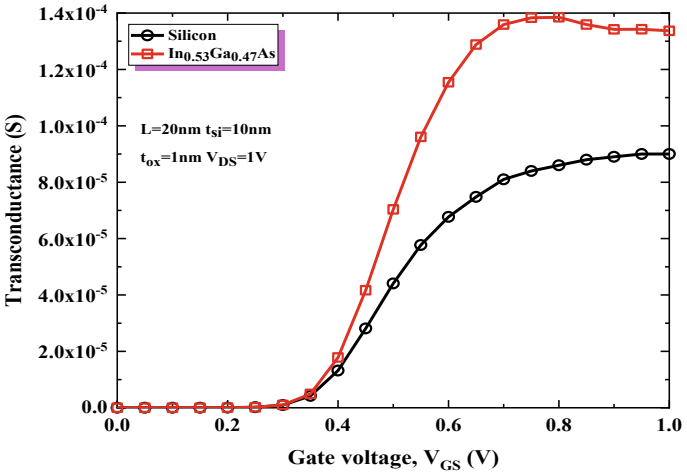

Fig. 6 Variation of trans-conductance (g_m) of Si-GAA and $In_{0.53}Ga_{0.47}As$-GAA MOSFET versus V_{GS} at $V_{DS} = 1$ V

region, TGF is vital for $In_{0.53}Ga_{0.47}As$-GAA MOSFET than the Si-GAA device. The more profitable value of TGF confirms the stable performance of the analog circuit even for low power supply.

Table 2 indicates the analog FOMs of Si-GAA and $In_{0.53}Ga_{0.47}As$-GAA MOSFET

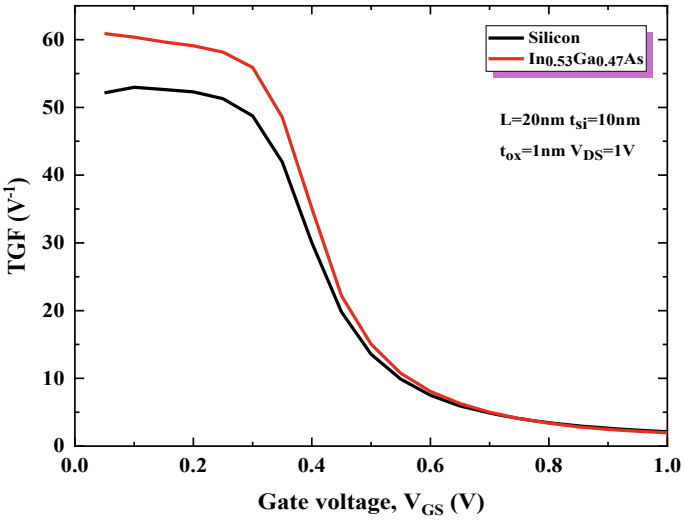

Fig. 7 Variation of TGF (g_m/I_D) of Si-GAA and $In_{0.53}Ga_{0.47}As$-GAA MOSFET versus V_{GS} at $V_{DS} = 1$ V

Table 2 Analog FOMs of Si-GAA and $In_{0.53}Ga_{0.47}As$-GAA MOSFET at $V_{DS} = 1.0$ at a constant threshold voltage

Parameters	Si-GAA	$In_{0.53}Ga_{0.47}As$-GAA
I_{ON} (A)	4.26×10^{-05}	6.80×10^{-05}
I_{OFF} (A)	2.0×10^{-12}	3.2×10^{-13}
I_{ON}/I_{OFF}	$2.13 \times 10^{+07}$	$2.1 \times 10^{+08}$
SS (mV/decade)	67.61	62.49
DIBL (mV/V)	18.47	6.06
g_m (S)	9.0×10^{-05}	1.38×10^{-04}
g_m/I_D	52.13	60.90

at $V_{DS} = 1.0$ at a constant threshold voltage. Table 2 shows that the $In_{0.53}Ga_{0.47}As$-GAA device is organized adequately for analog/RF performance compared to Si-GAA MOSFET. The ON-current ~ 59.62%, g_m ~ 53.33%, and TGF ~ 16.12% of $In_{0.53}Ga_{0.47}As$-GAA devices are higher than the Si-GAA device. However, the $In_{0.53}Ga_{0.47}As$-GAA MOSFET performance parameters such as OFF-current (I_{OFF}) with ~ 84%, subthreshold swing (SS) ~ 8.19%, and DIBL are decreased compared to Si-GAA MOSFET.

4 Conclusion

In this paper, the performance investigation of $In_{0.53}Ga_{0.47}As$-GAA MOSFET has been carried out and compared with the Si-GAA MOSFET for same parameters. Both devices are simulated using a 3D ATLAS TCAD device simulator from SILVACO. The $In_{0.53}Ga_{0.47}As$-GAA MOSFET has revealed much upgraded performance compared to Si-GAA MOSFET. The $In_{0.53}Ga_{0.47}As$-GAA MOSFET has presented superior SCEs immunity compared to Si-GAA. The higher value for ON-current (I_{ON}), g_m, and TGF of $In_{0.53}Ga_{0.47}As$-GAA device has been obtained as compared to the Si-GAA device. However, the $In_{0.53}Ga_{0.47}As$-GAA MOSFET performance factors such as OFF-current, subthreshold swing, and DIBL have been found to diminish compared to Si-GAA MOSFET. The $In_{0.53}Ga_{0.47}As$-GAA MOSFET can be considered to offer excellent analog performance compared to the Si-GAA device. Therefore, it is more superior for high-speed analog and switching applications.

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A Simple and Sturdy Hybrid Interference Canceller for a DS-CDMA System in Multipath Environment for Static and Mobile Users

Monica Khanore and Srija Unnikrishnan

1 Introduction

DS-CDMA uses code-division multiple access where a distinctive code identifies a user, the codes being orthogonal to avoid interference. The orthogonality of the codes ensures independent detection of each user. However, due to asynchronous transmission and different propagation delays because of variation in the distances of users from the receiver, the codes lose their orthogonality resulting in interference among the users. This interference is called multiple access interference (MAI). MAI makes it difficult to detect the users individually. This is a very common scenario in mobile communication system.

In addition to MAI, two other factors adding to interference in the received signal are multipath propagation and Doppler shift. Due to multipath propagation, duplicates of a signal reach the receiver with different relative delays. Thus, besides interfering with itself, the user signal interferes with other user signals. The mobility of users results in Doppler shift in the carrier frequency of user signals. The user signals may lose synchronization due to Doppler shift, and hence, the data recovered may not be accurate. Thus MAI, multipath propagation and Doppler shift result in degradation of the system performance. Consequently, error probability increases, so does the BER. As a result, the increase in BER reduces the capacity of the system; hence, it becomes imperative to incorporate some interference cancellation (IC) technique.

Serial interference canceller (SIC) and parallel interference canceller (PIC) are two important subtractive types of IC techniques. PIC has the advantage of being fast; however, it works well only in the presence of power control, that is, when the

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user powers are roughly equal. SIC is slow but can work well in varying user power environments. Besides, the BER performance of SIC is better than PIC. The benefits of both methods are integrated in Hybrid Interference Canceller (HIC), which is a mix of SIC and PIC.

In [1], the linear HIC detector is discussed using a matrix-algebraic approach. The detector is presented as a single shot linear matrix filter for single-stage and multistage interference cancellation. Simulation and analysis have been done for single-path propagation.

An HIC technique has been evaluated in the Rayleigh fading multipath environment in [2]. This canceller is found to be robust in the Rayleigh fading multipath environment even for users in motion. However, closed-loop power control is essential for obtaining acceptable BER performance.

BER performance of an HIC is investigated in [3], in AWGN as well as Rayleigh fading environment for single path and 3-path propagation. The Doppler frequency used is 100 Hz. The BER performance of the HIC is found to be at par with the performance of the SIC when the propagation delay is much shorter than the detection delay.

In [4, 5], a multistage SIC scheme is presented, which incorporates a non-decision directed (NDD) interference canceller followed by a decision directed (DD) canceller. Diversity combining is done using a RAKE receiver, which is slightly modified. The performance is evaluated for mixed modulation and multicode schemes. The receiver is found to be relatively less complex. Their results show that a multicode system with high data rates outperforms a system with lower rates and a system with high data rates, and mixed modulation. A minimum mean square error channel estimator is used which utilizes the correlations of the fading paths.

HIC scheme based on K–P–S configuration is presented in [6]. From the K users, P users are cancelled using PIC, and the remaining $S = K$–P users are cancelled by SIC. HIC is proposed for overloaded CDMA system in which the number of users is more than the processing gain in [7]. The users are divided in two groups and separate sets of orthogonal Gold codes are assigned to users in these groups. PIC cancels the interference within a group and the interference between the groups is cancelled by mSIC. HIC technique in which users are cancelled in groups in SIC, followed by PIC is proposed in [8]. This scheme provides notable reduction in the processing delay.

Most of the interference cancellers discussed above utilize RAKE receiver for diversity combining and for estimation of the transmitted data. However, there is a possibility of erroneous data estimates owing to interference caused by the cross-correlation between the spreading codes [9]. The interference canceller presented in this paper circumvents the need of a RAKE receiver; thus, occurrence of these errors is averted. This paper discusses the HIC detector scheme for multipath, Rayleigh fading environment. The performance of the detector for static as well as users in motion is analyzed. Furthermore, the convergence of the detector is tested.

The structure of remainder of the paper is as follows. Received signal model for multipath propagation is presented for static and moving users in Sect. 2. The interference canceller module and the HIC detector are explained in Sect. 3, and the

simulation results are discussed in Sect. 4. Finally, in Sect. 5, conclusion of the work reported in this paper is presented.

2 Receiver Signal Model

Mathematical model of the signal received at the input of the receiver of a multiuser, multipath CDMA communication system is described in this section. The model is presented for static as well as moving users assuming a Rayleigh fading channel. It is further assumed that after spreading, the signal is binary phase-shift keying (BPSK) modulated.

2.1 Received Signal Model for Static Users

The received signal, $\boldsymbol{y(t)}$ in continuous time t, including multipath signals of all static users is expressed as

$$y(t) = \sum_{n=1}^{N} \sum_{m=1}^{P} \{d_n(t - \tau_{nm}) w_n(t - \tau_{nm}) \cos \omega_0 t + \nu_{nm}\},$$

where N: number of active users,
P: number of multipaths,
d_n: data sequence of nth user,
w_n: spreading sequence of nth user of length L,
τ_{nm}: mth path delay of the nth user,
ω_0: carrier frequency, and
ν_{nm}: Rayleigh noise introduced by the channel to the nth user over the mth path [10].

2.2 Received Signal Model for Users in Motion

The received signal for moving users is expressed as:

$$y'(t) = \sum_{n=1}^{N} \sum_{m=1}^{P} \{d_n(t - \tau_{nm}) w_n(t - \tau_{nm}) \cos(\omega_0 \pm \omega_{dn}) t + \nu_{nm}\},$$

where ω_{dn} is the nth user Doppler shift, which takes values from 60 to 100 Hz for practical systems [10].

3 Interference Canceller Module

The structure of the interference canceller module is illustrated in Fig. 1. After coherent demodulation of the received signal, the demodulated signal is low pass filtered (not shown in the diagram). The filter output, $r(t)$, is a base-band signal consisting of desired user signals, mutual interference of N users, and channel noise.

The filter output $r(t)$ contains the interference from all active users and their multipath signals. As a part of the interference cancellation process, these $K = NP$ user signals are organized in the descending of their strength. Correlations of $r(t)$ with the spreading codes of the users are found using K matched filters (MF). These correlation coefficients $\{Z_{i,p}\}$, indicate the strength of each user's signal. For simulation, the correlation values for each of the K signals are found with the assumption that $\{\tau_{ip}\}$ of all signals are accurately estimated.

Once arranged from strongest to weakest, the K signals are split into N groups, with P signals in a group. S stages of HIC are then implemented. At every stage, PIC is performed within each group to obtain the estimates for P signals in the group. MAI incurred by a group is then evaluated using these estimates and subtracted (cancelled) from the input signal to the interference cancellation unit (ICU) of that group. The remaining signal then becomes an input signal to the ICU of the succeeding group. This process of parallel estimation and serial cancellation goes on until the interference due to the Nth group at the current stage is cancelled.

Remaining signal from the last group of a stage becomes an input signal to the first group of the next stage. At this stage, MAI evaluated for the group at the previous stage is reinserted. The estimates for the signals in the group are evaluated by performing PIC within the group. After the estimates of the signals in the group have been

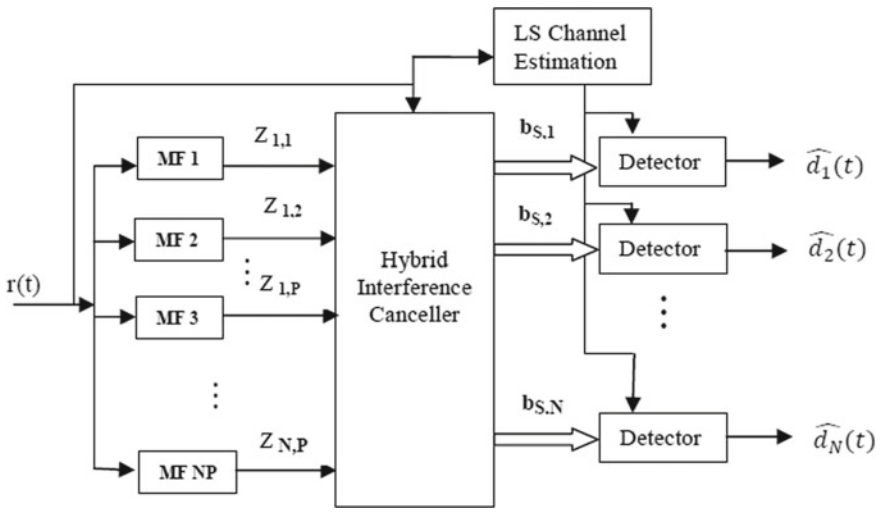

Fig. 1 Block diagram of interference canceller module

evaluated at the present stage, their estimates from the previous stage are added to these estimates. This improves the estimates of the signals in the group. Further, MAI due to this group is calculated using these estimates and subsequently cancelled from the residual input signal to the group. The same process of interference cancellation continues for the subsequent groups at that stage until the MAI due to the last group is cancelled. This procedure is repeated for subsequent stages [11].

Generalized mathematical expressions for the input signal to an ICU, the estimates for users in a group, and MAI due to that group are obtained as follows:

At stage 1:

$\boldsymbol{s}_{\mathrm{s,i}}$ of size $L \times 1$ is the input signal to the ICU of ith group at the sth stage, $\mathbf{r}$ is input signal vector of size $L \times 1$, vector $\boldsymbol{b}_{\mathrm{s,i}}$ of size $P \times 1$ contains the estimates of the signals of the ith group, $\boldsymbol{W}_{\mathrm{i}}$ is the code vector matrix of the ith group, of size $P \times L$, and $\Delta \boldsymbol{I}_{s,i}$ is the MAI incurred by ith group at sth stage.

$$\boldsymbol{s}_{1,n} = \boldsymbol{\varphi}_{n-1}\boldsymbol{r}, \tag{1a}$$

$$\boldsymbol{b}_{1,n} = \boldsymbol{W}_n^T \boldsymbol{\varphi}_{n-1}\boldsymbol{r}, \tag{1b}$$

and

$$\Delta \boldsymbol{I}_{1,n} = \boldsymbol{W}_n \boldsymbol{W}_n^T \boldsymbol{\varphi}_{n-1}\boldsymbol{r}, \text{ respectively,} \tag{1c}$$

where $\boldsymbol{\varphi}_n = \coprod_{j=n}^{1} \left(\boldsymbol{I} - \boldsymbol{W}_j \boldsymbol{W}_j^T\right)$ and $n = 1, 2, \ldots, N$, $\boldsymbol{\varphi}_0 = \boldsymbol{I}$, and $\boldsymbol{I}$ is an identity matrix, size $L \times L$.

At stage 2:

$$\boldsymbol{s}_{2,n} = (\boldsymbol{\varphi}_N + \boldsymbol{\psi}_n)\boldsymbol{\varphi}_{n-1}\boldsymbol{r}, \tag{2a}$$

$$\boldsymbol{b}_{2,n} = \boldsymbol{W}_n^T \left(\boldsymbol{I} + \boldsymbol{\varphi}_N + \boldsymbol{\psi}_n\right)\boldsymbol{\varphi}_{n-1}\boldsymbol{r}, \tag{2b}$$

$$\Delta \boldsymbol{I}_{2,n} = \boldsymbol{W}_n \boldsymbol{W}_n^T (\boldsymbol{\varphi}_N + \boldsymbol{\psi}_n)\boldsymbol{\varphi}_{n-1}\boldsymbol{r}, \tag{2c}$$

respectively, where,

$$\boldsymbol{\psi}_n = \sum_{j=1}^{n} \left(\boldsymbol{W}_j \boldsymbol{W}_j^T\right),$$

and

$$\boldsymbol{\psi}_0 = 0.$$

At stage 3:

$$\boldsymbol{s}_{3,n} = (\boldsymbol{\varphi}_N + \boldsymbol{\psi}_N + \boldsymbol{\psi}_n)\boldsymbol{\varphi}_{n-1}\boldsymbol{\varphi}_N\boldsymbol{r} + \boldsymbol{\Lambda}_n\boldsymbol{\varphi}_{n-1}\boldsymbol{r} + \boldsymbol{Z}_n\boldsymbol{\varphi}_{n-1}\boldsymbol{r}, \tag{3a}$$

$$\begin{aligned}\boldsymbol{b}_{3,n} = {} & \boldsymbol{W}_n^T(\boldsymbol{I} + \boldsymbol{\varphi}_N + \boldsymbol{\psi}_N + \boldsymbol{\psi}_n)\boldsymbol{\varphi}_{n-1}\boldsymbol{\varphi}_N\boldsymbol{r} + \boldsymbol{W}_n^T\boldsymbol{\Lambda}_n\boldsymbol{\varphi}_{n-1}\boldsymbol{r} \\ & + \boldsymbol{W}_n^T\boldsymbol{Z}_n\boldsymbol{\varphi}_{n-1}\boldsymbol{r} + \boldsymbol{W}_n^T(\boldsymbol{I} + \boldsymbol{\psi}_N)\boldsymbol{\varphi}_{n-1}\boldsymbol{r},\end{aligned} \tag{3b}$$

and

$$\begin{aligned}\Delta\boldsymbol{I}_{3,n} = {} & \boldsymbol{W}_n\boldsymbol{W}_n^T(\boldsymbol{\varphi}_N + \boldsymbol{\psi}_N + \boldsymbol{\psi}_n)\boldsymbol{\varphi}_{n-1}\boldsymbol{\varphi}_N\boldsymbol{r} \\ & + \boldsymbol{W}_n\boldsymbol{W}_n^T\boldsymbol{\Lambda}_n\boldsymbol{\varphi}_{n-1}\boldsymbol{r} + \boldsymbol{W}_n\boldsymbol{W}_n^T\boldsymbol{Z}_n\boldsymbol{\varphi}_{n-1}\boldsymbol{r},\end{aligned} \tag{3c}$$

where

$$\boldsymbol{\Lambda}_n = \sum_{j=1}^{n}\left(\boldsymbol{W}_j\boldsymbol{W}_j^T\right)^2,$$

and

$$\boldsymbol{Z}_n = \sum_{j=2}^{n}\left(\boldsymbol{W}_j\boldsymbol{W}_j^T\boldsymbol{\psi}_{j-1}\right).$$

These generalized equations can be further derived for S number of stages.

After S stages of interference cancellation, the multipaths of all users are grouped together and the estimates of these paths, $\{b_{S,i}\}$, are combined with the channel estimates of each path. The symbol detector uses this average to estimate the transmitted data symbol, $\left\{\widehat{di}(t)\right\}$. The channel estimates are found using Least Square method [12].

4 Simulation and Results

In this paper, we present the BER performance of the HIC detector explained in Sect. 3, in a Rayleigh fading channel considering an asynchronous system. The 3 independent paths delays of [0, 1, 2] chips are assumed. The processing gain, L, is 128 and the maximum number of users is 125. The simulation starts with obtaining the correlation values of all users, along all paths taken by the user signal, with their spreading codes. The correlation values indicate the strengths of the users. The $K = NP$ users are arranged in the decreasing order of their strength prior to staring the cancellation of interference. The simplicity of the LS channel estimation algorithm, and its quickness in calculating the estimation makes it best suited for the purpose.

Figure 2 shows the comparison of the BER performances of the proposed HIC detector for $L = \{64, 128\}$, and $N = \{50, 75, 100, 125\}$, respectively, for static users. It is conspicuous from the figure that increasing the processing gain improves the detector performance significantly. Also, there is a minute variation in the performance of the detector for $N = \{75, 100\}$. Furthermore, the target BER of 10^{-2} is obtained for both numbers of users for $E_b/N_0 \approx 10$ dB.

Figure 3 illustrates the performance of the detector for users in motion for $L = 128$ and $N = \{50, 75, 100, 125\}$. As expected, there is a slight degradation in the performance due to mobility of users. However, for $N = 125$ the detector seems to be less affected by the mobility of users. In the interference cancellers discussed in the literature survey, the target BER is achieved for maximum 30 users. The proposed

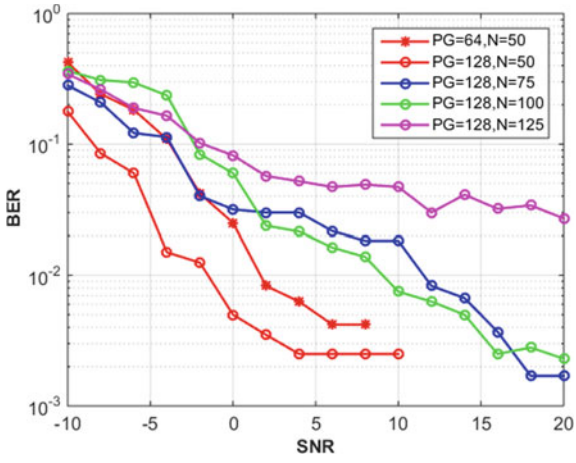

Fig. 2 BER performance of the HIC detector without Doppler shift

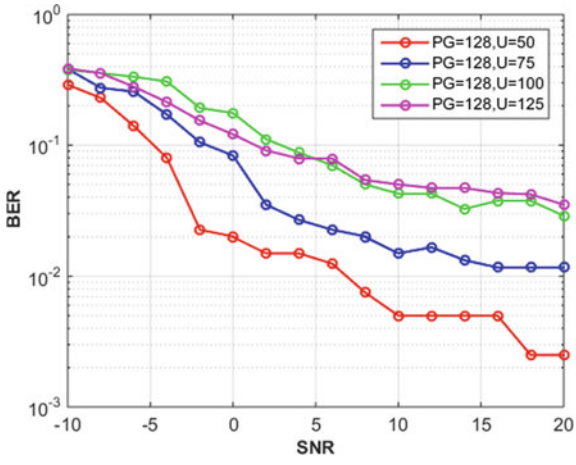

Fig. 3 BER performance of the HIC detector with Doppler shift

detector achieves the target BER for up to 100 users. Thus, it can handle much larger load efficiently.

In Fig. 4, the BER performance of the detector for varying number of users for $E_b/N_0 = 20$ dB, and $N = 128$ is shown. Marginal variation in BER is observed for increasing number of active users, this is the testament to the sturdiness of the detector.

The interference cancellation process is implemented for 8 stages of cancellation. For investigating the convergence behavior of the detector, the BER performance of the detector at every stage is plotted in Fig. 5. As it is apparent from the graph, the BER remains roughly constant with every stage of interference cancellation process. Thus, the convergence of the detector is assured. Also, irrespective of the amount

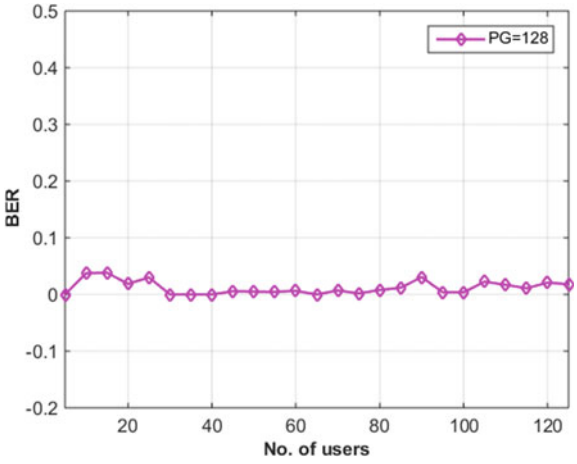

Fig. 4 BER performance depicting the sturdiness of the HIC detector

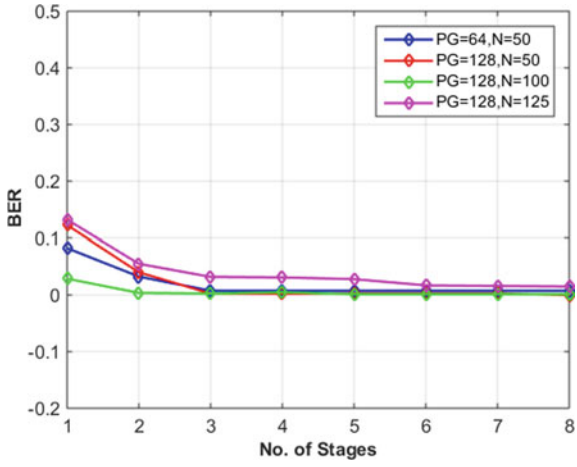

Fig. 5 BER performance of the HIC detector showing convergence

of load on the detector, the number of stages needed for convergence is roughly the same.

The RAKE receiver can make inaccurate data estimates because of the interference caused by the cross-correlation between the spreading codes. The advantage of the proposed detector is that it does not require a RAKE combiner, which averts such erroneous detection.

5 Conclusion

In this paper the bit error performance of the HIC detector in Rayleigh fading multipath environment for both static and moving users is evaluated. It is assumed that the signal of each active user takes three independent paths. The simulation was done for $L = \{64, 128\}$. Considerable improvement in the BER performance of the detector was observed for $L = 128$. Hence, $L = 128$ is a perfect choice for better BER performance. For $N = \{75, 100\}$, it was observed that the target BER was achieved for $E_b/N_0 \approx 10$ dB for static users. The detector was also checked for robustness. The increasing number of users hardly has any effect on the performance of the detector. The convergence test of the detector shows that the convergence of the detector is assured, and irrespective of the amount of load, roughly the same number of stages is needed for convergence. Small degradation is noted in the detector performance due to mobility of the users.

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Performance Evaluation of SPR Sensor on Using Graphene/TMDCs in Visible and Near Infrared Wavelength Regime

Vipin Verma, Sarika Pal, Narendra Pal, and Dharmendra Kumar

1 Introduction

Now days, surface plasmon resonance (SPR) sensor in optical sensor category has been widely preferred for biosensing and chemical sensing [1, 2]. SPR sensor has been used due to their efficient characteristics such as lable free, real time, reliable, low cost and sensitive detection capabilities [3]. Surface plasmon polaritons (SPPs) occur due to oscillation of electrons i.e., dense electron wave propagating between metal and dielectric medium, which was introduced by Wood [4]. SPR phenomenon is achieved when evanescent wave generated after attenuated total reflection (ATR) and surface plasmon wave (SPW) are coupled to each other [3]. Normally, the propagation constant of SPW is always greater than the propagation constant of incident optical wave. So, to achieve the resonance condition, incident wave is excited by using different coupling methods in order to match the momentum of photon of incident light wave with momentum of SPW [3, 5]. The prism coupling method is preferably used in Kretschmann configuration-based SPR sensors for optical excitation of resonance condition via angular interrogation method [5]. The reflection intensity detected by the photo detector indicates the dip in intensity at particular incident angle. SPR dip position changes with redistribution of electromagnetic field due to change in refractive index of sensing layer after adsorption of biomolecules on sensor surface [3]. The performance of SPR biosensor can be evaluated from SPR reflectance curve. Generally, a metal thin film is used to excite the resonance signal

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as it possesses large number of free electrons. Recently, nanostructured transparent conducting oxides are used in SPR sensor for SPPs generation in place of metals [6]. But, gold thin film is generally used as a plasmon active metal as it is free from oxidation and show high sensitivity and stability for analytic binding [3, 7]. The use of conventional gold metal thin films in optical SPR sensors over the prism shows weak attachment or binding ability of biomolecules. Thus, the sensitivity of conventional SPR sensor is limited [3, 7].

Over the past decades, several techniques have been developed to enhance the performance of SPR sensor such as employment of different SPR configurations, two dimensional (2D) materials, metamaterials, bimetallic plasmonic metals and hetrostructure of 2D materials [2, 7–13]. For the development of improved SPR sensors, the two dimensional (2D) materials possessing extraordinary optical, electrical and mechanical properties have shown their potential applications in sensor field [14, 15]. Graphene, a 2D material is a single carbon atom thick layer possessing carbon-based ring structures, high electrical mobility, high surface to volume ratio, stable atomic structure and zero band gap, which can enhance the performance of optical SPR sensor [14, 15]. Over the past few years, transition metal dichalcogenides (TMDCs) have shown their utility in electronic and optoelectronic area due to their unique optical and electrical properties [16–18]. A number of transition elements are included in TMDCs group, and it is represented as MX_2, where M symbolizes the transition metal (such as Mo, W, Ta and Nb), and X symbolizes the chalcogen element (such as Te, S and Se). To obtain TMDCs, the transition metal is packed between two layers of chalcogen element and bonded to each other via van der Waals forces [16]. The most intriguing property of TMDCs layers useful for sensing is their adsorption capabilities better to graphene and their rate of light adsorption which may be tuned by changing their layer numbers. Number of researchers have tried TMDCS along with other 2D materials to enhance the SPR sensor performance [7, 17, 18]. Ouyang et al. proposed the TMDCs-based SPR sensor to improve the sensitivity and performance of SPR sensor. Their group obtained sensitivity (155.68°/RIU) for monolayer of WS_2 TMDC film [19]. Pal et al. proposed an Au–Si–BP–T_MDC SPR biosensor in visible region to achieve sensitivity up to 163.1°/RIU for monolayer WS_2 [7]. However, investigation of sensitivity for TMDCs-based SPR sensor in other wavelength region is still illusive. So, in this work, we proposed an, Au-Graphene-TMDCs-based SPR sensor for analyte detection at 600, 725 and 1024 nm operating wavelengths.

2 SPR Sensor Modeling

2.1 N-layer Modeling

Transfer matrix method and Fresnel equations are used for obtaining the characteristic of N-layer SPR sensor [9]. This method does not consider any approximations

which makes it an efficient method to mathematically model a SPR sensor. The transverse magnetic (TM) light incident at SPR active metal layer at an angle θ_i, and the transmitted light is refracted at angle θ_N. The thicknesses of the k_{th} layer are denoted as d_k, dielectric constant (ε_k) and RI (n_k). On applying the boundary conditions, the tangential fields of E and H fields at first layer are related with the tangential field at last layer interface as follows; [10]

$$\begin{bmatrix} E_1 \\ H_1 \end{bmatrix} = M \begin{bmatrix} E_{N-1} \\ H_{N-1} \end{bmatrix} \tag{1}$$

where E and H are the tangential components of the electric fields and magnetic fields at the layer interface, respectively. M denotes the characteristics matrix of multilayer SPR sensor and given as:

$$M = \prod_{k=2}^{N-1} M_k = \begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix} \tag{2}$$

where

$$M_k = \begin{bmatrix} \cos\beta_k & -i\frac{\sin\theta_k}{q_k} \\ -iq_k \sin\beta_k & \cos\beta_k \end{bmatrix} \tag{3}$$

where

$$q_k = \frac{\left(\varepsilon_k - n_{BK7}^2 \sin^2\theta_1\right)^{1/2}}{\varepsilon_k} \tag{4}$$

And

$$\beta_k = \frac{2\pi n_k \cos\theta_k (Z_k - Z_{k-1})}{\lambda} = \frac{\pi d_k}{2}\left(\varepsilon_k - n_1^2 \sin^2\theta_1\right)^{1/2} \tag{5}$$

Reflection coefficients for TM light wave are:

$$r_p = \frac{(M_{11} + M_{12}q_N)q_1 - (M_{21} + M_{22}q_N)}{(M_{11} + M_{12}q_N)q_1 + (M_{21} + M_{22}q_N)} \tag{6}$$

And reflection intensity is

$$R_p = \left|r_p\right|^2 \tag{7}$$

The SPR curve is the variation of reflectance corresponding to incident angle of TM light wave. At specific incident angle, dip in reflectivity curve is obtained after

achieving resonance condition. The complete analytical analysis on the performance parameters of the sensor is carried out using MATLAB simulation software.

2.2 Performance Parameters of Sensor

The major performance factors of the SPR sensor are sensitivity and FWHM which helps to determine the other parameters like detection accuracy and the quality factor [7].

Sensitivity (S): sensitivity is most important parameter of SPR sensor that shows that how efficiently the sensor can detect the change in refractive index of sensing medium (Δn_s) with respect to change in SPR angle ($\Delta\theta_{SPR}$).

$$S = \frac{\Delta\theta_{SPR}}{\Delta n_s} \tag{8}$$

Full width half maximum (FWHM): The FWHM ($\Delta\theta_{0.5}$) is the angular width of the resonance curve corresponding to 50% reflectivity. It is defined as inverse of FWHM ($\Delta\theta_{0.5}$) of the reflection intensity curve. Its unit is Degree.

$$\text{FWHM} = \Delta\theta_{0.5} \tag{9}$$

Detection Accuracy: It is inversely proportional to angular width of SPR curve and its unit is Degree^{-1}.

$$\text{DA} = \frac{1}{\text{FWHM}} \tag{10}$$

2.3 Sensor Configuration

The proposed SPR sensor consists of four layers over the BK-7 prism, and the sensor configuration is shown in Fig. 1. Angular interrogation is used analyse sensor performance in both visible and infrared region by using excitation wavelengths 600, 785 and 1024 nm. BK-7 prism is used to couple incident p-polarized light form laser diode source to prism /metal interface in SPR sensor configuration [1, 7]. The selection of metallic film over the prism is essential in SPR sensor application. SPR active metal such as gold (Au), silver (Ag), aluminum (Al), copper (Cu), sodium (Na), etc., have lots of conduction band electrons which are able to resonate at incident light wave of particular wavelength [1, 20]. Gold (Au) is most practical and stable SPR active metal as compare to other metals because sodium is too reactive, aluminum,

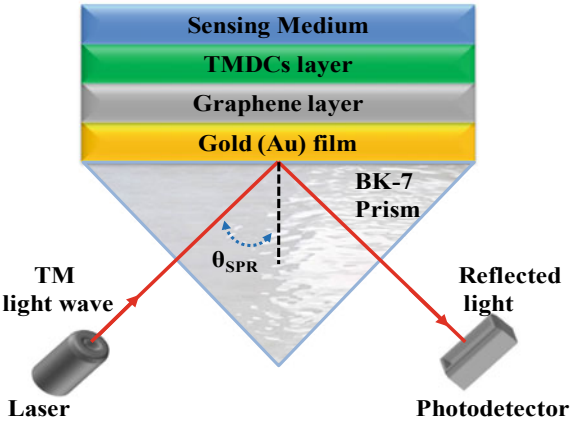

Fig. 1 Proposed SPR sensor structure

silver and copper have problems related to oxidation [20]. So, we have chosen gold metal film over the prism to induce the SPs. The wavelength dependent refractive index of BK-7 prism is calculated by following equation [21]:

$$n_{BK7} = \left(\frac{1.03961212\lambda^2}{\lambda^2 - 0.00600069867} + \frac{0.231792344\lambda^2}{\lambda^2 - 0.0200179144} + \frac{1.03961212\lambda^2}{\lambda^2 - 103.560653} \right) \tag{11}$$

As per Drude's model, we can calculate refractive index of gold (Au) from following Eq. [20]:

$$n_{\mathrm{m}} = \sqrt{\varepsilon_{\mathrm{m}}} = \left[1 - \frac{\lambda^2 \lambda_{\mathrm{c}}}{\lambda_{\mathrm{p}}^2 (\lambda_{\mathrm{c}} + i\lambda)} \right]^{1/2} \tag{12}$$

where λ_{p} and λ_{c} show the plasma wavelength and collision wavelength of the gold film, and their values are 1.6826×10^{-7} m and 8.9342×10^{-6} m, respectively. The third layer over the gold thin film is graphene, and thickness of monolayer graphene is 0.34 nm, and its wavelength dependent refractive index can be expressed as [22, 24]:

$$n_{\mathrm{G}} = 3 + i\frac{c}{3}\lambda \tag{13}$$

where c is approximately equal to 5.44 $\mu\mathrm{m}^{-1}$. The fourth layer of proposed SPR sensor is of TMDCs (MoS_2, $MoSe_2$, WS_2 and WSe_2), their thicknesses and refractive indices at different wavelengths are shown in Table 1 [23]. Fifth layer of SPR sensor is of sensing medium those refractive index is $1.33 + \Delta n_{\mathrm{s}}$, where Δn_{s} represents the change in refractive index of sensing medium after absorption of analyte.

Table 1 Optical refractive indices and thickness of TMDCs at different operating wavelengths [23]

TMDCs	Thickness (nm)	Wavelengths		
		600 nm	785 nm	1024 nm
MoS_2	0.65	$4.3934 + i1.2269$	$4.6348 + i0.1163$	$4.8690 + i0.2444$
$MoSe_2$	0.7	$4.7586 + i1.1504$	$4.2984 + i0.8225$	$3.8768 + i0.3561$
WS_2	0.8	$3.5202 + i0.6048$	$4.0123 + i0.0399$	$4.566 + i0.1058$
WSe_2	0.7	$4.5039 + i0.9340$	$4.3655 + i0.0367$	$5.0110 + i0.2562$

3 Results and Discussion

In this paper, three different wavelengths 600, 785 and 1024 nm are considered to study the performance of SPR sensor in visible and near infrared regions. So, firstly gold film thickness is optimized for proposed sensor configuration at three wavelengths. The thickness of gold layer is optimized in terms of minimum value of reflectance ($R_{\text{min.}}$), at which maximum incident energy is transferred to SPW. To optimize the gold film thickness at three wavelengths 600, 785 and 1024 nm, Fig. 2a–c are plotted, respectively. Figure 2a shows the optimized value of gold film as 49 nm at which value of $R_{\text{min.}}$ is minimum. The inset diagram within Fig. 2a shows the SPR curve with minimum reflectivity at different thicknesses of gold film i.e., 45, 50 and 55 nm. It is observed from inset diagram that the minimum value of $R_{\text{min.}}$ is obtained near to the 50 nm (exactly at 49 nm optimized thickness from Fig. 2a) of gold film. At 785 nm operating wavelength too, the optimized thickness of gold layer is again 49 nm as shown in Fig. 2b. In Fig. 2c, the optimized value of gold thickness decreases to 44 nm at 1024 nm of wavelength, and inset diagram within Fig. 2c shows the maximum energy transfer to SPs at 44-nm-thickness of the gold film.

The angular interrogation technique is applied here to analyse the performance of the SPR sensor at three different wavelengths through SPR curves. Figure 3a–d shows the SPR curves for the different 2D TMDC materials as a binding layer for analytes. The SPR angles vary with the variation of RI of sensing medium (1.33–1.335) after analyte binding and show different performance factors at different operating wavelengths i.e., 600, 785 and 1024 nm. In Fig. 3a–d, the solid line and dashed SPR curve indicate the RI of sensing medium before and after adsorption of analytes at different operating wavelengths i.e., 600, 785 and 1024 nm.

Figure 3a shows the SPR curve for MoS_2 layer in SPR sensor, in which SPR angle shifts obtained are 0.91°, 0.599° and 0.506° with change in sensing medium RI, $\Delta n_s = 0.005$, corresponding to operating wavelengths 600 nm, 785 nm and 1024 nm, respectively. The minimum reflectance ($R_{\text{min.}}$) values at $n_s = 1.335$ are 0.222, 0.008 and 0.003 a.u., corresponding to 600, 785 and 1024 nm operating wavelengths , respectively. The SPR curve for $MoSe_2$ layer in proposed SPR is shown in Fig. 3b, where SPR angles shifts obtained are 0.933°, 0.597° and 0.511°, and minimum reflectance ($R_{\text{min.}}$) obtained are 0.26, 0.048 and 0.004 a.u. corresponding to operating wavelengths 600 nm, 785 nm and 1024 nm, respectively. The SPR curve for WS_2

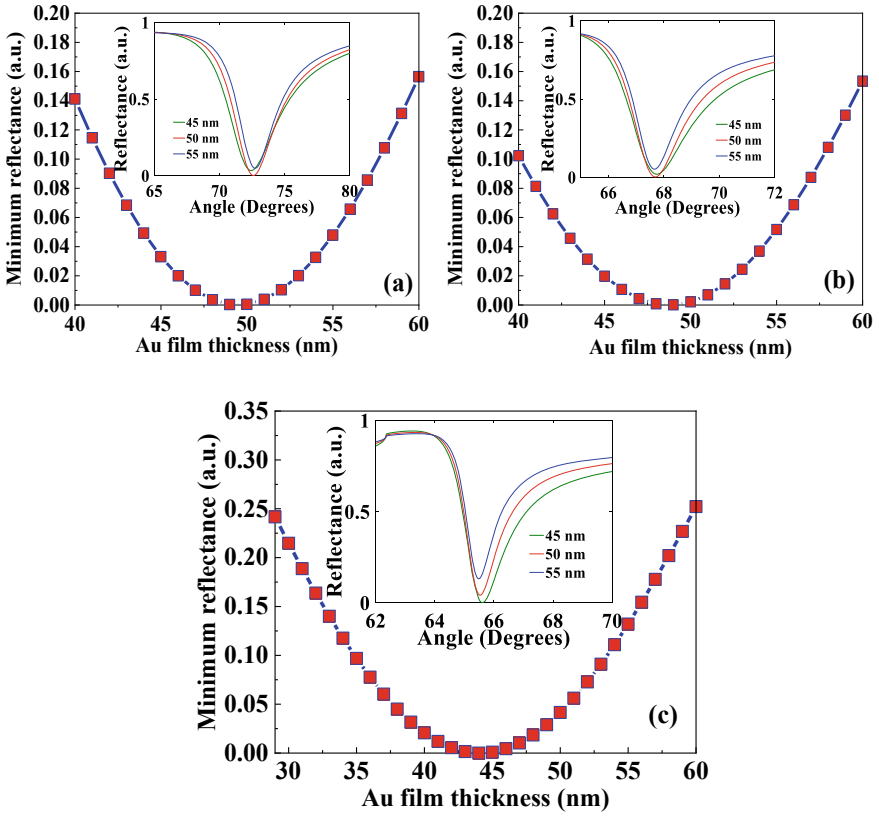

Fig. 2 Gold (Au) film thicknesses optimization curves of proposed SPR sensor at **a** 600 nm, **b** 785 nm and **c** 1024 nm of wavelengths of TM-polarized light

layer in proposed SPR is shown in Fig. 3c, where SPR angles shifts obtained are 0.932°, 0.6° and 0.509°, and minimum reflectance ($R_{\text{min.}}$) obtained are 0.124, 0.006 and 0.001 a.u. corresponding to operating wavelengths 600 nm, 785 nm and 1024 nm, respectively. Similarly, the SPR curve for WSe_2 layer in proposed SPR is shown in Fig. 3d, where SPR angles shifts obtained are 0.951°, 0.599° and 0.508°, and minimum reflectance ($R_{\text{min.}}$) obtained are 0.206, 0.005 and 0.003 a.u. corresponding to operating wavelengths 600 nm, 785 nm and 1024 nm, respectively. Then, SPR angle shift ($\Delta\theta_{\text{SPR}}$) and minimum reflectance ($R_{\text{min.}}$) are calculated from Fig. 3a–d to evaluate the sensor performance. Table 1 shows the fundamental performance factors of the SPR curves corresponding to different wavelengths (600, 785 and 1024 nm) for different TMDC materials i.e., MoS_2, $MoSe_2$, WS_2 and WSe_2 layer. The sensitivities of different TMDCs used in proposed SPR sensor at different operating wavelengths are also calculated by Eq. (8). It is clearly observed from Fig. 3a–d and Table 2 that narrower angular width of SPR curves i.e., better values of detection accuracy are obtained at higher wavelengths [20]. But, the higher sensitivities are obtained at

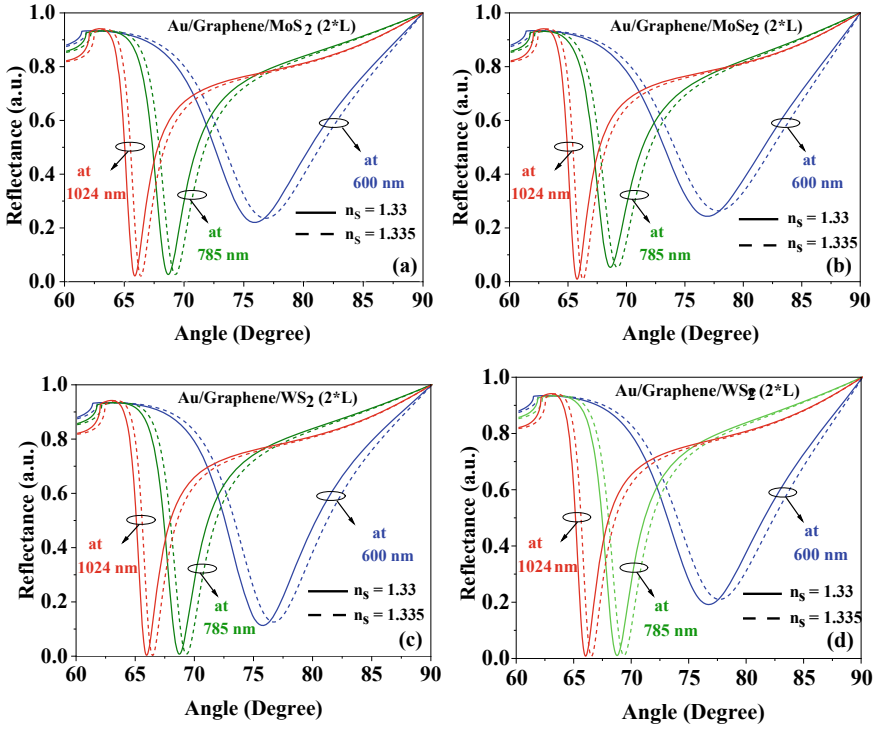

Fig. 3 SPR curves of proposed sensor on using TMDCs **a** MoS_2, **b** $MoSe_2$, **c** WS_2 and **d** WSe_2 with 1.33 (solid line) and 1.335 (dash line) RI of sensing medium at 600, 785 and 1024 nm wavelength

smaller wavelength i.e., 600 nm [20]. Thus, a tradeoff is observed between sensitivity, and detection accuracy is observed at different wavelength. Table 2 clearly suggests that the highest sensitivity (190.2°/RIU) is obtained for 2 layers of WSe_2 in proposed SPR at 600 nm operating wavelength, which is well justified with their order of light absorption capability [7]. Similarly, better detection accuracy is observed at higher wavelengths as per conventional trend observed in literature too. However, the best value of detection accuracy (0.347/°) is obtained for $MoSe_2$ layer in proposed SPR sensor at 1024 nm operating wavelength.

In Fig. 4a–d, we have plotted the SPR angle shifts ($\Delta\theta_{SPR}$) in terms of small refractive index changes (Δn_s) from 0.00025 to 0.0055 RIU for different 2D TMDC layers used in proposed SPR at operating wavelengths 600, 785 and 1024 nm. Figure 4a shows the comparative analysis of conventional SPR and proposed SPR on using 1, 2, 3 and 5 layer of WS_2. At operating wavelength 600 nm, the $\Delta\theta_{SPR}$ vary from 0.366° to 0.823°, 0.041° to 0.931°, 0.045° to 1.025°, 0.049° to 1.114° and 0.026° to 0.492° at variation n_s from 0.00025 to 0.0055 RIU for conventional SPR, mono layer, 2, 3 and 5 layer of WS_2-based SPR sensor, respectively. Figure 4b shows the $\Delta\theta_{SPR}$ vary from 0.366° to 0.823°, 0.042° to 0.954°, 0.045° to 1.027°, 0.038° to 0.821° and 0.008° to 0.140° at variation of n_s from 0.00025 to 0.0055 RIU for conventional SPR,

Table 2 Performance factors of proposed SPR sensor on using TMDCs at different operating wavelengths with $\Delta n_s = 0.005$

TMDCs	$\lambda = 600$ nm				$\lambda = 785$ nm				$\lambda = 1024$ nm			
	FWHM	R_{min}	S	DA	FWHM	R_{min}	S	DA	FWHM	R_{min}	S	DA
MoS_2	8.25	0.222	182	0.121	3.96	0.008	119.8	0.253	2.96	0.003	101.2	0.338
$MoSe_2$	8.47	0.26	186.6	0.118	4.39	0.048	119.4	0.228	2.88	0.004	102.2	0.347
WS_2	7.86	0.124	186.4	0.127	3.88	0.006	120	0.258	2.98	0.001	101.8	0.336
WSe_2	8.48	0.206	190.2	0.118	3.87	0.005	119.8	0.258	3.04	0.003	101.6	0.329

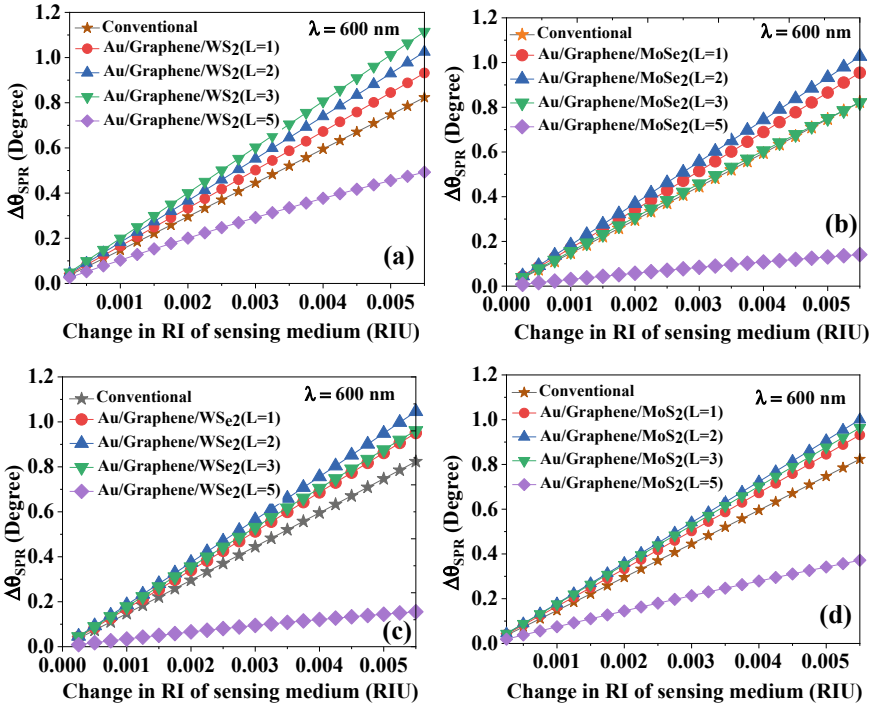

Fig. 4 **a–d** The optimization of the TMDCs layers in terms of the change in resonance angle shift to the RI change of sensing medium at 600 nm

mono layer, 2, 3 and 5 layer of $MoSe_2$-based SPR sensor, respectively, at 600 nm wavelength. Figure 4c shows the change in resonance angle is vary from 0.036° to 0.785°, 0.042° to 0.906°, 0.046° to 0.997°, 0.044° to 0.919° and 0.009° to 0.150° at variation of n_s from 0.00025 to 0.0055 RIU for conventional SPR, mono layer, 2, 3 and 5 layer of WSe_2-based SPR sensor, respectively, at 600 nm wavelength. Figure 4d shows the $\Delta\theta_{SPR}$ vary from 0.023° to 0.523°, 0.024° to 0.532°, 0.024° to 0.558°, 0.024° to 0.552° and 0.026° to 0.577° at variation of n_s from 0.00025 to 0.0055 RIU for conventional, mono layer, 2, 3 and 5 layer of MoS_2-based SPR sensor, respectively, at 600 nm wavelength.

Among all TMDC layers used in proposed sensor configuration at three different operating wavelengths, the highest sensitivity is ensured for WSe_2 layer at 600 nm operating wavelength. The sensitivity of proposed SPR sensor is compared with other angle interrogated SPR sensor in literature and shown in Table 3. The sensitivity of proposed SPR using 2 layers of WSe_2 is highest (190.2°/RIU) among all other reported sensitivities. The WSe_2 TMDC layer is the promising for sensitivity enhancement of SPR sensor due to direct band gap, higher light absorption rate and minimum electron energy loss [7]. The stacking of 2D TMDC layers, results in more

Table 3 Comparison of proposed SPR with other prism-based SPR sensors in visible range

Year	References	Configuration	λ (nm)	Sensitivity (°/RIU)
2014	Verma et al. [24]	Prism/Au/Graphene/Affinity Layer	633	33.98
2015	Maurya et al. [25]	Prism/Au/Si/MoS_2/Graphene/BRE	632.8	50.33
2018	Rahman et al. [26]	Prism/Au/WS_2-Graphene	633	95.71
2016	Mishra et al. [27]	Prism/Au/Silicon	632	106.29
2016	Ouyang et al. [28]	Prism/Au/Si/WS_2	600	155.68
2017	Pal et al. [29]	Prism/Au/Si/BP/Binding Layer	633	180
2016	Lin et al. [30]	Prism/Au/MoS_2/Au/Graphene	633	182
–	Proposed work	Prism/Au/Graphene/WSe_2	600	190.2

absorption of TM light wave but angular width also increases due to its larger imaginary part of dielectric constant. Therefore, large number of TMDC layers are not optimum as it increases FWHM and resulting in loss of detection accuracy. Here, 2 layers of WSe_2 are optimized at 600 nm operating wavelength, as it results in highest sensitivity as compared to other TMDCs layers when used at 785 and 1024 nm operating wavelengths.

4 Conclusion

In this paper, we have numerically investigated SPR sensors based on 2D TMDCs (MoS_2, $MoSe_2$, WS_2 and WSe_2) layer and graphene layer. To analyse the effect of wavelength on the sensing performance of SPR, we have investigated sensor performance at 3 different wavelengths, 600, 785 and 1024 nm. The thickness of gold film has been optimized at 49 nm for 600 nm and 785 nm of operating wavelength and at 44 nm for 1024 nm of wavelength of TM-polarized light. Among all TMDCs, use of WSe_2 established high sensitivity of 190.2°/RIU with minimum refractivity of 0.206 a.u. at 600 nm operating wavelength. SPR angle shifts are also analyzed for suitable range of refractive index of sensing layer on using different TMDCs at 600 nm wavelength.

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Integration of Mobile and Web Application with Accident Detection System

Meet Panchani, Kashyap Gohil, Devansh Saksena, Yash Panwar, Naja Makwana, and Rutu Parekh

1 Introduction

People use vehicles in their everyday lives. It makes a lot of things easier, but it also comes with its risks. Every day, thousands of vehicles are involved in accidents. According to WHO's Global status report on road safety 2018, every year the lives of approximately 1.35 million people are cut short as a result of a road traffic crash. Road traffic injuries cause considerable economic losses for the families of those involved. Road traffic crashes cost most countries 3% of their gross domestic product. A total of 93% of the world's fatalities on the roads occur in low- and middle-income countries, even though these countries have approximately 60% of the world's vehicles [1]. India, one of the most populous countries in the world, falls into the mentioned income country tier. A robust accident detection system and notification system (ADNS) can help to recover the losses caused by road accidents.

A wide range of vehicular encounters can turn out to be harmful accidents. In the paper by Khalil et al. [2], a brief review of the automatic road accident detection technique is presented. An automatic road accident detection technique based on low-cost ultrasonic sensors is proposed. In a system proposed in the paper [3], the accident detection system (ADS) uses GPS location tracking to detect the accident. GPS signal strength in the interior parts of the country where the network is an issue would make it difficult to detect the location. In [4], a novel vision-based road accident detection algorithm on highways and expressways is proposed. The algorithm consists of three main steps: motion detection, feature extraction and feature analysis, and accident recognition. A high computational load would require a high bandwidth internet connection for cloud computation or a heavier hardware system for the vehicle. Abnormality of the heart rate during stressful situations like accidents can be used for ADS [5]. This approach is not practical as the device to measure the heartbeat

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needs to be attached to the driver's body before every drive. The hassle of going through all that might lead the driver to not using the system at all. An approach described in the Bhatti et al. [6] resembles the ADNS, but it uses different parameters to check whether the accident has happened or not. The algorithm used in the system proposed here is more scalable. More sensors can be added to make the algorithm data-rich and more robust. This would help to make the predictions more accurate, and it would be precise in the details regarding the accident as well.

An hour after an accident is called "Golden Hour." If emergency medical service (EMS) is provided within this time, many lives can be saved. To provide EMS during this time, a real-time notification system paired with ADS can be of crucial importance. In the paper by Bonyár et al. [7], black box solutions for the notification system are discussed. Paper proposes the use of gadgets like e-call modules, smart tracker, etc. In [8], the notification system is suggested for the EMS provider to know about the accident. Incorporating GSM modules can be utilized to send SMS to the user's emergency contact [9, 10]. The use of mobile phones for accident detection is an idea that can be improved upon, i.e., using mobile phones to collect the data of the passengers [11].

A moderate hardware paired with the trivial notification system has been reported in [12]. The basic functionalities with a robust algorithm at its core are provided in the ADS. The notification system consists of a GSM module that sends an SMS whenever the accident has happened. The system proposed in this paper extends and improves upon the ideas of the notification system presented. The ADS proposed here consists of more than one sensor like an accelerometer and vibration sensor for better accuracy in the prediction. Adding more parameters in the already robust algorithm helps to achieve high accuracy. The notification system proposed in this paper uses a GSM module to send a message consisting of the details of the accident to the emergency contact number. A call is also made that communicates a pre-recorded message upon receiving the call. A mobile application and a web application are developed to pair with the ADS. The data collected from the mobile application are transmitted to the firebase cloud server. These data are then received and displayed on the web application. The mobile application is used to collect the data of the passengers and the driver, whereas the web application is developed to display the data collected from the accident site and the data gathered from the mobile application—all combined so that it can be seen together to establish a better understanding of the data and strategy for the EMS.

2 Overview of the Accident Detection and Notification System

The core of the ADNS is its algorithm. The algorithm is loaded inside the microcontroller. The hardware system is calibrated with the required data (i.e., the chassis number, time zone, etc.) and installed into the vehicle. The notification system

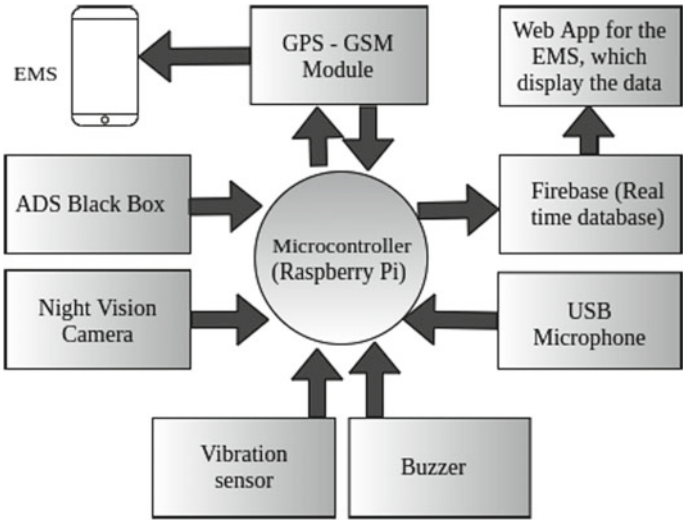


Fig. 1 Accident detection circuit diagram with all other modules

consists of a GSM–GPRS module and a web application. GSM module is used to send a message to the emergency contact that is provided using the mobile application. The GPRS module provides the geolocation of the accident site [13]. The mobile application also provides data about the passengers of the vehicle. This information can be crucial to recognize the victims of the accident. The web application is backed with the real-time firebase cloud server. Data gathered from the accident site, and the mobile application is sent to the firebase cloud server. Using the latitude and longitude from the retrieved data, the web application shows a pointer on the map on the site of the accident (Fig. 1).

When an accident happens, sensors used in the ADS feed in the data to the microcontroller. The microcontroller processes the data using an accident detection and severity prediction algorithm. The camera module and microphone, fit in front of the car, start recording audio and video. GPS module fetches the coordinates of the vehicle. All of these data are then sent to the firebase cloud server. On clicking the location pointer on the map in the web application, a pop-up screen appears where you can see the data about the accident sent by microcontroller from the ADS kit and the data added using the mobile application by the user. To identify every vehicle uniquely in the case of the accident, the chassis number of the vehicle is used as a unique key. All the data associated with the vehicle (driver, passenger details, their insurance number, accident details, etc.) are attached to the chassis number of that vehicle (Fig. 2).

Microcontroller and different modules were used to implement the ADS [14]. The microcontroller used in the circuit is Raspberry Pi as. The microcontroller runs the script to send the data to the firebase cloud server. In Fig. 2, the in–out flow of the microcontroller is shown. The controller is placed under the driver's seat of

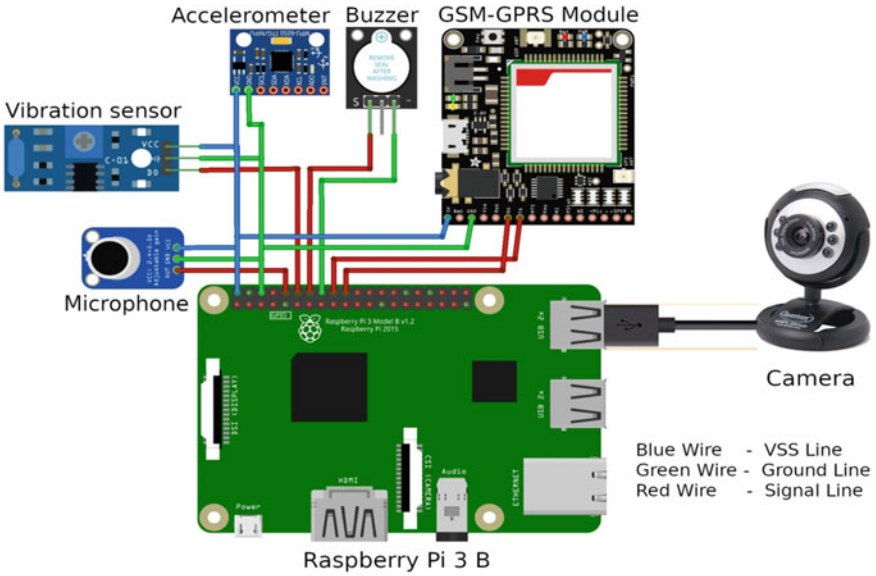


Fig. 2 Block diagram of the accident detection and notification system

the vehicle enclosed in a hard case made of honeycomb maze aluminum at the inner surface and glass fiber on the outer surface to prevent or minimize the damage during an accident. The system remains safe for most of the accidents unless the accident is too severe for the car to survive.

The system is attached to a 12 V li-ion battery which is sufficient to provide the 5 V power supply needed to operate the system. The battery gets charged from the main vehicle battery constantly enabling the system to work even after the accident. Li-ion battery has enough power to keep the system running even if the Li-ion battery is disconnected from the car battery. Once the microcontroller is attached to the power line of the vehicle, ADS starts. The microcontroller provides the central servicing platform for all the modules and the algorithm. It also provides a connection between the ADS and the firebase cloud server.

The accelerometer, GSM–GPRS module, vibration sensor module, the camera modules are used in cooperation with the microcontroller to collect the necessary data and predict the severity of the damage caused by the accident. Accelerometer (MPU 6050 Board GY 521) and vibration sensor modules are the two sensory devices used in the circuit [15]. Connected to the microcontroller, the accelerometer measures acceleration with a minimum full-scale range of $\pm$ 3 g. It can measure the static acceleration of gravity in tilt-sensing applications [3]. Using the difference in the acceleration, the severity of the accident is predicted [12]. Using the roll angle of the GY-521 module, the side of impact is decided [2]. The vibration sensor module provides us with the secondary confirmation of the accident detection. If the feedback from the vibration sensor module is above the accident potential threshold, the

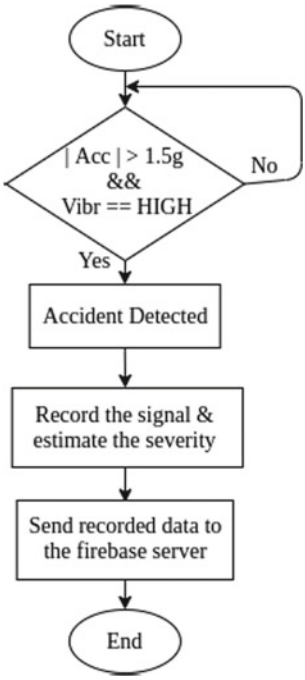


Fig. 3 Flow chart of the accident detection system

microcontroller starts gathering data from other sensors and modules. Detailed use of the accelerometer and the vibration sensor is provided in the algorithm section (Fig. 3).

The GSM–GPRS Module (SIM 808 GSM–GPRS Module) helps to get the geolocation of the car and communicate. The module is paired with the microcontroller. GPRS module provides the geolocation of the car. Put in the vehicle with enough peripheral openings, a GPRS module gives the coordinates of the accident site. It gives the latitude and longitude that are sent to the firebase cloud server. GSM module is used for communication purposes. When the accident happens, all the data are gathered in the microcontroller and via the GSM module, SMS is sent to the emergency number that has been set using mobile applications. GSM module also provides the internet service needed for the connection with the online firebase cloud server. The microcontroller connects to the hotspot provided by the GSM module via Wi-Fi. Using the connection, the microcontroller sends the data to the online firebase cloud server. In the case of the weak internet connectivity, all the data gathered from different modules and sensors will be stored inside the memory card attached to the microcontroller. As soon as a connection is established, all of the saved data will be sent to the firebase cloud server.

The active buzzer module (KY-012) is used to notify the accident as a loud noise. Buzzer operates at 5 V. The power used by the buzzer module is 150 mW. It generates a sound of approximately 2.5 kHz when the accident is detected. The main purpose of the buzzer is to alert the upcoming vehicles about the accident. The buzzer module

can be replaced with a more powerful module if the need be. The microcontroller would decide when to fire the buzzer. It is used to warn other people and cars coming in the direction of the accident site.

The camera module is placed in front of the car in a protective cover. Other modules are placed in the appropriate places. Unless the car encounters an accident, in which the car receives severe damage, modules would not be disconnected, and if such a case happens, the related field in the data will be empty so it can be recognized and fixed. In the scenario, where a module or sensor is unable to provide the feedback (module/sensor stops working, are broken, etc.), the data field for that particular module/sensor will be empty. That way we can check the sensor/module for which we get the empty field. A validation check for the data received from the sensors and modules helps to check whether the module or sensor is working properly or not. If the value of the data goes out of the bound set for the particular sensor/module, the module should be checked. Wild fluctuations in the data received on a consistent base would also mean malfunctioning of the sensor/module. Timely maintenance of the system is also required to ensure that there is no discrepancy in the data gathered from the sensor/module. The camera module along with the microphone is used to capture the video for a short amount of time after the accident. Both modules are connected to the microcontroller, and the recordings are sent to the firebase cloud server.

3 The Algorithm

The algorithm used in the microcontroller helps to determine the accident and also predicts the severity of the damage. Using all the feedback gathered from the sensors and accelerometer, it predicts the severity of the accident. The algorithm script also connects the ADS hardware with the online firebase cloud server.

In [12], if deceleration of a vehicle exceeds 5 g (where $g = 9.8$ m per s^2), then it has to be considered as an accident. This threshold was set based on the fact that the maximum braking deceleration of $F1$ cars does not exceed 5 g. Therefore, any deceleration above 5 g is significant in an accident, but it is also mentioned in the paper that maximum braking deceleration for normal cars does not exceed 1 g because the maximum acceleration of the fastest car in the world is 1.55 g (approx. 1.5 g). Therefore, it can be concluded that any deceleration between 1.5 and 5 g indicates the possibility of an accident. For most of the cars, airbags get deployed if deceleration is in the range of 5–13 g or change in velocity of the car during a crash is in the range of 12.8 km per h. The following table gives us an idea about the severity of an accident. Here, P is the maximum deceleration magnitude and Delta-V changes in velocity (Table 1).

The acceleration or deceleration can be directly measured by using an accelerometer. Velocity is an integration of the acceleration signals. An increase or decrease in the velocity of the vehicle can be used to know the side of the impact of the accident. If the velocity of the vehicle has increased (vehicle has accelerated), the side

Table 1 Accident severity criteria

Condition	Severity
(1.5 g < P < 5 g) and (Delta V < 12.8 km/h)	Moderate
(5 g < P < 13 g) or (12.8 km/h < Delta V < 22.5 km/h)	High
(P > 13 g) or (Delta V > 22.5 km/h)	Extreme

of impact is from the backside. If the velocity of the vehicle has decreased (vehicle has decelerated), the side of impact is from the front side. Using the GY-521 module (accelerometer with gyroscope), the roll angle of the vehicle is found. If the roll angle is less than 90 − threshold, the side of impact is from the left side. If the roll angle is greater than 90 + threshold, the side of impact is from the right side [11]. The vibration sensor gives a LOW or HIGH output based on the threshold set for the vibration sensitivity. To set up the threshold for the vibration, changes can be made to the potentiometer readings. Using different variations, the threshold can be determined [12]. Using these two sensor's feedbacks, the algorithm predicts if the accident has happened or not. If all the necessary conditions are satisfied, then it will be declared as an accident.

After the incident is declared as an accident, the camera and microphone placed at the front of the vehicle are activated to take a short video footage of the surrounding and possibly detecting other damages (i.e., pedestrian impacted by the accident, other vehicles involved in the accident, etc.). The algorithm has a preset time after which video and audio recordings will end. After all the data are collected, it is sent to the remote firebase cloud server for which the destination link is calibrated in the algorithm.

4 Result and Discussion

After the accident occurs, all the data are collected from the respective modules. All these data are then sent to the emergency contact number using the GSM module. An SMS is also sent to the emergency contact number, so in the absence of the internet, help can still reach the victim. The message structure and details can be seen in Fig. 4.

The total energy consumption of the system is around 5.4 W when all the modules are active. Microcontroller, GY-521 (accelerometer with gyroscope), and vibration sensor are the only modules that stay active from starting the vehicle to turning it off. Other modules are activated only after the accident is detected and stay active for a short amount of time. Hence, using a commercial battery of 15,600 mAh, 12 V, the system can sustain for 52 h (if not connected to the car battery). Lower power consumption can be achieved by using Nitrogen8n mini instead of Raspberry Pi. Other modules such as GPS-GSM modules, camera modules can be changed to even lower power consumption.

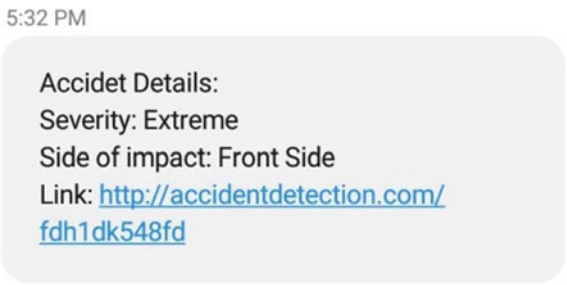


Fig. 4 Message sent from the accident detection system

4.1 The Mobile Application

A mobile application is created to collect information about the driver, passengers, and vehicle in which the ADS hardware is implemented. The user has to enter the vehicle details like chassis number and insurance number of vehicles. This application collects details from the driver like name, mobile number, address, blood group, insurance number, number of passengers and also collects details of passengers like name, mobile number, address, blood group, and insurance number of passengers. Users can also remove and edit the details that were previously added and can also see the current details added for a particular vehicle. Figure 5 shows the process of how to enter all the required data in the mobile application.

This application has a login screen that requires authentication from the user. After logging in, the user can see the main screen as described in Fig. 5a. From the main screen, user can use one of the three features provided in the application: enter details of the vehicle as shown in Fig. 5b, enter details of the driver as shown in Fig. 5c, enter details of passengers as shown in Fig. 5d. After entering the details, if the user clicks on the submit button, all the details will be stored on a firebase database on a unique hardware id. The other feature is for view and removal of details as shown in Fig. 5e. This application is created using MIT App Inventor. Firebase database is used for storage purposes. From the Firebase database, web application can fetch and display the data on the screen when the user of the web application clicks on a particular pointer at the location of the accident.

4.2 The Web Application

The web application is used to display all the data gathered from the ADS. This application also provides authentication to secure your data. It shows all the data of the car accident within a year. The web application is made using tools like Express.js, HTML5, CSS3. This application uses the firebase for storage purposes. Web application requires the user to authenticate themselves. Once logged in, a screen with the map can be seen with location pointers. This location pointers show

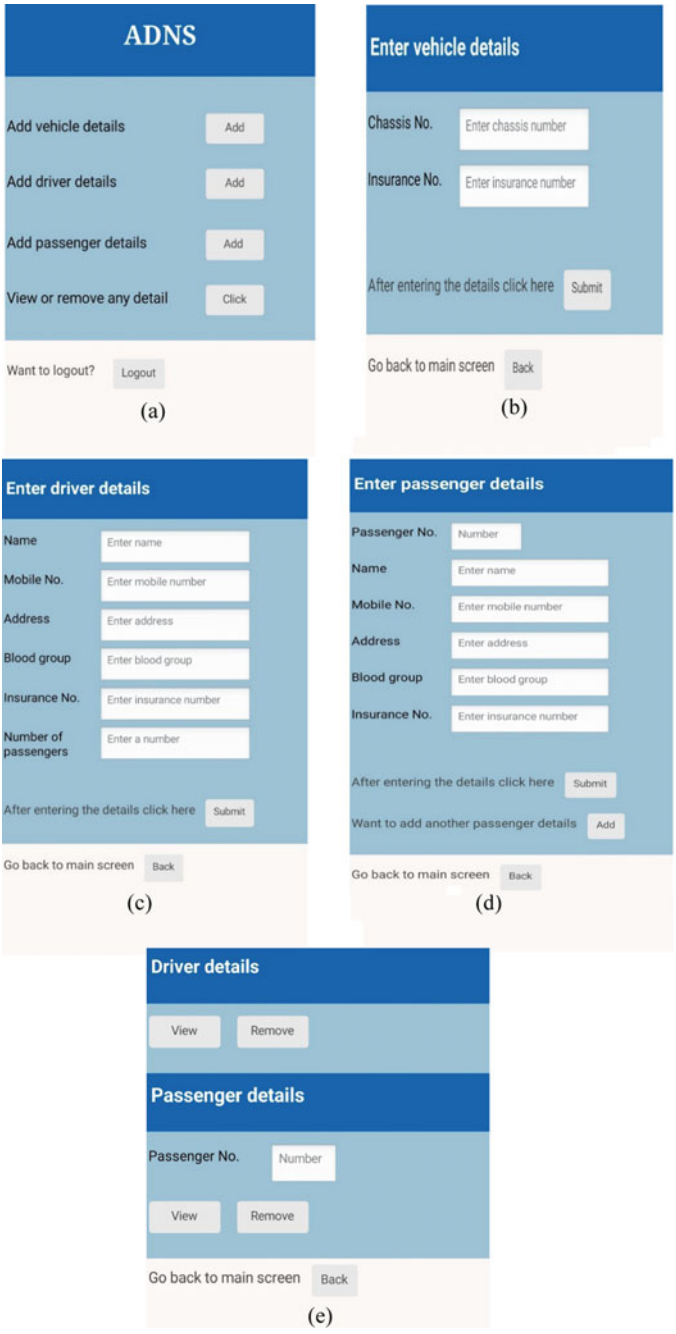


Fig. 5 Android application for ADS **a** main screen, **b** vehicle details, **c** driver details, **d** passenger details, **e** view or remove any details

the places of the accidents. As you click on the location pointer, a window emerges which contains all the details about the accident that has been transmitted from the ADS and the details of the car that has been entered from the mobile application.

The main part of the web application is the real-time database and storage done in the firebase. Firebase provides data, videos. When the accident happens, the data are collected and sent to the firebase server. The update is registered in the database. New coordinates that have been added in the database are instantly pinpointed on the web application using the real-time database. Firebase server also stores the video and audio data gathered from the accident spot which can be seen after clicking on the pinpoint.

In Fig. 6, there are sample images of the web application. Figure 6a shows the map with the location pointer. Location pointer is the coordinates of the accident site of the car. Clicking on the location pointer, details of the driver, and the passengers alongside the details of the car are shown in Fig. 6b.

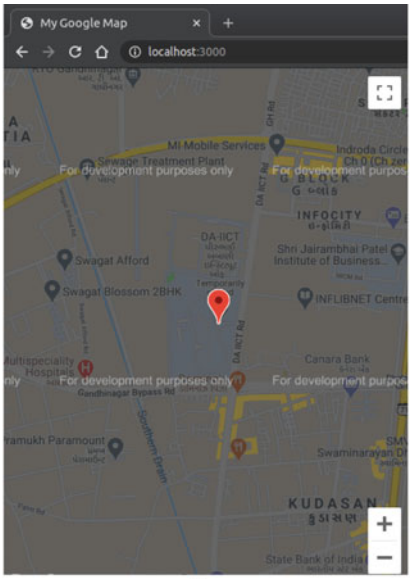
With mobile application and web application as a notification system, communication problem during the accident in a remote area is solved. The details provided from the mobile application (i.e., blood group, insurance number, etc.) can be helpful if the person affected is seriously injured and needs to be hospitalized. The data received from the vehicle can be used by the insurance companies as a way to monitor the driving patterns of their client. This could help the companies as well as the person. A person with the bad driving patterns and habits can be warned not to be precarious during the driving.

5 Conclusion

Successful implementation of the hardware system integrated with web application and mobile application for the real-time accident detection and notification system has been achieved. The accident detection system and notification system have been tested rigorously to make the system fault safe. During the simulation of the accident, within the few milliseconds of detecting the accident, a message is sent to the mobile phone. All the details collected from the accident site are transmitted to the firebase cloud server. Data from the android application and data from the accident site are then integrated into the server in real-time. These data can be accessed from the web application instantaneously. Using this data and location coordinates, EMS providers can easily track the accident site and can provide the necessary assistance to the affected ones. Hence, it can be said that working on a robust algorithm, the ADNS can help to save many lives. The ADNS provides real-time assistance for the accident victims and also gives the user the hope of being rescued in the hard times in an accident.

Future Scope

The ADNS is working on a very robust algorithm, but more sensors can be added for more precision parameters to detect the accident. The video analysis with the high



(a)

(b)

Fig. 6 Web application for ADNS **a** Site of the accident, **b** overview for the details shown on the web application

bandwidth internet network can be used to guess the speed of the car and predict the accident [4].

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Design and Analysis of Multiplexer Based D-Flip Flop Using QCA Implementation

Allam Naveen, C. V. Priyanka, and R. K. Kavitha

1 Introduction

With the rise in demand for faster operation and low power consumption for computing devices, we depend on reducing the transistor size and increasing the density of transistors per unit area. It is clear from the latest survey of ITRS-2015 [1] that the transistor could encounter the problem of the saturation point of scaling down the feature size by 2021. To meet future demands, quantum-dot cellular automata technology can be used as a better alternative to this CMOS technology for high-speed applications at the nano-scale with less power consumption [2, 3]. With the help of QCA technology, we can achieve significant improvements in the performance of clock frequency, density, scalability, and energy consumption when compared to corresponding implementations in CMOS VLSI technology. These advantages make the QCA technology favorable for digital applications where we require real-time data processes and less power consumption [2–4].

A large number of researches have been done on QCA and its circuit implementation on digital electronics in the past decade [2]. In high-speed synchronous systems, flip flops and latches require to operate at high speed. For achieving these high speeds, we use advanced pipelined architectures that require low pipeline overhead. This overhead is associated with the latency due to the flip flops. We can increase the speed of these systems by decreasing the latency of the flip flops. By improving these basic blocks, there will be a larger improvement in the working performance of complex circuits. A significant deal of work had been done in the past by researchers in designing flip flops with less power and latency [5, 6]. In this paper, a novel design of rising edge and falling edge-sensitive D-flip flops using QCA technology

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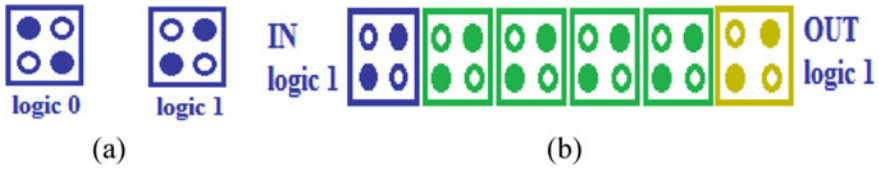

Fig. 1 **a** QCA cells logic '0' and logic '1', **b** schematic of binary wire

is proposed and it is implemented with less number of cells in such a way that it leads to better performance characteristics such as the reduction in delay, improvement in area utilization factor and helps for faster operation.

1.1 QCA Fundamentals

The cell is the elementary building element in QCA. Every cell has a proper configuration of charge to represent a binary bit. A cell contains four metal islands called quantum dots which act as conductors. Each quantum dot in a cell shows quantum mechanical properties. The cellular automata concept is because at any given cycle the configuration of a given cell relies on the configuration of its neighboring cells during the previous cycle. These dots are situated where the charges sit. Between these four quantum dots, the electrons in the cell can tunnel. In order to reduce the Coulomb force of repulsion, the electrons will occupy opposite diagonal quantum dots because they are more stable than electrons in adjacent quantum dots. This effect results in two possible configurations, each one will be used to represent a binary logic state '0' or '1'as shown in Fig. 1a.

By simply placing a negative potential to a lead close to the quantum dot occupied by an electron, the logic can be altered. To reduce the columbic force of repulsion, the ground state of the next cell is changed. This interaction between the cells allows the transfer of the information which helps to replace the physical interconnection of the devices. In this way, logic '1' or '0' is transmitted from one cell to another and thus acts like a binary wire as given in Fig. 1b.

1.2 Basic Gate Implementation Using QCA

The Columbic forces of repulsion are used to design the majority voter gate and inverter. By placing two QCA cells diagonally, due to Coulomb force of repulsion they will have opposite polarizations as shown in Fig. 2a, which works as an inverter whose output is inverse of the input.

The majority voter gate returns output logic which is equal to the logic of the majority of the inputs. For example, if we take a 3-input majority gate, if the inputs

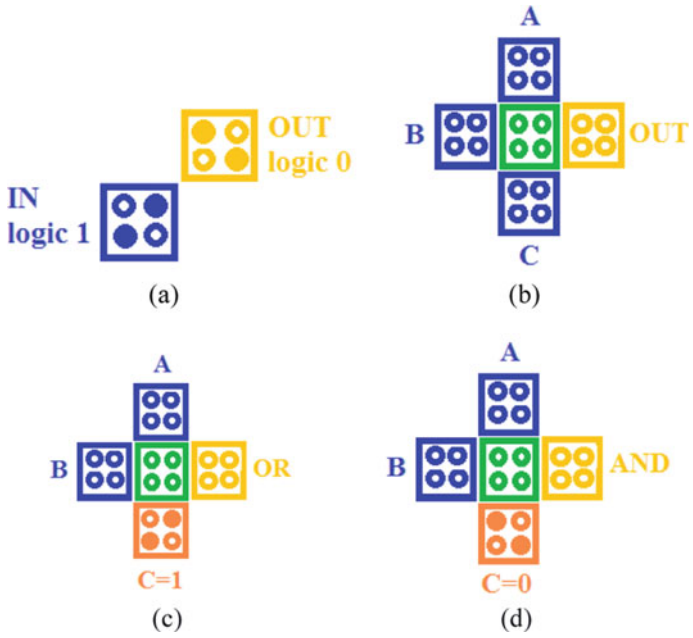

Fig. 2 QCA implementation of **a** inverter, **b** 3-input majority gate, **c** OR logic gate, **d** AND logic gate

are '110', then the output will be 1 which represents the most of the inputs. Hence, the final output function is given by OUT $= A \cdot B + B \cdot C + C \cdot A$ where A, B, C are data inputs and, OUT is the output of majority voter gate. QCA realization of the majority gate is shown in Fig. 2b.

When one of the inputs is fixed at 0, the majority gate works like AND gate. QCA realization of OUT $= A \cdot B$ (Boolean expression of AND gate) is shown in Fig. 2d. Similarly, the majority gate works like an OR gate, when one of the inputs is kept at 1. The QCA realization of OUT $= A + B$ (Boolean expression of OR gate) is shown in Fig. 2c

2 Implementation of Proposed D-FF Using QCA

Flip flop is a fundamental block of any sequential logic circuit, hence constructing flip flops using QCA technology is one of the prime importance of current research. Flip flops are used for memory storage as well as for data processing. The major functions of D-flip flop are to provide a delay in timing circuits, sampling data at specific intervals.

2.1 *Proposed Positive Edge-Triggered D-FF*

The schematic diagram of the proposed positive edge-triggered flip flop is shown in Fig. 3a. The clock is used as a select for the first mux and $\overline{\text{clock}}$ is used as a select for the second mux. When the clock is LOW, i_o is selected in the first mux and the output of the first mux is *D* which becomes available as an input of i_o of second mux. When the clock rises from LOW to HIGH, the first mux continues to be in the previous state, and for the second mux since $\overline{\text{clock}}$ is LOW, i_o of second mux is selected and already available *D* at i_0 of the second mux comes out as output. Thus, the above circuit acts as the rising edge *D* flip flop. Figure 3b shows the QCA realization of the proposed rising edge-triggered *D* flip flop design.

2.2 *Proposed Negative Edge-Triggered* D-*FF*

In Fig. 4a, $\overline{\text{clock}}$ is used as select for the first mux and clock is used as select for

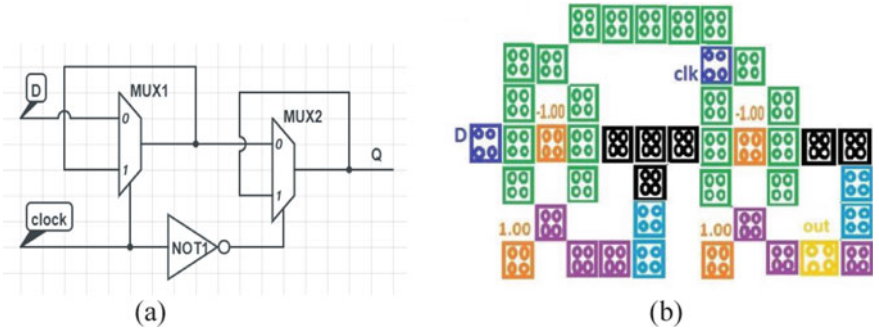

Fig. 3 **a** Schematic diagram of proposed positive edge-triggered FF, **b** proposed positive edge-triggered FF in QCA

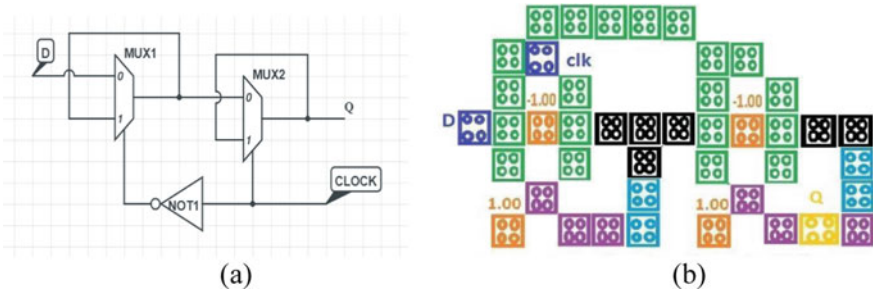

Fig. 4 **a** Schematic of proposed negative edge-triggered FF, **b** proposed negative edge-triggered FF in QCA

the second mux. When the clock is HIGH, i_o is selected in the first mux and the output of the first mux is D which becomes available as input of i_o of second mux. When the clock falls from HIGH to LOW transition, the first mux continues to be in the previous state, and for the second mux since the clock is low, i_o is selected and already available D at i_o comes out as output. Thus, the above circuit acts as the falling edge or negative edge D-flip flop. Figure 4b shows the QCA realization of falling edge-triggered D-FF design.

2.3 *Proposed Design of D-FF with Set/Reset Ability*

Asynchronous inputs: In a flip flop, those inputs which can control outputs independent of clock signal status are called asynchronous inputs. Asynchronous inputs in a given flip flop are preset and clear. The 'preset' changes FF output to logic 1 and the 'clear' resets the output to 0.

In our proposed work, rising and falling edge-triggered D-flip flops with asynchronous Set/Reset are implemented. In our design (shown in Fig. 5a, b), a 2:1 multiplexer (mux3) is used for adding Set/Reset functions for the proposed flip flop

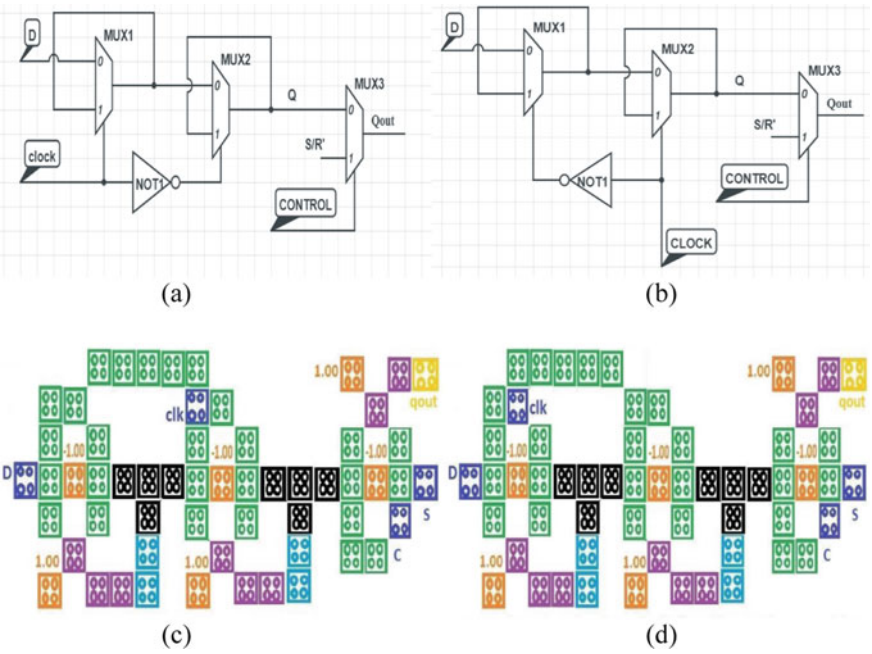

Fig. 5 Schematic diagram of proposed D-flip flop with asynchronous set/reset abilities **a** rising edge triggered, **b** falling edge triggered, proposed D-flip flop with asynchronous set/reset abilities in QCA, **c** rising edge, **d** falling edge

designs. In this asynchronous Set/Reset design, the input of D-flip flop is D and the output of D-flip flop is represented as Q. Q is given as i_o for mux3 and Set/Reset ($s/\overline{r}$) signal as i_1 for mux3 and control (C) is the select for mux3 and the output (Q_{out}) of the mux3 gives the required output with asynchronous Set/Reset abilities.

$$Q_{\text{out}} = Q \cdot \overline{C} + (s/\overline{r}) \cdot C$$

The proposed circuit uses a simple 2:1 mux to include asynchronous Set/Reset inputs. With the help of the control line, we can enable the Set/Reset ability which is shown in Fig. 5c, d

2.4 Implementation of 3-Bit Shift Register Using Proposed D-FF

Flip flops have the ability to store a single bit of data. In order to store more than one bit of data, we have to use registers which use multiple flip flops connected in a serial manner. For transferring the data bits stored within these registers, we have to use the clock signal as shown in Fig. 6a. In our proposed design of 3-bit shift register, 3 flip flops are connected serially.

The clock generator and the delay generator circuits [7] are used to implement the shift register. The control inputs ($C3$ and $C4$) in the clock generator are to activate the pulse generator to get the output pulse needed. The function of the control inputs is as follows:

1. If $C3 = 0$ and $C4 = 1$, then the pulse generator acts as a positive edge-triggered pulse generator.
2. If $C3 = 1$ and $C4 = 0$, then the pulse generator acts as a negative edge-triggered pulse generator.

In our proposed design, the positive edge-triggered pulse generator [7] has been used. For the function of the proposed shift register C5 of the delay generator is taken as 0. The delay generator is used to fix the timing issues between two Flip flops. Figure 6b, c shows the QCA implementation and its corresponding output waveforms.

3 Simulation Results and Discussions

QCA designer software version 2.0.2 has been used for simulating the proposed design. Bistable approximation engine has been used for simulating the circuits because it provides faster capability and all other simulation parameters and software settings were kept in a default configuration.

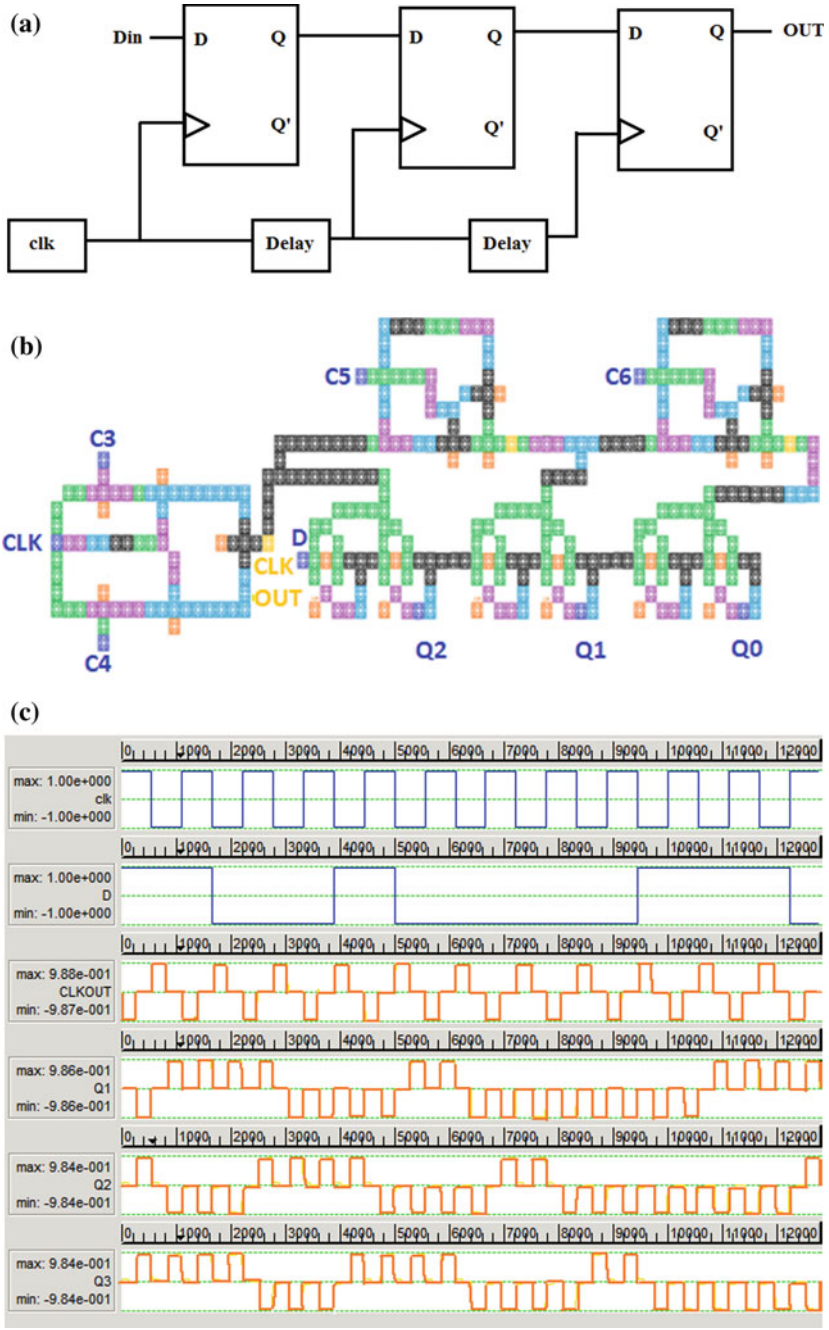

Fig. 6 **a** Schematic diagram of 3-bit serial shift register. **b** Schematic of 3-bit serial shift register using QCA. **c** Waveform of 3-bit serial shift register

We analyzed and verified the working of proposed designs for different kinds of inputs by using a Vector Table. QCA DesignerE has been used for finding the energy dissipation data.

The QCA circuit in [8] uses the master–slave configuration, and it contains 133 QCA cells and the latency of the circuit is two clock cycles. The multiplexer-based D-flip flops proposed in [9] have Set/Reset ability. This design occupies less cell area and less no. of cells compared to previous works of its time.

The flip flop proposed in [8] uses more no. of QCA cells which occupies more amount of area and has a latency of 2 clock cycles. The flip flop designed in [9] contains 56 cells and covers an area of 0.06 μm^2 and has a delay of 2.5 clock cycles which is high. To decrease the area and latency, we are using a mux-based flip flop design which decreases area and latency.

The cell count is 43 cells, the area occupied is 0.03 μm^2 and the latency is 1.5 in our proposed edge-triggered D-flip flop (both positive and negative edge-sensitive). The cell count is 58 cells, the area occupied is 0.05 μm^2 and the latency is 2.5 clock cycles for the proposed edge-triggered D-flip flop (both positive and negative edge-sensitive) with asynchronous Set/Reset inputs. Table 1 shows the performance comparison of the proposed flip flops with the various flip flop designs. Table 2 illustrates the power performance of the proposed designs. Table 3 gives the performance parameters of the 3-bit shift register implemented using the proposed D-flip flop. From Table 1, we can infer that the proposed D-flip flop is an improved version of erstwhile works in terms of cell count, area, and latency.

Table 1 Performance comparison of various flip flops with proposed D-flip flops

	Cell count	Area (μm^2)	Delay (clock cycle)	Set/reset ability
[8]	133	0.16	2.0	No
[9]	56	0.06	2.5	No
Proposed	43	0.03	1.5	No
[9]	79	0.12	3.0	Asynchronous
Proposed	58	0.05	2.5	Asynchronous

Table 2 Power performance of the proposed D-flip flop

Total energy dissipation (meV)	Average energy dissipation per cycle (meV)	Set/reset ability	Sensitive
2.38	0.216	No	Positive
2.15	0.196	No	Negative
29.7	2.7	Asynchronous	Positive
27.8	2.52	Asynchronous	Negative

Table 3 Performance analysis of 3-bit serial shift register

3-bit shift register parameters	Data
Total area	0.52 μm^2
QCA cell count	359
Total energy dissipation	1.38e−001 eV
Average energy dissipation per cycle	1.25e−002 eV

4 Conclusion

The proposed QCA design of positive and negative edge-triggered D-flip flop consists of 43 cells, area = 0.03 μm^2, delay = 1.5 clock cycles. Proposed QCA design of positive and negative edge-triggered D-flip flop with asynchronous Set/Reset consists of 58 cells, area = 0.05 μm^2, delay = 2.5 clock cycles. There is a 23% decrease in cell count, a 50% decrease in area, a 40% decrease in latency in our design of edge-triggered D-flip flop when compared to the existing circuits. There is a 27% decrease in cell count, a 58% decrease in area, a 17% decrease in latency in our design of edge-triggered D-flip flop with asynchronous Set/Reset ability when compared to the existing circuits. An efficient shift register QCA circuit has been implemented using the proposed D-flip flop circuit. Thus, our proposed design reduces the no. of QCA cells used, the occupied area, and the latency when compared to the past works. Dual edge-sensitive Flip flop can also be designed using the proposed flip flop. For the proposed design, synchronous Set/Reset capability can be added. It can be used in designing digital circuits such as counters, registers, memory cells.

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A Novel High-Throughput Medium Access Control Protocol for Concurrent Transmissions in Internet of Things

Shubham Gupta, Arun Kumar Khosla, Pawan Kumar Verma, and Rajesh Verma

1 Introduction

Today, the Internet-of-things (*IoT*) paradigm has become a necessity of the world. The term "IoT" is mainly concerned with the interconnectivity of smart devices or "things" to analyze the situation and perform accordingly. A large number of such devices are deployed to perform multiple tasks in certain geographical areas [1]. While having such a smart scenario, we still have some limitations. To accommodate a large number of devices which are trying to communicate with each other, we need to find a way to use the channel efficiently so that concurrent transmissions could take place [2].

To support massive channel access in *IoT*, we have several contention-based *MAC* protocols (such as *CSMA, ALOHA and Slotted-ALOHA*) and reservation-based *MAC* protocols (such as *TDMA, FDMA, CDMA and IEEE 802.11 DCF*). Out of these medium access control protocols, *CSMA* and *IEEE 802.11 DCF* have been regarded as the best contention-based and reservation-based *MAC* protocols, respectively, for a wireless ad hoc network. But still, these protocols have some restrictions as they do not allow concurrent transmission with devices in its proximity range even if it is

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possible [3, 4]. Thus, in this paper, we propose an *HT-MAC* protocol that supports concurrent transmission.

High-throughput *MAC* (*HT-MAC*) for concurrent transmission has a time frame structure, where each frame is comprised of two portions: one is contention interval (*CI*) and another is transmission interval (*TI*), where *CI* supports *CSMA/CA*, while *TI* supports concurrent transmission [5].

The rest of the sections in this paper are organized as follows. In Sect. 2, we highlight the background and related work. Section 3 is further categorized in three subsections, first one explaining the network scenario, where the proposed *HT-MAC* protocol is used. The second subsection explains the operation of each time frame, and finally, the third subsection briefly summarizes the operation of *CT-MAC* protocol. Section 4 covers the simulation results followed by the conclusion in Sect. 5.

2 Background and Related Work

Several attempts have been made earlier in single-hop multiple concurrent transmissions just to enhance the throughput of the network. As 802.11 *DCF* is a four-way handshaking mechanism, some researchers have modified the protocol by inserting an Addition Control Gap (*ACG*) between *RTS/CTS* and *DATA* packets for concurrent transmission scheduling. This gives the neighboring nodes within the proximity range of the primary nodes (which first schedule their transmission) to attempt for the channel access for transmission (only during the *ACG* period). In *MBAA-MAC* protocol [6], such concurrent transmissions take place. Though this protocol outperforms the *IEEE 802.11DCF*, still it has a multi-beam direction antenna that reduces the coverage of antenna. Therefore, it may cause the communication links to break in the network. Additionally, in the *POWMAC* protocol [7], the concurrent transmission is possible, but at the cost of a large number of limitations, and requires an additional hardware. That could make its commercial implementation complex.

3 System Model

In this section, we discuss a network scenario having densely deployed devices enabled with *CT-MAC* protocol. In this scenario, all the deployed devices are in the proximity range of gateway. It also explains the operation of time frame of the proposed *HT-MAC* protocol, along with the brief details of *CT-MAC* protocol.

3.1 Network Scenario

Figure 1 shows 3 crystal-like networks having one backbone network (gateway) along with 14 multi-sub-networks (nodes) in each crystal. All the sub-networks are in the proximity range of the backbone network and are *CT-MAC* enabled. The backbone network controls different sub-networks and acts as a medium between the device domain and the application domain as shown in the system model in [8]. On the one hand, it collects and transfers data to the application domain, while, on the other hand, it notifies devices about the contention among devices and subsequent transmissions from those devices using the frame structure as shown in Fig. 2. The gateways manage access control, security-related issues, multimedia conversion and quality of services (QoS).

In our proposed scenario, we assume there are total P devices, and the number of active devices is Q during single-frame transmission. Therefore, during each frame,

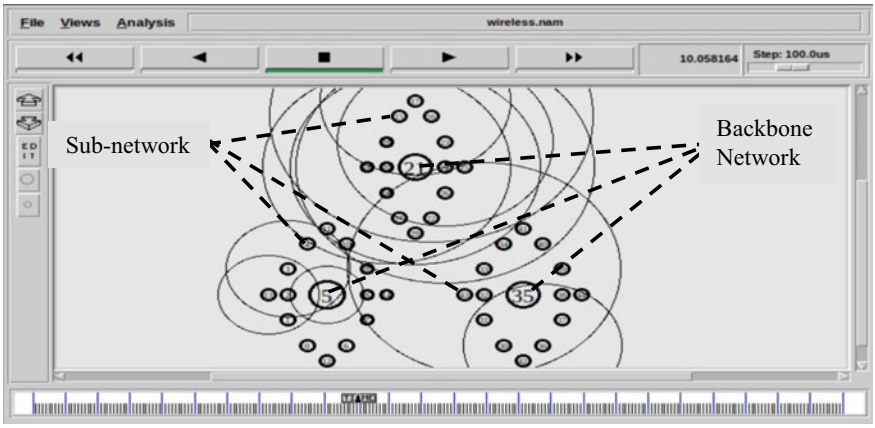

Fig. 1 A scenario of 42 sub-network having 3 backbone networks

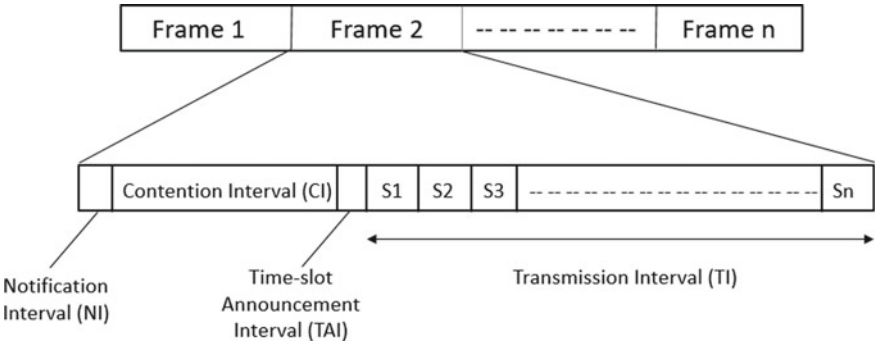

Fig. 2 Shows the frame categorization of the CT-MAC protocol

we have (*P*-*Q*) silent devices that are in power-saving mode. Also after *CI*, let *R* devices succeed which means (*Q*-*R*) devices fail to participate in that frame. Hence, *R* devices win the *TDMA* time slots and transmit data during the *TI* period.

3.2 Time-Frame Structure Operation

Figures 2 and 3 show the each frame categorization of the proposed *HT-MAC* protocol. The frame is comprised of 4 parts, namely notification interval (*NI*), contention interval (*CI*), time-slot assignment interval (*TAI*) and transmission interval (*TI*). Initially, the gateway announces to the devices *(P)* about the arrival of *CI* frames during its *NI* period. During *CI* all the active devices *Q* participate to access the channel. *CI* follows a *p*-persistent *CSMA* protocol and makes *R* devices succeed.

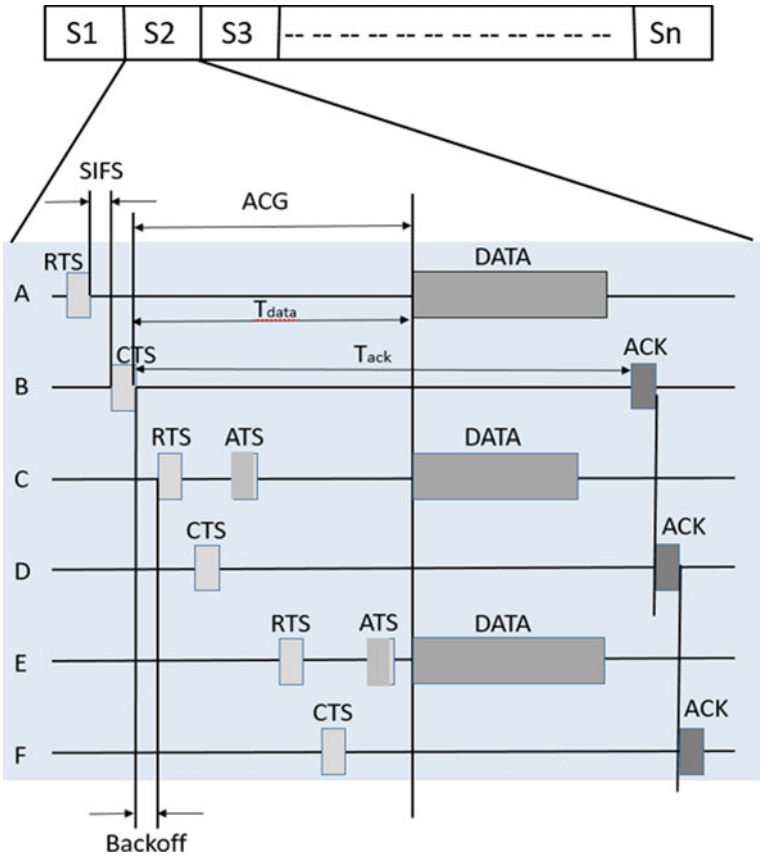

Fig. 3 The concurrent transmission management in each time slots

As soon as the *CI* period ends, the gateway announces the declaration to all the active devices that contention period is over and *TI* is about to begin. All this broadcasting happens during the *TAI* period. In addition to this, the gateway also distributed the time slots to each qualifying device. Now *TI* follows time division multiple access (*TDMA*) mechanism and allots the different time slots to all the successful devices (*R*) [8]. Now, as all the devices are *CT-MAC* enabled; therefore, in each *TDMA* time slot, there will be multiple concurrent transmissions as shown in Fig. 3. Thus, on a complete note, our protocol utilizes the services of *p*-persistent *CSMA* [9], *TDMA* [10], and *CT-MAC* [5] protocol. Additionally, due to these concurrent transmissions within each *TDMA* time slot, the proposed protocol exhibits significant increase in throughput and decrease in end-to-end delay among adjacent node transmissions. As shown in Fig. 2 given, *S*1, *S*2, *S*3, …, *Sn* are equal time slots of *TI*. As soon as the gateway receives the small transmission request messages during *CI* period from the devices within its proximity range, it starts assigning different time slots to different devices one by one. Such a scenario is shown in Fig. 3, where three transmitters *A, C* and *E* are transmitting data concurrently to their respective receivers *B*, *D* and *F*.

Note that each device is *CT-MAC* protocol enabled and its operation is described below in the next subsection. In our time frame structure, we fix the duration of each frame as *T*frame that should always be greater than the sum of *T*CI and *T*TI, i.e.,

$$T_{\text{frame}} > T_{\text{TI}} + T_{\text{CI}} \tag{1}$$

Thus, it is interesting to observe that if we increase the *CI* duration, *TI* duration will decrease. Moreover, the count of successful devices will also increase and now we have fewer transmission slots available resulting in lesser no. of transmissions. On the other hand, if we invert the scenario such that the *TI* duration is increased, then *CI* duration will automatically decrease, and we will be left with more number of transmission slots but less number of successful devices from contention. Thus, we need to balance the situation as shown in [8]. Moreover, the mathematical modeling and experimentation of this time-frame structure have already been discussed in [11].

3.3 Operation of CT-MAC Protocol

CT-MAC is the modified or extended form of the original *IEEE 802.11 DCF*. The concept of a negative *CTS* packet is added along with *ATS* (adjust-to-send or abrogate-to-send) packet that allows concurrent transmissions. Normal *CTS* (clear-to-send) packet from the receiver informs the transmitter that it is ready to receive *DATA* just like *IEEE 802.11 DCF*, while in *CT-MAC*, depending on the situation, receiver is free to modify the values of *T*data and *T*clk delivered by the transmitter in the *RTS* packet and overwrites the new value [5].

In Fig. 3 shown above, node *A* transmits an *RTS* packet to receiver node *B* that includes *A's* start time of data packet (T_{data}) and *B's ACK* packets starting time (*T*clk). These nodes are called the primary transmitter–receiver pair. During this duration,

C and *E* are free to initiate their exchange process. But, as *C,* and *E* cannot schedule their transmissions to *D and F,* before that of *A*, they are called secondary transmitter and receiver pairs, respectively [5].

The *ATS* packet for the secondary transmitter acts in two situations. Firstly, when the secondary receivers (*D* and *F*) modify the values of *T*data or *T*clk set by the secondary transmitter, *ATS* from the secondary transmitter informs the neighbors about the modification. Secondly, when it is not possible for the secondary receiver to receive the data, it sends a negative *CTS* packet, and accordingly, *ATS* from the secondary transmitter informs the neighbors to cancel the schedule [5].

Moreover, the *ACK* packet is synchronized in such a way that all the slave receivers send the packets in sequence after the one master receiver sends. Thus, this eliminates the risk of collision between *ACK* and *DATA* packets. The detailed operation is shown in [5].

4 Simulation Results

We have simulated the scenario on network simulator (version 2.35) ns-2 [12], on UBUNTU 12.04 LTS platform. The simulation parameters are summarized in Table 1. We have compared the performance of *HT-MAC* and *IEEE 802.11 DCF* in terms of per time-slot throughput as shown in Fig. 4a–c. We consider the data packet as fixed

Table 1 Simulation parameters

Propagation model	Free space path loss model
Data packet size	2 KB
Data rate	2 Mbps
Area of transmission	800*800 m^2
SINR	6 dB
Frame duration (*T*frame)	1500 ms
Interval for individual *IoT* device	2.5 ms
Notification Interval duration (*T*NI)	8 us
Contention Interval duration (*T*CI)	10.5 us
Time-slot announcement interval duration (*T*TAI)	10.5 us
Acknowledgement duration (*T*ACK)	8 us
Short inter-frame space duration (*T*SIFS)	2.5 us
Back-off inter-frame space duration (*T*BIFS)	7.5 us

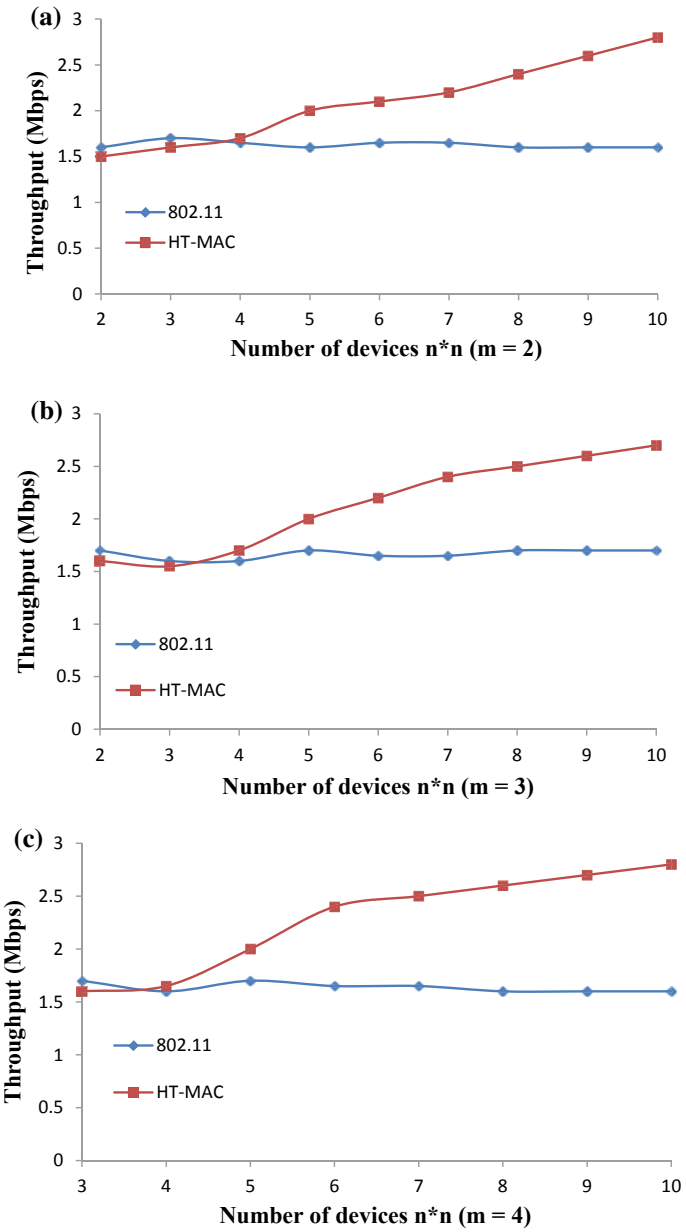

Fig. 4 **a** Throughput of *HT-MAC* versus *IEEE 802.11 DCF* protocol when $m = 2$. **b** Throughput of *HT-MAC* versus *IEEE 802.11 DCF* protocol when $m = 3$. **c** Throughput of *HT-MAC* versus *IEEE 802.11 DCF* protocol when $m = 4$

2 KB in size. Here, we have considered three different scenarios of concurrent transmissions with corresponding simulation results showing significant improvement in the throughput.

First, we consider a square area (800×800) m^2, where nodes are placed randomly in a grid topology, total grid having split $n * n$ small squares. Let us consider there are m concurrent transmissions in each *TDMA* time slot, and the transmitter devices are always ready to send packets. In contrary to this concurrent transmission, in *IEEE 802.11 DCF* protocol, there will be only one transmission at a time.

The performance shown in Fig. 4 indicates that the density of nodes directly affects the overall throughput of the network of our proposed *HT-MAC* protocol. As the node-density increases, throughput increases, and the average spacing between the transmitter and receiver node (neighboring grids) decreases. Therefore, it allows more concurrent transmissions, which in turn increases the overall throughput of the network.

5 Conclusion

In this paper, we have proposed the *HT-MAC*, a high-throughput medium access control protocol for densely deployed IoT devices. The proposed protocol is capable of allowing maximum possible concurrent transmissions per *TDMA* time slot. The proposed protocol consists of a time frame containing contention interval (*CI*) enabled with *CSMA/CA* protocol and a transmission interval (*TI*) enabled with *TDMA* scheme. Within each *TDMA* time slot, the devices use the *CT-MAC* protocol for concurrent transmissions. We have simulated the scenario, where the communicating devices are placed in a random grid topology. We have positioned each node in such a way that each of them is within the proximity range of the gateway. The simulation results show more than 150% increase in per time-slot throughput in comparison with the standard *IEEE 802.11* protocol.

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A Comparative Investigation of SiGe Junctionless Triple Gate (JLTG) and Junctionless Gate-All-Around (JL-GAA) MOSFET

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1 Introduction

According to the International Technology Roadmap for Semiconductors (ITRS) roadmap [1], the MOSFET sizes shrinking conventionally down to the nanometer regime. We are facing with short channel effects (SCEs) [2, 3] like poor sub-threshold swing, high drain-induced-barrier-lowering (DIBL), increased leakage currents, etc., leading to sub-optimal performance of transistors [4, 5]. Researchers have studied several architectures and techniques like junctionless devices [6], multi-gate architecture [7], hetero-high-κ gate oxides [8], lower doping concentrations, high mobility substrate materials that allow lower device size, but without the disadvantage of severe SCEs [9, 10]. Saini et al. showed that among all other multi-gate architectures, triple gate junctionless devices exhibit superior gate controllability [11–14]. Recently, gate-all-around nanowire has become a promising architecture for scaling of MOSFETs [15, 16].

In this paper, we compare two junctionless multi-gate (JLMG) architectures: junctionless gate-all-around (JL-GAA) and junctionless triple gate (JLTG) each with different high-κ gate oxides to further improve the gate control. These devices derive the advantage of high mobility of Silicon–Germanium material (1538 $cm^2/V \cdot s$ at 6×10^{17} cm^{-3} doping) [17]. Section 2 explains the structure and simulation of these devices. Section 3 comprises extensive comparison between the devices basis electrostatic, analog and RF parameters. Conclusions are summarized in Sect. 4.

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2 Device Structure and Simulation

Two junctionless devices of Silicon–Germanium material are discussed, both with a uniform n-type doping concentration of 3×10^{19} cm^{-3}, gate electrode workfunction 5.0 eV, and channel length of 20 nm. The junctionless gate all-around (JL-GAA) device has a circular cross section of SiGe substrate (diameter 6 nm). Figure 1 shows the 3D and 2D representation of the JL-GAA device, which has two layers of oxides, HfO_2 ($\kappa = 22$) of thickness 2.5 nm stacked over SiO_2 ($\kappa = 3.9$) of thickness 0.5 nm [insert Arunabh/16]. The junctionless triple gate (JLTG) device has a rectangular cross section of SiGe substrate (6 nm × 6 nm). Figure 2 shows the 3D and 2D representation of JLTG device, which includes four oxide materials. SiO_2 ($\kappa = 3.9$) and Si_3N_4 ($\kappa = 7.5$) with thickness 0.5 nm constitute the bottom oxide layer. HfO_2 ($\kappa = 22$) and Al_2O_3 ($\kappa = 9$) with thickness 2.5 nm constitute the top oxide layer [8].

Atlas 3D device simulator from Silvaco is used for simulating the two devices. Shockley–Read–Hall recombination model, concentration-dependent mobility model, field-dependent mobility model and CVT model are employed and the simulations are done at room temperature (300 K) [18]. The design parameters for JL-GAA and JLTG MOSFETs are presented in Table 1.

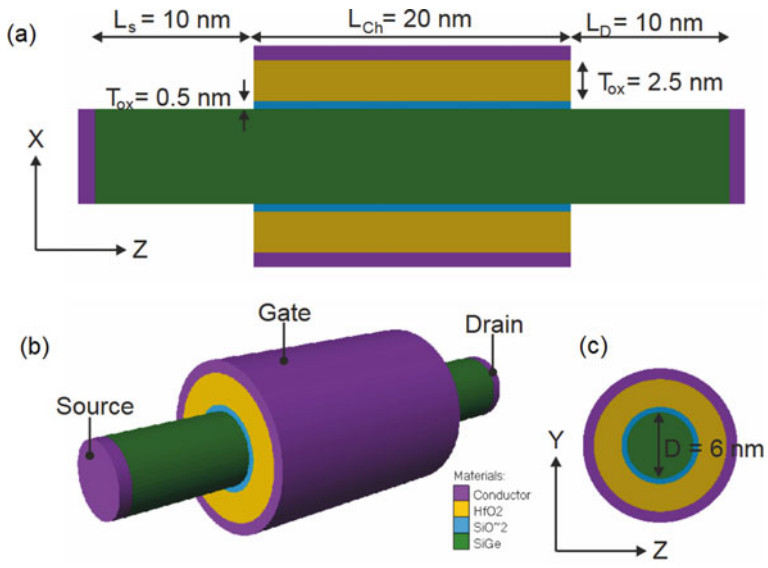

Fig. 1 **a** *XZ* cut plane view; **b** 3D view; **c** *YZ* cut plane view of junctionless gate-all-around (JL-GAA) device

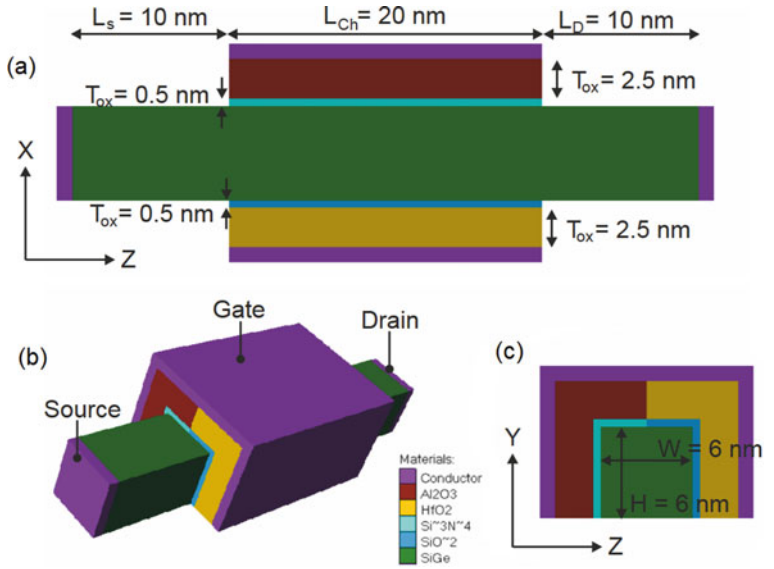

Fig. 2 **a** *XZ* cut plane view; **b** 3D view; **c** *YZ* cut plane view of junctionless triple gate (JLTG) device

Table 1 Design parameters

Parameters	JL-GAA	JLTG
Mole fraction (Si_xGe_{1-x})	$x = 0.5$	$x = 0.5$
Channel length	20 nm	20 nm
Source and drain length	10 nm	10 nm
Gate electrode workfunction	5.0 eV	5.0 eV
Doping concentration	3×10^{19} cm^{-3}	3×10^{19} cm^{-3}
Total effective oxide thickness	$\sim$ 0.68 nm	$\sim$ 0.68 nm(SiO_2 and HfO_2), $\sim$ 1.02 nm(Si_3N_4 and Al_2O_3)

Table 2 Electrostatic FOMs

Parameter	JL-GAA	JLTG
On/off ratio	4.6605×10^{9}	1.1249×10^{6}
Threshold voltage (at $V_{DS} = 1.0$ V) (V)	0.5241	0.2685
Off-state leakage current (A)	1.8935×10^{-15}	1.0599×10^{-11}
On-state current (A)	8.8246×10^{-6}	1.1923×10^{-5}
Sub-threshold swing (mV/dec)	60.4139	63.5693
DIBL (mV/V)	13.2056	29.8811

3 Results and Discussion

3.1 Electrostatic Performance

For comparing the two devices on the basis of electrostatic performance, important figure of merits (FOMs) like on/off current ratio, threshold voltage, off-state leakage current, sub-threshold swing, drain-induced barrier lowering (DIBL) are considered.

JL-GAA exhibits a considerable advantage over JLTG structure in terms of gate controllability. As evident from Table 2, JL-GAA shows an on/off ratio of 3 orders of magnitude greater than JLTG (~ 4100 times), accompanied with an approximately 99% lower leakage current. This can be attributed to the gate-all-around architecture in JL-GAA, which alleviates the non-uniform gate control observed in JLTG by reducing the impact of drain region on the electrostatics of channel region [19]. Burenkov et al. investigated the persistent corner effect in double and triple gate devices which gives rise to additional leakage current, thus deteriorating the overall performance [20, 21]. It is also worth mentioning that JL-GAA shows 56% lower DIBL than JLTG. The sub-threshold swing of both devices is found to be above 60 mV/dec, which makes both the devices suitable for low power applications.

Figure 3 shows drain current and trans-conductance as a function of gate voltage at $V_{DS} = 1.0$ V. It may be noted that the on-state current of JLTG device is 35% higher than that of JL-GAA. Trans-conductance (g_m) may be viewed as the slope of drain current—gate voltage curve.

3.2 Analog Performance

A large part of the real-life applications require devices to exhibit exceptional analog performances. To evaluate the two devices for the same, analog FOMs like Early voltage, intrinsic gain, output conductance, trans-conductance and trans-conductance generation factor (TGF) are considered.

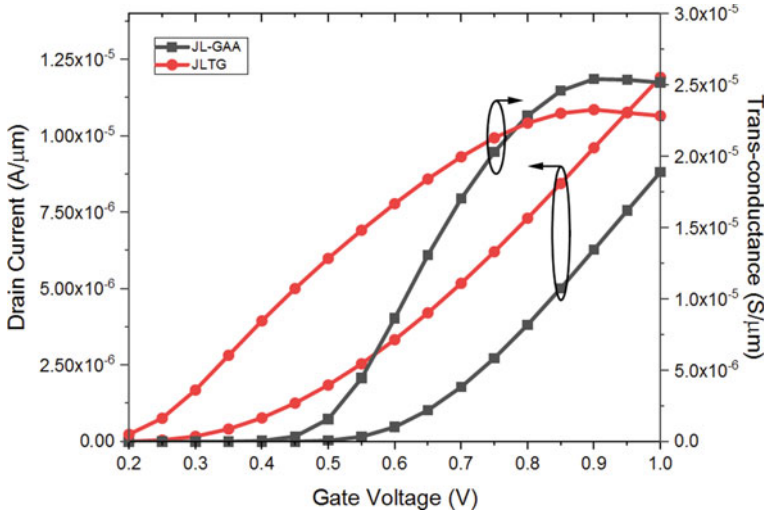

Fig. 3 Drain current and trans-conductance as a function of gate voltage at $V_{DS} = 1.0$ V

Figure 4 shows the variation of early voltage and intrinsic gain as a function of gate voltage, at $V_{DS} = 1.0$ V, which are expressed as:

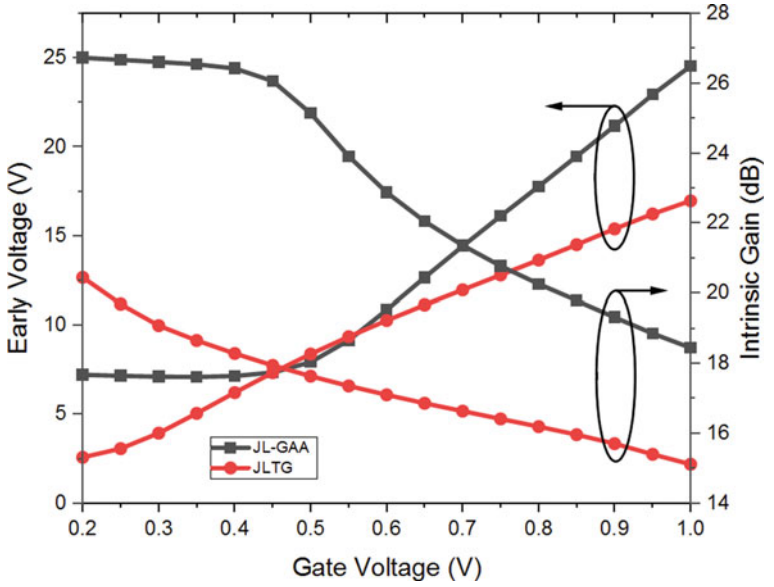

Fig. 4 Early voltage and intrinsic gain as a function of gate voltage at $V_{DS} = 1.0$ V

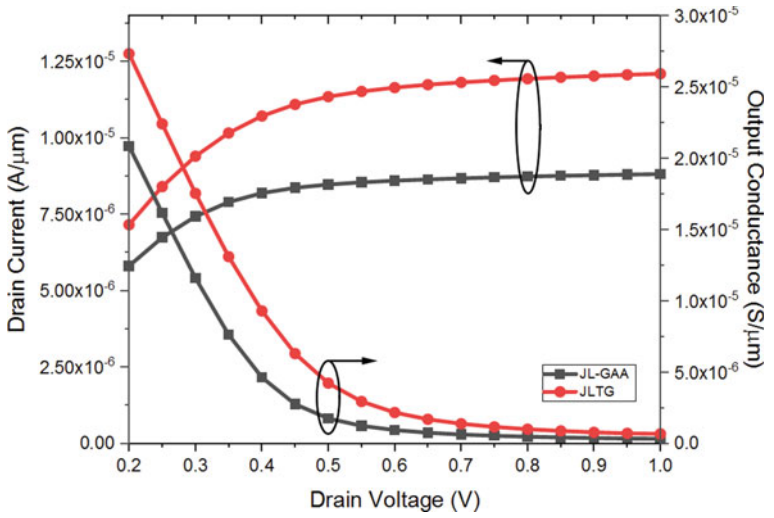

Fig. 5 Drain current and output conductance as a function of drain voltage at $V_{GS} = 1.0$ V

$$\text{Early Voltage, } V_{EA} = \frac{I_D}{g_d} \tag{1}$$

$$\text{Intrinsic Gain, } A_v = \frac{g_m}{g_d} \tag{2}$$

In the case of JL-GAA, early voltage is observed to be higher than in JLTG, indicating that JL-GAA suffers less from channel length modulation effect as compared to JLTG device. The intrinsic gain is also considerably higher in case of JL-GAA for all values of gate voltage. Considering the peak values, it may be compared that JL-GAA shows ~ 44% higher early voltage as well as ~ 30% higher intrinsic gain than JLTG. Figure 5 shows the output characteristics—drain current as a function of drain voltage, along with output conductance (g_d) at $V_{GS} = 1.0$ V. Clearly, JLTG has higher drain current and output conductance as the drain voltage increases. It may be emphasized that JLTG shows ~ 95% higher output conductance than JL-GAA, indicating an overall lower output resistance, favoring higher on-state current. Output conductance is calculated as

$$g_d = \frac{dI_{DS}}{dV_{DS}} \tag{3}$$

The variation of trans-conductance (g_m) and trans-conductance generation factor (TGF) as a function of gate voltage at $V_{DS} = 1.0$ V is shown in Fig. 6 which are calculated as

$$g_m = \frac{dI_{DS}}{dV_{GS}} \tag{4}$$

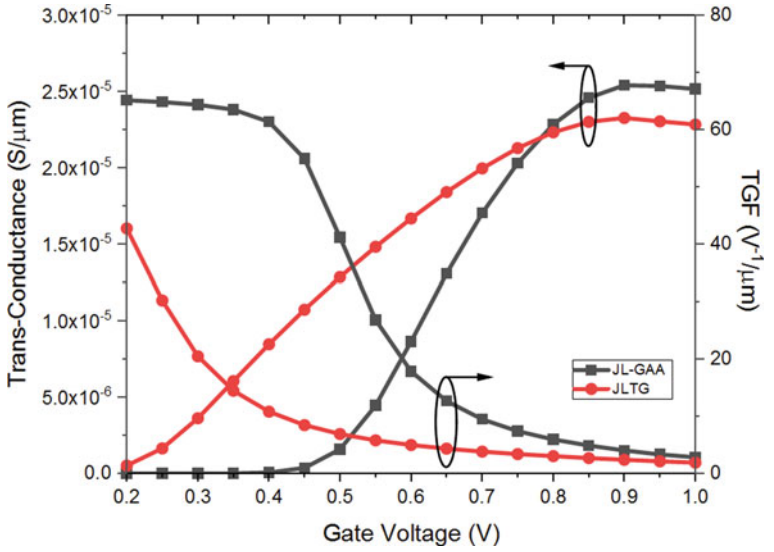

Fig. 6 Trans-conductance and trans-conductance generation factor (TGF) as a function of gate voltage at $V_{DS} = 1.0$ V

Table 3 Analog FOMs

Parameters	JL-GAA	JLTG
Early voltage (V)	24.552	16.979
Intrinsic gain (dB)	26.7376	20.4550
Output conductance (S)	3.5942×10^{-7}	7.0224×10^{-7}
Trans-conductance (S)	2.5428×10^{-5}	2.3282×10^{-5}
Trans-conductance generation factor (V^{-1})	65.1872	42.7808

$$\text{TGF} = \frac{g_m}{I_D} \tag{5}$$

Considering the peak values of these parameters, JL-GAA shows 9.26% higher g_m as well as ~ 52% higher TGF than JLTG. This further reinforces the superior analog performance of JL-GAA over JLTG. Table 3 summarizes the peak values of analog FOMs for both the devices.

3.3 RF Performance

Nowadays, a number of commercial applications like mobile telephony, amplifiers, transmitters, etc., demand MOSFETs with exceedingly high RF performance, which

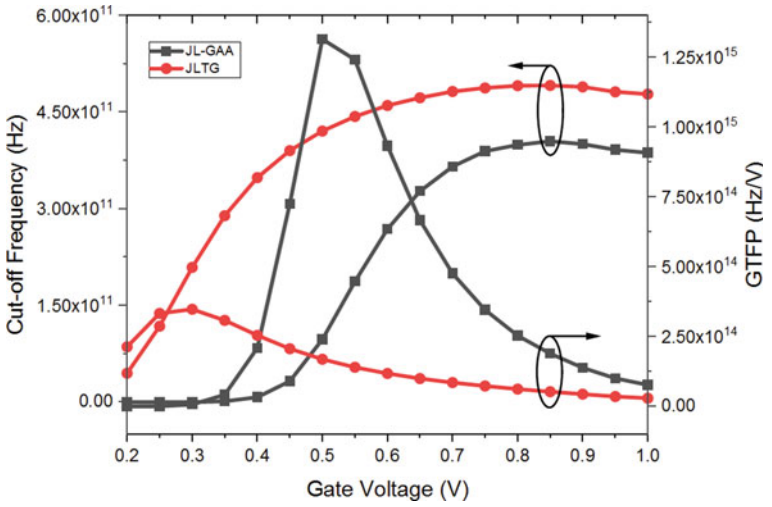

Fig. 7 Cut-off frequency and GTFP as a function of gate voltage at $V_{DS} = 1.0$ V

can be reliably measured in terms of RF FOMs like cut-off frequency, gain trans-conductance frequency product (GTFP), intrinsic gate capacitances (gate-to-source and gate-to-drain), gain frequency product (GFP) and trans-conductance frequency product (TFP).

A DC ramp voltage of 0–1 V with step size of 50 mV at 1 MHz frequency is used to calculate these FOMs. Cut-off frequency and GTFP as a function of gate voltage are shown in Fig. 7. It can be observe that cut-off frequency increases rapidly after gate voltage equal to threshold voltage of respective devices, and although JLTG shows higher cut-off frequency for the whole range of gate voltage, JL-GAA shows a significantly high peak in GTFP, indicating a better trade-off point [22]. Also, higher cut-off frequency in JLTG device signals lower delay time for electrons to transit from source to drain [23, 24].

Cut-off frequency is given as

$$f_T = \frac{1}{2\pi} \frac{g_m}{(C_{gs} + C_{gd})}, \text{ and GTFP} = \left(\frac{g_m}{g_d}\right) \times \left(\frac{g_m}{I_D}\right) \times f_T \tag{6}$$

Figure 8 shows the variation of intrinsic capacitances C_{gs} and C_{gd} as a function of gate voltage. C_{gs} for both devices is of the order of 10^{-18}, and increases as the gate voltage is increased. C_{gd} for JL-GAA is at most 5.1909×10^{-19} F, which is ~ 10% lower than JLTG.

GFP is given as GFP $= \left(\frac{g_m}{g_d}\right) \times f_T$, and TFP $= \left(\frac{g_m}{I_D}\right) \times f_T$. Figure 9 shows their variation for both the devices as a function of gate voltage. GFP peaks are observed at gate voltages greater than respective threshold voltages of both devices, and similar

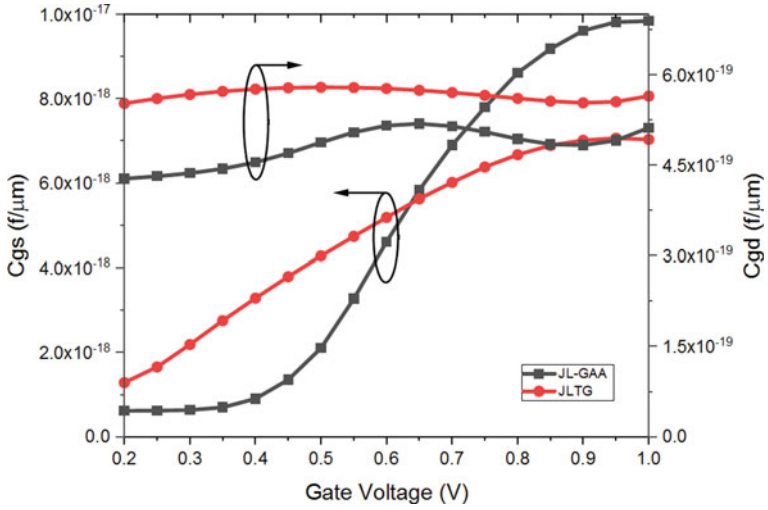

Fig. 8 Intrinsic capacitances (gate-to-source (C_{gs}), gate-to-drain (C_{gd})) as a function of gate voltage at $V_{DS} = 1.0$ V

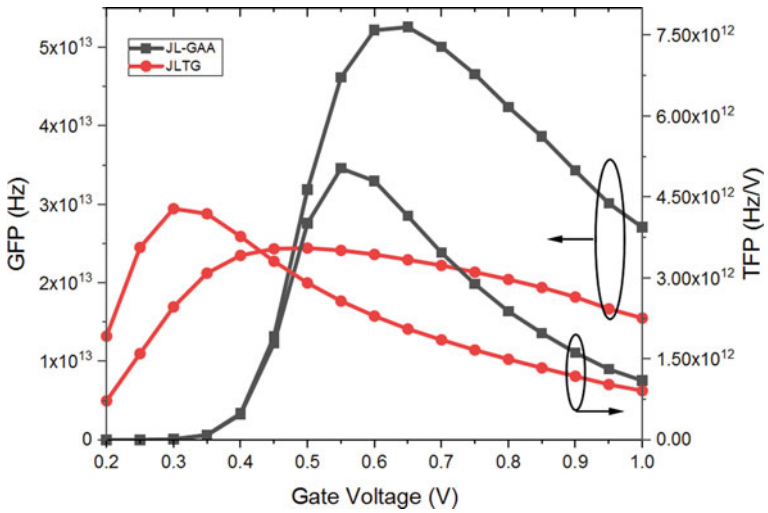

Fig. 9 GFP and TFP as a function of gate voltage at $V_{DS} = 1.0$ V

pattern is observed for TFP as well. It may be noted that JL-GAA shows higher peak values for both GFP and TFP than JLTG.

Table 4 summarizes the peak values of RF FOMs for both devices. It is worth mentioning that JL-GAA shows ~ 278% higher GTFP, ~ 115% higher GFP and ~ 17% higher TFP than that of JLTG. Further, the symmetry of gate oxides in JL-GAA contributes to ~ 10% lower C_{gd} than JLTG.

Table 4 Peak values of RF FOMs

Parameters	JL-GAA	JLTG
Cut-off frequency (Hz)	4.0504×10^{11}	4.9165×10^{11}
Gain trans-conductance frequency product (Hz/V)	1.3157×10^{15}	3.4815×10^{14}
Gate-to-source capacitance (C_{gs}) (F)	9.8504×10^{-18}	7.0700×10^{-18}
Gate-to-drain capacitance (C_{gd}) (F)	5.1909×10^{-19}	5.7952×10^{-19}
Gain frequency product (Hz)	5.2634×10^{13}	2.4476×10^{13}
Trans-conductance frequency product (Hz/V)	5.0379×10^{12}	4.2915×10^{12}

4 Conclusions

In this paper, two SiGe junctionless devices with hetero-high-κ gate oxides, namely JL-GAA and JLTG are compared on the basis of various important electrostatic, analog and RF FOMs. JL-GAA exhibits superior gate controllability and hence, an excellent on/off ratio $\left(\sim 5 \times 10^{9}\right)$, which makes it a good choice for high-switching-speed applications. It is also observed to have reduced short channel effects as compared to JLTG. Further, JL-GAA shows ~ 2.78 times higher GTFP than JLTG. Adding the fabrication feasibility of JL-GAA device, it is considered to be superior to JLTG overall.

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Thermal Stability Analysis of Graded-Channel Dual-Material Double-Gate (GCDMDG) MOSFET for Analog Application

Anjali Priya, Abhinav Gupta, Neha Agrawal, Sanjeev Rai, and Ram Awadh Mishra

1 Introduction

The advancement of semiconductor industries is a driving force for MOSFET scaling. But as the dimensions of the device are reduced, short channel effects degrade the performance of the device [1]. The scaling of channel length reduces the controllability of gate over the channel region by increasing the charge sharing from source/drain. Due to this, the threshold voltage of MOS device becomes smaller. According to international technology roadmap for semiconductor (ITRS) [2], inclusion of new technologies is turning out to be a critical issue for sub-nanometer MOS devices. Researchers are still working with many device structures to find out a device that can be used in high-frequency application with low power consumption.

Since past few decades, the double-gate (DG) MOSFET has shown potential in sub-nanometer regime due to its superb resistance to short channel effects (SCEs) [3]. Researchers have been working with various double-gate structures [4–9]. Many theoretical-, simulation- and experimental-based studies have been reported in the literature on DMDG MOSFET. Reddy et al. [10] have reported that the DMDG MOSFET can offer a noteworthy reduction in the hot carrier effects (HCEs). Increased drain breakdown voltage, reduced drain conductance, improved transconductance and desired threshold voltage roll off can be achieved with a DMDG MOSFET below 100 nm channel length. Other than above structures, there are more devices such as quadruple gate [11] MOSFET and Triple Metal Gate Recessed

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Source/Drain MOSFET [12] which are contributing to advance the device performance in terms of SCEs and current transport efficiency. These devices are also used to improve analog and RF performances.

To achieve improved ON current and reduced SCEs and HCEs, graded-channel-doped engineering has been explored. This can be done by providing low doping near the drain end and high doping near the source end. The peak electric field reduces near the drain end due to low doped region which in turn reduces the impact ionization and hence, HCEs at the drain side of the device. Along with these advantages, the graded-channel (GC) MOSFET also leads to an enhancement in ON current and transconductance compared to uniformly doped devices [13]. Chiang [14] proposed an analytical sub-threshold behavior model for single halo (SH) [15] dual-material gate (DMG) [16] silicon on insulator (SOI) MOSFET with graded-channel concept.

All the studies have demonstrated that both DMDG and GCDG MOSFETs are used to control SCEs and HCEs. In this paper, double-gate (DG) MOS transistors with both channel engineering and metal gate work function engineering have been used which provides better immunity to short channel effects. There are numerous applications in which the transistor at nano-regime is used at low and high temperatures. So, temperature plays important role in the stability of the device. First time in this paper, performance of various analog/RF parameters of graded-channel dual-material double-gate (GCDMDG) MOSFET has been studied over wide range of temperature to find thermal stability point (TSP). Thermal stability point (TSP) is defined as the gate voltage at which parameters show minimum variation over wide range of temperature [17–19]. In the analysis of stability issue, temperature is varied at wide range (200–500 K). Away from this thermal stability point, drain current shows reversed behavior with temperature deviation. It is because of high electric field and mobility degradation at larger bias. So, biasing in analog and digital circuits is preferred at TSP. Section 2 describes the GCDMDG device structure followed by the introduction. The thermal stability analysis of GCDMDG MOSFET is investigated in Sect. 3. Further, in Sect. 4, a common source amplifier has been designed using DMDG, GCDG and GCDMDG MOSFETs. The drain current, output voltage and gain of CS amplifier are also shown. Finally, Sect. 5 presents the conclusion of this paper.

2 Device Design Structure

The cross-sectional view of GCDMDG MOSFET is shown in Fig. 1. The graded-channel region contains two regions of L_1 and L_2 (where $L_1 + L_2 = L$.) with different doping concentration N_{a1} and N_{a2} where N_{a1} is greater than N_{a2} to reduce the impact ionization near the drain end. Source and drain have doping concentration of N_d. Gate insulator of SiO_2 has been used. The channel length, oxide thickness and silicon channel thickness are represented by L, t_{ox} and t_{si}, respectively. This device is biased with gate voltage of V_{gs}. For DMG structure, the two metals with different work function are taken in which work function of metal M_1 (Au) is higher than the metal

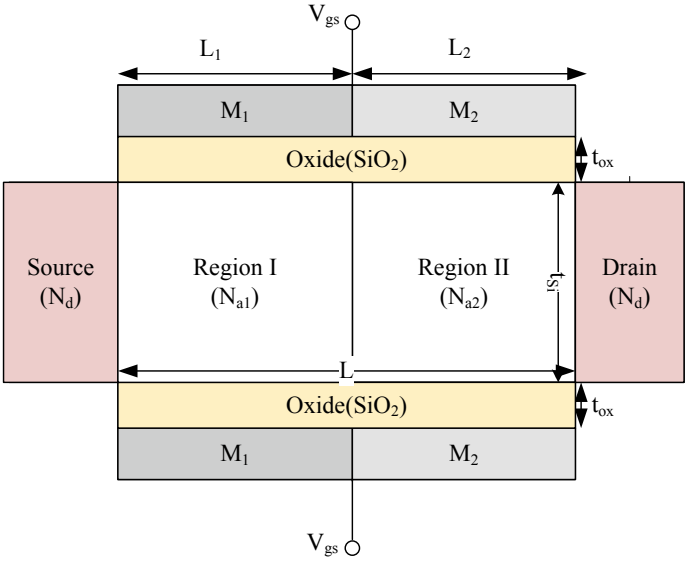

Fig. 1. 2D view of GCDMDG MOSFET

Table 1 Parameter values for device structure

Parameters	Values
L	60 nm
t_{ox}	2 nm
t_{si}	10 nm
N_d	1×10^{19} cm^{-3}
N_{a1}	1×10^{17} cm^{-3}
N_{a2}	1×10^{16} cm^{-3}
ϕ_{M1}	4.8 eV
ϕ_{M2}	4.6 eV
V_{ds}	0.1 V

M_2 (M_o). M_1 and M_2 are the control and screen gates, respectively. The values of the device parameters are shown in Table 1.

3 Thermal Stability Analysis

Thermal stability analysis has been explained in this section in terms of analog and radio frequency performance with temperature deviation. Figure 2 illustrates I_D and g_m variation with V_{GS} with varying temperature keeping V_{ds} as a constant. The

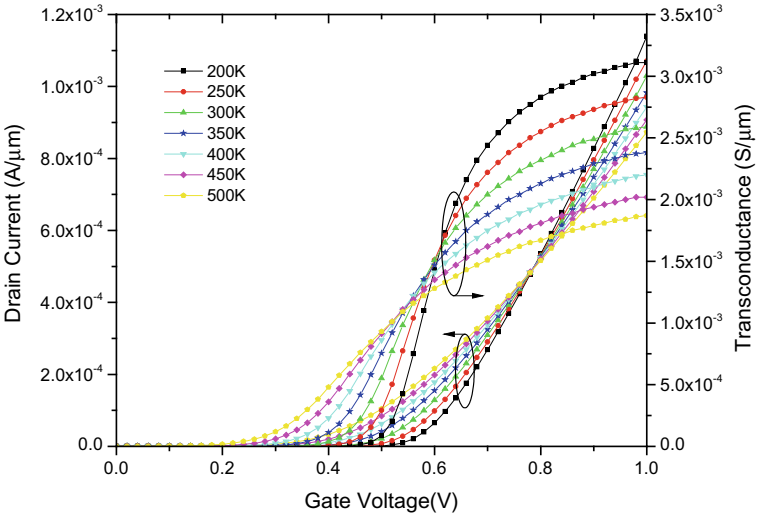

Fig. 2 I_D and g_m variation with V_{GS} with varying temperature

thermal stability point of drain current is found at $V_{gs} = 0.8$ V. It shows the bias point to keep DC level of current constant. Away from this thermal stability point, drain current shows reversed behavior with temperature deviation. It is because of high electric field and mobility degradation at larger bias. The TSP of transconductance is found about $V_{gs} = 0.55$ V. This point of transconductance shows the biasing point for stable circuit. So, biasing in analog and digital circuits is preferred at TSP.

Figure 3 illustrates g_m and TGF variation with V_{GS} with varying temperature. From the figure, it is found that the thermal stability point for TGF lies between $V_{gs} = 0.6$ V. Figure 4 demonstrates V_{ea} and A_V variation with V_{GS} with varying temperature. The TSP of early voltage is obtained at $V_{gs} = 0.6$ V. Since gain is dependent on early voltage, high gain has been obtained at this point due to high value of early voltage.

Figure 5 shows C_{gs} and C_{gd} variation with V_{GS} with varying temperature. It has been calculated at the 1 MHz frequency with ramp voltage 0–1 V. The graph shows the reversal of gate to source capacitance at particular gate bias, while gate to drain capacitance is increased by increasing bias. The TSP point of C_{gs} is 0.65 V. Figure 6 shows how the cutoff frequency and GTFP changes with change in gate voltage over 200–500 K. Cutoff frequency is reversed at TSP point which is from 0.5 to 0.6 V. Due to mobility degradation, cutoff frequency is better for lower temperature which shows the advantage of double-gate MOSFET. GTFP is reversed almost at 0.5 V (TSP point).

Figure 7 shows GFP and TFP variation with V_{GS} with varying temperature. GFP shows the maximum gain at particular frequency, whereas TFP explains the bottleneck between bandwidth and power. The TSP point of both GFP and TFP is approximately at 0.5 V. Table 2 indicates utmost values of all analog and RF performance

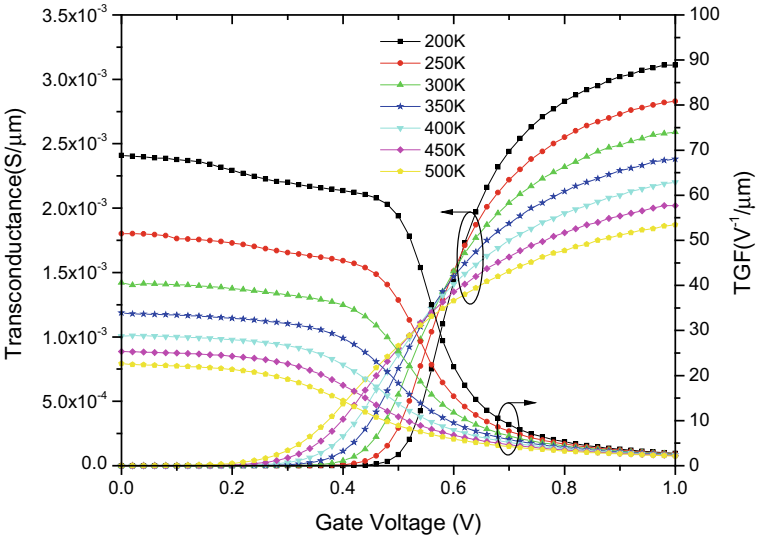

Fig. 3 g_m and TGF variation with V_{GS} with varying temperature

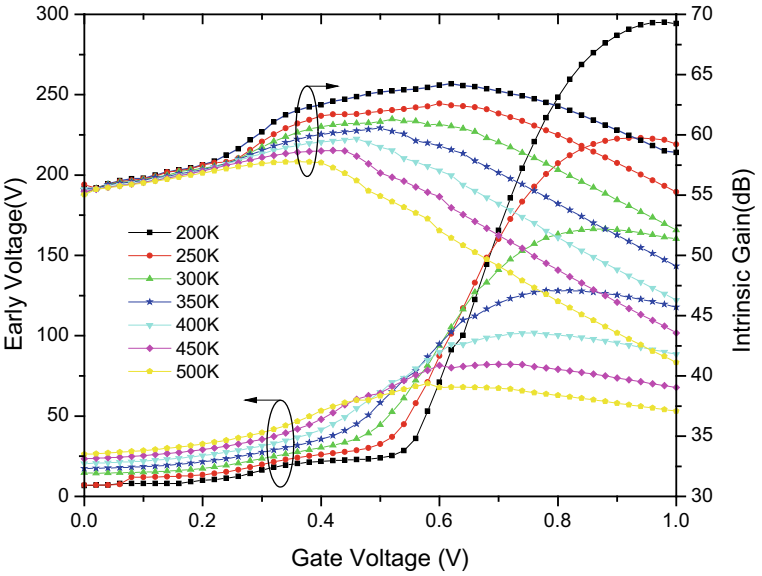

Fig. 4 V_{ea} and A_V variation with V_{GS} with varying temperature

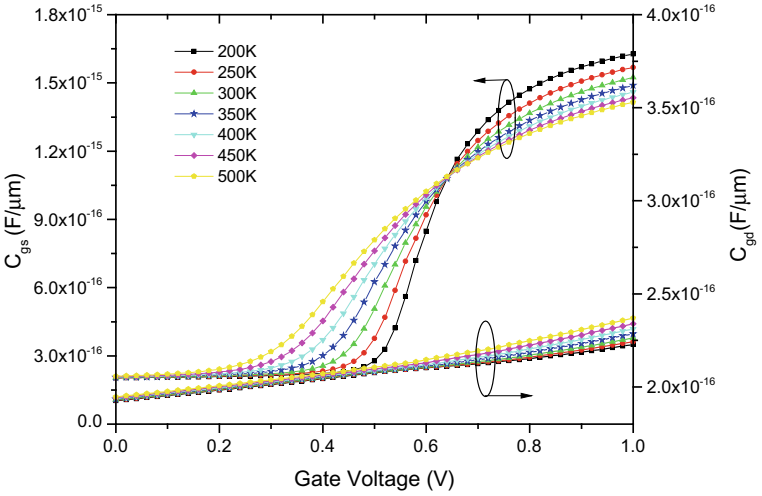

Fig. 5 C_{gs} and C_{gd} variation with V_{GS} with varying temperature

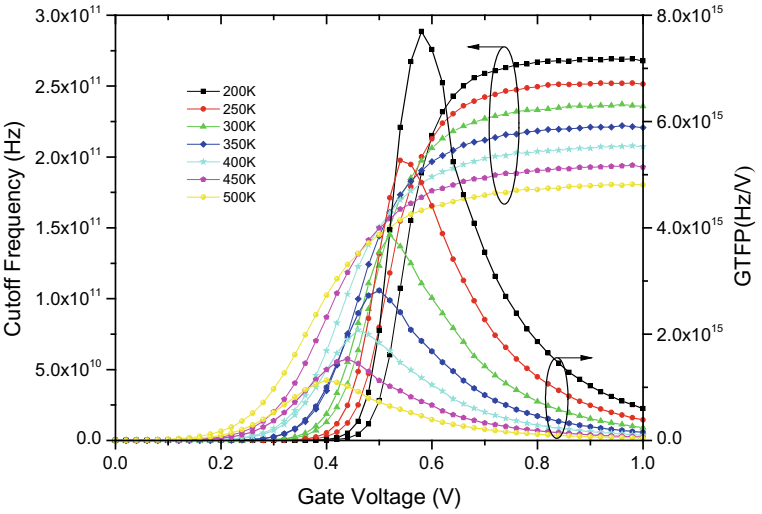

Fig. 6 F_T and GTFP variation with V_{GS} with varying temperature

parameters. It has been culminated from Table 2 that with the increase in temperature, all analog/RF performance parameter reduces.

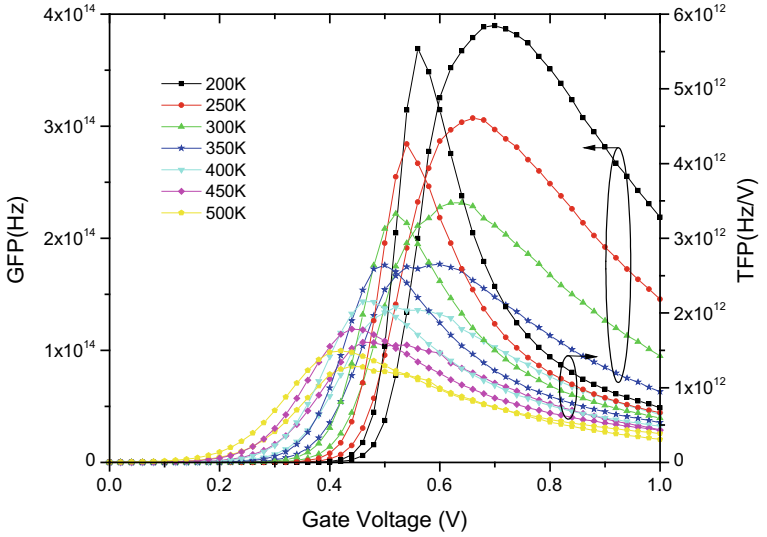

Fig. 7 GFP and TFP variation with V_{GS} with varying temperature

Table 2 Simulates analog and RF parameters at wide range of temperatures

Parameters	200 K	250 K	300 K	350 K	400 K	450 K	500 K
g_m (S/μm)	3.11×10^{-3}	2.83×10^{-3}	2.59×10^{-3}	2.38×10^{-3}	2.21×10^{-3}	2.02×10^{-3}	1.87×10^{-3}
TGF (V^{-1})	70.79	54.39	40.37	33.65	28.83	25.20	22.36
C_{gs} (F/μm)	1.62×10^{-15}	1.57×10^{-15}	1.52×10^{-15}	1.49×10^{-15}	1.46×10^{-15}	1.44×10^{-15}	1.41×10^{-15}
C_{gd} (F/μm)	2.23×10^{-16}	2.24×10^{-16}	2.26×10^{-16}	2.29×10^{-16}	2.31×10^{-16}	2.34×10^{-16}	2.37×10^{-16}
A_v (dB)	64.23	62.59	61.31	60.57	59.67	58.71	57.77
V_{EA} (V)	295.08	223.07	166.34	128.02	101.89	82.19	70.20
f_T (Hz)	2.69×10^{11}	2.52×10^{11}	2.37×10^{11}	2.22×10^{11}	2.08×10^{11}	1.94×10^{11}	1.81×10^{11}
GTFP (Hz/V)	7.69×10^{15}	5.27×10^{15}	3.87×10^{15}	2.82×10^{15}	2.08×10^{15}	1.53×10^{15}	1.13×10^{15}
GFP (Hz)	3.89×10^{14}	3.07×10^{14}	2.32×10^{14}	1.77×10^{14}	1.38×10^{14}	1.07×10^{14}	8.59×10^{13}
TFP (Hz/V)	5.53×10^{12}	4.26×10^{12}	3.33×10^{12}	2.64×10^{12}	2.16×10^{12}	1.78×10^{12}	1.49×10^{12}

4 Common Source Amplifier

In most analog and digital circuits, amplification is an essential function. Amplifiers are used to circumvent the noise of subsequent stage or to provide logic levels to digital circuits. The implementation of novel structures shows great improvement in the CMOS circuit [20–23]. This section proposes a unique attempt to investigate the drain current, output voltage and voltage gain of common source amplifier. Figure 8 shows a basic common source amplifier with diode connected load. In this configuration, the transistor T_2 is always on in saturation region as the gate and drain terminals have the same applied bias. The maximum voltage swing of this amplifier stage is V_{DD}–V_{th2} where V_{th2} is the threshold voltage of transistor T_2. The transistor T_2 has been taken from SILVACO TCAD model library such that it is having a threshold voltage of 0.2 V. The input voltage is applied to the gate terminal of proposed MOS transistor T_1 and the output is taken from the drain terminal of transistor T_1 having a load capacitance of 3fF.

Drain current variation in common source amplifier for DMDG, GCDG and GCDMDG MOSFET with input bias voltage is compared in Fig. 9. From Fig. 9, it has been observed that the drain current of an amplifier increases linearly with input bias voltage and gets saturated as the transistor T_1 enters into the saturation region of operation. Drain current of DMDG and GCDMDG is slightly low as compared to GCDG due to higher threshold voltage. GCDG is vulnerable to short channel effects due to lower threshold voltage. Figures 10 and 11 show the output voltage and gain of common source stage with input voltage, respectively. From Figs. 10 and 11, it has been observed that the GCDMDG MOSFET provides higher gain compared to DMDG and GCDG MOSFETs when used as an amplifier.

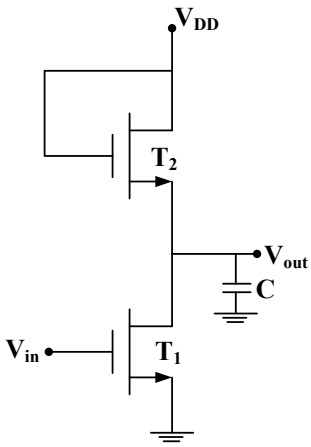

Fig. 8 Basic common source amplifier with diode connected load

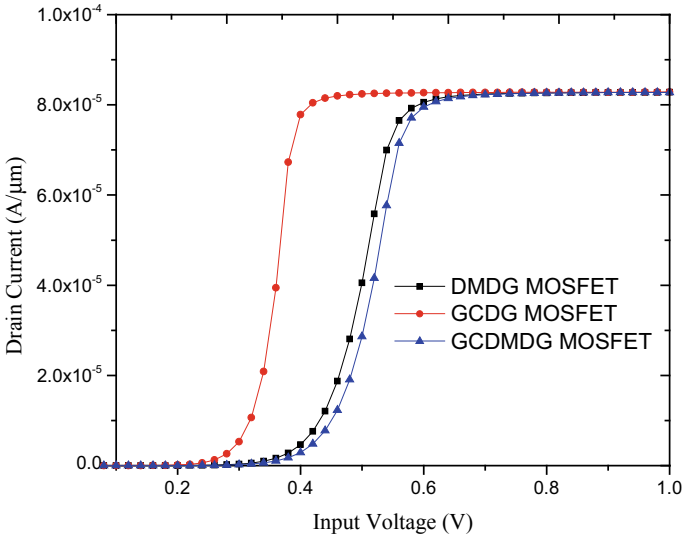

Fig. 9 I_D variation with V_{in} for DMDG, GCDG and GCDMDG MOSFETs in a common source amplifier

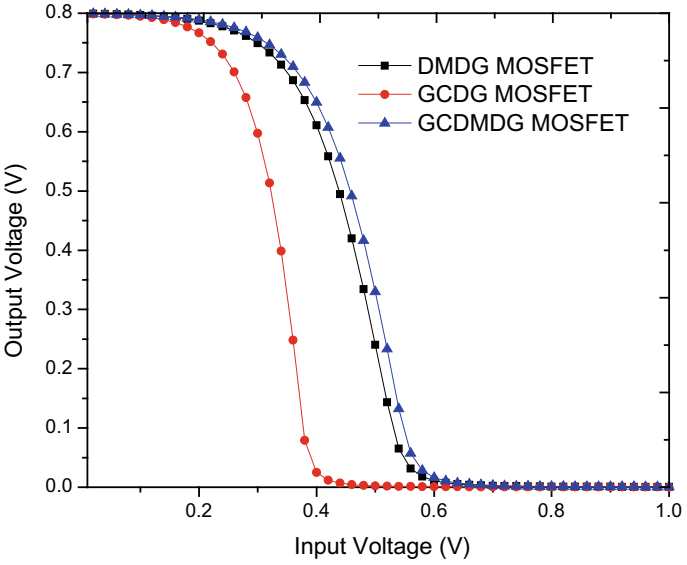

Fig. 10 Variation in V_{out} with V_{in} for DMDG, GCDG and GCDMDG MOSFETs in a common source amplifier

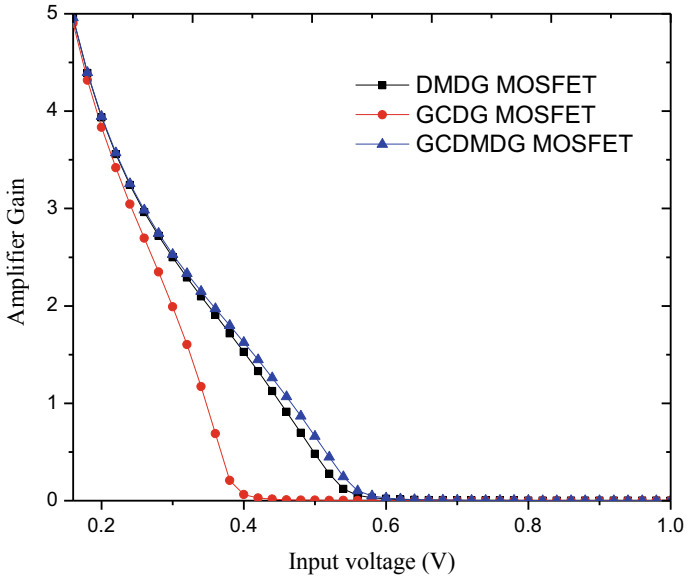

Fig. 11 Variation in voltage gain with input voltage for DMDG, GCDG and GCDMDG MOSFETs in a common source amplifier

5 Conclusion

In this paper, thermal stability of graded-channel dual-material double-gate (GCDMDG) MOSFET has been discussed in terms of analog and RF performances and simulated by 2D TCAD simulator. It has been analyzed that drain current is reversed due to change in mobility and variation in V_{th} with temperature. The reversal of both early voltage and intrinsic gain is due to mobility degradation. The value of gate to drain capacitance is negligible as compared to gate to source capacitance and increases with increasing bias voltage. RF performance parameters show better characteristics at lower temperature. Therefore, GCDMDG MOSFET has been proved to be thermally stable, and the thermal stable point for all analog/RF device parameters has been obtained in between 0.4 and 0.8 V. Further, the gate engineering of GCDMDG MOSFET with non-uniform doping profile can be analyzed and simulated. Further, common source amplifier has been analyzed using this device. GCDMDG MOSFET provides higher amplification gain, compared to GCDG and DMDG MOSFETs, when used as a common source amplifier.

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Data and Bandwidth Analysis of CAN Bus in a System Using MATLAB

P. Anirvinnan and B. S. Premananda

1 Introduction

CAN bus is a serial data communication protocol which was invented in the year 1986 by German BOSCH Corporation [1]. This was initially designed for car industry which later on was developed for all vehicular standards. Data frames which have sizes up to 8 bytes are supported by CAN. A 15-bit CRC is linked with a large overhead possessed by the CAN protocol which makes it more secure and dependable [2]. This protocol uses the technique of carrier sense multiple access/collision avoidance (CSMA/CA). Since the communication rate is dependent on the distance between the nodes, a rate up to 40 Mbps is achievable only when the distance is less than 40 m. Some of the CAN bus protocol properties include message prioritization, latency time guarantee, flexible configuration, time synchronization during multicast reception, data consistency, multi-master communication, detection of error and signalling, retransmission of corrupted messages automatically as soon as the bus is idle again and distinction between permanent failures and temporary errors of nodes [3].

Nodes are nothing but different units. In other forms of different networks such as USB, the messages are shared in CAN bus to entire network such that every node has consistent data [4]. There are two CAN bus specifications, namely 11-bit identifier and 29-bit identifier. Several mechanisms are used to detect errors in CAN such as Cyclic Redundancy Check (CRC), verifying transmitted bit levels, frame format and bit encoding and acknowledgement scheme. A highly reliable network is guaranteed by these error detections, but also they make a little difficult to quantify this reliability. CAN is a vehicle bus standard protocol which is specifically designed for automotive application. A hardware and software design of CAN bus is shown in [2]. The actual ECU node of vehicle system is usually adapted with CAN bus system

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design. CAN bus has been used widely in in-vehicle networks which increase the demand of data rates.

In-vehicle network uses CAN protocol predominantly. Therefore, the data rate demand has increased sharply which delimits the normal CAN communication leading to limited bandwidth. A method has been proposed in [1] to increase the bandwidth of the channel by using pass band communication system. As the CAN communication system has robustness to errors and efficiency of control signal inside the vehicles, the CAN has been adopted for in-vehicle networking.

A CAN flexible data rate is discussed in [5] where the author presents the CAN format that improves the data rate of CAN from 1 Mbps to 2.5 Mbps by adding extra bits in the control field to enable the CRC sequence to secure longer frames. To improve the CAN communication dependability, a research on online fault diagnosis is performed in [6]. One of the bandwidth allocation schemes is proposed in [7] where the algorithm not only satisfies the requirement in performances of real-time system but also utilizes the bandwidth fully.

The paper discusses about the data format and transmission of data in CAN bus. Section 2 describes the detail of a CAN bus node. CAN data format is discussed in Sect. 3. The amount of data transmitted in a particular system is calculated and analysed for a period of time in Sect. 4. Obtained results are discussed in Sect. 5. The conclusion derived is discussed in Sect. 6.

2 CAN Bus Node

A CAN bus node requires a microprocessor or host processor and a Central Processing Unit which decides what the messages that are received means and what messages are needed to be transmitted. Figure 1 shows a basic CAN node. The host processor is connected to devices such as actuators, control devices and sensors. The next important part in the node is Controller Area Network (CAN) controller. In the receiving side, the CAN controller stores the received signal bits of the message that is available in the bus. Triggering an interrupt by the host ensures the fetching of the messages. On the sending side, the host processor sends the transmit messages to CAN controller which when the bus is free transmits the bits serially. After the CAN controller, the next part is the CAN transceiver. As the name suggests, it transmits and receives data.

The stream of data from the CAN bus levels is converted by the CAN controller which is transmitted to the levels that it can use on the receiver side. There is a defensive circuitry present to shield the CAN controller. The stream from the CAN controller is converted by the trans receiver to CAN bus levels that are on the transmitting side. The nodes in the CAN bus send and receive messages, but the process is not simultaneous. The message comprises of the ID which decides the significance of the message.

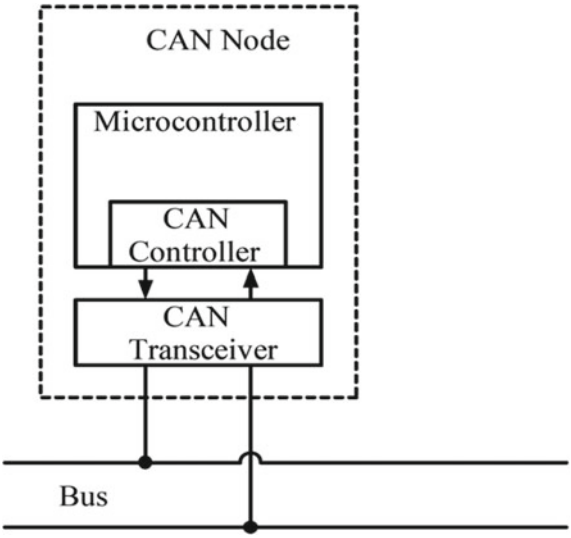


Fig. 1 CAN bus node

3 Data Format of CAN Bus

The message in the CAN bus is transmitted serially using a non-return-to-zero (NRZ) format. It uses the term "dominant" bits for a logical '0' where the transmitter dives the signal actively to a voltage and the term "recessive" bits for logical '1' where the resistor passively returns a signal to a voltage. The representation of the CAN signal is shown in Fig. 2. When a dominant bit is transmitted by the one node and a

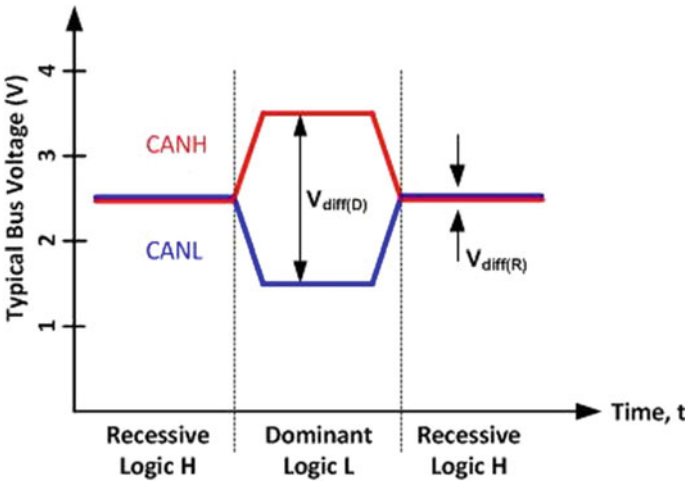


Fig. 2 CAN bus signal

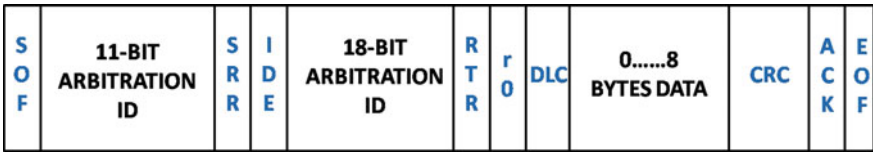


Fig. 3 CAN bus data frame

recessive bit is transmitted by another at the same time, the node with the dominant bit wins over the other node during their collision. This makes sure that there is only transmission of highest priority message whit no delay. The lower priority message transmitting node now tries to retransmit the same message after a six-bit clock from the time the dominant message is transmitted. As the CAN protocol uses multi-master, the transmitted signal is viewed by all the receivers and the receivers accept the data if it belongs to it. Therefore, when all the nodes transmit only dominant bits or only recessive bits, logical '0' or '1' is seen by all the nodes including the transmitting node, whereas all the nodes end up seeing logical '0' irrespective of being logical '1' when multiple nodes transmit dominant bits and multiple nodes transmit recessive bits.

A CAN bus has four frame types, namely overload frame, data frame, remote frame and error frame. The destination node can request the data from the source using a remote frame. The remote frame does not have any data in it. The error frame is used to detect any error in the message [8]. CAN bus performs five levels of error detection, namely frame checks, cyclic redundancy checks, acknowledgement checks at message level, stuffing and monitoring at bit level.

When an error is found during the transmission of the message, the nodes will immediately abort the transmission and broadcast the error frame. When the messages are received faster than it can be processed by the CAN node, the overload frame gets generated. When this frame is activated, an extra time is provided for the successive bits. The actual data are sent through the data frame which is shown in Fig. 3 which contains two message formats, namely base frame format with eleven identifier bits and extended frame format with twenty-nine identifier bits.

The frame format for the CAN bus is as follows:

- SOF indicates Start of Frame
- Identifier states the content of message and priority
- IDE—Identifier extension which distinguishes between CAN standard, CAN extended 29-bit identifier and a 11-bit identifier.
- RTR means Remote Transmission Request
- DLC is the Data Length Code
- Data mainly hold up to 8 bytes of data
- ACK is Acknowledge
- CRC stands for Cyclic Redundant Check
- EOF indicates End of Frame

- IFS—Intermission Frame Space, is the minimum number of bits separating messages.

4 Data Analysis in CAN Bus

The CAN bus is implemented in MATLAB 2016b, and communication toolbox was used. A 128-bits frame of CAN with the bus speed of 250 Kbps was chosen to analyse the bus. The total amount of data is analysed and tabulated, and the bandwidth consumption of the bus is performed. A system which needs CAN bus to transmit data is taken, and total amount of data is analysed in this section.

The amount of data that are transmitted in the bus have to be known. The amount of data helps in indicating the maximum amount of bus bandwidth, memory space and processing power that is necessary to maintain the system without loss of data. The amount of data is calculated and tabulated for the bandwidth analysis.

The headings in the tables are as follows:

- Data from Source to Destination—Tells the type of device that is sending the data.
- Number of Instances
- Data Size (bits)
- Total data instance amount (TDIA) with respect to bits is derived using Eq. (1)

$$\text{TDIA} = \text{Number of instances} \times \text{Data size} \tag{1}$$

- Data Repetition Rate (ms)
- Average loading (AL) of data in Kbps is calculated using Eq. (2)

$$\text{AL} = \frac{\frac{1000}{\text{Data Repetition Rate (ms)}} \times \text{TDIA (bits)}}{1000} \tag{2}$$

Table 1 shows an example of amount of data calculated for the communication of

Table 1 Data analysis in CAN bus

Message ID	Number of data instances	Data size (bits)	Total data instance (bits)	Data repetition rate (ms)	Average loading (Kbps)	Bytes
100	32	1	32	10	3.2	4
150	22	1	22	500	0.044	3
200	22	1	22	100	0.22	3
250	3	16	48	10	4.8	6
300	21	1	21	10	2.1	3
350	64	1	64	500	0.128	8
400	64	1	64	100	0.64	8

a system that uses CAN Bus. The formulas discussed is used to calculate the amount of data and the amount of average loading in Kbps. Maximum size of the data is only 8 bytes, and the total amount of bits is 273. With the repetition rates for each message, the total average loading in the bus is 11.132 Kbps. A MATLAB program is written for the bandwidth analysis for the amount of data that are sent from the system. A virtual channel is created, and the data are sent through. CAN function is used to transmit and receive data through the created virtual channel. The bus speed used in the CAN node is 250 Kbps which is chosen for the program. Each message is given an ID, and according to the amount of data the payload in bytes is given as the CAN message.

Figure 4 shows the number of messages, CAN ID and the payload in bytes which are the inputs provided to the CAN bus. Figure 5 illustrates the period for which the

```
Enter the number of messages : 7
Enter the CAN ID for message 1 : 100
Enter the amount of payload in Bytes for message 1 : 4
Enter the CAN ID for message 2 : 150
Enter the amount of payload in Bytes for message 2 : 3
Enter the CAN ID for message 3 : 200
Enter the amount of payload in Bytes for message 3 : 3
Enter the CAN ID for message 4 : 250
Enter the amount of payload in Bytes for message 4 : 6
Enter the CAN ID for message 5 : 300
Enter the amount of payload in Bytes for message 5 : 3
Enter the CAN ID for message 6 : 350
Enter the amount of payload in Bytes for message 6 : 8
Enter the CAN ID for message 7 : 400
Enter the amount of payload in Bytes for message 7 : 8
```

Fig. 4 Input of messages for the CAN Bus in MATLAB

```
Enter the period (secs) for Message 1 to repeat : .01
Enter the period (secs) for Message 2 to repeat : .5
Enter the period (secs) for Message 3 to repeat : .1
Enter the period (secs) for Message 4 to repeat : .01
Enter the period (secs) for Message 5 to repeat : .01
Enter the period (secs) for Message 6 to repeat : .5
Enter the period (secs) for Message 7 to repeat : .1
```

Fig. 5 Input of periods for the messages to repeat

messages must be repeated in the CAN bus. The bandwidth is found with the total amount of data and the time for which the data are sent.

5 Results and Discussion

CAN protocol is implemented in MATLAB where the bus speed is 250 Kbps and the channels for transmitting and receiving data were created as virtual channel. The bandwidth was found by using the length of all the payload and total number of messages of each CAN IDs. The payload for the CAN bus is decided using the number of messages in Table 1. The bandwidth of the bus was analysed for a period of 5 s. Figure 6 describes the details of the transmitter and the receiver channel of the CAN bus where it can be analysed that the bus speed is 250 Kbps. The total number of messages transmitted and received is same which infers that there is no loss of data. The channel used is a virtual channel named 'Virtual 1' as shown in Fig. 7 through which the data are transmitted and received.

Figure 7 illustrates the graph of message transmission for a period of 5 s. The graph also indicates that the messages with the IDs 100, 250 and 300 repeat at a very little interval of time, whereas messages with IDs 150 and 350 repeat for a longer time interval. The messages with less time interval mean that the data are needed very often due to more criticality, whereas the messages with more time interval mean that the data are required less often.

Figure 8 shows the bandwidth utilization of the CAN bus for the data in Table 1. It can be inferred from the pie chart that only 16.3504% of the entire bus is used which is 40.876 Kbps.

6 Conclusion

The CAN protocol is discussed, and a method is proposed to find the bandwidth utilization of the CAN bus in a system using MATLAB simulation. The CAN node is discussed, and the total data needed to communicate through data bus are calculated. The data are sent as payload in CAN bus depending upon the number of bits each CAN ID is transmitting. With the repetitions of messages for each CAN ID, the bandwidth of the data bus is found by considering the total amount of data that are sent. The transmitted data are expressed in a form of graph with different CAN IDs. For the system considered, the bandwidth utilization was only 16.35% of the entire bus which is 40.876 Kbps.

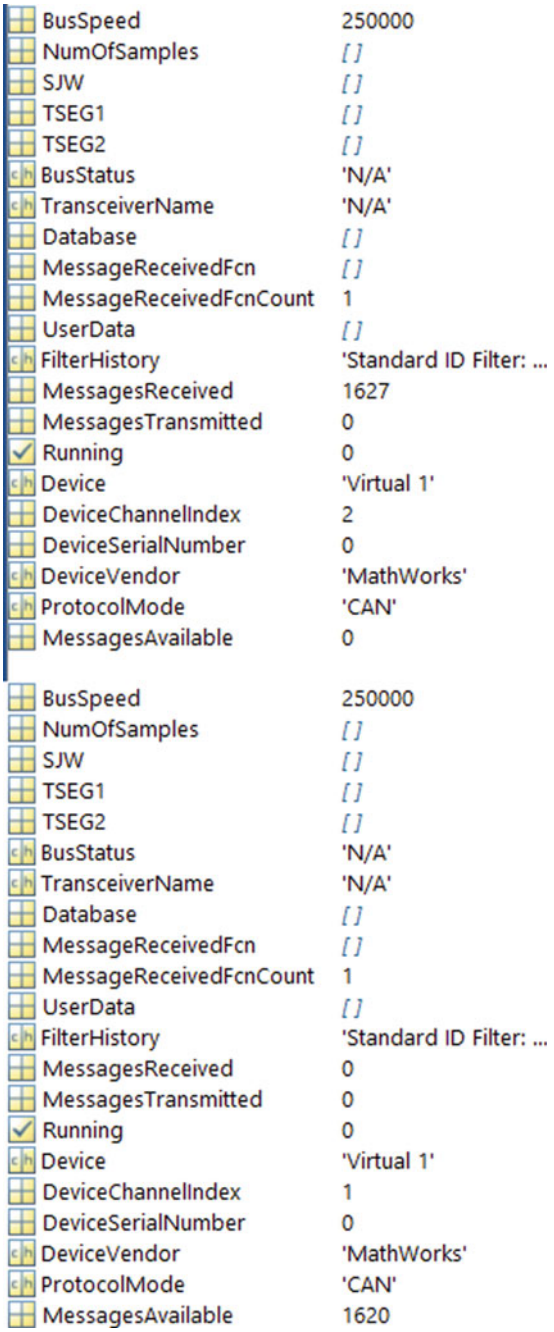


Fig. 6 Transmitter and receiver channel of CAN Bus

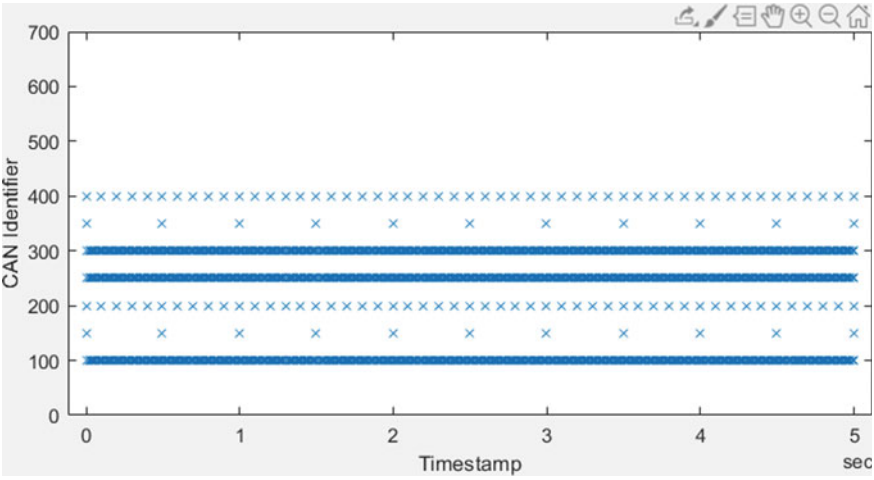
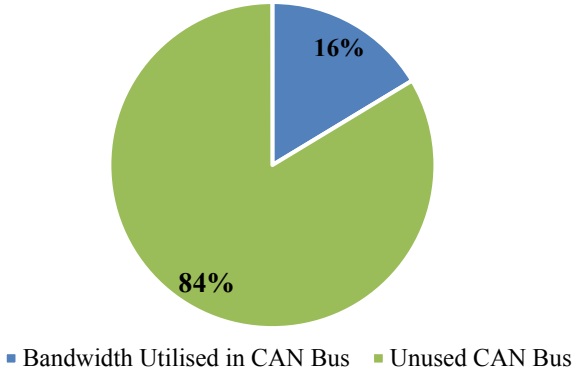


Fig. 7 Output graph of payload sent in CAN bus

Fig. 8 Bandwidth utilization of CAN bus



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DV-EXCCCII-Based Electronically Tunable Current Mode Filter

Priyanka Singh, Vikrant Varshney, Ankur Kumar, and Rajendra Kumar Nagaria

1 Introduction

Since several decades, current mode became an important and more efficient approach to design an analog circuit. Analog circuit designed using current mode technique results in high-performance circuit with high slew rate, greater linearity, simple circuit design, low power consumption and large bandwidth in comparison with its voltage mode counterparts. Filter is an important circuit element in many analog signal applications. Among all the filters, the first-order filter has application in video, audio, communication, instrumentation and many other areas where low power and simple circuitry are priority. The first-order universal filter is a circuit which is able to realize first-order low-pass (LP), high-pass (HP) and all-pass (AP) filters. Several first-order filters are reported in the literature employing operational amplifier [1, 2]. Due to potential advantages of current mode (CM) approach over voltage mode (VM), researcher's attention shifted toward CM technique. Previously, a lot of first-order universal filters employing current mode active blocks are discussed in the literature. Some of the most discussed active analog blocks are CCI [3], CCII [4–6], DDCC [7], DVCC [8–11], DX-MOCCII [12, 13], DO-CCII [14], CDTA [15], CCCCTA [16], MOCCII [17], COA [18], CFOA [19], CFA [20], ICCII [21], DXCCII

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[22], and many more. Previously discussed filter in the literature using these active blocks suffers from either of these limitations:

- Use of more no of analog blocks
- More no of passive elements are needed
- Use of floating passive component
- Matching is required
- Not electronically tunable
- Does not realize all three filter functions
- Does not produce all three filter at single-output terminal.

The proposed universal filter employs single active block, i.e., DV-EXCCCII [23] which simplifies filter circuit configuration and one capacitor which is grounded making it easy for IC implementation. This configuration is able to realize LP, HP and AP filters at a single terminal using proper input combination. DV-EXCCCII is an electronically tunable block so filter response can be electronically varied with bias current of DV-EXCCCII. To implement all the three filters, any kind of matching constraints is not required.

Organization of the paper is given as follows: Brief introduction of the work is presented in Sect. 1. In Sect. 2, the proposed first-order filter with mathematical analysis is given. Non-deal analysis of the filter and sensitivities due to these non-idealities are also discussed in this section. Comparison of proposed work with previously available filters is given in Sect. 3. Section 4 of the paper provides simulation results of the proposed filter. In Sect. 5, paper is concluded.

2 Circuit Description and Analysis

2.1 Circuit Implementation

Block diagram of DV-EXCCCII is shown in Fig. 1, and its CMOS implementation is represented in Fig. 2.

Relationship of input and output signals can be expressed by matrix given below:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_{X1} \\ V_{X2} \\ I_{Z1\pm} \\ I_{Z2\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & R_{X1} & 0 & 0 & 0 \\ 1 & -1 & 0 & R_{X2} & 0 & 0 \\ 0 & 0 & \pm 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_{X1} \\ I_{X2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix} \tag{1}$$

where R_{x1} and R_{x2} are the internal resistance of current terminals X_1 and X_2, respectively. This resistance depends on the bias current I_0 and can be expressed as:

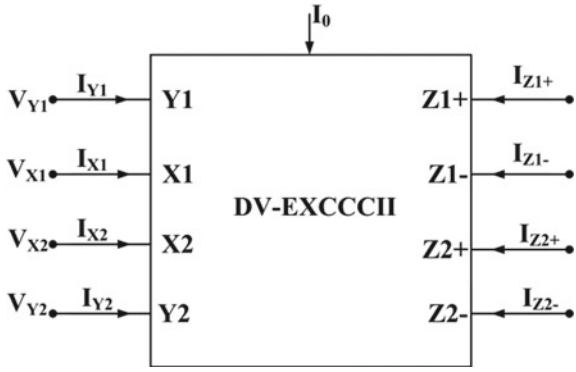

Fig. 1 Symbol of DV-EXCCCII

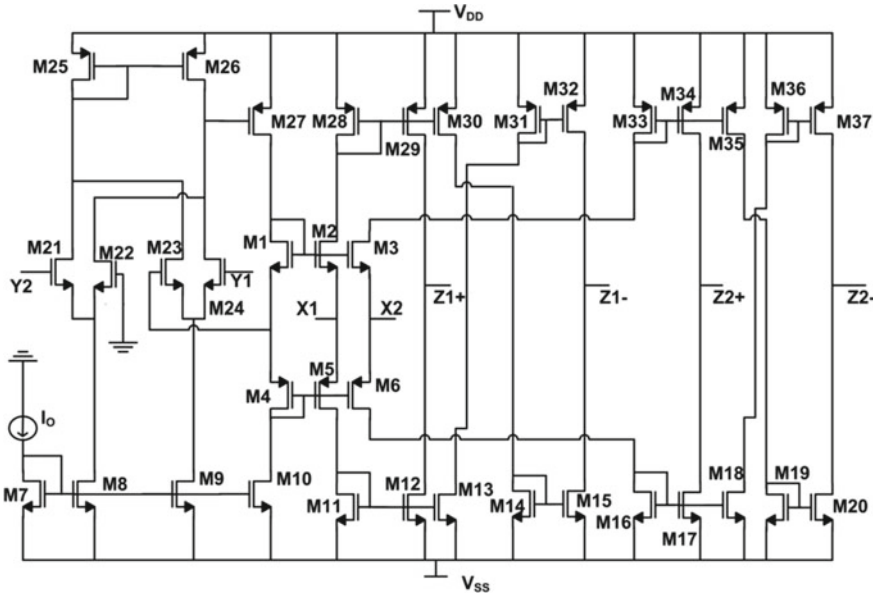

Fig. 2 CMOS representation of DV-EXCCCII

$$R_{X1} = R_{X2} = R_X = \frac{1}{\sqrt{8\mu C_{0X}\left(\frac{W}{L}\right) I_o}} \tag{2}$$

where μ is mobility of the charge carrier, C_{0x} is the oxide capacitance, W/L is the aspect ratio, and I_o is the bias current of active block.

This active block has two current terminals (X_1, X_2) and two voltage terminals (Y_1, Y_2). Current terminals are low input impedance terminals, and voltage terminals are high input impedance terminals. All the output terminals (Z) of the block are high output impedance current terminals. Plus sign (+) shows that currents of X and Z

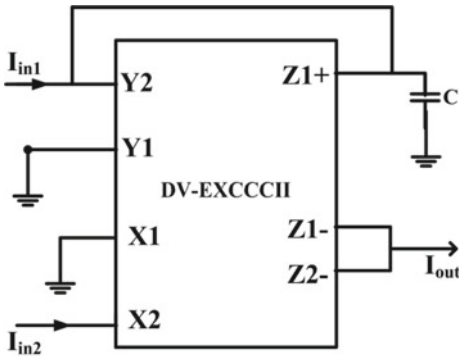

Fig. 3 Proposed filter configuration

terminals are in the same phase and minus sign (−) shows that they are in opposite phase. As application demands, many number of Z terminals can be created.

The proposed filter configuration employing DV-EXCCCII is depicted in Fig. 3. Two input current signals I_{in1} and I_{in2} and one grounded capacitor are used to design this filter. By taking proper input combination LP, HP and AP filters are obtained at single-output terminal I_{out} without considering any matching condition. The proposed filter is electronically tunable with bias current I_0.

Some intermediate expressions are written as:

$$V_{Y2} = \frac{I_{\text{in1}} - I_{Z1+}}{sC} \tag{3}$$

$$I_{X1} R_X = \frac{I_{\text{in1}} - I_{Z1+}}{sC} \tag{4}$$

Output current of the proposed filter is obtained as:

$$I_{\text{out}} = I_{Z1-} + I_{Z2-} \tag{5}$$

$$I_{\text{out}} = \frac{I_{\text{in1}} + I_{\text{in2}}(1 + sR_XC)}{1 + sR_XC} \tag{6}$$

From the above expression, LP, HP and AP filters can be obtained by taking required input. These input combinations are given in Table 1.

Transfer function obtained in Table 1 shows that no matching is required to realize these filters.

Pole frequency is observed as:

$$f_o = \frac{1}{2\pi R_X C} \tag{7}$$

Phase of all-pass filter can be derived as:

Table 1 Input required for the proposed filter

Response	Input		Transfer function
	I_{in1}	I_{in2}	
Low pass	I_{in}	0	$\frac{I_{out}}{I_{in}} = \frac{1}{1+sR_XC}$
High pass	$-I_{in}$	I_{in}	$\frac{I_{out}}{I_{in}} = \frac{sR_XC}{1+sR_XC}$
All pass	$2I_{in}$	$-I_{in}$	$\frac{I_{out}}{I_{in}} = \frac{1-sR_XC}{1+sR_XC}$

$$\phi = -2\tan^{-1}(\omega R_X C) \tag{8}$$

2.2 Non-ideal Analysis

In this section, non-ideal behavior of circuit is explained. Taking nonidealities of DV-EXCCCII into consideration, terminal relationship of the active block is modified as:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_{X1} \\ V_{X2} \\ I_{Z1\pm} \\ I_{Z2\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0\ 0 \\ 0 & 0 & 0 & 0 & 0\ 0 \\ \beta_{11} & -\beta_{12} & R_{X1} & 0 & 0\ 0 \\ \beta_{21} & -\beta_{22} & 0 & R_{X2} & 0\ 0 \\ 0 & 0 & \pm\alpha_{1\pm} & 0 & 0\ 0 \\ 0 & 0 & 0 & \pm\alpha_{2\pm} & 0\ 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_{X1} \\ I_{X2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix} \tag{9}$$

where β_{11}, β_{12}, β_{21}, β_{22} are the voltage transfer errors and $\alpha_{1\pm}$, $\alpha_{2\pm}$ are the current transfer errors. Reanalysis of the filter circuit shown in Fig. 3 results in the following expressions:

$$I_{out} = \frac{\alpha_{1-}\beta_{12}I_{in1} + \alpha_{2-}I_{in2}(\beta_{12}\alpha_{1+} + sR_XC)}{\beta_{12}\alpha_{1+} + sR_XC} \tag{10}$$

$$\text{Low pass}: \ I_{out} = \frac{\alpha_{1-}\beta_{12}I_{in1}}{\beta_{12}\alpha_{1+} + sR_XC} \tag{11}$$

$$\text{High pass}: \ I_{out} = \frac{-\alpha_{1-}\beta_{12} + \alpha_{2-}I_{in2}(\beta_{12}\alpha_{1+} + sR_XC)}{\beta_{12}\alpha_{1+} + sR_XC} \tag{12}$$

$$\text{All Pass}: \ I_{out} = \frac{2\alpha_{1-}\beta_{12} - \alpha_{2-}(\beta_{12}\alpha_{1+} + sR_XC)}{\beta_{12}\alpha_{1+} + sR_XC} \tag{13}$$

Pole frequency will now become:

$$f_0 = \frac{\beta_{12}\alpha_{1+}}{2\pi R_X C} \tag{14}$$

Sensitivity of pole frequency caused by non-ideality and by passive components can be derived as:

$$S_C^{f_0} = S_{R_X}^{f_0} = -1; \quad S_{\beta_{12}}^{f_0} = S_{\alpha_{1+}}^{f_0} = 1; \tag{15}$$

$$S_{\alpha_{1-}}^{f_0} = S_{\alpha_{2+}}^{f_0} = S_{\alpha_{2-}}^{f_0} = S_{\beta_{11}}^{f_0} = S_{\beta_{21}}^{f_0} = S_{\beta_{22}}^{f_0} = 0 \tag{16}$$

It can be observed from (15) and (16) that sensitivities caused by non-idealities are low.

3 Comparative Research

In the literature, several high-performance active blocks based on current mode technique are discussed. A number of filters are discussed in the previous work using these high-performance active elements. Proposed first employing DV-EXCCCII is compared with available first-order filters in the literature. Filters discussed in [14–17] use more than one active element, and some filters [10–12, 14, 17, 18] use more passive elements due to which circuit become complex. In the filters given in [14, 15, 18], passive components used are not grounded due to which circuit become less suitable for IC implementation. Electronic tuning property is missing in filters discussed in [10–12, 14, 17, 18]. Matching of components is required to realize filter function [12]. Filters specified in [10, 11, 15, 16, 18] do not realize all three filters of first order.

The proposed first-order filter uses one DV-EXCCCII and single grounded capacitor to obtain LP, HP and AP filters at single-output terminal without any matching condition. This filter configuration is electronically tunable due to which frequency of the filter may be varied with bias current of the DV-EXCCCII. Comparison of the proposed filter with the already available first-order filters is summarized in Table 2.

4 Simulation Results

The proposed filter design configuration using DV-EXCCCII is implemented in CADENCE Virtuoso, and responses are verified using UMC 180 nm CMOS technology process parameters. Supply voltage $V_{DD} = -V_{SS} = 0.9$ V is used for simulation. To verify filter response, bias current of active block $I_0 = 100\ \mu$A and capacitor value $C = 50$ pF are taken. Intrinsic impedance of the filter at current terminals is observed as $R_{X1} = R_{X2} = 813\ \Omega$. Using these values, pole frequency of the filter

Table 2 Comparative study of the proposed filter

References	Number, type of block	# Passive elements	Grounded passive elements	Electronic tuning	Component matching	Universal
[10]	1, DVCC	2	Yes	No	No	No
[11]	1, DVCC	2	Yes	No	No	No
[12]	1, DX-MOCCII	4	Yes	No	Yes	Yes
[14]	2, DOCCII	2	No	No	No	Yes
[15]	2, CDTA	1	No	Yes	No	No
[16]	2, CCCCTA	1	Yes	Yes	No	No
[17]	2, MOCCII	2	Yes	No	No	Yes
[18]	1, COA	2	No	No	No	No
Proposed work	1, DV-EXCCCII	1	Yes	Yes	No	Yes

$f_0 = 3.9$ MHz is found. Figure 4 shows magnitude response for LP and HP filter. Figure 5 represents magnitude and phase variation of APF, and it can be observed that phase varies from 0° to 180°.

The proposed universal filter is electronically tunable with bias current of DV-EXCCCII. To represent tunable characteristics of the filter, different values of bias currents (30, 50, 100 μA) are assumed. Figure 6 represents magnitude response of LPF at different bias currents, and its pole frequency is obtained as 2.8 MHz, 3.2 MHz and 3.91 MHz at bias current of 30 μA, 50 μA and 100 μA, respectively. Figure 7 shows tunable property of HPF, and pole frequencies 2.6 MHz, 2.98 MHz and 3.87 MHz are obtained at 30 μA, 50 μA and 100 μA, respectively. Figure 8

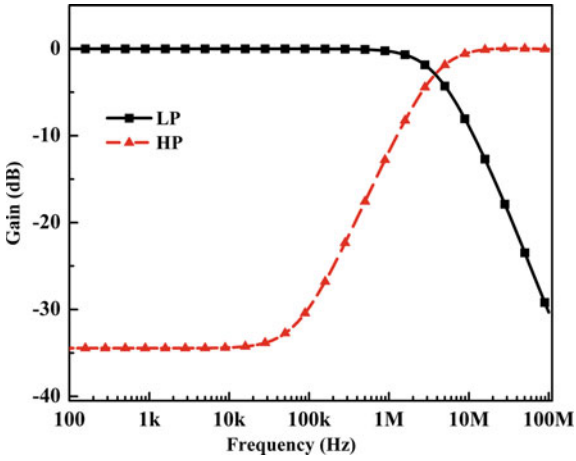

Fig. 4 Magnitude response for the first-order LP and HP filter

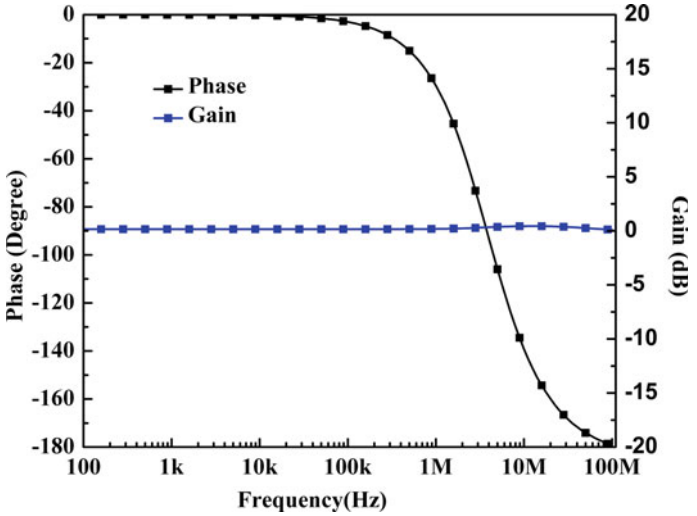

Fig. 5 Magnitude and phase response for AP filter

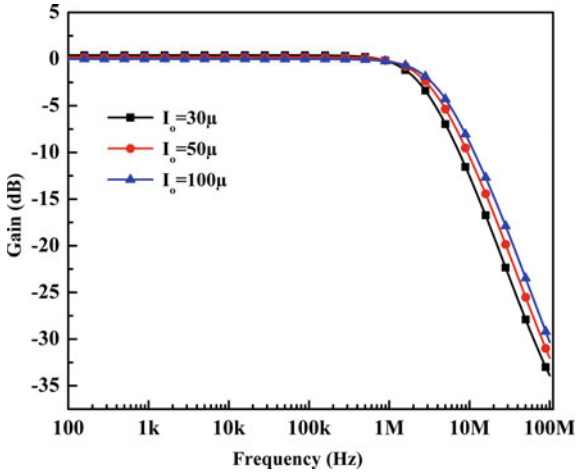

Fig. 6 Frequency response of LP at different bias currents

shows phase response of APF with frequency 2.5 MHz, 3.1 MHz and 3.92 MHz at bias current of 30 µA, 50 µA and 100 µA, respectively.

Impact of small supply voltage variation is shown by LPF gain response in Fig. 9. Frequency of LPF is 4.2 MHz, 3.91 MHz and 3.56 MHz at supply $V_{DD} = -V_{SS} =$ 0.95 V, 0.9 V and 0.85 V, respectively. Temperature variation effect on filter is shown in Fig. 10 with LPF magnitude response at different temperatures. Pole frequency of LPF 4.3 MHz, 3.98 MHz and 3.76 MHz is obtained at temperature −50 °C, 0 °C and 50 °C, respectively.

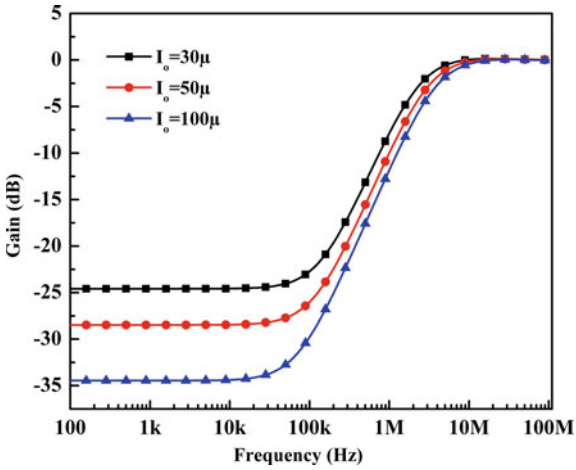

Fig. 7 Frequency response of HP at different bias currents

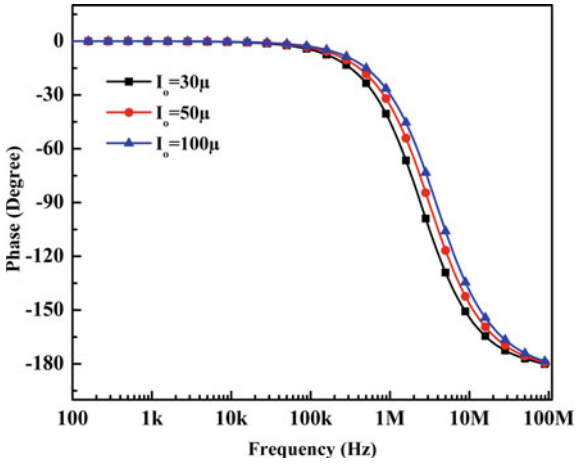

Fig. 8 Phase variation of AP at different bias currents

5 Conclusion

The first-order universal filter employing a new analog block DV-EXCCCII is proposed. Filter circuit uses one analog block and single grounded capacitor making it easy for IC implementation. This filter can realize all three filters LP, HP and AP at single-output terminal by proper choice of input combination without considering any matching constraints. This configuration is electronically tunable, and its response can be varied with bias current of the active block. Nonideal behavior is explained, and sensitivities due to these non-idealities are found to be low. Filter results are verified by simulation which confirms theoretical analysis.

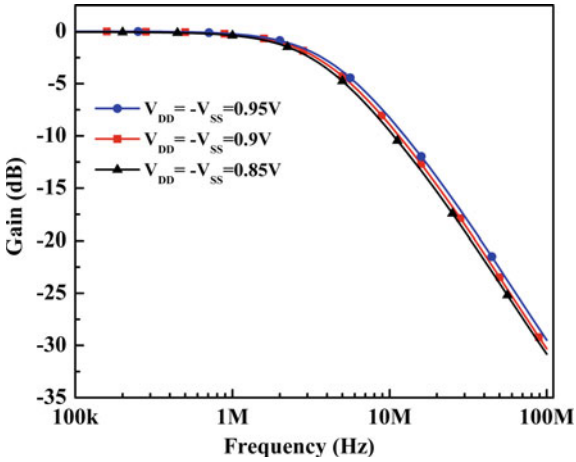

Fig. 9 Magnitude response for LP filter at different supply voltages

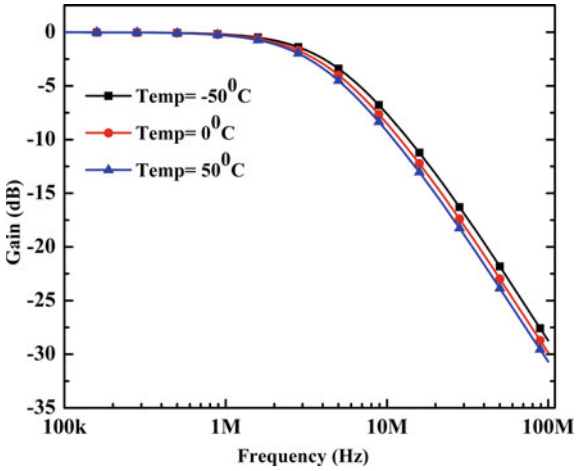

Fig. 10 Magnitude response for Lp filter at different temperatures

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Non-destructive Quality Estimation of Packaged Ceramic Tiles Using Millimeter Wave Imaging Radar

Smriti Agarwal and Dharmendra Singh

1 Introduction

Millimeter wave (MMW) frequency offers many interesting applications in different diverse and fundamental application areas viz., security screening, industrial quality monitoring, medical imaging, etc. [1–5]. In contrast to existing EM-based imaging modalities, it provides much better resolution, penetration to opaque objects and has no health hazards [6, 7]. Recently, applicability of MMW imaging for non-destructive testing and estimation applications has been gaining attention of researchers, for example, use of one dimensional imaging array at 30 GHz for embedded defect detection [8], localized anomalies detection in space shuttle at 33.5, 70 or 100 GHz [9], estimation of fatigue cracks at 24 GHz, 90 GHz using rectangular waveguide probes [10, 11], monitoring of moisture and disinfestation of sculptures [12], finding corrosion under paint at Ka and V band [12]. Millimeter wave radar system provides a non-invasive, simple and precise scrutiny technique instead of currently employed time-consuming and monotonous manual surveying method. In this paper, a MMW radar system-based imaging methodology has been recommended to identify and classify packaged ceramic tiles as cracked/non-cracked for real time industrial quality monitoring applications. The underline novelty of the paper is that it is newest of its kind to establish the capability of MMW radar for non-destructive testing for quality monitoring for industrial applications. The challenging aspect of MMW imaging is to extract relevant and unique features from low resolution radar images in contrast to

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camera images. Additionally, reflected target signals suffer from higher path loss and noise from surroundings. Rest of the paper is partitioned as follows: Sect. 2 describes setup used for MMW radar, Sect. 3 discusses methodology used for undercover fault detection, and Sect. 4 covers result and discussion. Lastly, Sect. 5 provides conclusion.

2 Millimeter Wave Imaging Radar System Design

2.1 Experiment Arrangement

A V band MMW imaging radar system has been indigenously designed at Microwave Imaging and Space Technology Applications Laboratory (*MISTA*) research lab, Department of ECE at Indian Institute of Technology Roorkee, India [13]. The EM wave is transmitted in stepped frequency continuous wave (SFCW) mode having bandwidth of 2 GHz around 60 GHz center frequency. The monostatic V band horn antenna transmits signal at the distant target mounted on a 2D wooden scanner placed at a certain distance of $R = 0.5$ m. The scanning frame was designed such that it facilitates full vertical and horizontal movement of the target in successive steps of 2 cm. The complete target data acquisition (A-scan, B-scan, C-scan) has been achieved by 18 vertical and 30 horizontal scanning locations with 201 frequency points in downrange. The image resolution characteristics of the designed radar are;

$$\text{Range resolution} = \Delta R = \frac{C}{2N\Delta f} = 7.5 \text{ cm} \tag{1}$$

$$\text{Cross - range resolution } \Delta\text{CR} = \frac{\lambda R}{D} = 4.17 \text{ mm} \tag{2}$$

Here, D is the synthetic aperture of V band horn antenna due to target's lateral movement i.e., $0.02 \text{ m} \times 30 = 0.60$ m.

2.2 Concealed Target Fault Detection Application

Target arrangement for non-destructive concealed fault detection has been shown in Fig. 1. It consists of a large wooden sheet (35 cm $\times$ 43.6 cm) on which a thick polystyrene sheet was placed in order to suppress any background reflection. On this polystyrene sheet, test target i.e., commonly available ceramic tile with varying crack/no-crack configurations was placed. Further, in order to mimic concealed packaged good, the respective tiles were covered with packaging cardboard in view of practical industrial NDT applications. Total 10 non-faulty (zero crack) tiles and 16 faulty tiles (cracked tiles) were taken. Out of 16 faulty tiles, four tiles for each possible

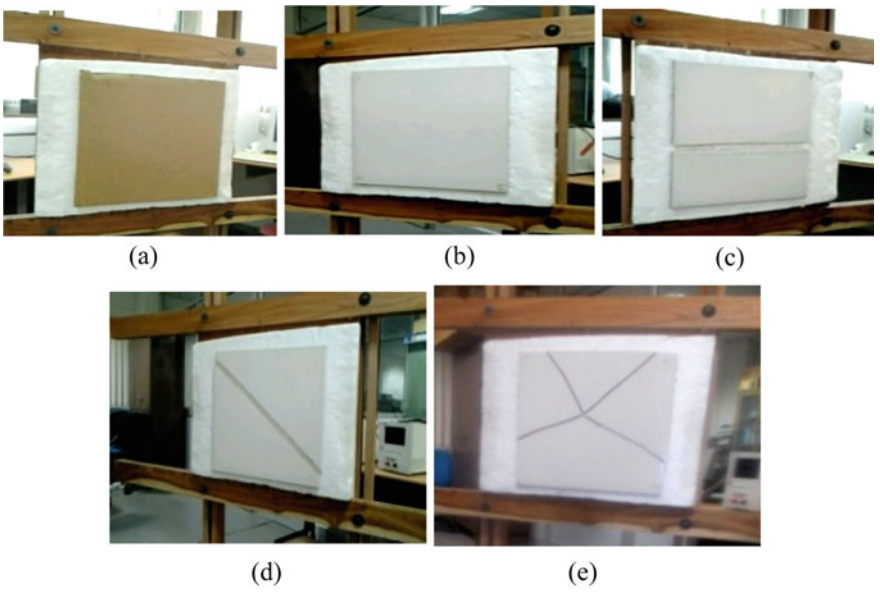

Fig. 1 Experimental arrangement of concealed cracked/non-cracked ceramic tile targets used in different configurations **a** final packaged tile, **b** full no-crack, **c** horizontal crack, **d** diagonal crack, **e** random crack tile

crack type viz., horizontal crack, vertical crack, diagonal crack and random crack were considered as undercover targets as shown in Fig. 1.

3 Methodology for Undercover Target Fault Classification

3.1 Signal Pre-processing

Scattering parameters (S11) due to reflected waves from the distant concealed targets were recorded in real time from different horizontal and vertical scanning locations. This provides details of the target and surroundings in the form of horizontal extent, vertical extent and down range extent i.e., complete target information in the form of 3D data matrix. This raw data require signal pre-processing to convert it into usable form for end user. The steps of signal pre-processing are: inverse fast fourier transform (IFFT), time to spatial domain conversion and sheet calibration. The details of these steps can be found in [6]. After signal pre-processing, target's C-scan image at the target downrange location corresponding to reflection peak in the range profile plot was formed. A complete flow chart showing different signal processing steps for classification of undercover ceramic tile targets is shown in Fig. 2.

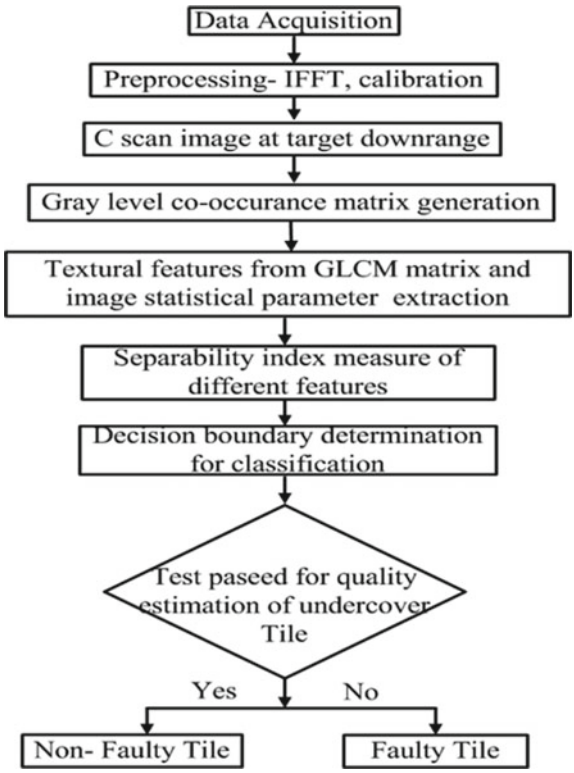

Fig. 2 Flow chart showing statistical features-based target fault classification methodology

3.2 Signal Post-Processing—Feature Extraction

After signal pre-processing, target's exact location can be known but still it is quiet challenging to correctly classify hidden ceramic tiles as cracked / non-cracked correctly. Hence, there is a need of good post-processing methodology for correct classification of unknown targets. In view of this feature extraction techniques prove to be a good choice. Features are invariable descriptors of any image that consists of relevant and unique information in order to successfully discriminate it. Image consisting of spatial local gray tone variations is termed as "texture" depending upon the image type and can be used in determining the quality (faulty/ non-faulty) of undercover ceramic tiles. The gray tone spatial dependence characterizes texture by its co-occurrence, defined by gray level co-occurrence matrix (GLCM) [14]. Hence, different textural features viz.,*contrast,sum entropy, sum variance, entropy, homogeneity, inverse difference moment, correlation, difference entropy, sum average and information measure of correlation* were extracted from respective GLCM matrices formed by corresponding target images as the second order statistical measures.

Apart from this, first order image statistical parameters viz., mean, standard deviation, variance and lacunarity have also been evaluated as features to classify the hidden targets.

3.3 Best Feature Estimation—Separability Measure

Total fifteen different statistical features (first and second order statistics) were extracted from respective concealed targets of different crack/no-crack tile configurations. Now, in order to find best fit textural features out of all these features, a separability measurement test was performed which would tell the level of separation between two considered classes i.e., cracked or non-cracked tile. The separability index is defined as [3]:

$$S_{ij} = \frac{|\mu_i - \mu_j|}{(\sigma_i + \sigma_j)} \tag{3}$$

Here, μ and σ are the mean and standard deviation of the two classes, i.e., cracked tiles and no-crack tiles for any given feature. In particular, $S_{ij} > 0.8$ signifies an authentic feature for separation of two classes i and j correctly.

4 Results and Discussion

Figure 3 shows the plot of separability index for different features. As seen in the figure, five features i.e., contrast, correlation, variance, standard deviation and lacunarity show separability index $S_{ij} > 0.8$. Hence, these features were selected as best fit for classification of packaged tiles into two classes viz. crack and non-crack. Next step is to find the decision boundaries for separation of two classes by analyzing statistical measures (maxima, minima, mean, standard deviation) of the selected textural features using number of different test targets of varying crack / no-crack configurations. Finally, range of the five best fit texture features for the two classes were found as shown in Table 1, by determining [min: max] = $[(\mu - \sigma): (\mu + \sigma)]$.

Further, validation tests were performed on a completely different set of targets i.e., five non-faulty tiles and ten faulty tiles having different crack configurations. Firstly, the best fit five features were calculated for all the validation targets. Then, as per decision boundary given in Table 1 classification of unknown concealed tiles was performed to check whether undercover tile is cracked or non-crack full tile. Table 2 shows the result of classification of the independent validation targets. As shown in Table 2, the developed classification methodology shows very good classification results and in accordance with the actual target type beneath the packaging. Additionally, statistical features lacunarity and standard deviation show 100% overall

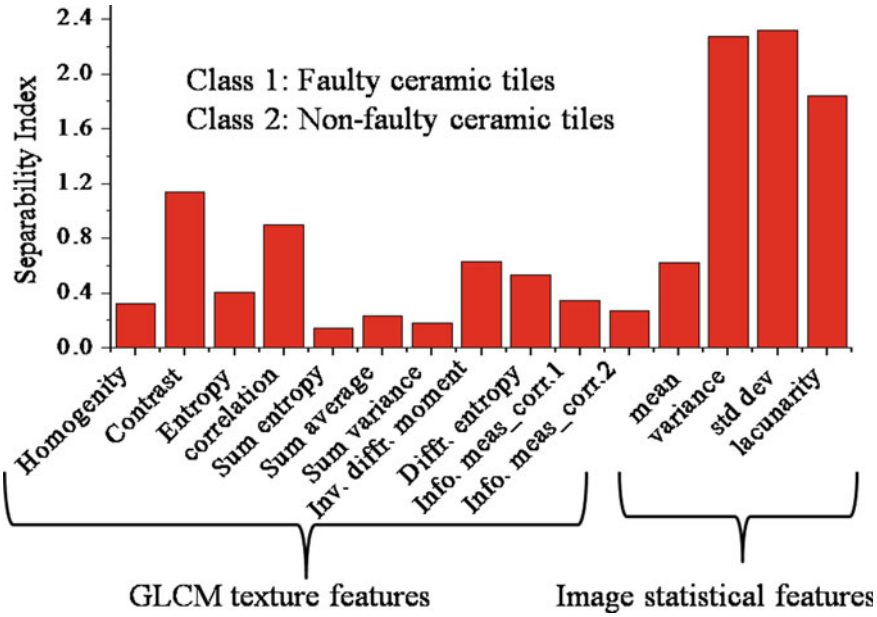

Fig. 3 Separability index measure for faulty/non-faulty tiles

Table 1 Decision boundary of different features for faulty and non-faulty undercover ceramic tiles

S.No.	Parameter	Non-faulty tile				Faulty tile			
		μ	σ	$(\mu - \sigma)$	$(\mu + \sigma)$	μ	σ	$(\mu - \sigma)$	$(\mu + \sigma)$
1	Contrast	1.23	0.37	0.85	1.60	3.3	1.48	1.86	4.82
2	Correlation	0.79	0.09	0.71	0.89	0.51	0.23	0.28	0.74
3	Variance	0.02	0.01	0.01	0.02	0.05	0.01	0.04	0.05
4	Std.deviation	0.13	0.02	0.11	0.15	0.21	0.02	0.19	0.23
5	Lacunarity	1.04	0.015	1.03	1.06	1.15	0.04	1.11	1.19

Table 2 Classification results using independent validation target tiles of different configurations

S. No.	Feature type	Predicted class/true class		
		Faulty/non-faulty	Non-faulty / faulty	Overall accuracy (%)
1	Contrast	0/5	2/ 10	86.6
2	Correlation	1/5	2/10	80
3	Variance	0/5	2/10	86.6
4	Std.deviation	0/5	0/10	100
5	Lacunarity	0/5	0/10	100

classification accuracy. Further, the overall classification accuracy can be made more robust under noisy background by simultaneously considering more than one texture features instead of considering any one feature at a time for classification.

5 Conclusion

A non-destructive concealed target quality monitoring approach has been developed employing millimeter wave imaging radar. Results show very good classification accuracy using a combination of first and second order statistical features for non-destructive quality testing and estimation. Further, the proposed approach can be used for a variety of other industrial applications. MMW-based radar imaging has an added advantage of providing realtime, non-destructive, fast and user friendly quality monitoring instead of conventional long and tedious practices in industries. Use of this NDT technique will certainly boost industry production and fiscal growth.

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Analysis of Negative Capacitance Double-Gate Junctionless Transistor for the Variation of Device Parameters

Manish Kumar Rai and Sanjeev Rai

1 Introduction

In past few years, MOSFET technology has evolved various changes to cope with the problems arising due to rapid scaling. These changes are done mainly to increase the control of gate over channel, to reduce the process complexity at smaller dimensions, to control the leakage current and power consumption. Various such techniques are FinFETs, TFETs, i-MOS, and junctionless transistors. Junctionless transistors remove the limitations arising due to formation of ultra-short junctions which requires quiet complex and costly millisecond annealing process [1]. Further, there is limitation of MOSFET subthreshold swing (60 mV/decade) called Boltzmann Tyranny. This limits a steep switching from OFF to ON condition of the transistor. This limitation arises due to the fundamental thermionic emission mechanism of current conduction in the MOSFET where current increases exponentially with decrease in barrier height [2]. Boltzmann Tyranny also limits the reduction in supply voltage as for satisfactory operation of MOSFET the ratio of ON current to OFF current should be larger than 10^4 but reduction in supply voltage will reduce this ratio. Hence, reduction in the subthreshold swing below fundamental limit of 60 mV/decade is the primary objective of most of the device designers. In ideal case, it should be very close to 0 mV/decade for the abrupt turn on of the MOSFET. Different device architectures are used to improve the device performance which follow different mechanisms of current conduction such as band-to-band tunneling (BTBT) of charge carriers from channel region to drain or impact ionization and so on [3]. Some other mechanisms are based on the improving the electrostatic control of the gate over

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channel region. Although TFET and I-MOS reduce the subthreshold swing, but they have various limitations such as low ON current, asymmetric structure, and high operating voltage. Due to asymmetric structure, the existing circuits and layouts designed for MOS technology have to be redesigned to use these structures, which is quiet complex process. The negative capacitance in MOSFET reduces the power consumption through internal voltage amplification mechanism ($\partial V_g/\partial \Psi_s < 1$) [4, 5]. This voltage amplification using the ferroelectric material scales the supply voltage and reduces the power dissipation [6] which is directly proportional to the square of supply voltage. ($P_{avg} \propto V^2$).

Unlike TFET, it has symmetrical structure which is quite favorable for circuit design. Therefore, NCFETs are considered as a better alternative to conventional MOSFETs. NCFETs are obtained by replacing the gate oxide of a MOSFET by a ferroelectric material. Although NCFET seems to be better alternative to the conventional MOSFET, it suffers from a number of challenges. If designing of NCFET is not proper then its operation becomes unstable and hysteresis takes place [7–9]. This induces different threshold voltages while turning ON and turning OFF. Most of the ferroelectric materials are incompatible to the CMOS process flow and may contaminate the process. Time for the polarization switching of the ferroelectric materials limits the speed of NCFET. Zirconium-doped hafnium oxide (HfZrOx)-based materials have shown negative capacitance and polarization switching for a frequency of 1 MHz [10]. The simulation results have shown that using silicon-doped HfO_2 as a ferroelectric material makes it possible to fabricate the short channel FeFETs with improved performance even without using buffer oxide layer [11]. In simulated device, ferroelectric layer is used in stack with a thin layer of SiO_2. Section 2 presents the device structure and simulation setup to obtain leakage current and other electrical parameters. In Sect. 3, the effect of parameter variation on electrical characteristics is presented. Finally, conclusion of the simulation result is presented in Sect. 4.

2 Device Structure and Simulation Setup

Two-dimensional schematic of symmetric DGJLT with negative capacitance is shown in Fig. 1 where the thickness of ferroelectric layer is denoted by t_f, t_{in} denotes the thickness of insulator (SiO_2) and t_{si} indicates the silicon channel thickness, respectively. The device is highly doped to generate significant ON current and gate consists of Si-doped hafnium oxide as ferroelectric layer in stack with a thin layer of oxide. 2D Silvaco Atlas tool is used for device simulations. Device parameters are given in Table 1.

In device simulations, drift–diffusion model is applied along with the Fermi Dirac statistics to consider the carrier transport. Mobility degradation model due to high device doping and velocity saturation effects at smaller dimensions are also included. Further Shockley–Read–Hall (SRH) and Auger models are included to consider the recombination. To include the effect of band to band tunneling of electrons the BTBT model is included in the simulation. Gate work function is kept 5.2 eV ($p +$

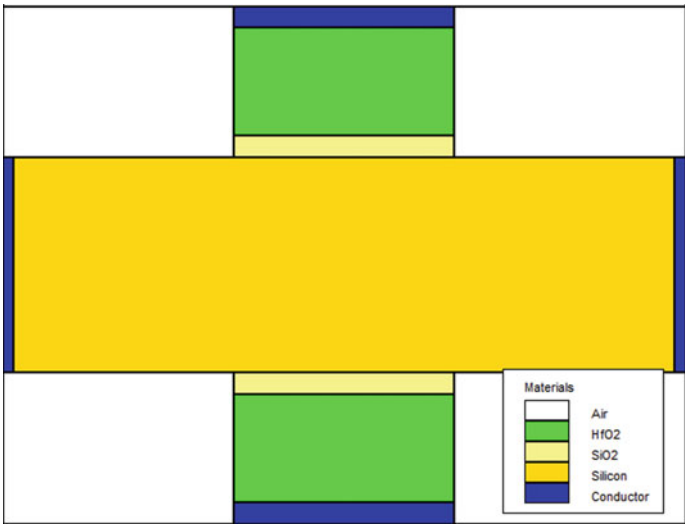

Fig. 1 2D diagram of NC-DGJLT

Table 1 Parameters of the proposed device

Parameter	Value
Channel length	20 nm
Oxide thickness	1 nm
Source/drain doping conc	1×10^{19} atoms cm^{-3}
Channel doping conc	1×10^{19} atoms cm^{-3}
Source/drain electrode work function	4.2 eV
Ferroelectric layer thickness	4 nm
Gate electrode work function	5.2 eV

polysilicon) and device doping concentration is taken equal to 1×10^{19} atoms cm^{-3} to achieve the high ON current and required SS. Using the model parameters of calibrated JLT, we simulate NC-DGJLT structure by including 1-D Landau model for the analysis of stacked ferroelectric layer.

3 Simulation Result and Discussion

Quantum mechanical effects are not considered in simulations since; the silicon layer thickness is more than 6 nm [4]. The voltage between drain and source terminal of device is fixed at 0.1 V and gate to source voltage is varied to plot the transfer characteristics. Temperature is kept at 300 K and ferroelectric layer parameters are optimized to quantitatively analyze the device performance.

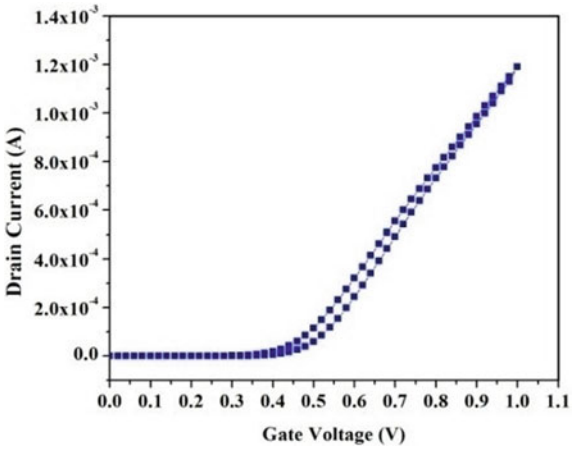

Fig. 2 I_d V_g characteristics of NCDGJLT in forward and reverse sweep of gate voltage

The change in drain current of device in forward and reverse sweep of gate voltage is indicated in Fig. 2. The difference in threshold voltage is found due to hysteresis of ferroelectric material used. We find that the difference in current is very small due to use of silicon-doped HfO_2 as ferroelectric material.

3.1 Impact of Ferroelectric Layer Thickness

In negative capacitance devices, device performance changes with the change in the thickness of ferroelectric layer. As thickness increases, its capacitance decreases and voltage drop across ferroelectric increases. Hence, thick layer of ferroelectric requires higher voltage to produce equal amount of charge [12, 13]. As shown in Fig. 3a leakage current increases with increase in t_f for given gate voltage in the subthreshold regime ($V_{gs} < V_{FB}$) of operation. Subthreshold swing also increases with the increase in ferroelectric material thickness due to reduction in its capacitance (Fig. 3b).

Although ON current slightly reduces with reduction in ferroelectric layer thickness as shown in Fig. 4a, the ON to OFF current ratio significantly increases due to significant reduction in the leakage current Fig. 4b.

3.2 Impact of Oxide Layer Thickness Variation

Variation in thickness of gate oxide varies the oxide capacitance and hence induced charges in the channel vary. The increase in gate oxide thickness reduces its capacitance, this result in a higher voltage drop across the oxide layer and a smaller voltage

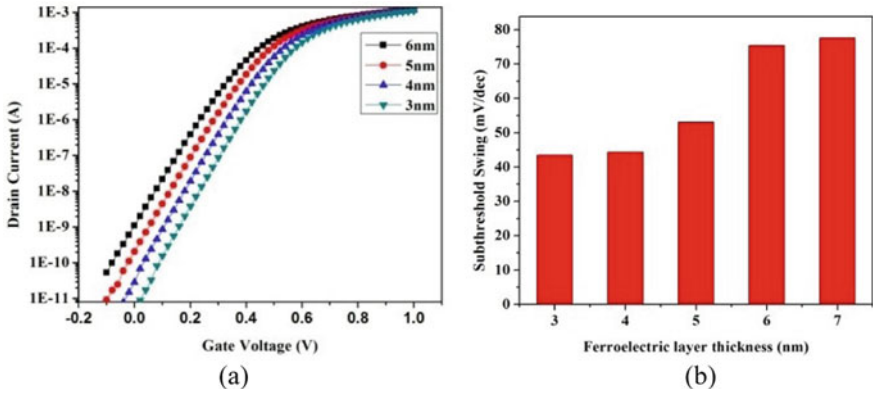

Fig. 3 Variation of **a** leakage current and **b** subthreshold Swing with ferroelectric layer thickness

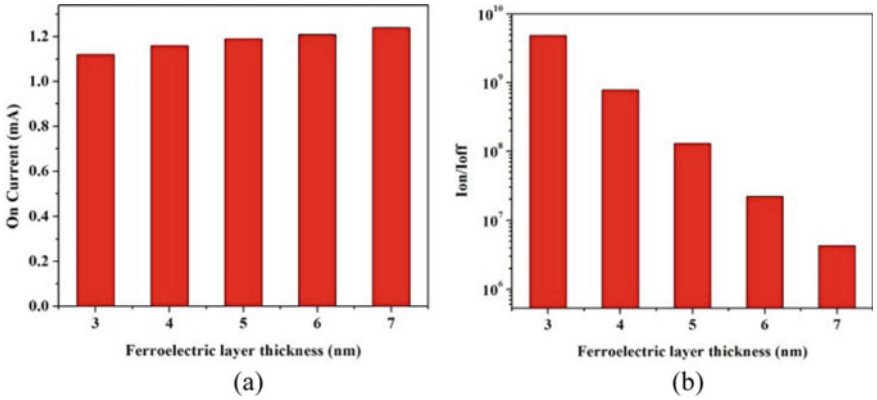

Fig. 4 Variation of **a** ON current and **b** ON to OFF current ratio with ferroelectric layer thickness

drop across ferroelectric layer [14, 15]. The smaller voltage drop across ferroelectric layer reduces its control over channel and increases the leakage current as to at smaller field the magnetic dipoles are not oriented properly. As we find in Fig. 5a the leakage current is much larger for 1.5 nm thickness of SiO_2 in comparison with 0.5 nm. Again threshold voltage reduces with the increase in oxide thickness and subthreshold swing increases (Fig. 5b). The SS value becomes more than 60 mV/dec for a thickness greater than 1 nm.

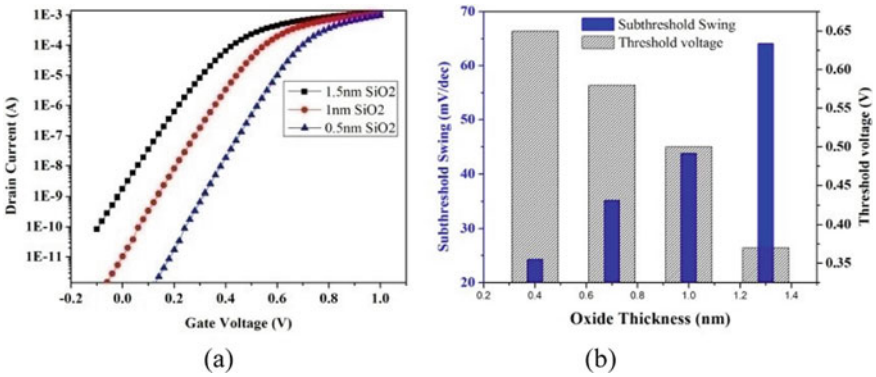

Fig. 5 Variation of **a** ON current and **b** SS and threshold voltage with oxide layer thickness

3.3 Impact of Silicon Thickness Variation

Silicon layer thickness is an important parameter for junctionless transistor. A thicker device could not be depleted completely by the work function difference in OFF state. Hence, from Fig. 6a, we find that thicker device provides higher leakage current due to incomplete removal of charge carriers. Again subthreshold swing value increases with the increase in silicon thickness which degrades the device performance shown in Fig. 6b. Reduction in threshold voltage obtained due to increase in silicon thickness resulted in increased leakage current [16, 17]. Again we find that there is very small variation in the ON current of the device due to increase in silicon thickness which indicates that thinner devices can be used without degrading the ON current with much smaller leakage current.

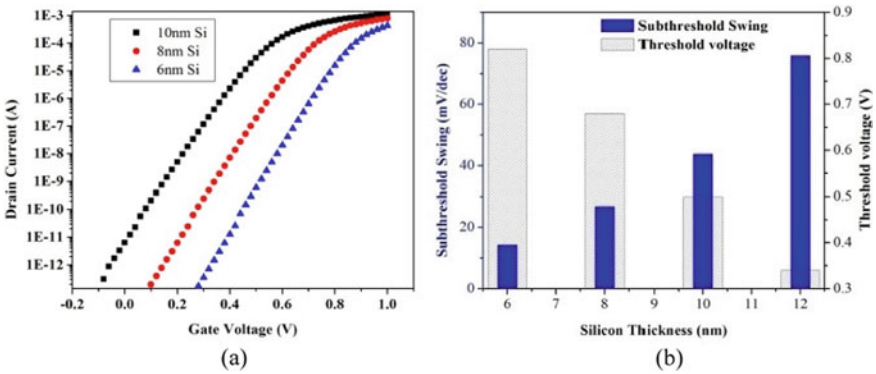

Fig. 6 Variation of **a** ON current and **b** SS and threshold voltage with Si layer thickness

4 Conclusion

The detailed analysis of NCDGJLT has been done for the variation of various parameters of the device such as ferroelectric layer thickness, gate oxide thickness and device thickness. It is concluded that device shows improved switching characteristics by reducing the ferroelectric layer thickness which increases its capacitance. The reduction in the thickness of oxide layer also reduces the voltage drop across oxide layer and creating more charge at smaller voltage. The reduction in the silicon thickness reduces the total no of charge carriers in the channel region which are depleted completely by the gate of device due to difference in the work function of gate material and silicon channel.

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A Compact Size Planar Microstrip-Fed Patch Antenna with Hexagonal DGS Slot for WLAN Application

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1 Introduction

In recent years, high-speed data rate in wireless communication is demanded. To fulfill this demand, wireless local area network (WLAN) is used for high-data rate. The different types of channel for WLAN for Wi-Fi communication are following: (0.90, 2.4, 3.6, 4.9, 5, 5.9, 60) GHz bands [1–3]. For high data rate, a wide band and high-gain antenna are needed. Lots of research are already going on to develop wide band and high-gain antenna. Some of the research works are as discussed below.

A ultra wide band (UWB) radar array has been developed in year 2007 for band range of 23.6 – 24 GHz. It has bandwidth of 400 MHz [4]. L. Dang et al. in 2010 developed multi-band band antenna for WLAN and WiMax having resonant frequencies of 2.7, 3.5 and 5.6 GHz having bandwidth of 600, 430 and 1300 MHz respectively [5]. Sun et al. in 2011 developed an antenna array for WLAN application having resonant frequency of 5.8 GHz and bandwidth of 780 MHz [6]. In 2013, a circularly polarized wideband antenna was developed which works in frequency range of (1.1-1.6) GHz having bandwidth of 500 MHz [7]. A Vee shape dipole antenna was developed in 2014 which having band range of (2.95-3.2) GHz [8]. Sood et al. in 2016 compare three different types of patch antenna for WLAN application having resonant frequencies of 5.49, 5.38 and 5.34 GHz with bandwidth of 140, 95, and 105 MHz respectively [9].

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Sharma et al. in 2016 developed tri-band cylindrical dielectric resonator antenna having three different bandwidth of 410, 800 and 800 MHz respectively and gain at 2.5 and 3 GHz is 2.7 dBi each [10]. Roy et al. in 2017 designed U-shaped antenna for WLAN and ITV band for band ranges of 5.72–5.85 GHz and 8.1–8.5 GHz respectively, bandwidth of 130MHz and 400 MHz respectively and maximum gain of 3.5 dBi [11]. Saraswat et al. in 2018 developed octagonal shaped multiband antenna for WLAN and WiMax application 2.4, 3.5, 5.2 and 5.8 GHz resonant frequencies with bandwidth of 80, 290, 200, 75 MHz respectively and maximum gain of 3.5 dBi [12]. Liu et al. in 2019 developed CPW fed multiband antenna for WLAN and WiMAX application having resonant frequencies of 2.4 GHz, 3.5 GHz and 5.8 GHz having bandwidth of 0.460, 0.60 and 2.03 GHz respectively and gain of 2.1, 1.08 and 1.28 dBi, respectively [13]. P. R. Sura in 2019 designed Psi shaped dual band antenna for WLAN and Wi-Fi application having resonant frequencies of 2.4 and 5.2 GHz with gain of 3.1 and 4.2 dB, respectively [14].

In this manuscript, a regular hexagonal shape DGS slot antenna has been developed. The proposed antenna has very high gain and having wide band range. The DGS is used to enhance bandwidth and gain of antenna [15–17]. The aperture coupled fed line is used of circular polarization [18]. A notch slot has been added in hexagonal slot for proper impedance matching and produces desired resonant frequency.

This manuscript has been divided into four sections. Section 1 is introduces the manuscript. Design specification has been discussed in Sect. 2. Results are discussed in Sect. 3 and finally concluded in Sect. 4.

2 Design Specification

In this section, the proposed antenna design specification has been discussed. There are two antenna has been designed and developed: (a) Antenna with regular hexagonal DGS structure (b) Antenna with regular hexagonal DGS structure. The proposed antenna is designed using substrate NELTEC 9320 having dielectric constant 3.2 and height 1.524 mm. The loss tangent or dissipation factor of substrate (tan δ) 0.0025. The total dimension of the Asymmetric antenna is 31 mm $\times$ 41 mm $\times$ 1.524 mm and the Symmetric antenna is 33 mm $\times$ 41 mm $\times$ 1.524 mm. The design of proposed antenna structure is shown in Fig. 1. The parameter values of proposed antenna discussed in Table 1.

The proposed antenna is designed and simulated on HFSSv15 software. The prototype of both structures has been developed, and antenna results are measured in laboratory. The prototype of both structure are shown in Figs. 2 and 3. Figure 2 shows irregular hexagonal DGS slot antenna, and Fig. 3 shows regular hexagonal DGS slot antenna. The simulated and measured results almost match each others.

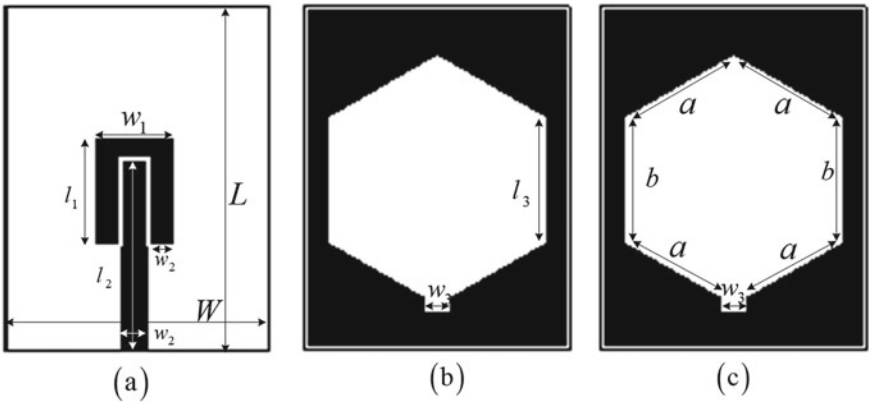

Fig. 1 Proposed structure of antenna **a** top view **b** bottom view of symmetric antenna **c** bottom view of asymmetric antenna

Table 1 Parameters Values

Parameter	L	W	l_1	l_2	l_3	w_1	w_2	w_3	a	b
Value in (mm)	41	33 (Symmetric antenna) 31 (Asymmetric antenna)	12	23	15	10	3	3	13	15

3 Results and Discussion

In this section, simulated and measured results of irregular and regular patch antenna are discussed. Figure 4 shows simulated and measured return loss in dB. This return result is achieved for irregular hexagonal DGS slot structure of antenna. Figure 5 shows simulated and measured return loss in dB regular hexagonal DGS slot structure of antenna. The results of irregular and regular structure are discussed in Table 2.

From Table 2 it is shown that the regular hexagonal DGS slot structure give better measured result in comparison with irregular hexagonal DGS slot structure. The regular hexagonal DGS slot gives two resonant frequencies of 2.4 GHz and 3.1 GHz with return loss of −22 dB and −32 dB, respectively. It has bandwidth of 3 GHz from band range of 2.2–5.2 GHz. The large bandwidth is achieved by hexagonal DGS slot. The regular hexagonal shape of slot produces two resonant frequencies. The notch slot with hexagonal DGS slot is used in impedance matching. The uniform aperture coupled microstrip fed line with uniform resonator helps in producing large bandwidth and also makes antenna approximate circularly polarized. Due to better results achieve in regular hexagonal DGS slot further on this shape, result is discussed in this manuscript.

Figure 6 shows simulated surface vector current distribution over regular hexagonal DGS slot structure of antenna. The current is varies over corner of regular

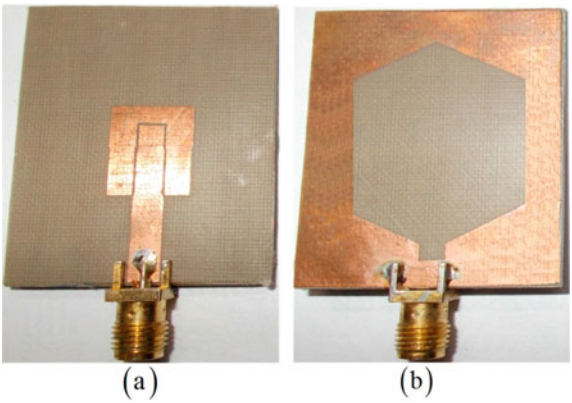

Fig. 2 Prototype of irregular hexagonal DGS slot antenna **a** top view, **b** bottom view

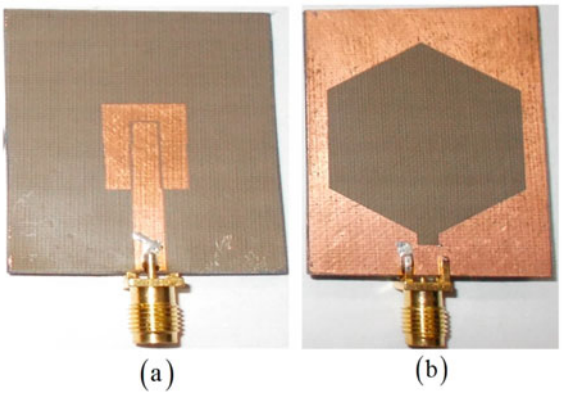

Fig. 3 Prototype of regular hexagonal DGS slot antenna **a** top view, **b** bottom view

hexagonal DGS slot, and this variation produces large bandwidth. The current over notch and on strip line is distributed maximum which helps in proper impedance matching.

Figure 7 shows measured E- and H-plane of regular DGS slot antenna at 2.4 and 3.1 GHz frequencies. This figure shows the polarization of antenna.

Figure 8 shows simulated 3D radiation pattern of gain in dB of regular DGS slot antenna at 2.4 and 3.1 GHz frequencies. This figure shows the variation of gain in dB with respect to theta and phi. The red area shows the maximum gain at this angle.

Figure 9 shows measured gain in dBi with respect to frequency in GHz plot. This figure is gain versus frequency plot. The gain is varies for 2 GHz frequency range to 5 GHz frequency range. The figure the gain of antenna varies in increasing order from 2 to 5 GHz then further it remain constant near 5 GHz frequency. The maximum gain achieved from this figure is 3.9 dBi. The gain at 2.4 GHz and 3.1 GHz is 2.75 dBi and 3 dBi respectively. The proposed work is also compared with recently published work as shown in Table 3. From this table, it is shown that the proposed antenna has better performance that as compared in Table 3.

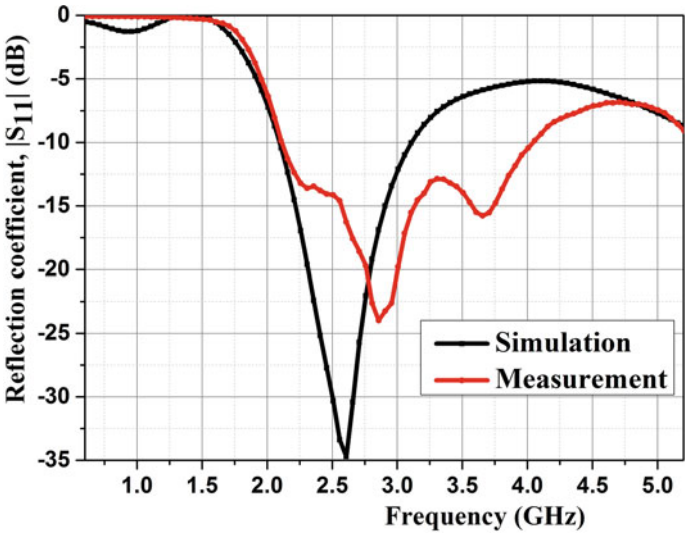

Fig. 4 Return loss in dB versus frequency in GHz graph for irregular DGS slot antenna

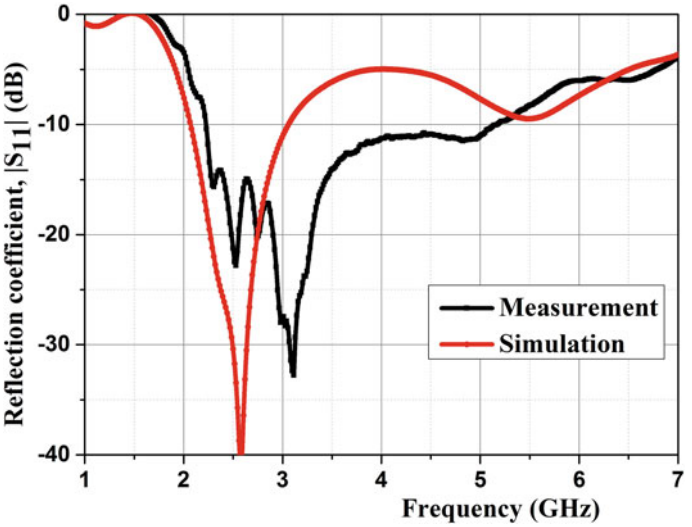

Fig. 5 Return loss in dB versus frequency in GHz graph for regular DGS slot antenna

Table 2 Return loss results

Parameter	Irregular hexagonal DGS slot		Regular hexagonal DGS slot	
	Simulated	Measured	Simulated	Measured
Centre frequency in GHz	2.6	2.8	2.5	2.4, 3.1
S11 in dB	−35	−24	−40	−22, −32
Bandwidth in GHz	1	1.9	1	3

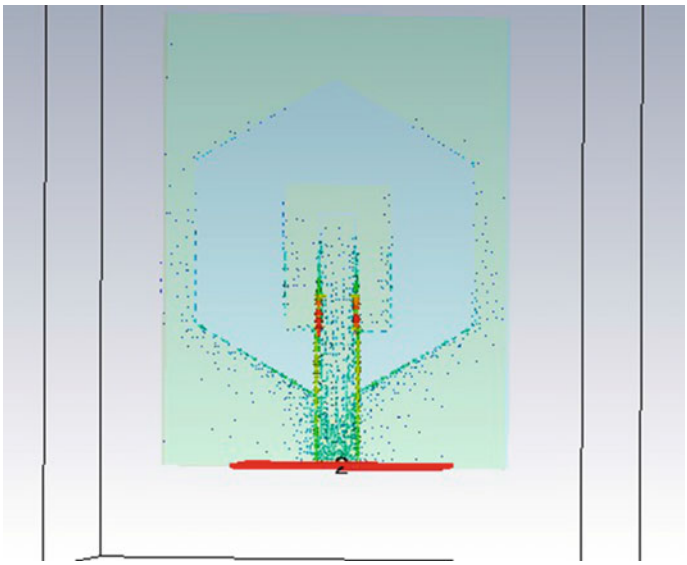

Fig. 6 Surface vector current distribution over regular DGS slot antenna

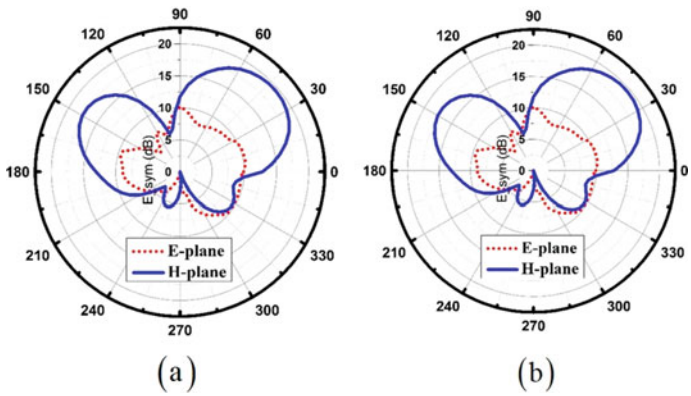

Fig. 7 E-plane and H-plane radiation pattern of regular hexagonal DGS slot antenna at frequency **a** 2.4 GHz and **b** 3.1 GHz

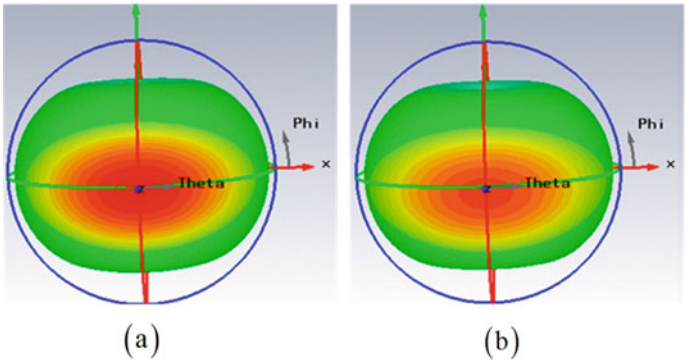

Fig. 8 3D radiation pattern of regular hexagonal DGS slot antenna at frequency **a** 2.4 GHz and **b** 3.1 GHz

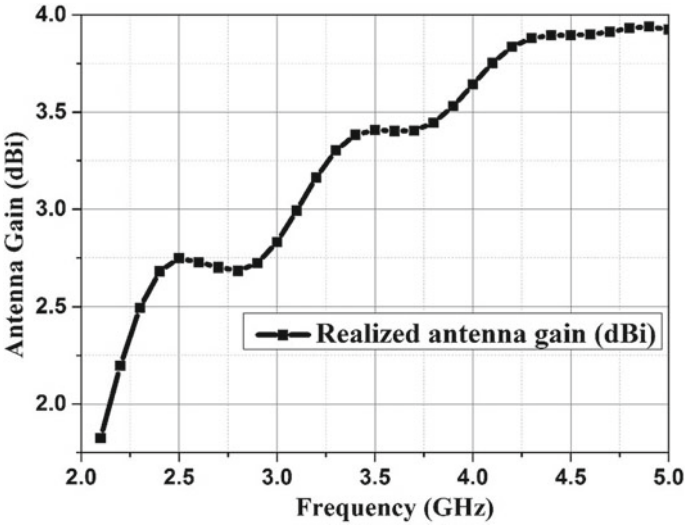

Fig. 9 Gain in dBi versus frequency in GHz plot for regular DGS slot antenna

Table 3 Return loss results

References/parameters	Resonant frequency in GHz	Bandwidth in MHz	Maximum gain in dBi
Sharma et al. in 2016 [10]	2.4, 3.2, 5.8	410, 800, 800	2.7
Roy et al. in 2017 [11]	5.8, 8.2	130, 400	3.5
Saraswat et al. in 2018 [12]	2.4, 3.5, 5.2, 5.8	80, 290, 200, 75	3.5
Liu et al. in 2019 [13]	2.4, 3.5, 5.8	400, 600, 2030	2.1
Proposed Work	2.4, 3.1	3000	3.9

4 Conclusion

In this manuscript, two different antennas are designed, and prototype is developed; one with regular hexagonal DGS slot antenna, and other is irregular hexagonal DGS slot antenna. The simulated amd measured results matches well with each other. The regular hexagonal DGS slot antenna produces better results than the irregular hexagonal DGS slot antenna. The regular hexagonal DGS slot produces two resonant frequencies of 2.4 and 3.1 GHz. It has bandwidth of 3 GHz with band range of 2.2–5.2 GHz. The proposed antenna has maximum gain of 3.9 dBi and it is approximately circularly polarized in nature. This whole band range is mostly used for WLAN application. Also, the proposed antenna is compared with recently published work and gives better result. So, the proposed antenna gives better performance for WLAN application with wide band and high gain.

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Throughput Enhancement in Wireless Sensor Network by Novel Genetic Algorithm-Fuzzy Method (NGA-F)

N. Prakash, M. Rajalakshmi, and R. Nedunchezhian

1 Introduction

Wireless sensor network WSN as also said as Remote Sensor Networks RSN are created to help the users. This incorporate traffic control, home robotization, brilliant combat zone, condition checking and many more. RSN consolidates diverse sensors which disseminates around a specific hub for accomplishing computational activities. Steering is said to be a significant assignment in WSN which will be taken care of cautiously. In order to send the information, the Steering system is required. This is done between the sensor hubs and base stations, to set up correspondence. The principle paradigm, that has been included in the manuscript is about the steering convention which differs dependently on the application. Issues prompt by routing diminished system lifetime with expanded vitality utilization. Different Routing conventions is put forth for limiting the vitality utilization and for augmenting the system lifetime. The directing conventions can be arranged dependent on the hubs' cooperation, bunching conventions, method of working and system structure. The different difficulties that exists in routing incorporates vitality utilization, hub arrangement, adaptability, availability, inclusion, security. The remote sensor system's routing protocol are clarified before. WSN is outfitted with restricted power source. This is because of the equipment limitations. For most of the applications, recharging intensity assets is inconceivable. Accordingly, in a sensor network life expectancy is emphatically subjected to the battery life. A wireless sensor network comprises of hubs which are of remote sensors.

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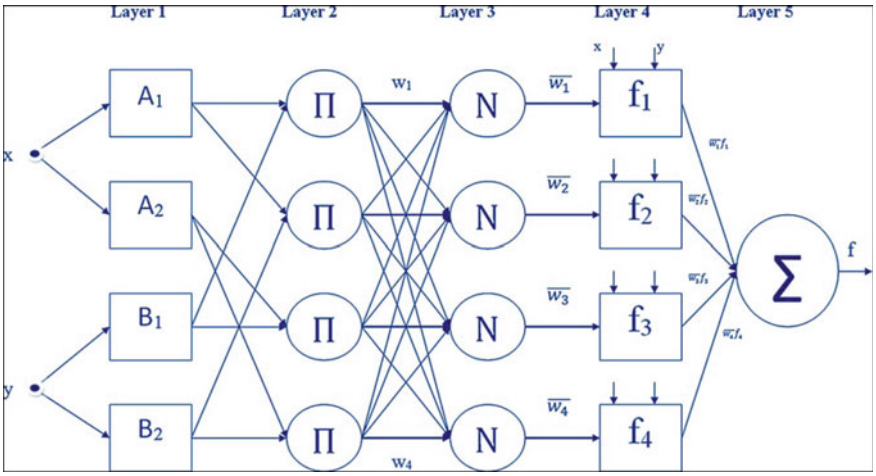

Fig. 1 Adapted network-based fuzzy inference system (ANFIS) structure having two I/P and one O/P

Remote Unveiling insightful practices of machines is given out by utilizing computerized reasoning procedures. Different computerized reasoning methods have been wished-for, for instance, fuzzy rationale, neural systems, enhancement calculations like hereditary calculation, molecule swarm improvement, counterfeit honey bee state calculation. These take care of a wide range of issues that arises from various regions. One of another critical man-made consciousness systems are counterfeit neural system. A few capacities acknowledged by human mind are shown here. False neural systems are shaped by false neurons. For demonstrating a framework utilizing false neural systems, it ought to be prepared utilizing train informational index.

Figure 1 shows the Adapted network-based fuzzy inference system (ANFIS) layer structure having two I/P and one O/P. The figure tells us that there two sources for information. Along with which one yield is present. There are four principles and participation capacities.

2 Related Works

Karaboga and Kaya [1] decided to raise the parameters by utilizing angle plummet, outcome parameters are discovered with the strategy of least squares estimation. On creation of ANN, it is utilized in demonstrating along with identification of various frameworks and victories have been accomplished. The choice of advancement technique used in preparing are essential for obtaining powerful outcomes with adapted network- based fuzzy inference system. It is seen that derivate based and heuristic calculation based are utilized in connectionist systems preparing.

Adnan et al. [2] presents five sorts of examination directed on FL strategies utilized in machining process. Fuzzy logic was considered for expectation, determination, checking, control and enhancement of machining process. Writing demonstrated that processing contributed the most noteworthy number of machining task that was displayed utilizing Fuzzy logic (FL). As far as FL, focus of gravity technique was for the most part used to perform de-fuzzification. Also, triangular for the most part was considered to perform participation work. The surveys expands examination on the basis of capacities, constraints and solid adjustments of Fuzzy logic. The investigation drives creators to presume that Fuzzy logic is the most mainstream artificial intelligence systems utilized in displaying of machining process.

Akay and Karaboga [3] surveyed on the uses of counterfeit honey bee settlement in picture, and video handling. The manuscript shows the issues Swarm intelligence calculation that are connected in the fields. They portray the Swarm intelligence calculation which was utilized in the methodologies for taking care of issues that are arosed. Aliabadian et al. [4] centers around the proficiency of the hereditary calculation for locating the ideal ANN structure and its application to anticipate the disfigurement modulus of shake mass. For locating the ideal number of participation work, GA is used. The learning rates and the energy coefficients and to choose for info factors. The outcomes are then contrasted and those of experimentation system. A database that includes information of about 188 informational indexes.

Aljawarneh et al. [5] presents the engineering and assessment of every technique. It also includes the execution of utilized. Such execution was cultivated through utilization of the Needleman–Wunsch calculation (NWC). This seemed to be lacking because of invariant parts and separations confinements of the polymorphic worm. Subsequently, an Enhanced Contiguous Substring Rewarded calculation was proposed and projected for improve the outcome extraction from the NWC and produce exact marks. The assessment results demonstrated that the mark contains conjunctions of tokens, that are created for lost indispensable data. This could be seen as disregarding one-byte token or rather dismissing the confinement separations. Moreover, the Simplified Regular Expression should be refreshed and precise when contrasted and signature and polygraph techniques.

Bagheri et al. [6] talked about the Financial guaging utilizing adaptive neuro- fuzzy inference system systems. To imitate the manner in which genuine brokers make expectations. This strategy utilizes both verifiable market information and outline instances for estimating market patterns. To start with, wavelet full disintegration of time arrangement investigation was utilized as an ANFIS input information for determining future market costs. The later stage of the manuscript deals with the novel half and half Dynamic Time Warping–Wavelet Transform (WT) technique for programmed design extraction. The outcomes show that the displayed half and half strategy is an extremely helpful and also a viable one. This is important for budgetary value estimating and monetary example extraction.

Çavdar et al. [7] deals with molecule swarm improvement ANFIS. The molecule swa improvement ANFIS equalizer was reproduced on a versatile correspondence model along with Inter symbol interface. The utilized preparing strategy and FCM

gave the best relapse of framework demonstrating to fit to remote channel. The exhibitions of molecule swarm improvement ANFIS equalizer were assessed and contrasted with the equalizers of Maximum-Likelihood Sequence Estimation, Recursive Least Squares and Artificial Neural Network- molecule swarm improvement. The reenactment results demonstrated that the presentation of molecule swarm improvement-ANFIS equalizer along with FCM bunching gives the best execution. The outcome has been compared with the referenced nonlinear leveling procedures.

Ch and Mathur [8] inquired and accomplished by joining the Adaptive Neuro Fuzzy Inference System (ANFIS) to assess the target work inside molecule swarm improvement structure. Afterward, the ANFIS PSO calculation is connected to four issues. The first issues are a solitary loose parameter for outspread stream to a well. Then are two uncertain parameters for 1D solute transport in relentless uniform stream. Then the issue has three uncertain parameters for a 2D heterogeneous enduring stream issue lastly. Finally, the four uncertain parameters for the issue of 2D solute transport. The outcomes demonstrate that with the Adaptive Neuro Fuzzy Inference System PSO calculation, the computational weight is diminished impressively when contrasted with the usually utilized vertex technique.

Dai et al. [9] completed a study on hereditary calculation based face acknowledgment. Generally, unique items can be distinguished and perceived by the format coordinating technique. Yet the acknowledgment speed has consistently been an issue. Furthermore, for acknowledgment by a neural system, preparing the information is consistently tedious. The article presents strategy for hereditary calculation based face acknowledgment is condensed, and explores for constant use are depicted. The chromosomes produced by the hereditary calculation contains parameters about the face, and hereditary administrators are utilized to distinguish and acquire the situation of the substance of enthusiasm for a picture. The parameters considered are directions such as (direction 'x', direction 'y') of the focal point of the face. The rate of scale, and the edge of pivot, are encoded into the GA. Dalkilic and Apaydin [10] examined the versatile systems having utilized for developing a model. The techniques that are proposed for classes quantities of free factors heuristically. On the other hand, in characterizing the ideal class number of free factors, the utilization of recommended legitimacy standard for fuzzy grouping has been pointed. For the situation that autonomous factors have an exponential appropriation, a calculation is put forth for characterizing the obscure parameter of the exchanging relapse model. This is done for getting the evaluated qualities in the wake of acquiring an ideal participation work, that are reasonable for exponential circulation.

Ghosh and Banerjee [11] proposed an information social event approach in which some portable authorities visit just certain stay focused. Here the information gathering is focused instead of all sensor hubs. The versatile authorities begin their voyage of social event data about the system from the sink. The information is assembled from the sensors. The information is then passed on to the sink. This issue has been addressed by calculating named Mobile Collector Path Planning. Mobile Collector Path Planning composition is approved by means of PC recreation considering both snag free and deterrent opposing system. It is dependent on measurements like vitality utilization by the static sensor hubs and system life time. The reproduction results

demonstrate a decrease in vitality utilization and an improvement in system lifetime as contrasted with the existing calculations.

Halim et al. [12] introduced an examination on the current methodologies for the recognition of hazardous driving examples of a vehicle used to anticipate mishaps. Computer based intelligence methods are reviewed for the recognition of dangerous driving style and crash forecast. Various measurable techniques are utilized for anticipating the mishaps by utilizing diverse vehicle and driving highlights are likewise shrouded. The methodologies considered in the manuscript are looked at as far as datasets and expectation execution. Additionally, given a rundown of datasets and the systems are tested and accessible for mainstream researchers to lead look into in the subject area. The manuscript additionally recognizes a portion of the basic open inquiries that should be tended to for street wellbeing utilizing artificial intelligence methods.

Kalpana et al. (2018) recommended Shifted Adaption Homomorphism Encryption. This is viewed as the better choice for all the flow research going on. Shifted Adaption Homomorphism Encryption actualizes the littlest open key and scrambles the whole number and genuine numbers. A noteworthy issue in the field of research is trouble in securing client's inquiries. This is tended to by considering an open key encryption system which depends on the turned around record. This strategy is fitting for portable learning since the projected calculation will not utilize the versatile memory or power.

Ke et al. [13] examined the Energy mindful progressive bunch based directing convention. In a vitality mindful directing methodology, most proposed calculations go for limiting the complete vitality utilization system lifetime. A novel vitality mindful progressive group based is proposed and projected directing convention with two objectives. It includes limiting the all-out vitality utilization and guaranteeing decency of vitality utilization between hubs. Model of the hand-off hub picking issue as a nonlinear programming issue and utilizes the property of curved capacity to locate the ideal arrangement. The assessment are proposed along with calculation by means of reproductions towards the finish of the present manuscript.

Preparing of Adaptive Network-based Fuzzy Inference System means deciding the parameters in its structure utilizing an enhancement calculation. In the preparation stage, reason and outcome parameters are used. So as to get compelling outcomes with ANN, an effective preparing is fundamental. Since the primary improvement of Adaptive Network-based Fuzzy Inference System, distinctive preparing methodologies have been recommended to accomplish better execution. These methodologies are separated into three. They are subsidiary based, heuristic based and half and half. Adaptive Network- based Fuzzy Inference System comprises of two sections as reason and outcome. In preparing of these parts, two unique circumstances has been experienced as indicated by the methodologies recommended in the writing. In the main case, just a single advancement calculation is utilized in preparing of all parameters of ANN. In the subsequent case, half and half learning methodologies are proposed as another strategy for expanding the presentation. Consequently, the issue of nearby least is dispensed with and better exhibitions is gotten. It is seen that half

and half learning methodologies comprising of subsidiary based and heuristic calculations are used broadly. Moreover, there are half and half preparing calculations which utilize just subordinate based techniques.

3 Classification Models Based on Training Approaches

Structure learning and parameters distinguishing proof are the two elements of adapted network-based fuzzy inference system (ANFIS) preparing. Some have concentrated on both two measurements, while others have attempted to chip away at both of the issues. Yet, keeping balance, between decreasing the intricacy of the ANN structure and expanding its precision by parameter tuning. This is a frequent test that is considered. The first adapted network-based fuzzy inference system (ANFIS) anticipated uses half breed realizing. Be that as it may, the downsides of multifaceted nature and inclination to trap in nearby minima have picked the scientists to various options. These choices involve metaheuristic calculations. The essential thought of populace based enhancement calculations is to make a populace of arrangement competitors. The arrangement applicants iteratively investigate the pursuit space and trade data, in this manner odds of meeting on the worldwide minima are fundamentally expanded. Broad writing survey demonstrates that an assortment of metaheuristic calculations has been incorporated with ANN. For the most part, particle swarm optimization and its variations have been connected on ANFIS preparing and streamlining. PSO have been utilised in blending with least square estimator to alter the forerunner and the resulting parameters of ANN models, individually. They are simply cantered around parameter learning, and did not advance fuzzy guideline set. They created ANFIS based expectation models at foreseeing power costs, wind power and consumer loyalty for another item. particle swarm optimization is connected for alone for preparing both the reason and subsequent parameters of artificial neural network based models. Particle swarm optimization is utilized for ANN preparing. Notwithstanding parameter identification, they additionally streamlined FL standard based by applying edge an incentive on the guidelines' terminating quality. Other than the standard of PSO has additionally been utilized to ANFIS learning. Another variation of particle swarm optimization, Adaptive Weighted PSO (AWPSO) with Forgetting Factor Recursive Least Square which one of least square strategies, to recognize the reason and ensuing parameters, separately. The previous research was improved by utilizing Extended Kalman Filter. Aside from PSO, as observational investigation recommends, genetics algorithm is the second most basic way to deal with ANN recognizable proof. Genetic algorithm in mix with least square strategies is actualized to secure ideal ANFIS arrange. Earlier research utilizes ANN for taking care of grouping issue.

Feedforward neural network, especially ANN, has not just unravelled XW the issue of ANFIS yet in addition accomplished more exactness. ANFIS models has increased more notoriety when compared to Feedforward neural network because

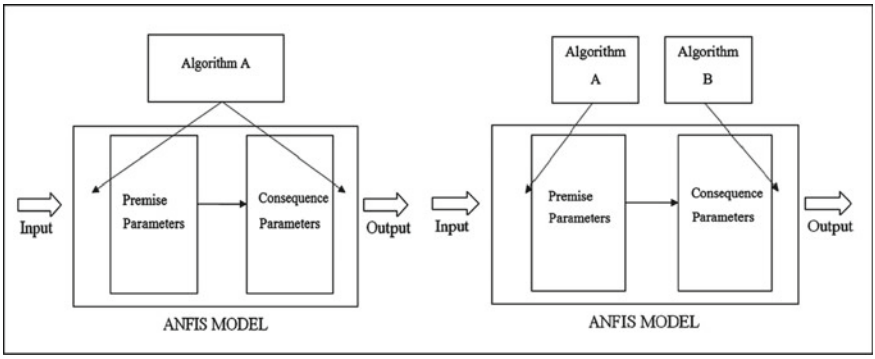

Fig. 2 ANFIS model with single and double algorithm

of the upside of productivity in figuring, adequately versatile with enhancement systems.

Figure 2 shows the ANFIS model with single and double algorithm. It is seen that that are two types of input. In the first there is only one algorithm where as the second input has two different algorithms. Between the input and output, we have the premise parameters and consequences parameters.

4 Proposed Hybrid ANFIS for Throughput Improvement

As the examination is done, a wireless sensor network comprises of hubs was displayed the ceaselessly watch of the system. Information that is obtained by the cluster head (CH) are sent to the hubs in the group. The CH that are present in the system join and minimized the deliberate information and communicate them to the base station. The accompanying presumptions are made as following. Each sensor hub are displayed by the Wireless Sensor Network is consistently disseminated with a similar vitality sources. Distinguish on independently displayed WSN for each sensor unit. Next the sensor hubs relate to the help of a symmetrical radio. Then is the separation between the hubs. It is estimated utilizing a remote radio sign. Base stations area is chosen at the focal point of the system region. The hubs along with the principle station stay latent after they are haphazardly masterminded.

The parameters for the displayed sensor network were taken and are tested for the planned and projected calculation. The model, known as first-request radio model, can be isolated into free space frameworks and multipath blurring frameworks relying upon the space between the transmitting sensor hubs and accepting sensor hubs. A symmetrical correspondence diverts utilized for convention.

Genetic Algorithm (GA) separates sensor hubs into areas in a Sensor network. GA based grouping technique is used to clarify. GAs is a nature propelled approach that utilizes streamlining issues. The hopeful arrangement is made for GA and is

spoken by a populace of people. Iterative methodology is used by GA, adjusting the applicant arrangement set at every emphasis. Every hopeful arrangement set, it is also related with a wellness or target work. The wellness capacity indicates how well the created arrangement performs. The calculation begins by making an underlying populace. After instatement, the calculation chooses a portion of the people from the present populace. This is considered as guardians utilizing roulette wheel choice at each progression. At that point, utilizing the guardians, the number-crunching hybrid capacity is connected to create kids for the people to come. Likewise use transformation over the posterity. Following posterity age, the calculation computes the wellness of everybody. In view of the determined wellness, another populace is resolved. With this iterative methodology, competitor arrangements advance toward an ideal arrangement.

To isolate the sensor hubs, the separation between the sensor hubs and base station is utilized. The wellness capacity is taken as the space between sensor hubs and base station. In the wake of framing the group with genetic algorithm, the middle hub is selected as the underlying bunch head for each group.

Applying ANN for Selecting CH and Finding Energy-Efficient Routes in wireless sensor networks. When sensor hubs send their information legitimately to the base station. The vitality utilization at that point of sensor hubs builds, leading to shortening of the life expectancy of the system. For extending the life expectancy of the system, bunches are made utilizing Genetic Algorithm, and CH and steering are surrounded utilizing the ANFIS organize. For expanding vitality efficiency, one of the hub is chosen as leader of Cluster of nodes. This is done for gathering the detected information. The collected information are consolidate and sent to base station. The cluster head is chosen by expanding vitality effectiveness. This is done by choosing the courses from the sensor hubs in the groups to the base station that limits the general vitality utilized during information gathering. Shaping the bunches utilizing genetic algorithm is done. ANFIS is then connected to the group of nodes that are created. This is done for choosing the cluster head in each group of nodes. The NF derivation framework is connected utilizing the vitality and the good ways from every sensor hub from underlying group head.

The initial phase in the configuration of ANFIS is done. It is done to collect the needed information that are needed for the arrangement of ANFIS. ANFIS contributes to the sensor hub lingering vitality of each bunch in the system also there exists a space between the CH and sensor hub. The yield from the ANFIS system is the likelihood for each group. Once the data or the information is gathered, the information is applied the participation capacity of the fuzzy deduction framework utilizing the subtractive grouping technique. The present manuscript deals with utilizing the network parceling strategy to begin the enrolment work. The information received by the sources are appropriated with triangular participation capacities. Once the instatement of the enrolment work is done. The framework is trained utilizing a blend of backpropagation and least squares estimation. Least squares estimation is utilized to refresh the parameters of the yield participation capacity, and backpropagation is utilized to refresh the parameters of the information enrolment work. After

the preparation procedure, a fuzzy induction framework is made for the given info and yield information.

Sensor Clustering is performed by classifying sensors into different groups. At that point, in each group, a sensor is chosen as the CH. For moving data to the focal station, every sensor sends its data to the bunch head. The data is sent at that point to the focal station. The bunch head can be chosen in different ways. The article performance is utilized in Fuzyy strategy.

Sensors Clustering Using the ANFIS Clustering Algorithm is discussed. Sensors are separated into different groups for sending motion to the focal station. Different bunching strategies exist, but the Fuzzy groupings are considered as extraordinary compared to other bunching techniques. ANFIS that are being utilized in the manuscript, is the most prominent fuzzy bunching calculation. In fuzzy bunching, for every approaching instance, participation of fuzzy gets credited to each group. The ANFIS calculation limits the objective capacity, this relies on bunch focuses and enrolment of fuzzy approaching examples to the group focuses. The objective capacity is characterized as pursues:

$$Sv(x, y) = \sum_{u=1}^{n} \sum_{v=1}^{c} D_v^u d^2(X_u, Y_v) \tag{1}$$

where,

Sv	is denoted as the sensor vector,
S	is denoted as total number of sensor nodes,
C	denotes the number of clusters,
n	is denoted as the quantity of sensors,
X_u, Y_v	is denoted as Euclidean separation,
V	is denoted as a fixed parameter.

After the quantity of bunches is resolved and the group discovering ANFIS calculation is performed on the system sensors. Every sensor having a fuzzy participation gathering is associated with every one of the groups. Every sensor is designated to a group with greatest measure of fuzzy that connects the bunch. At last, to recreate the quantity of group changes, the quantity of ideal bunches is considered.

$$d^2(X_u, Y_v) = \|X_u, Y_v\|^2 \tag{2}$$

CH Selection Using Fuzzy Logic is discussed. A sensor is chosen as the head group. This is done among several sensors. At first, every sensor sends its bundle to the related bunch to move its information to the focal station. At that point, the head group moves this information to the focal station. In any case, head group choice is performed in an unexpected way. The present article, CH choice is performed through fuzzy rationale. For instances in each group, the more vitality a sensor has and the shorter its good ways from the focal station, the higher its fuzzy likelihood turning into a head bunch. For this reason, two fuzzy information sources are utilized

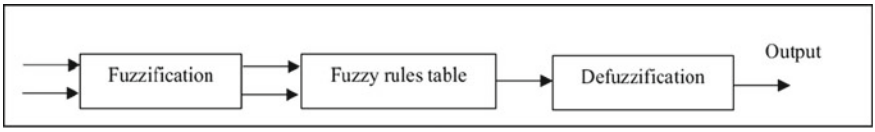

Fig. 3 The structure of the fuzzy system

Table 1 Fuzzy rules for choosing a cluster head by considering two fuzzy inputs

Guidelines	Outstanding energy of the sensor	Sensor standby to indispensable position	Gathering preference subject as a bunch heading
1	Low	Low	High
2	Low	Medium	Low
3	Low	High	Medium
4	Medium	Low	High
5	Medium	Medium	Low
6	Medium	High	Medium
7	High	Low	High
8	High	Medium	Low
9	High	High	Medium

in this article to decide the head bunch. The fuzzy yield is the need level of a sensor turning into a head bunch. Furthermore, five information participation capacities and five yield enrolment capacities are utilized. These capacities comprise of less, little and normal. In every reiteration, nonfuzzy data sources are standardized over period (0, 1) and fuzzy propensities are in this way assigned to different capacities.

The vitality level is the power that every hub devours and disseminates utilizing a triangular participation work. This is shown in Fig. 3. The structure of the fuzzy system is seen. There are two inputs seen in the fuzzification. The fuzzification is connected to Fuzzy rues table. The table in turn is connected to Defuzzification. From which the output was obtained.

The CH choose fuzzy participation capacities are sorted out in Table 1. Where by and large demonstrates that, the higher the vitality of a sensor and the shorter its good ways from the focal station, the almost certain it is to turn into a group head. Table 1 additionally abridges choice standards we use with the fuzzy framework. Table 1 shows the Fuzzy rules for choosing a cluster head by considering two fuzzy inputs. 9 guidelines have been chosen. Outstanding energy of the sensor, Sensor standby to indispensable position and Gathering preference subject as a bunch heading are compared.

5 Results and Discussion

The yield information for the ANFIS is discussed as organized. The vitality level and the separation among group head and the sensor hubs contributes to the ANN. The hub that has been selected is the most extreme likelihood of being head of the cluster. After introduction, the system prepares the utilization of a mixture calculation for 100 cycles, and the last guidelines are produced. The preparation is done by testing. Subsequent for preparing the ANFIS arrange, the grid for sensor network is set up. The zone or the grid that is considered is around 200×200 m^2. The typical hub, propelled hub and the base station of the system is seen that are present in WSN. The typical and propelled hubs are haphazardly circulated in the region. Covered area for the base station is said to be (100,100) meters. The system that was considered having 40 nodes, 20 nodes are made physically that are called as sensor hubs. There is a load that is present is trust worthy. When a false information is transmitted the trust, load diminishes by 0.2. When the point of trust worth load surpasses to 0.6 of any hub. The hub is set as an aggressor hub.

Algorithm for formation of cluster, determining the cluster head and routes.

Step 1: Initialize and deploy the sensor nodes WSN areas.
Step 2: Apply GA clustering for deployed sensor nodes based on distance between base station and sensor nodes.
Step 3: ANFIS is applied for routing algorithm based on energy level of sensor nodes and distance between CH and Sensor nodes in the cluster.
Step 4: Applying weighted trust evaluation for malicious nodes in the WSN.
Step 5: Compare the number of nodes greater than frequency.
Step 6: If the number of nodes greater than frequency, move to next step, that is Step 7.
Step 7: If the number of nodes is not greater than frequency, move to Step 2.

As the sensor network repeats itself. For each round, the sensor hubs that are prepared send information are detected and are to the base station. The hubs send the information which they received to the CH. Once the CH gathers the information, they course the information gathered from the sensors to the BS. When directing information from sensor hubs, the information is checked by the group head and rethinks about the trust estimation of the sensor hubs. The system life expectancies for Proposed NGA-Fuzzy method (NGA-F), Dual Fuzzy Logic-Cluster Protocol (DFLCP), Low-Energy Adaptive Clustering Hierarchy (LEACH), Centralized Low-Energy Adaptive Clustering Hierarchy (LEACH-C), Enhanced Distributed Energy Efficient Clustering (EDEEC), Hybrid Energy Efficient Distributed clustering (HEED) strategy are appeared in the following figures. The graphical representation is seen. The flat line demonstrates the quantity of reiterations and the vertical line shows vitality of sensors that are alive.

Figure 4 shows the Number of alive sensors compared for various method having different algorithm. NGA-F, DFLCP, LEACH, LEACH-C, EDEEC, HEED is all graphically represented. It is clearly depicted that as the number of rounds increases,

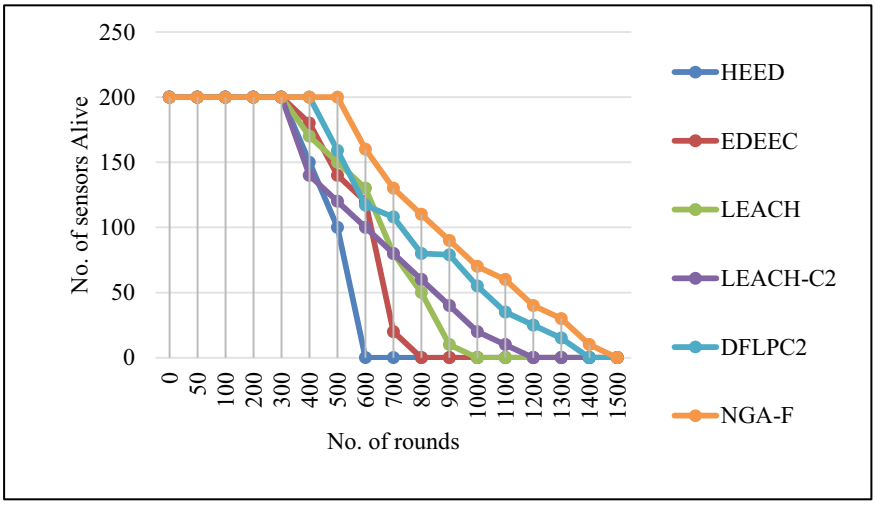

Fig. 4 Number of alive sensors compared for various method having different algorithm

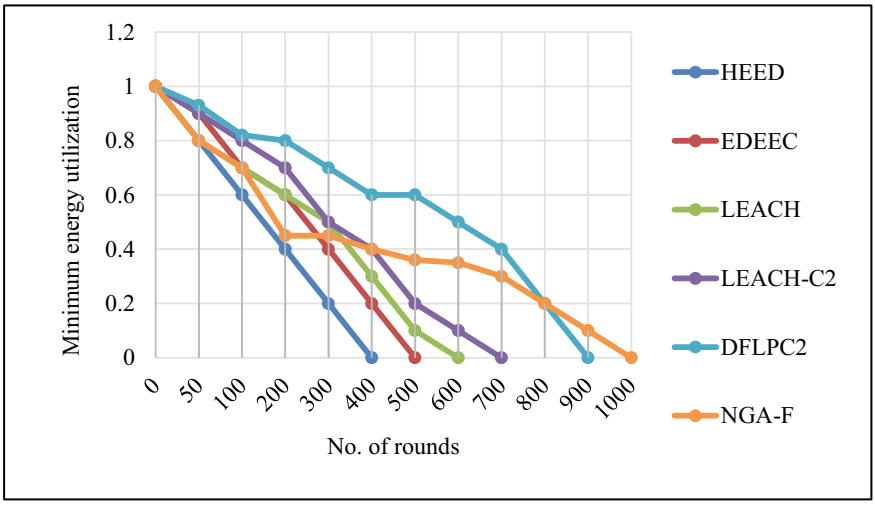

Fig. 5 Minimum energy utilization comparison of the NGA-F with other methods

the number of sensors that are alive increase from other methodologies to the proposed method.

Figure 5 shows the Minimum energy utilization comparison of the NGA-F with other methods. Its is clearly seen that the energy used get minimised as more number of nodes. The maximum number of nodes seen is 1000 nodes. Maximum energy utilization is considered to be 1.

Figure 6 shows the average energy is compared for proposed NGA-F method with

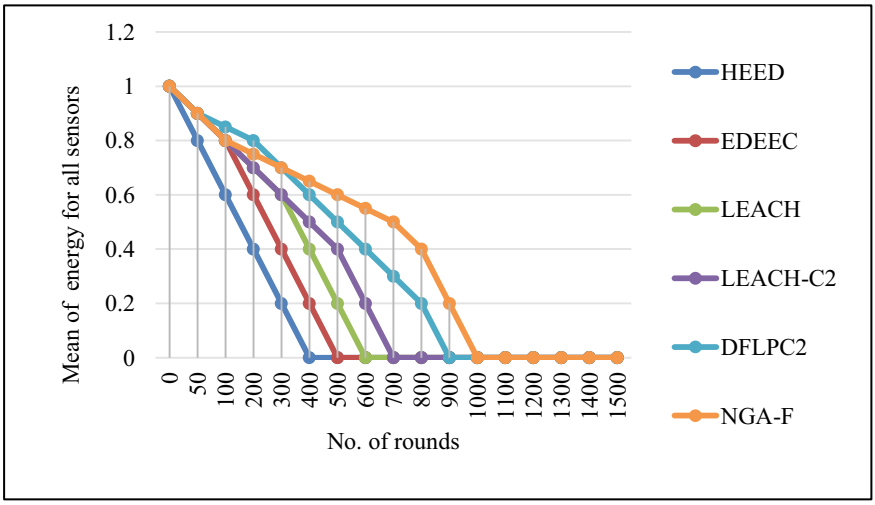

Fig. 6 Average energy is compared for proposed NGA-F method with other existing method

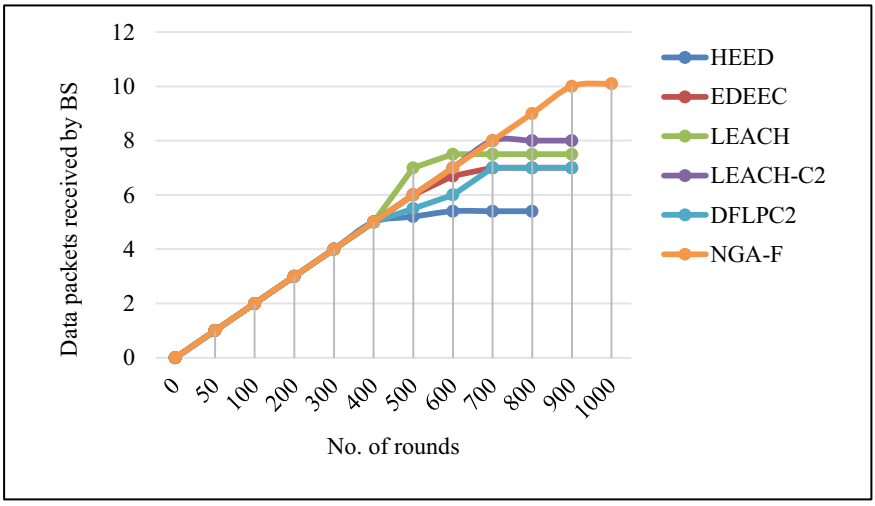

Fig. 7 Data packets received by the base station

other existing method. It is seen that when the number of rounds reaches around 400, 500 to 1000, the mean of energy becomes constant or rather 0. Mean of energy for all sensors decreases accordingly.

Figure 7 shows that the Data packets received by the base station. Here initially there is a linear growth of the graph of Data packets received by base station. NGA-F, DFLCP, LEACH, LEACH-C, EDEEC, HEED increases linearily. At a point the methods diverts and varies for different methods.

6 Conclusion

Remote ANFIS has not just beated ANNs but also different kinds of Fuzzy Inference Systems. However it has been broadly connected in business as well as in money. ANFIS is prominent in different kinds of Fuzzy Inference Systems. It is straightforward, adaptable, as well as versatile. In any case, when the quantity of sources of information augments, exponential flood in the quantity of standards builds its intricacy and computational expense. The initial two-pass learning calculation utilizes inclination search strategy. This strategy is computationally costly and less effective. The proposed technique is an expansion of wireless sensor network life expectancy by diminishing vitality devoured for information transmission. The hereditary calculation is consolidated along with the fuzzy strategy. For directing, the utilization of hereditary calculation is done by the group head. The fuzzy technique and ANN are utilized. The weighted trust assessment has been proposed to identify noxious hubs. Further the increment of life expectancy for the wireless sensor network. Our proposed NGA-Fuzzy method (NGA-F) strategy is contrasted with five existing strategies Dual Fuzzy Logic-Cluster Protocol (DFLCP), Low-Energy Adaptive Clustering Hierarchy (LEACH), Centralized Low-Energy Adaptive Clustering Hierarchy (LEACH-C), Enhanced Distributed Energy Efficient Clustering (EDEEC), Hybrid Energy.

Efficient Distributed clustering (HEED). Recreations are performed utilizing the software MATLAB of latest version. From the reproduction results, we saw that the life expectancy of the system was higher than that of the DFLCP, LEACH, LEACH-C, EDEEC, HEED methodologies. Finally the proposed strategy is successful projected and implemented for CH determination, information steering in Wireless Sensor Network.

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Numerical Analysis of Transversely Porous Core PCF with Square Airhole Cladding

Anurag Upadhyay, Y. K. Prajapati, and Rajeev Tripathi

1 Introduction

These days, optical fibers are the backbone of the telecommunication industry [1]. Due to few limitations of conventional optical fibers such as core-cladding index matching, low power handling capacity, small dispersion control and poor birefringence, photonic crystal fibers (PCF) came into picture [2]. PCF have an advantage of being more flexible, better birefringence, negative dispersion, improved power handling, low confinement loss, because of being constructed of the single material [3]. Hence PCF are applicable in numerous applications, such as biomedical fields, and polarization sustain fiber [3, 4]. Across the whole length of the PCF, air holes are running periodically throughout the cladding structure, hence creating a refractive index (RI) contrast between core and cladding structure. Hence, PCF operates on total internal reflection (TIR) theory in which core RI is greater than that of the cladding, while photonic band gap (PBG) principle works for vice versa RI index value [5]. Merely by controlling diameter (D) and pitch (Λ) of the airholes, optical properties of PCF can be easily handled [6].

In 2003, by modifying the structure of PCF, low transmission loss along with nearly ZDW is achieved [7]. Introduction of linear or nonlinear airholes in cladding and core hole defect increase the degree of dispersion parameter control [8]. In 2008,

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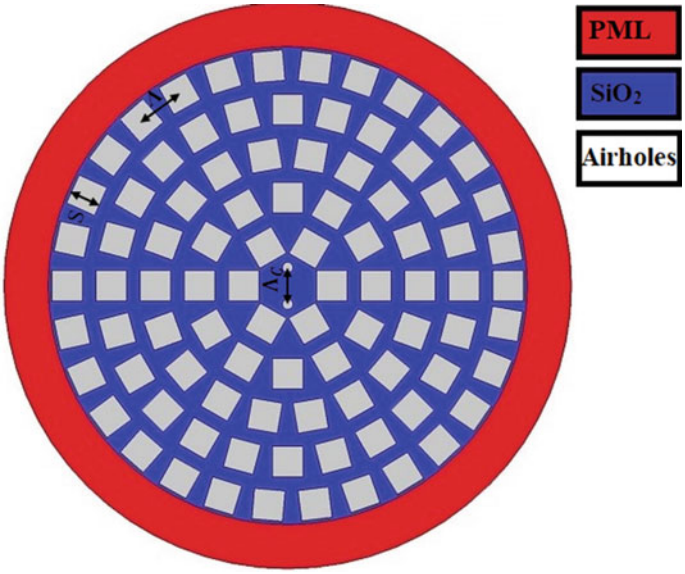

Fig. 1 2D schematic diagram of the proposed PCF with square airhole cladding and transversely perforated core

a very good negative dispersion equal to −185 ps/nm/km is achieved by Marcos et al. [9]. Sensing application utilizes birefringence and nonlinear coefficients properties [10]. In 2020, Upadhyay et al. also demonstrated that the ZDW can be varied by introducing airholes in the core of propounded PCF [11].

In this paper, four annular rings of square airholes have been considered in the proposed PCF for confining light in the core as shown in Fig. 1. Excellent results are presented during analysis, through vital optical performance parameters, as like chromatic dispersion, birefringence and nonlinearity coefficient. The propounded structure is practically integrable. The proposed structure is analyzed with finite element method (FEM)-based COMSOL Multiphysics. The paper is arranged in the prescribed manner; Sect. 1 presents introduction of PCF. Section 2 deals with the proposed architectural design and its mathematical modeling. Section 3 provides various results obtained during analysis and discussion over it, while Sect. 4 presents conclusion of the manuscript.

2 Mathematical Modeling of the Proposed Structure

The proposed PCF contains circular airholes in the core along with five circular rings of square airholes in the cladding region. Here square-shaped airholes are preferred because of larger hole packing density as compared to circular airholes of same size [12]. Large HPD ratio resulted in larger refractive index (RI) contrast difference

between core and cladding. Henceforth more amount of light energy can be trapped across the core region of the proposed structure [12]. Radius of each circular ring and number of square airholes in that ring can be formulated as

$$R_{\text{ring}} = \Lambda \times \eth \tag{1}$$

$$N_{\text{Airhole}} = 6 \times \eth \tag{2}$$

where Λ denotes pitch, which is basically separation in two adjacent circular rings in the cladding, while ðdenotes the number of circular rings from the core of PCF. In order to satisfy light propagation criterion in the core and large wavelength range investigation, large HPD ration must be maintained. Besides this, hole packing density (HPD) ratio of square-shaped air holes and circular-shaped airholes is compared. The diameter of circular holes (D) and side of square holes (S) are of same value. The HPD ratio (S/ Λ) is calculated using Eqs. (3) and (4) [12]

$$\text{HPD})_{\text{SQ}} = (S/\Lambda)^2 \tag{3}$$

$$(\text{HPD})_C = (\pi/4) \times (D/\Lambda)^2 \tag{4}$$

where $(\text{HPD})_{\text{SQ}}$ depicts HPD ratio of square hole, $(\text{HPD})_C$ shows HPD ratio of circular ring, S represents side length of square hole, Λ denotes pitch, and D indicates diameter of circular hole. The first radius of air hole ring is equivalent to pitch (i.e. Λ = 1.2um). From calculations, it is proved that HPD ratio of square hole ring is larger than HPD ratio of circular hole ring. Larger HPD ratio is necessary to confiscate maximum light energy in the core due to larger RI difference between core and cladding of PCF. Recommended PCF core is perforated by two circular airholes of same diameter in transverse direction of PCF. The whole structure is optimized for pitch of core circular airholes $\Lambda_C = 1$ μm, side length (S) of square airhole = 0.85 μm and pitch = 1.2 μm with HPD ratio (S/Λ) equals to 0.70.

The background material is used in the structure is SiO_2 as it is translucent in the in the communication window (1330–1550 nm). RI of silicon dioxide can be predetermined with the use of Sellmeier's equation [13].

$$n_{SiO_2} = \sqrt{1 + \frac{0.6961\lambda_{op}^2}{\lambda_{op}^2 - 0.0684^2} + \frac{0.4079\lambda_{op}^2}{\lambda_{op}^2 - 0.1162^2} + \frac{0.8974\lambda_{op}^2}{\lambda_{op}^2 - 9.8961^2}} \tag{5}$$

Generally, PCF is fabricated through Stack and Draw method in which silica capillaries are stressed down to PCF length and provide mechanical stability to the PCF structure. For square hole PCF fabrication, solgel method can be preferred [14]. An outer layer of 1 μm thickness used to absorb the unwanted scattering losses, is known as perfectly matched layer (PML). The whole structure is subdivided into few triangular substructures and mesh analysis is applied over these triangular subspaces

and PCF is divided into 7116 domain elements and 1319 boundary elements along with degree of freedom equal to 50,297. FEM-based COMSOL Multiphysics software is used to solve the Maxwell's equation for triangular subspaces. The following equation has been derived using Maxwell's equation [15];

$$\nabla \times \left(\left[\sum \right]^{-1} \nabla \times \vec{E} - k_0^2 n^2 \left[\sum \right] \vec{E} \right) = 0 \tag{6}$$

Here, $[\sum]^{-1}$ and $[\sum]$ show tridiagonal matrices for absorbing PML and inverse PML layer, respectively. $k_0 = (2 \times \pi)/\lambda$ is wavenumber, while E is the electric field. The propagation constant 'β' can be defined as:

$$\beta = k_0 \times N_{\text{eff}} \tag{7}$$

where N_{eff} denotes the effective refractive index (ERI) of the structure which can be estimated by simulation.

When light in the core is transmitted through the fiber length, light is decomposed into two fundamental polarized modes (x- and y-). Due to external stress, birefringence effect is observed, which is generated due to difference of effective RI between the x- and y- polarized modes [16]. The birefringence (BF) is given as

$$\text{BF}(\lambda) = \left| N_{\text{eff}}^X - N_{\text{eff}}^Y \right| \tag{8}$$

The dispersion of the fiber is the sum of material dispersion and waveguide dispersion. Material dispersion is always positive for any structure. This in order to cancel the effect of material dispersion, waveguide dispersion must be negative and it can be defined as [11]

$$d = -\frac{\lambda_{op}}{C} \frac{d^2 N_{eff}}{d\lambda_{op}^2} \tag{9}$$

where λ_{op} designates operating wavelength, C denotes the speed of light in free space, and N_{eff} shows ERI of the PCF.

The area in which light trapped in the core of PCF is known as effective area (A_{eff}), and it is formulated as [11].

$$A_{\text{eff}} = \frac{\iint \left(|E|^2 \text{d}A \right)^2}{\iint \left(|E|^4 \text{d}A \right)} \tag{10}$$

where E is the electric field of the fundamental mode in the core of PCF.

Nonlinear coefficient (γ_{NL}) is related to nonlinear phenomenal application of fiber, and high nonlinear coefficient is necessary with high birefringence for the sensing application of the proposed PCF. It can be calculated as [13]

$$\gamma_{\mathrm{NL}} = \frac{2 \times \pi \times n_R}{\lambda_{op} \times A_{\mathrm{eff}}} \tag{11}$$

where n_R is the nonlinear RI of the SiO_2 and A_{eff} denotes the effective area of the PCF.

Confinement loss (CL) is basically the loss associated with deviation of the core light from the fiber core, and it can be calculated using Eq. (12) [16, 17]

$$\mathrm{CL}(\mathrm{d}B/m) = 8.686 \times k_0 \times \ \mathrm{Img}(N_{\mathrm{eff}}) \tag{12}$$

where $\mathrm{Img}(N_{eff})$ denotes the imaginary part of ERI of proposed structure.

3 Results and Discussion

This section deals with fluctuation in the optical variables of proffer PCF such as waveguide dispersion, γ_{NL}, A_{eff} and CL with contrast in the structural parameters such as change in core airhole pitch. Structural parameters can vary with an anomaly in the designing parameter in the fabrication process. Hence, fabrication tolerance is taken up to $\pm$ 2%.

Figure 2a–d displays the distribution of electric field intensity of core mode which is totally confined in the core of proposed PCF. Figure 2 a, b shows the *x*-polarized and *y*-polarized electric field for core pitch ($\Lambda_C = 1.0$ µm), respectively, while Fig. 2 c, d shows the *x*-polarized and *y*-polarized electric field for core pitch ($\Lambda_C = 0.5$ µm), respectively.

Birefringence is basically the RI difference between two fundamental core mode such as *x*-and *y*-polarization. This may be enumerated using Eq. (8). From Fig. 3, it is seen that maximum obtained birefringence values are 4.2×10^{-3} and 2.3×10^{-3}

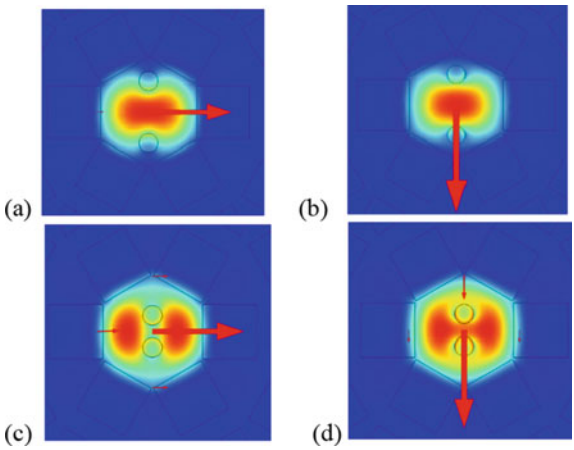

Fig. 2 Electric field scattering of the rudimentary core mode of the propounded structure on **a** *x*-polarization for $\Lambda_C = 1.00$ µm **b** *y*-polarization at $\Lambda_C = 1.00$ µm **c** *x*-polarization for $\Lambda_C = 0.50$ µm **d** *y*-polarization for $\Lambda_C = 0.50$ µm respectively

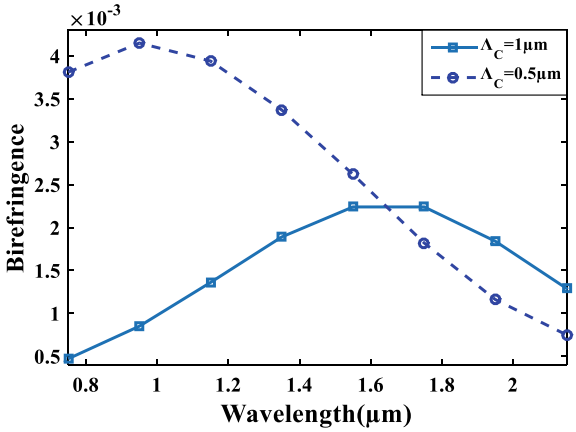

Fig. 3 The birefringence versus wavelength curve for the variation in the pitch of circular core airhole

for $\Lambda_C = 0.5$ μm and $\Lambda_C = 1$ μm, respectively. Such high value of birefringence is useful in polarization maintaining fiber application.

The dispersion profile for projected PCF and notably evaluated with Eq. (9). Negative dispersion is obtained for $\Lambda_C = 0.5$ μm quietly appreciable from Fig. 4, whereas after 1.2 μm wavelength chromatic dispersion is negative for $\Lambda_C = 1.0$ μm. Henceforth, for both core pitch values the proposed PCF shows highly negative dispersion values for communication window (1.3–1.55 μm) and the maximum obtained value is −425.5 ps/nm/km. Such high values of dispersion make the proposed PCF suitable for dispersion compensating fiber.

Effective area basically defines the confinement area of fundamental mode in the core of fiber, and it can be numerically investigated using Eq. (10). From Fig. 5, it is seen that fundamental mode confines in very small core area and its minimum value equal to 1 μm^2 is observed at 0.8 μm operating frequency for *x*-polarization of both core pitch values.

High value of nonlinearity is essential parameter for a fiber to be applied for supercontinuum generation and frequency conversation. From Fig. 6, it is seen that very high nonlinearity equal to 204 W^{-1} km^{-1} is obtained at 0.75 μm of operating

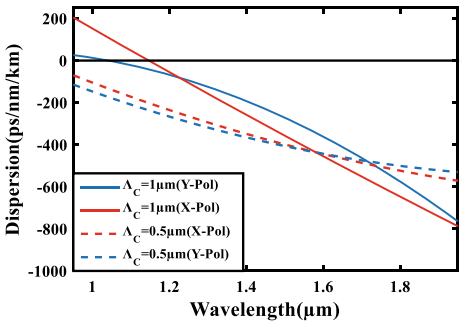

Fig. 4 The figure of dispersion deviation with wavelength for the change in pitch of core airholes

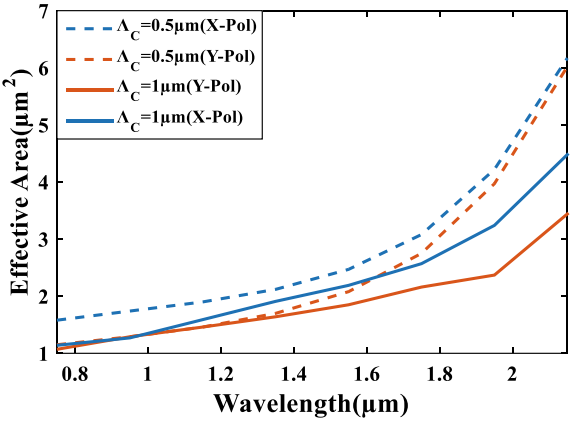

Fig. 5 The graph for A_{eff} variation with wavelength against alternation in pitch of core airholes

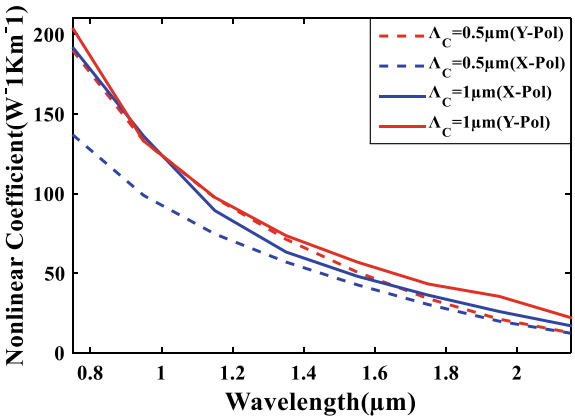

Fig. 6 Nonlinear coefficient versus operating wavelength graph for the change in the pitch of circular core airholes

frequency for x-polarization of $\Lambda_C = 1$ μm. Thus, the proposed PCF is a potential candidate for supercontinuum generation application.

Confinement loss is basically the measure of core mode light deviation from the core region to cladding region of the fiber. Hence, it defines the loss incurred with fundamental core mode of PCF. It can be calculated with Eq. (12). From Fig. 7, it is obvious that CL increases with variation in wavelength and its minimum observed value is 10^{-11} dB/m for both *x*- and *y*-polarization at $\Lambda_C = 1$ μm, while loss incurred is 10^{-5} and 10^{-4} for 1.55 μm at $\Lambda_C = 1$ μm and $\Lambda_C = 0.5$ μm, respectively. Such low loss values drive the desired PCF for low loss waveguide implementation.

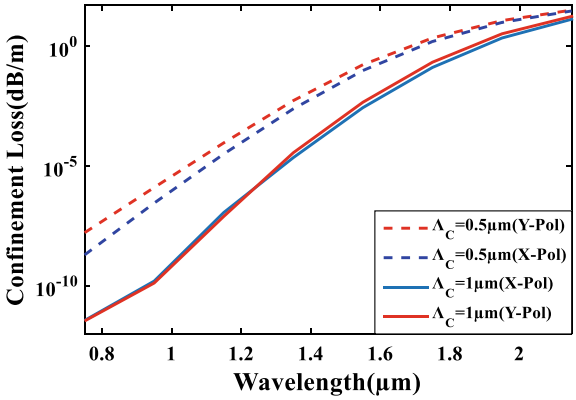

Fig. 7 The graph of change in confinement loss with variation in operating wavelength for different pitch values of circular core airhole

4 Conclusion

A simple circular airhole porous core with five circular rings of square-shaped cladding airholes is proposed. The structure is optimized for optical parameters variation with change in its structural parameters using FEM. From results, we achieved high values of birefringence and nonlinearity equal to 4.2×10^{-3}, 204 W^{-1} km^{-1}, respectively. The proposed PCF also shows very large negative dispersion value of -800 ps/nm/km. A very low confinement loss and effective area equal to 10^{-11} dB/m and 1 μm^2 has also been achieved from optimized results. Henceforth, the propounded design can be used in polarization maintaining fiber, dispersion compensator, low loss waveguide and in biomedical imaging and sensing applications.

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Single-Side-Polished Gold-Coated SPR-Based PCF RI Sensor

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1 Introduction

Nowadays, PCF-based SPR sensor devices have gained recognition because of its high sensitivity and a broad range of operating wavelengths. SPR-based optical sensors are frequently used in various useful applications like food quality testing, medical diagnostics as well as environmental monitoring [1]. PCF is much advantageous over conventional optical fiber because of its compact structure, low confinement loss, high flexibility and large mode area [2]. Surface plasmon resonance is a phenomenon in which the free electrons (in the form of electron gas density) propagate along the metal–dielectric interface at a certain resonance condition. At resonance, the maximum available core mode energy is transferred to the polariton (SPP) mode. Due to this, a sharp resonance peak (or loss peak) is obtained at a certain wavelength for the analyte RI to be investigated [3]. When an analyte of the particular RI is placed on the top of the metallic surface, a shift in wavelength is observed which indicates the detection of the analyte. In SPR-based PCF, an active metal (gold, silver, copper) film can be deposited either into the holes or on the top polished fiber surface.

Silver (Ag) and Au are the frequently used active metals that can be utilized for the coating of fiber. Among them, Au is the most extensively used metal as it has good chemical stability [4]. The main advantage of using Au is that it provides large resonance shift between consecutive analyte RIs. But, at the same time the obtained resonance peak for the analyte becomes wide which may reduce its detection accuracy. On the other side, Ag provides narrow peak and leads to better detection accuracy [5]. However, the major issue with Ag is its rapid oxidation when exposed to an aqueous environment which can reduce the PCF-based sensor's performance.

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An optical sensor mainly relies on two basic types of sensing approach. One of them is internal sensing. In this approach, the liquid analyte infiltrates into the particular holes and causing the complex sensing mechanism. While another one is based on external sensing which offers direct flow of the liquid on the metal coated outer plane of the fiber [6]. Among both the approaches, the external sensing approach is most favorable for the real-time sensing application because it avoids internal filling or coating of an active metal. Moreover, the fabrication becomes much easier for the optical sensor that relies on external sensing mechanism [7].

Recently, the external sensing-based single-side-polished (or D-shaped) structures have been used and reported [8, 9]. Among them, Gangwar et al. [10] in 2016 proposed the Au-coated one-side-polished SPR-based PCF RI sensor. By doing so, they have obtained maximum sensitivity of 7700 nm RIU^{-1} with RI resolution as 1.30×10^{-5} RIU in the detection range of 1.43 to 1.46. In 2018, Liu et al. [11] reported SPR-based D-shaped PCF for RI detection. After optimizing the structural parameters, the highest sensitivity was obtained as 15,180 nm RIU^{-1} over the detection range 1.40–1.43. Further, in the same year, Wu et al. [12] demonstrated a D-shaped sensor. The Au layer was coated only on the polished surface instead of internal coating of the air holes. Therefore, the maximum achieved sensitivity and resolution were of 31,000 nm/RIU and 3.31×10^{-5} RIU, respectively, within the detection range of 1.32–1.40.

In this article, a highly sensitive Au-plated single-side-polished PCF RI sensor is proposed. The plasmonic metal Au is employed on the flat surface for the generation and excitation of plasmons. In addition, it has good chemical stability and it also exhibits large resonance shift even for the minor analyte RI variation. In the proposed structure, a solid core is surrounded with cladding consisting air holes of a fixed size. Silica is used as a background material. The two large and two small air holes near to the solid core form a circular ring around it which helps to concentrate and transfer the large amount of existing core mode power to the SPP mode. Moreover, the geometrical dimensions such small and large hole diameter along with Au thickness have been optimized for better sensing performance of the proposed D-shaped optical sensor.

2 Geometrical Modeling and Numerical Analysis

The simulation and numerical analysis of the stated PCF have been carried out with the help of FEM-based COMSOL Multiphysics software. Figure 1 depicts 2D schematic of the proposed structure. It consists of a core surrounded by the two circular air hole rings. The inner ring contains two large air holes of diameter (D) 1.3 μm placed symmetrical with respect to the solid fiber, while the second outer ring of cladding region contains air holes with diameter (d) 0.6 μm. The lattice spacing (Λ) between the air holes is taken as 2.4 μm. Moreover, the base material silica is used to form core and cladding region, while the holes are kept empty. The Au-coated polished surface is used for the generation of an adequate surface plasmons on the

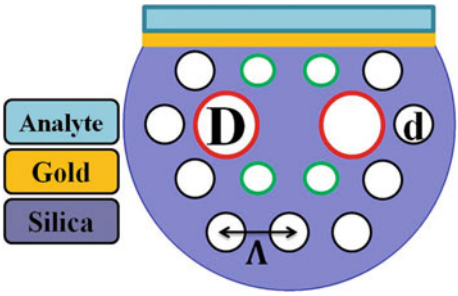

Fig. 1 Schematic cross section of the proposed optical sensor

metallic surface so that the plasmonic wave can propagate along the metal–dielectric interface. The gold permittivity (ε_G) can be estimated using Drude model given as [12]:

$$\varepsilon_G = \varepsilon_\infty - \frac{\omega_D^2}{\omega(\omega + i\gamma_D)} - \frac{\Delta\varepsilon\Omega_l^2}{\left(\omega^2 - \Omega_l^2\right) + i\Gamma_l\omega} \tag{1}$$

The various optical constants such as plasma (ω_D), damping (γ_D) and oscillation (Ω_l) frequency along with spectral width (Γ) can be obtained using [12].

The confinement loss (α_l) through the PCF can be determined as [13].

$$\alpha_l = 8.686 \times \frac{2\pi}{\lambda} \times I_m(n_{eff}) \times 10^4 \text{ dB/cm} \tag{2}$$

where, λ and $I_m(n_{eff})$ denote wavelength and imaginary portion of the effective RI.

2.1 The Proposed sensor's Fabrication Compatibility

The fabrication of the propose structure can be started by bundling solid rods along with thin and thick capillaries with the help of standard stack and draw technique [14]. To make a flat D-shaped surface, a solid rod is polished to a certain depth. After structure fabrication process, a thin gold nanolayer will be plated on the polished fiber surface using the existing deposition technique such as chemical vapor deposition (CVD) [15, 16]. Therefore, with such well-known fabrication method and deposition techniques, the proposed PCF can be easily fabricated.

3 Results and Discussion

In this section, simulation was performed with the proposed structure and several modes like core, SPP and resonance mode have been verified. Moreover, the dispersion relationship has also been discussed thoroughly for different analyte RIs.

3.1 Dispersion Relations

Figure 2a–d shows the field intensity profiles obtained at different modes after simulation of the proposed PCF. Figure 2a, b shows the *x*-and *y*-component of core mode energy in which the entire field is concentrated in the core area. Then, the core directed energy transferred to the metal–dielectric interface, called as SPP mode, depicted in Fig. 2c. Figure 2d displays the condition when core and SPP mode energies linked with each other, called as coupling mode or resonance mode. This mode indicates the analyte detection.

Figure 3a–d shows dispersion relations and loss curve for different values of

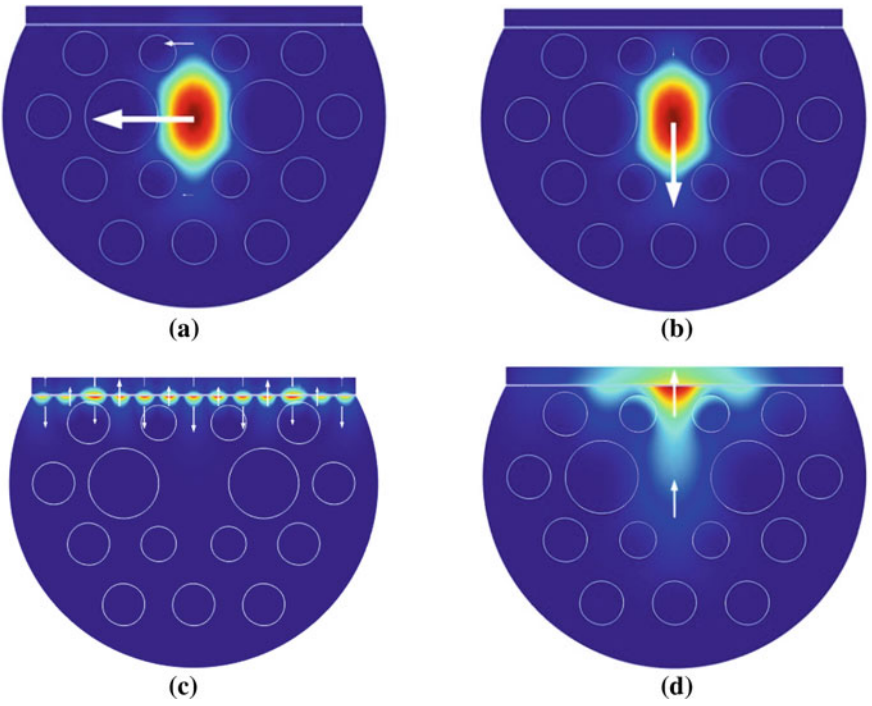

Fig. 2 Intensity profiles in various modes **a** *x*- and, **b** *y*- polarized core mode **c** SPP mode **d** coupling mode

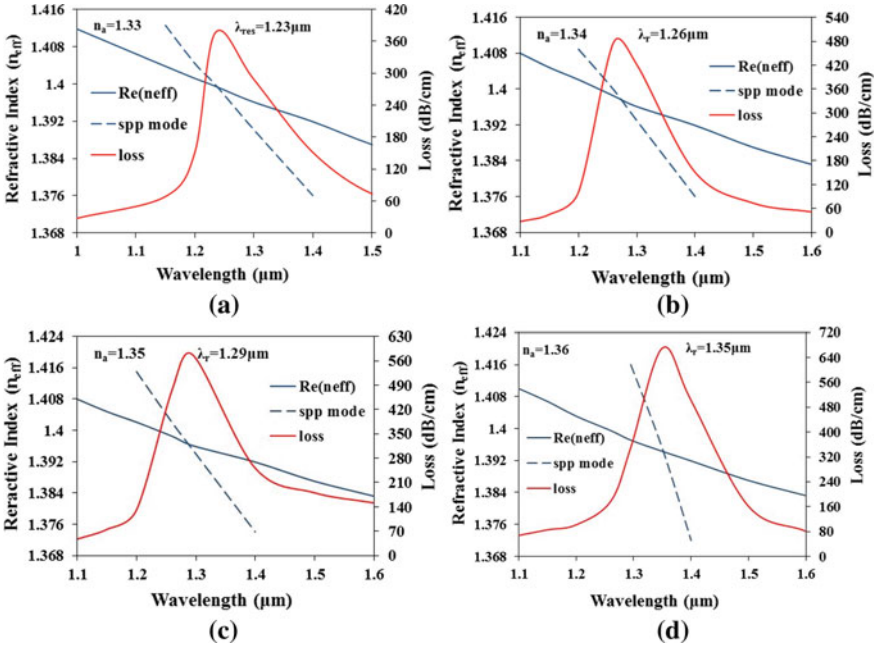

Fig. 3 Change in loss profile and dispersion relation with wavelength when n_a changes from 1.33 to 1.36 with an optimized Au thickness (t = 40 nm), large (D) and small **d** air hole diameter of 1.3 μm and 0.4 μm, respectively

analyte RI (n_a). From the above Fig. 3a–d, the solid blue line corresponds to core mode effective RI which is responsible for dispersion, while the red curve indicates imaginary part which accounts for overall confinement loss of the PCF. Moreover, the blue-dashed line indicates SPP mode. Now, if we consider the dispersion relation for $n_a = 1.33$, then it is clearly visible in Fig. 3a that at a certain resonance wavelength (i.e.,λ_{res} = 1.29 μm), both the lines intersect each other. At this intersecting point, resonance occurs. Due to this, a sudden hike in the loss value is observed as both the modes get coupled. Therefore, mode coupling between core and SPP causes unknown analyte/sample detection.

Further, the sensitivity is calculated on the basis of shift in the resonant peak (λ_r) using the technique known as wavelength interrogation [17]:

$$S_W = \frac{\Delta\lambda_{peak}}{\Delta n_a} \text{ nm RIU}^{-1} \tag{3}$$

where, S_W is the wavelength sensitivity, $\Delta\lambda_{peak}$ indicates the necessary shift and Δn_a reveals the variation in n_a.

The calculated sensitivity using above Eq. 1 is 6000 nm/RIU. Moreover, the resolution is also estimated as [18]:

$$R = \frac{\Delta n_a \Delta \lambda_{min}}{\Delta \lambda_{peak}} \text{ RIU} \quad (4)$$

where, R is the sensor resolution, Δn_a is the change in analyte RI and $\Delta \lambda_{min}$ assumed to be 0.1 nm. The highest resolution achieved using Eq. 2 is 3.55×10^{-5} RIU.

Table 1 displays numerical study of the proposed PCF for multiple analyte RIs. It is clearly visible from Table 1 that sensitivity increases with analyte RI for *x*-pol, *y*-pol, and it reaches to maximum value of 6000 nm/RIU for the change in n_a from 1.35 to 1.36 (sustaining *y*-polarized mode). In addition, the maximum resolution is also found high as 3.33×10^{-5} RIU at $n_a = 1.33, 1.34$.

Figure 4 displays the fitting curve with analyte RI. Red dots represent the resonant points. Initially, the first resonant point (i.e., 1.23 μm) is observed at analyte RI 1.33. Then, it is shifted to 1.35 μm at $n_a = 1.36$. Therefore, the overall shift in resonance wavelength is obtained as 120 nm. Additionally, the fitting curve is found linear in the entire analyte RI range of 1.33–1.36 with R^2 value of 0.9943.

In Table 2, the proposed sensor's parameters such as wavelength sensitivity and resolution have been compared and found better than the recently published research works listed in Table 2.

Table 1 Numerical analysis of the proposed sensor with respect to sensitivity and resolution for $n_a = 1.33$–1.36

n_a	λ_{res} (nm)		$\Delta\lambda_{res}$ (nm)		Sensitivity (nm/RIU)		Resolution (RIU)	
	x-pol	*y*-pol	*x*-pol	*y*-pol	*x*-pol	*y*-pol	*x*-pol	*y*-pol
1.33	1235	1230	25	30	2500	3000	3.33×10^{-5}	3.33×10^{-5}
1.34	1260	1260	30	30	3000	3000	3.33×10^{-5}	3.33×10^{-5}
1.35	1290	1290	50	60	5000	6000	1.88×10^{-5}	1.67×10^{-5}
1.36	1340	1350	–	–		–	–	–

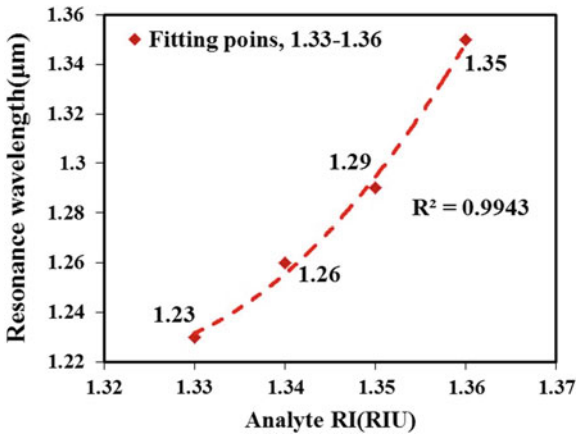

Fig. 4 Fitting curve combined with different resonant points for analyte RI range of 1.33–1.36

Table 2 A comparative study of the proposed D-shaped PCF with other reported PCFs

References	configuration	Detection range	Sensitivity (nm/RIU)	Resolution (RIU)
[19]	Grapefruit PCF	1.33–1.335	2400	–
[20]	Helical PCF	1.33–1.38	4600	–
[21]	D-shape	1.333–1.398	4122	–
[22]	Dual ring hexagonal PCF	1.33–1.37	4000	–
[23]	D-shaped	1.32–1.35	4000	3.31×10^{-5}
[24]	Microchannel-based hexagonal PCF	1.32–1.34	5000	2×10^{-5}
Proposed	D-shaped	1.33–1.36	6000	3.31×10^{-5}

3.2 *Effect of Gold Layer Thickness* (t)*, Small* (d) *and Large* (D) *Air Hole Diameter on Sensing Performance*

Figure 5 depicts change in the loss peaks with respect to wavelength in accordance with the variations in Au thickness, small (d) and large (D) air hole diameter. It is

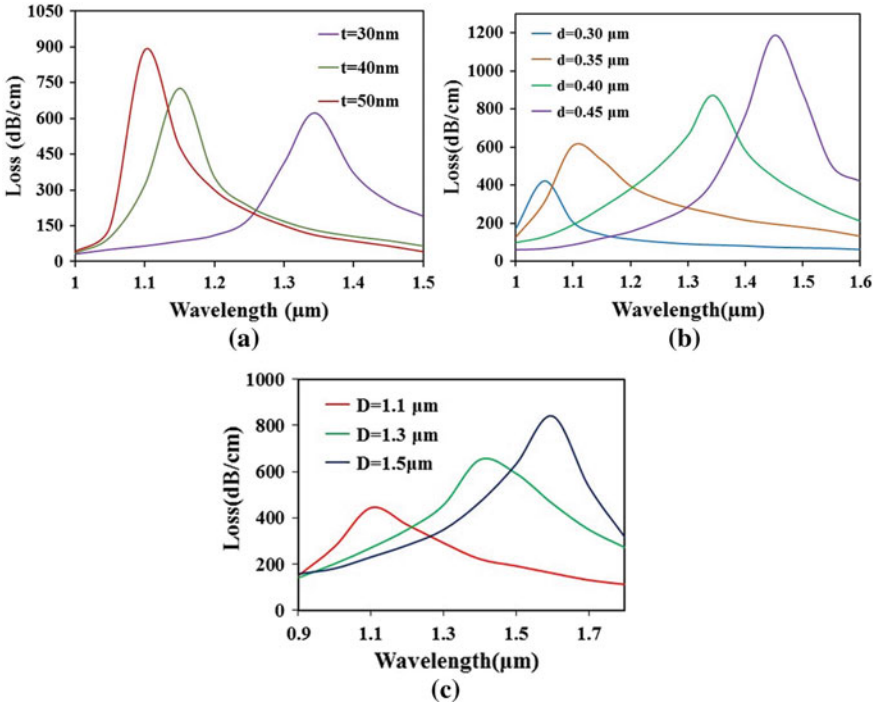

Fig. 5 Variation in loss peak with **a** Au thickness, **b** small, and **c** large hole diameters

seen from Fig. 5a that the loss values are 601 dB/cm, 726 dB/cm and 891 dB/cm with Au thickness, $t = 30$, 40 and 50 nm, respectively. Although the minimum loss value is obtained at $t = 30$ nm but at the same time, the loss peak gets broadened which may degrade the detection accuracy. This happens mainly due to the higher amount of plasmon damping at the metal–dielectric interface. Therefore, the gold layer thickness in our simulation has been optimized to 40 nm. The effect of varying hole diameter present in the cladding region can be observed in Fig. 5b. It is found that that the loss peak values are 401 dB/cm, 600 dB/cm, 810 dB/cm and 1190 dB/cm with an increasing diameter (d) values of 0.30, 0.35, 0.40 and 0.45 μm, respectively. The effect of varying two large air hole diameters (D) is shown in Fig. 5c. The loss peak shifts toward higher wavelengths, and its maximum values are obtained as 443.59 dB/cm, 651.37 dB/cm and 840.41 dB/cm at $D = 1.1$, 1.3 and 1.5 μm, respectively. Moreover, it is also worth to notice that the coupling loss is high at $D = 1.5$ μm. It is because of squeezing the maximum available core mode energy by these two large air holes toward the metal–dielectric interface.

4 Conclusion

Gold-deposited single-side-polished plasmonic RI sensor is numerically verified. The numerical analysis was done by finite element method. SPR effect was observed when the phases of SPP and core mode were exactly matched. The gold film thickness was optimized to 40 nm. Further, the small (d) and large (D) air hole diameters were kept at 0.40 and 1.3 μm. By doing so, the highest wavelength sensitivity reached to 6000 nm/RIU along with RI resolution of 3.33×10^{-5}RIU within the RI ranges from 1.33 to 1.36. Hence, our proposed sensor can be effectively utilized in biosensing applications.

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Application of Carbon Nanotube (CNT) in Glucose Liquid Sample Sensing Using SPR Technique

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1 Introduction

A healthy person should have maintained blood glucose level because contradistinction from standard value causes various diseases like diabetes, abnormal functioning of neurons and brain, and many more [1]. International agency American Diabetes Association sets a standard level of glucose for a healthy human body. As per standard, pre-meal and after-meal glucose level must be 90–130 mg/dl and 180 mg/dl, respectively [2]. In this paper, we are focused toward the proper sensing of glucose concentration in a liquid sample using surface plasmon resonance (SPR)-based biosensor [3]. SPR-based sensors already commercialized for many biological applications like DNA hybridization, drug industries, food quality inspection, enzyme detection, and many more [4]. SPR is nothing but the excitation of surface plasmon waves (SPWs) at the metal–dielectric interface. It was first introduced by Otto [5] and commercialized by Kretschmann [6, 7]. Later, Nylander and Liedberg et al. utilized SPR Kretschmann configuration another area than biological in gas sensing also [8]. Since then, a diverse range of sensing like measurements of temperature, humidity, chemical, and biological composition, concentration utilize SPR virtue, as all these parameters cause a variation of the refractive index of the analyte [9]. Biosensor, an analytic device, includes two significant parts first one is bioreceptor another one is a transducer (or detector). Bioreceptor interacts with targeted analyte while transducer transforms the signal from the interaction into a form that can be easily measured like voltage. From the last decade, carbon nanotubes (CNTs) made significant progress in biosensing applications. CNTs are 1D nanosheets that allow signals to transport in confined space and make them extremely sensitive for any electrical and chemical changes in their contacting environment. In 1991, Japanese physicist and scientist Lijima discovered [10] extensively utilized nanomaterial CNT

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which proves itself the most significant material in various research areas due to their unique properties. CNTs are categorized mainly into single-walled or SWCNT and many-walled or MWCNT. SWCNT has the electrical properties that are not owned by the MWCNT structure. This allows the development of SWCNT structures into nanowires because it can be a good conductor. MWCNT and SWCNT differ from each other in respect of optical properties. If we look forward for chemical structure, MWCNT possess optical properties matched to graphite while SWCNT resembles to carbon [11]. SWCNTs are a hexagonal network of rolled graphene cylindrical tubes of diameter 1 nm with no overlapping edge. Based on different chirality SWCNTs shows semiconducting or metallic nature because of variable bandgap (0–2 eV), this property provides great flexibility to users to use in THz as well as plasmonic applications. When a CNT performs as a conductor, it has very high conductivity up to 1 billion Ampere/cm^2. CNTs have the electrical current density 1000 times greater than metal (e.g., copper, silver). Besides this, a high surface-to-volume ratio and excellent biocompatibility make it more suitable to use in biomolecular detection. If one can choose CNT in biosensing application, then it can provide a very favorable condition because CNT is compatible with physiological cells and tissues Also, it is chemically inert and thermally stable, reusable so cost-effective, and provide very high sensing efficiency. Although some other 2D materials like graphene, black Phosphorus, TMDC significantly contribute to increase the sensitivity of SPR sensor but they have some limitations like bandgap absent in graphene [12] which makes its application limited, TMDC MoS2 have tunable bandgap but low mobility and less stability as a BRE layer and monolayer black phosphorus or phosphorene have a large tunable bandgap in compare to MoS_2 but it is not stable in ambient environment. SWCNTs possess almost the same chemical property sustained by fullerenes and graphene [13, 14]. SWCNTs conserve their electrical properties even in thin transparent films this makes it suitable for the application in optically sensitive transparent films [15, 16]. In this work, we functionalized the proposed SPR sensor with thin layer of single-walled carbon nanotubes to study the interactions of glucose molecules with SWCNT (Tables 1, 2 and 3). We have fixed the range of liquid sample refractive index from 1.3326 to 1.3822, computed by varying glucose concentration (refer to Table 4).

Table 1 Comparative analysis of the performance parameter of different kind of prism working at incident light of 633 nm wavelength

Types of prism	RI	FWHM	θ_{SPR} (RI = 1.3326)	$\Delta\theta$ (Δn = 0.0496)	S (°/RIU)	FoM (RIU$^{-1)}$	DA (deg^{-1})
2S2G	2.358	1.09	37.34	1.89	38.10	34.95	0.917
SF11	1.7786	1.92	53.53	3.41	68.75	63.07	0.52
SF10	1.723	2.11	56.09	3.77	76	36.01	0.47
BK7	1.5151	3.7	70.32	7.89	159.07	42.99	0.27
FK51A	1.4853	4.28	78.25	10.96	220.96	51.74	0.23

Table 2 Optimum values of layer thickness and optical parameter

Type of layer	Optimized thickness	Refractive index
Silver (Ag)	40 nm	0.056206 + 4.2776i
Gold (Au)	2 nm	0.18344 + 3.4332i
Silicon (Si)	1 nm	3.53 + 0.39i
Fe_3O_4	0.5 nm	2.162 + 1.178i
SWCNT	1 nm	2.4015

Table 3 Sensitivity and reflectance curve shift analysis obtained when performing with different models at 633 nm incident light wavelength

Structure arrangement	SPR angle shift	Sensitivity(°/RIU)
Prism + silver metal layer	8.07	162.70
Prism + bimetal	8.43	169.95
Prism + bimetal + Silicon	9.62	193.95
Prism + bimetal + Silicon + Fe_3O_4	9.94	200.40
Prism + bimetal + Silicon + Fe_3O_4 + SWCNT	10.96	220.96

2 Theoretical, Mathematical Overview and Design Consideration

The schematic structure arrangement shown in Fig. 1 is kind of Kretschmann's configuration [17–19] based on the attenuated total reflection (ATR) phenomenon. A TM or P-polarized light incident on a metal-dielectric surface at different angles. At a certain angle (greater than the critical angle) when the wavevector matching condition takes place between incident light and surface plasmon wave a significant dip observed in the reflection intensity curve, this is the essential condition for surface plasmon resonance (refer to Eq. 1). The total reflection of incidence light at boundary causes to generate an evanescent wave that interacts with the plasma wave if the metal has the thickness in the nanometer order. The angle where the maximum dip observed known as the resonance angle θ_{SPR}. More general, in this paper, angle interrogation-based SPR sensing scheme has been followed at a fixed wavelength. Mathematically resonance condition expressed as [20]

$$k_o n_{\text{prism}} \sin\theta_{spr} = Re\{k_o\sqrt{\varepsilon_m\varepsilon_s/(\varepsilon_m+\varepsilon_s)} \tag{1}$$

where $\varepsilon_m and \varepsilon_s$ are the dielectric constants of the metal and the sensing layer, respectively, and $k_0 = {}^{2\pi}/_{\lambda_0}$ is the wavenumber of the incident light vacuum. Interestingly, only materials (Ag, Au, Cu, Al, etc.) having complex refractive index are capable of exhibiting surface plasmons [21]. According to Eq. (1), θ_{SPR} increases with the increase of ε_s, which is related to the sensing gas physical condition like temperature, concentration, pressure, humidity, etc. An SPR curve relies on dip position, peak depth of angle, a width of the curve [22]. The maximum dip in curve refers to

Table 4 Effect of glucose concentration increment on SPR angle obtained through proposed doped and undoped SWCNT-based sensing device

Glucose concentration (g/l)	Refractive index	SPR angle obtained through undoped SWCNT-based structure	Sensitivity (°/RIU)	SPR angle obtained through doped SWCNT-based structure	Sensitivity (°/RIU)
0	1.33230545	73.65372	–	74.22668	–
20	1.33468325	74.0548	152.32	74.57046	154.36
40	1.33706105	74.39857	156.6259	74.97153	156.6259
60	1.33943885	74.79964	160.6415	75.3726	160.6415
80	1.34181665	75.20071	162.6493	75.77367	162.6493
100	1.34419445	75.60178	163.854	76.1747	163.8506
120	1.34657225	76.00285	164.6571	76.57581	164.6571
140	1.34895005	76.46122	168.6733	77.09147	172.1153
160	1.35132785	76.91958	171.685	77.54984	174.6972
180	1.35370565	77.37795	174.0278	78.0655	179.3824
200	1.35608345	77.83632	175.9021	78.52387	180.7213
220	1.35846125	78.29468	177.4352	79.03953	184.007
240	1.36083905	78.81034	180.721	79.61249	188.7533
260	1.36321685	79.32601	183.5016	80.12815	190.9156
280	1.36559465	79.89896	187.6056	80.64381	192.7691
300	1.36797245	80.47192	191.1627	81.15947	194.3755
320	1.37035025	80.98758	192.7691	81.96161	203.3111
340	1.37272805	81.5032	194.1854	82.59187	206.9434
360	1.37510585	82.36268	203.4785	83.56589	218.2038
380	1.37748365	82.93564	205.4513	84.2534	221.9371
400	1.37986145	83.56589	208.4315	85.34206	233.7324
420	1.38223925	84.59722	220.1602	86.31609	244.1088

the minimum intensity and maximum reflection and minimum width of the curve responsible for maximum resolution and highest Signal-to-noise ratio (SNR) [23]. Shifting of SPR angle dip by changing the refractive index of sensing medium, measured by using the proposed sensor. Table 1 includes major design parameters like refractive index, the thickness of the layer for the proposed sensor. In this paper, we have taken the bimetal stack of gold (Au) over silver (Ag) because to take the advantage of gold in terms of stability and prevents Ag to get oxidized, sulfurized while Ag contributes in the sharpness of resonances curve. The term sensitivity (S) [24] characterizes the minimal measurable variation of refractive index, defined as-

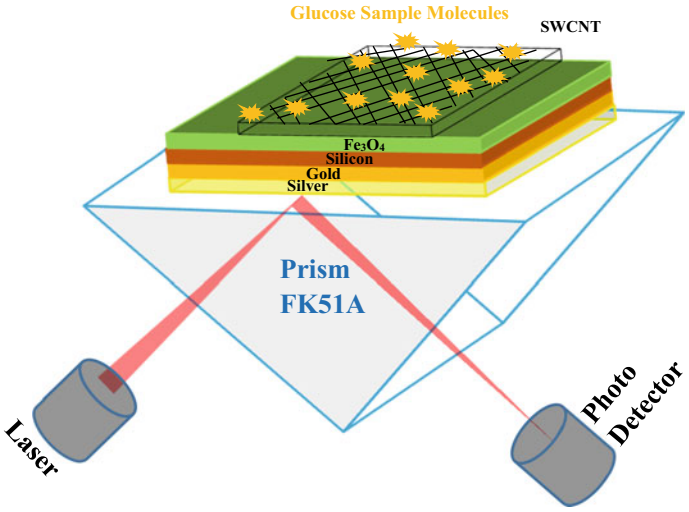

Fig. 1 Proposed SWCNT-based glucose-sensing biosensor

$$S = \frac{\delta\theta_{res}}{\delta n_c} \ (^\circ/\text{RIU}) \tag{2}$$

where $(\delta\theta_{res})$ shift in the SPR angle position and (δn_c) is the change in RI of sensing medium occurring due to abnormality takes place in the physical condition of sensing medium. As mentioned earlier, figure of merit is also a key parameter that affects the sharpness of SPR angle or signal-to-noise ratio. The value of the FoM [25] can be estimated as

$$\text{FoM} = \frac{S}{\text{FWHM}} \ \text{RIU}^{-1} \tag{3}$$

Thus, FWHM must be as least as possible for high FoM and high detection accuracy $\left(\text{DA} = \frac{1}{\text{FWHM}}\right)$ of SPR sensor.

The gold layer-based conventional structure absorbs biomolecules poorly, and this results in poor sensitivity. By applying a thin silicon layer directly over the bimetallic layer, it is observed that the sensitivity enhanced significantly. Existence of dielectric silicon layer enhances the field intensity of the exciting light [26]. In a conventional SPR sensor, the only metal layer is responsible for absorption whereas due to the addition of silicon layer the absorption takes place both in metal as well as silicon layer. This will increase the overall absorption and field intensity as a result excitation of SPs get enhanced [27]. The Fe_3O4 (iron oxide or magnetite) magnetic nanoparticles (MNP) as an active ingredient in SPR biosensors help to quickly detect glucose contents present in the liquid sample [28, 29]. To be applicable in these areas, it is important to consider the particle size, magnetic properties, and surface properties of the nanoparticles themselves. The Fe_3O_4 nanoparticles may

be super-paramagnetic. As a dielectric material, FK51A glass-based prism exhibits excellent performance while used in visible range like negligible dispersion and outstanding transmission characteristics [30]. As an incident light, monochromatic light of wavelength 633 nm is preferred because optical nonlinearity increases at high frequencies. Moreover, at 633 nm, wavelength sensitivity of the sensor is enhanced at a minimal possible Kerr effect. The schematic diagram of the proposed sensing device is given in Fig. 1

3 Result Discussion

(a) Result obtained from Prism + bimetal + Silicon + Fe_3O_4+ SWCNT combination

Prism is a key element for an angle interrogation-based SPR sensor which contributes in to match the wavevector of surface plasmon wave with wavevector of incident light. So to get excellent performance parameter, prism selection must be done carefully. In Fig. 2a–b, an SPR angle comparative study has been given for different prisms in order to get minimum reflectance (Rmin) and maximum resolution. From the results obtained in Fig. 2, we come at an end that FK51A fill the required condition. The wavelength-dependent RI of FK51A glass-prism can be calculated by using Eq. 4 as:

$$n_{\mathrm{FK51A}} = \sqrt{1 + \frac{0.971247817\lambda^2}{\lambda^2 - 0.00472301995} + \frac{0.216901417\lambda^2}{\lambda^2 - 0.0153575612} + \frac{0.904651666\lambda^2}{\lambda^2 - 168.68133}} \tag{4}$$

The design parameters like the optical constant, optimized thickness of each material layer used in the structure are given in Table 2 (Fig. 3).

In Fig. 4, by using different color shift in SPR angle shown for different layer combinations and the major outcomes obtained from simulation put in Table 3.

From a graphical overview given in Fig. 4 and results have put in Table 4, it is concluded that the combination based on Prism + bimetal + Silicon + Fe_3O_4 + SWCNT shows a large shift in SPR angle as well as provides the highest sensitivity up to 220.96°/RIU. Apart from the abovementioned results, the dephasing time (t) also called decay or damping time [31] for each obtained resonance angle is calculated based on FWHM value. The estimation formula is given in Eq. 5, where ħ refer to reduced Plank's constant –

$$t = {}^{2 \times \hbar}/_{FWHM} \tag{5}$$

The dephasing time is calculated as 3.10 fs (femtosecond) when glucose concentration in the water sample is zero or the sample refractive index is 1.3326. It gradually

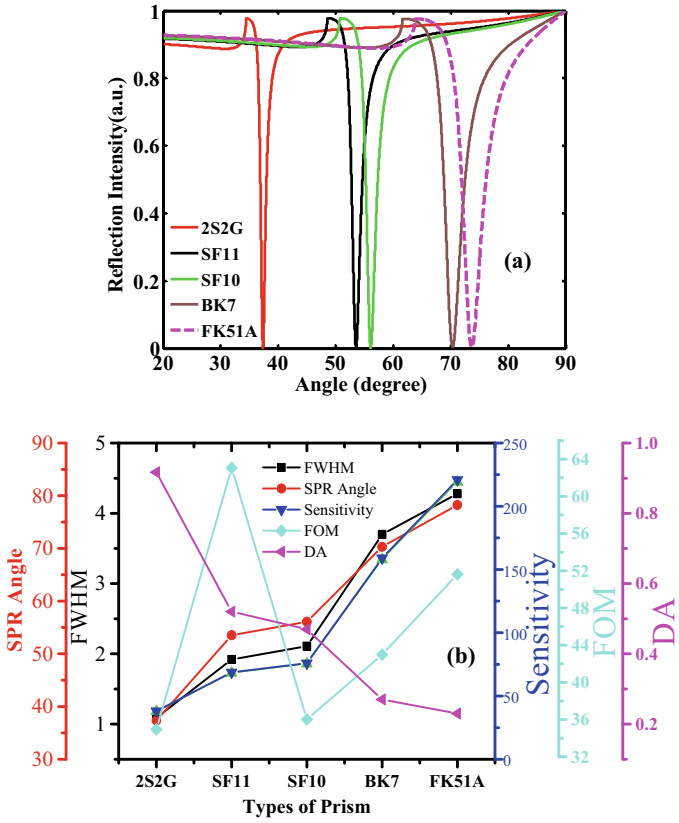

Fig. 2 **a** reflectance curve analysis for different prism applicable in proposed structure, **b** comparison in the performance parameter

decreases to 2.06 fs when glucose concentration reaches to 420 g/l or sample refractive index increases to 1.3822. Obtained values reveal that the proposed SPR sensor has smaller lifetime when glucose concentration reaches to its max value or maximum opted value of refractive index. Longer dephasing time supports high-quality factor and put a positive environment for sensing application.

(b) **Effect of doping in SWCNT**

Doping of SWNTs either with electron donors (alkali metals like Li or Na) or through electron acceptors (halogens) exhibits promising macroscopic properties [32]. Doping also required to change the optical performance of CNT or more generally to control their electronic properties. Hence, this is a way to modulate the properties of SWCNTs as a bulk. Dispersion relation of alkali metal-doped [33, 34] given through Eq. 6 is as follows-

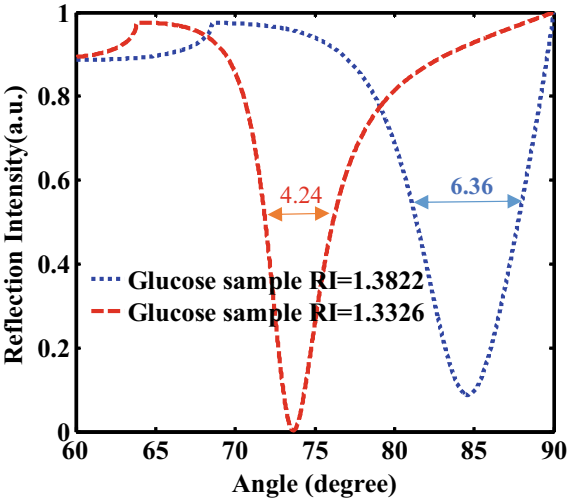

Fig. 3 Shift in SPR angle observed in the proposed sensor by varying the refractive index of liquid glucose sample

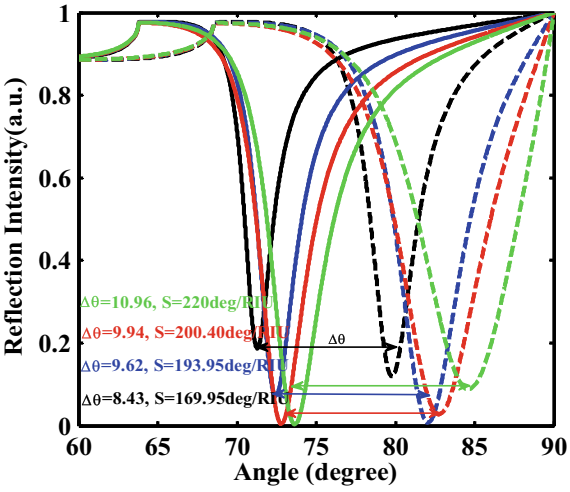

Fig. 4 Comparative study of shift in SPR angle **a** black color graph dedicated for prism + bimetal-based sensing structure, **b** blue color graph for Prism + bimetal + Silicon-based SPR sensor, **c** blue color graph for Prism + bimetal + Silicon + Fe_3O_4 sensing structure, **d** green color graph dedicated for Prism + bimetal + Silicon + Fe_3O_4 + SWCNT sensing structure

$$\varepsilon_{\mathrm{SWCNT}} = 1 - \frac{\lambda^2}{\lambda_{p,0}^2(1 + i\gamma_0\lambda)} + \frac{\lambda^2\lambda_{T,1}^2}{\lambda_{p,1}^2\left(\lambda^2 - \lambda_{T,1}^2 - i\gamma_1\lambda\lambda_{T,1}^2\right)} \tag{6}$$

In expression (6), $\lambda_{p,0} = 0.6702\ \mu\mathrm{m}$, $\lambda_{p,1} = 0.2725\ \mu\mathrm{m}$ are the plasmon wavelengths, corresponds to Drude (intra-band) and Lorentz (inter-band) charge carriers, and $\lambda_{T,1} = 0.2883\ \mu\mathrm{m}$ is the resonance wavelength of the inter-band transition. $\gamma_0 = 0.3226\ \mu\mathrm{m}^{-1}$ and $\gamma_1 = 1.8551\ \mu\mathrm{m}^{-1}$ are damping coefficients, λ is incident light wavelength (0.633 μm in our case).

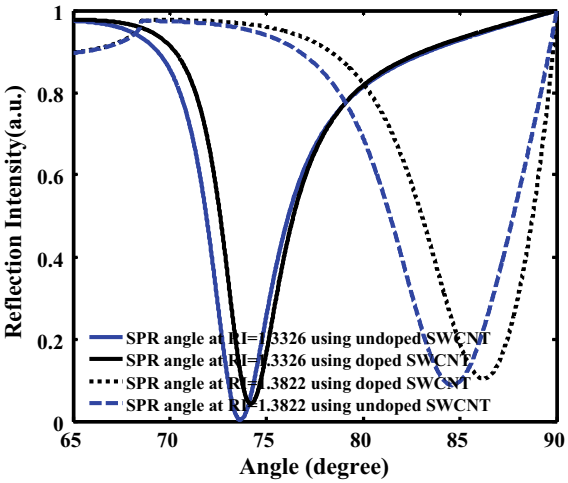

Fig. 5 SPR angle shift comparison between doped SWCNT and undoped SWCNT applied in the proposed sensor

It is observed that by applying the alkali-metal doping, a longer SPR angle shift observed than the previous case (as observed in undoped SWCNT) which leads to enhance the sensitivity of the proposed sensing device. Maximum shift in SPR angle, $\Delta\theta = 12.04$, and sensitivity obtained as 244.75°/RIU which is better than previously observed sensitivity. It is the point to be noted that the optimized layer thickness for the proposed device is Ag = 40 nm, Au = 2 nm, Si = 1 nm, Fe_3O_4 = 1.5 nm, and $SWCNT_{(doped)}$ = 1 nm. In Fig. 5, it appears that the proposed sensing device shows a large shift in SPR angle when functionalized with doped SWCNT.

(c) **Glucose concentration effect on SPR angle and Sensitivity analysis**

In the year 2008, Yen-Liang Yeh [35] developed a system to measure the average refractive indices of liquid sample by varying glucose concentrations from 0 to 200 g/l. A linear relationship or mathematical expression between the average refractive index and glucose concentration obtained through some experimental treatment is given as:

$$n_{g/l} = 0.00011889C + 1.33230545 \tag{7}$$

In this expression, C is the glucose concentration (g/l) and $n_{g/l}$ is the average refractive index. By following Eq. 7, in this study, the analysis is carried out by varying glucose concentration zero (pure water) to 420 g/l.

The corresponding results obtained from glucose concentration variation in liquid sample using undoped as well as doped SWCNT-based SPR sensor is summarized in Table 4. In first sight, results shows that the RI of liquid sample increase by varying glucose concentration Moreover, an increment in SPR angle also observed in both of the sensing structure taken for observation.

The influence of glucose concentration variation on SPR angle obtained both of the cases, when proposed structure functionalized with doped as well as the undoped

SWCNT, is given in Fig. 6b. Sensitivity analysis concerning the surrounding materials discussed with the help of Fig. 6c. This figure indicates the change in sensitivity with respect to change in RI of the sensing medium for the proposed structure. Table 4 depicts the effect of increasing glucose concentration on SPR angle obtained through

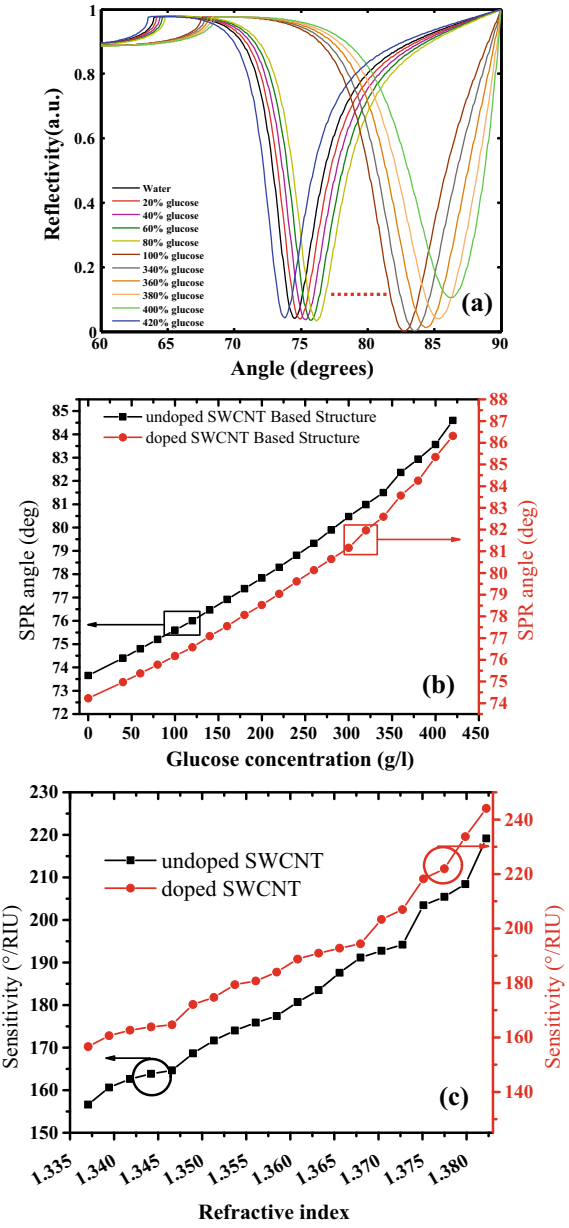

Fig. 6 **a** Shift in SPR angle concerning glucose concentration variation in comparison to normal water sample, **b** effect of glucose concentration variation on SPR angle for proposed sensing structure functionalized with doped as well as undoped SWCNT, **c** sensitivity analysis by varying refractive index obtained from Eq. 7

doped and undoped SWCNT-based sensing devices. Using Eq. 7, refractive index of the liquid sample by varying glucose concentration (g/l) estimated and at each case of refractive index variation the SPR angle observed.

The theoretical study shown in this paper expected to be verified by experimental investigations because materials used in this study are readily available [36], and on the nanometer level, there is a number of experimental papers are available for realization.

4 Conclusion

A theoretical concept of a biosensor for glucose concentration detection in simple water has been studied based on SPR sensing scheme. By measuring the shift in the position of resonance dip of the reflected spectrum due to modulation of the incident light angle, the variation in the refractive index can be monitored. The theoretical study has been carried out by following the structure based on the combination of single-wall carbon nanotube with Fe_3O_4 nanoparticle and silicon. It is observed that the sensing device shows high sensitivity and almost four times better FoM than a conventional SPR sensor. The proposed design of the investigated sensor is really capable and very sensitive for measuring low as well as a wide range of glucose concentrations. We have also shown the doping effect of SWCNT when doped with alkali metal on the performance parameter of the sensor. By applying the suitable formula, the refractive index has been calculated by varying the glucose concentration, and on each variation, the SPR angle and sensitivity analysis also carried out.

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Sensing Range Analysis in Non-Conventional WSNs: MI Communication

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1 Introduction

In conventional media, wireless communication technologies account electromagnetic (EM) waves for signal transmission. The electromagnetic waves experience a high level of attenuation, multi-path effects and interference in non-conventional media. To support the large range communications, the antennas required in this systems must have high-radiation resistance. Thus, in non-conventional media like underground and underwater WSNs, EM wave system is not suitable. To mitigate all these problem in non-conventional media, magnetic induction (MI) based communication technique has used [1–6]. Instead of radiated wave, MI system use non-propagating magnetic field. As MI system exhibits short-range communication, lesser power is required for the reliable transmission and higher security. One more advantage of MI communication is that its design is simple, small and inexpensive and it does not have a issue of multi-path fading because of small proportion of their radiated energy [7]. MI communication has a many application for near field communication system. In MI communication system, transmit and receive antenna are designed as the primary and secondary coil of transformer. In desiging of non-conventional MI system, we have considered the various factors in the analysis which

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includes number of turns in coil loop, water properties, coil size, operating frequency, and coil resistance [8–10].

Wireless MI sensor nodes are deployed in non-conventional media [11–13]. These MI nodes sense and gather the information about the physical objects or process and make them available for the external systems and the networks at sink nodes. In wireless networks, coverage and connectivity play an important role. To how much extent, the deployed network correctly monitor the area of interest is the coverage. It depends on the detection sensing models designed for the sensor nodes. In this paper, we implement the traditional distance based and angular-based sensing models in MI based communication in non-conventional media. This models give the sensing probability based on distance and 3D angle, respectively.

1.1 Motivation

Kumar et.al. [14] have proposed a multi-layer transmitter enabled novel energy model for designing of MI communication based energy efficient non-conventional WSNs. Along with that they developed the layout of MI transceiver based on multi-layer coil structure and four feasible compensation circuits. Sun et al. [15] developed a MI based wave-guide technique that characterizes the bandwidth and path loss of MI system and decreases the high path loss of the system. Further, they analyzed a comparative study on MI system and EM wave system. Sharma et.al. [16] in this paper, they surveyed the MI communications technique for the non-conventional media applications. A comparative analysis in terms of different performance metrics of all existing communication techniques are studied and focused the issue related to information transmission and design of antenna for MI communication for non-conventional media has done. Li et al. [17], in this paper authors have proposed Target Involved Virtual Force Algorithm (TIVFA) for sensor deployment optimization problem and target tracking. The proposed algorithm can increase the coverage and the detection probability and adjust the sensor networks configuration on the basis of the intelligence and the detected targets. Cao et al. [18], in this paper they have focused on resolving the problem associated to deployment of three dimensional (3D) industrial wireless sensor network. Furthermore, this paper has also focused on lifetime, coverage and reliability of industrial wireless sensor network.

1.2 Contribution

In this paper, we have implemented the two sensing models namely the distance based and angular based sensor detection models which will detect the target in 3D space in non-conventional media through MI based communication. The main contributions of this paper are as follows:

1. Mathematical analysis of distance based sensing probability of sensor nodes in MI based communication.
2. Mathematical analysis of angular based sensing probability of sensor nodes in MI based communication.
3. Comparative analysis of these two models for different media like sea water, wet soil and dry soil.

The remainder of this paper are categorized as follows: In Sect. 2, two sensing models in MI non-conventional WSN has been explained. Results and analysis of the proposed model are presented in Sect. 3. Lastly, Sect. 4 concludes the paper.

2 Sensing Models in MI Based Non-Conventional Media

The traditional sensing models are implemented to an individual sensor. In 3D space, a sensor attempts to observe a target. There is clear line of sight between them when there is no obstacle. And thus a sensor and target can see each other. Otherwise, we say that Non line of sight exists. Thus, the important condition for sensor to detect the target is line of sight. The line of sight function can be represented in following [18] form

$$P^S_{\text{LOS}}(s,t) = \begin{cases} 1, & if\ LOS \\ 0, & if\ NLOS \end{cases} \tag{1}$$

The sensing probability that a sensor can sense is calculated using the following formula,[18]

$$P^S(s,t) = P^S_{\text{LOS}}(s,t) P^S_D(s,t) P^S_H(s,t) P^S_V(s,t) \tag{2}$$

where $P^S_D(s,t)$ is the sensing probability of sensing distance, $P^S_H(s,t)$ is the sensing probability of horizontal sensing angle and $P^S_V(s,t)$ is the sensing probability of vertical sensing angle. Here, we have considered the effect of different media. The following expressions represent the attenuation factor, skin depth in sea water and soil media.

$$G = e^{\frac{-r}{\delta}} \tag{3}$$

where r is the distance between transmitter and receiver. For sea water, formula for skin depth is given as,

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \tag{4}$$

For dry and wet soil, formula for skin depth is given as,

$$\delta = \frac{1}{2\pi f \sqrt{\frac{\mu\varepsilon}{2}\left(\sqrt{1+\left(\frac{\sigma}{2\pi f\varepsilon}\right)^2}\right)-1}} \tag{5}$$

where μ is permiability of free space, σ is the conductivity of medium, ε is the permittivity of free space, δ is the skin depth of the media and f is the frequency of operation.

2.1 Distance Based Sensing Model

In distance based sensing model, we have considered the deterministic distance denoted by D_r and an uncertain distance denoted by D_f. The mathematical formulation for the sensing probability in non-conventional media through MI based communication is given as follows [18],

$$P_D^S(s,t) = \begin{cases} 1, & d(s,t) \in [0, D_r] \\ e^{-\gamma_1 G d_1^{\beta_1}/d_2^{\beta_2}}, & d(s,t) \in (D_r, D_r + D_f) \\ 0, & d(s,t) \in [D_r + D_f, +\infty] \end{cases} \tag{6}$$

where,

$$d_1 = d_{s,t} - D_r \tag{7}$$

$$d_2 = D_r + D_f - d_{s,t} \tag{8}$$

where $d(s,t)$ is the distance between sensor and target. γ_1, β_1, β_2 are the distance sensing model parameters. By adjusting their values, we can simulate the sensors with various characteristics.

2.2 Angular-Based Sensing Model

We have considered the two angular sensing dimensions as vertical angular range and horizontal angular range. We can formulate the sensing probability of any 3D angle on the basis of the sensing probability with respect to these two sensing angles. For both the models, the sensing behavior remains same. The three threshold angles that are considered in this work are α_1, α_2 and α_3 such that,

$$\alpha_1 < \alpha_2 < \alpha_3 \tag{9}$$

The model in non-conventional media is as follows,

$$P_A^S(s,t) = \begin{cases} 1, & \phi_A(s,t) \in [0, \alpha_1] \\ 1 - Gv^A e^{1-\left(\frac{\alpha_2 - \alpha_1}{\phi_A(s,t) - \alpha_1}\right)^{t_1^A}}, & \phi_A(s,t) \in (\alpha_1, \alpha_2] \\ G\tau^A e^{1-\left(\frac{\alpha_3 - \alpha_2}{\alpha_3 - \phi_A(s,t)}\right)^{t_2^A}}, & \phi_A(s,t) \in (\alpha_2, \alpha_3) \\ 0, & \phi_A(s,t) \in [\alpha_3, +\infty) \end{cases} \tag{10}$$

$$\phi_A(s,t) = \mid (dt_A \times \psi_A(s,t)) \mid \tag{11}$$

where, $\psi_A(s,t)$ is the deflection angle and $\phi_A(s,t)$ is its modified value with modification ratio dt_A. v, τ, t_1^A and t_2^A are the angle sensing model parameters.

3 Results and Analysis

In this paper, the MI sensors are deployed in 3D space. We have implemented the two sensing models namely the distance based and angular-based sensor detection models in non-conventional media. Mathematical analysis of the equations given above are

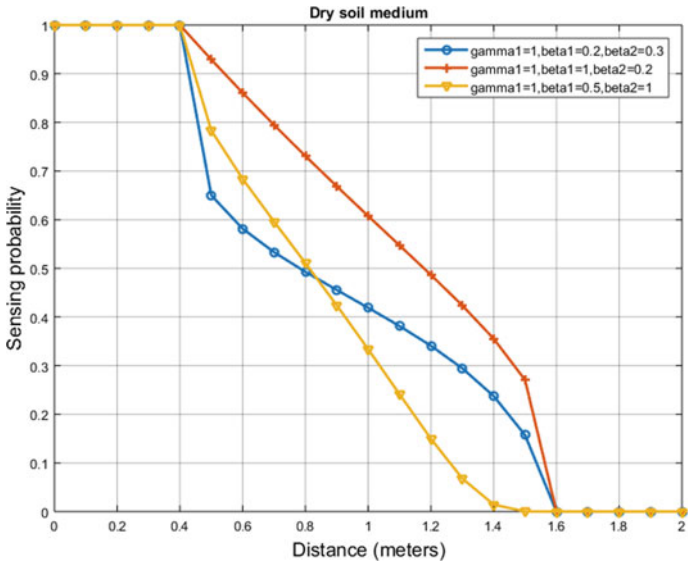

Fig. 1 Comparitive analysis of sensing probability versus distance (dry soil)

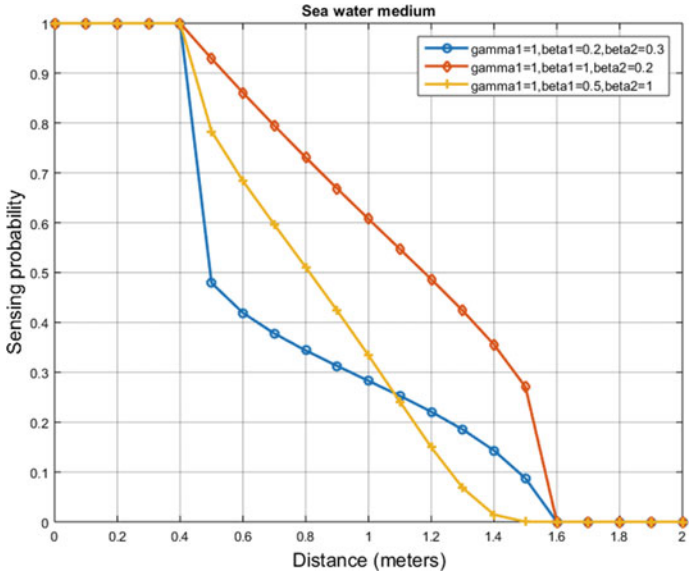

Fig. 2 Comparitive analysis of sensing probability versus distance (sea water)

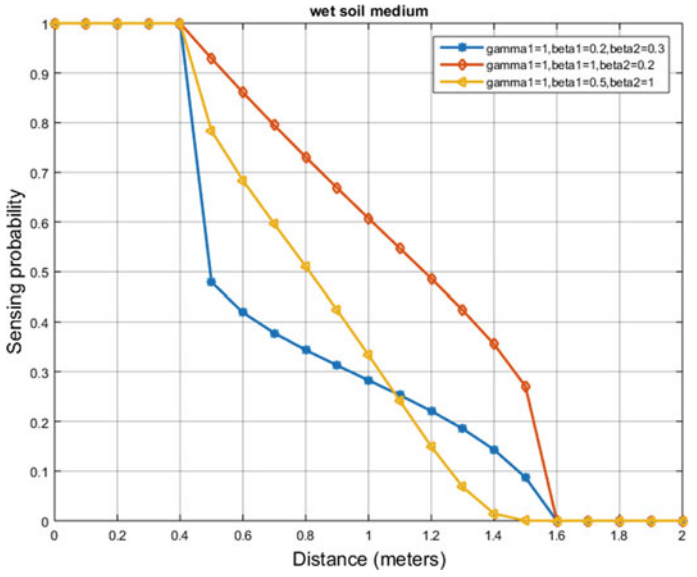

Fig. 3 Comparitive analysis of sensing probability versus distance (wet soil)

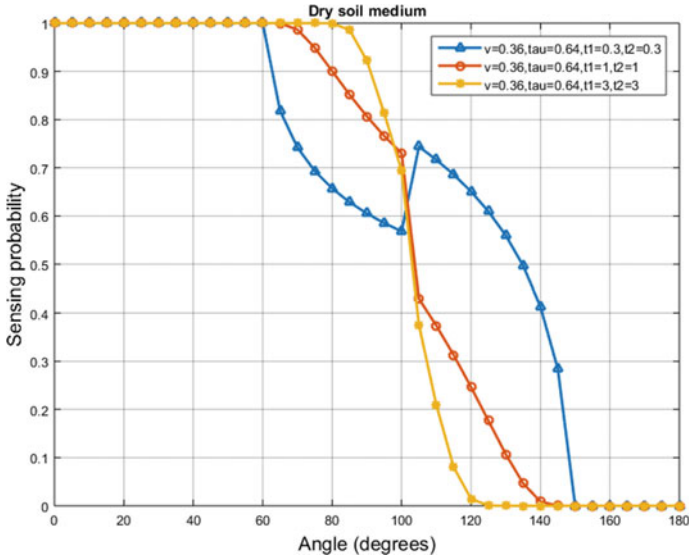

Fig. 4 Comparitive analysis of sensing probability versus angle (dry soil)

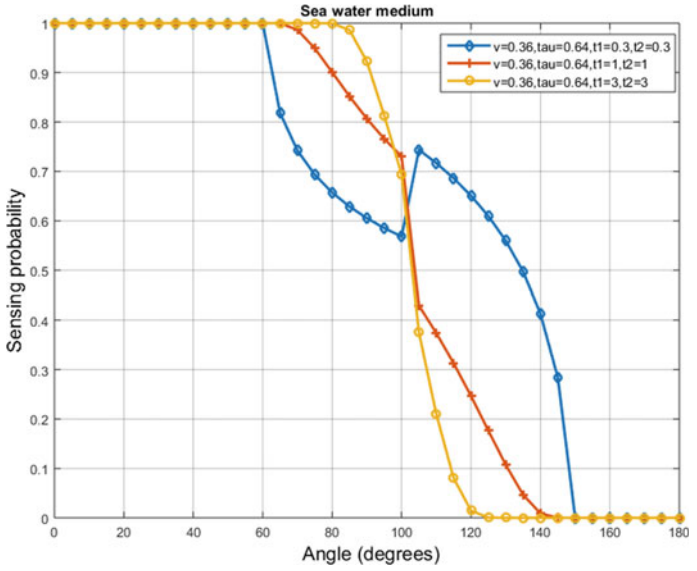

Fig. 5 Comparitive analysis of sensing probability versus angle (sea water)

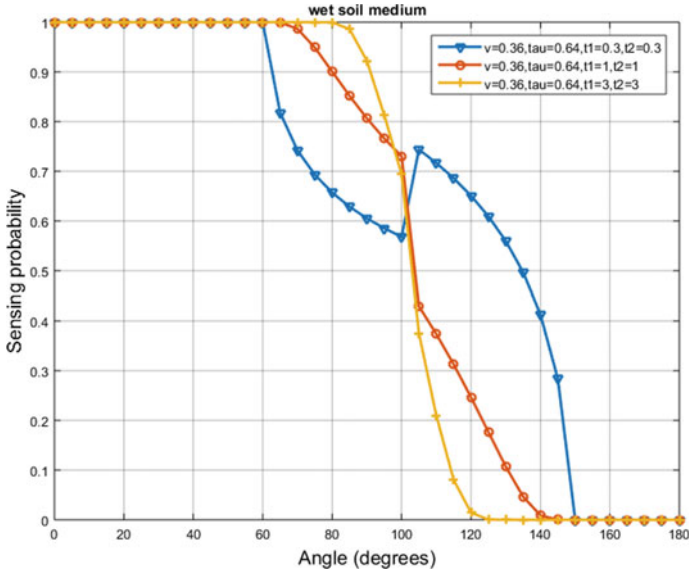

Fig. 6 Comparitive analysis of sensing probability versus angle (wet soil)

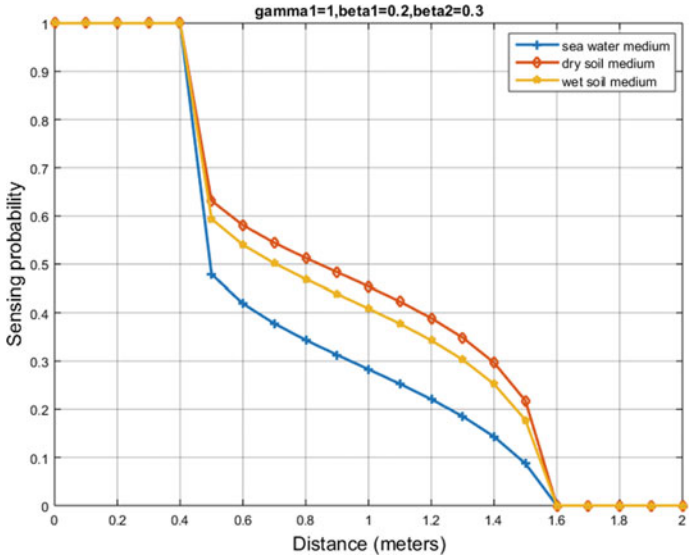

Fig. 7 Sensing probability versus distance in three media

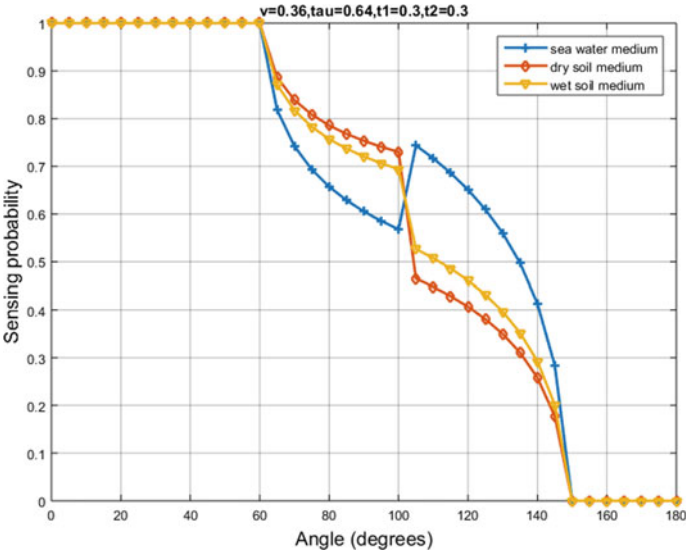

Fig. 8 Sensing probability versus angle in three media

performed in MATLAB R2016a from MathWorks at frequency 1 KHz. Besides, a comparative analysis of the two sensing models is done for different media (sea water, wet soil and dry soil). From Figs. 1, 2, 3, 4, 5, 6, 7 and 8 it can be inferred that for the three considered media, dry soil medium shows a good performance in terms of sensing probability with respect to distance and angle. Because, the skin depth is the inverse function of the conductivity of medium, i.e., as the conductivity of medium increases, skin depth of the respective medium decreases gradually. The conductivity of DS medium is less in compare to other like, sea water and wet soil so wireless propagation through this media attenuate less and propagate more distance in that media. It is observed that the sensing probability is the highest in dry soil. The sensing probability is the lowest in sea water.

3.1 Distance Based Model

A distance based model is applied for individual sensor nodes to different media like sea water, dry soil and wet soil. The probability of sensing is evaluated for different distance sensing parameters γ_1, β_1 and β_2. These are measuring detection probability parameters. The values of deterministic distance and fuzzy distance are kept constant for all media. In dry soil medium, for 1 m measuring distance, the sensing probability is 0.6 for parameters $\gamma_1 = 1$, β_1=1, $\beta_2 = 0.2$. It is 0.42 for $\gamma_1 = 1$, β_1=0.2, β_2=0.3 and for parameters $\gamma_1 = 1$, β_1=0.5, β_2=0.1, the sensing probability is 0.33.

Table 1 Parameters settings for models

Symbol	Quantity	Symbol	Quantity
γ_1,β_1,β_2	(1,1.5,1)	$\alpha_1,\alpha_2,\alpha_3$	(60,100,150)
D_r	1	t_1^A,t_2^A	(3.6,3.6)
D_f	0.6	v^A,τ^A	(0.5,0.5)

3.2 Angular Based Model

Like distance based model, angular-based model is also applied to individual sensor nodes. The model is applied to different media like sea water, wet soil and dry soil. We have considered the horizontal and vertical angular sensing dimensions. Different angular sensing model parameters are considered in this model. In dry soil medium, for measuring the target in an angle of 80°, the sensing probability is 1 for parameters $v = 0.36$, $\tau = 0.64$, $t_1 = 3$ and $t_2 = 3$. Similarly, it is 0.9 for $v = 0.36$, $\tau = 0.64$, $t_1 = 1$, $t_2 = 1$ and for $v = 0.36$, $\tau = 0.64$, $t_1 = 0.3$, $t_2 = 0.3$ the sensing probability is 0.744.

Angular based model exhibits better performance for the angle below 100° and for the parameters $v = 0.36$, $\tau = 0.64$, $t_1 = 3$, $t_2 = 3$ and similarly, for the angle above 100° and for the parameters $v = 0.36$, $\tau = 0.64$, $t_1 = 0.3$, $t_2 = 0.3$ (Table 1).

4 Conclusion

In this paper, we have implemented the two detection models namely, distance based and angular-based sensing models to detect the target in 3D space more precisely in MI based communication in non-conventional media (dry soil, sea water and wet soil). The individual sensing model has great impact on the sensor network detection and coverage. From the analytical results, we observe that the implemented model performs the best for certain sensing parameters of the model.

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Design and Analysis of Bulk-Driven Linear Voltage-Controlled Oscillator

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1 Introduction

In the present digitalized world, the analog-to-digital conversion (ADC) has become an overriding constraint, so the analog blocks need to be efficient enough to produce the required digital outputs accordingly. One of such analog blocks is voltage-controlled oscillator, and it brings linearity between the input voltage of the analog signal and the oscillation frequency of the output signal. Generally, voltage-controlled oscillator is used in several applications such as phased-locked loop (PLL) and frequency synthesizers. The performance of analog circuits is reduced because of shrinking supply voltages and transistor parameters while achieving low power dissipation [1, 2]. As the trend is moving towards architecture that uses digital blocks, new architectures are needed to replace traditional analog circuits. So, VCO-based ADCs use VCO as quantizer which replaces analog comparators, and output of VCO is encoded to digital output using frequency to digital converter (FDC) [3, 4]. Designers have introduced several methodologies to reduce the distortions and to maintain the linearity between voltage and frequency such as current-starved VCO control voltage given to NMOS, current-starved VCO control voltage given to PMOS, diode connection PMOS and diode connection NMOS transistor [5–7]. However, current-starved PMOS has high linearity along with high power consumption. NMOS diode VCO has low power consumption with less linearity.

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This paper is arranged as follows, and the introduction is the part of the Sect. 1. Section 2 presents the literature review on various voltage-controlled oscillators. Section 3 consists of the proposed novel architecture VCO with bulk driver. Section 4 has the comparative results of different methodologies. Section 5 concludes the paper followed by references.

2 Literature Review

In this section, literature survey of various linear VCOs has been presented. VCO is classified into different types based on the elements present in the circuit such as LC VCO and ring oscillator-based VCO. LC VCO is not preferable because of low quality factor due to losses of silicon substrate and large chip area. Ring VCO is widely preferred as it is easily integrable, CMOS compatible, has compact design and consumes low power. Frequency of oscillation can be calculated as $f = 1/(2 * N * t_d)$, where N is the number of stages, and t_d is propagation delay of each stage [8, 9].

2.1 Current-Starved NMOS VCO

Shruti suman et al. have proposed current-starved VCO to overcome the problem of using voltage as the controlling element. The output frequency is not stable when it is dependent on supply voltage. This is made stable by supplying current to each inverter instead of VDD control. The amount of current available to charge or discharge the capacitive load of each stage present in the ring oscillator is controlled. The structure has additional PMOS and NMOS transistor acting as current tuning circuits along with the basic CMOS inverter [10]. However, it has very less tuning range from 0.5 to 0.7 V.

2.2 Current-Starved PMOS VCO

In current-starved PMOS VCO, control input is given to extra PMOS. As, the aspect ratio is more for PMOS than NMOS, the resistance is low for PMOS since on resistance is indirectly proportional to aspect ratio. So, the linearity between input voltage and supply current to each inverter is proportional to output frequency. Hence, the linearity increases between the input voltage and the output frequency [4]. The tuning range is more than the current-starved PMOS design, and tuning range is from 0.1 to 1.1 V.

2.3 NMOS Diode VCO

Panda M. et al. proposed a diode connection VCO. Additional NMOS transistor is connected as a diode that is the gate terminal is connected to the drain terminal of transistor. The control input is given to additional PMOS. NMOS is in diode connection and thus acts as constant current source, and it is in saturation region. So, current is directly proportional to the square of voltage which is nonlinear [11]. This configuration degrades the linearity between the input and output, and the design has very less tuning range which is in between 0.1 and 0.6 V.

2.4 PMOS Diode VCO

The transistor PMOS added is in diode connection, and the control input is given to the supplementary NMOS transistor. NMOS is in diode connection; nonlinear relation exists between the voltage and current. It reduces linearity between the input and output. PMOS transistors are connected in stack which provides more resistive path and thus degrades the tuning range (0.2–0.4 V).

3 Proposed Circuit

Both current-starved PMOS, NMOS designs and diode connection PMOS, NMOS designs are having inadequate tuning range, along with the less linearity and high-power dissipation. However, these circuits are not suitable for the low-power and high-frequency application. In this section, we proposed a novel circuit for low-power and high-frequency applications. The proposed design has two controlled voltages, V1 has connected to the stacked PMOS transistor, and $V2$ is connected to the stacked NMOS transistor. In addition to that, bulk bias techniques have been applied to proposed designs. Thus enhances the drain current in the transistors based on the control voltage and further it improves tuning range. Hence, the linearity increases between the input control voltage and output frequency.

In general, the bulk and source terminals of a transistor connected together in order to maintain constant threshold voltage. Variable threshold voltage can be achieved by the reverse bulk bias (RBB) and forward bulk bias (FBB). Reverse bulk bias can be attained by additional voltage which is greater than the supply voltage applied to the body terminal of PMOS transistor. In case of NMOS, additional negative voltage is applied to body terminal, and forward bulk bias can be achieved by the vice versa [12, 13]. This causes changes in depletion width which changes threshold voltage of the transistor.

Small gate input-controlled voltage is enough to form the inversion layer and thus increases the linearity between the input control voltage and output frequency.

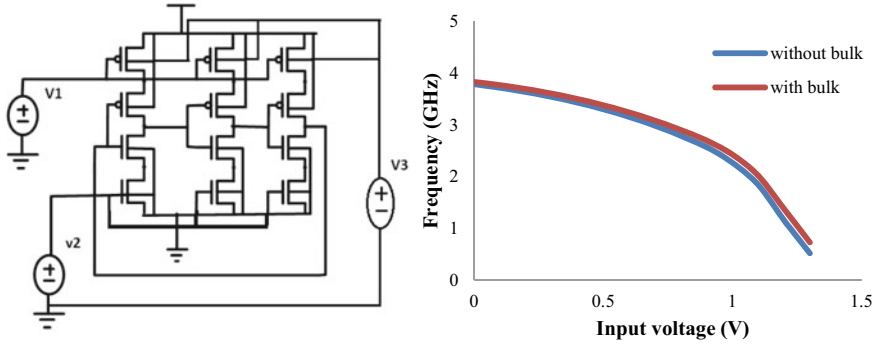


Fig. 1 **a** Proposed design with bulk driver and **b** frequency response

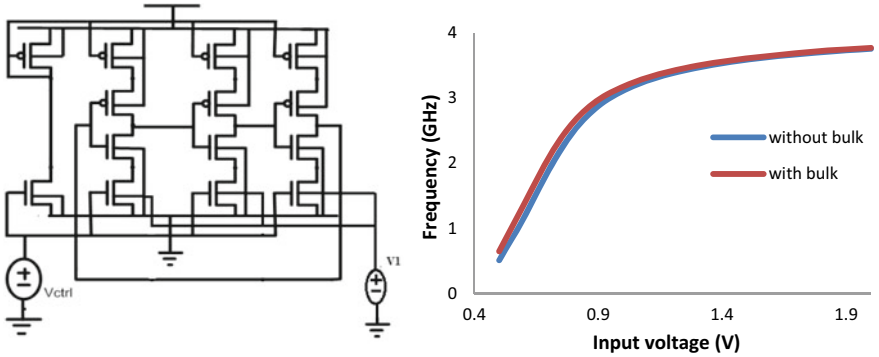
Simulation analysis shows that the bulk bias techniques applied to the voltage control oscillator attained the increase in tuning range along with the high linearity [14]. VCO circuit has basic CMOS inverter (M1 PMOS and M2 NMOS) along with the additional PMOS M3 and NMOS M4. The same cycle repeats for odd number of stages for obtaining the oscillations. In the proposed design, the pull-up network stacked PMOS transistor is biased with the control voltage ($V3$) of 1.6 V. The proposed bulk driver VCO is as shown in Fig. 1a. The frequency response of the proposed design with and without bulk driver is as shown in Fig. 1b.

3.1 Current-Starved NMOS VCO with Bulk Driver

In the current-starved NMOS circuit, bulk bias is provided to pull down network. Body terminal of stacked NMOS is biased with an additional control voltage of 0.2 V. The forward bulk bias decreases the threshold voltage of NMOS transistor. Further, pull down network increases the linearity in between input voltage and output frequency as compared to basic current-starved NMOS design. Modified architecture of current-starved NMOS VCO with bulk driver is shown in Fig. 2a. The frequency response of current-starved NMOS with and without bulk driver is shown in Fig. 2b.

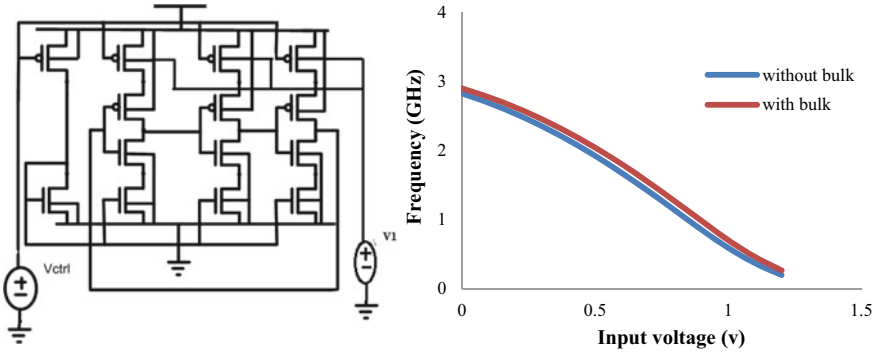
3.2 Current-Starved PMOS VCO with Bulk Driver

Bulk bias is applied to the current-starved PMOS circuit, and the pull up network PMOS body terminal is biased with a voltage of 1.6 V which increases the threshold voltage of PMOS transistor. Hence, operational frequency window increased



(a) (b)

Fig. 2 **a** Bulk driver current-starved NMOS circuit and **b** frequency response



(a) (b)

Fig. 3 **a** Bulk driver current-starved PMOS circuit and **b** frequency response

compared to the current-starved PMOS design. Improved architecture of current-starved PMOS VCO with bulk driver is shown in Fig. 3a. The frequency response of current-starved PMOS with and without bulk driver is shown in Fig. 3b.

3.3 NMOS Diode VCO with Bulk Driver

In NMOS diode connection VCO, bulk bias is provided to the pull up network. Body terminal is biased with a voltage of about 1.6 V which moderates threshold voltage of NMOS transistor. Hence, linearity between input control voltage and output frequency has been increased without affecting the phase noise and low power

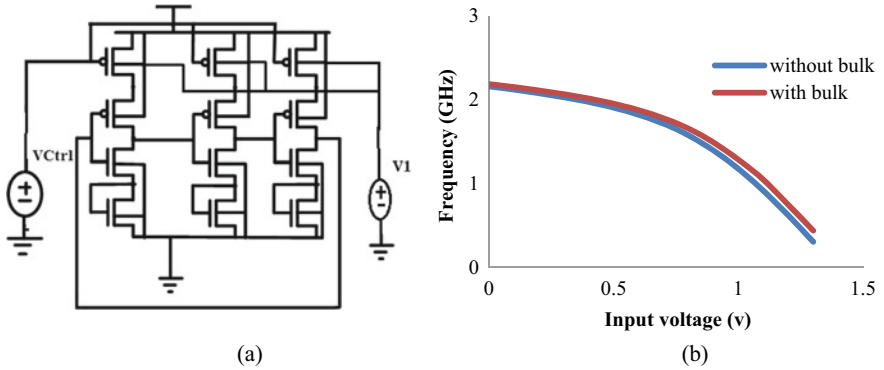


Fig. 4 **a** NMOS diode VCO with bulk driver circuit and **b** frequency response

dissipation as compared to the basic NMOS diode connection VCO. Improved architecture of NMOS diode VCO with bulk driver is shown in Fig. 4a. The frequency response of NMOS diode VCO with and without bulk driver is shown in Fig. 4b.

3.4 PMOS Diode VCO with Bulk Driver

In PMOS diode connection design, bulk bias is provided to the pull down network that is the body terminal is biased with a voltage of 0.2 V which led to decrease in threshold voltage of PMOS, the linear frequency window increased, and phase noise and power dissipation are moderately increased as compared to the case without bulk bias. Architecture of PMOS diode VCO with bulk driver is shown in Fig. 5a. The

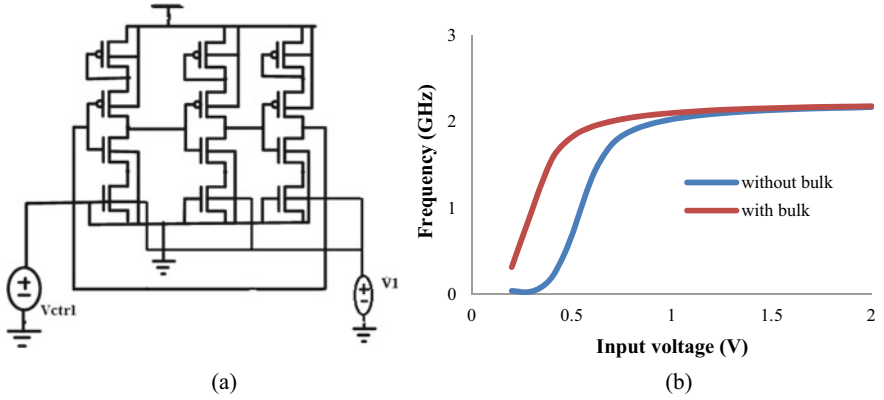


Fig. 5 **a** PMOS diode VCO with bulk driver circuit, **b** frequency response

frequency response of PMOS diode VCO with and without bulk driver is shown in Fig. 5b.

4 Comparative Results

In this section, comparative simulations have been shown for the current-starved PMOS and current-starved NMOS with and without bulk driver, PMOS diode, NMOS diode with and without bulk driver and proposed design with and without bulk driver mainly in terms of tuning range, linearity, power dissipation and phase noise. Simulations have been carried out using the cadence virtuoso 130 nm TSMC technology with the supply voltage of 1.8 V. Similar aspect ratio has been followed for all the CMOS inverters, in which NMOS width is twice the length of a transistor and PMOS width is twice the NMOS width in order to maintain equal rise and fall time. Odd number of inverters is connected to obtain the oscillations. External bulk bias has been applied to obtain the maximum linearity without affecting the phase noise. Parametric analysis has been performed by varying the input control voltage from 0 to 3 V [15]. Further, input control voltage is selected at high linearity without affecting the phase noise. Parametric analysis of input voltage for proposed VCO is as shown in Fig. 6. Phase noise is calculated by following the transient, pss and pnoise analysis. Phase noise response of the proposed design with and without bulk driver is as shown in Fig. 7. It shows that phase noise (dBc/Hz) of bulk driver designs is nearly equal to the circuits without bulk driver designs [16, 17].

In addition to that, power consumption of each design has been calculated using transient and DC analysis for dynamic and static power dissipation. Power consumption slightly increases for the bulk driver circuit due to external driver voltage and

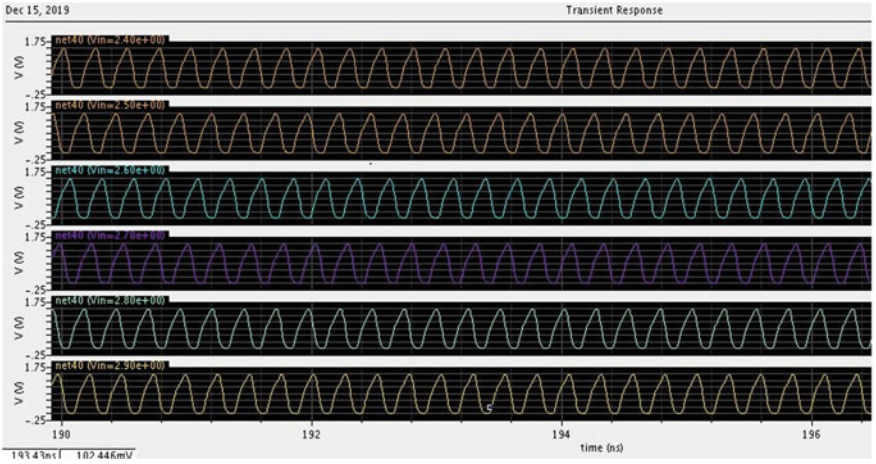


Fig. 6 Parametric analysis of input voltage for proposed VCO

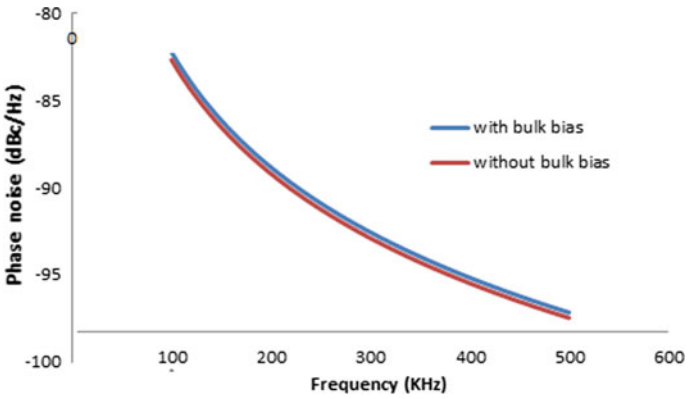


Fig. 7 Phase noise response of the proposed VCO

variation in threshold voltage of the transistor [18]. Tuning range, linearity, power dissipation and phase noise of the various methodologies without and with bulk bias are listed in Table 1. Moreover, the proposed design significantly increases tuning range, linearity between input voltage and oscillation frequency while maintaining the low power consumption and phase noise as compared to other current-starved and diode connection VCO.

5 Conclusion

In this paper, brief literature review of VCO with the current-starved PMOS, current-starved NMOS, diode connection NMOS, diode connection PMOS is discussed in terms of linearity, tuning range, power dissipation and phase noise. Further, we introduced bulk driver to these circuits in order to obtain high linearity while retaining the same low power dissipation and phase noise. In addition, we proposed a highly linear voltage-controlled oscillator expending the bulk driver and additional control input. Each design is simulated, and the frequency response versus input voltage is shown in the figures. Further, tuning range, linearity, power dissipation and phase noise for all the designs have been calculated and presented in tabulation. However, current-starved PMOS has high linearity along with high power consumption. NMOS diode VCO has low power consumption with less linearity. Hence, the proposed design increased the tuning range, high linearity while maintaining the same low power and phase noise. The proposed circuit attained high tuning range from 0.1 to 0.8 V and linearity range from 2.797 to 3.786 GHz. On employing bulk bias, the rate of increase in operational frequency window is far greater in comparisons with the rate of increase in power consumption of the circuit without bulk bias. So, the proposed design can be used for applications of L and S band like RADARS, GPS, aircraft surveillance, communication satellites, etc. The linearity range increased from MHz to GHz, so

Table 1 Tuning range, linearity, power dissipation and phase noise of the various methodologies without and with bulk bias

Methodology	Tuning range (V)		Linearity range (GHz)		Power consumption (mW)		Phase noise (dBc/Hz)	
	Without bulk driver	With bulk driver	Without bulk driver	With bulk driver	Without bulk driver	With bulk driver	Without bulk driver	With bulk driver
Current-starved (NMOS)	0.5–0.7	0.5–0.8	0.50–1.89	0.65–2.63	1.564	1.567	−98.45	−97.31
Current-starved (PMOS)	0.1–1.0	0.1–1.1	0.367–2.69	0.70–2.77	0.979	0.989	−95.34	−94.89
NMOS diode	0.1–0.6	0–0.7	1.81–2.16	1.78–2.15	0.268	0.274	−98.89	−99.06
PMOS diode	0.2–0.4	0.4–0.7	1.34–1.74	0.32–1.56	0.565	0.944	−98.87	−105.6
Proposed design	0.1–0.8	0–0.9	2.79–3.79	2.69–3.83	0.349	0.609	−94.53	−94.1

designs have several other short-range applications like wireless microphones, RFID systems merchandise, baby monitors and wireless doorbells.

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Comparative Analysis of Decimal Fixed-Point Parallel Multipliers Using Signed Digit Radix-4, 5 and 10 Encodings

Debaprasad Ghose, Dharamvir Kumar, and Manoranjan Pradhan

1 Introduction

Since the introduction of IEEE 754-2008 standard for floating point arithmetic, many researchers have put their effort in the area of decimal arithmetic hardware circuit design and implementation [1]. It is also justified as it finds applications in financial, banking, scientific, stock market and other important fields. Also, some processors have dedicated hardware unit for decimal arithmetic like eServer, POWER6, z10 processor, etc. [2–4]. Decimal arithmetic is getting attention because of the inefficiency of binary number system to perform decimal number calculations, e.g. 0.2 decimal number cannot be represented exactly in binary number system.

Multiplication is one of the most commonly used operations in the application areas mentioned above. When decimal multiplication is performed with binary arithmetic-based hardware, it becomes more complex to design, and it also lowers the speed. This happens because in decimal multiplication more number of multiplicand multiples (MM) are required [1] and also because of the inefficiency of binary number system already mentioned.

Basically, the decimal multiplication process requires three steps as follows:

1. Partial products (PPs) generation.
2. Reduction of partial products into two operands.
3. The calculation of final product by a carry propagation addition.

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In this paper, we perform a comparative analysis between 16-digit (64-bit) decimal fixed-point multipliers based on SDR-4, 5 and 10 encodings. Fixed-point multipliers are used to design floating point multipliers [5, 6]. For producing the MM, minimally redundant radix schemes are used for each of the three cases. For recoding of the multiplier, one-hot encoding is used. For reduction of partial products (PP), a reduction tree scheme based on binary-coded decimal (BCD) 4221 format is used [7, 8].

In rest of the paper, Sect. 2 describes the methods for efficient implementation of decimal fixed-point parallel multipliers, Sect. 3 shows the results obtained, and Sect. 4 presents conclusion.

2 Method

2.1 Generation of Multiplicand Multiples

The multiplicand (P) and multiplier (Q) are assumed to be unsigned decimal integer having p-digits. Hence, we can write

$$P = \sum_{i=0}^{d-1} P.10^i \tag{1}$$

And

$$Q = \sum_{i=0}^{d-1} Q_i.10^i \tag{2}$$

Figure 1 shows that for obtaining the multiple $2P$, a left shift of 1-bit is done after recoding the digit from BCD-4221 to BCD-5211. Multiple $3P$ is obtained by a carry propagate BCD addition of multiples P and $2P$. The latency of the partial product generation for the SD radix-10 scheme follows the path of $3P$. The $5P$ multiple is obtained by 3-bit left shift of the 4221 recoded multiplicands, with resultant digits coded in BCD-5211. Then, a digit recoding from BCD-5211 to BCD-4221 is performed. Decimal multiple $8P$ is obtained by 2 * $4P$. The second *2 operation is again computed by a digit recoding from BCD-4221 to BCD-5211 followed by a 1-bit left shift [5, 8, 9].

The multiples for the negative digits are obtained by inverting the corresponding positive multiples. SDR-4 uses the set of different multiples such as $\{-2P, -P, 0, P, 2P, 4P, 8P\}$, SDR-5 uses multiples that are $\{-2P, -P, 0, P, 2P, 5P, 10P\}$, and SDR-10 requires the set of decimal multiples such as $\{-5P, -4P, \ldots, 0, \ldots, 4P, 5P\}$ as shown in figure below.

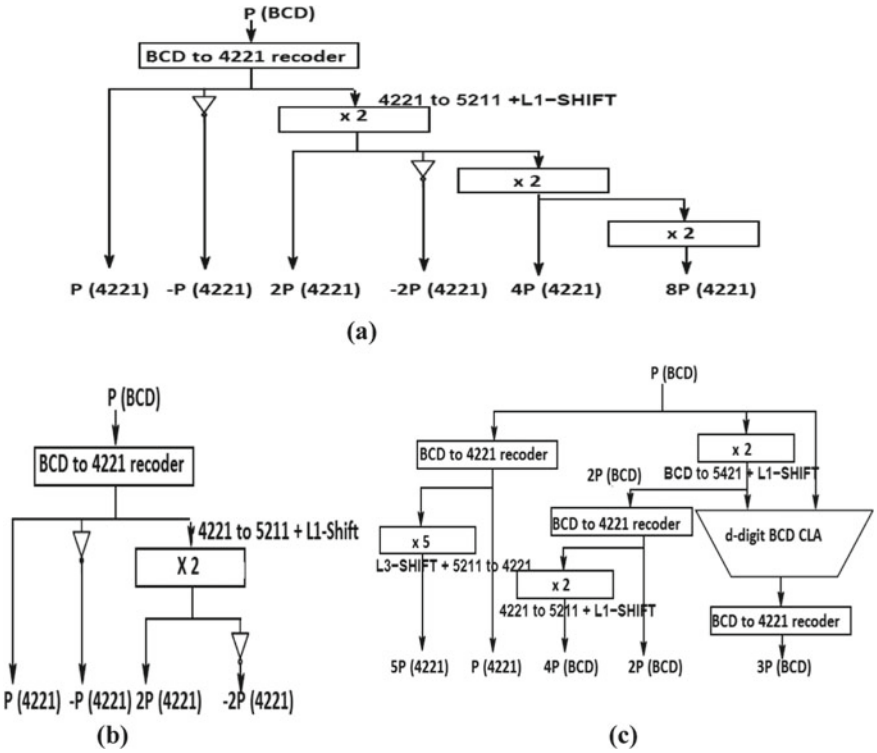

Fig. 1 Multiplicand multiples calculation for **a** SDR-4, **b** SDR-5, **c** SDR-10

2.2 Multiplier Recoding

By using this recoding technique, each BCD digit of decimal number, Q, is coded into two digits $\mathbf{Q_i^U} \in \{\mathbf{0}, \mathbf{1}, \mathbf{2}\}$ (upper part) and $\mathbf{Q_i^L} \in \{-\mathbf{2}, -\mathbf{1}, \mathbf{0}, \mathbf{1}, \mathbf{2}\}$ (lower part) such that $\mathbf{Q_i} = \mathbf{Q_i^U} \cdot \mathbf{4} + \mathbf{Q_i^L}$. The computation of decimal multiples such as $4P$ and $8P$ requires two times and three times latency as compared to the computation of $2P$. Multiples ($+4P$, $-4P$, $+8P$, $-8P$) are selected by upper signals, and multiples ($-2P$, $-P$, $+P$, $+2P$) are selected by lower signals. This recoding scheme, two radix-5 digits $\mathbf{Q_i^U} \in \{\mathbf{0}, \mathbf{1}, \mathbf{2}\}$, $\mathbf{Q_i^L} \in \{-\mathbf{2}, -\mathbf{1}, \mathbf{0}, \mathbf{1}, \mathbf{2}\}$ are produced per BCD digit ($\mathbf{Q_i} = \mathbf{Q_i^U} \cdot \mathbf{5} + \mathbf{Q_i^L}$). This recoding scheme transforms a BCD digit $\mathbf{Q_i} \in \{\mathbf{0}, \mathbf{1}, \ldots, \mathbf{8}, \mathbf{9}\}$ into a SDR-10 digit $\mathbf{Qb_i} \in \{-\mathbf{5}, \ldots, \mathbf{5}\}$. The value of $\mathbf{Qb_i}$ depends on the value of $\mathbf{Q_i}$ and on a signal $\mathbf{q_{i-1,3}}$ (sign) that indicates whether $\mathbf{Q_{i-1}}$ is greater than or equal to 5. Thus, the z-digit BCD multiplier Q is recoded into $(z + 1)$-digit SDR-10 multiplier $\mathbf{Q_b} = \sum_{\mathbf{i=0}}^{\mathbf{z}} \mathbf{Qb_i 10^i}$ with $\mathbf{Qb_z} = \mathbf{qs_{z-1}}$ [5].

2.3 Partial Product Generation

All the schemes generate PPs in parallel. The MMs are produced in a faster way in case of SDR-4 and SDR-5, whereas for SDR-10, to generate complex multiples, a carry propagate BCD addition is required. The SDR-4 recoding scheme generates $2z$ partial products using the set of multiples, such as $\{-2P, -P, 0, P, 2P, 4P, 8P\}$ [10, 11]. This recoding scheme is quite similar to conventional SDR-4 recoding for binary numbers. Figure 2 shows the diagram of generation of partial products.

To generate $5P$ and $10P$, we use mixed 4211/5211 decimal coding. So, we only need to evaluate $\{-2P, -P, P, 2P\}$ coded in 4221. Each digit $\mathbf{Qb_i}$ generates a PP PP[i] by choosing the proper MM. The one-hot coded signals $(q5_i, q4_i, q3_i, q2_i, q1_i)$ generate the PP by selecting one of the MM passing through 5:1 multiplexers. The sign signal qs_i determines if the negative MM should be produced by 9's complement of the corresponding positive MM. This is done by inverting the bits of the positive MM. This inversion is performed by XOR gates which are operating on the value of qs_i.

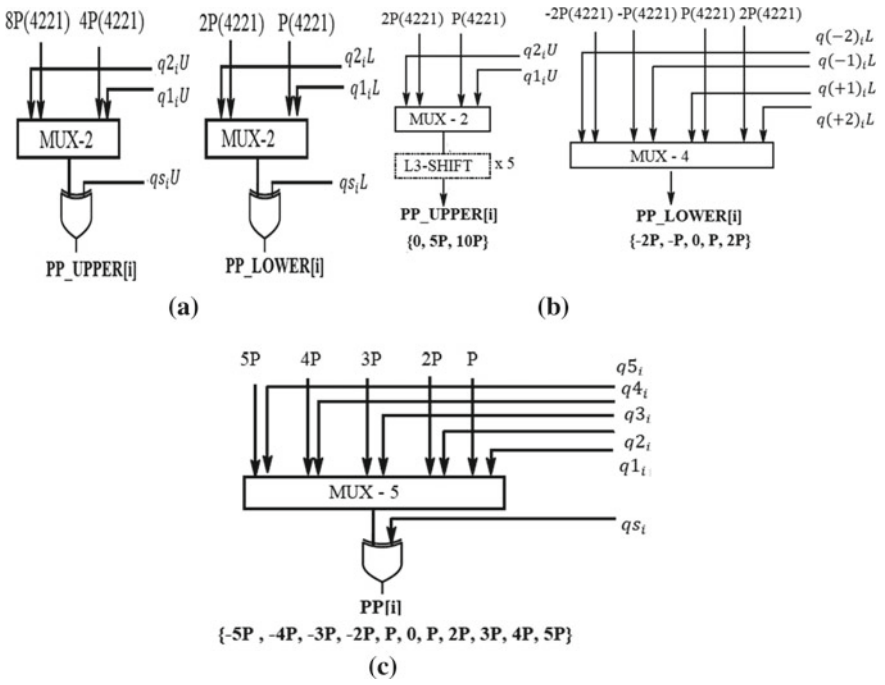

Fig. 2 Partial product generation for **a** SDR-4, **b** SDR-5, **c** SDR-10

2.4 Partial Product Reduction (PPR)

After the generation of decimal PPs, they are aligned and then reduced to two decimal operands using q:2 decimal compressors [8]. The alignment of the partial products is done according to their decimal weight as

$$Z = P \times Q = \sum_{i=0}^{z} (\text{PP\_UPPER}[i] + \text{PP\_LOWER}[i])10^i \quad (\text{SDR} - 4 \text{ and } 5) \quad (3)$$

$$Z = P \times Q = \sum_{i=0}^{z} \text{PP}[i]10^i \quad (\text{SDR} - 10) \quad (4)$$

These alignments do not need any logic, as they are performed using 4-bit wired left shifts. The corresponding PPs for each digit are added using carry propagate BCD addition if the sign bit is 1, else they are added using 9's complement BCD addition. By doing this, now we got z number of summation results which are aligned by 4i-bit wired left shift and reduced by using q:2 decimal compressors. For SD radix-10, PPs produced are aligned by 4i-bit wired left shift and reduced by using q:2 decimal compressors. All the PPs encoded in 4221 are at most of $(z + 3)$-digit long [11].

2.4.1 Decimal 3:2 Compressor

The proposed decimal 3:2 compressor adds three decimal operands to produce a decimal sum (S) and a carry word (H) multiplied by 2. All these operations are done in BCD-4221. The decimal digit 3:2 CSA is designed by utilizing a 4-bit binary 3:2 CSA [8, 12, 13]. At first, three operands coded in 4221 are given as input to the four 3:2 binary compressors which are based on full adder. The output of the binary compressors producing sum and carry digit is also in BCD-4221. Then, the carry digit is recoded into 5211-format followed by 1-bit left shift. This 3:2 compressor will be used for constructing 17:2 compressor, which, finally, would be used to reduce all the generated PPs. This forms a significant part of decimal fixed-point multipliers and further a part of floating point multipliers [14] (Fig. 3).

2.4.2 Decimal 17:2 Compressor

There had been many novel PPG techniques proposed in the literature like in [13]. A decimal 17:2 compressor consists of six levels of 3:2 decimal compressors. A total number of 15 decimal 3:2 CSAs or compressors are required to implement the decimal 17:2 compressor. Here, 17 decimal operands coded in 4221 are reduced into two decimal operands which are also coded in 4221 (Fig. 4).

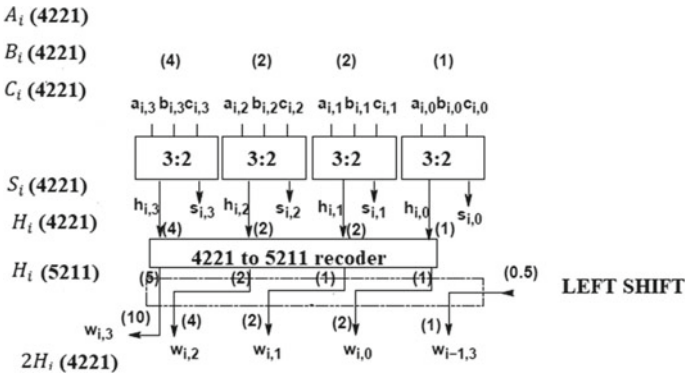

Fig. 3 Decimal 3:2 compressor

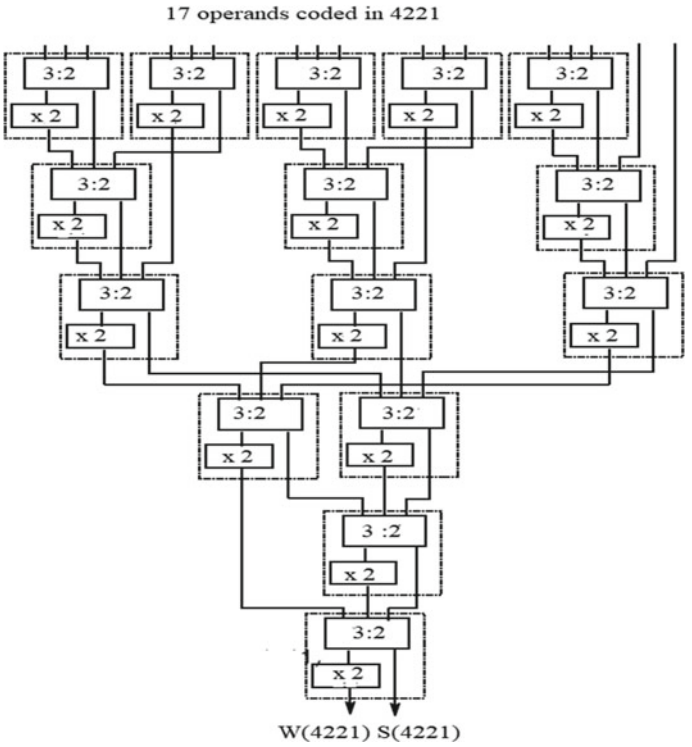

Fig. 4 Decimal 17:2 compressor

3 Results and Discussion

The 16-digit decimal multipliers have been synthesized using 90 nm CMOS standard cell library with Cadence Genus synthesis solution. The results are obtained for slow, typical and fast libraries. Figure 5 shows the power, timing and area comparison of SDR-4, 5 and 10 decimal fixed-point parallel multipliers. From the figure, it is clear that SDR-10-based multiplier is performing best among all three. It is the fastest among all as shown in Fig. 5b. The reason for SDR-10 based multiplier to be the fastest is that it produces the least number of partial products. The SDR-10-based multiplier turns out to be 9.72 and 6.47% faster than SDR-4 and 5-based multiplier, respectively. On the area side, it is 63.97 and 54.56% smaller that SDR-4 and 5-based multiplier, respectively. The number of PPs generated for SDR-10 is 17 as compared to 32 for SDR-4 and 5. In the multiplier, the most resource consuming portion is PP reduction stage. So, less number of PPs means less complex PP reduction tree and hence a faster multiplier. This same reason also results in SDR-10 based multiplier consuming least power and area.

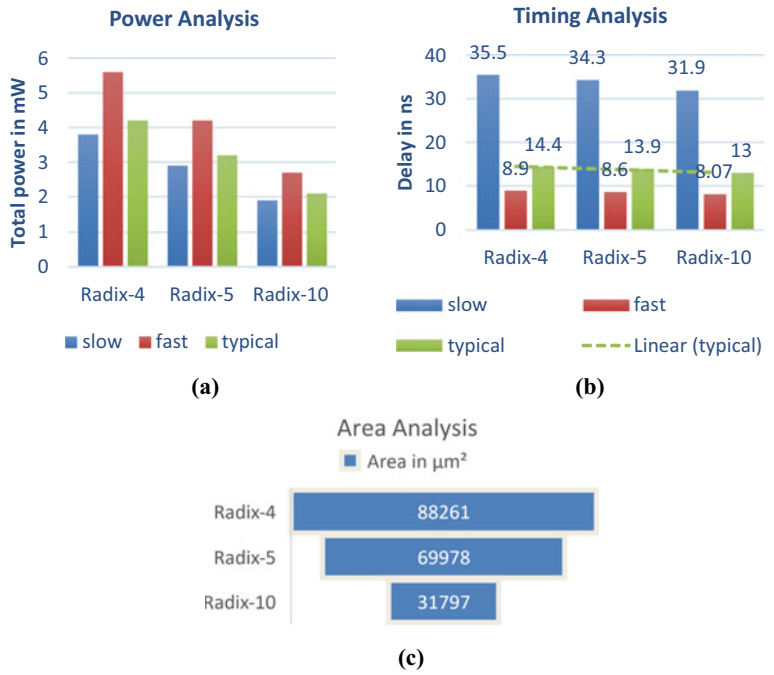

Fig. 5 **a** Power, **b** Timing, **c** Area analysis of proposed multipliers

4 Conclusion

We have implemented and analysed 16-digit SDR-4, SDR-5 and SDR-10 decimal fixed-point multipliers. The partial products were generated parallelly with the usage of simplified multiplier recoding and MMs. This work uses a decimal compressor based on carry-save addition using unconventional 4221 codes for the reduction of partial products. Among the three 16-digit multipliers we have designed, the SDR-10 multiplier gives the best results in terms of area, power and delay. SDR-4 multiplier performs worst for all parameters, while SDR-5-based multiplier shows an average performance that lies between SDR-10 and SDR-4 results. So, from the comparative study, it is clearly visible that the SDR-10 decimal multiplier is the exciting option for performing decimal multiplication which can further be used for designing floating point arithmetic units.

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Consensus Mechanism for Peer-to-Peer Energy Trading

Amit Kumar Vishwakarma, Haiwang Zhong, and Yatindra Nath Singh

1 Introduction

The rapid development in the living standards of human beings, while maintaining quality of environment, requires large fraction of clean energy. The distributed renewable energy sources integrated with smart grid are a possible approach to fulfil this requirement. The proposed system can also help in providing electricity to remote areas where utility companies can not reach. The smart grids will allow the customers to trade their surplus energy among themselves leading to more reliable energy. In order to allow for trade with fairness, a trading system is needed. One approach is to sell the excess energy to the main grid which in turn will distribute the energy to the customers having energy deficit. The second approach is to use a decentralized system and enable the trading between excess energy nodes and their neighbours with energy deficit [1]. This is expected to allow for energy transfer through shorter paths. The blockchain technology [2, 3] is one of the possible solutions for distributed peer-to-peer trading.

A lot of research have been reported on peer-to-peer energy trading, but most of the papers just discussed the theory, and few of them have discussed implementation details.

The blockchain-based energy trading can be divided into three parts (Fig. 1): transaction, consensus mechanism, and optimization. In this paper, we will only study the various types of consensus mechanisms and compare their performance.

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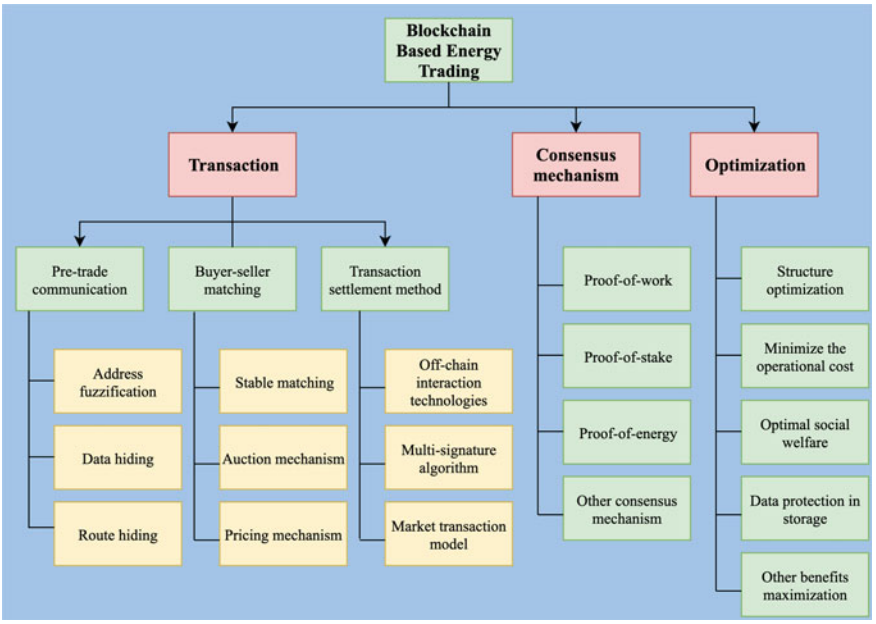

Fig. 1 Classification of blockchain-based energy trading

Based on the performance comparison, we also report implementation of delegated Byzantine fault tolerance-based blockchain network for peer-to-peer energy trading.

The rest of the paper is organized as follows. Section 2 discusses the consensus mechanisms for peer-to-peer energy trading. Section 3 concludes the paper along with the further research directions.

2 The Consensus Mechanism for P2P Energy Trading

The consensus is the process of reaching a point of mutual agreement by major number of miner nodes in blockchain network. It ensures that all the nodes in the network maintain the same distributed ledger. In case of a centralized regulator in the network [4], there is no need for consensus mechanism because the centralized regulator node makes all the decision, but a distributed ledger like blockchain requires consensus mechanism to reach an agreement by majority of the nodes. Three different kinds of consensus mechanism and their implementation are discussed further in the paper.

Consider a distributed network with N nodes forming the set S_N. Each node can work as producer as well as consumer. When a consumer acts as a producer, it is termed as prosumer. A node can switch back and forth between prosumer and consumer roles. Let P be the total number of prosumer nodes forming the set S_p, and

C be the total consumer nodes forming the set S_c. Let n nodes form a blockchain network and constitute the set S_n. Here, $S_n \subset S_N$, $S_p \subset S_N$, and $S_c \subset S_N$. The surplus energy of a prosumer p ($p \in S_p$) be $E_p \ \forall p \in S_p$, and the power deficiency of consumer c ($c \in S_c$) is $E_s \ \forall c \in S_c$. If the prosumer nodes wants to sell their surplus energy to the consumers, they will announce the amount of surplus energy and minimum rate at which they are willing to sale in the blockchain network.

All the consumer nodes will read the offers floated by prosumers and will put what they would like to have in the blockchain. Since the offers from seller and buyers are in blockchain, they cannot refute it. Finally, all the nodes, figure out using this information, using same algorithm, who is going to buy from whom. The resulting liabilities are automatically generated by each node in the next cycle and added to next block. When the transaction is completed and added to blockchain, the nodes will verify these transaction based on the consensus mechanism before the next transaction to ensure who owes whom, how much. After the validity check, the transactions are done and then broadcasted to the network as well as the next block. At the end of cycle, a new block get added to the blockchain network.

2.1 Proof-of-Work

PoW (Proof-of-Work) is the first consensus mechanism opted by early blockchain developers. The mechanism uses a sophisticated computer puzzle solved by miners, and the process is called mining. Solving this puzzle requires lot of computational power and time, the node which solves first, will get the chance to add a block in the blockchain and receives a reward for creating the block. A random number called nounce is used for deciding the level of difficulty. The miners will solve the puzzle by guessing the nounce based on SHA256 hash algorithm [5]. The mining can use different type of hardwares like CPU mining, GPU mining, FPGA mining, ASIC mining, mining pool, or cloud mining. The nodes who want to act as minor need to have access to such hardware. The difficulty depends on the frequency of block creation and its level increases with time. This makes PoW unsustainable in near future [6]. Thus, the developers moved to different consensus mechanisms.

Figure 2 shows the block header for PoW-based blockchain. It consists of four main components: Nounce, hash of the previous block, Merkle root, and timestamp. Nounce is a random number used to define the difficulty level of transaction. Hash of the previous block is used to link all the previous blocks recursively, with the current block to make an unalterable chain. The hash is supposed to maintain certain property such as certain bits of the hash has to be zero. All the miners search for the nounce value such that hash with the stipulated property is found. Whoever finds it first is the winner. That nouce goes into the block, and the computed hash becomes part of next block. The merkle root contains the hash of all the transaction happened in the current block. As Fig. 3 shows, to create a new block, the block header hash will be compared to the target hash generated by adding nounce. If miners can meet the target, new block will be created.

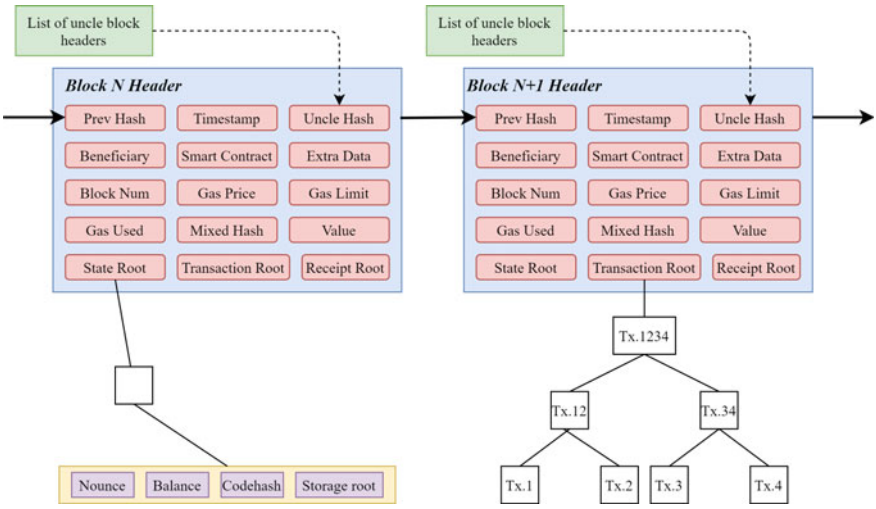

Fig. 2 The block header of PoW-based blockchain

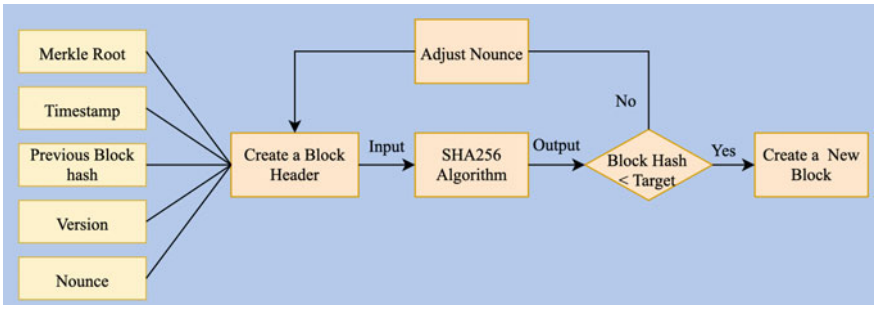

Fig. 3 The flow of PoW consensus mechanism

PoW consensus mechanism has two major drawbacks; first, it uses a huge amount of electricity to solve the computer puzzle of finding the nounce. The second is the problem of security; if the network is small, then the chance of 51% miner colluding is more.

2.2 Proof-of-Stake

Proof-of-stake (PoS) is based on validators' economic stake, the node (one of the all nodes acting as validator) having more stake will get the chance to add the block in the blockchain. There is no reward for adding the block into the blockchain network, and the miners get only transaction fees. A user has to stake their part in order to

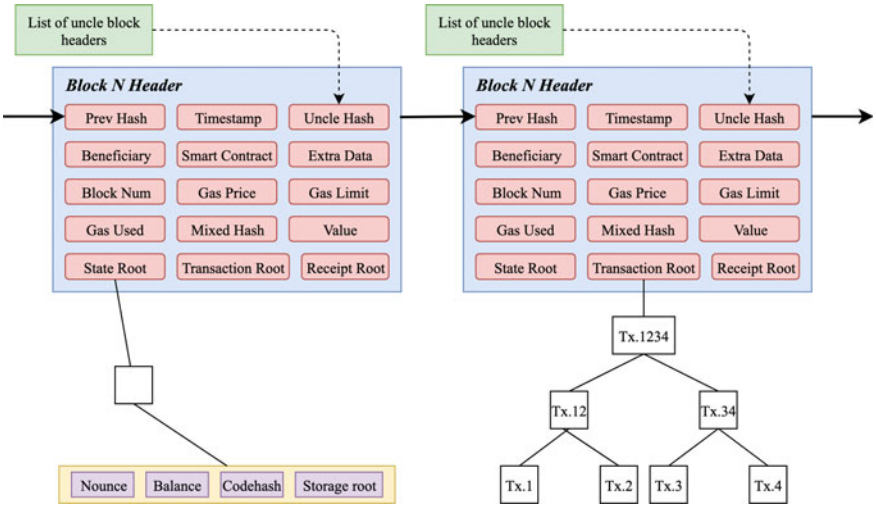

Fig. 4 The block of PoS-based ethereum blockchain

mine a block. The nodes are randomly chosen to participate in the mining process; once the nodes get chosen for mining, there will be voting to choose one miner for mining. Now the chosen node will have to stake minimum amount required [7].

Figure 4 shows the block header of the PoS-based consensus algorithm. The previous hash implies the hash of the previous block. The smart contract is a computer code used for negotiations in the transaction. GAS is used to pay to the network for making any transaction and one can own it in the form of ETH (The native currency of Ethereum). The nounce used in PoS is different from PoW. It shows the number of contracts or transaction exchange in the block. State root is the hash of the root node of nounce, balance, codehash, and storage root [8]. Transaction root contains the hash of all the transactions. Receipt root contains the hash of transaction root.

Figure 5 shows the working diagram of PoS-based blockchain. Node A wants to add the block into the network, a block header gets created, and then the hash value of header gets generated. The stake value of node A will be calculated, and if it matches with the target, new block will be created. Otherwise in the next round, the new node will get selected to add the block. PoS have many advantages; it is more eco-friendly, the processing power is less, and the coin value is also higher than PoW. Is also reduces chance of attach by 51% of nodes becoming rogue. The main disadvantage is that if a node has more stake into the network, then most of the time he will get the chance to add the block (The rich become richer).

There are two major types of PoS. In the first one—Chain-based PoS, pseudo-randomly assigned validator creates the new block. The second type, the Byzantine fault tolerance-based PoS, randomly selects the validator to propose a new block. CAP theorem, FLP impossibility, and the DLS paper prove that the BFT-based PoS is more secure, fast, reduces centralization risk and free of 51% rogue node-based attack.

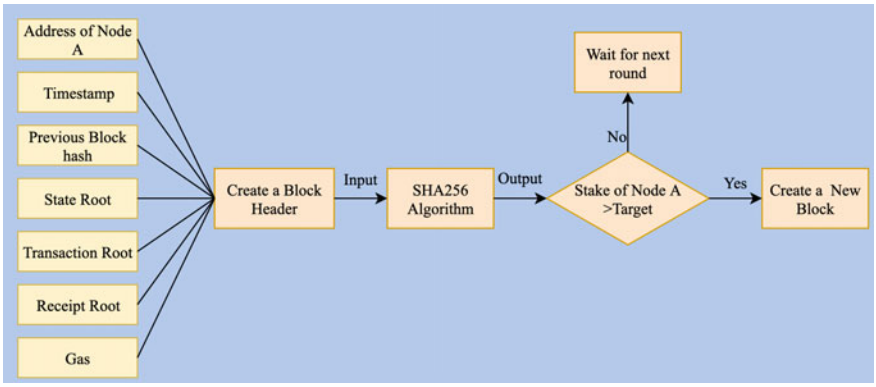

Fig. 5 The flow of PoS-based blockchain

BFT-based PoS works specially on two rules: Finality conditions and slashing conditions. The finality condition finalizes the hash, and slashing condition tells the condition when the validator can be slashed.

2.3 Delegated Byzantine Fault Tolerance

NEO (a smart contract compmany's blockchain implementation, NEO is name of its currency) uses delegated Byzantine fault tolerance to validate all the transactions. If a node stakes their NEO, the node will be able to generate GAS. The GAS is the platforms main circulating currency. The node will have to pay up to a certain amount of GAS fee for every transaction. That is why the more NEOs, a node will stake, more GAS, the node will get.

The DBFT is somehow the same as PoW, and it allows the user to vote for validating transaction based on NEO token holder. NEO is a blockchain platform and currency which uses smart contract very efficiently. These are few terms which will be used in further discussion.

- Consensus node: this node can vote and propose. It will also participate in the consensus mechanism.
- Ordinary node: It can only make a transaction. It cannot participate in the consensus mechanism.
- Delegates: These are chosen randomly. They are responsible for proposing the blocks. Maximum of d byzantine nodes can be there, and the proposed block will be accepted if and only if more than $2d + 1$ node will approve the block.
- Speaker: a speaker is chosen by the delegate nodes to create and transmit the proposed block.

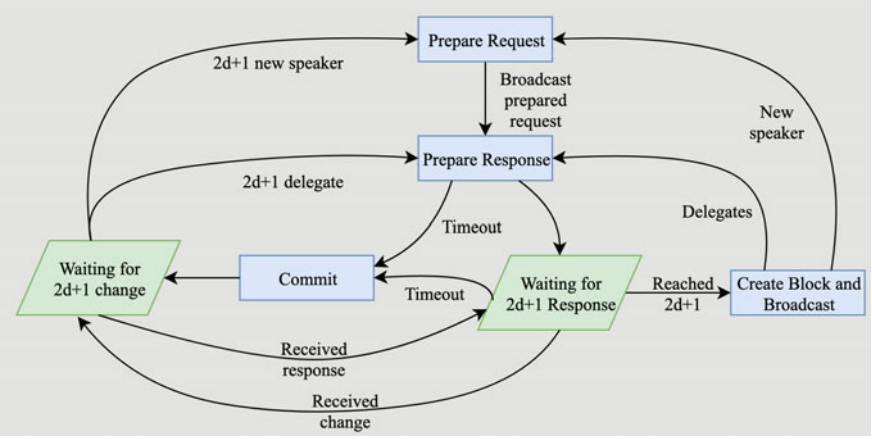

Fig. 6 The flow of DBFT-based blockchain

Anyone can become the delegate node if they fulfil the following requirement - good Internet connection, 1000 GAS (GAS is fees used to run the smart contract on blockchain platform), and specific equipment which can support the transaction. The energy nodes will vote for the delegates to choose a speaker randomly. The delegates are responsible for all the transactions in the network, and they also maintains the track of the transactions and update the ledger. The randomly chosen speaker will add the block, the speaker will send the block to all the delegates, and if 2/3 of them approve the block, it will get added; otherwise, they will again choose a new speaker.

As Fig. 6 shows, the algorithm comprises of four phases.

- prepare a request, broadcast it to the delegates, and initiate a block creation.
- prepare response after receiving the proposed block. The delegate will choose a speaker to verify the block.
- commit (if $N - d$ nodes verify the block, block is good to go to publish), and
- create the block and broadcast (The node is verified and added into blockchain and now can be published to the other nodes).

Let us suppose there are N number of energy nodes, d number of delegated nodes (d should not be more than $(N - 1)/3$), k number of attempts to find the speaker, and b be the block comprising of current transaction. Let p be the address of the speaker. The prosumer node will broadcast a cryptographically signed smart contract to the blockchain network. The N nodes will receive the record of transactions, and they will find the consumer based on the smart contract. The NEO token validates the credibility of energy nodes, and the GAS amount will decide the transaction. The GAS amount depends on the energy amount and the time. After the transaction, the consensus nodes find the speaker p, $N - 1$ delegates will receive the block b, and all of them will verify and then broadcast. The speaker should receive at least $N - d$ verification to publish the node.

A public-private key is used for encryption and decryption. SHA256 hashed ECDSA or redeem script is used to generate an address for a user as shown in the following equations [10].

$$hash = RIPEMD160(SHA256(SHA256(pubKey \oplus rScript)) \quad (1)$$

$$checksum = Truncate(SHA256^2(hash||0x00)) \quad (2)$$

$$address = Base58(hash||0x00||checksum) \quad (3)$$

Algorithm

Algorithm 1: Delegated Byzantine fault Tolerance

Prepare Request
make prepare request
list of transaction broadcast
blockchainnetwork.mempool
Prepare Response *smart contract verification*
transaction verification
policy.maximumtransactionperblock
tr.hash$\leftarrow SHA256(traddr\ N \parallel EnergyAmount \parallel NEO \parallel GAS \parallel Timestamp)$
$transaction \leftarrow SHA256(energy\ amount \parallel NEO \parallel GAS \parallel timestamp)$
$BlockConsensus \leftarrow SHA256((N\text{-}d) \parallel (N\text{-}1) \parallel traddr\ N \parallel timestamp)$
$timestamp = Block.timestamp$
$Nounce = BlockConsensus.Nounce$
$transhash$
Commit
$If\ speaker\ is\ found\ in\ one\ round$
$transaddr(N-1) = transaddr.broadcast(dig.sign \parallel transaction \parallel timestamp)$
$checktransaddr(N-1).(2/3)dapproved$
Change Ownership
$change\ owner\ and\ add\ block\ into\ ledger$
If dig.sign is confirmed **then**
$Exchange\ energy$
$exchange\ NEO$

The PoW has proven resilient against external and internal attack, but it is high energy consuming and requires complex hardware. PoS is energy efficient, and it also penalize the dishonest validator, but it increases the risk of fork and promote centralization in favour of nodes having high stakes. The DBFT uses no forks, execution is faster for high value chained transaction, and finality of transaction is 100% after first confirmation. By comparing the properties of consensus mechanisms, DBFT gives absolute finality, fault tolerance is 33%, and power consumption is negligible. This

Property	*PoW*	*PoS*	*DBFT*
Type	*Probabilistic-Finality*	*Probabilistic-Finality*	*Absolute - Finality*
Fault Tolerance	*50%*	*50%*	*33%*
Power Consumption	*Large*	*Less*	*Negligible*
Scalability	*Good*	*Good*	*Bad*
Application	*Public*	*Public*	*Permissioned*

Fig. 7 The comparison of consensus protocol

consensus only can be implemented in the permissioned system, and this makes it suitable and secure for peer-to-peer energy trading. The scalability is the main issue for this mechanism (Fig. 7).

3 Conclusion

The paper discussed the three different types of consensus mechanism for P2P energy trading. All the consensus mechanisms have different types of properties which makes them unique. If the anonymity, security, and privacy are the major issues, then PoW is the best option, but the disadvantage is the cost, latency, high energy, and high transaction cost. If the system is small and priority which is not the security and privacy, then PoW is the best option. PoS provides faster transaction, low transaction cost, and required less hardware for real-time implementation. DBFT ensures the finality for the transaction once confirmed, has no forks, fast transaction, and low energy consumption.

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Circularly Polarized Wideband Ring CDRA for Wireless Applications

Chandravilash Rai, Sanjai Singh, and Ashutosh Kumar Singh

1 Introduction

Dielectric resonator (DR) antenna is a more useful antenna in the last twenty years, due to its various attractive characteristics (like low profile, high gain, high radiation efficiency, and low metallic losses at high frequency) [1]. DR has some fundamental shape like rectangular, cylindrical, and spherical but some modified shapes also possible like a disk, ring, triangular, half-split, notch rectangular, conical, and elliptical [1, 2]. Last few years, many researchers focus on the enhancement of bandwidth with a different method like ring shape DR, multi-segment DR, and adopted hybrid feeding structure in DRA [3, 4]. Main objective behind this method is the enhancement of bandwidth (30–75%) by reducing *Q*-factor. The *Q*-factor is reduced by placing DR above the ground plane [4–6].

In the present age of wireless communication, we are more focused on circular polarization (CP) because it has removed the disadvantage of linear polarization (LP). The main disadvantaged of linear polarization is multiple-path between transmitting and receiving antenna and misalignment between them [7]. There are many techniques which can be used to achieve CP (like difference shape of dielectric resonator with various feeding mechanism, two orthogonal electric field components, or 90° phase difference between these field components). Wideband antenna is more useful in cogitative radio applications [8–10].

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Hear ansoft HFSS is used for simulation of a proposed ring CDRA; in this paper, wideband can be improved as well as *Q*-factor can be minimized by removing the central portion of DR. The proposed ring CDRA exhibits an impedance bandwidth of 43.31% from 6.15 to 9.55 GHz. The axial ratio (AR < 3 dB) bandwidth is 4.12% and 2.08% between the frequency range 8.08–8.42 GHz and 9.03–9.22 GHz, respectively. Gain between frequencies is positive.

2 Design and Geometry of the Antenna

Figure 1 exhibits the illustrative diagram of the proposed ring CDRA. The circular ring-shaped aperture etch on the top of the FR-4 epoxy substrate (with ε_r sub = 4.4, tanδ = 0.02, and height 1.6 mm), where the bottom side consists of hook-shaped microstrip feed line. Ring CDRA is manufactured by alumina (with $\varepsilon_r = 9.8$, tanδ = 0.002) and pest above of the substrate with the help of gluey. Details of the optimized parameter are shown in Table 1.

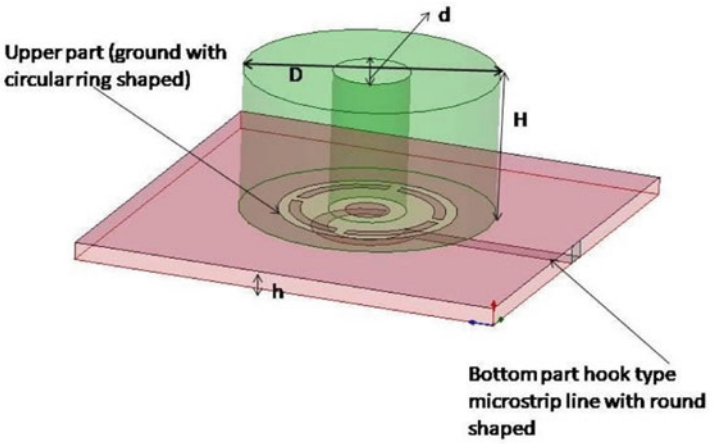
3 Result and Discussion

The simulated value of return loss, axial ratio, gain, and radiation pattern for the proposed ring CDRA has been discussed in this part. The return loss graph of the proposed antenna is shown in Fig. 2. It is clear from Fig. 2 that the ring CDRA exhibits an impedance bandwidth of 43.31% from 6.15 to 9.55 GHz. The bandwidth is achieved by reducing the quality factor.

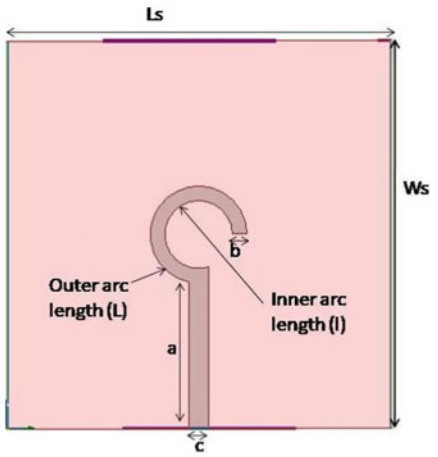
The ring CDRA exhibits an axial ratio bandwidth of 4.12% for (8.08–8.42 GHz) and 2.08% for (9.03–9.22 GHz) as shown in Fig. 3. We know that essential condition for the generation of CP wave, two-field components are equal in magnitude and orthogonal to each other [11, 12]. In the proposed CDRA, ring-type circular slot behaves as a magnetic dipole, while hook type microstrip lines behave as electric dipole, and orthogonal field components created by the combination of an electric and magnetic dipole. So ring-type circular slot and hook type line are responsible for the generation of CP.

Figure 4 exhibits the gain versus frequency of proposed ring CDRA, where at frequency 6.62 GHz gain 2 dB, at 8.02 GHz gain 0.5 dBi, and 9.20 GHz gain 6 dB. From Fig. 3, we are concluded that the proposed radiator exhibits good gain values.

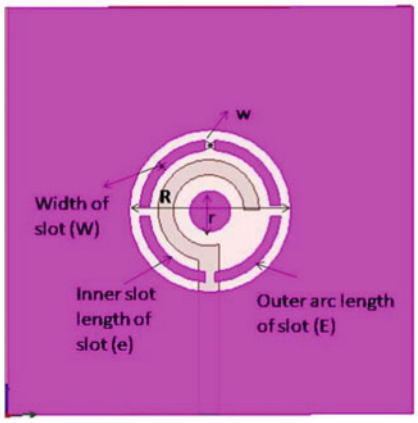
Figure 5 shows the RHCP and LHCP pattern of the proposed ring CDRA at frequency 8.12 and 9.20 GHz. It is clear from the figure that the proposed ring CDRA has more than 20 dB difference that can be seen between the RHCP and LHCP patterns of the antenna. It is confirm from Table 2 that the proposed R-CDRA has better impedance bandwidth.



(A) Perspective view



(B) Feeding structure



(C) top view

Fig. 1 Schematic diagram. **a** Perspective view, **b** feeding structure, **c** top view

Table 1 The optimized parameter of proposed CDRA

Symbol	Dimension (mm)	Symbol	Dimension (mm)	Symbol	Dimension (mm)
Ls	40.00	W	01.00	E	09.99
Ws	40.00	w	01.00	e	08.42
L	22.45	D	23.00	a	15.10
l	17.40	d	07.00	b	01.50
R	15.00	H	13.00	c	02.00
r	04.00	h	01.60		

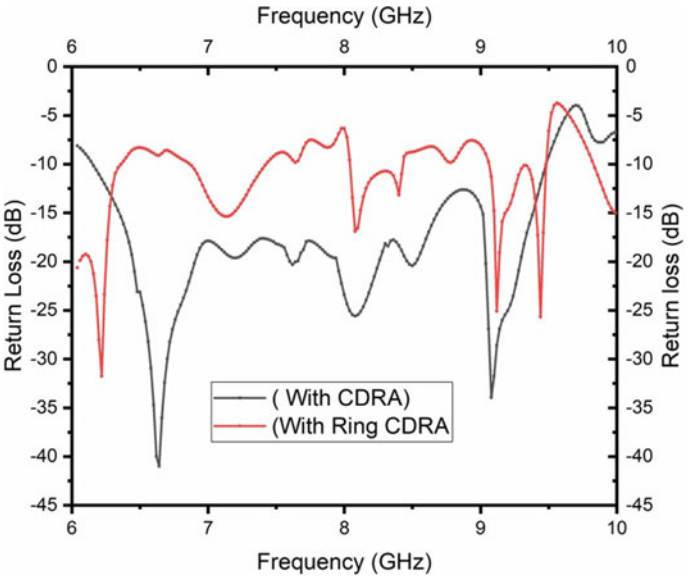


Fig. 2 $|S_{11}|$ graph of proposed ring CDRA and CDRA

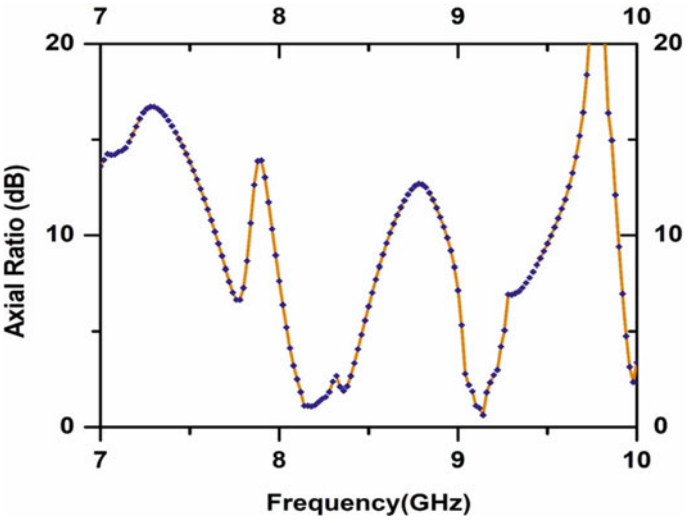


Fig. 3 AR of proposed ring CDRA

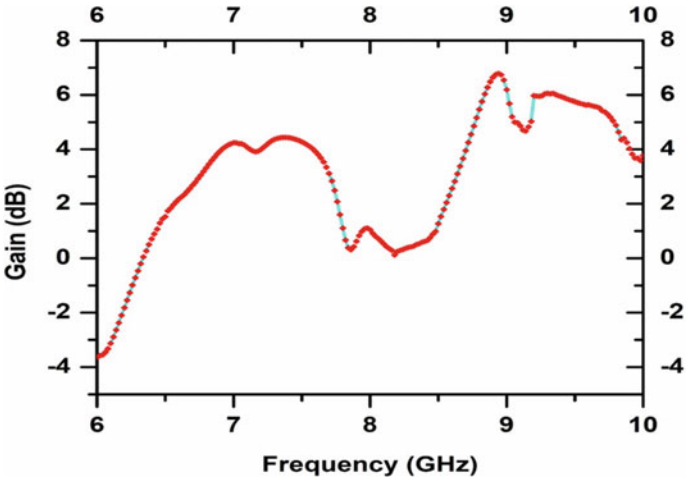


Fig. 4 Gain of proposed ring CDRA

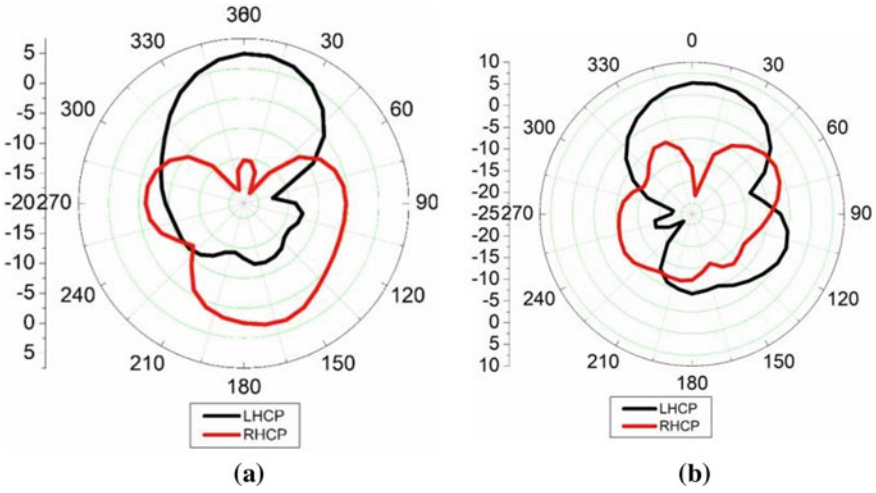


Fig. 5 **a** RHCP and LHCP at 8.12 GHz. **b** RHCP and LHCP at 9.20 GHz

Table 2 Comparison table of previous work on DRA

Type of DRA	Feeding method	Impedance bandwidth (%)	AR bandwidth (%)
CDRA [3]	Quadruple strip feed	34	25
CDRA [4]	Quadruple strip feed	30	28
RC-DRA [12]	Co axial feed	20	13
Proposed R-CDRA	Microstrip line feed	43	4 and 2

4 Conclusion

In this article, a circularly polarized wideband ring CRDA is presented. The proposed radiator exhibits an impedance bandwidth of 43.31% from 6.15 to 9.55 GHz. Ring-type circular slot and hook type line are responsible for the generation of CP wave in frequency bands (8.08–8.42 GHz and 9.03–9.22 GHz) with axial ratio (AR < 3 dB) bandwidth 4.12% and 2.08%, respectively. This antenna is useful in wireless applications.

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Performance Improvement of 28 GHz Antenna Array for Fifth-Generation Wireless Communication System

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1 Introduction

In the present technology, higher data rates and large bandwidth are important objects for fifth- and next-generation wireless applications [1]. The band for 5G technology approved by ITU is from 24.0 to 86.0 GHz. For the fifth generation, mainly the focus is on the antenna array design for the improvement of gain and better transmission characteristics [2]. Microstrip patch antennas are extensively used in wireless communication because of compact size, light weight, low cost [3] and easiness for both fabrication and integration [4]. Various types of antenna array have been designed. The designed system technique used was hybrid coupler, and the gain measured was 12.398 dBi at the resonant frequency of 26 GHz [5]. A high-gain 24-patch element microstrip patch antenna array was reported for 60 GHz which is mainly used in WLAN/WPAN applications where peak measured gain of 19.26 dBi was reported at 61.56 GHz resonant frequency [6].

Microstrip feed is preferred because substrate cutting does not require and protect conduction layers as compared to coaxial feed line therefore its helped to minimized surface waves [7]. A simple series fed patch antenna phase array has been proposed. The antenna is designed on Rogers RT/duroid 5880 substrate. The measured gain reported is 15.6 dBi at 28 GHz [8]. A broadband antenna array for 28 GHz with a 4-way feed network was designed for the operating band in 25.052–34.923 GHz with a peak gain of 12.15 dBi and radiating efficiency of 85% [9]. A linear dielectric resonator antenna array with a modified feeding structure is investigated, and the measured gain is found to be 12.1 dBi [10]. A 16 × 16 array is constructed for the Ku band with a measured gain of 29.5 dBi and the first side lobe level of −

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26.5 dB [11]. A high-gain 4 × 4 antenna array was designed for 5G applications on Rogers RT/duroid 5880 substrate of size 30.65 × 39.3 mm^2 with a return loss of −16.37 dB and measured gain of 17 dBi with the bandwidth of 308 MHz [12]. A linear array consisting of 16 elements with defected ground structures has also been proposed on low-loss Teflon-based RT/duroid 5880 substrate. The gain and the radiation efficiency observed were 17.4 dBi and 91.8%, respectively [13]. A circularly polarized antenna array using two-layer structures was designed. The gain achieved lies from 13 to 16 dBi from 28.5 to 31.5 GHz [14]. The 16-element antenna array for 5G wireless application using series–parallel feeding was designed with measured gain and radiation efficiency reported which were 17.1 dBi and 92% [15]. A 2 × 8 MIMO antenna array was proposed and designed with Rogers RT/duroid 5880 substrate. The frequency band measured is 27.49–29.42 GHz. At 28.0 GHz resonant frequency, gain is 11.33 dBi and radiation efficiency is 88.58% [16]. The above-mentioned antennas have limited gain [12–15], less radiation efficiency [14, 15] and return loss [12–14]. Also, the size of the antenna [12, 15] is less than the proposed work.

Considering the above discussion, the work presented in this paper has focused on the design of 1 × 16 tapered antenna designs with tapered feed and used right-hand and left-hand elliptical polarization between the last two patches of each four columns which help to improve the antenna parameters like gain, radiation efficiency, return loss and compactness of the antenna.

2 Proposed Antenna Design

The proposed array antenna consisting of 1 × 16 elements is designed on the Rogers RT /duroid 5880 dielectric substrate and occupied 26 × 36 mm^2 space. The Rogers RT/duroid 5880 has dielectric constant of 2.2, 0.0009 tangent loss and thickness of 0.79 mm.

In the proposed design, a tapered feed line is selected with the array antennas. The first two patches of each column are having inset feed for proper impedance matching. The last two patches of each columns slot are tapered from point w to z at an angle of 45° for providing left- and right-hand polarization between the last two patches to decrease the cross-polarization, and the feed line is tapered from x to y to improve the gain of the design antenna. The schematic front and back view of the proposed antenna is shown in Fig. 1. The 50Ω impedance port is used for achieved impedance matching. All the design parameters are optimized using built-in particle swarm optimization algorithms in CST Microwave Studio which are given in Table 1.

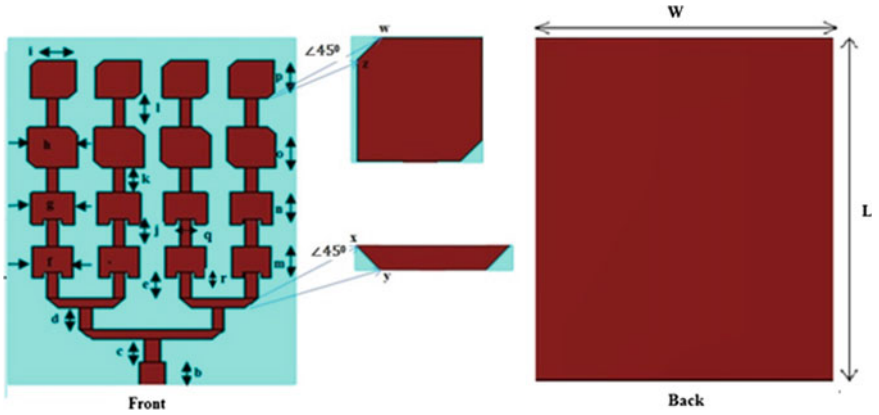

Fig. 1 Schematic front and back view of proposed antenna geometry with extended view for tapered feed and truncated or slant slot showing quarter wave transformer and series–parallel tapered feed lines with inset feed for impedance matching. The last two patches of each column having truncated corner, $L = 30$ mm, $W = 36$ mm

Table 1 Optimized dimension of proposed antenna array

Parameters	Value (mm)	Parameters	Value (mm)	Parameters	Value (mm)
a	2.3	*g*	3.7	*m*	2.8
b	2.3	*h*	4.2	*n*	3.3
c	1	*i*	3.8	*o*	3.4
d	1	*j*	2.8	*p*	3.2
e	0.9	*k*	2.8	*q*	0.5
f	3.4	*l*	2.8	*r*	0.3

3 Results and Discussion

3.1 Resonant Frequency

The proposed antenna array consists of four steps. All the design steps are shown in Fig. 2, and their $S11$ parameters are compared and shown in Fig. 3. In design Step 1, a single microstrip patch antenna with inset feed designs is designed. The antenna is resonating at 27.8 GHz and covers 27.72–28.24 GHz bandwidth in − 10 dB return loss bandwidth. The return loss calculated is − 12.42 dB.

In design Step 2, 1 × 4 antenna array with tapered feed line is designed. The first two patches are having inset feed for proper impedance matching, and in the last two patches, truncated slot is made with an angle of 45° to provide left- and right-hand polarization. The antenna resonates at 29 GHz and occupies 28.65–29.389 GHz bandwidth in − 10 dB return loss band. The return loss is about − 30.46 dB. In

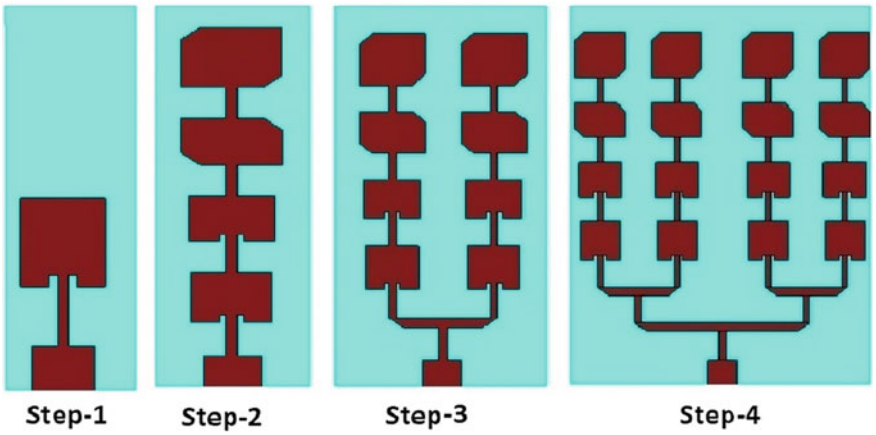

Fig. 2 Design steps of proposed microstrip antenna array. Step 1, single patch antenna. Step 2, 1 × 4 array. Step 3, 1 × 8 array. Step 4, 1 × 16 array

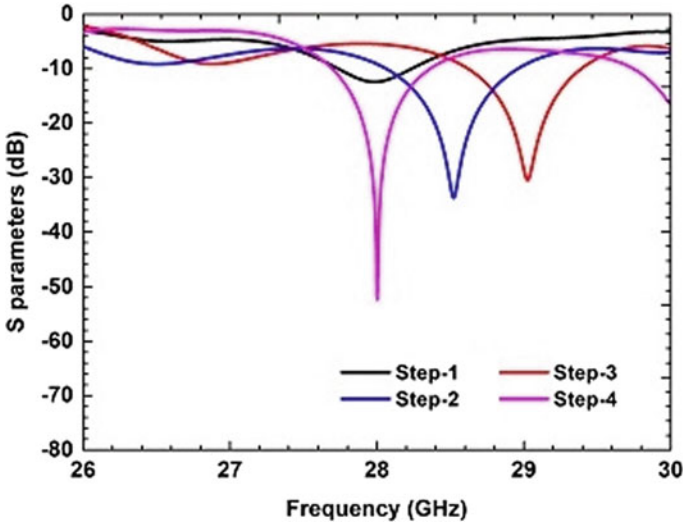

Fig. 3 $S11$ parameter of design Step 1 to Step 4. Step 1, $S11 = -12.42$ dB, Step 2, $S11 = -30.46$ dB, Step 3, $S11 = -33.3$ dB, Step 4, $S11 = -52.34$ dB

the design Step 3, 1 × 8 antenna array is designed which covers 27.99–29.00 GHz bandwidth with VSWR ≤ 2. The return loss is about − 33.3 dB, and the gain is 13.35 dB. In design Step 4, 1 × 16 antenna array with corporate series tapered feed is designed. Here, we can observe that as the size of the antenna is increasing, the frequency is shifted toward 28 GHz which is the resonant frequency and the

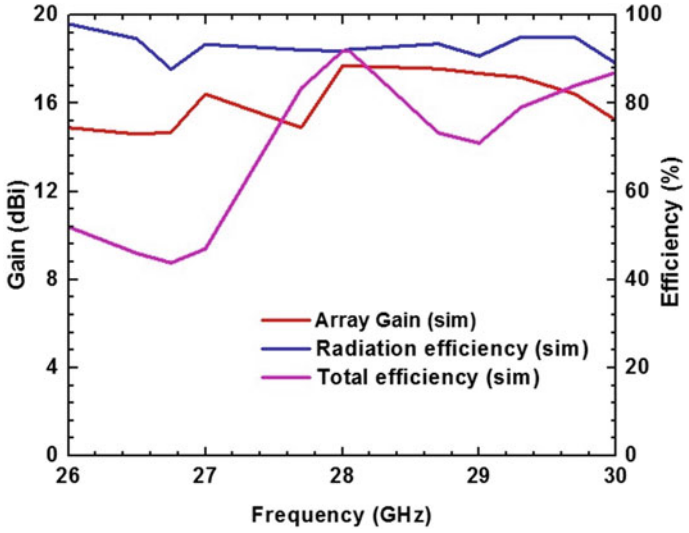

Fig. 4 Gain and efficiency of the proposed antenna array. The gain at 28 GHz resonant frequency is 17.7 dBi, and radiation efficiency is 93.36%

return loss becomes higher. The antenna covers an impedance bandwidth of 27.70–28.38 GHz. The gain calculated is 17.7 dBi at 28 GHz resonant frequency. The return loss is − 52.34 dB.

3.2 Gain–Efficiency

The gain and efficiency of the proposed antenna array are shown in Fig. 4. The proposed antenna array has gain varying from 15.5 to 17.7 dBi in the whole band, and the radiation efficiency in the band varies from 87.98 to 98.82%. The total efficiency in the band varies from 52.93 to 91.95%. At the resonant frequency, the gain is 17.7 dBi as shown in Fig. 5 and the radiation efficiency 93.36%.

3.3 Radiation Patterns

The 3-dimensional *E*-field and *H*-field radiation patterns are shown in Figs. 6 and 7, respectively. The proposed antenna array has 32.1 dBV/m value of *E*-field at the resonant frequency and − 19.4 dBA/m value of *H*-field for the radiator connected at 50Ω impedance port.

The antenna array has 24.70° beamwidth, and the main lobe direction of *E*-field and *H*-field is 0° as shown in Figs. 8 and 9, respectively. Both the normalized *E*-field

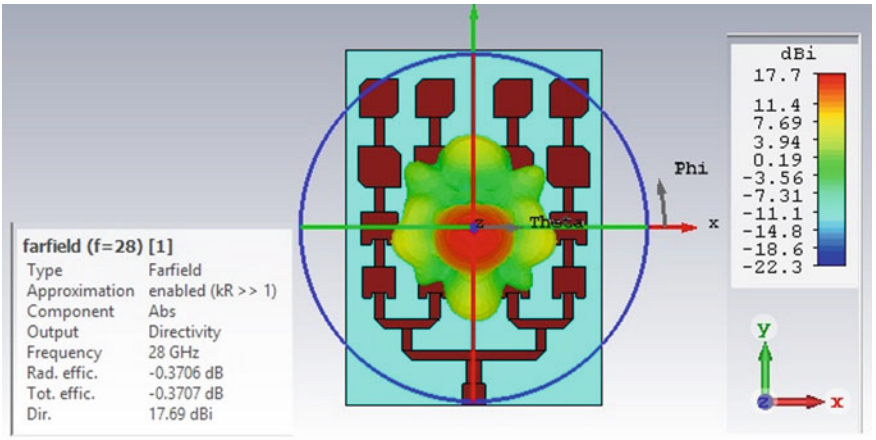

Fig. 5 Gain pattern. A gain of 17.7 dBi, radiation efficiency of 93.36% and total efficiency of 92.36%

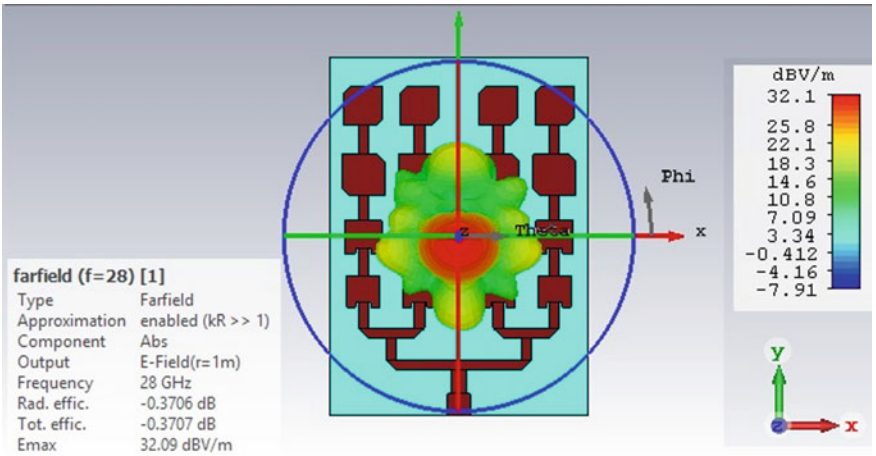

Fig. 6 *E*-field pattern. *E*-field value of 32.1 dBV/m at 28 GHz resonant frequency

and *H*-field indicated that the antenna is directional in nature at 24.70° beamwidth and 0° beamwidth, respectively.

As can be seen in Figs. 10 and 11, the simulation result shows that the isolation between the co-polar and cross-polar in *H*-plane is more than − 55 dB at 0° and in the *E* plane, the isolation is more than − 40 dB as shown in Fig. 11. It is seen that right-hand and left-hand elliptical polarization used in the design for patches helps to reduce the cross-polarization.

A comparison of the present work and the previous reported works is shown in Table 2. It can be clearly seen that the proposed antenna array at 28 GHz has enhanced

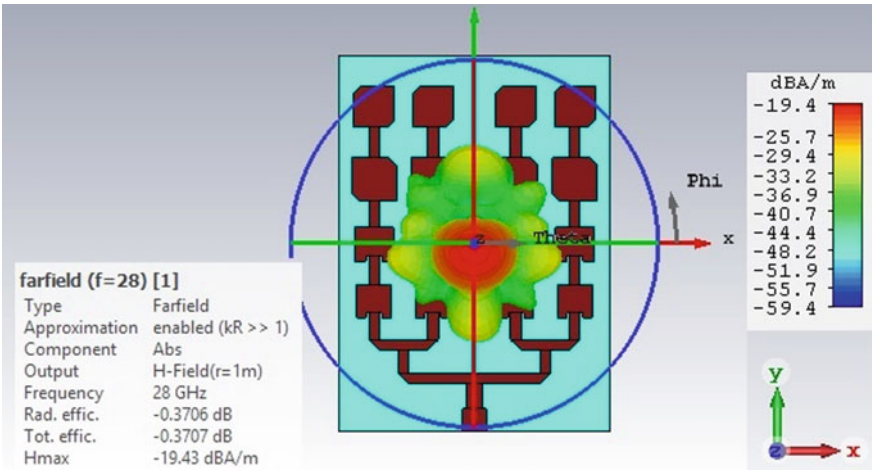

Fig. 7 *H*-field pattern. *H*-field value of − 19.4 dBA/m at 28 GHz resonant frequency

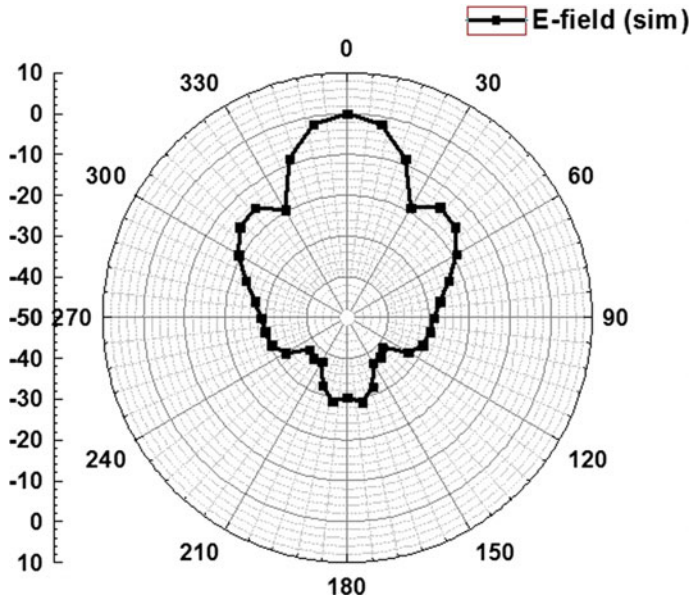

Fig. 8 Normalized *E*-field pattern. The main lobe magnitude = 17.8 dBi, main lobe direction = 0°, angular width (3 dB) = 21.4° and side lobe level = − 11.7 dB

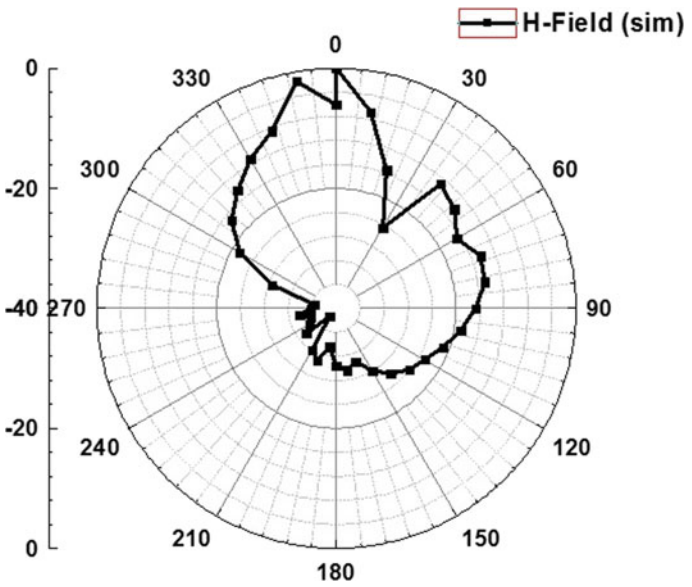

Fig. 9 Normalized *H*-field pattern. The main lobe magnitude = 17.8 dBi, main lobe direction = 0°, angular width (3 dB) = 18° and side lobe level = − 11.4 dB

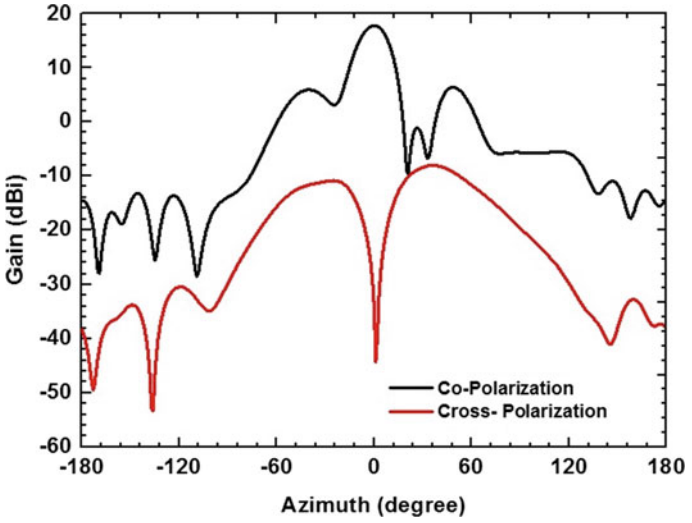

Fig. 10 Co-polarization and cross-polarization plot of the proposed antenna array in *H*-plane

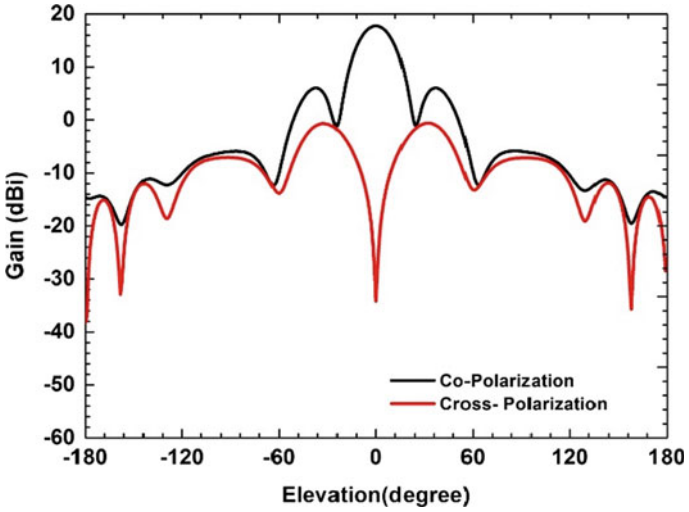

Fig. 11 Co-polarization and cross-polarization plot of the proposed antenna array in *E*-plane

Table 2 Comparison of proposed work with considered references

Reference papers	Frequency (GHz)	No. of elements	Size of substrates (mm^2)	Gain (dBi)	S11 (dB)	Radiation efficiency (%)
12	28.0	16	31 × 39	17.0	− 46.5	–
13	28.5	16	–	17.4	− 30.0	91.1
14	29.5	–	–	16.0	− 42.0	–
15	27.1	16	88 × 25	17.1	− 63.0	92.0
Present work	28.0	16	30 × 26	17.7	− 52.34	93.36

gain, radiating efficiency, return loss and compactness as compared to other antennas previously reported.

4 Conclusion

In this work, a tapered antenna array using a tapered feed of size 30 × 26 × 0.79 mm^3 is presented. The present antenna is designed for fifth-generation wireless communication in the 28 GHz band. The array is designed with a gain of 17.7 dBi, and the radiation efficiency is 93.36%. The antenna − 10 dB impedance bandwidth varies from 27.70–28.38 GHz with VSWR ≤ 2. Compared to the previous design

reported, the proposed work has improved the performance of the antenna parameters like return loss, gain and radiation efficiency. Also, the reported antenna has occupied less size of the substrate 30×26 mm^2 which makes it the right choice for fifth-generation wireless communication system.

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Design and Implementation of Phase Frequency Detectors for Low-Power PLL

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1 Introduction

A PLL produces an output signal with phase proportional to that of the given input signal. The PLL has phase/frequency detector (PFD), charge pump, loop filter, voltage-controlled oscillator (VCO) and a divide by N counter. PLL has wide variety of applications [1], which includes the operation of the circuit at high frequencies. Thus, the amount of power consumed by the PLL will be high. To minimize the power consumption of the PLL, it is required to reduce the consumption of power for every component of PLL so as to obtain a power efficient PLL.

Phase detectors are fundamentally of two types: XOR gate-based phase detector and phase frequency detector (PFD). PFD determines the frequency and phase difference between the output signal of the VCO and the given input reference signal. The outputs of PFD are UP and DOWN signals, which are signalled based on the phase and frequency difference between the two signals. The output signal of the PFD is then given to the charge pump. Charge pump produces a DC voltage proportional to the outputs of the PFD [2]. This DC voltage is given as an input to the VCO [3] which controls the frequency of the signal produced by VCO. The lock time and the timing jitter of the PLL depend upon the performance of the PFD. The sensitivity of PFD can be defined as the lowest phase/frequency difference that the PFD can detect. Greater the sensitivity of the PFD implies a better performance of the PLL [4]. As the frequency of the operation increases, the switching power increases and thus the overall power consumption increases.

Larger-power dissipation requires larger heat sinks and hence requires larger area. As the data rate increases, the power consumption of the device also increases which enables a requirement for low-power devices. One of the methods which is discussed

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in this paper is Adaptive Voltage Level Ground (AVLG) which reduces the power of the circuits. AVLG is an add-on circuit which is used to raise the ground potential, due to this, the power consumed in the circuit reduces and thus low power is achieved. By integrating the AVLG circuit to the PFD circuit, the power consumption of the PFD reduces.

The objective of this paper is to design and implement a low-power PFD which also functions at higher frequency. The paper is organized as follows: related works as well as the description about characteristics of PFD are discussed in Sect. 2. The proposed architectures of pass transistor-based PFD with AVLG and the PFD without clock reset path are indicated in Sect. 3. Section 4 deals with the analysis of power consumption of the circuits implemented in Sect. 3. Further part of the paper deals with the conclusion and the future scope relating to the existing work.

2 Literature Review

PLL is an important component of a trans-receiver. It helps in generation of a stable clock, can generate the clock frequency directly from the received data and also has the ability to generate high frequency signal from low frequency signals. The PFD proposed in [1] is a dead-zone free PFD. Dead-zone free PFD is achieved since reset is not used in the circuit. The detector proposed in the paper consists of four inverters, two PMOS, two NMOS and two pass transistors. The area of the PFD is less when compared to the conventional one since reset is not present in the proposed PFD circuit.

A PFD design implemented using CMOS technology, True Single-Phase clock (TSPC) logic, Differential Cascade Voltage Switch Logic and Current Mode logic is proposed in [4]. All circuits are implemented and then compared in terms of transistor count and power consumption. The TPSC logic-based PFD design is found to be of higher efficiency compared to that of the others and is implemented for further comparison with all the other circuits available [5].

A PFD design using the pass transistor technology rather than the conventional CMOS transistors is proposed in [6]. The usage of pass transistors is mainly done since they ensure the operation at higher frequencies and also eliminates the reset path logic that is being used in the conventional CMOS circuit designs. The usage of pass transistors reduces the transistor count and thereby reducing the area consumed by the overall circuit.

The PFD can be improved further in terms of power consumption using the concept of adaptive voltage level (AVL). The AVLG technique has been used here in this paper to improve the power consumption of the PFD circuits. The use of AVLG technique and implementation is proposed in [7]. The concept of reset path in the conventional PFD circuits usually increases the transistor count and the power consumption. Thus, the concept of reset path has to be replaced. The technique of replacing the reset path is discussed in [8]. This technique includes reference clock and VCO clock being shared among the upper part and the lower part of the PFD.

The circuits indicated in this paper have been implemented using Cadence Virtuoso, and the simulation has been done using the Cadence Spectre. GPDK 180 nm CMOS technology is used for the implementation of the circuits. The power consumption of the circuit is also calculated. The proposed architecture is found to be highly efficient than the other architectures mentioned in this section.

2.1 Characteristics of Phase/Frequency Detector

Phase detector, logic circuit or an analogue multiplier which is used to generate a voltage signal in order to represent a phase difference between the two input signals. A conventional PFD is basically constructed using flip-flops. Fig. 1 presents the top level diagram of PFD where the CLK_REF is the reference signal, and CLK_VCO is the feedback signal from the VCO, and the outputs of the PFD are represented as UP and DOWN. Fig. 2 presents the operation of the PFD using state diagram. When both the CLK_REF and the CLK_VCO are low the output signals UP and DOWN is low. If the CLK_ REF leads the CLK_VCO, then the UP signal is high and the DOWN signal remains low. When the CLK_VCO is high, DOWN signal is also high. Since both UP and DOWN signals are high, the PFD resets and thus making both UP and DOWN signals low.

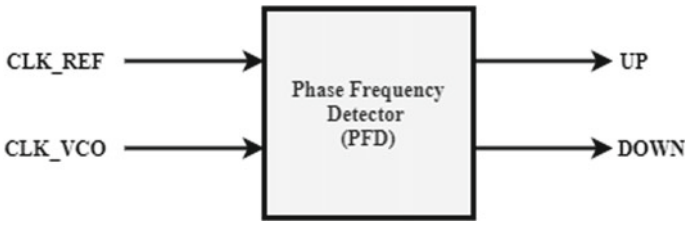

Fig. 1 Block diagram of PFD

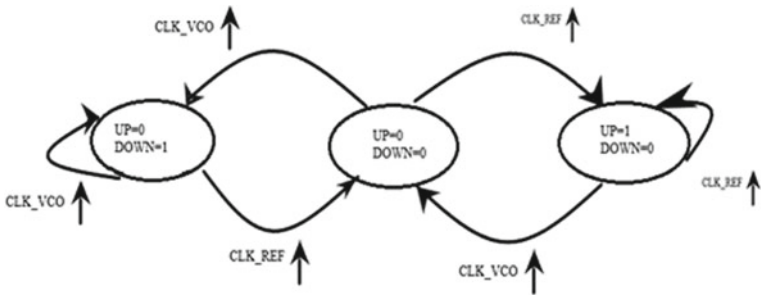

Fig. 2 State diagram of PFD [9]

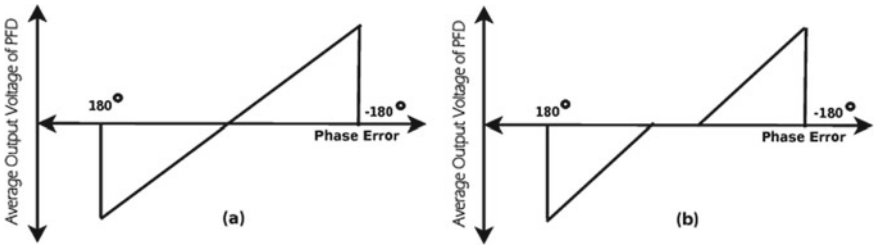

Fig. 3 Transfer characteristics of PFD **a** without dead-zone, **b** with dead-zone

The operation principle remains the same even when the CLK_VCO leads the CLK_REF. The dead-zone is an important factor of PFD that limits the range of detection of PFDs and thus affects the locking range of PLL [9]. When the phase difference between two input signals is close to zero, the width of the output signal produced by the PFD will be very small. The low width UP and DOWN signal will not be able to charge and discharge the switches of charge pump and thus cannot produce an output which can be given to the loop filter to produce a constant DC control voltage to the VCO. This reduces the loop gain and also increases the jitter in the PLL. The transfer characteristic of the PFD with and without dead-zone is indicated in Fig. 3.

The difference in phase between CLK_REF and CLK_VCO is indicated in Eq. (1).

$$\Delta\emptyset = \frac{\Delta t}{T_{\text{ref}}} \tag{1}$$

where $\Delta\emptyset$ = Phase error

Δt = Time delay between the peak of two input signals

T_{ref} = Time period of the input reference signal.

The phase error $\Delta\emptyset$ is zero when the PLL is in locked condition. The output voltage of the PFD, VPFD, can be calculated using Eq. (2).

$$\text{VPFD} = \left[\frac{\text{VDD} - 0}{4\pi}\right] * [\Delta\emptyset] \tag{2}$$

Thus, the gain of the PFD can be calculated using Eq. (3).

$$\text{KPFD} = \frac{\text{VDD}}{4\pi} \tag{3}$$

where KPFD = Gain of the PFD (V/rad).

3 Implementation of Phase/Frequency Detector

PFDs are always active in a PLL system, due to which consumption of power in the PFD is high [10]. Therefore, there is a need to design PFDs to minimize the power consumption and thus when integrated with the PLL, reduces the power consumption of PLL. The methods used to reduce power consumption are by using AVLG, reducing transistor count with the help of pass transistor logic and by eliminating the reset path by sharing the reference clock and VCO clock signal in the initial stages. The NOR gate-based PFD was also implemented, but since it performed better only at lower frequencies, the remaining architectures have been shown along with the corresponding results.

The PFD circuits are designed and implemented using Cadence Virtuoso, in GPDK 180 nm CMOS technology. Circuits are simulated using Cadence Spectre. This section deals with the implementation of proposed pass transistor-based PFD with AVLG and proposed PFD circuit without reset.

3.1 Pass Transistor-Based PFD

The PFD circuit can also be constructed by replacing the conventional CMOS transistors logic with the pass transistor logic. The alternative ensures that there is reduction in the power consumption in spite of the voltage degradation as it reduces the transistor count. Fig. 4 presents a pass transistor-based PFD circuit. The reference clock

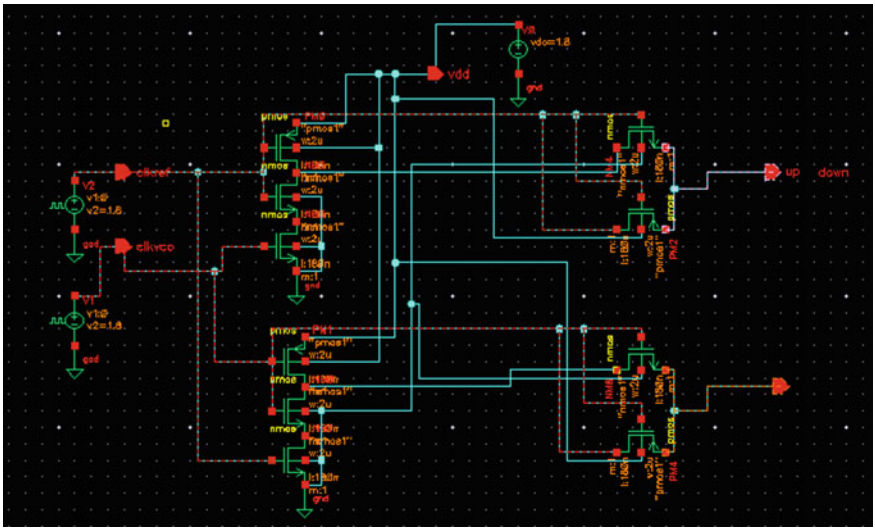

Fig. 4 Pass transistor-based PFD

signal that is the input to the upper half of the PFD is represented as 'CLK_REF' and the signal 'CLK_VCO' represents the input to the lower half of the PFD circuit. The outputs of the PFD are represented using 'UP' ad 'DOWN,' respectively.

3.2 *Proposed Pass Transistor-Based PFD with AVLG*

The pass transistor-based PFD with AVLG circuit has been achieved by incorporating the AVLG technique to the circuit shown in Fig. 4. AVLG increases the ground potential and thus help in reduction of power. Fig. 5 presents the AVLG circuit where "CLK" is a clock signal that is provided to the AVLG circuit. The AVLG circuits contain one NMOS and two PMOS transistors making the overall transistor count to three. This AVLG circuit is added to the pass transistor-based PFD circuit to minimize the total consumption of power. Instead of the circuit being directly connected to the ground, it is connected to the AVLG circuit and then that is connected to the ground. Fig. 6 represents the pass transistor-based PFD with AVLG where the inputs are represented by "CLK_REF" and "CLK_VCO" to the upper and lower halves of the PFD, respectively, and CLK is the clock signal for the AVLG circuit and the outputs of the PFD are represented by UP and DOWN.

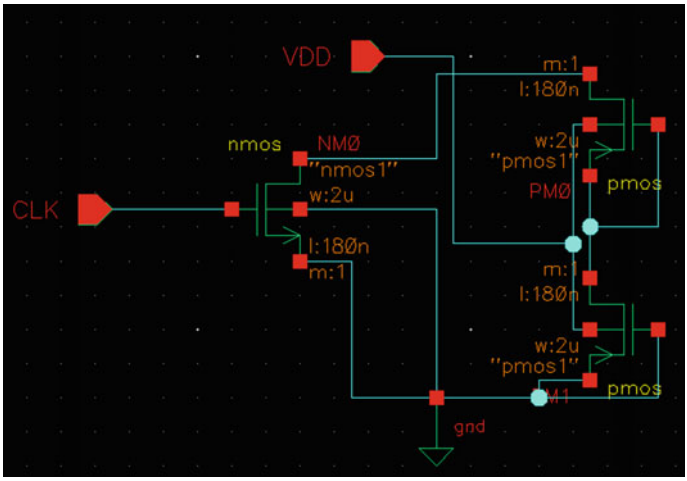

Fig. 5 Adaptive voltage level ground circuit

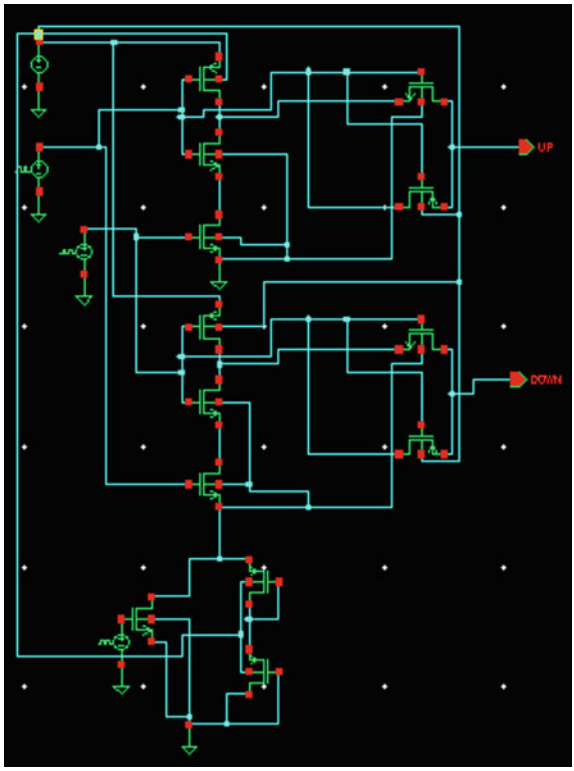

Fig. 6 Proposed pass transistor-based PFD with AVLG

3.3 Proposed PFD Circuit Without Reset Path

The usage of reset path in the implementation of the PFD circuit has always been a common factor. The reset path is a feedback line followed back to input line. The feedback or the reset path used in the circuit is the NOR gate. The NOR gate is fed with Up and Down outputs of the PFD, and the resulting output is given as one of the inputs at the initial stages. The usage of this reset path may be cumbersome sometimes due to increase in the usage of transistor which further increases the area consumed. Thus, the reset path can be replaced by sharing the reference clock and VCO clock signal in the initial stages itself [8]. This concept of replacing the reset path is carried out and a new design of PFD is proposed. The proposed PFD circuit without the reset path consists of 14 transistors and the PMOS and NMOS transistor count being at 8 each. Fig. 7 presents the Proposed PFD circuit without reset. The simulation results of reference and proposed PFD architectures are discussed in next section along with the power consumption of these architectures at operating frequency ranging from 100 kHz to 4 GHz with the supply voltage of 1.8 V.

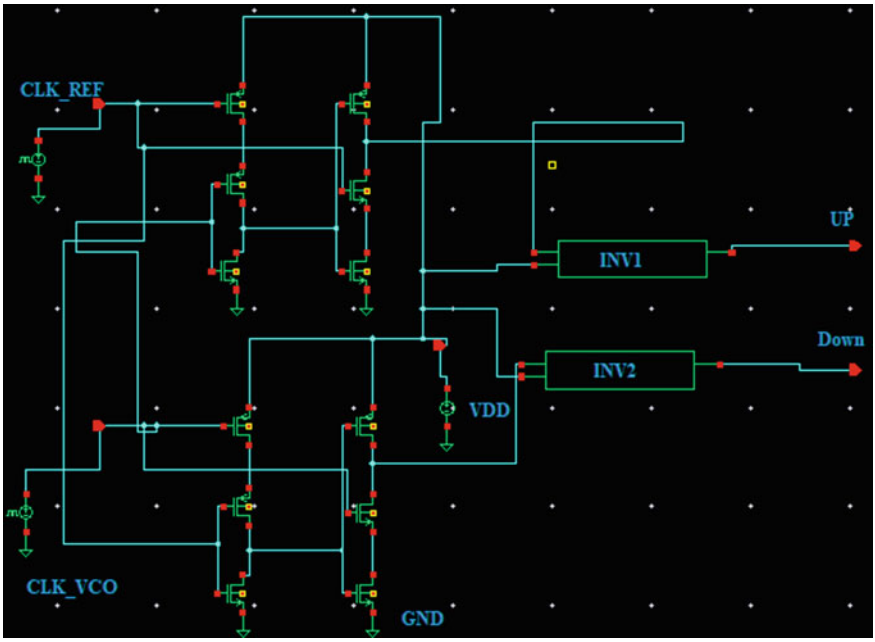

Fig. 7 Proposed PFD circuit without reset

4 Results and Discussions

The architectures of PFD circuits are implemented and have been discussed in the previous section. The simulation results and performance analysis of the circuits in terms of power consumption are discussed in this section. The simulation of the circuits has been done in the frequency range of 100 kHz to 4 GHz with a supply voltage for all the circuits been set to 1.8 V. Simulated waveform of the proposed pass transistor-based PFD with AVLG is shown in Fig. 8.

The simulated output is represented with the CLK_REF and CLK_VCO representing the first two waveforms where the clock signals are similar to another with delay given to the latter waveform. UP and DOWN outputs are represented by the third and fourth waveforms, respectively. The performance analysis has been done in terms of the transistor count and power consumption.

The architectures of PFD discussed in the previous section are now classified based on their operational frequencies into two sections. One, where the operational frequency ranges from 100 kHz to 2 GHz and the other deals with higher operational frequencies greater than 2 GHz. The first classification consists of architectures from [6] and the proposed pass transistor-based PFD with AVLG. The second class consists of architecture from [8] and the proposed PFD without reset path.

Table 1 lists the power consumption in μW at different frequencies. When

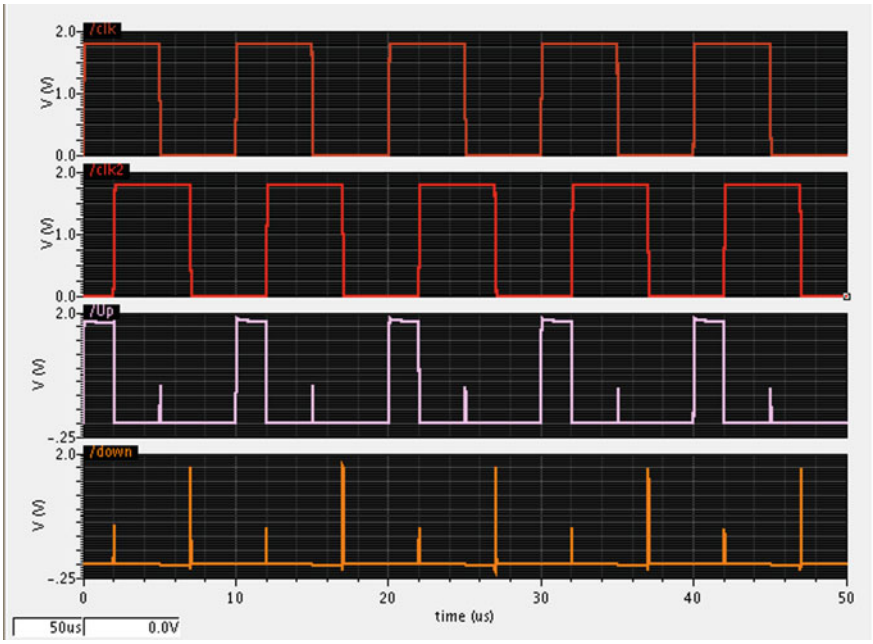

Fig. 8 Simulation waveform for pass transistor-based PFD with AVLG

Table 1 Power consumption of PFD architectures at different frequencies

PFD architectures	Power consumption (μW)			
	100 kHz	100 MHz	1 GHz	2 GHz
Pass transistor-based PFD [6]	1.021	7.86	84.88	175.2
Proposed pass transistor-based PFD with AVLG	0.858	7.68	81.72	147.7

compared to the architecture in [6], there is a 16% reduction in the power consumption. For frequencies in the megahertz to the gigahertz range, there is a change in the trend of power consumption, where the existing pass transistor-based consumes lesser power than the AVLG-based PFD. The architecture of PFD from [8] and the proposed PFD without reset path have been discussed in this section and their graphical comparison in terms of power consumption in μW has been represented at frequencies ranging from 1 to 4 GHz. Fig. 9 infers that the proposed PFD without reset consumes a power of 174 μW in comparison to that of [8] which consumes 356.5 μW at 1 GHz.

At lower frequencies, the usage of the proposed PFD without a reset path has a very slight effect on the reduction of power consumption, but as the frequency of operation changes to higher values, there is significant difference in the power consumption

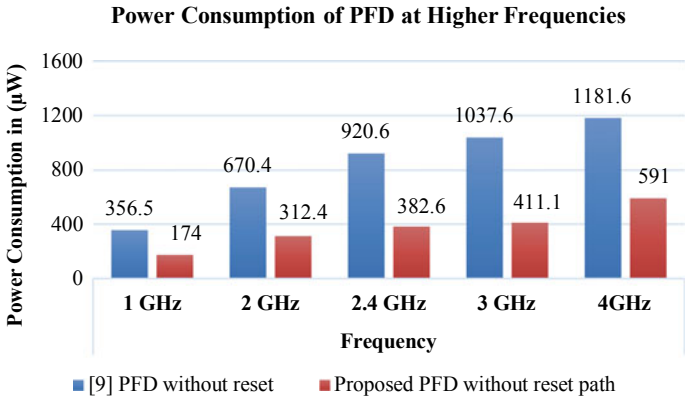

Fig. 9 Comparison of power consumption at different frequencies

between the architecture in [8] and the proposed PFD without a reset path. Almost a 50% reduction of power is a great aspect considering the high operational frequencies.

5 Conclusion

The work carried out in this paper is design and implementation of low-power PFD using the CMOS 180 nm technology. The performance of the PFD circuits mentioned is analysed in terms of power consumption in order to opt a more efficient PFD design for implementation of the PLL circuit. The PFD circuits have been implemented and simulated at a frequency ranging from 100 kHz to 4 GHz. At lower frequencies, the pass transistor-based PFD with AVLG consumes 16% lesser power in comparison to existing architecture. When the PFD operates at higher frequencies, the proposed PFD without reset consumes a very less power compared to PFD without reset [8]. The proposed pass transistor PFD with AVLG is more efficient than the existing architecture at frequencies ranging from 100 kHz to 2 GHz whereas the PFD without reset path is even operable at frequencies beyond 2.4 GHz. Though the power consumption is higher than the other proposed PFD circuit, the maximum operating frequency for the PFD without reset is very high. The future scope of this paper is to integrate proposed PDF along with other components to design a power efficient PLL circuit.

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Analysis of QCA-Based Serial Concatenated Convolution Coding Encoder for Error Correction

T. N. Dhanush, Vaishnavi S. Parashar, and B. S. Premananda

1 Introduction

SCCC is a class of FEC which is used for the efficient transmission of high-quality data over the noisy channels. SCCC is used to increase the reliability of the data that are transmitted. Since the error can be detected and corrected at the receiver, the need for retransmission is eliminated and thus improves the efficiency of the usage of bandwidth [1]. Such encoding technique is used to implement an encoder which can be used in the channel encoder part of the transmission end of the communication system.

SCCC encoder has three stages, namely Outer Encoder, Pseudo-Random Interleaver (PRI), and Inner Encoder. The Outer Encoder is a common (n, k, N) Bose Chaudhary Hocquenghem (BCH) Encoder, and the Inner Encoder is just a classical conventional encoder [2]. The paper summarizes some of the related works that are carried out and also portrays the path in which the proposed architecture is achieved.

The encoder can be implemented using several low power technologies. Some of the available technologies are CMOS, Reversible Logic, Adiabatic Logic, and Quantum-dot Cellular Automata (QCA). CMOS is used efficiently at the micron level, but as the technology tends toward nan level, these become very inefficient in design. Similarly, the Reversible Logic and Adiabatic become disadvantageous in terms of area occupied. To overcome these disadvantages, Quantum-dot Cellular Automata is preferred.

QCA is a transistor-less technique used to replace the transistor-based CMOS technology and is also found to be more efficient than the adiabatic logic in terms of energy dissipation [3]. The QCA circuits are operational at the nanoscale level and hence are preferred.

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The objective of the paper is to propose an area and energy-efficient QCA-based SCCC encoder for error correction. The proposed design in this paper is found to be more compact and efficient than the existing SCCC architecture. It was achieved through a thorough literature review of all the existing architectures. The organization of the paper is as follows: related works and basic QCA background are discussed in Sect. 2. QCA-based implementation of the proposed SCCC encoder is discussed in Sect. 3. The obtained results are analyzed in Sect. 4. Conclusions derived are discussed in Sect. 5 along with the references.

2 Related Works

The related works required to achieve the goal of the area and energy-efficient QCA-based design of the SCCC encoder are discussed in this section. The QCA logic involves the construction of a basic logic gate using the majority voter gate along with the most basic and more commonly used inverter gates. These majority voter and inverter gates function as the building blocks in QCA [4]. The majority voter gates and inverter gates are used to implement a 2:1 multiplexer which is further used to implement D flip-flops.

The architectures of the multiplexers from [5] are used to design D flip-flops. Designed D flip-flops are used to implement shift registers which are efficient than the ones in [6, 7]. These shift registers are basic blocks of the serial-to-parallel converter (SPC) and parallel-to-serial converter (PSC) that are further used in the Outer Encoder and PRI stages of the SCCC encoder.

SCCC encoder plays a vital role in the communication domain where data security has become one of the important criteria to be fulfilled for efficient transmission of the data between the source and destination. The proposed SCCC encoder is a derivative of the encoder in [2] which is improved by reanalysis and reusability of the cells available. The existing circuits are implemented and are then compared with the proposed encoder circuit.

The implementation of the required SCCC encoder has to be carried out using QCA logic. The QCA logic mainly includes QCA cell, majority voter, inverter, and crossovers along with the simulation engines. The QCA cell acts as the primary unit of QCA. These cells are used to implement majority voter and inverter gates. The QCA cell is shown in Fig. 1. The two aspects of the cell, electron and dots, are observed in Fig. 1. The majority voter gate is a three-input and one-output gate with five cells in total.

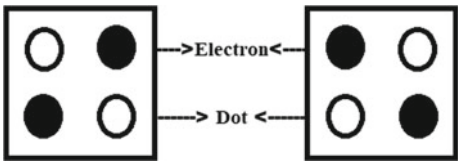

Fig. 1 QCA cell with electron and dot representation

An inverter gate is obtained by placing two cells diagonally at 45° to one another which results in the output to be in inversion to that of the input. In addition to the majority voter gate and inverter gate, the crossovers play an important role in the implementation of the circuits. The crossovers are of two types namely multilayer and coplanar [8]. Multilayer crossover as the name suggests is a kind of crossovers in which multiple layers are used for two different input arrays, whereas the coplanar is the one in which all the cells are along the same plane. Two different kinds of simulation engines are used in QCADesigner, namely Bi-stable approximation and Coherence vector.

3 Implementation of Proposed SCCC Encoder

This section summarizes the operation of these three stages along with their QCA-based implementation and performance analysis of these circuits. The implementation of the proposed SCCC encoder is performed using the CAD tool, QCADesigner 2.0.3. The SCCC encoder is implemented in QCA logic using the concept of bottom-up approach where the primary blocks are used to design the fragments of the SCCC encoder such as the Outer Encoder, Interleaver, and Inner Encoder. The Interleaver constructed here is pseudo-random. The SCCC encoder operates at three stages, namely Outer Encoder, Pseudo-Random Interleaver (PRI), and Inner Encoder [9]. The block diagram representation of the SCCC encoder is shown in Fig. 2.

Outer Encoder

The Outer Encoder is the first stage of the SCCC encoder where the message bits are given as inputs and the systematic codeword is the required output obtained. The Outer Encoder usually consists of a 4-bit SPC, parity bit generator, and the 3-bit PSC. The first stage of the Outer Encoder is the 4-bit SPC which converts the serial form of the data message bits into parallel form. The input message bits (D) which are 4-bit data are fed to the SPC, and then, it converts the serialized message bits to parallel form [A_0, A_1, A_2, A_3]. Figure 3 represents the QCA-based design of a 4-bit SPC. D represents the message bits to be transmitted.

In Fig. 3 $A3$, $A2$, $A1$, $A0$ are the outputs of the SPC, i.e., the parallelized output for the serialized message bits. The second stage of the Outer Encoder is the parity bit generator, used to generate parity bits. The generated parity bits are used at the receiver end to see if the received bits are error-free. The parity bit generator is constructed using modulo-2 adders [10] to generate a 3-bit parity code using the

Fig. 2 Block diagram of SCCC encoder

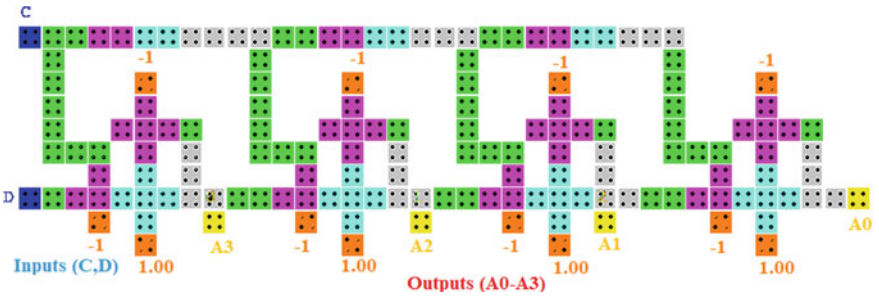

Fig. 3 QCA-based design of 4-bit SPC

4-bit output of the SPC. Figure 4 represents the QCA-based implementation of a parity bit generator where $A3$, $A2$, $A1$, and $A0$ are the inputs and $R2$, $R1$, and $R0$ are the required parity bits. The last stage of the Outer Encoder is the 3-bit PSC where the generated parity bits are serialized to be combined with the parallelized output of the SPC and obtain the required systematic code word.

At the Outer Encoder stage, the parity bits $R2$, $R1$, and $R0$ which are parallel are converted into a serial form, represented as R. Figure 5 depicts the 3-bit PSC where the parity bits $R2$, $R1$, and $R0$ act as inputs to the PSC and R as the serial output of the PSC. This output, R, is then connected to the message bits which results in the systematic codeword (C). Figure 6 represents the complete QCA-based design of an Outer Encoder.

Figure 6 represents the overall design of the Outer Encoder where D is the initial input to the Outer Encoder with $A3$, $A2$, $A1$, and $A0$ acting as outputs of SPC. $R2$,

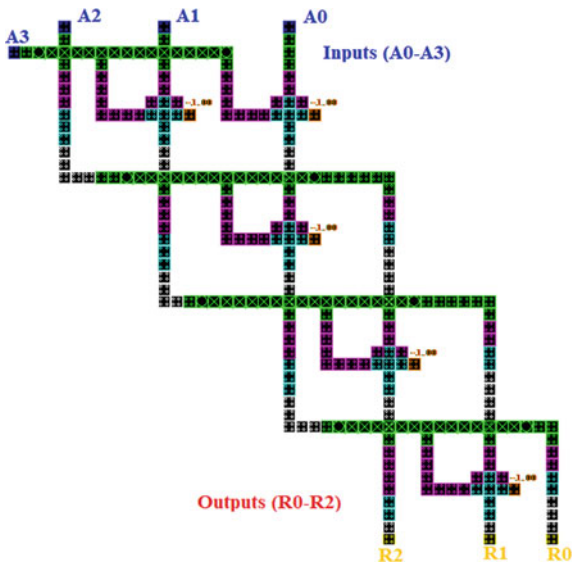

Fig. 4 Proposed QCA-based 3-bit parity bit generator

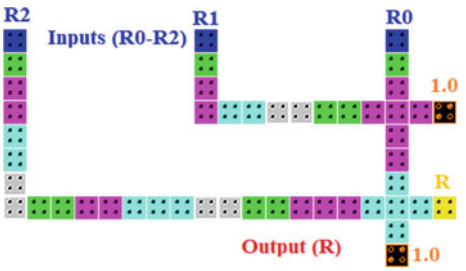

Fig. 5 Proposed 3-bit parallel-to-serial converter

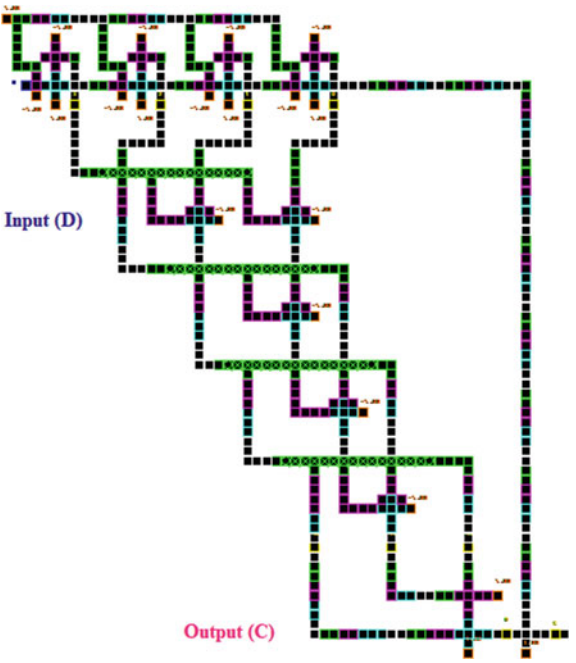

Fig. 6 QCA-based Outer Encoder

$R1$, and $R0$ are the outputs of the parity bit generator, whereas R is the output of the PSC, and C (systematic codeword) is the final output of the Outer Encoder.

Pseudo-Random Interleaver

Interleaver is a data mixing part of the SCCC encoder where the systematic codeword is disorganized using a 7-bit PRI. The Interleaver consists of two stages, namely SPC and PSC (both 7-bit). The SPC first parallelizes the systematic codeword C as $C = [C0, C1, C2, C3, C4, C5, C6]$ into seven separate values where $C6$ and $C0$ are the MSB and LSBs, respectively. The parallelized bits are now interchanged and interchanged upside down, and the resulting output is then again serialized using the PSC (7-bit) resulting in a permuted codeword (I) [1].

The combination of these PSC and SPC makes the inert-leaver pseudo-random in nature hence the name PRI. Figure 7 represents the QCA-based design of 7-bit PRI where the systematic codeword (C) from the Outer Encoder is the input to the SPC and is parallelized, and then, the parallelized set of 7-bits are fed into the 7-bit PSC that serializes the 7-bits to form the permuted codeword (I).

Inner Encoder

The final stage of the SCCC encoder is the Inner Encoder; it provides two sets of outputs. The QCA-based design of an Inner Encoder is given in Fig. 8. The permuted codeword is the input to the Interleaver and $Y1$ and $Y0$ are the expected outputs.

The previously discussed components of the SCCC encoder are integrated efficiently to obtain the overall structure of QCA-based SCCC encoder which is shown

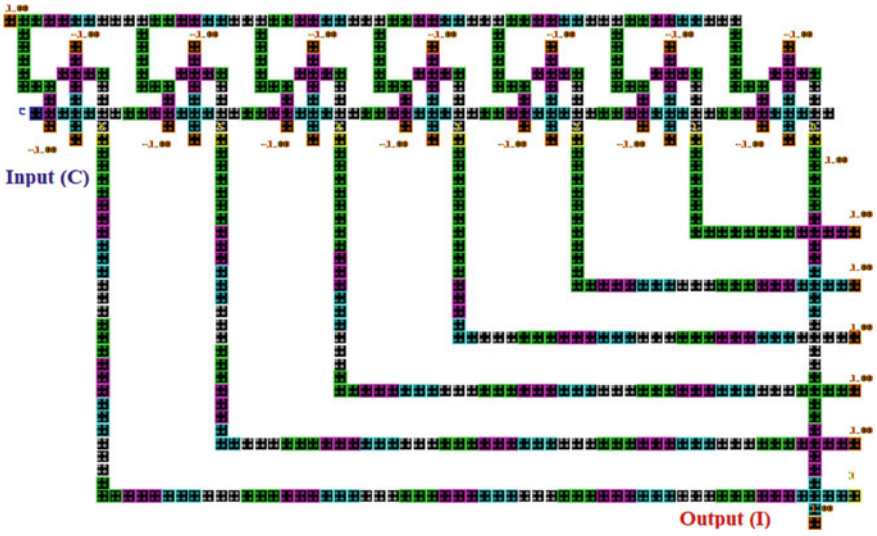

Fig. 7 QCA-based design of 7-bit PRI

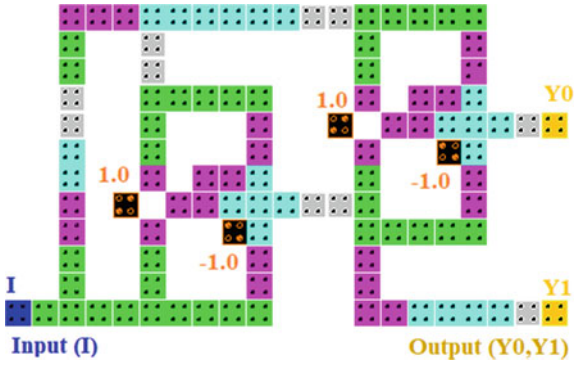

Fig. 8 Proposed QCA-based design of Inner Encoder

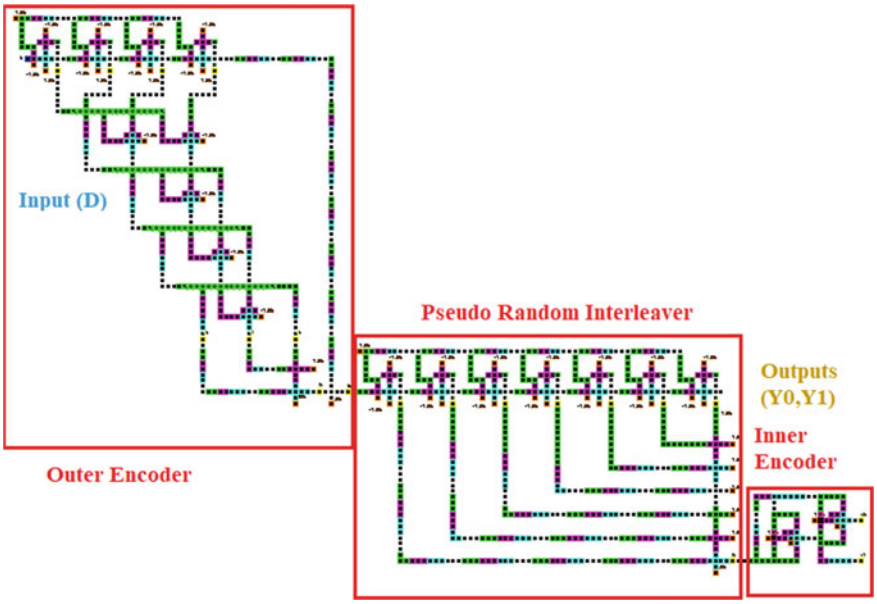

Fig. 9 QCA-based SCCC encoder

in Fig. 9. The three stages of the encoder are first designed and then are integrated serially to ensure the flow of data from the Outer Encoder stage to the Inner Encoder stage through a PRI which is the intermediate stage.

Figure 10 shows the resulting waveforms at end of every stage of the SCCC encoder. The input message (1011) is fed as input to the encoder at the primary stage (OE), and the resulting output from the intermediate stage (PRI) is shown in the second waveform. The final two waveforms represent the outcomes ($Y0$ and $Y1$) of the encoder at the Inner Encoder stage $Y0 = 1101001$ and $Y1 = 1110011$.

4 Results and Discussion

The QCA-based SCCC architectures are simulated using the QCADesigner 2.0.3. The obtained cell count, area occupied, and energy dissipation of the reference and proposed SCCC architectures have been discussed in this section.

Figure 11 represents the cell count comparison of components of proposed and existing SCCC encoder architecture in [2] such as parity generator, Outer Encoder, Interleaver and SCCC encoder, etc. The proposed SCCC encoder shows a reduction in cell count with 1325 cells which is 975 cells lesser than the [2] which has a total of 2300 cells. The overall reduction in the cell count was achieved as a result of the reanalysis of the existing logic and increasing the reusability of the available cells.

Figures 12 and 13 represent the comparison of components of SCCC encoder

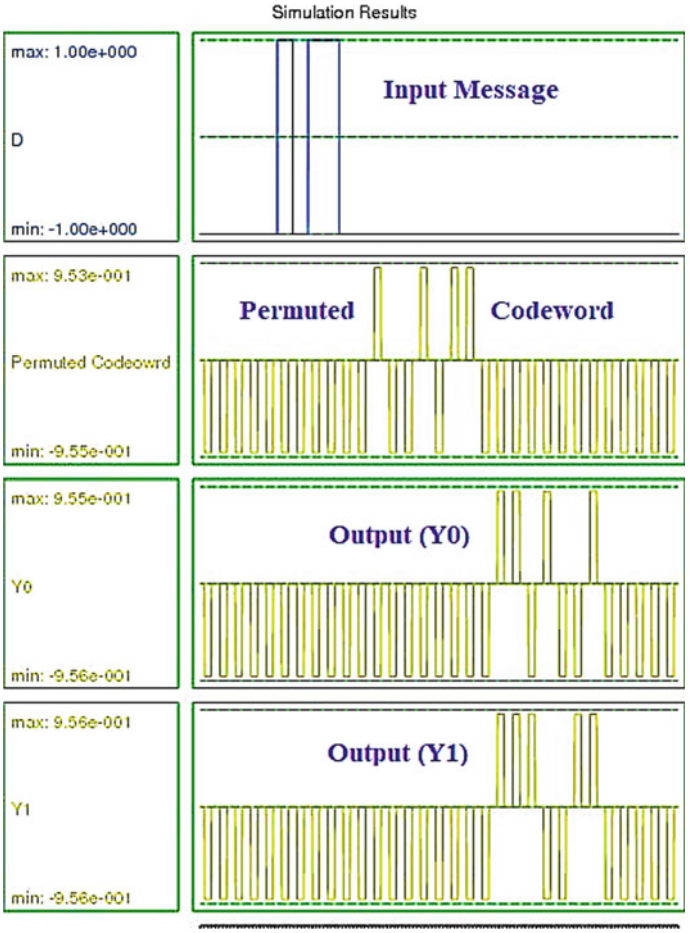

Fig. 10 Simulation results of the SCCC encoder

such as parity generator, Outer Encoder, Interleaver, and integrated SCCC encoder, in terms of area occupied and energy dissipated, respectively. Figure 12 shows the overall comparison of the SCCC encoder and its components in terms of the total area occupied. The proposed SCCC encoder occupies an area of 2.78 μm^2 (40%) lesser than the SCCC in [2] which occupied an area of 4.56 μm^2.

Figure 13 illustrates the comparison between the proposed and reference SCCC encoder in terms of energy dissipation. The SCCC encoder in [2] has an energy dissipation of 0.38 eV, whereas the proposed has energy dissipation of 0.245 eV, i.e., 35.5% more efficient.

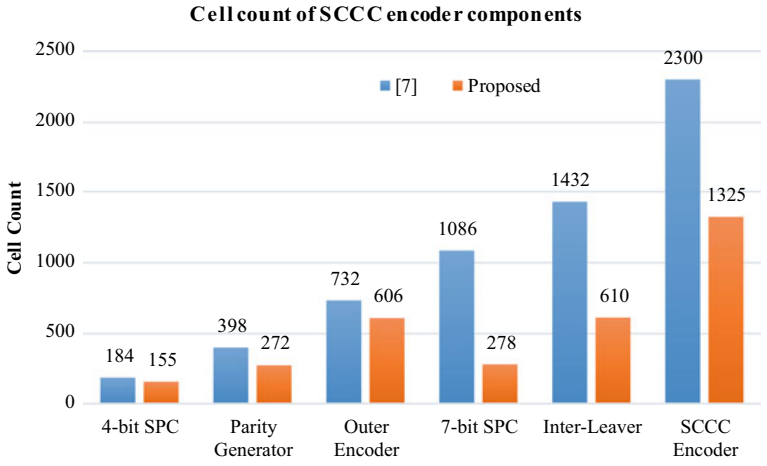

Fig. 11 Comparison of cell count of components of SCCC encoder

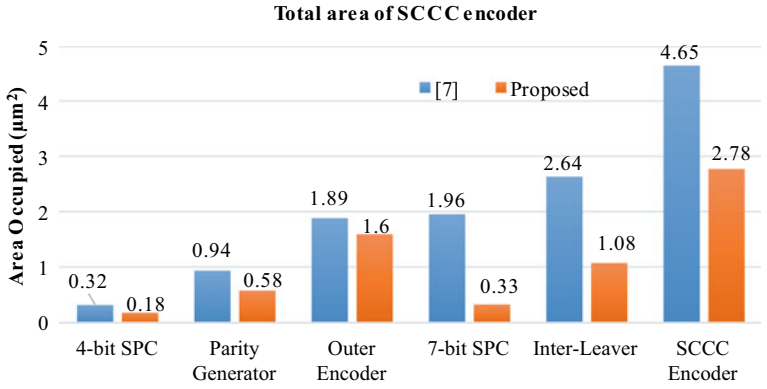

Fig. 12 Comparison of area occupancy of components of SCCC encoder

5 Conclusion

This paper proposes a design of the area and energy-efficient implementation of QCA-based SCCC encoder. The SCCC encoder has a vital role in digital communication where the data transmission without any external interference is a must. The SCCC is the integration of the Outer Encoder, Inner Encoder, and Pseudo-Random Interleaver. The proposed SCCC encoder is 42.39, 40, and 35.5% more efficient than the SCCC encoder [2] in terms of cell count, area occupancy, and energy dissipation, respectively. The future scope of the work is to design a SCCC encoder with an even higher range of BCH encoders and Interleaver. The BCH encoders can also be implemented using other higher forms such as (15, 11, 1), (15, 7, 2), and (31, 16, 3).

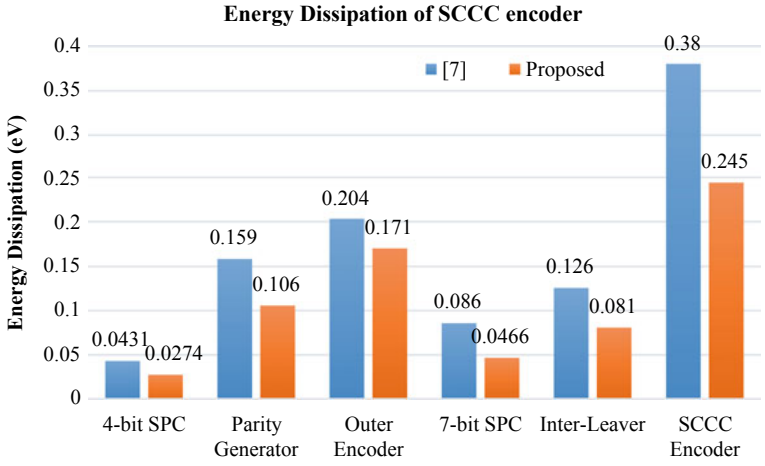

Fig. 13 Comparison of energy dissipation of the components of SCCC encoder

These BCH encoders can be supported by CC encoders of higher bits implemented in the Inner Encoder.

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Performance Evaluation of Master–Slave D Flip Flop Based on Charge Retention Feedback Pass Transistor Logic in Nanotechnology

Sweta Tripathi, Anum Khan, and Subodh Wairya

1 Introduction

In this era of digitalization and multitasking, power-efficient multi-functioning portable gadgets cover huge market area of VLSI designs and hence, the gadgets should be area efficient with longer battery life. The advancement in VLSI technology with scaling shows that the chips are getting denser and could be implemented on that tiny chip. Besides that, the latency of circuits must be reduced because of the compact time account at high-frequency operation. The latches and flip flops are the fundamental element for sequential and synchronous system in terms of power consumption. Flip flops are the basic storage module in all digital systems, utilizing major portion of static and dynamic power. The clocked devices devour large amount of total active power in digital systems. Flip flop's performance is compared by area, delay and power consumption [1] in designing System on Chips (SoCs) and there is trade off among these parameters. The area is determined by the components used, size of device and routing techniques used. The power factor is decided by supply voltage, switching activity and charge leakage due to the presence of unnecessary components. In digital electronics, a flip flop or latch is bi-stable circuit and there states can be changed by the signals applied to control the inputs. The D Flip Flop and latches are level sensitive and as the clock becomes active HIGH, transparency is achieved for entire level of HIGH clock so as to transfer input data to output in that period of time. These flip flops cover a wide range of application area such as shift registers, finite-state machine, pulse counter and for synchronizing fluctuating-timed input signals to some reference timing signal. These low power and high-speed circuits are used in sequential circuits and microprocessors [2].

In this paper, two power-efficient D flip flops are proposed based on charge retention feedback pass transistor logic designed by analyzing C^2MOS FF [3–5],

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CPLSDFF and CPLDDFF. It includes both static and dynamic structures named as CRPLS-DFF and CRPLD-DFF, respectively. Also, there is no use of transmission gate in the proposed circuits and therefore clock load issue is not present here. The limitations of transmission gate can be seen through a conventional Power PC 603 FF [6] reported in this paper for comparison purpose.

This paper is organized in 5 sections. Section 1 depicts the introduction to flip flops, there functioning and issues. Section 2 talks about the literature reviews of the flip flops designed and selection of conventional and latest flip flops for comparison with the proposed work in terms of area, power, temperature dependency and delay. Section 3 describes the techniques implemented in designing the proposed flip flops (CRPLS-DFF and CRPLD-DFF). Here, proposed design is discussed in detail regarding the parametric values and purpose of each component utilized in the system. Section 4 presents the simulation results and comparative graphical plots and Sect. 5 is the final conclusion of the proposed work.

2 Flip Flop Design Approach

Numerous flip flop architectures have been proposed over the years, each having its own merit and demerit. Also there is necessitate to follow the setup time and hold time [7] so as to avoid faulty data at output due to transmission error. The master–slave flip flops are used to evade race conditions and hold the data stored at the negative edge of clock during low clock level. The clock conditions are pursued as per the setup and hold time rules so as to authenticate that the input data transmitted and hence the race conditions are avoided. The setup time is defined as the time span just before the clock signal is arrived and during that time, the data should be stable so as to avoid transmission of faulty signal. The hold time is the time span on which the data must be held stable after the clock event, for reliable sampling [8]. A conventional clocked CMOS flip flop (C^2MOS FF) based master–slave structure presented in Fig. 1. The master segment is active in the first period of the clock cycle; on the other hand, slave section is active in second period of the clock cycle. The operation of C^2MOS based D flip flop can be elaborated by considering the case when CLK is at high level with low input D signal then the master stage is active and the pre-charging the node M1 to VDD and feedback to the inverter (T5, T6) at node M2. When the circuit works in active mode, consumes excess run-time power. In idle mode, there is unnecessary static power consumption as charge leaks through transistors T13 and T14 and unwanted switching needs to be done in order to store charge in pull-down network. The next stage of the C^2MOS FF design is slave stage and is active when clock is in low phase and whatever the value was stored at M2 was forwarded to Q output. Due to the issues mentioned above, power consumption, delay and area are more in the conventional C^2MOS FF circuit.

Power PC 603 FF (Fig. 2) [6] is one of the most proficient static designs with the merit of low-power keeper architecture and low latency straight output path eliminating huge leakage charge and hence power. The major limitations are the

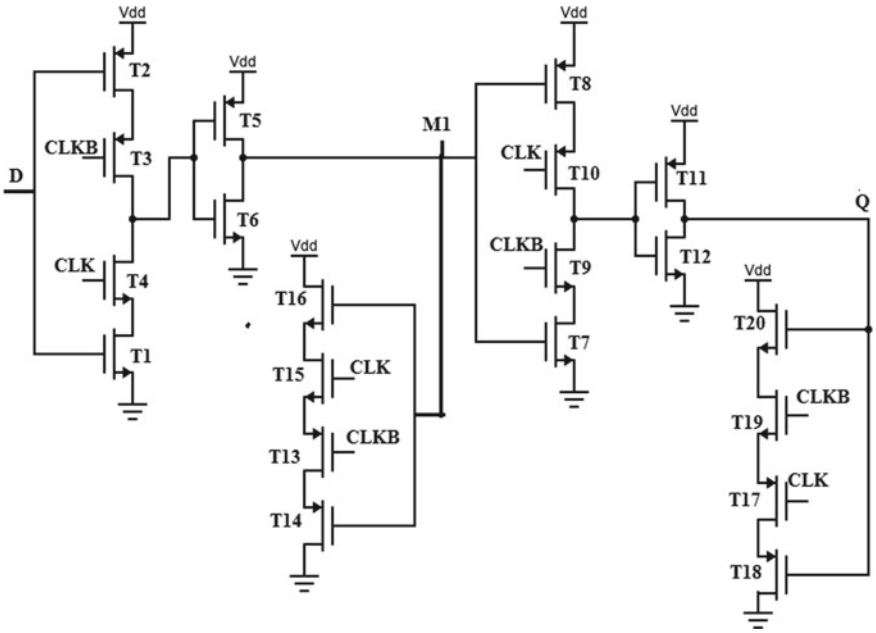

Fig. 1 C^2MOS master–slave D flip flop circuit [5]

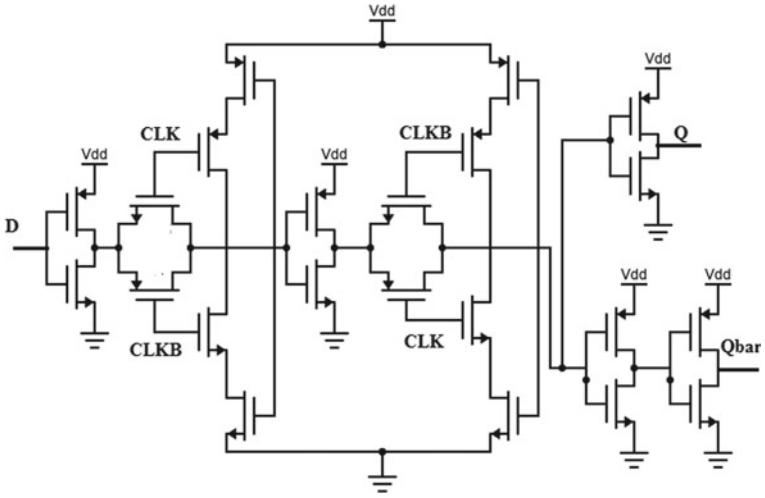

Fig. 2 Power PC 603 FF [6]

increased D–Q delay as a result of positive setup-time with the heavy input and clock nodule, affecting the performance efficiency. However, static system is still favored where low power is the prime concern regardless of all these limitations.

Figure 3 shows semi-dynamic flip flop (SDFF) [9] with a demerit of huge power dissipation due to the addition of heavy capacitors, overloading the circuit. The circuit design is simple; however, the superfluous switching activity is the main cause of power loss. After deep analyzing of SDFF, it can be seen that charging and discharging of inner node X is the major cause of power dissipation in spite of high logic stable input. Glitches may cause noise problem at the resulted side.

Figures 4 and 5 show two latest conditional pass transistor-based static as well as dynamic master–slave D flip flop [10]. The drawback of these designs is large capacitor value in transitional path and an excess data to output delay as of positive setup time. The total efficiency of the system is affected as per issues mentioned above. But the design is still favored for system if the power saving is a prime factor instead of speed.

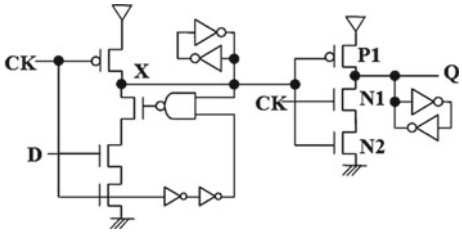

Fig. 3 SDFF [9]

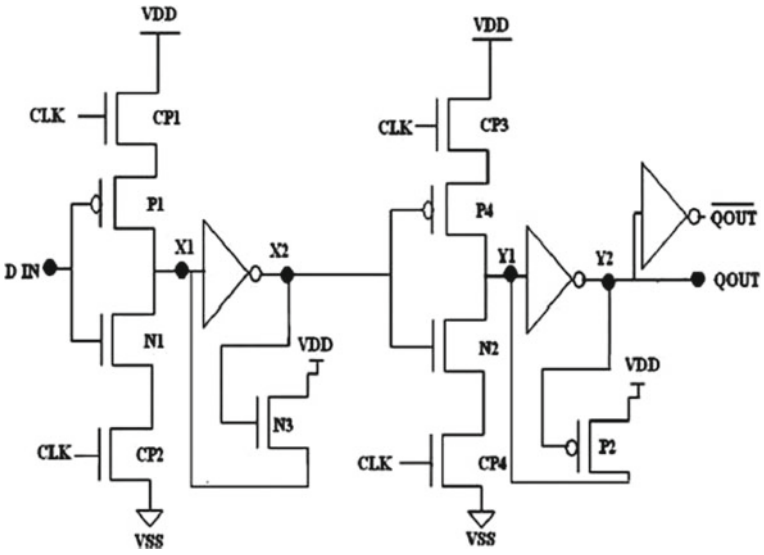

Fig. 4 CPLSDFF [10]

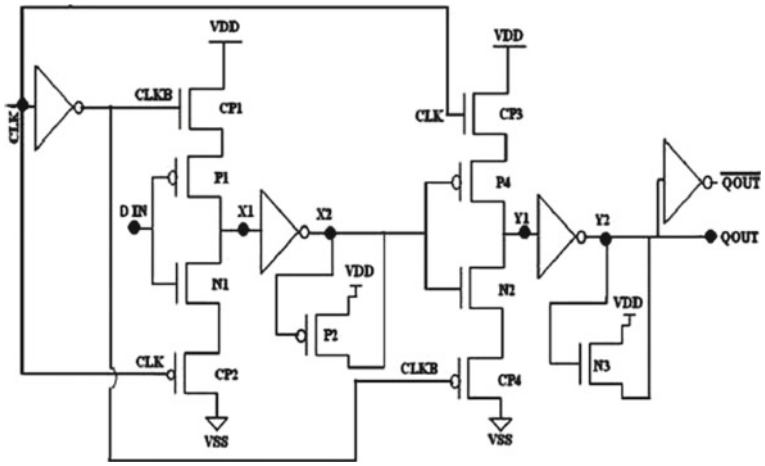

Fig. 5 CPLDDFF [10]

The hybrid latch Flip flop (HLFF) is appropriate for system where minimum power requirement is the key concern as compared with SDFF with the penalty of high-speed reduction. HLFF [11, 12] possesses more positive hold time as shown in Fig. 6. The main issue is the superfluous parasitic capacitance on the intermediate and there is instability in system with excess number of nmos transistor mounted at output stage in the pull-down path. The former issue causes speed reduction in comparison with the SDFF and not appropriate to propose intricate sequential circuits due to the increased D to Q delay.

The dual dynamic D Flip flop [13] as shown in Fig. 7 consists of a pseudo-dynamic intermediate structure and a dynamic output stage composed of high-speed system as compared with the SDFF and HLFF. The main merit is less power dissipation, negative setup time and enhanced hold time that makes the input to output delay (D–Q) as minimum as possible. The pre-charge phase of the semi-dynamic node

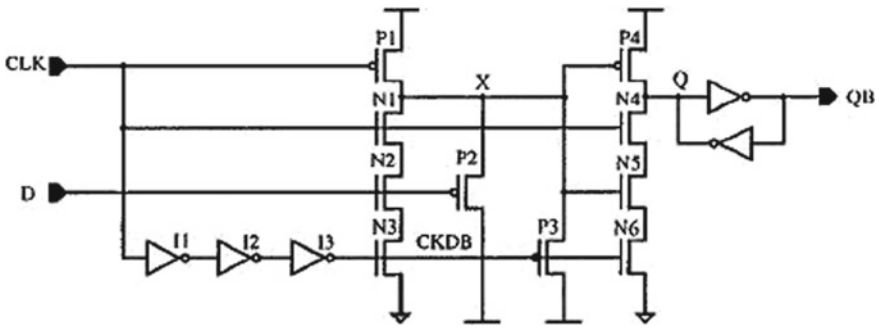

Fig. 6 HLFF flip flop [11]

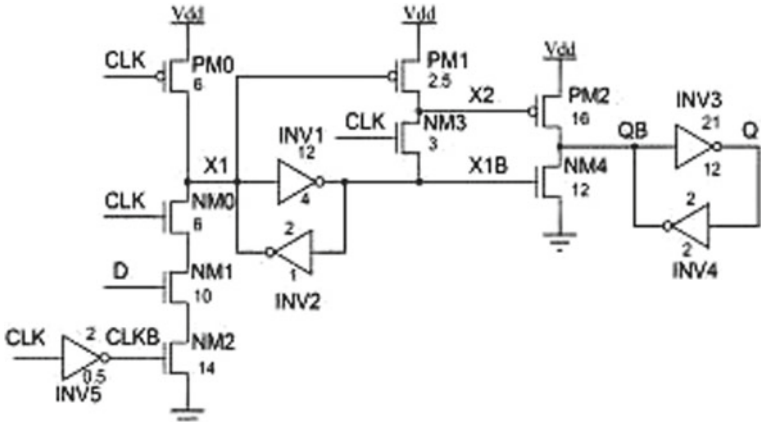

Fig. 7 Dual dynamic flip flop [13]

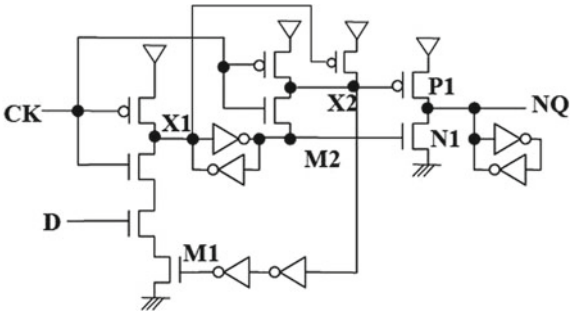

Fig. 8 Cross charged couple flip flop [14]

M1 is unstable because of the parasitic capacitance formed in the master stage with different data and clock conditions.

In XCFF [14] as shown in Fig. 8, the redundant events are avoided with the introduction of two dynamic nodes. Since the dynamic node is split into two, power consumption is reduced without compromising the speed. It has comparatively low clock driving load. It also produces smaller power-delay products than other sequential CMOS flip flops. XCFF reduces the power dissipation by selectively switching the output pull-up and pull-down transistors separately at every cycle of the clock.

Another flip flops are reviewed on the basis of power, delay and area parameters. Multi threshold D flip flops [15, 16] are designed to reduce leakage power in deep sub-micron. The high threshold transistors are used as sleep transistors and these sleep transistors work as a virtual supply gate to the main logic circuit and reduce leakage during sleep mode or idle mode. But this method is advantageous only if the idle period is more. Also sizing of sleep transistor is an issue. A complex charge retention circuit is needed to retain the charge stored in the circuit when transition takes place from active to sleep and sleep to active mode. Autonomous Data Retention Flip Flop [17] is used to reduce power consumption when the circuit is in sleep and

idle mode for long time, but the disadvantage is that it increases the size of circuit due to increased size of high threshold sleep transistors. More power consumption takes place when the circuit transitions from active to sleep mode and vice versa. Here, sizing of sleep transistors is difficult to analyze with increased layout area. Single edge-triggered Master–slave register was designed, but number of transistors is more and high capacitive load attached to the clock signal [18]. Each register has a clock load of eight transistors. One outlook to reduce the clock load at the cost of fortitude is to make the circuit rationed.

Out of these reviewed flip flops, four flip flops C^2MOS FF, Power PC 603 FF, CPLSDFF and CPLDDFF are chosen for showing the efficiency and robustness of proposed circuits by the comparative analysis on the basis of parameters such as power, delay, area, temperature sensitivity and technology scaling. C^2MOS FF is selected as a base architecture in proposed design, while power pc 603 FF is simulated in order to present the limitations of transmission gate. Due to the use of transmission gate, the circuit becomes heavy and hence data transmission is delayed with excess heat generation. CPLSDFF and CPLDDFF are preferred as these are the latest designs reported.

3 Proposed Work

Considering structural issue in conventional C^2MOS master–slave D flip Flops, charge retention feedback pass transistors based static (CRPLS-DFF) and dynamic master–slave D flip flops (CRPLD-DFF) are designed by modifying the charge restoring feedback path and using low threshold transistors in critical path shown in Figs. 9 and 10. The major concern in proposed design was the use of capacitors in transitional nodes that might create huge delay due to charging and discharging in active mode. But this issue was resolved through low threshold transistors used in critical path of the circuit compensating the overall increased delay in the system. Here, critical path defines the shortest path between the transitions of data to output. The minimum value of capacitors used in dynamic circuit is 10 fF at 45 nm technology node so as to maintain the efficient charging and discharging swing upto 80% in transition period without overloading the system. Low value of capacitors is taken in order to reduce layout area without affecting the efficiency of proposed design. The capacitors used in 90 and 180 nm are of value 50 fF and 100 fF, respectively. Hence, we can say that proposed system is preferable for low-power applications where speed is not the major concern. The overall effectiveness of the design is a function of setup time, hold time, CLK conditions, switching activity and parasitic capacitances. All these parametric concerns are resolved successfully.

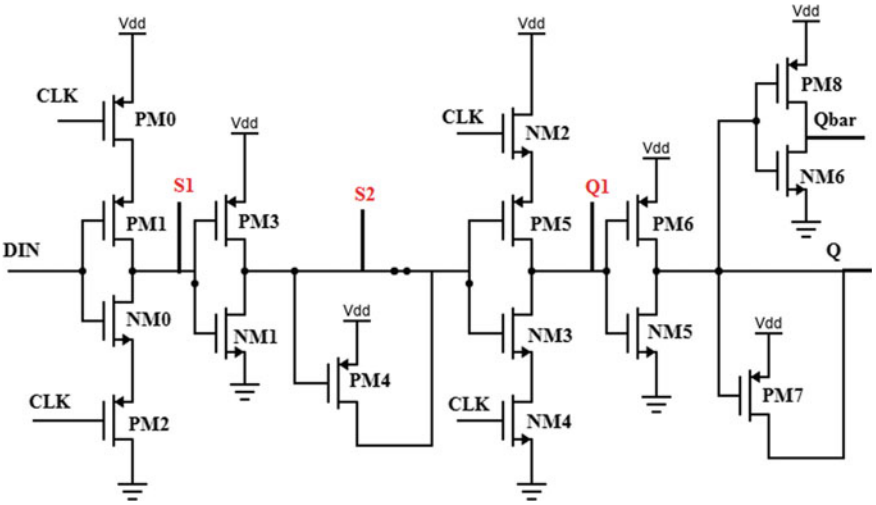

Fig. 9 Proposed CRPLS-DFF circuit

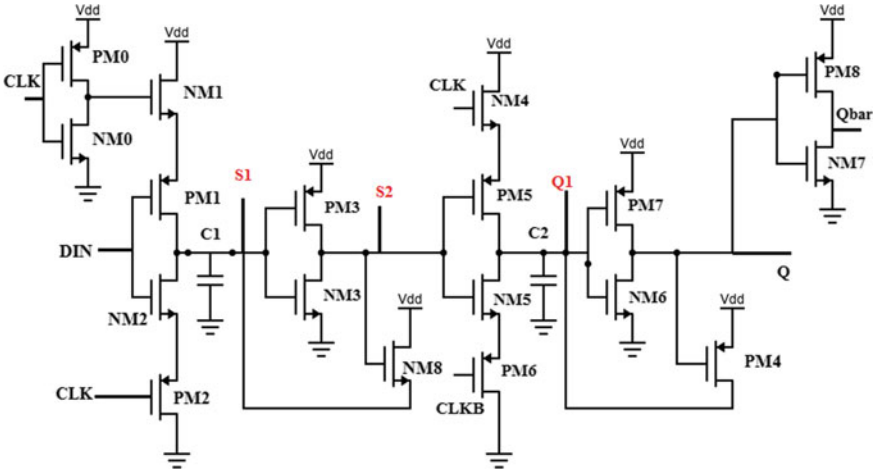

Fig. 10 Proposed CRPLD-DFF circuit

3.1 Charge Retention Pass Logic Static DFF (CRPLS-DFF)

In CRPLS-DFF shown in Fig. 9, the intermediate node state S1 depends upon the input and initial CLK triggering. The clock load has also been reduced in the proposed system because number transistors loading CLK signal is 4 as compared to 8 or more in other master–slave D Flip flops designed. It can reduce the power consumption through CLK load by limiting the transistor switching up to 50%. When clock is LOW

then the logic is retained in the output due to feedback transistors PM7. When CLK signal is high then the circuit output changes as per the input conditions applied and whatever the value stored in master stage is transferred to slave stage after maintaining the setup and hold time between clock pulse and input pulse. Considering the case of LOW CLK signal with Din as LOW logic, transistors PM0, PM1 and PM2 are on, forcing node S1 to logic HIGH. PM4 is the charge retention feedback pass transistor meant for the purpose of data retention at node S2 till the slave stage is active.

When Din is HIGH and CLK is LOW, transistors NM0 and PM0 and PM2 are ON, discharging the node S1 making it LOW logic. In both the input conditions, there is no undeviating way for charge leakage as mentioned in conventional C^2MOS FF where charge leaks via nMOS transistors connected in series discussed in [4]. If clock is at a HIGH level, the transistor NM2 and NM4 are on and whatever logic sustained at S2 is transferred to slave stage. Output is sustained in case of low CLK signal. In slave stage, Q1 is the intermediating node from where logic is forwarded to output level and PM7 is mount for logic retention pass transistor.

3.2 Charge Retention Pass Logic Dynamic DFF (CRPLD-DFF)

The proposed CRPLD-DFF mentioned in Fig. 10, using dynamic characteristic as it uses capacitors for holding charge in order to maintain logic in intermediating nodes. The capacitances used here are of 10 fF playing significant role in order to get full charging and discharging swing for errorless data transmissions in each stage. CRPLD-DFF architecture uses two phases of clock (CLK and CLKB). The node S2 depends upon the status of input and clock. When clock is equal to LOW then NM1 and PM2 are on and for CLK at logic HIGH, NM4 and PM6 are active. If Din is LOW, then S1 is charged to VDD and hence S2 is LOW and vice versa. There is no path for charge leakage due to feedback nMOS keeper circuit mounted in master stage and similarly PM4 is there for slave stage. In the next clock cycle i.e., positive cycle, if the logic retained in master stage was LOW, then Q1 pre-charged to VDD and output is maintained LOW. Suppose if the logic maintained at master stage was HIGH and clock goes HIGH, then Q1 is discharged and hence output is turned into HIGH logic.

4 Simulation Results and Discussion

The performance of proposed work and existing flip flop designs has been analyzed by simulating 45 nm technology at 27 °C. Figures 11 and 12 show the simulated input–output waveform of Power pc 603 FF and C^2MOS FF, respectively. Also the proposed work is evaluated with the latest design of CPLSDFF and CPLDDFF

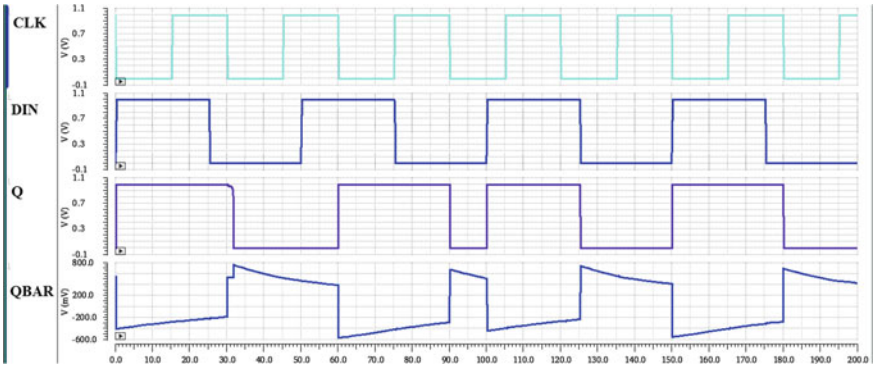

Fig. 11 Simulated input–output waveforms of the power PC 603 FF [6]

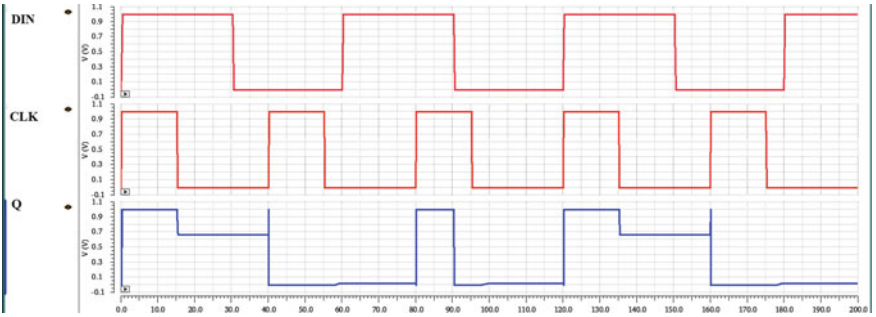

Fig. 12 Simulated input–output waveforms of the C^2MOS FF [5]

reported in [3] and is illustrated in Figs. 13 and 14. The simulated input–output waveform of proposed work (CRPLS-DFF and CRPLD-DFF) is demonstrated in Figs. 15 and 16, respectively, illustrating that it works as an edge-triggered master–slave flip flop where whatever value is stored at the last edge of the pulse is transferred to the next stage i.e., from master to slave and from slave to output.

Temperature disparity of proposed system on the basis of average dynamic power and static power is investigated through Figs. 17, 18, 19 and 20, presenting that the circuit is temperature insensitive as there are negligible fluctuations in measured values. Power consumption and delay are the determining factors for the efficient performance of the master–slave flip flop. Hence, these parameters are calculated and compared to confirm the superiority of proposed circuits over conventional flip flops. All the simulations presented in this paper are with a minimum voltage of 1 V. The voltage can be further reduced to 750 mV, but the output gets somewhat distorted and in case of increased voltage, the simulation results are more accurate but the power consumption exceeds which is not economical.

Table 1 shows the comparative values of the implemented flip flops considering average dynamic power, static power, CLK-Q (clock to output) delay and D–Q (data

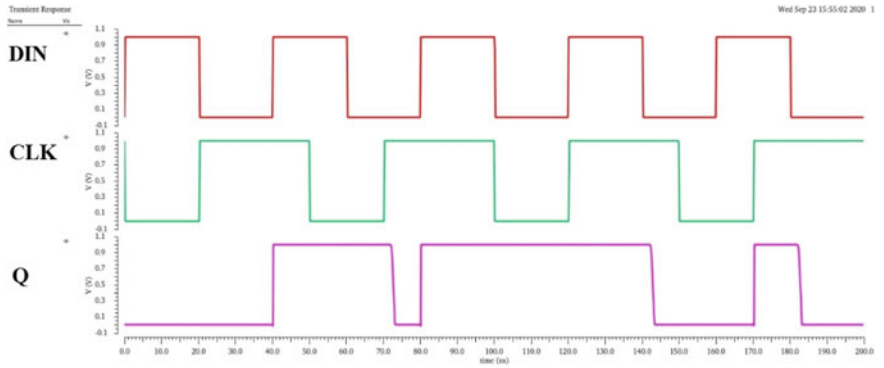

Fig. 13 Simulated input–output waveforms of the CPLSDFF [10]

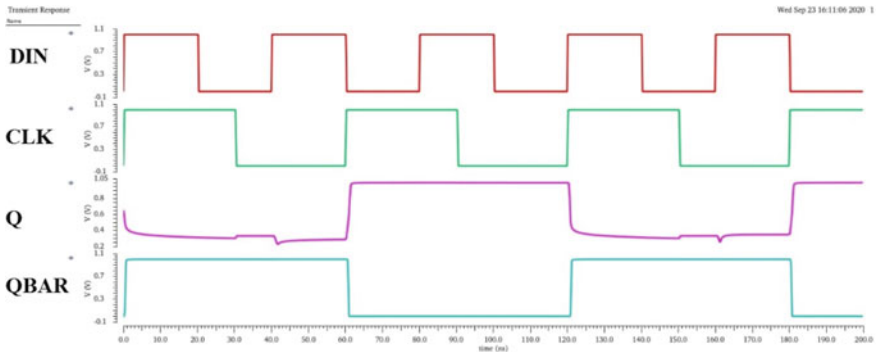

Fig. 14 Simulated input–output waveforms of the CPLDDFF [10]

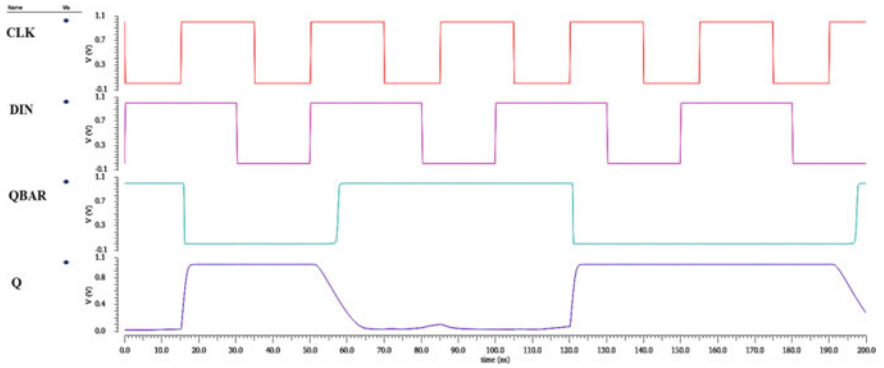

Fig. 15 Simulated input–output waveforms of the proposed CRPLS-DFF

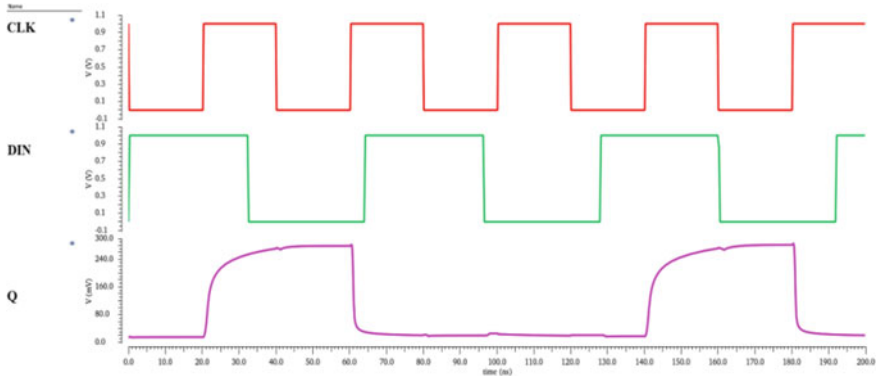

Fig. 16 Simulated input–output waveforms of proposed CRPLD-DFF

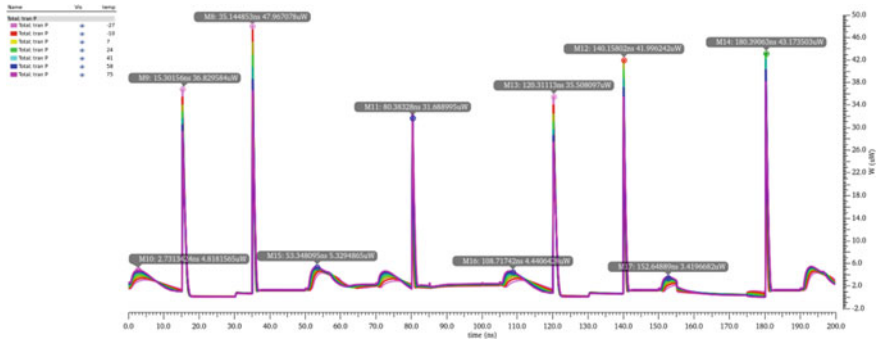

Fig. 17 Transient analysis with temperature variation of CRPLS-DFF

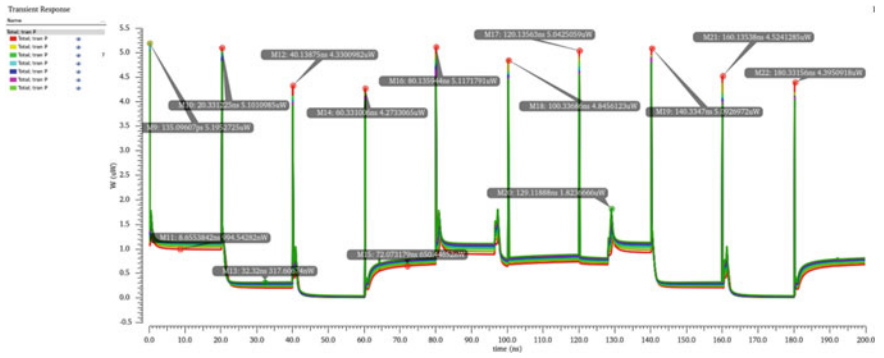

Fig. 18 Transient analysis with temperature variation of CRPLD-DFF

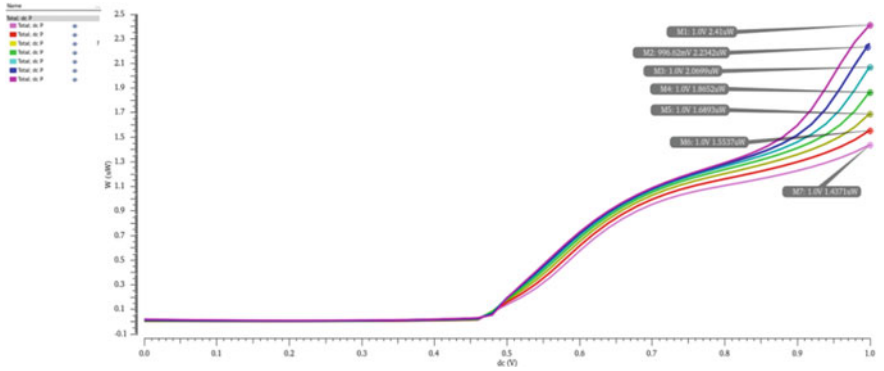

Fig. 19 DC analysis of CRPLS-DFF with temperature variation

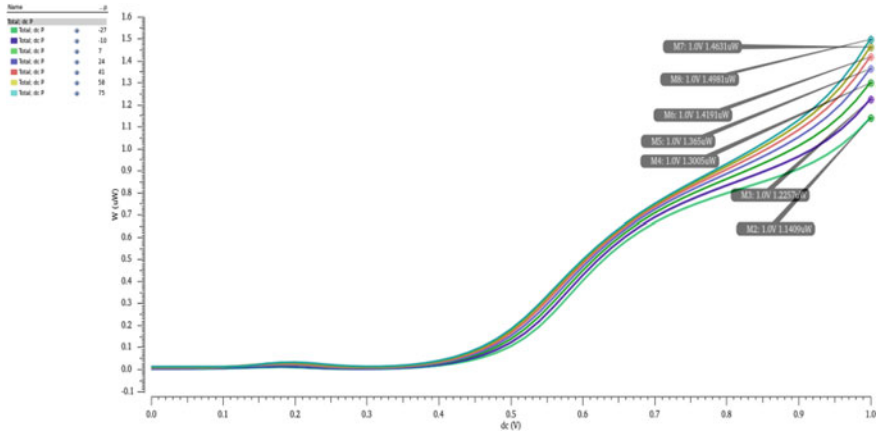

Fig. 20 DC analysis of CRPLD-DFF with temperature variation

Table 1 Comparison of PDP of conventional and proposed flip flop at 45 nm

Flip flop	Static power (μW)	Dynamic power (μW)	Delay (ps)		PDP (J)× 10^{-15}	EDP (J-s) × 10^{-25}
			CLK-Q	D-Q		
POWER PC 603 FF[6]	30.3	45.6	102.3	127.8	8.732	10.046
C^2MOS FF [5]	12.8	21.4	79.9	90.1	2.907	2.471
CPLSDFF[10]	4.33	6.99	98.7	104.8	1.152	1.172
CPLDDFF[10]	2.93	2.01	102.5	112.6	0.531	0.571
Proposed CRPLS-DFF	1.86	4.65	78.5	89.8	0.547	0.461
Proposed CRPLD-DFF	1.48	0.850	91.9	99.4	0.223	0.213

Table 2 Comparison of elements used in conventional and proposed designs

Flip flop	No. of transistors	No. of capacitors
POWER PC 603 FF [6]	22	0
C^2MOS FF [5]	20	0
CPLSDFF [10]	16	0
CPLDDFF [10]	18	0
Proposed CRPLS-DFF	16	0
Proposed CRPLD-DFF	18	2

to output) delay and summarizing improvement in PDP. It can be clearly inferred that proposed flip flops consume less power while maintaining delay in the circuit and hence more efficient than their conventional counterparts. As compared to Power PC 603 FF, there is 93.7% reduction in PDP in static proposed system CRPLS-DFF. In comparison with C^2MOS FF, PDP is reduced to 81.1–92.3% in CRPLS-DFF and CRPLD-DFF correspondingly. For the case of CPLSDFF and CPLDDFF correspondingly, PDP is decreased to 52.7% in comparison with CRPLS-DFF and 58.0% less in CRPLD-DFF. PDP is calculated as product of total power (static and dynamic) and average of delay (CLK-Q and D-Q). EDP is defined as the product of PDP and delay. On comparing EDP of static and dynamic proposed static circuit with reported static and dynamic circuit (CPLSDFF and CPLDDFF) [10], respectively, there is 60.7 and 62.6% reduction in EDP.

Table 2 is listing out the number of elements used in conventional and proposed designs and it can be seen that overall area is less in comparison to static power PC 603 FF and C^2MOS FF. Also the area of proposed design is comparable to reported flip flops CPLSDFF and CPLDDFF. But in case of CRPLD-DFF area is increased due to addition of two capacitors. An extensive simulation performance analysis has been performed on Cadence environment using 45 nm technology to evaluate the reported and proposed Master–Slave Flip Flop topologies. The proposed flip flop CRPLS-DFF and CRPLD-DFF topologies are presented here to achieve low PDP. The performance parameters viz propagation delay, power dissipation, PDP, topologies have been evaluated. Consequently, the proposed topologies are appropriate for the realization of low-power high-performance VLSI design.

The immunity of the circuits to the ambient temperature has also been taken into consideration. The proposed topologies/designs are simulated in temperature range (− 27 to 75 °C) on simulation environment Spectre. Table 3 shows the variation of power dissipation with technology scaled. Power dissipation of the conventional and proposed flip flop topologies for different temperatures at supply voltage VDD = 1 V are listed in Tables 4 and 5, respectively. Moreover, the proposed designed circuits can work at other supply voltages also and are completely robust to voltage variations. It is obvious that the proposed topologies can perform reliably in the temperature range between (− 27 to 75 °C). It means that the proposed designs have an acceptable functionality in a vast temperature range.

Figure 21 presents the graphical comparison of power utilization of proposed work with reported conventional circuits at 45 nm technology within room temperature.

Table 3 Power consumption of implemented flip flops at with different technologies

Flip flop	Static power (μW)	Dynamic power (μW)
CRPLS-DFF(180 nm)	15.6	21.5
CRPLS-DFF(90 nm)	6.67	11.7
CRPLS-DFF(45 nm)	1.86	4.65
CRPLD-DFF(180 nm)	12.34	7.8
CRPLD-DFF(90 nm)	4.62	2.61
CRPLD-DFF(45 nm)	1.48	0.850

Table 4 Dynamic power consumption (μW) of proposed flip flop topologies at different temperatures and various technologies at supply voltage V_{DD} (max) = 1 V

Flip Flop	Temperature (°C)						
	− 27	− 10	7	24	41	58	75
CRPLS-DFF (180 nm)	20.81	20.93	21.4	21.6	21.7	21.8	21.9
CRPLS-DFF (90 nm)	12.65	12.05	12.69	11.65	11.87	12.5	12.7
CRPLS-DFF (45 nm)	3.42	3.21	3.86	3.39	4.91	4.99	5.04
CRPLD-DFF (180 nm)	7.82	7.91	8.91	7.66	7.91	7.94	7.99
CRPLD-DFF (90 nm)	2.84	2.82	2.56	2.66	2.62	2.59	2.62
CRPLD-DFF (45 nm)	0.799	0.834	0.844	0.847	0.861	0.863	0.866

Table 5 Static power consumption (μW) of proposed flip flop topologies at different temperatures and various technologies at supply voltage V_{DD} (max) = 1 V

Flip flop	Temperature (°C)						
	− 27	− 10	7	24	41	58	75
CRPLS-DFF (180 nm)	15.522	15.383	15.252	15.601	15.644	15.654	15.653
CRPLS-DFF (90 nm)	6.661	6.847	6.946	6.671	6.688	6.707	6.724
CRPLS-DFF (45 nm)	1.782	1.835	1.845	1.866	1.873	1.878	1.879
CRPLD-DFF (180 nm)	12.064	12.223	12.224	12.343	12.345	12.347	12.354
CRPLD-DFF (90 nm)	4.524	4.544	4.566	4.623	4.629	4.630	4.632
CRPLD-DFF (45 nm)	1.313	1.343	1.346	1.480	1.475	1.479	1.481

The temperature independency of proposed systems (CRPLS-DFF and CRPLD-DFF) at different technology, considering average dynamic and static power as comparative parameter is depicted in Figs. 22, 23, 24 and 25. As the proposed flip flops give satisfactory performance at 45 nm, layout of the circuits has been designed after DRC check, LVS check and QRC extraction shown in Figs. 26 and 27. Total area occupied by the design has been calculated using the layout. It is observed that CRPLS-DFF which employs 16 transistors occupies an area of 202.4 μm^2, whereas CRPLD-DFF that has 18 transistors occupies an area of 278.7 μm^2.

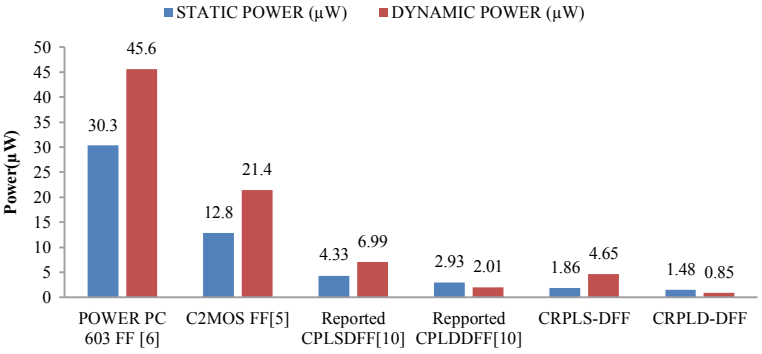

Fig. 21 Comparison of power consumption of proposed flip flop and reported flip flop topologies at 45 nm

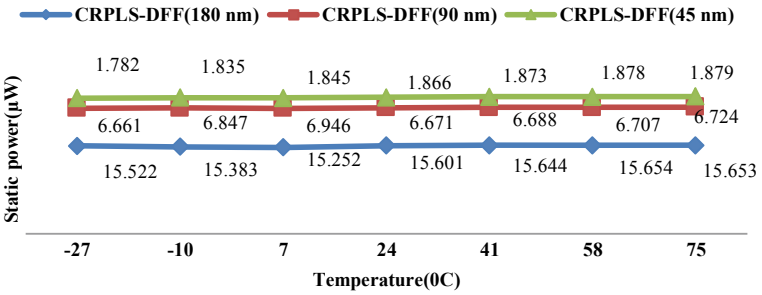

Fig. 22 Comparison of static power consumption of CRPLS-DFF at different temperature ranges with technology scaling

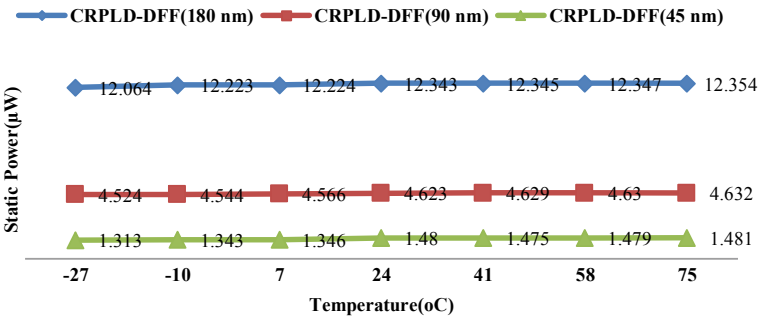

Fig. 23 Comparison of static power consumption of CRPLD-DFF at different temperature ranges with technology scaling

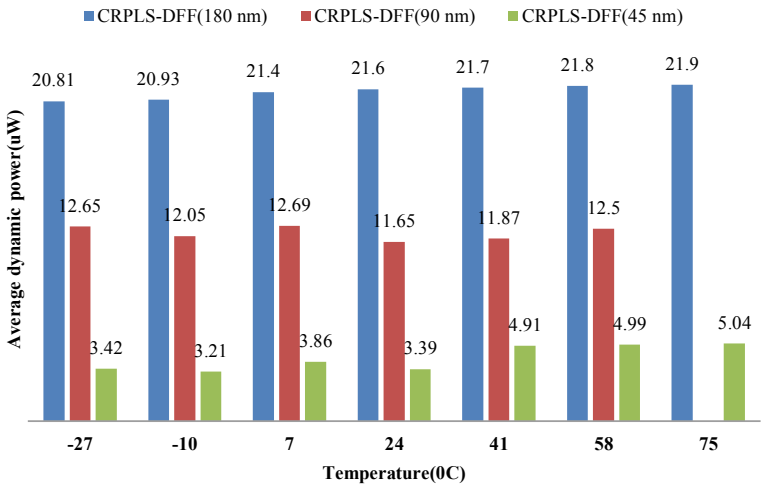

Fig. 24 Comparison of average dynamic power consumption of CRPLS-DFF at different temperature ranges with technology scaling

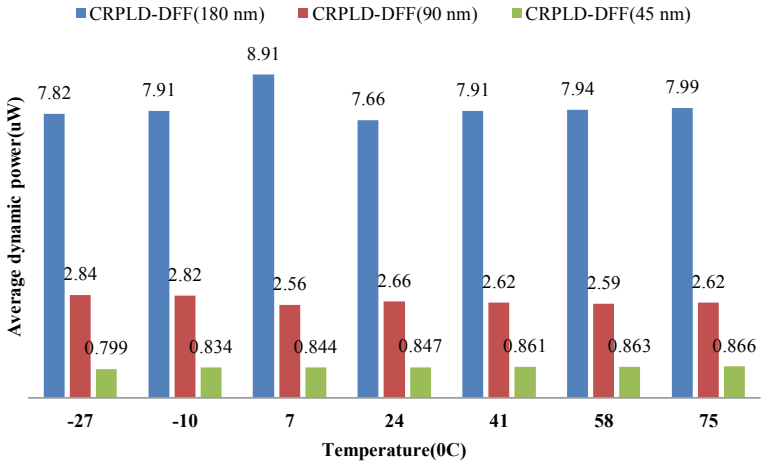

Fig. 25 Comparison of average dynamic power consumption of CRPLD-DFF at different temperature ranges with technology scaling

5 Conclusion

In this paper, the proposed designs are a combination of two logic styles with static and dynamic topologies, offering low power consumption. The proposed energy-efficient Charge retention feedback pass transistors based static (CRPLS-DFF) and dynamic master–slave D flip flop (CRPLD-DFF) topologies have been implemented,

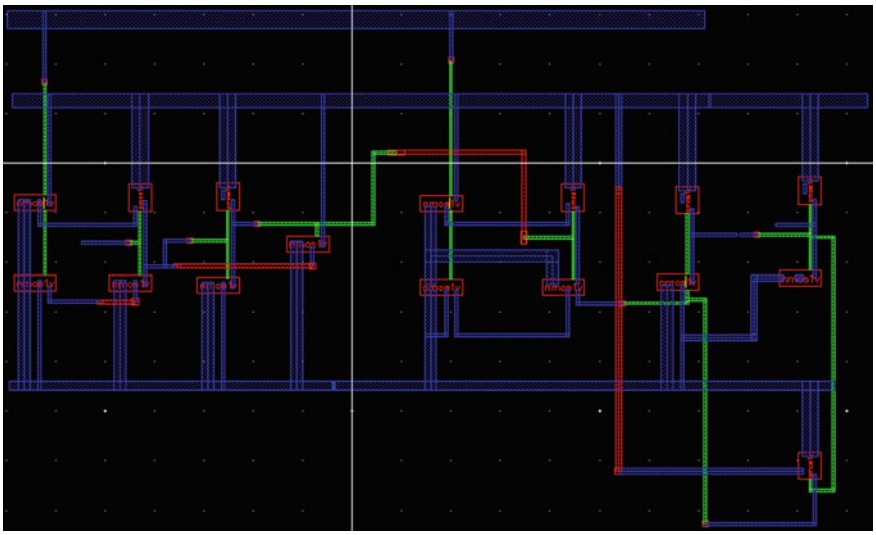

Fig. 26 Simulation layout of CRPLS-DFF at 45 nm

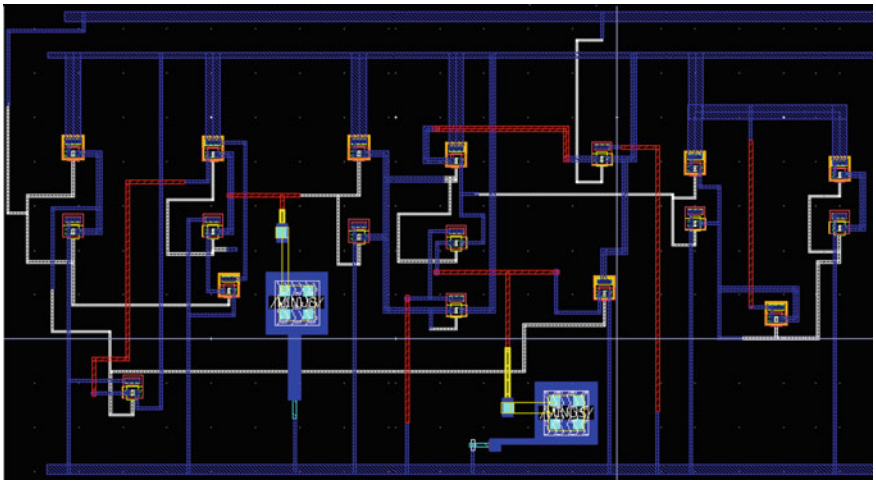

Fig. 27 Simulation layout of CRPLD-DFF at 45 nm

simulated, analyzed and compared with the existing latest flip flop architectures. In this paper, a simple feedback pass transistor-based logic retention flip flop circuits are designed with less transistor counts. The transistors in critical path acquire low threshold value so as to achieve minimum delay. The average transient power dissipation is curtail by eliminating the inessential transistor switching for input data at

diverse clock conditions and also eliminates the issue of charge sharing in the intermediate nodes of the conventional C^2MOS FF circuits. There is excess decline in PDP in CRPLS-DFF and CRPLD-DFF circuit as compared to conventional structures reported in this paper. After scaling down of technology from 180 to 90 nm and then 45 nm, the power dissipation has been minimized to great extent. The total power consumption in the proposed flip flop is showing negligible effect on temperature variations. The layout area has been minimized as number of transistors is less as compared to conventional circuits and is organized at 45 nm technology. Also the layout area is comparable to reported designs but with enhanced power-saving feature. Low value of capacitors are used in order to get reduced layout area without affecting the utility of device. After Quantus Extraction Simulations (QRC), all the pre-resistors and pre-capacitors are calculated and reduced. So proposed design topologies are proficient in terms of area, speed and energy efficiency.

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Subthreshold Gain Enhanced Bulk- and FVF-Driven Self-cascode Current Mirror OTA and Its Applications

Tripurari Sharan and Anil Kumar Gautam

1 Introduction

The shrinking channel length of CMOS devices with downscaling has reduced the thickness of silicon di-oxide which ultimately needs reduced DC power supply for safe operation of CMOS transistors. The extremely high component density dissipates more power which drains battery of low-power gadgets very frequently and need of frequent charging of its battery arises. To mitigate this drawback, the CMOS devices should be biased by using low-voltage supply ($\leq$0.6 V), and it must dissipate ultra-low-power, so that its battery may deliver power for a long time within its charge and discharge cycles [1]. The digital parts of a SoC chip work well under 0.5 V supply in deep submicron era, but the analog parts do not work satisfactorily in this low-supply voltage condition owing to threshold voltage over heads in gate-driven approach. Two-separate DC power supply for digital and analog subcircuits is not advisable, so the circuit designers choose a single low-power supply comparable to device threshold voltage level for biasing the SoC chip. Under this low-voltage condition, the conventional gate-driven input pair-based differential amplifiers fail to operate properly. So, many non-conventional circuit-level design techniques have been proposed by several authors in the past literature [2, 3]. The voltage-to-current converter, i.e., operational transconductance amplifier (OTA), is used in the input core of many analog active cells, such as op-amp, current conveyors, and current feedback amplifiers (CFOAs).

The high-performance linear low-voltage ultra-low-power OTA is required to design many analog building blocks. To fulfill these demands, the circuit designers are using bulk-driven approach-based circuit-level design technique, just after its first proposal and implementation as addressed in [4–6]. Several authors have proposed

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bulk-driven (BD) OTAs and op-amps working below 1 V or even at 0.5 V supply in 180 nm CMOS process which in general requires 1.8 V supply for gate-driven (GD) circuits [6–12]. The BD-MOSFET circuits increase the linearity, offer rail-to-rail input common mode range, and ensure low-voltage design possibility at the cost of reduced bandwidth, unity gain bandwidth (GBW), and increased input referred spectral noise density at its bulk-fed input terminals [2, 3]. The CMOS transistors are kept on by properly biasing its gate terminal and the addition of small-AC signal at their bulk-terminals does not find the threshold voltage in its signal path, so 0.4–0.6 V power supply is just sufficient to drive them rather than 1.8 V required for GD-MOSFET circuits. Further, the use of either pMOS input or nMOS input pair is also dependent on selection of n-tub or p-tub CMOS process. In single-tub standard CMOS process, only pMOS input pairs can be fabricated in isolated n-tub, whereas in p-tub process, nMOS input pair can be fabricated in isolated p-tub. The circuits which require nMOS and pMOS both types of dual-input pairs require costly twin-tub process. The standard n-tub process favors pMOS input pair-based design, so this types of OTAs and op-amps have been reported very often in past literature [2, 8].

The reduction of g_m, bandwidth, and GBW does not matters for small frequency (<500 Hz) bio-signal processing. Several authors have proposed partial positive feedback approach, either in input pair side (negative-resistance-based degeneration) [13] or diode-connected load side (current-starving method) which can be used to improve its transconductance and GBW [7, 13, 14]. The use of flipped-voltage followers (FVFs) in input pair drives it in power efficient class AB mode and favor low-voltage design, so several authors have addressed its use while designing OTAs and op-amps circuits [8, 9]. The single-stage balanced current mirror load type OTAs are proposed and used very often in the literature [14, 15]. But in bulk-driven case, it offers a limited gain of around 25 dB, so to increase its gain self-cascode current mirrors (SC-CMs) can be utilized in the design of symmetric OTA. The SC-CM increases the output impedance investing a single device-drop (V_{DS}) rather than more device voltage ($2V_{DS}$) invested by conventional cascode mirrors. So, the use of SC-CM loads at output node fairly increase the output signal swing [14, 16].

The use of subthreshold (weak-inversion) operation is indeed a good choice for ultra-low-power low-frequency electronic gadgets. The sub-100 nA tail current offers ultra-low-power possibility, so circuits made for bio-signals processing can be operated in weak-inversion region. It is very power efficient and offers maximum transconductance to current efficiency (G_m/I_d) ratio. In this case, the cascode-side device and rail-side device of self-cascode structure must fulfill the ratio of their aspect ratios to be 20:1 to remain in the weak-inversion saturated condition. In this case, cascode device invests a bit increased area [17–21].

In this work, a bulk-driven FVF and pMOS input pair-based balanced self-cascode current mirror load OTA is designed in subthreshold region of operation. It also utilizes load-side partial positive feedback (PPF) or current-starving techniques to enhance its performance.

The remaining portion of this chapter are divided in the following sections. Section 2 presents the block-level and overall circuit schematics and brief description of this OTA. Section 3 presents its various simulation results. Section 4 describes its

use as single input multiple output (SIMO) and multiple input single output (MISO) types of biquadratic filters, three-phase oscillator, and an instrumentation amplifier. Finally, the Sect. 5 concludes this work.

2 Circuit Schematic of Bulk-Driven OTA

Figure 1 presents the block-level structure of this gain enhanced bulk-driven self-cascode balanced current mirror load OTA (BD-SC-CM-OTA) biased in weak inversion. The pMOS input pair P_5, P_6 is source driven by using two FVFs and bulk driven by applying input signal into its bulk-terminals. The anti-phase inputs into FVF and concerned pMOS input transistor are set to add these two-generated drain currents in same phase which increases the bulk-driven transconductance (g_{mb}) by two-times. So, overall transconductance, G_m contributed by input pair side becomes $G_m = 2g_{mb}$ [22, 23]. In the bottom side, the SC pairs (N_{R1}, N_{C1}) and (N_{R2}, N_{C2}) form the PPF current-starving network which further increases the transconductance by $1/(1-K)$ times, where K (0.75) is the ratio of current distribution ($\beta/\alpha < 1$) in between PPF and diode connected nMOS load. In this case, the effective transconductance becomes [24]

$$G_m(\text{effective}) = 2g_{mb}/(1-K) \tag{1}$$

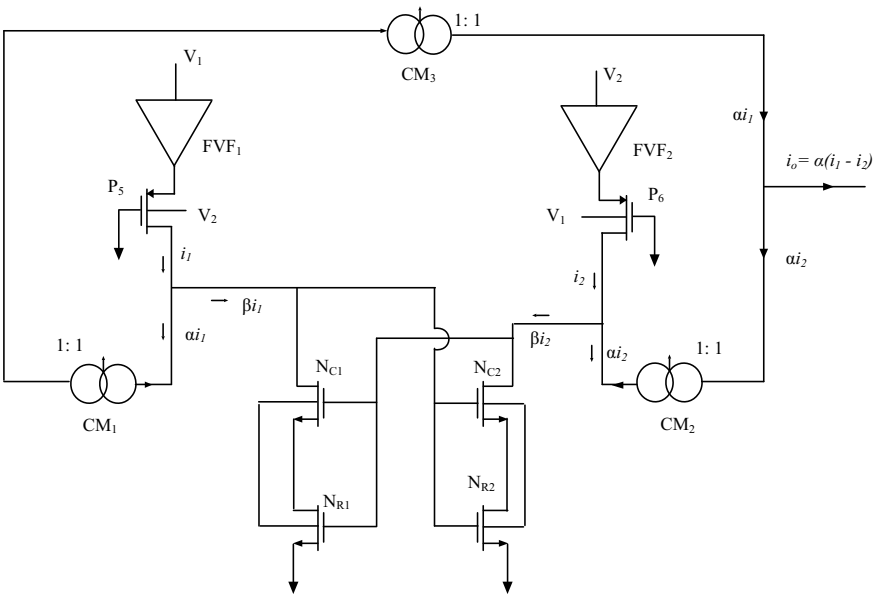

Fig. 1 Block-level diagram of BD-SC-CM-OTA

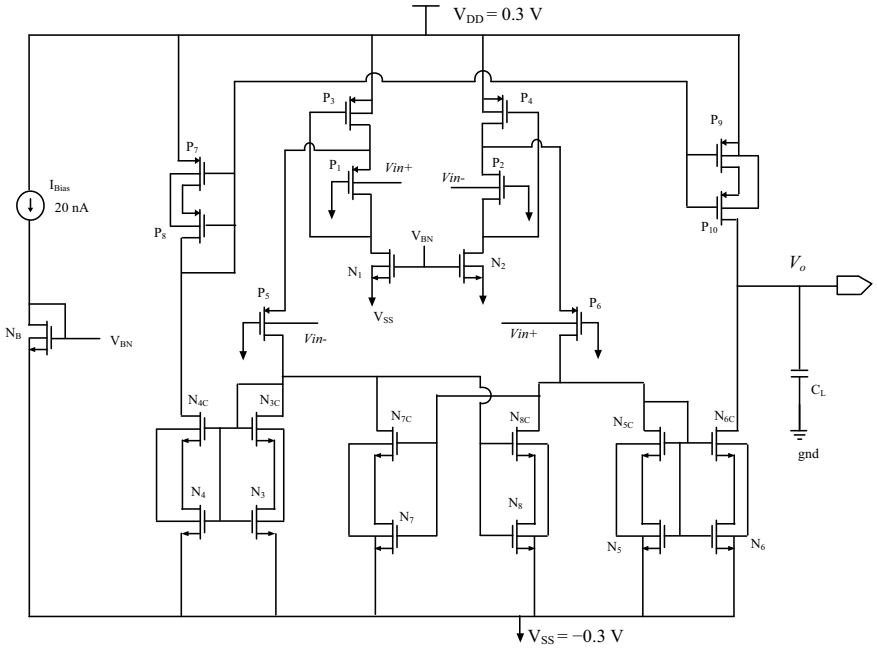

Fig. 2 Circuit schematic of BD-SC-CM-OTA

The three self-cascode current mirrors CM_1, CM_2, and CM_3 each of current mirror ratio (1:1) are used in this balance CM-OTA structure. The SC-CM loads ensured extremely high output resistance at single-ended output node and offered high open loop low-frequency gain of 70.2 dB.

Figure 2 shows overall circuit schematic of this BD-SC-CM-OTA. It is biased in weak-inversion region using dual-power supply of ±0.3 V. The current sources in FVF section are set to 20 nA by using I_{Bias} current source, N_{B}, N_1, and N_2 each of same aspect ratio. The input signal when applied into the bulk-terminals of P_1, P_2 is conveyed to their corresponding source terminal by the FVF action. Further, this voltage is conveyed to source terminals of P_5, P_6. The input signal is also applied into the bulk-terminals of P_5, P_6 with opposite polarity. Thus, P_5 and P_6 are simultaneously bulk and source driven and offer twofolds of transconductance from its nominal low bulk-transconductance value of g_{mb} and ensure nearly rail-to-rail input common mode range. Further, this balanced current mirror OTA utilizes load-side partial positive feedback to enhance its gain and gain bandwidth. It is comprised of self-cascode-based current mirrors which drastically increases its output impedance and overall voltage gain without excess voltage overheads to ensure low-voltage operation. The drain currents of P_5 is fed to two-parallel path, αi_1 parts into SC-current mirror CM_1, and βi_1 parts into PPF SC-composite pair transistors N_7, N_{7C} to ensure current starving which further enhances transconductance by $1/(1 - K)$ times as stated in block-level descriptions. The same is applied for right part of the

input pair [24]. Three-SC-current mirrors comprised of (N_3, N_{C3} and N_4, N_{4C}), (N_5, N_{5C} and N_6, N_{6C}), and (P_7, P_8 and P_9, P_{10}) ensure single-ended output node (V_o) of extremely high output impedance. The load capacitor is of value 15 pF. This circuit is self-load compensated, so additional compensation capacitor for this single-stage balanced-OTA is not required.

3 Simulation Results

The AC, DC sweep, sinusoidal, and pulse transient analysis of this OTA are simulated in n-tub standard CMOS process technology using Tanner EDA tools of version 16.1. All the CMOS transistors are biased in weak-inversion region of operation. Table 1 shows aspect ratios of all the CMOS devices, DC bias current, and load capacitor used during these simulations. The AC sweep analysis is performed using a load capacitor, C_L of 15 pF. The slew rates and GBW are inversely proportional to the load capacitor. If load capacitor is increased, these parameters decrease.

3.1 AC Response in Open Loop Configuration

Figure 3 shows the open loop gain and phase plots under AC analysis setup simulated at 300 K in typical-typical (TT) corner. It has ensured low-frequency open loop gain, GBW, phase margin (PM), and gain margin (GM) of 70.8 dB (at 1 Hz), 8.6 kHz, 76°, and 31 dB, respectively, and dissipates total power of 80 nW.

Figure 4 shows the effect of all process corners, say TT, fast-fast (FF), slow-slow (SS), slow-fast (SF), and fast-slow (FS) on gain, GBW, and phase margin of the OTA.

Table 1 Component size used for BD-SC-CM-OTA

S. No.	Component name	Device size (W/L), (μm/μm), $M = 1$
1	P_1, P_2, P_5, P_6	10/0.6
2	N_B, N_1, N_2	5/1
3	P_3, P_4	20/0.6
4	N_3, N_4, N_5, N_6	2/1
5	N_{3C}, N_{4C}, N_{5C}, N_{6C}	40/1
6	P_7, P_9	6/1
7	P_8, P_{10}	60/1, $M = 2$
8	N_7, N_8	1.6/1
9	N_{7C}, N_{8C}	32/1
10	Load C_L	15 pF
11	I_{Bias}	20 nA

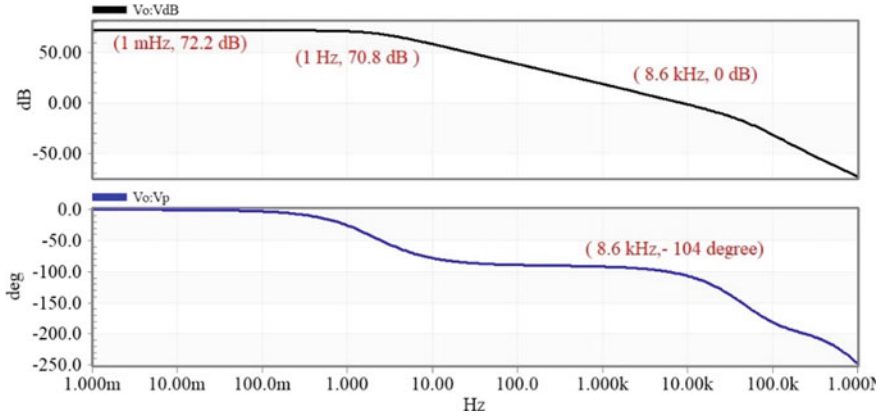

Fig. 3 AC sweep response to yield gain, phase, GBW, PM of this OTA

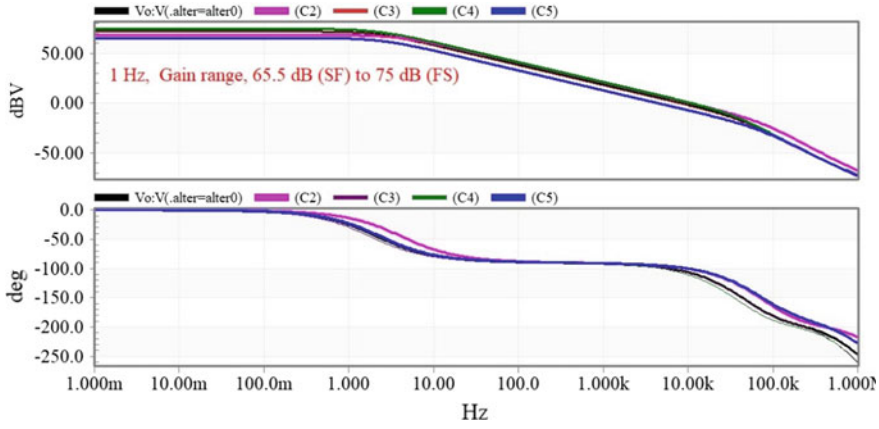

Fig. 4 Effect of device process corners on gain and phase plots under AC sweep circuit setup

This OTA has ensured reduced gain variation lying in the range of 65.5 dB for SF to 75 dB for FS corner. Its GBW varies in the range of 4.3 kHz (SF) to 12 kHz (FS), and phase margin varies in the range of 64° (FS) to 86° (SF). This reasonably high PM range has ensured its stable operation under all process corners.

Figures 5 and 6 show the CMRR plot and positive rail PSRR$_+$ as well as negative rail PSRR$_-$ under AC analysis. It ensured the CMRR, PSRR$_+$, and PSRR$_-$ of 100 dB, 75 dB, and 86 dB, respectively. A high CMRR and PSRRs are desirable to reduce the effect of stray noise produced in SoC chips. It increases the output versus input signal-to-noise ratio of low-amplitude desired signal which is generally buried within stray noise of comparable amplitude.

Figure 7 shows input referred noise (inoise) of the OTA referred at its input bulk-terminals. The bulk-driven OTA contributes $1/\eta^2$, i.e., 9 times inoise than its

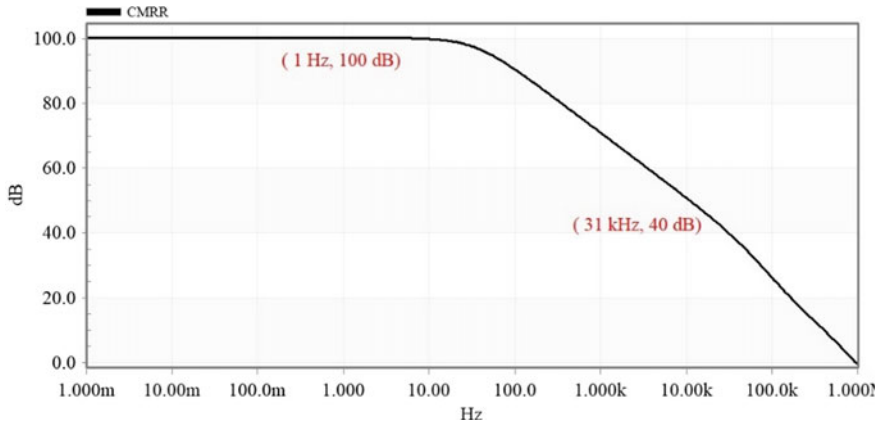

Fig. 5 CMRR of designed BD-SC-CM-OTA under AC analysis

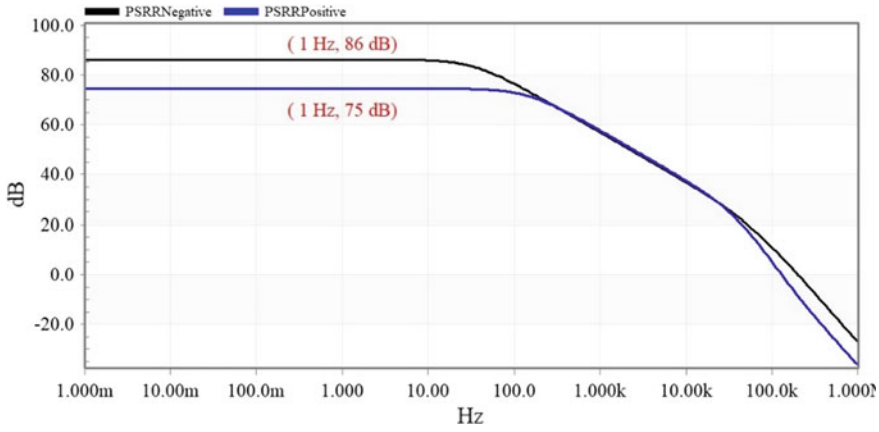

Fig. 6 AC sweep response to yield PSRR+ and PSRR− of the designed BD-OTA

gate-driven counterpart, where η is the bulk to gate transconductance ratio g_{mb}/g_m which is nearly 1/3 in 180 nm CMOS process. The inoise of this OTA is found to be 818 nV/$\sqrt{}$Hz at 1 kHz frequency.

3.2 Simulation Under Unity Gain Configuration of BD-SC-CM-OTA

Figure 8 shows DC sweep response of this differential input and single-ended (SE) output OTA. Its output voltage showed good linearity for input common mode range

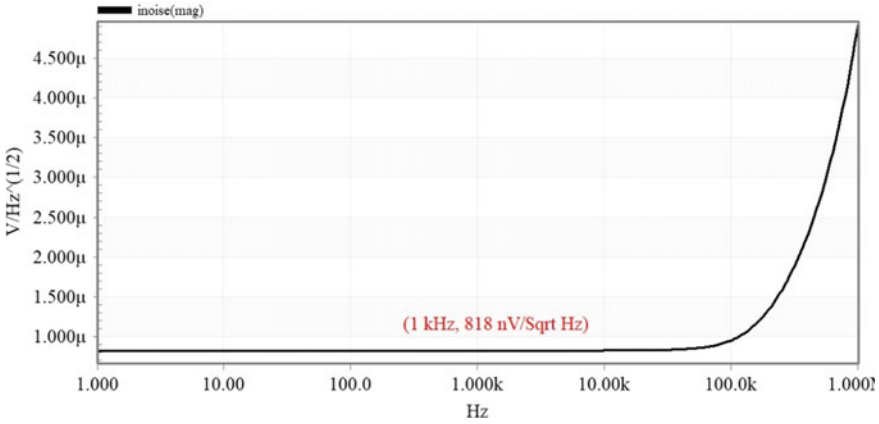

Fig. 7 Input referred contribution of BD-SC-CM-OTA

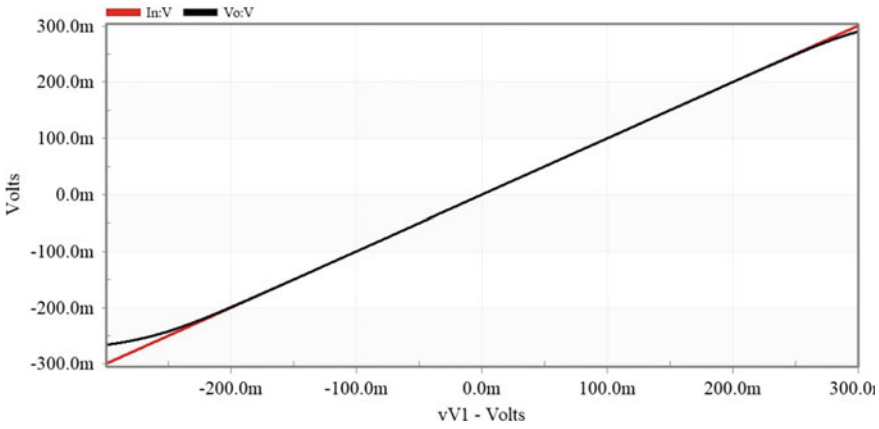

Fig. 8 DC sweep response and input common mode range of this OTA

of ±250 mV. So, transient response with sinusoidal input of ±250 mV peak-to-peak can insure less or acceptable total harmonic distortion (THD).

Figure 9 shows difference in V_{out} and V_{in} voltage levels as the function of DC input sweep. It showed minimum difference of −1.2 mV at 250 mV sweep, whereas its difference is 8 mV at negative-side DC sweep of—250 mV. The output offset error at 0 mV input DC sweep has been found to be 10 µV.

Figure 10 shows pulse transient simulation of OTA in unity gain configuration. A pulse of amplitude 250 mV and frequency 500 Hz ensured positive and negative slew rates of 5.7 and 3.33 V/ms, i.e., average slew-rate of 4.5 V/ms.

Table 2 lists the simulated performances results of this single-ended output OTA.

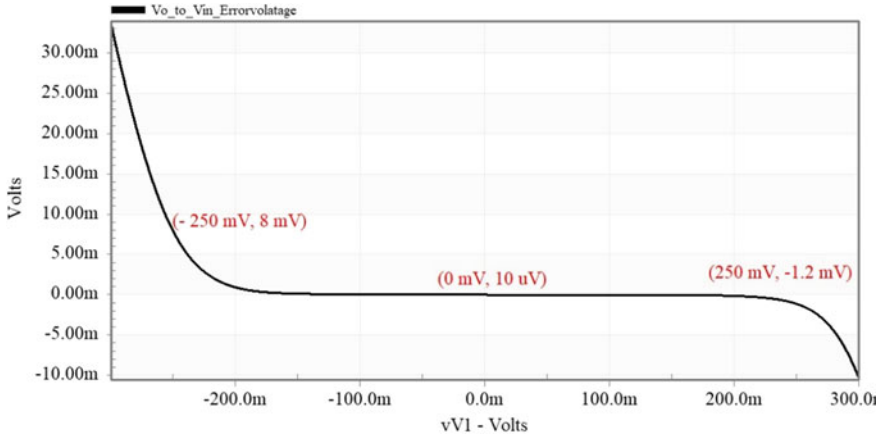

Fig. 9 DC sweep error voltage ($V_o - V_{in}$) voltage of BD-SC-CM-OTA

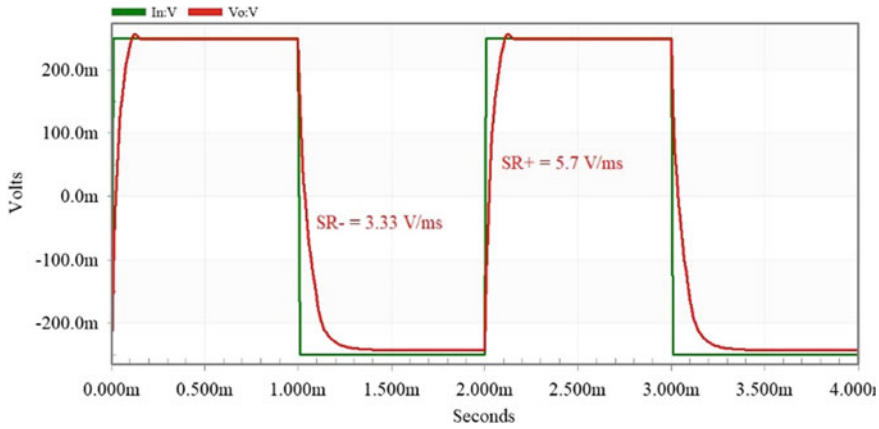

Fig. 10 Pulse transient response-based slew rates and settling behavior of BD-SC-CM-OTA

4 Application of BD-SC-CM-OTA Cells

The transconductance gain of the OTA can be tuned by slightly varying its DC bias current. This unique property of OTA facilitates possibility of off-chip tunability. The OTA can be easily connected as tunable resistor of value $1/G_m$, and this facility ensure its multi-folds usability for the design of various voltage mode and current mode analog subcircuits [25].

Table 2 Simulated performance results of BD-SC-CM-OTA

Performances	Simulation condition	Results
Open loop gain (dB)	Load $C_L = 15$ pF	70.8
GBW (kHz)	do	8.6
PM (degree)	do	76
GM (dB)	do	31
CMRR (dB)	do	100 @ 1 Hz
PSRR+ (dB)	do	75
PSRR− (dB)	do	86
Inoise (nV/Sqrt Hz)	Single-ended node	818 @ 1 Hz
Slew rates (V/ms)	Single-ended unity gain mode	5.7, 3.33
THD (dB)	0.25 V peak, 100 Hz sine wave	−38
Power dissipation (nW)	V_{DD} and $V_{SS} = \pm 0.3$ V, $I_{Bias} = 20$ nA	80

4.1 SIMO Biquadratic Filter

The SIMO biquadratic filters provide all types of responses, say low-pass (LPF), high-pass (HPF), band-pass (BPF), band-reject (BRF), and all-pass (APF), simultaneously available at its different nodes. The second-order biquadratic filters are very frequently used in various analog signal processing applications, such as antialiasing low-pass and band-pass filters, and wide and narrow-band notch filters. Table 3 shows transfer functions of all five-generic second-order standard prototype filters [26].

Figure 11 presents the circuit schematic of a SIMO biquadratic filter using four OTA cells and two-grounded capacitors C_1 and C_2 adopted from [26]. The g_{m3} and g_{m4} cells functions as integrators, whereas g_{m1} works as adders with different feedback paths and g_{m2} presents a resistor of value $1/g_{m2}$ in between V_{HP} and V_{BP} nodes (see Fig. 11). This filter provides high-pass, band-pass, and low-pass filter functions at V_{HP} and V_{BP}, and V_{LP} nodes, respectively. The routine nodal analysis generates three main transfer functions as given by (2–4)

Table 3 Transfer functions of all generic second-order standard prototype filters

Filter type	Transfer function	Pass-band gain
Low-pass (LPF)	$T(s) = A_0/\left[s^2 + s(\omega_0/Q) + \omega_0^2\right]$	$A_0/{\omega_0}^2$
Band-pass (BPF)	$T(s) = A_1 s/\left[s^2 + s(\omega_0/Q) + \omega_0^2\right]$	$A_1 Q/{\omega_0}^2$
High-pass (HPF)	$T(s) = A_2 s^2/\left[s^2 + s(\omega_0/Q) + \omega_0^2\right]$	A_2
Band-reject (BRF)	$T(s) = A_2\left(s^2 + \omega_0^2\right)/\left[s^2 + s(\omega_0/Q) + \omega_0^2\right]$	A_2
All-pass (APF)	$T(s) = A_2\left(s^2 - s\omega_0/Q + \omega_0^2\right)/\left[s^2 + s(\omega_0/Q) + \omega_0^2\right]$	A_2

where ω_0 and Q are the pole frequency and quality factor

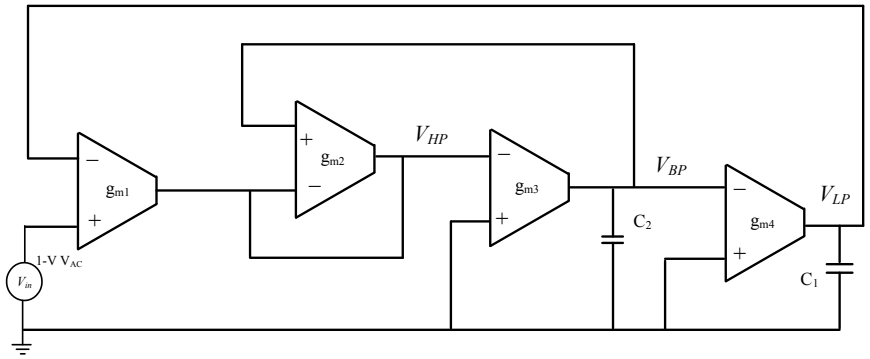

Fig. 11 Circuit schematic of SIMO biquadratic filter using 4-OTA cells and 2-grounded capacitors [26]

$$\frac{V_{\mathrm{HP}}}{V_{\mathrm{in}}} = \frac{g_{\mathrm{m1}}s^2/g_{\mathrm{m2}}}{s^2 + g_{\mathrm{m3}}s/C_1 + g_{\mathrm{m1}}g_{\mathrm{m3}}g_{\mathrm{m4}}/g_{\mathrm{m2}}C_1C_2} \tag{2}$$

$$\frac{V_{\mathrm{BP}}}{V_{\mathrm{in}}} = \frac{-g_{\mathrm{m1}}g_{\mathrm{m3}}s/g_{\mathrm{m2}}C_2}{s^2 + g_{\mathrm{m3}}s/C_1 + g_{\mathrm{m1}}g_{\mathrm{m3}}g_{\mathrm{m4}}/g_{\mathrm{m2}}C_1C_2} \tag{3}$$

$$\frac{V_{\mathrm{BP}}}{V_{\mathrm{in}}} = \frac{g_{\mathrm{m1}}g_{\mathrm{m3}}g_{\mathrm{m4}}/g_{\mathrm{m2}}C_1C_2}{s^2 + g_{\mathrm{m3}}s/C_1 + g_{\mathrm{m1}}g_{\mathrm{m3}}g_{\mathrm{m4}}/g_{\mathrm{m2}}C_1C_2} \tag{4}$$

From these equations, the attenuation factor $\alpha = \omega_{\mathrm{o}}/Q = g_{\mathrm{m3}}/C_1$ and square of angular frequency, $\omega_{\mathrm{o}}^2 = g_{\mathrm{m1}}g_{\mathrm{m3}}g_{\mathrm{m4}}/g_{\mathrm{m2}}C_1C_2$ the central angular frequency and quality factor Q of band and band-reject responses are given by Eqs. (5) and (6).

$$\omega_{\mathrm{o}} = (g_{\mathrm{m1}}g_{\mathrm{m3}}g_{\mathrm{m4}}/g_{\mathrm{m2}}C_1C_2)^{1/2} \tag{5}$$

$$Q = (g_{\mathrm{m1}}g_{\mathrm{m4}}C_1/g_{\mathrm{m2}}g_{\mathrm{m3}}C_2)^{1/2} \tag{6}$$

For all the equal components design, $\omega_{\mathrm{o}} = g_{\mathrm{m}}/C$ and $Q = 1$. The AC response of this SIMO filter has been simulated with $C_1 = C_2 = C = 1$ nF, and its response is shown in Fig. 12. This filter has yielded the central and angular frequencies of 138 Hz, i.e., 867 rad/s which ascertain the equivalent transconductance of 867 nS from (5). Increasing or decreasing the filter's capacitance, C by 10 folds, the central frequency also decreases or increases by 10 folds. Thus, its central frequency linearly tracks the chance in filter's capacitance C. The quality factor Q from (6) can be increased by setting the ratio C_1/C_2. This filter has dissipated low power of 320 nW.

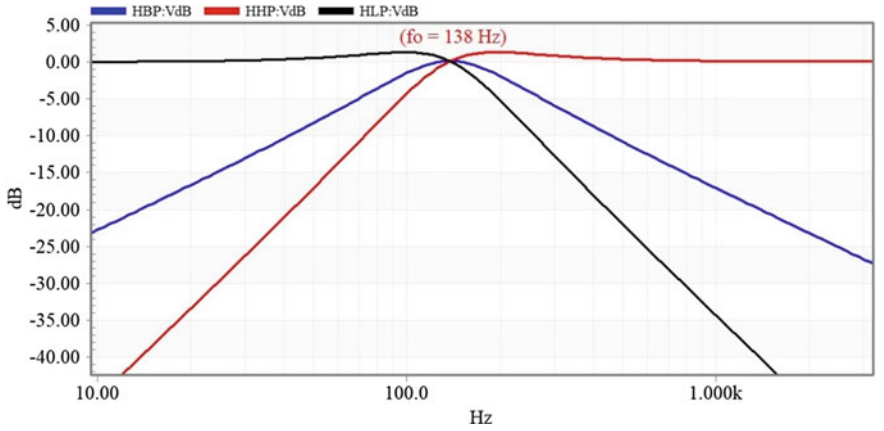

Fig. 12 Simulated response of SIMO biquadratic filter

4.2 Multiple Input Single Output Biquadratic Filter

Figure 13 shows a MISO type biquadratic filter which uses five numbers of g_m cells and two capacitors adopted from [26]. The one capacitor C_2 is grounded, whereas the grounding condition of C_1 depends on the type of filter response. It has three input nodes E_1, E_2, E_3 and a single output node V_o.

The routine nodal analysis of the circuit sets its s-domain transfer function given by (7)

$$V_o(s) = \frac{N(s)}{D(s)} = \frac{E_3 s^2 + E_2 g_{m4} s/C_2 + E_1 g_{m2} g_{m5}/C_1 C_2}{s^2 + g_{m3} s/C_2 + g_{m2} g_{m1}/C_1 C_2} \tag{7}$$

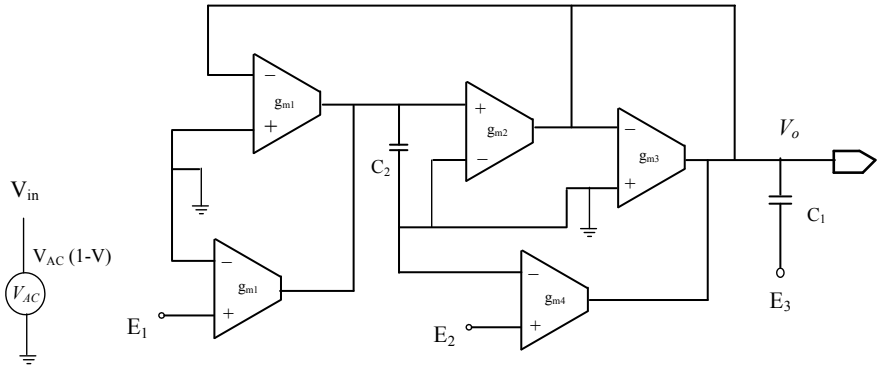

Fig. 13 MISO biquadratic filter using five OTAs and two capacitors [26]

Table 4 Setup to obtain HP, BP, LP, band-reject (BR) responses, ω_o and Q factor

Filter type	Transfer function	Simulation setup
HP	$V_o(s)/E_3(s) = s^2/D(s)$	$E_3 = V_{in}$, $E_1 = E_2 = 0$
BP	$V_o(s)/E_2(s) = g_{m4}s/D(s)$	$E_2 = V_{in}$, $E_1 = E_3 = 0$
LP	$V_o(s)/E_1(s) = (g_{m2}g_{m5}/C_1C_2)/D(s)$	$E_1 = V_{in}$, $E_2 = E_3 = 0$
BR	$V_o(s)/E_1(s) = \left[s^2 + (g_{m2}g_{m5}/C_1C_2)\right]/D(s)$	$E_1 = E_3 = V_{in}$, $E_2 = 0$
ω_o	$g_m/\sqrt{(C_1C_2)}$	For all g_m of equal values
Q	$\sqrt{C_2}/\sqrt{C_1}$	$Q = 1$ for $C_1 = C_2$

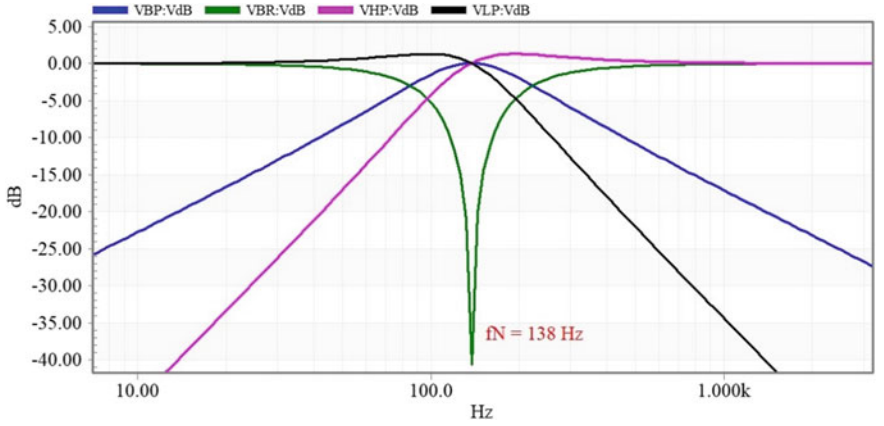

Fig. 14 Simulated AC response of MISO biquadratic filter

The LPF, HPF, and BPF responses can be obtained from (7) by applying input signal to any one terminal and grounding remaining two-terminals as listed in Table 4. The band-reject response can be obtained by applying input signal to E_1 and E_3 nodes and grounding the node E_2 in condition of $g_{m1} = g_{m5}$.

In case of equal transconductors and $C_1 = C_2 = C = 1$ nF, all four prototypes filter's responses are simulated in their own individual circuit setup, and their combined frequency response is shown in Fig. 14. The central and notch frequencies are 138 Hz, i.e., its angular frequency $\omega_0 = 867$ Hz. Since angular radian frequency, $\omega_o = g_m/C$, so simulated value of transconductance g_m comes out to be 867 nS. This filter dissipates the total power of 400 nW.

4.3 Low-Frequency Three-Phase Oscillators

Three-phase oscillator are required in many communication circuits and in bio-signal instrumentation testing and design. The 50–60 Hz three-phase power supply with

phase difference of 120° with each other states its example. Figure 15 shows three OTA and three shunt-connected RC network-based three-phase oscillator. To produce low-frequency oscillation, high value of R is desired. However, active OTA-based resistors each of value $(1/g_m)$ can replace these passive resistors (R) to realize a compact circuit. The transfer function between each of two adjacent nodes is given as $V_2/V_1 = V_3/V_2 = V_1/V_3 = g_m R/(RCs+1)$. This three-stage mutually coupled circuit oscillates in the condition of $R = 2/g_m$ and resonating angular frequency $\sqrt{3}/RC$. The three generated signals V_1, V_2, and V_3 differ by 120° w.r.t. each other. The three resistors each of value $2/g_m$ is realized by using OTA cell of transconductance $g_m/2$. To realize such half-value transconductor, its bias current is reduced from 20 nA (OTA cell) to 10 nA ($1/R$ cell) adopted from [25].

Figure 16 shows the simulated wave forms of three 120° phase-shifted outputs. Its peak-to-peak levels swings between positive and negative saturation limits, i.e.,

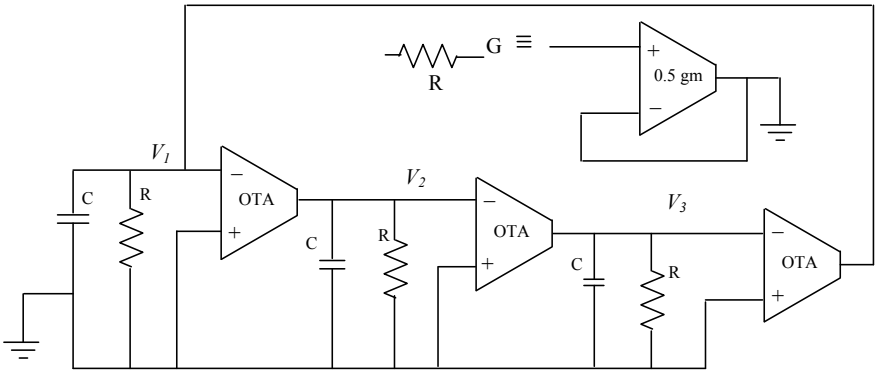

Fig. 15 Low-frequency three-phase oscillators using three OTAs and three RC networks [25]

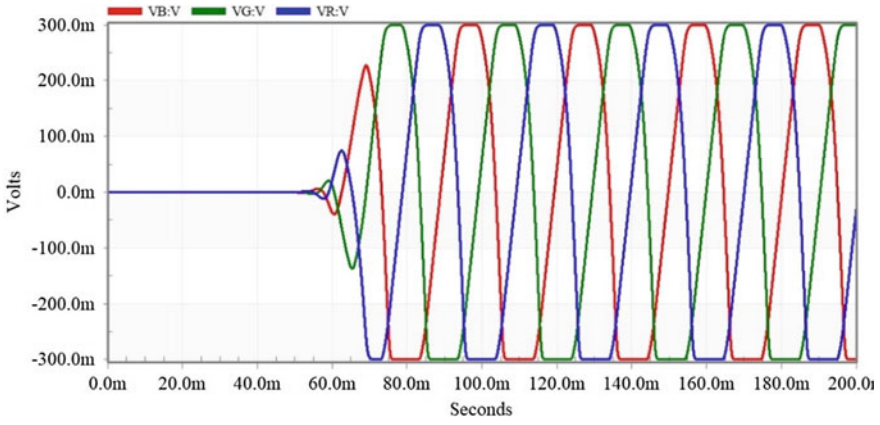

Fig. 16 Low-frequency three-phase oscillatory voltage wave forms of time-period 33.33 ms

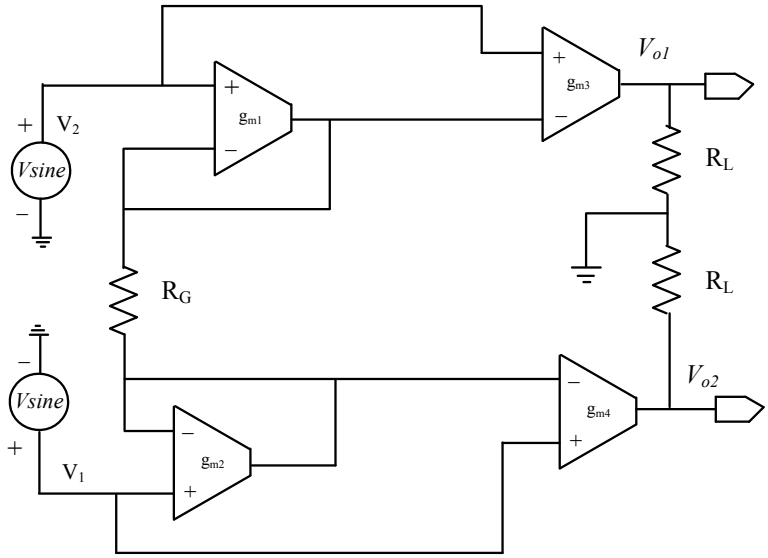

Fig. 17 Four OTA based instrumentation amplifier using gain adjusting resistor R_G and loads R_L [25]

$\pm V_{sat}$ which is ± 300 mV and output signal time-period and frequencies are 33.33 ms and 30 Hz for equal capacitors of value 10 nF.

4.4 OTA Based Instrumentation Amplifier

The weak-inversion biased OTA can be employed to design variable gain instrumentation amplifier to amplify very weak signal of low-frequency related to bio-medical processing. Figure 17 shows 4 OTAs based instrumentation amplifier using gain adjusting resistor R_G and two loads R_L adopted from [25]. The input differential signals, say V_1 and V_2, are applied into the non-inverting terminals of transconductance cells g_{m1} and g_{m2}. So, these input signals experience extremely high input impedances, and their signal sources are not loaded. The first output V_{o1} available at output node of g_{m3} in case of $g_{m1}R_G \gg 1$ can be derived using routine nodal analysis as given in (8).

$$V_{o1} = \frac{g_{m_3} R_L (V_2 - V_1)}{g_{m_1} R_G} \tag{8}$$

Similarly, the second output V_{o2} available at output node of g_{m4} for the case of $g_{m1}R_G \gg 1$ can be derived using routine nodal analysis as given in (9).

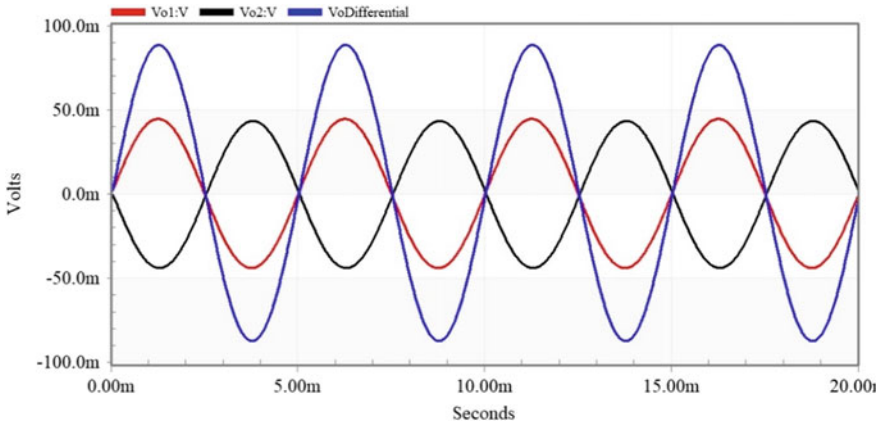

Fig. 18 Transient response of IA with differential input of 10 mV and gain of 5 at 200 Hz frequency

$$V_{o1} = \frac{g_{m_4} R_L (V_1 - V_2)}{g_{m2} R_G} \tag{9}$$

Thus, two-appositive polarity signals are available at outputs of g_{m3} and g_{m4} cells. For equal transconductors, the output voltages depend upon the ratio of R_L and R_G. This IA has been applied with two independent sinusoidal input sources V_2 and V_1 of amplitude 10 and 5 mV having equal frequency of 200 Hz. To ensure $g_m R_G \gg 1$, the R_G is taken as 20 MΩ and $R_L = 200$ MΩ which sets a gain of 10 from (8, 9). So, for the differential input of 5 mV amplitude, outputs V_1 and V_2 each of amplitude 50 mV are desired. The simulated single-ended and fully differential outputs are shown in Fig. 18.

The transient sinusoidal simulation has ensured nearly 44 mV amplitude for V_1, V_2, and fully differential output is of amplitude 88 mV. For a required value of R_G as per the criteria ($g_{m1} R_G \gg 1$), the gain of IA can be increased by increasing load R_L.

5 Conclusions

This paper has presented the design aspects of a gain enhanced bulk-driven balanced self-cascode load single-ended output OTA biased in weak-inversion region for its ultra-low-power consumption. It has offered open loop gain, GBW, and phase margin of 70.8 dB, 8.6 kHz, and 76°, respectively, with load capacitor of 15 pF. This OTA has been utilized to design a SIMO and MISO types biquadratic filters, three-phase oscillator, and an OTA-based instrumentation amplifier suitable for bio-medical signal processing.

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Low-Power MISO Biquadratic Filter and Diode-Less Full Wave Rectifier Using CM-BD-MO-OTA for Bio-signals

Tripurari Sharan and Akho John Richa

1 Introduction

The continuous shrink in size of CMOS technology has reduced the DC bias voltage, silicon dioxide thickness and intrinsic gain of CMOS devices which necessitates the design of low-voltage ultra-low-power circuits for safe operation without thermal break down of the mixed SoC chip. For such low-voltage devices near rail-to-rail input, common mode range and maximized output signal swing become essential requirement [1].

Most of the SoC chips have both analog and digital parts embedded within it. The digital circuits function satisfactorily at voltage level below 0.6 V but same is not true for the analog circuit parts. This happens because of the threshold voltage overhead conditions in case of gate-driven MOS transistors; to mitigate this problem, bulk-driven MOS transistors (BD-MOST) techniques are preferred in place of gate-driven method. BD-MOST has the advantage that the small-signal voltage applied to the bulk of the transistor does not encounter the threshold voltage of MOSFETs in its signal path, so a low voltage of 0.6 V or even below it can be used as power supply for various analog circuits designed using bulk-driven MOSFET [2–12].

With the emerging market of small portable devices such as sensors, biomedical implants, testing and design of biomedical instruments the low-power analog circuit design has become essential for these battery-powered devices to run for a longer period of time on a single charge [13, 14]. In conditions where very low-power budget is available, the subthreshold (or weak inversion) operation of MOSFET is preferred over strong inversion operation. The weak inversion and bulk-driven topology is a suitable choice to process low-frequency signals with ultra-low-power budget [15, 16].

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Operational transconductance amplifier is an important building block for analog circuit design, and it is widely employed as the input core of various analog active blocks, such as op-amp, current conveyors and current feedback amplifiers (CFOAs). For biomedical signal processing, a number of bulk-driven OTA structures operating in subthreshold region have been proposed [2–20], where main challenge is to achieve considerable open-loop gain with the modest unity gain bandwidth (GBW) and slew rate (SR) as bio-signals are generally of weak amplitude confined within the frequency range of 0.1 Hz to 1 kHz [21].

In the bio-signal processing chain, the low-noise analog instrumentation amplifiers to amplify and full wave rectifier for wave shaping are required [22–24]. The half wave and full wave rectifiers are required in analog signal-processing applications such as instrumentations, measurement, control systems [25], sensor interfaces and power converters [26]. Biomedical signal processing is also an emerging field where low-voltage low-power full wave rectifiers are used [27].

The passive diode rectifiers are not suitable for processing extremely low-voltage signals, mainly because of the diode's cut-in voltage limitations (which is 0.7 V/0.3 V for Si/Ge-diodes), which can be mitigated by using high-gain active amplifiers in feedback loop to assist rectification operation at low-voltage levels [25, 28]. These circuits also need some diodes with op-amps, positive second-generation current conveyor (CCII+) cells, current feedback operational amplifier (CFOA) cells, etc. Some authors have reported diode-less rectifiers based on active devices such as operational amplifiers (OAs), OTAs, CCII and current-controlled current conveyors (CCCII) [29] in the past literature [25, 27, 30].

This chapter presents the low-power diode-less full wave rectifiers [28] and multiple input single output (MISO)-type biquadratic filter using bulk-driven current mirror load multi-output OTA (BD-CM-MO-OTA) [31–33]. Figures 1 and 2 show the symbol and full circuit structure of fully differential multiple-output OTA used to design the full wave rectifier and MISO filter. It has a bulk-driven differential input

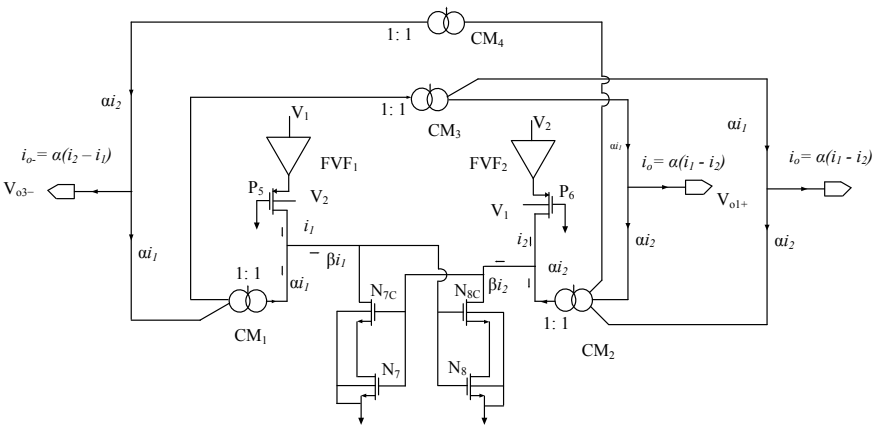

Fig. 1 Block-level circuit of BD-SC-CM-OTA

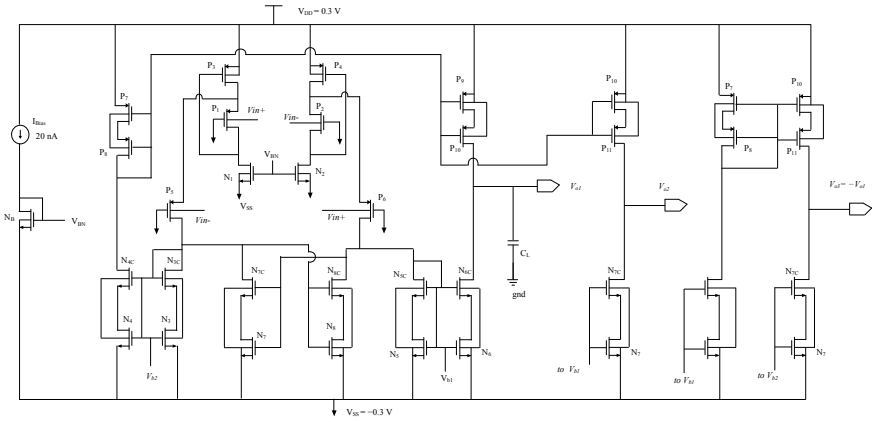

Fig. 2 Circuit schematic of BD-SC-CM-MO-OTA

with three output, namely V_{o1} first positive output, V_{o2} second positive output and V_{o3-} being the negative polarity output.

The rest of this chapter is organized in following sections. The circuit description of proposed BD-CM-MO-OTA and its simulation results are presented in Sects. 2 and 3. Section 4 presents its applications as LV-LP diode-less full wave rectifiers and MISO biquadratic filter. The conclusions are drawn in Sect. 5.

2 Circuit Schematic of Current Mirror Bulk-Driven MO-OTA

Figure 1 presents the block-level structure of this gain-enhanced bulk-driven self-cascode balanced-current mirror load multiple output OTA (BD-SC-CM-MO-OTA) biased in weak inversion. The pMOS input pair P_5, P_6 is source-driven by using two-FVFs and bulk-driven by applying input signal into its bulk-terminals [34]. The anti-phase inputs into FVF and concerned pMOS input transistor are set to add these two generated drain currents in same phase which increases the overall bulk-driven transconductance (g_{mb}) by two times [35]. So, overall transconductance contributed by input pair side becomes $2g_{mb}$. The bottom side the self cascode (SC) pairs (N_7, N_{7C}) and (N_8, N_{8C}) form the partial positive feedback (PPF) current starving network which further increases the transconductance by $1/(1-K)$ times [34], where K (set to 0.75) is the ratio of current distribution ($\beta/\alpha < 1$) in between PPF and diode-connected nMOS load. In this case, the effective transconductance gets, further, enhanced as shown in (1).

$$G_m(\text{effective}) = 2g_{mb}/(1-K) \tag{1}$$

The three self-cascode current mirrors CM_1, CM_2 and CM_3 each of current mirror ratio (1:1) ensure single-ended output node of extremely high output resistance to offer open-loop low-frequency gain of 72 dB. Similarly, multiple outputs nodes are generated by using different CMs to obtain duplicated positive node V_{o2} and one more negative output node V_{o3-}.

Figure 2 shows overall circuit schematic of this BD-SC-CM-MO-OTA. It has been biased using dual-power supply of ±0.3 V in weak inversion of operation, and current sources in flipped voltage follower (FVF) section are set to 20 nA by using I_{Bias} current source, matched N_B, N_1 and N_2 pMOS transistors, each of same aspect ratio. The input signal when applied into the bulk terminals of P_1 and P_2 is conveyed to their corresponding source terminal by the FVF action. Further, this voltage is conveyed to source terminals of P_5 and P_6. The input signal is also applied into the bulk terminals of P_5 and P_6 with opposite polarity. Thus, P_5 and P_6 are simultaneously bulk and source-driven and offer twofold of transconductance. The drain currents of P_5 is fed to two parallel path, αi_1 parts into SC-current mirror CM_1 and βi_1 parts into PPF SC-composite pair transistors N_7 and N_{7C} to ensure current starving which, further, enhances transconductance by $1/(1-K)$, i.e., four times as stated in block-level descriptions [19, 36, 37]. The same is applied for right part of the input pair. Three SC-current mirrors comprised of (N_3, N_{C3} and N_4, N_{4C}), (N_5, N_{5C} and N_6, N_{6C}) and (P_7, P_8 and P_9, P_{10}) ensure single-ended output node (V_o) of extremely high output impedance. The load capacitor used is 15 pF. This circuit is self-load compensated, so additional compensation capacitor for this single-stage balanced OTA is not required. Furthermore, this circuit in fully differential mode is comprised of six-branches structure, and its DC level at output nodes are pre-defined, so the common mode feedback circuit is not essential requirement, and it is not used [24, 38].

The output impedance (r_o) and low-frequency voltage gain (A_v) are given by (2)

$$r_o = \left(g_{mP_{10}} r_{oP_{10}} r_{oP_9} \| g_{mN6C} r_{oN6C} r_{oN6}\right) \text{ and } A_v = g_{mp_1} r_o \tag{2}$$

where g_{mi} and r_{oi} present the transconductance gain and output resistance of the concerned CMOS devices [22–24]. The simple bulk-driven OTA contributes the open-loop voltage gain of 24 dB only. The FVF-based input core has increased its gain by 6 dB and PPF network by four times which has contributed a gain rise of 12 dB over bulk-driven simple structure. Further, the self-cascode load has increased its gain by 34 dB, so, overall open-loop gain for single-ended output node is about 72 dB. So, it has offered fully differential open-loop voltage gain of 78 dB.

3 Simulation Results

To validate the applicability of SC-CM-BD-MO-OTA, its own performances and three applications, i.e., full wave rectifiers, MISO filter and instrumentation amplifier (IA) are designed and simulated in standard 180 nm CMOS process using Tanner

Table 1 Component size used for BD-SC-CM-MO-OTA

S. No.	Component name	Device size (W/L), (μm/μm), $M = 1$
1	P_1, P_2, P_5, P_6	10/0.6
2	N_B, N_1, N_2	5/1
3	P_3, P_4	20/0.6
4	N_3, N_4, N_5, N_6	2/1
5	$N_{3C}, N_{4C}, N_{5C}, N_{6C}$	40/1
6	P_7, P_9	6/1
7	P_8, P_{10}	60/1, $M = 2$
8	N_7, N_8	1.6/1
9	N_{7C}, N_{8C}	32/1
10	M_n, M_p	40/0.5 and 80/0.5
11	Load C_L	15 pF
12	R_L	1.2 MΩ
13	I_{Bias}	20 nA

EDA simulation tool. This OTA is biased using dual-power supply of $\pm$0.3 V at 20 nA bias current. All the MOSFETs are biased to operate in subthreshold region. The drain/source currents of CMOS transistors are exponential function of input voltage, like to the BJT, and their transconductance gain $\left(G_m = I_{DS}/nU_T\right)$ is proportional to their DC operating-point bias current, where n is the subthreshold slope factor (n_p for pMOS and n_n for nMOS transistors) and U_T is the thermal voltage (25.6 mV at 300 K) which shows very weak dependency on temperature [12]. Table 1 lists the size of the devices used in these implementations.

3.1 Simulations in Open-Loop Configuration

The AC analysis for open-loop gain and phase response of this OTA is shown in Fig. 3; the open-loop fully differential (FD) gain, GBW, phase margin (PM) and gain margin (GM) as obtained from simulations are 78 dB (at 1 Hz), 13.5 kHz, 63° and 31 dB, respectively, while consuming total power of 104 nW.

Figure 4 shows the effect of device corner variations (TT, FF, SS, FS, SF) on fully differential gain and phase response of this SC-CM-BD-MO-OTA, where the open-loop FD gain is found to be varying in range of 70–81 dB for different device corners.

Figures 5 and 6 show the single-ended (SE) output version of CMRR plot and positive rail PSRR as well as negative rail PSRR under AC analysis. It ensured the CMRR, PSRR+ and negative-line PSRR of 100 dB, 75 dB and 86 dB, respectively. A high CMRR and PSRRs are desirable to reduce the effect of stray noise produced

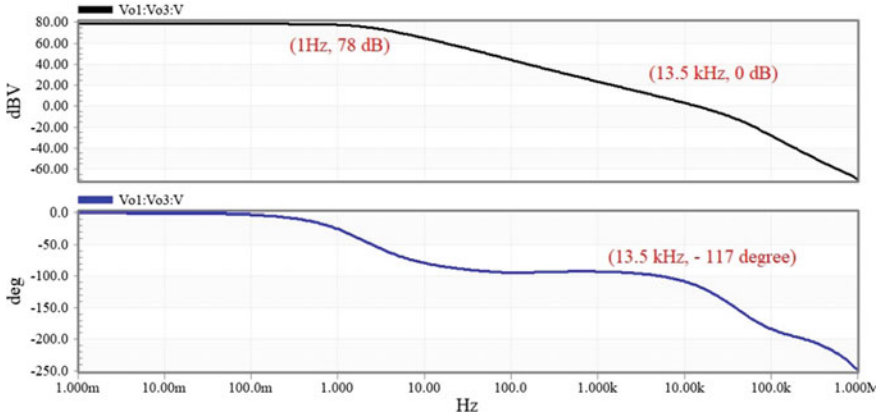

Fig. 3 AC sweep response to yield FD gain, phase, GBW and PM and GM of BD-OTA

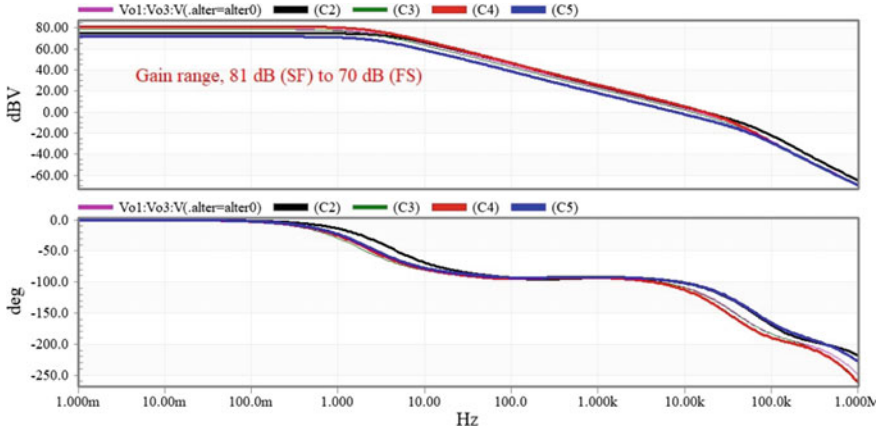

Fig. 4 Effect of device process corner on FD gain and phase plots under AC sweep response setup

in SoC chips [21]. It increases the SNR of desired signal of low amplitude buried within stray noise of comparable amplitude [24].

The input-referred noise (Inoise) of the OTA in single-ended output configuration is found to be 818 nV/$\sqrt{}$Hz at 1 kHz frequency, as shown in Fig. 7. Its Inoise is 9 times more as compared to gate-driven circuit since gate g_m is 3 times of bulk g_{mb} in 180 nm CMOS process [6].

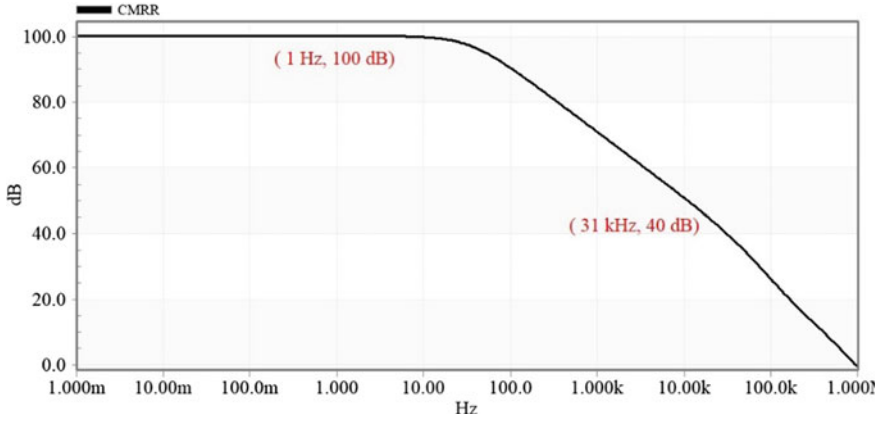

Fig. 5 AC sweep response to yield CMRR of the designed BD-OTA

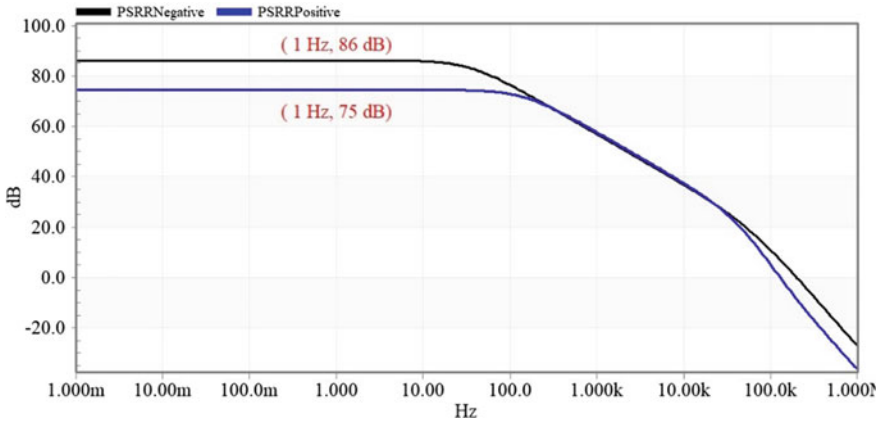

Fig. 6 AC sweep response to yield PSRR+ and PSRR− of the designed BD-OTA

3.2 Simulation Under Unity Gain Configuration of BD-CM-MO-OTA

Figure 8 shows DC sweep response plots, i.e., positive polarity FD voltage, ($V_{o} - V_{o-}$), and negative polarity FD voltage, ($V_{o-} - V_{o}$), for SC-CM-BD-OTA. This DC sweep has been simulated in unity gain configuration of fully differential OTA using four numbers of resistors each of 10 kΩ [36].

Figure 9 shows the single-ended output node-based error voltage ($V_{o1} - V_{in}$) in DC sweep simulation setup for single-ended output node of V_{o1}. It has shown good linearity for input common mode range of ±200 mV. So, sinusoidal amplitude up to the 200 mV can ensure good linearity and less total harmonic distortion (THD).

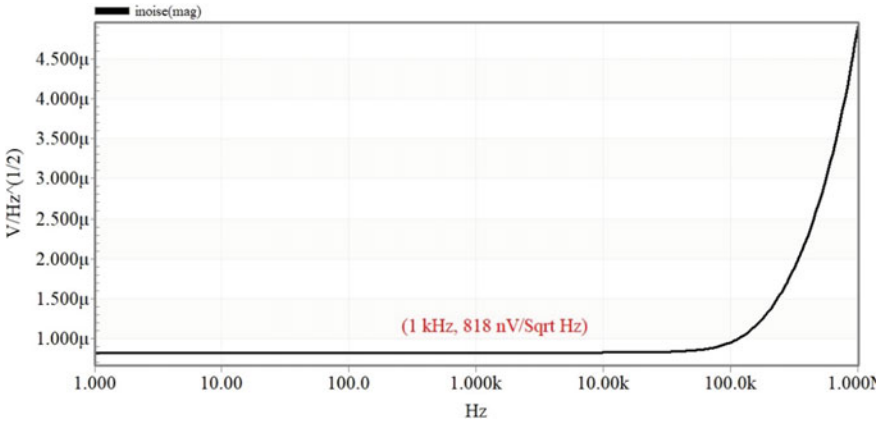

Fig. 7 Inoise contribution of BD-CM-MO-OTA

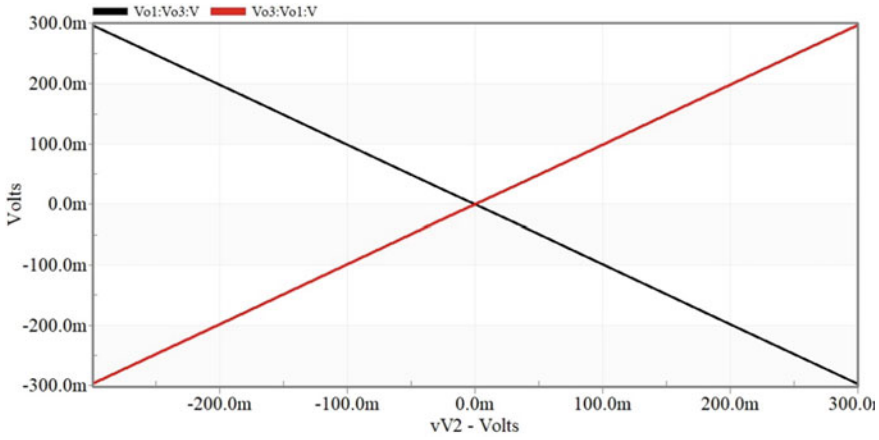

Fig. 8 DC sweep response and input common mode range of the designed FD-BD-SC-CM-MO-OTA

Figure 10 shows transient response when pulse of 250 mV amplitude of 500 Hz frequency is applied to non-inverting terminal in unity gain configuration of OTA. The output pulse in single-ended output case has ensured the positive and negative slew rates of 5.7 and 3.33 V/ms. However, equal positive and negative sloping rates for fully differential case are found to be 40 V/ms (figure is not placed for FD cases). Thus, average slew rates for SE and FD conditions are 4.5 and 40 V/ms.

Table 2 lists simulation results of this BD-MO-OTA. It shows some of results, say gain, GBW, PM and GM in fully differential mode, some others, say CMRR, PSRRs, Inoise in single-ended mode, THD and slew rates are simulated in unity gain configuration of FD-OTA. To convert a FD-OTA into unity gain mode, four equal resistors each of 10 kΩ are used. Two resistors are used in positive output to

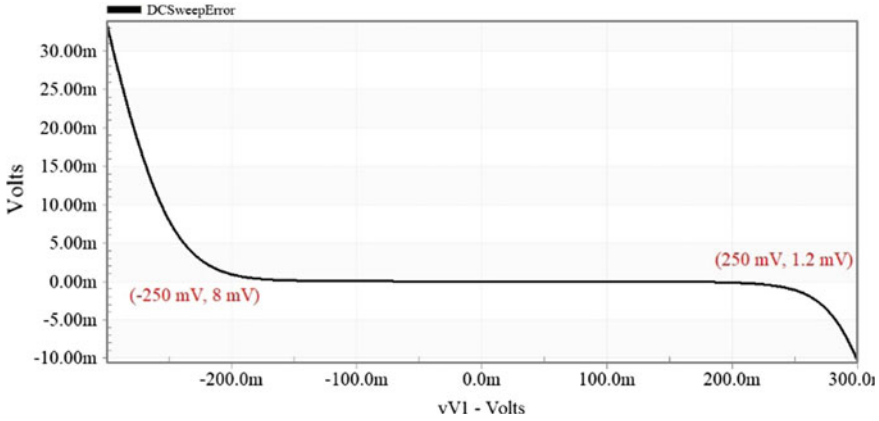

Fig. 9 DC sweep error voltage of BD-MO-OTA in single-ended output condition

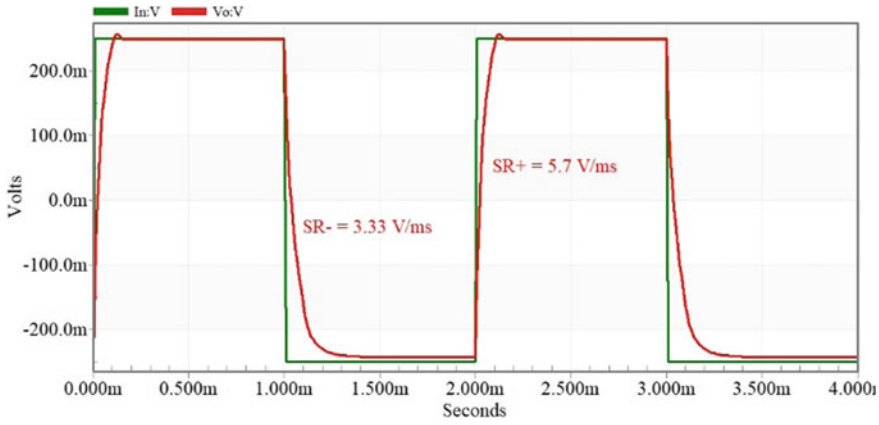

Fig. 10 Pulse transient response-based slew rates and settling behavior of BD-MO-OTA for its single-ended output node mode

inverting input path, and remaining two are used in negative output to non-inverting input path to ensure 100% negative feedback of both the output nodes [38]. However, its slew rates are simulated for both of SE and FD cases. It has shown quite symmetric positive and negative slew rates in FD configuration.

Table 2 Simulated performance results of BD-SC-CM-MO-OTA

Performances	Simulation condition	Results
FD gain (dB)	$[(V_{o+}) - (V_{o-})]$, Load $C_L = 15$ pF	78
FD GBW (kHz)	do	13.5
FD PM (°)	do	63
GM (dB)	do	31
SE CMRR (dB)	do	100
SE PSRR+ (dB)	do	75
SE PSRR− (dB)	do	86
Inoise (nV/Sqrt Hz)	Single-ended mode	818
Slew rates (V/ms)	Single-ended mode	5.7, 3.3
Slew rates (V/ms)	Fully differential mode	40, 40
THD (dB) unity gain	0.25 V peak, 100 Hz sine wave	−38
Power dissipation (nW)	V_{DD} and $V_{SS} = \pm 0.3$ V, $I_{Bias} = 20$ nA	104

4 Applications of BD-CM-MO-OTA Cells

Multiple output OTAs are usable in SIMO and MISO filters containing minimum numbers of active cells, FD-OTAs-based integrators, rectifiers, instrumentation amplifiers, etc. FD output versions provide noise immunity due to extremely high CMRR and reduced THD due to even harmonic cancelations. So, the designed MO-OTA can be used in several applications.

4.1 Diode-Less Full Wave Rectifier

Figure 11 shows MO-OTA-based full wave rectifier which does not need diodes. It uses a differential input and three-outputs-type OTA, say SC-CM-BD-MO-OTA used in this work. Two similar polarity outputs are V_{o1} and $V_{o2,}$ and the third one is an anti-phase output, say $V_{o3} = -V_{o1} = -V_{o2}$. It uses two controlling switches made of CMOS devices M_n and M_p and one load resistor R_L of value 1.2 MΩ. The single-ended input V_{in} generates positively saturated, $+V_{sat}$ (0.3 V), and negatively saturated, $-V_{sat}$ (−0.3 V), voltage levels at V_{o2} node in positive and negative cycles of input signal, respectively [27, 28]. Thus, during positive half-cycle M_n is ON and M_p is OFF and vice versa during negative half of input cycle. But, during both the cycles, the load current flows in same direction and full wave rectified output voltage appears across its load R_L.

Figure 12 shows simulated results of full wave rectifier when a sine wave input of 1 Hz frequency and 20 mV amplitude is applied in single-ended input configuration.

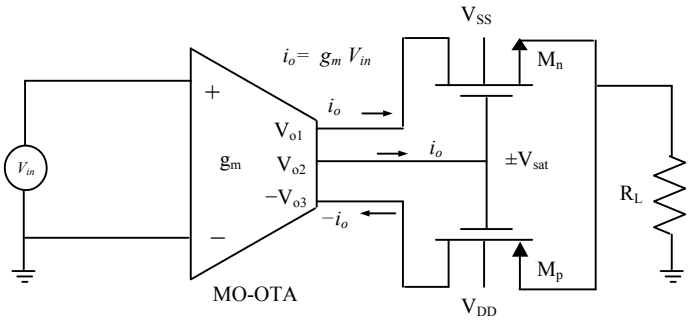

Fig. 11 MO-OTA-based non-inverting full wave rectifier

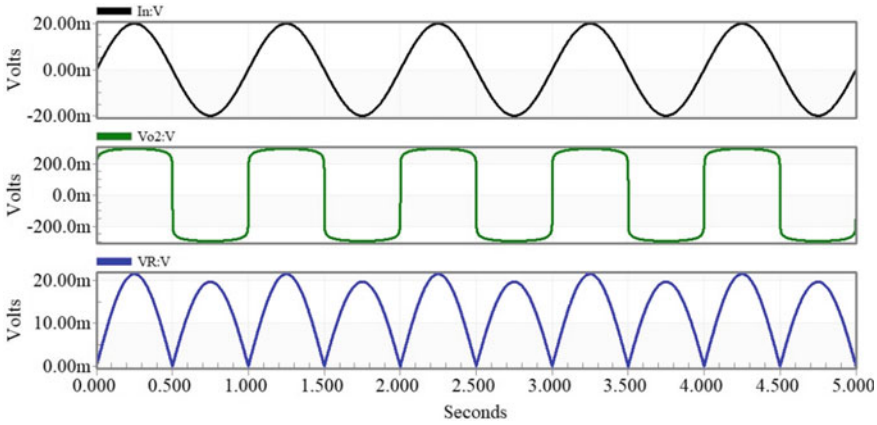

Fig. 12 Simulated result of SC-CM-BD-MO-OTA-based non-inverting FWR

The input, $V_{o2,}$ and output wave forms are shown in Fig. 12. It can rectify sine wave input of frequency range 1–500 Hz and amplitude range 100 µV to 30 mV with good accuracy. The aspect ratio of switches M_n and M_p are of values 40 µm/0.5 µm and 80 µm/0.5 µm, respectively, with load $R_L = 1.2$ MΩ.

Figure 13 shows the circuit schematic of inverting FWR, in which nMOS switch M_n is driven by negative output $V_{o3-,}$ and pMOS switch M_p is driven by positive V_{o1} signals, and common gates of switches are driven by positive output V_{o2}. This circuit works as inverting FWR [28, 30].

Figure 14 shows output of negative peak rectifier with switching MOS sizes of $M_n = 40$ µm/0.5 µm and $M_p = 80$ µm/0.5 µm.

Figures 15 and 16 show the DC transfer characteristics of non-inverting and inverting FWR circuits which depict the maximum processing amplitude limit of these rectifiers, and it is limited to 30 mV [39].

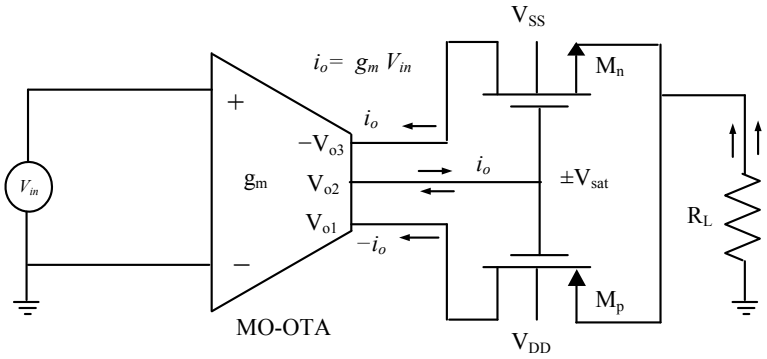

Fig. 13 Simulated result of SC-CM-BD-MO-OTA-based current mode inverting FWR

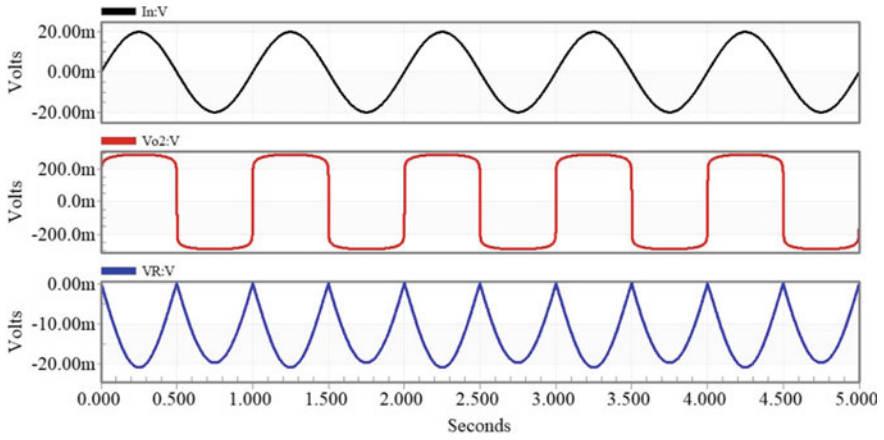

Fig. 14 Simulated result of SC-CM-BD-MO-OTA-based current mode inverting FWR

4.2 MISO Biquadratic Filter Using BD-MO-OTA

The designed MO-OTA can be applied to achieve voltage mode and current mode MISO and SIMO types of low-power low-frequency biquadratic filters usable for biosignal processing [31–33]. This SC-CM-BD-MO-OTA has been utilized to design a voltage mode biquadratic filter which provides band pass (BP), low pass (LP), high pass (HP), band reject (BR) and all pass (AP) MISO-type filters as shown in Fig. 17 [31]. This filter is comprised of one BD-MO-OTA (g_{m3}) which contains two positive and one negative output nodes and four numbers of single-ended output transconductors, namely g_{m1}, g_{m2}, g_{m4} and g_{m5}. The OTA cells g_{m4} and g_{m5} are configured as resistors of values $1/g_{m4}$ and $1/g_{m5}$, respectively. This MISO filter contains three inputs V_{in1}, V_{in2}, V_{in3} and a single output node V_{out}.

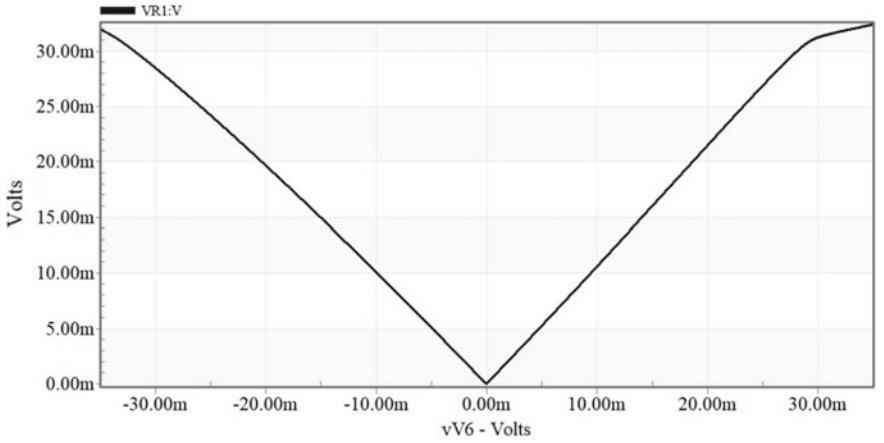

Fig. 15 DC transfer curve current mode non-inverting FWR

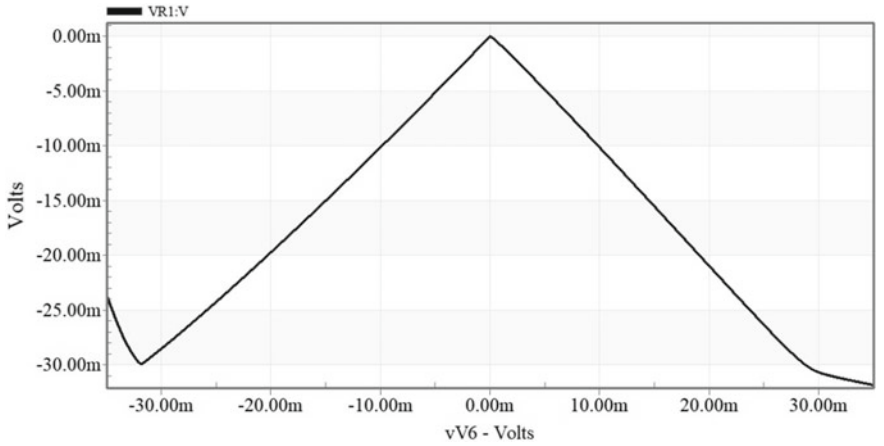

Fig. 16 DC transfer curve current mode non-inverting FWR

This MISO filter is to be separately programmed for each type of filter response. Table 3 lists the transfer functions of all five standard generic prototype responses and circuit setup conditions for MISO-type filter.

The routine nodal analysis of this MISO filter can be performed to get its overall transfer function as shown in (3)

$$V_o(s) = \frac{N(s)}{D(s)} = \frac{V_{in3} g_{m3} C_1 C_2 s^2 - V_{in2} C_1 g_{m2} g_{m3} s + V_{in1} g_{m1} g_{m2} g_{m3}}{g_{m4}\left(s^2 C_1 C_2 + s C_1 g_{m3} + g_{m2} g_{m3} g_{m4}\right)} \quad (3)$$

where $g_{m3} = g_{m4}$ has been considered. The (3) can be rearranged to (4)

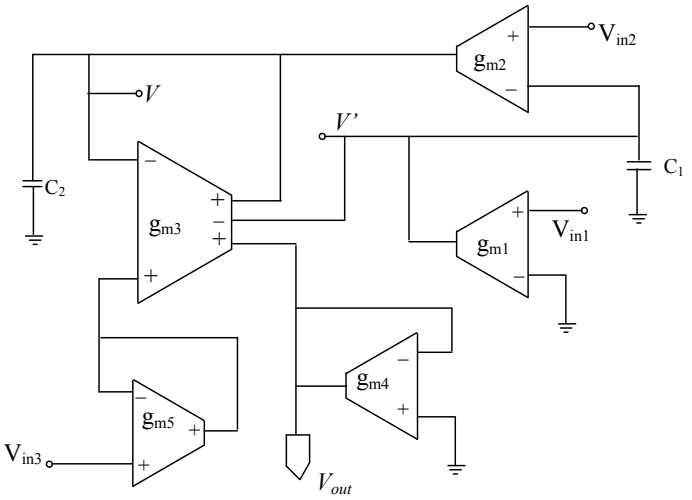

Fig. 17 MISO-type biquadratic filter using single three-output BD-MO-OTA and four SE OTAs [31]

Table 3 Standard generic transfer functions and circuit setup for MISO filter

Filter-type	Standard-generic transfer function	Pass-band gain	Circuit set-up for MISO
LPF	$A_o/\left(s^2+\omega_o s/Q+\omega_o^2\right)$	A_o/ω_o^2	$V_{in1}=V_{in}$, $E_2=E_3=0$
HPF	$A_2 s^2/\left(s^2+\omega_o s/Q+\omega_o^2\right)$	A_2	$V_{in3}=V_{in}$, $V_{in1}=V_{in2}=0$
BPF	$A_1 s/\left(s^2+\omega_o s/Q+\omega_o^2\right)$	$A_1 Q/\omega_o^2$	$V_{in2}=V_{in}$, $V_{in1}=V_{in3}=0$
BRF	$A_2\left(s^2+\omega_o^2\right)/\left(s^2+\omega_o s/Q+\omega_o^2\right)$	A_2	$V_{in1}=V_{in3}=V_{in}$, $V_{in2}=0$
APF	$A_2\left(s^2-\omega_o s/Q+\omega_o^2\right)/\left(s^2+\omega_o s/Q+\omega_o^2\right)$	A_2	$V_{in}=V_{in2}=V_{in3}=V_{in}$ and $g_{m3}=g_{m5}=g_m$

where ω_0 and Q are the pole frequency and quality factor

$$V_o(s)=\frac{N(s)}{D(s)}=\frac{V_{in3}s^2-V_{in2}g_{m2}s/C_2+V_{in1}g_{m1}g_{m2}/C_1C_2}{s^2+g_{m4}s/C_2+g_{m2}g_{m4}/C_1C_2} \tag{4}$$

Comparing (4) to second-order standard transfer function given in Table 2, we can find the central angular frequency (ω_0) and quality factor (Q) for BPF and BRF

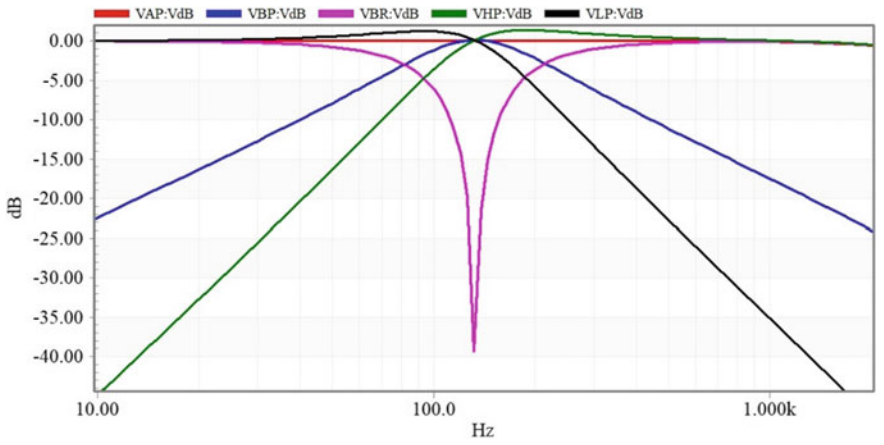

Fig. 18 Simulated responses of MISO biquadratic filter using filter capacitor $C = 1$ nF

to be:

$$\omega_0 = (g_{m2}g_{m4}/C_1C_2)^{1/2} \text{ and } Q = \sqrt{g_{m2}C_2/g_{m4}C_1} \tag{5}$$

For equal component design, if $C_1 = C_2 = C$ and equal value of each transconductors $Q = 1$ and $\omega_0 = g_m/C$ [31], the various responses of this filter when simulated with $C = 1$ nF are shown in Fig. 18. These simulations have been carried out in specific connection diagram for each response as mentioned in Table 3.

The band reject response has offered band reject deepness of −40 dB and angular notch frequency of 132 Hz, and its band pass response has offered f_L, f_H, ω_0, bandwidth and Q of 80 Hz, 220 Hz, 132 Hz, 140 Hz and $Q = 0.95$, respectively, whereas the cut-off corner frequencies for LPF and HPF responses are found to be $f_H = 170$ Hz and $f_L = 105$ Hz. This voltage-mode MISO filter has consumed total power of 384 nW. Its central and cut-off frequencies can be tuned by slightly adjusting the bias current of the concerned transconductor through its external pin.

5 Conclusion

This paper has presented a low-voltage bulk-driven subthreshold multiple-output OTA operating in weak inversion region. This OTA is utilized to implement non-inverting and inverting low-voltage full wave rectifiers and MISO-type biquadratic filter. In the emerging field of biomedical single processing OTAs, rectifiers and filters are an important building block. The OTA has offered fully differential open-loop gain, GBW and phase margin of 78 dB, 13.5 kHz and 63°, respectively. The CMRR and PSSR of OTA of the designed OTA are high enough to attenuate the stray noise to a large extent. The power consumption of OTA is 104 nW. The non-inverting

and inverting full wave rectifiers consumed low power of 110 nW, whereas MISO biquadratic filter consumed low power of 384 nW which is suitable for band limiting and wave shaping of biomedical signals.

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A Multi-tiered Automatic License Plate Recognition Strategy Using YOLOv2 Detector

R. Shivadeep and R. Srikantaswamy

1 Introduction

Automatic license plate recognition (ALPR) is a system that intends to achieve detection and recognition of vehicle number plates without necessitating direct human intervention. It is of paramount importance in both civilian and commercial applications. This includes electronic tolling system, parking and billing automation, vehicle tracking, access control, vehicle security and law enforcement, etc.

Research in ALPR is being pursued to develop and improve upon several lacunae in the current set of methodologies in order to increase its accuracy and universality of deployment. Also, the approach toward producing a highly efficient ALPR system is unique for every country, as the number plate length, format, and environmental conditions vary widely. This is especially true in the Indian context as number plates do not follow a standardized display, and image acquisition is complicated due to interfering ambiences [1].

Typical ALPR approaches can be divided into two significant phases: license plate detection and extraction and license plate recognition. Although, a number of works further treat them as consisting four main stages: moving vehicle detection and extraction, license plate detection and extraction, character segmentation, and character recognition. Commonly used algorithms for these stages include: Haar-cascade classifiers, Lukas-Kanade optical flow approach for moving vehicle detection, preprocessing with extraction of global image and edge features for plate detection, spectral analysis for character segmentation, SVM, LDA and CNN models for character recognition, etc. Most of these techniques are ad hoc in nature and thus compromise

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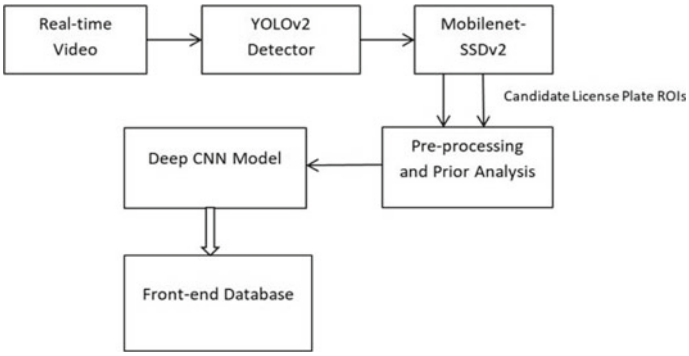

Fig. 1 Process flow of the proposed ALPR system

universality for accuracy [5]. The proposed ALPR system uses a multi-tiered strategy (refer Fig. 1) for license plate detection and extraction using YOLOv2 object detector to segment the moving target vehicle and mobilenet-SSD (single shot detector) to localize candidate license plate ROIs, thereby reducing the search space for recognition. After the application of various morphological operations and prior knowledge for character analysis, the license plate characters are segmented for consequent recognition by a custom trained deep CNN model.

The rest of the paper is organized as follows: Sect. 2 describes the YOLOv2 detector for moving vehicle detection, Sect. 3 discusses the popular single shot detection model mobilenet-SSDv2 for license plate ROI extraction, Sect. 4 elaborates on pre-processing techniques used, Sect. 5 explains prior knowledge needed for efficient character analysis, Sect. 6 details the deep CNN model employed, Sect. 7 shows the experimental results obtained, and Sect. 8 concludes the paper by discussing the key improvisations over previous works.

2 Moving Vehicle Detection and Segmentation

The goal of this stage is to detect and segment only the moving target vehicle from the input video sequence. The key challenges in this stage include motion blur induced due to the capturing of a fast moving car on a low frame rate device and the presence of other moving objects that resemble the target vehicle's pre-defined parameters such as windshield aspect ratio, frontal area, edge features, and so on. The proposed ALPR system employs the YOLOv2 (designed by J. Redmon et al.) [9] deep CNN object detection model to achieve extremely fast generalized object recognition capable of decoding the contextual information by looking at the video frame only once (hence the name 'You Only Look Once') and classify the objects into different classes accordingly (including non-vehicle objects like traffic lights, road studs, humans crossing the road, etc.).

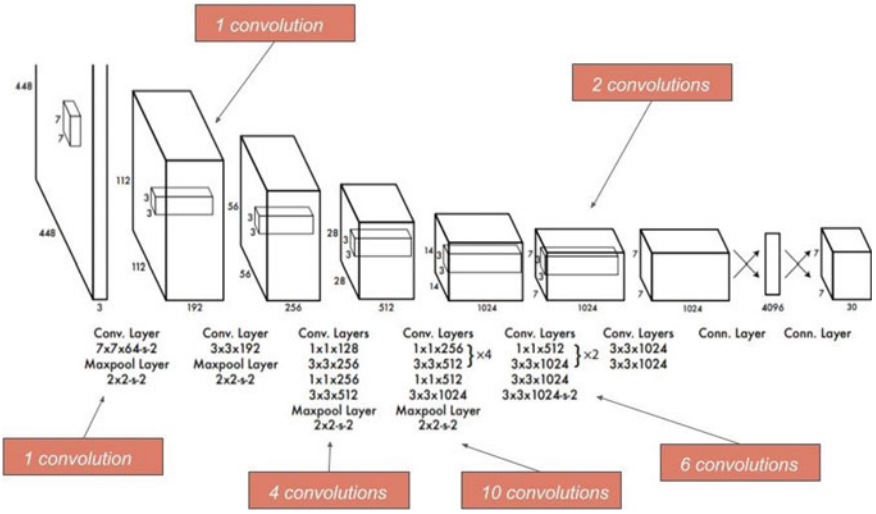

Fig. 2 YOLOv2 architecture

YOLOv2 is an ingenious deep CNN object detection system that parses the input frame only once to establish bounding boxes with corresponding class probabilities over different moving objects after partitioning the image into distinct regions based on a non-max suppression function that avoids repeated detection of the same object, thus making it faster and more precise compared to Haar-feature cascade classifiers and R-CNN models [12].

The proposed ALPR system utilizes the high mAP and superior frame parsing rate (155 FPS) of the YOLOv2 architecture (refer Fig. 2) to improvise over the earlier works.

The network is designed to make full use of local intelligible differentia such as number and shape of tires, lamp shape, head light contour, etc., that exist in the lower layers of the CNN by applying a multi-layer feature fusion strategy. The local features go through 3×3 and 1×1 convolution layers followed by Reorg/4 for down-sampling with a factor of 2, in order to preserve the feature maps in lower layers. This is followed by the fusion of local and global features to understand the nuances among different vehicle types. The repeated high-level convolution layers of size $3 \times 3 \times 1024$ are removed if the vehicles do not possess many intelligible differentia.

The bounding box added around the target vehicle in a real-time video input by YOLOv2 detector is as shown in Fig. 3.

Among the several detected moving objects in a video frame, the one with the maximum class probability (decided on the basis of proximity and frame of reference of approach towards the camera) of being the target vehicle is cropped from the image by applying the following pre-processing morphological operations sequentially:

Fig. 3 Bounding box with maximum class probability

(1) *Throwing the image to HSV space:* This is done to separate image luminance from the color information, as color description of the vehicle needs to be preserved for license plate segmentation [2].
(2) *Adaptive threshold the HSV image:* This is performed to binarize the non-bounding box regions for cropping.
(3) *Close the thresholded image (refer* Fig. 4*):* A pair of 5×5 structuring element $\{s1, s2\}$ is applied to enlarge the boundaries of bright regions in the image (f) by probing shadowed and illuminated regions using *Hit and Miss Transform* [2] as given by the equation:

$$f \circledast \{s_1, s_2\} = (f \ominus s_1) \cap (f^c \ominus s_2) \tag{1}$$

(4) *Extract edge features of the closed image:* This is performed using a 3×3 Sobel kernel. The contiguous edges extracted are sorted based on area using the merge sort algorithm to locate the nth largest continuous contour representing

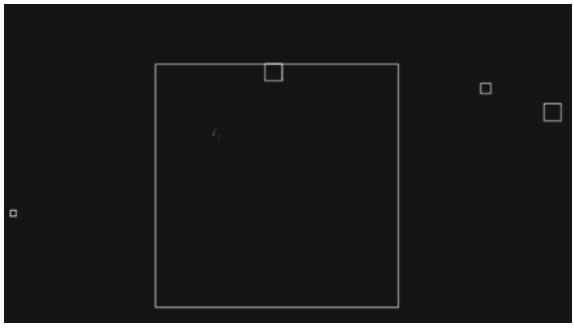

Fig. 4 Closed image showing different bounding boxes

Fig. 5 Cropped image of the target vehicle

the bounding box around the target vehicle with maximum class probability, using which the vehicle image is cropped out (refer Fig. 5).

3 License Plate Detection and Extraction

The proposed ALPR uses the single shot detector (SSD) model mobilenet-SSDv2 (proposed by Google) as it is relatively faster (achieves > 70% mAP at 60 FPS) and more accurate compared to R-CNN and ad hoc hybrid algorithms employing morphological operations, while being able to process the entire image in one shot by handling both region proposal and bounding box prediction by itself (thus, the name 'Single Shot Detector') on embedded processor-based applications [10]. The SSD neural network architecture performs depth-wise separable convolutions. The training phase consisting of feeding about 15,000 620 × 480 PNG images of different vehicles annotated with the tuple ($x$min, $y$min, $x$max, $y$max) describing the corner coordinates of the license plate. The convolution layer performs two sub-tasks: a depth-wise convolution to filter the relevant features and a 1 × 1 point-wise convolution to parse the filtered inputs, thereby forming the depth-wise separable convolution block collectively [2]. This drastically reduces the computational latency encountered in traditional convolution approaches.

A. *Network Architecture*

The expansion layer branches input channels into multiple output channels. For a 24-channel tensor going into the input block, the expansion layer produces a new tensor having 24 × 6 = 144 channels upon which the depth-wise separable convolution

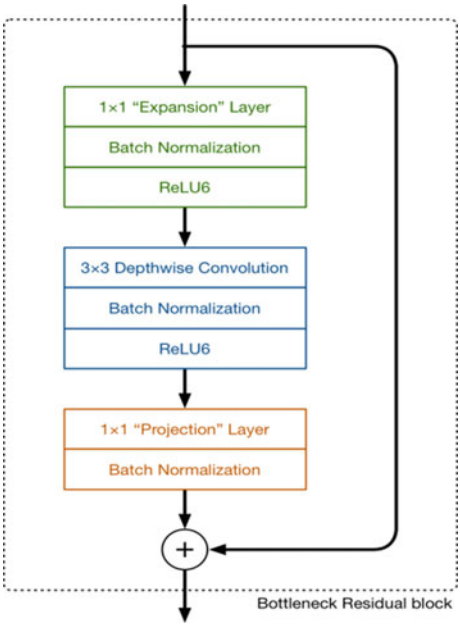

Fig. 6 SSDv2 workflow

layer performs convolution before the projection layer diminishes it back into a 24-channel tensor to retain its dimensions (refer Fig. 6).

B. *Loss Function*

For N number of matched bounding boxes, the loss function depends on the localization loss L_{loc} and confidence loss L_{conf} functions as shown in Eq. 2.

$$L(x, c, l, g) = \frac{1}{N}(L_{\text{conf}}(x, c) + \alpha L_{\text{loc}}(x, l, g)) \tag{2}$$

L_{loc} is the localization loss (resembling that in Faster R-CNN) which is the smooth $l1$ loss between the predicted box (l) and the ground-truth box (g) parameters, which include the offsets for the center point (c_x, c_y), width (w), and height (h) of the bounding box.

C. *Default Box Scale and Aspect Ratio*

To predict from m feature maps, the kth feature map is used to find Sk (scale). Assuming the conventional values for $s$min (scale at the lowest layer) as 0.2 and $s$max (scale at the highest layer) as 0.9, and all layers as being equally spaced, the scale of default boxes is as defined by Eq. 3.

$$s_k = s_{\min} + \frac{s_{\max} - s_{\min}}{m - 1}(k - 1), \quad k \in [1, m] \tag{3}$$

Fig. 7 Cropped license plate ROI

For each scale *Sk*, there are five non-square aspect ratios as given by Eq. 4.

$$a_r \in \left\{1, 2, 3, \frac{1}{3}, \frac{2}{3}\right\}; \quad w_k^a = S_k\sqrt{a_r}; \quad h_k^a = S_k\sqrt{a_r} \tag{4}$$

For a 1:1 aspect ratio (typically in a resized license plate ROI), the scale $S^{'}$ is obtained as defined by Eq. 5.

$$S_k' = \sqrt{S_k S_{k+1}} \tag{5}$$

Thus, there can only be 6 bounding boxes in all with different aspect ratios. For layers having 4 bounding boxes, $ar = 1/3$ and 3 are omitted [12].

The mobilenet-SSDv2 model ejects candidates for license plate ROI (for images with large vehicle density) based on the learned parameters from training dataset and selects the most probable ROI based on the default box scale and aspect ratio as decided by the loss function [11]. This skips the tedious processes of applying morphological operations on the segmented vehicle image to analyze edge features, area, character distribution, etc., as performed in customized hybrid algorithmic approaches [7]. The cropped license plate region tagged as being most probable by the SSD is shown in Fig. 7.

4 Pre-processing of Segmented ROI

The segmented ROI needs to be subjected to a series of morphological operations [3] in order to reduce misrecognition rate. Following are the pre-processing techniques applied on the extracted license plate ROI:

A. *Grayscaling*

The extracted license plate ROI is transformed inside a HSV model to preserve and isolate the color content, after which it is grayscaled (refer Fig. 8) based on the

Fig. 8 Grayscale image

intensities of RGB color channels as shown in Eq. 6.

$$\text{Gray level} = 0.299 \times \text{R} + 0.587 \times \text{G} + 0.114 \times \text{B} \tag{6}$$

The **cv2.split()** method parses across the 640x480 HSV PNG image to grayscale it.

B. *Contrasting and Gaussian Blurring*

The character attributes in the grayscale image are accentuated by contrasting. The *White Top Hat Transform* is generated by removing the *opened* image from its original form. The *Black Top Hat Transform* is further obtained by extracting grayscale features from the *closed* form.

Let f: $E \rightarrow R$ be the grayscale image, mapping points from Euclidean space R^2 into the real line with $b(x)$ being the structuring element.

White top hat transform is given by:

$$T_w(f) = f - f \circ b \tag{7}$$

Black top hat transform is given by:

$$T_b(f) = f - f \bullet b - f \tag{8}$$

The contrasted image is produced by subjecting every pixel value to the linear function (refer Fig. 9) as given by Eq. 9.

$$f_{\text{contrast}} = f + T_w(f) - T_b(f) \tag{9}$$

The undesired detail and noise present in the contrasted image are eliminated by blurring it with Gaussian smoothing (2D isotropic) operator having a standard 5 × 5 kernel (refer Fig. 10).

C. *Adaptive Gaussian Thresholding*

Fig. 9 Contrasted image

Fig. 10 Gaussian blurred image

Fig. 11 Thresholded image

The threshold (t) is a linear transform of weighted average of pixel intensities in the immediate neighborhood. Noisy outliers are removed, and color gradients are smoothened by inverting the adaptively binarized function (block size used is 19). Figure 11 shows the binarized image of license plate ROI [4].

5 Prior Analysis Strategies

Character contours are exploited to ease segmentation process by applying different prior analyses strategies. The OpenCV function **cv2.findcontours()** employs *Green's Theorem* (refer Eq. 10) to discover and group relevant contours into a list, by determining a line integral over the non-negative, unbroken character outline C, and a double integral over the ROI surface enclosed by C. Later, the (x, y, w, h) coordinates of bounding boxes (refer figure) are produced based on the contours, for enclosing all the character attributes extracted from the training database (refer Fig. 12). The strategy vaguely approximates bounded characters based on pre-defined attributes like corner distribution, edge features, and encompassing area [9].

$$\oint_0^c (L\,\mathrm{d}x + M\,\mathrm{d}y) = \int\int_0^D \left(\frac{\partial M}{\partial x} - \frac{\partial L}{\partial y}\right)\mathrm{d}x\,\mathrm{d}y \tag{10}$$

where L and M are functions of (x, y) defined on an open region containing D and having continuous partial derivatives.

CCA [6] with a 4 × 4 raster scan is applied on this image to obtain the fully annotated image showing bounding boxes around the characters (refer Fig. 13).

A. *Finding List of Lists of Matching Characters*

Once the contours are extracted, they are compared against an existing database of character contours to generate a list that contains lists of matching contours for all

Fig. 12 Possible characters based on contours

Fig. 13 Fully annotated image

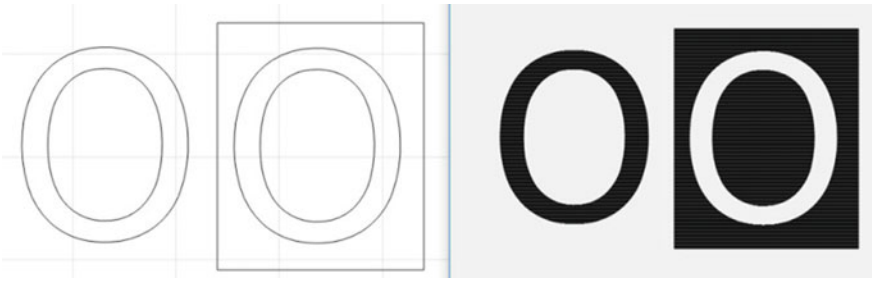

Fig. 14 Overlapping contours

characters. If any of the proposed contours do not match in length or attribute to the one extracted from the ROI, they are ignored from further operations.

B. *Final List of Matching Characters*

The most probable character for a given contour is extracted for every contour in the ROI to ultimately form a list of matching characters. This is done by parsing every character in the database for attributes like pixel density, tilt, and dimensions against the obtained parameters of character contours.

C. *Removal of Overlapping Contours*

Some of the characters that contain identical contours inside them need additional prior analysis in order to cut down the computational latency by repeated parsing of irrelevant contour definitions (refer Fig. 14). This is pre-dominantly observed in case of letters like D and O and for numbers like 9, 6, and 0. If overlapping contours are not segregated, the character recognition engine runs the risk of exceeding standard license plate text length by including inner and outer outlines for some characters.

6 Character Recognition

Initially, the resized 24 × 14 character input is parsed with a 5 × 5 kernel to generate 6 20 × 10 feature maps in the variable receptive field, which is followed by a 2 × 2 subsampling layer to reduce the feature map dimension to 10 × 5, again followed by a 5 × 5 convolutional layer (using convolutions in higher dimensional spaces)

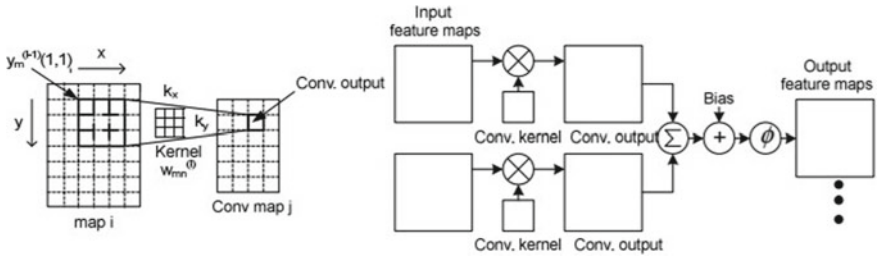

Fig. 15 Spatial convolutions in convolutional layer

(refer Fig. 15) in a feed-forward network trained with back propagation aiming to minimize the loss function [6]. The fully connected layer accepts 16 6 × 1 feature maps to classify the input among one of 35 possible alpha-numeric characters present in separate engines for numbers and alphabets. The generalization capability of the network is improved with cross-validation between training and testing datasets that are relevant to Indian license plates. Seldom used letters like 'I,' 'O,' and 'Z' are deemed as least probable if there is a tie-up between the competing characters. While padding the input, the feature units are centered on the border, and each convolution layer reduces the feature size from n to $(n - 4)/2$ [8]. The total numbers of training and testing datasets involved are 12,800 images and 1730 images, respectively.

7 Results

The proposed ALPR system performs with increased accuracy and speed, mainly because of YOLOv2 and mobilenet-SSDv2 deep CNN detectors employed in a two-tier license plate extraction scheme, which is error-prone if achieved using composite ad hoc algorithms like optical flow approach or Haar-cascade classifier. The performance parameters of YOLOv2 are defined in the following execution status .cmd file (refer Fig. 16). With YOLOv2, the system's ability to swiftly and accurately detect the moving target vehicle among other objects in the frame is significantly increased to 94.55% as given by the detection parsing rate. This has an overbearing impact on the character recognition rate as well as defined by the comparatively higher recognition parsing rate of 89.90%. For cropping the target vehicle from the most optimal frame by mobilenet-SSDv2, an appreciable bounding box confidence score of 0.92 is significant.

A series of tables showing the succession of ALPR phases (in order) along with the key intermediate stages such as prior analysis techniques and morphological operations for multifarious environmental conditions viz. reflective ambience, motion blur, BG clutter, trailing shadows, and non-standard fonts is included in this section to demonstrate the efficacy of the proposed ALPR on different vehicles like cars, bikes, and auto-rickshaws.

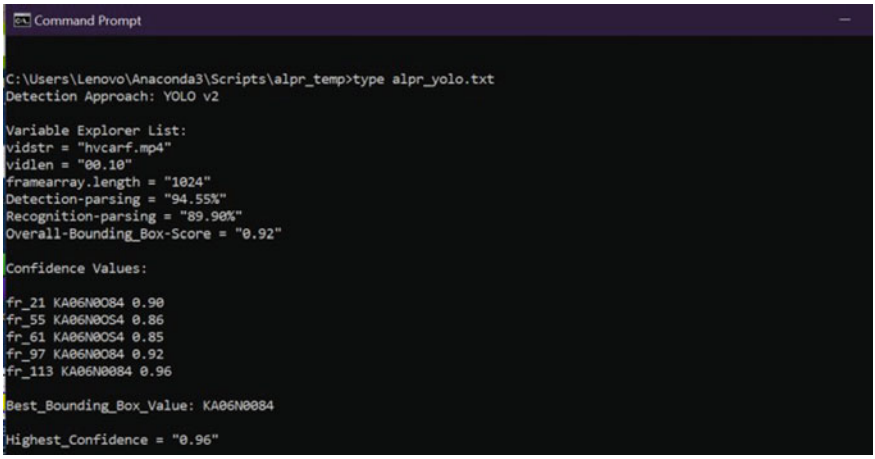

Fig. 16 YOLOv2 performance parameters

Figure 17 demonstrates the efficiency of YOLOv2 in identifying the moving target vehicle despite contrasting illumination above and below the license plate ROI. This is because of attaching the maximum class probability to the bounding box around the target vehicle based on parameters such as frontal area that remain invariant to lighting conditions. Also, the deep CNN detector of mobilenet-SSDv2 ignores the prefix 'IND' symbol at the beginning of the license plate character stream.

Figure 18 demonstrates the ALPR system for induced motion blur deliberately caused by erratic movement of a lower frame rate camera with poor resolution. Misrecognition of the pipe symbol (|) was by restricting the length of license plate characters to not lesser than 9 and not greater than 10 alpha-numerals.

Figure 19 demonstrates the system for a two-wheeler (implying flexible classification attributes for YOLOv2) with shadowed license plate.

Fig. 17 Results of the proposed ALPR system under contrasting illumination conditions

Fig. 18 Results of the proposed ALPR system with induced motion blur

Fig. 19 Results of the proposed ALPR system with trailing shadow regions

Figure 20 demonstrates the performance of the ALPR system on license plates having non-standard and irrelevant text format for an auto-rickshaw. The deep CNN

Fig. 20 Results of the proposed ALPR system with non-standard license plate text

character recognizer can identify the 'K' even when the letter's vertical line is missing in the list of possible contours.

8 Conclusion

The adoption of a multi-tiered ALPR strategy with YOLOv2 and mobilenet-SSD detection models is shown to be effective in counteracting several shortcomings of previous approaches that depend on regularized implementation of ad hoc techniques or hybridization of algorithms like Lukas-Kanade optical flow approach, Haar-cascade classifier, Harris corner detection models, etc. The capability of YOLOv2 to detect multiple objects at once, combined with mobilenet-SSDv2's fastness over R-CNN reduce both computational latency and resource overloading factors drastically. The progressive deployment of shallow CNN with the SSD model followed by a deep CNN for character recognition narrows down the search space appreciably, thus increasing the overall speed and accuracy of the system. In lieu of applying a succession of morphological transforms at each stage of ALPR, performing prior character analyses with removal of overlapping contours in characters like D, O, 0, 9, etc., restricting the license plate text length subject to the context and region, auto-suggesting characters based on missing contours plays a crucial role in hastening the segmentation process while improving the recognition rate significantly.

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Bandwidth Enhancement of Trapezoidal Toothed Log-Periodic Antenna Using Slot Configuration

Situ Rani Patre and Satya Prakash Singh

1 Introduction

The trapezoidal toothed log-periodic antennas (TTLPAs) belong to the family of frequency independent antenna (FIA). The FIA ideally provides infinite bandwidth due to their self-scaling, self-complementary and self-similar characteristics. All three aforesaid principles are applicable to the geometry of conventional TTLPA; however, practical antenna has finite size which makes it a broadband antenna. It was discovered by DuHamel [1] in late 1950. The conventional TTLPA has symmetrical arms therefore exhibits balanced property and, hence, requires a balanced-to-unbalanced transition (balun) for appropriate excitation. The finite size of antenna and requirement of balun either degrade its impedance and/or pattern bandwidth or increases its complexity due to antenna-balun integration. In our previous work [2], the performance of metallic TTLPA excited using two different configurations of planar baluns was studied. The lower and upper cut-off frequencies and, hence, bandwidth of TTLPA depend on the length of largest and shortest tooth elements. Therefore, increment in elements size or modifications in antenna geometry becomes necessary for bandwidth improvement and/or size reduction of such antennas. However, the concept of dielectric loading is utilized for bandwidth improvement of metal TTLPA without disturbing the geometry and dimensions [3]. The dielectric-loaded TTLPA (DLTTLP) is efficient for bandwidth enhancement and/or size miniaturization but the radiation pattern distorts. Also, both TTLPA and DLTTLPA have non-planar configurations and require balun for excitation which makes it inconvenient for modern system. Furthermore, modern wireless systems require compact planar antennas, so that it can be accommodated within the limited size of devices along

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with other circuit components. Some planar log-periodic antennas are described in the literature but most of them are double-sided and provide unidirectional radiation pattern. In [4], a log-periodic dipole antenna fed through balun is described which provides unidirectional pattern, but its size is large. The requirement of balun is mitigated using CPW feed, but antenna size is large, and its radiation pattern is distorted [5]. CPW-fed slot antennas presented in [6, 7] are smaller in size, but the impedance matching is not good. In [8], author proposed a leaf-shaped log-periodic slot antenna that mitigates the aforementioned issues though the geometry design, and translation of such structure into other frequency range is a tedious task.

This paper aims to provide a comparative study on bandwidth enhancement techniques of trapezoidal toothed log-periodic antennas. For this study, different variants of TTLPAs designed by same author have been considered. In addition, a single-sided compact and wideband trapezoidal toothed log-periodic slot antenna (TTLPSA) is proposed, and its characteristics are described. Further, the bandwidth and geometrical property of proposed TTLPSA are compared with characteristics of earlier published TTLPAs. The proposed TTLPSA simultaneously provides wider impedance bandwidth of 8.25:1 (1.6–13.2 GHz) compared to earlier published TTLPAs. It also offers nearly stable gain and bidirectional radiation pattern over its operating bandwidth without utilizing balun.

2 Design Principle of TTLPA

The design principle of any log-periodic antenna is same as given in [1].

$$\tau = \frac{f_n}{f_{n+1}} = \frac{R_{n+1}}{R_n} \tag{1}$$

$$\sigma = \frac{r_n}{R_n} = \frac{r_n}{r_{n+1}} \tag{2}$$

where τ is geometric ratio, σ is the spacing factor, f_n and f_{n+1} are, respectively, the design frequencies of teeth of lengths R_n and R_{n+1} and r_n is the distance of corresponding tooth (R_n) from the centre. For the proposed antenna $f_{n+1} > f_n$ and $R_n > R_{n+1}$.

For this comparative study, the lowest design frequency is selected as 3 GHz, and four pair of elements is fixed. The length of largest element "R_1" is almost $\lambda/4$ long at the lowest design frequency of 3.1 GHz. Rest of the dimension are calculated using design Eqs. (1) and (2). Three different configurations of TTLPA are considered: metal TTLPA (TTLPA), dielectric-loaded TTLPA (DLTTLPA) and trapezoidal toothed log-periodic slot antenna (TTLPSA). The geometrical dimensions of all three antennas are kept same.

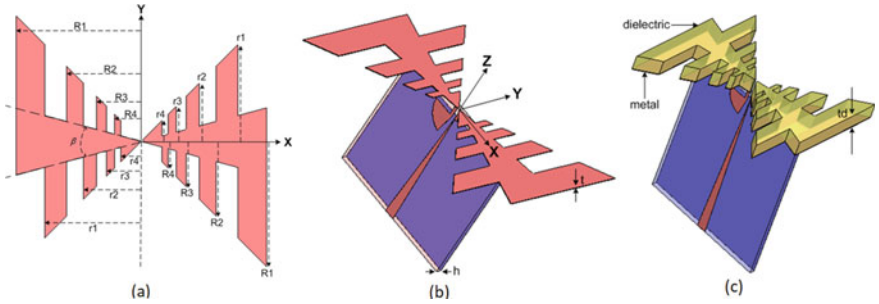

Fig. 1 Trapezoidal toothed log-periodic antennas: **a** geometrical dimensions, **b** metal TTLPA, and **c** dielectric-loaded TTLPA [3]

3 Antenna Configurations

3.1 Non-planar TTLPA

The metal TTLPA and DLTTLPA fall into non-planar category due to the vertical connection of antenna and balun as shown in Fig. 1. The detailed design optimum dimensions of antenna as well as balun (i.e. microstrip-to-coplanar stripline transition) can be found in [3]. For dielectric loading, a 5 mm thick Rogers RT/duroid 6010 having relative permittivity of 10.2 and loss tangent of 0.0023 is used.

3.2 Planar TTLPA

The planar version of TTLPA utilizes the slot arrangement, and the antenna is named as trapezoidal toothed log-periodic slot antenna (TTLPSA). The proposed TTLPSA is shown in Fig. 2. It is designed on 1.6 mm thick low cost FR4 substrate having relative permittivity of 4.4 and physical size of 50.9 $\times$ 50.9 mm^2. The 50 Ω CPW feed with tapered central strip is used to excite the slot antenna at its centre (zoomed section is shown in Fig. 2b). The present configuration is inspired by half-wavelength (0.5 λ) dipole slot antenna and metal trapezoidal toothed log-periodic antenna. Owing to the configuration of slot and modified CPW feed, the proposed TTLPSA antenna has overall electrical size of only 0.27 λ $\times$ 0.27 λ at its lowest frequency of 1.6 GHz, which is slightly larger than quarter-wave antenna. In other words, the proposed antenna is very compact as compared with the conventional TTLPA.

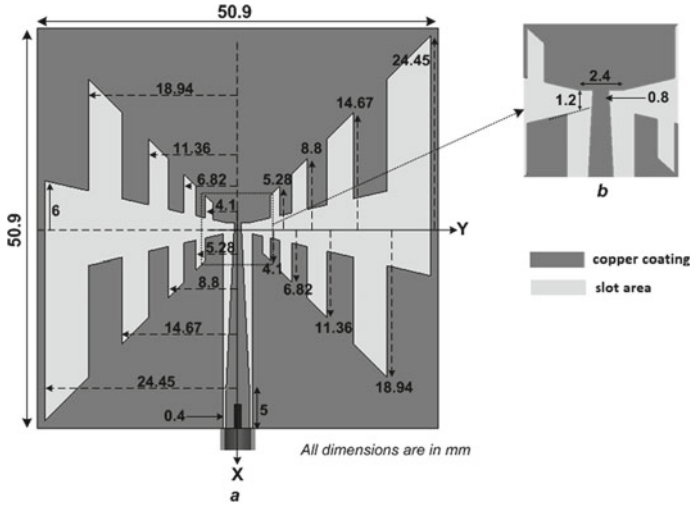

Fig. 2 Proposed trapezoidal toothed log-periodic slot antenna: **a** geometrical configuration along with optimum dimensions and **b** zoom section of central region

4 Result and Discussion

Simulations study of all the discussed antennas were carried out using finite element method-based Ansys high frequency structure simulator (HFSS).

4.1 Bandwidth Comparison

Bandwidth comparison is done using − 10 dB reflection coefficients. The reflection coefficient versus frequency characteristics of all three configurations of TTLPAs is shown in Fig. 3. It is seen from Fig. 3 that the proposed TTLPSA offers − 10 dB reflection coefficient bandwidths of 11.6 GHz (1.6–13.2 GHz) whereas metal TTLPA and DLTTLPA provide bandwidth of 7.6 GHz (3.2–10.8 GHz) and 8.6 GHz (2.2–10.8 GHz), respectively. This comparison signifies that dielectric loading lowers the lower cut-off frequency by 1 GHz, i.e. from 3.2 GHz for metal TTLPA to 2.2 GHz for DLTTLPA. The higher value of relative permittivity of loaded material increases the effective length which reduces the operating frequency and, hence, enhances the bandwidth. Further, it is observed that the TTLPSA extends the operating frequency range towards both lower (1.6 GHz) and higher frequency (13.2 GHz) side. However, the geometrical dimensions of all TTLPAs are same that shows the proposed slot antenna has compact size compared to other antennas which are discussed. The enhancement in the bandwidth is obtained due to the proposed configuration of trapezoidal toothed log-periodic shaped slot designed on single-sided copper coated

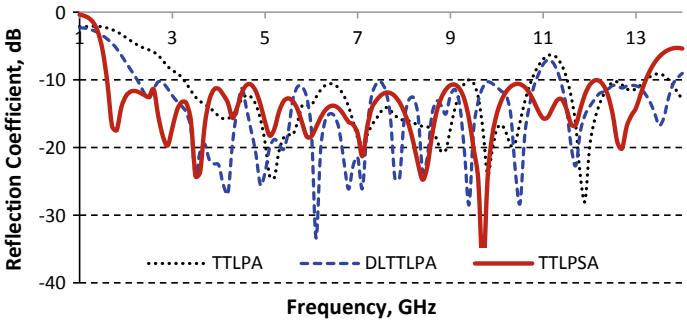

Fig. 3 Reflection coefficient-frequency characteristics of different configurations of TTLPAs

dielectric substrate and excellent impedance matching provided by tapered CPW feed. Further, it is observed that multiple resonances occur due to multiple radiating slots of different sizes.

4.2 Current Distribution on Antenna Surface

The mechanism of multiple resonances can be easily understood through the current distributions on the surface of the proposed antenna as shown in Fig. 4 at discrete frequencies of 1.6, 4, 6, 8, 10 and 12 GHz. At lowest frequency of 1.6 GHz, the outer slots of the antenna are responsible for resonance; whereas at higher frequency of 12 GHz, the smallest elements are responsible. The portions of the slot antenna responsible for resonance accommodate higher levels of current. As frequency increases, the higher level of surface current moves from larger to smaller slot type

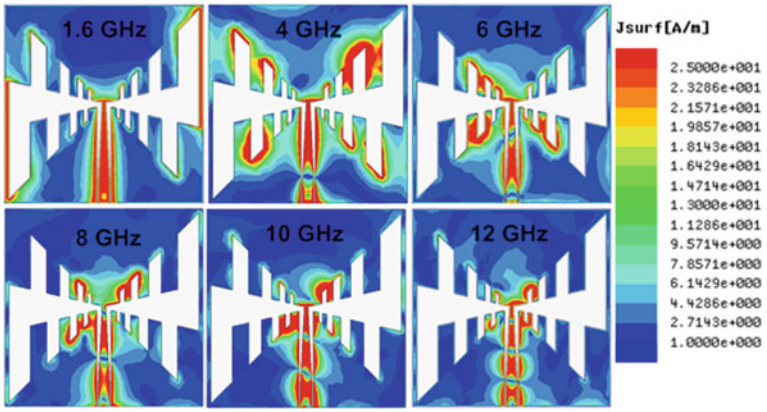

Fig. 4 Surface current distribution

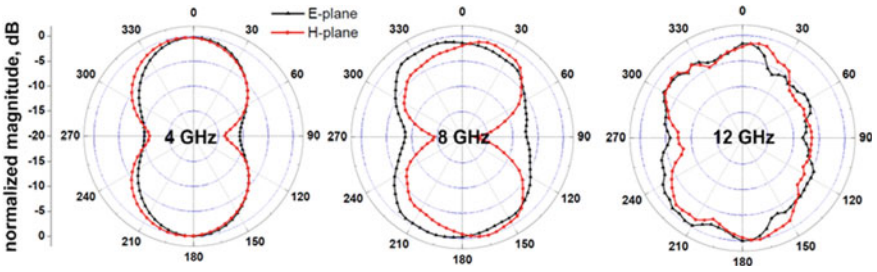

Fig. 5 Radiation patterns

tooth element of antenna. It is due to the inverse relation of frequency and wavelength and direct proportionality between wavelength and antenna slot size.

4.3 Radiation Pattern

To understand the radiation properties, simulated radiation pattern of the proposed TTLPSA in E- and H-planes at 4, 8 and 12 GHz is shown in Fig. 5. It can be observed from Fig. 5 that both E- and H-plane patterns are bidirectional in the shape of "dumb-bell" with maximum radiation along normal (along z-axis) to antenna plane (xy-plane). It is interesting to note that the patterns of the antenna are smoother as compared to TTLPA and DLTTLPA.

4.4 Gain and Efficiency

Figure 6 shows the simulated realized gain and radiation efficiency of proposed antenna in broadside direction. It can be observed that the realized gain values of the

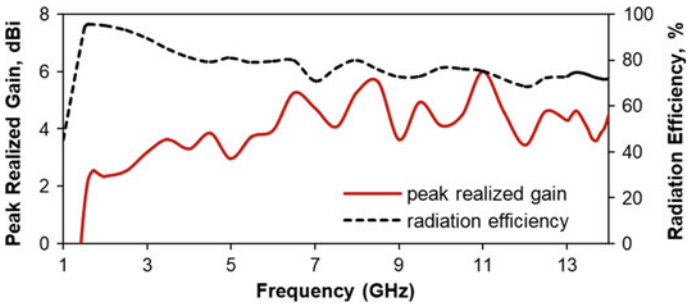

Fig. 6 Peak realized gain and total radiation efficiency

Table 1 Comparison of properties of different configurations of TTLPAs

Parameter	TTLPA [2]	DLTTLPA [3]	TTLPSA (present work)
Aperture size	48.9 × 48.9 mm^2	48.9 × 48.9 mm^2	50.9 × 50.9 mm^2
Impedance bandwidth (GHz)	3.2–10.8	2.2–10.8	1.6–13.2
Peak realized gain (dBi)	1.6–5.0	1.3–5.7	2–6.0
Geometry type	Non-planar	Non-planar	Planar
Balun used	Yes	Yes	No

antenna lie in the range 2 (at 1.6 GHz) − 6 dBi (at 11 GHz) with more than 70% radiation efficiency over its operating frequency range.

To briefly summarize the comparative study on enhanced bandwidth of different configurations of TTLPAs, the characteristics of all three antennas are compared in Table 1. It is investigated from Table 1 that proposed slot-based TTLPA, i.e. TTLPSA offers widest bandwidth, higher gain and stable radiation patterns among all antennas considered in this study. Also, it has compact size and planar structure without requirement of balun.

5 Conclusion

Three different non-planar and planar versions of TTLPAs are compared with respect to bandwidth. The dielectric loading on metal TTLPA improves impedance bandwidth or miniaturizes the antenna size at the cost of distorted radiation pattern, whereas the slot-based TTLPA enhances the bandwidth even more without distorting radiation pattern. A single-sided planar and compact wideband trapezoidal toothed log-periodic slot antenna is presented in this paper. A bandwidth of 11.6 GHz has been obtained due to multiple resonances of different slots of the proposed antenna. The proposed configuration of slot and modified CPW feed has made the antenna compact. The maximum length of the proposed slot antenna is only 0.27 λ instead of 0.5 λ at the lowest frequency of operation. Further it has been observed that as frequency increases the smaller slots become more active and longer slots less active. The radiation patterns of the antenna are very smooth and bidirectional along with reasonable realized gain and radiation efficiency over its wide operating frequency range. These paramount properties demonstrate that the proposed TTLPSA is extremely efficient over non-planar TTLPAs.

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DV-EXCCCII-Based Electronically Tunable Voltage Mode All-Pass Filter

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1 Introduction

Since few decades, active devices [1] are mostly used in analog signal processing. These are also used in filter, oscillator, instrumentation amplifier, inductance simulator and so on. These active blocks can be categorized as either voltage mode or current mode. In voltage mode, technique information is represented in the form of voltage, whereas in current mode, technique information is represented as current signal. Nowadays, current mode (CM) technique-based circuit design is preferred over voltage mode (VM) technique due to its inherent property of large bandwidth, high slew rate, simple circuitry, low power consumption, etc. Some of the most considered current mode active analog block is second generation current conveyor (CCII) [2–6], third generation current conveyor (CCIII) [7], current controlled current conveyor (CCCII) [8], differential voltage current conveyor (DVCC) [9–11], differential difference current conveyor (DDCC) [12–15], differential current conveyor (DCCII) [16], voltage differencing transconductance amplifier (VDTA) [17], modified current conveyor (MCCII) [18], dual-X second generation current conveyor (DXCCII) [19], fully differential second generation current conveyor (FDCCII) [20], current feedback operational amplifier (CFOA) [21], current feedback amplifier (CFA) [22], differential voltage extra-X current controlled current conveyor (DV-EXCCCII) [23], operational transresistance amplifier (OTRA) [24] and many more.

Analog filter employing these analog building blocks (ABB) enhances filter performance. Among all the filters, all-pass filter (APF) is one of the most important

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filter circuit. All-pass filter is needed where phase change between input and output signal is required while keeping its magnitude constant. APF is also known as phase shifter. In first order, APF phase varies from 0° to 180°. Several number of voltage mode APF using high-performance analog blocks are reported in the literature.

Proposed voltage mode APF is based on single DV-EXCCCII [25] and single capacitor. Two APF circuit can be designed from the same circuit topology only by changing position of input and output signals. Both filter circuits provide same transfer function for APF. No matching of components is required to realize filter response. Pole frequency of proposed APF can be varied by changing the bias current of DV-EXCCCII so presented filter is electronically tunable.

This paper is organized in the following manner: Introduction of proposed work is summarized in Sect. 1 of the paper. Proposed filter design and analysis is given in Sect. 2. Non-ideal analysis and sensitivities caused by these non-idealities are also discussed in this part of the paper. In Sect. 3, proposed work is compared with previously reported work. Proposed filter is verified through simulation in Sect. 4. In Sect. 5, conclusion of the work is given.

2 Proposed Filter Analysis

2.1 Circuit Implementation

The electrical symbol for DV-EXCCCII is represented in Fig. 1 and circuit implementation is given in Fig. 2.

Input and output signals relationship can be expressed by matrix given as follows.

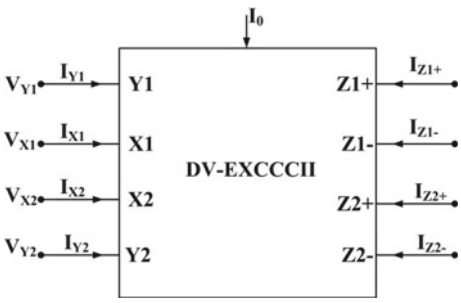

Fig. 1 Symbol of DV-EXCCCII

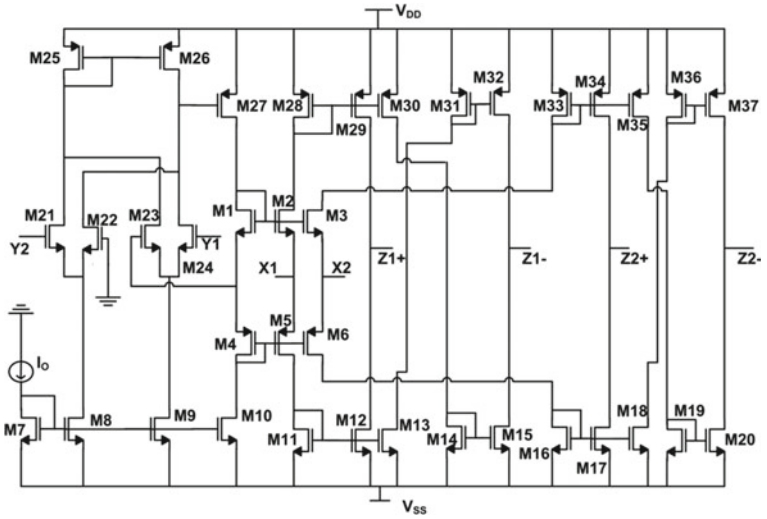

Fig. 2 CMOS representation of DV-EXCCCII

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_{X1} \\ V_{X2} \\ I_{Z1\pm} \\ I_{Z2\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & R_{X1} & 0 & 0 & 0 \\ 1 & -1 & 0 & R_{X2} & 0 & 0 \\ 0 & 0 & \pm 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_{X1} \\ I_{X2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix} \tag{1}$$

where R_{x1} and R_{x2} are internal resistance of current terminals X_1 and X_2, respectively. This resistance depends on the bias current I_0 and can be expressed as

$$R_{X1} = R_{X2} = R_X = \frac{1}{\sqrt{8\mu C_{0X}\left(\frac{W}{L}\right) I_o}} \tag{2}$$

Here, μ is mobility of the charge carrier, C_{ox} is oxide capacitance, W/L is aspect ratio and I_0 is bias current of active block.

This DV-EXCCCII has two current terminals and two voltage terminals. Current terminals ($X1$, $X2$) are low input terminals, and voltage terminals ($Y1$, $Y2$) are high input terminals. All the output terminals (Z) of the block are high output current terminals. Plus sign (+) shows that current of X and Z terminals is in same phase and minus sign (−) shows that they are in opposite phase. As application demands, many number of Z terminals can be created.

Two circuit designs for VM all-pass filter are proposed based on DV-EXCCCII, and they are represented in Fig. 3. Both the circuits can be obtained from same circuit

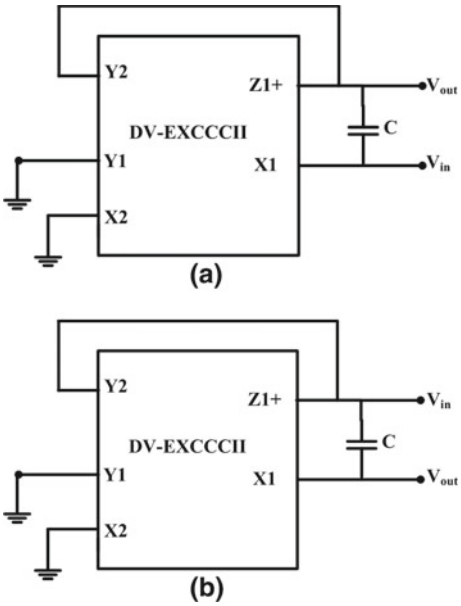

Fig. 3 Proposed filter configuration **a** circuit 1; **b** circuit 2

configuration only by interchanging input and output signals position. Single DV-EXCCCII and single capacitor are used in both circuits to realize the response for APF. Input voltage V_{in} is applied to obtain APF output at V_{out} terminal.

For both the circuits, same transfer function will be obtained and their expression can be given as

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{R_X C s - 1}{R_X C s + 1} \tag{3}$$

Above expression shows that matching of components is not needed to realize voltage mode all-pass filter transfer function for both circuit configurations.

Pole frequency can be given as

$$f_o = \frac{1}{2\pi R_X C} \tag{4}$$

Phase variation for both circuits can be expressed as

$$\phi = \pi - 2\tan^{-1}(\omega R_X C) \tag{5}$$

2.2 Non-ideal Behavior

Non-ideal behavior of DV-EXCCCII is explained here. Taking non-idealities of active block into consideration, port relationship of DV-EXCCCII is modified as

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_{X1} \\ V_{X2} \\ I_{Z1\pm} \\ I_{Z2\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0\ 0 \\ 0 & 0 & 0 & 0 & 0\ 0 \\ \beta_{11} & -\beta_{12} & R_{X1} & 0 & 0\ 0 \\ \beta_{21} & -\beta_{22} & 0 & R_{X2} & 0\ 0 \\ 0 & 0 & \pm\alpha_{1\pm} & 0 & 0\ 0 \\ 0 & 0 & 0 & \pm\alpha_{2\pm} & 0\ 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_{X1} \\ I_{X2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix} \tag{6}$$

where β_{11}, β_{12}, β_{21}, β_{22} are voltage transfer errors and $\alpha_{1\pm}$, $\alpha_{2\pm}$ are current transfer errors. Considering these, coefficient filter expression is modified as

For Circuit 1:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{R_X C s - \alpha_{1+}}{R_X C s + \beta_{12}\alpha_{1+}} \tag{7}$$

Modified pole frequency:

$$f_0 = \frac{\beta_{12}\alpha_{1+}}{2\pi R_X C} \tag{8}$$

Sensitivities due to non-ideality and passive components can be given as

$$S_C^{f_0} = S_{R_X}^{f_0} = -1; \quad S_{\beta_{12}}^{f_0} = S_{\alpha_{1+}}^{f_0} = 1; \tag{9}$$

$$S_{\alpha_{1-}}^{f_0} = S_{\alpha_{2+}}^{f_0} = S_{\alpha_{2-}}^{f_0} = S_{\beta_{11}}^{f_0} = S_{\beta_{21}}^{f_0} = S_{\beta_{22}}^{f_0} = 0 \tag{10}$$

It can be observed from (9) and (10) that sensitivities caused by non-idealities are low for circuit 1.

For Circuit 2:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{R_X C s - \beta_{12}}{R_X C s + 1} \tag{11}$$

Pole frequency:

$$f_0 = \frac{1}{2\pi R_X C} \tag{12}$$

Sensitivities due to non-ideality and passive components can be given as

$$S_C^{f_0} = S_{R_X}^{f_0} = -1 \tag{13}$$

$$\begin{aligned} f\, S_{\alpha_{1+}}^{f_0} &= S_{\alpha_{1-}}^{f_0} = S_{\alpha_{2+}}^{f_0} = S_{\alpha_{2-}}^{f_0} \\ &= S_{\beta_{11}}^{f_0} = S_{\beta_{12}}^{f_0} = S_{\beta_{21}}^{f_0} = S_{\beta_{22}}^{f_0} = 0 \end{aligned} \tag{14}$$

It can be observed from (13) and (14) that sensitivities caused by non-idealities are zero for circuit 2.

3 Comparative Research

Several high-performance analog building blocks (ABB) are reported in the literature. Using these high-performance active blocks, many number of first-order voltage mode APF are discussed previously. In this section of the paper, comparison of presented work with previously reported work is given. In [11], differential voltage current conveyor-based first-order VM APF is reported. In this paper, two DVCC, one resistor and one capacitor are used. Matching condition is not required to realize filter response. Electronic tunable property is absent in this filter. Differential difference current conveyor-based filter is reported in [13]. This filter also uses two DDCC and four passive components due to which circuit becomes complex. Matching is not required for filter realization, and filter is not electronically tunable. Filter given in [16, 18, 19] uses single active element but passive components used are large in number. In these filters, matching of components is required for APF realization. These are not electronically tunable filters. APF reported in [14] employed two DDCC and four passive components. Component matching is required in this filter. Single FDCCII-based APF is presented in [20]. It uses single resistor and single capacitor to obtain all-pass filter response without matching constraints. Single DDCC-based filter employed one resistor, and one capacitor is reported in [15] without matching of components. In many reported work, electronically tunable property is missing.

Proposed filter is resistor-less and uses one DV-EXCCCII and single capacitor. Matching of components is not needed to obtain all-pass response. This filter is electronically tunable so response can be changed with bias current of the DV-EXCCCII. Comparison of proposed filter with already available first-order VM all-pass filters is summarized in Table 1.

Table 1 Comparison of proposed filter with previously reported filter

References	Type of ABB	No. of ABB	No of resistor/capacitor	Matching constraints	Electronically tunable
[11]	DVCC+	2	1/1	No	No
[13]	DDCC+	2	3/1	No	No
[16]	DCCII	1	2/1	Yes	No
[18]	MCCII−	1	2/1	Yes	No
[19]	DXCCII	1	2/2	Yes	No
[14]	DDCC+	2	3/1	Yes	No
[20]	FDCCII	1	1/1	No	No
[15]	DDCC+	1	1/1	No	No
Proposed	DV-EXCCCII	1	0/1	No	Yes

4 Simulation Results

To prove the analyzed theory, proposed voltage mode first-order APF is simulated taking UMC 180 nm CMOS parameters through SPECTRE simulator of CADENCE VIRTUOSO. Supply voltage ± 0.9 V is used for simulation. Proposed APF is designed for $f_0 = 3.9$ MHz using $C = 50$ pF. Bias current of DV-EXCCCII is taken as $I_0 = 100$ μA, and for this value of bias current, intrinsic impedance of active block at current terminals $X1$ and $X2$ is found to be $R_{X1} = R_{X2} = 813$ Ω.

Gain and phase response of filter is presented in Fig. 4. It can be seen from response that magnitude is constant with frequency variation. Phase of proposed filter is changing from 180° to 0°.

Proposed filter is electronically tunable with internal current (I_0) of DV-EXCCCII. Electronic tunable property of the filter is represented in Fig. 5. Pole frequency of

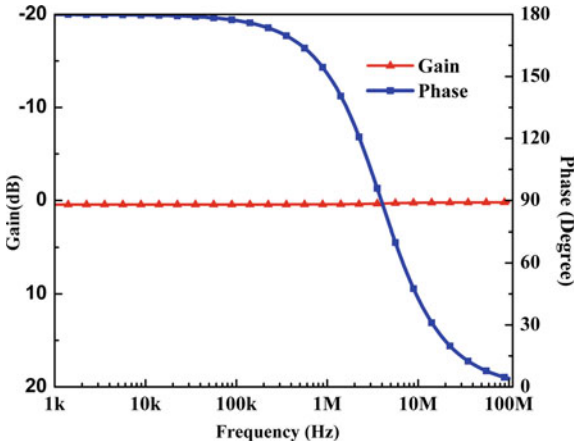

Fig. 4 Magnitude response for first-order APF

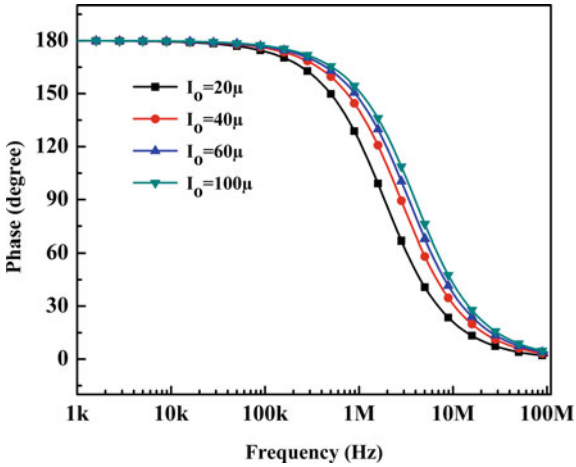

Fig. 5 Phase variation in APF at different I_0

both the filter circuit configurations can be varied with internal bias current of the DV-EXCCCII. To verify this property of the all-pass filter, phase response is shown at 20 µA, 40 µA, 60 µA and 100 µA of bias current and pole frequency is obtained as 1.7 MHz, 2.8 MHz, 3.2 MHz, 3.95 MHz, respectively.

Transient behavior of the proposed APF is shown in Fig. 6. To obtain time domain response, 50 mV peak-to-peak input voltage is applied at 3.9 MHz frequency. It can be observed from response that output voltage is 900 phase shifted with input at pole frequency which verifies theoretical analysis.

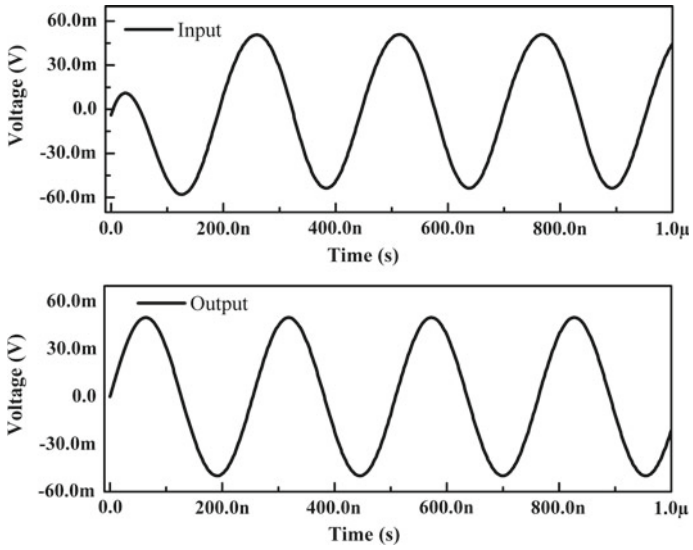

Fig. 6 Time domain input and output signal of APF

5 Conclusion

In this paper, resistor-less first-order voltage mode APF using DV-EXCCCII is reported. Two APF circuits can be obtained from same configuration just by interchanging the position of the input and output signal. Single DV-EXCCCII and single capacitor are employed to realize APF without requirement of matching of components. Filter has capability of electronic tuning so frequency can be varied by changing internal current (I_0) of DV-EXCCCII. Proposed topology is simulated by taking UMC 180 nm CMOS parameters with supply voltage of $\pm$ 0.9 V to verify theoretical analysis.

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Low-Power Shift Registers Using Fully Static Contention Free Single-Phase Clocked Flip Flop

Priti Tripathi, Anum Khan, and Subodh Wairya

1 Introduction

In recent years, the power reduction has become the major aim of the digital designer to design any circuits. Downgrading the supply voltage reduces the power consumption; therefore, operating the circuit at near threshold voltage (NTV) or sub-threshold voltage reduces static and dynamic power consumption. Single-phase clocked (SPC) flip flop has been operated at NTV for ultra-low power applications.

For operating the circuit at low voltage, robustness becomes the primary factor for designing ultra-low-power flip flops. For ultra-low-power designs, static operation is preferred because dynamic nodes are highly prone or sensitive to PVT variations at low voltages. Additionally, for low power flip flops, single-phase clocked operation increases power efficiency in the near threshold voltage region, hence the inverter chain (which provides clock signal that is complemented) can be removed [1]. With voltage scaling, contention path is also eliminated in ultra-low-power FF design. Single-phase clocked FF means all clock signals are transmitted on one wire which avoids toggling of internal clock inverters, which in turn also reduces power consumption. SPC FF is considered as one of the best technologies used in digital circuit due to its reduced transistor count as well as due to its robustness nature. Various researchers have done a great deal of work in this direction but mostly conventional SPC flip flop circuits are being presented as well as analyzed by most of them. 18 T SPC FF are still lesser explored part of the SPC FF, and this acted as the motivation for working in this direction. This paper delves into the designing of shift registers using this specific 18 T SPC FF, and various simulation performance analysis has been done.

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Lecture Notes in Electrical Engineering 777,
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1.1 Conventional True Single-Phase Clock (20 T) D Flip Flop

The above circuit represents the *D* FF circuit with 20 transistors operated on a single-clock signal [2]. On using this edge-triggered FF, the ripple through condition can be avoided to a large extent. Now consider the above circuit, the transistor $M19$ and $M20$ act as a reset input. When $D = 0$, CK $= 1$ then the wire from transistor $M2$–$M6$ remains floating and in this condition transistors $M7$, $M8$, $M9$, $M15$, $M17$ and $M18$ become poly biased. This operation when operated at NTV changes its behavior so power dissipation is significant. This circuit cannot be operated well at ultra-low voltages, and it is a dynamic operation means contention paths are observed in this circuit. Since this is the conventional form of flip flop, it is taken as comparison point for other implemented circuits so as to give an idea of performance improvement (Fig. 1).

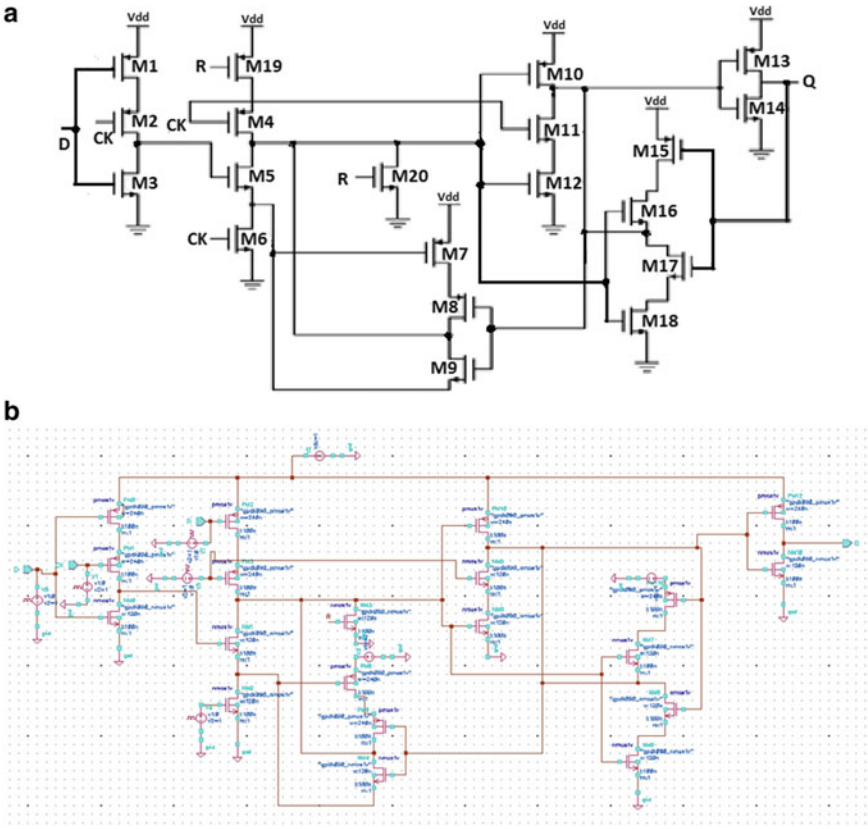


Fig. 1 **a** Circuit diagram of true single-phase clock. **b** Schematic of true single-phase clock

The circuit used in this paper is a master slave type which provides the better result at the triggering of the clock signal. The FF provides better power consumption and reduced gate delay and is used in various industrial applications.

Since this circuit gives unsatisfactory performance at low-supply voltage, therefore, contention free single-phase clocked flip flop having 18 transistors is explored [3]. The conventional and reference circuit are operated at different technology, and its PDP has been compared which shows that the reference circuit has better performance.

2 Contention Free Single-Phase Clocked Flip Flop

This circuit design claims to minimize the cell area and reduce the power consumption without affecting the circuit performance. The schematic of the 18 T SPC flip flop is shown in Fig. 2 [4]. At the clock edge, this D flip flop circuit transfers the input data

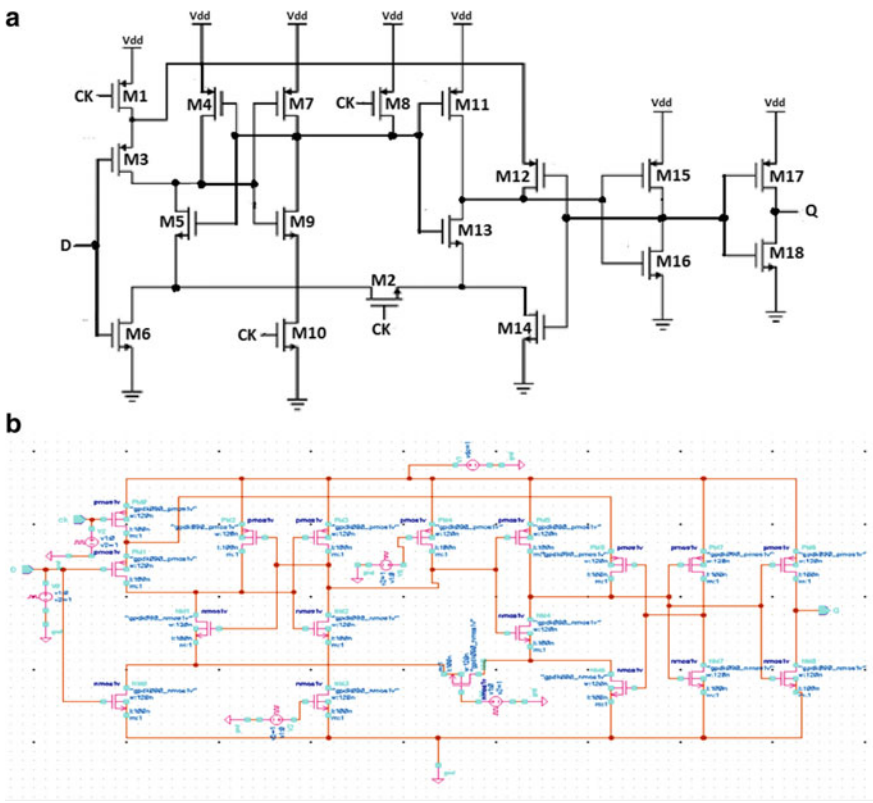


Fig. 2 **a** Circuit diagram of 18 T SPC flip flop [4]. **b** Schematic of 18 T SPC flip flop

to the output. As the clock edge arrives, the input does not change instantaneously but it considers the clock signal or data input just before the clock edge. Consider a case when CK = 0, $D = 0$.

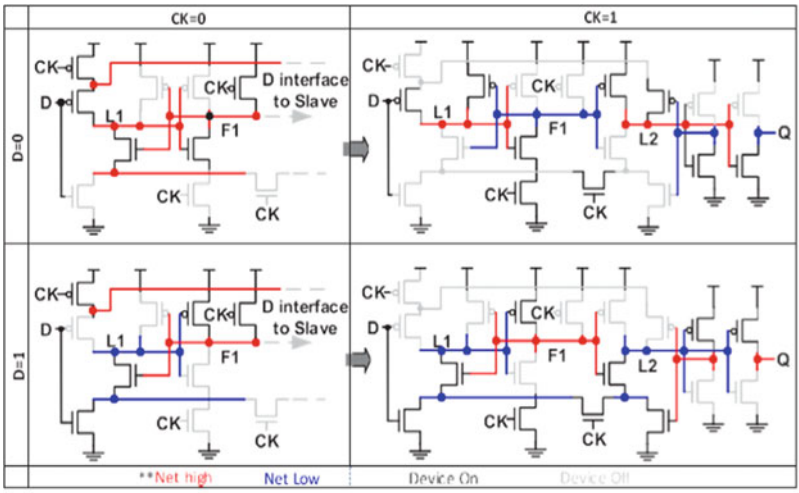
Clock signal transits from 1 to 0, therefore when CK becomes 0, then just before 0 it was 1, therefore $M1$ transistor will be OFF. Similarly, when D becomes 0, then just before 0 it was 1, therefore $M3$ transistor becomes ON. From this result, 0 is passed from $M3$ transistor to the $M7$ and $M9$ transistor which in turn makes $M7$ transistor ON and $M9$ transistor OFF. Then, 1 is passed to $M11$ and $M13$ transistor which is a inverter which produces the output as 1 at $M12$ transistor which makes this transistor OFF. Then, 0 is passed to $M15$ and $M16$ transistor which is also a inverter which produces the result 1. This 1 is fed to the $M17$ and $M18$ transistor which produces the output as 0. Therefore, input $D = 0$ and output $Q = 0$ which is the definition of D flip flop.

This 18 T SPC FF can be operated successfully at near threshold voltage region NTV [4], and it is seen that it becomes two times more efficient than conventional flip flops. Since only 18 T is used, therefore, area has also been reduced as compared to conventional FFs. When this flip flop is operated at NTV, it is a static operation; therefore, dynamic nodes or contention paths are eliminated. Also, the area is reduced in this circuit since numbers of transistors are reduced compared to the conventional SPC flip flop.

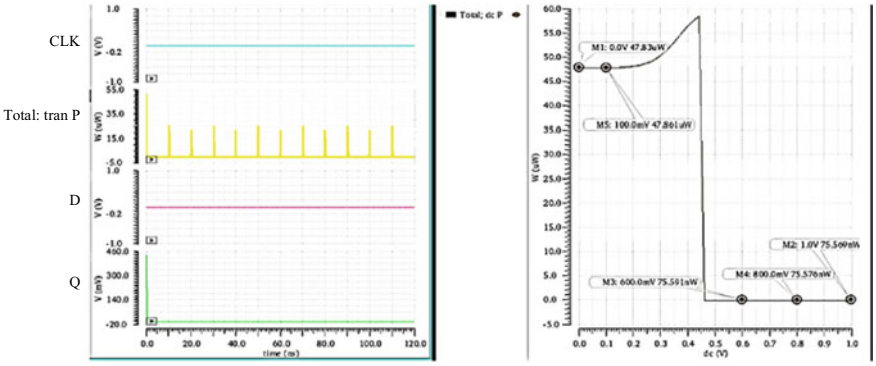
The clock (CK) signals are transmitted on single wire that is known as single-phase clocked (SPC). This avoids toggling of internal clock inverters which in turn reduces power dissipation. The schematic of this reported 18 T flip flop circuit has been implemented and verified on Cadence Virtuoso at 90, 65 nm as well as 45 nm. It is observed that the circuit's performance is unaffected by scaling. All the four states are free from dynamic nodes or contention paths. The circuit is observed at different D and CK states, and its dynamic power is compared. The circuit is also checked at NTV which have a significant impact on variability and performance [4–6]. Simulated outputs are depicted in Fig. 3.

The dynamic power dissipated for each state has been calculated. It is seen that as the no. of supply is increasing power dissipation is also increasing accordingly. It is clear from table that if $D = 0$ then there is a less difference between the power consumption but as the D input becomes high, and the power consumption also increases. The static power does not change at this point since the operation is performed at same voltage. The dynamic power changes, when data input is not applied then there is a minute difference in the dynamic power consumption. But as the data input is applied there is vast difference in the power consumption. The same can be inferred from Table 1. This means as the loading effect increases the power dissipation also increases.

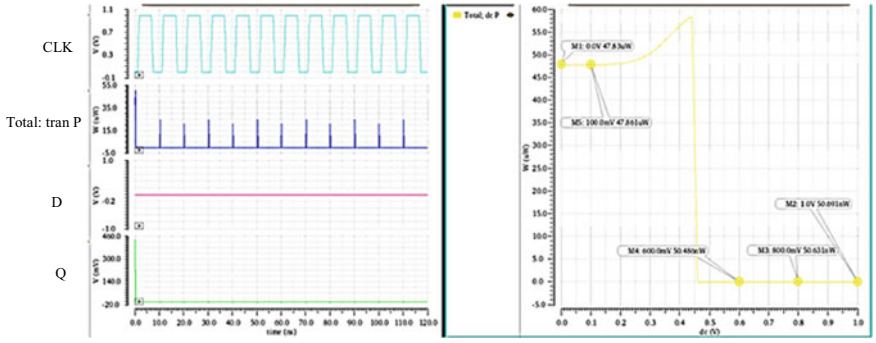
Influenced by this theory, digital designers have focused on developing the FF circuits with low power and reduced variability especially operating it in the low-voltage region [7–18]. It is evident from the results and simulation that this circuit provides low-power consumption along with reduced delay and hence is an efficient flip flop, and this provides motivation to design efficient shift registers based on contention free SPC flip flop.



(a) 18T SPC operation diagram at different CK and D states

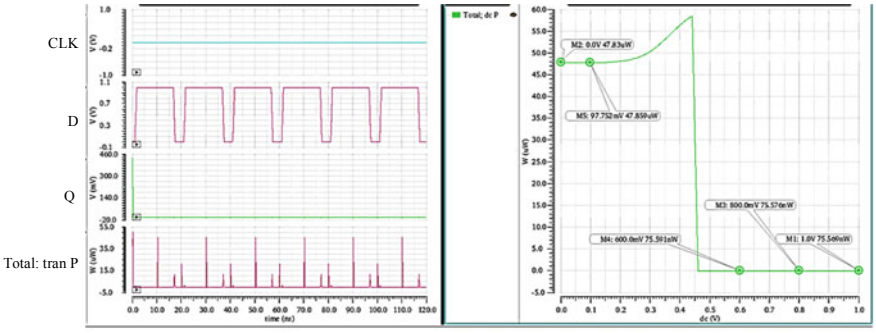


(b) Waveform of Dynamic Power at D=0, CK=0

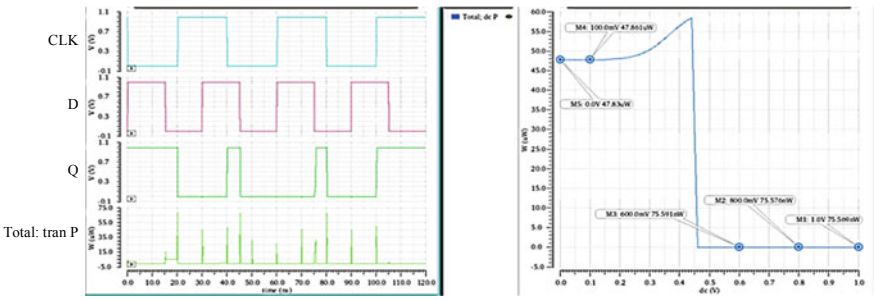


(c) Waveform of Dynamic Power at D=0, CK=1

Fig. 3 Simulated waveform of 18 T single-phase clock D flip flop at different states. **a** 18 T SPC operation diagram at different CK and *D* states [4]. **b** Waveform of dynamic power at $D = 0$, CK $= 0$. **c** Waveform of dynamic power at $D = 0$, CK $= 1$. **d** Waveform of dynamic power at $D = 1$, CK $= 0$. **e** Waveform of dynamic power at $D = 1$ and CK $= 1$



(d) Waveform of Dynamic Power at D=1, CK=0



(e) Waveform of Dynamic Power at D=1 and CK=1

Fig. 3 (continued)

Table 1 Analysis of dynamic power (μW) at different D and CK inputs

Input	CK = 0	CK = 1
$D = 0$	17.37	17.39
$D = 1$	25.59	42.90

3 Proposed 4-bit Shift Registers Topologies

Registers are used to store the data. Number of bits stored is equal to number of flip flops used. Each flip flop can be used to store bits. By cascading n number of flip flops, one can store n bits of information. Shift registers are used to store the data and can also be used to shift the data from MSB to LSB (right shift) or from LSB to MSB (left shift). By cascading n number of flip flops registers can be implemented serially. Various shift registers can be implemented depending upon the arrangement of input and output of flip flops. With the less number of transistors and lesser load, the shift registers perform well [7]. Shift registers are sequential circuits which are synchronous that is they use same clock signal to produce the output. Serial in serial out (SISO) shift register, parallel in parallel out (PIPO) shift register and serial in parallel out (SIPO) shift register topologies have been proposed using 18 T SPC flip flop.

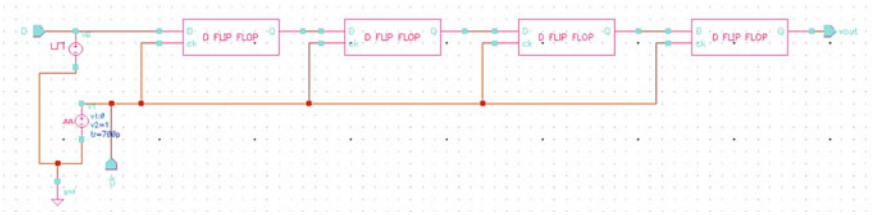


Fig. 4 Schematic of 4 bit SISO shift register

Table 2 Truth table of SISO shift register

CLK	I/P bit	FF1	FF2	FF3	FF4 = Q
0	1	1	0	1	0
1	0	0	1	0	1
2	1	1	0	1	0
3	0	0	1	0	1

3.1 Proposed Serial in Serial Out (SISO) Shift Register Based on 18 T SPC Flip Flop

The input given to this type of shift register is in serial manner, i.e., one bit after the other sequentially by a single data line and serial output is obtained. Because only one output is there, a serial pattern is formed when the data exits the shift register one bit at a time, therefore, the name is serial-in-serial-out shift register. The logic schematic of SISO shift register is shown in Fig. 4.

All the flip flops are connected in series, and each flip flop is synchronous to the other as each flip flop is running on the same clock signal. As it is clear from the logic diagram that input bit 1010 is fed serially from right so the shift register will shift (move) the data bit to left. The truth table of SISO shift register is shown in Table 2.

3.2 Proposed Parallel in Parallel Out (PIPO) Shift Register Based on 18 T SPC Flip Flop

The shift register which takes parallel input as well as it produces parallel output, such register is called as PIPO shift register. In this type of shift register, there is no interconnection between the flip flops because data is not shifted serially. Data is given to each flip flop input separately, and similarly, output is obtained from each flip flop separately. The logic circuit of PIPO shift register is depicted in Fig. 5.

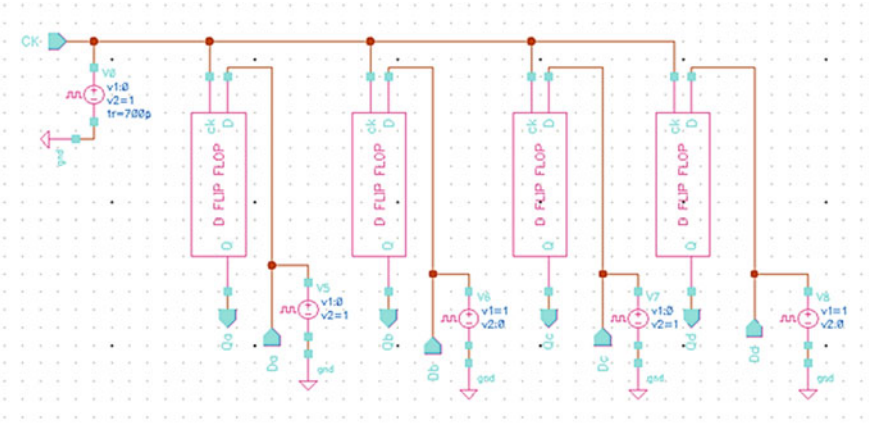


Fig. 5 Schematic of PIPO shift register

Table 3 Truth table of PIPO Shift register

CLK	*D*1	*Q*1	*D*2	*Q*2	*D*3	*Q*3	*D*4	*Q*4
0	0	0	0	0	1	1	1	1
1	1	1	1	1	1	1	0	0
2	1	1	0	0	1	1	0	0
3	0	0	1	1	0	0	1	1

All the flip flops are operated at same clock but they are not interconnected with each other. Each flip flop individually is provided with the data input, and similarly, output is obtained individually from each flip flop. The truth table of PIPO Shift register is shown in Table 3.

3.3 Proposed Serial in Parallel Out (SIPO) Shift Register Based on 18 T SPC FF

The shift register which has serial data input, i.e., one bit after the other by a single-data line and generates output in parallel, such type of shift register is called as SIPO shift register. The output of the first flip flop is given as input to the second flip flop and so on. The flip flops are synchronous to each other because each flip flop is working on the same clock signal. The logic circuit of SIPO shift register is shown in Fig. 6.

All the flip flops are operated at same clock frequency, and they are interconnected with each other. The data is applied serially, and output is obtained in parallel. The

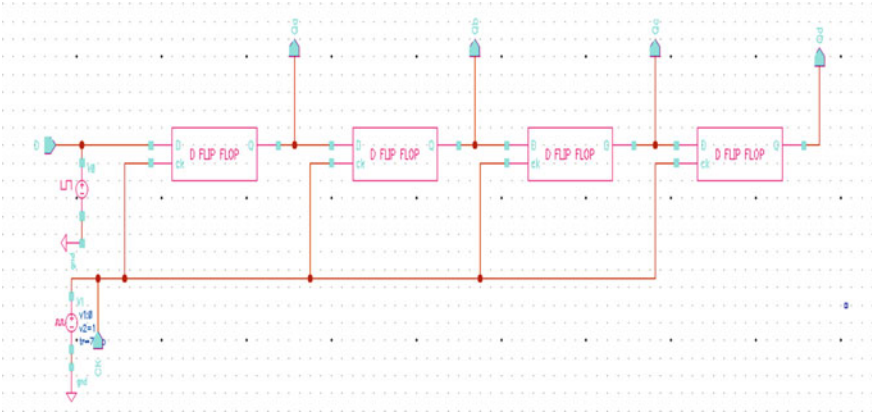


Fig. 6 Schematic of 4 bit SIPO shift register

Table 4 Truth table of SIPO shift register

CLK	I/P bit	FF1	FF2	FF3	FF4
0	0	0	0	0	1
1	1	1	0	0	0
2	0	0	1	0	0
3	0	0	0	1	0

output of first flip flop acts as input to the second flip flop and so on. The truth table of SIPO shift register is shown in Table 4.

All the aforementioned 4 bit shift registers are implemented using both conventional 20 T D flip flop and 18 T SPC flip flop (reference circuit). Their performances in terms of power consumed, delay and PDP are analyzed and compared for 1 V supply voltage.

4 Simulation Results Analysis

The reference circuit, i.e., contention free 18 T SPC flip flop has been implemented on Cadence Virtuoso EDA tool at 1 V supply and 100 MHz clock. The output waveforms obtained by the circuit is shown in Fig. 7. The performance parameters viz power, delay and PDP have been analyzed for each technology, and a comparison is done between reference circuit and conventional circuit for the power supply of 1 V as shown in Table 5. The Cadence Virtuoso was used for schematic circuit.

Reference circuit is more efficient than conventional circuit. Power dissipation is reduced on working at NTV region. Power dissipation increases as the technology is increased. Simulation result shown that overall PDP is reduced. It is evident that at

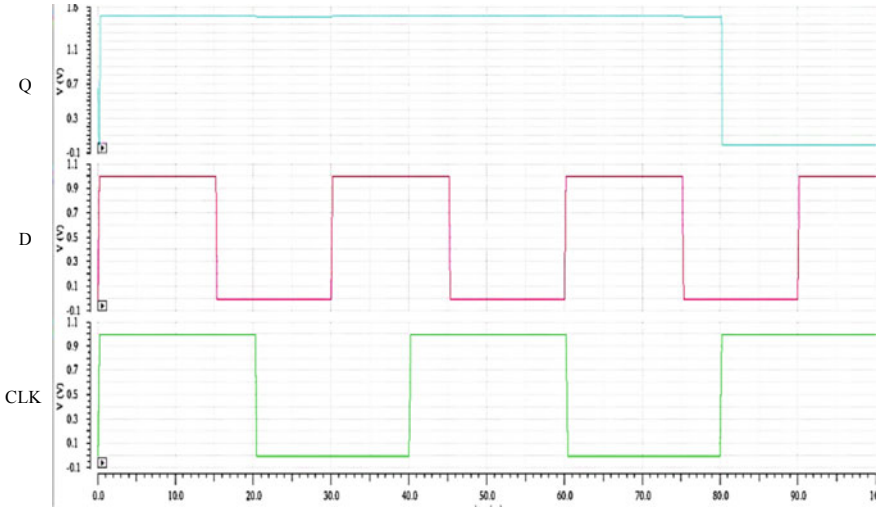


Fig. 7 Simulation waveform of 18 T SPC D flips flop circuit

Table 5 Comparative table for power, delay and PDP with technology scaling (nm)

Technology (nm)	Power/delay/PDP	18 T SPC circuit	Conventional circuit
45	Power dissipation (uW)	30.5	48.7
	Delay (psec)	68.1	80.34
	PDP (fWs)	2.077	3.9
65	Power Dissipation (uW)	71.45	98.65
	Delay (psec)	42.04	67.76
	PDP (fWs)	3.003	6.68
90	Power dissipation (uW)	89.40	119.34
	Delay (psec)	39.62	47.65
	PDP (fWs)	3.54	5.68

each implemented technology node the contention free SPC flip flop produces less power dissipation and delay.

The proposed shift registers topologies have been design using the 18 T SPC flip flop. The simulated transient response of the proposed circuits is shown in Figs. 8, 9 and 10 which verifies the proper functioning and working of the designed circuit of SISO shift register, PIPO shift register and PISO shift register, respectively. Tables 6 and 7 summarize the performance parameters obtained for shift registers topologies.

To establish the robustness of implemented shift registers, the power dissipation and delay are calculated at different supply voltages including near threshold voltage. The power dissipation of the proposed shift registers has been calculated for different supply voltages in the range of 0.6–1.2 V and has been plotted and compared with

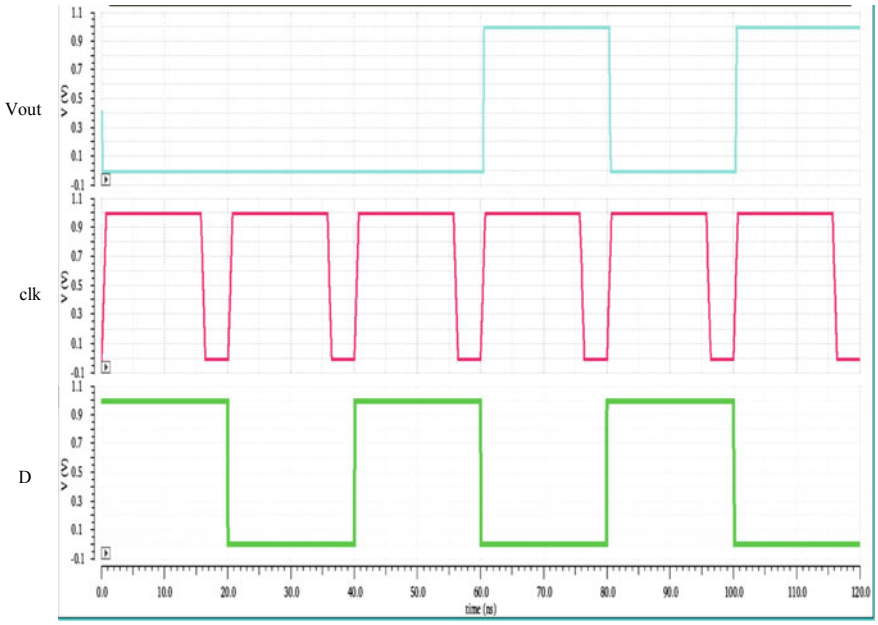


Fig. 8 Simulation waveform of proposed SISO shift register circuit

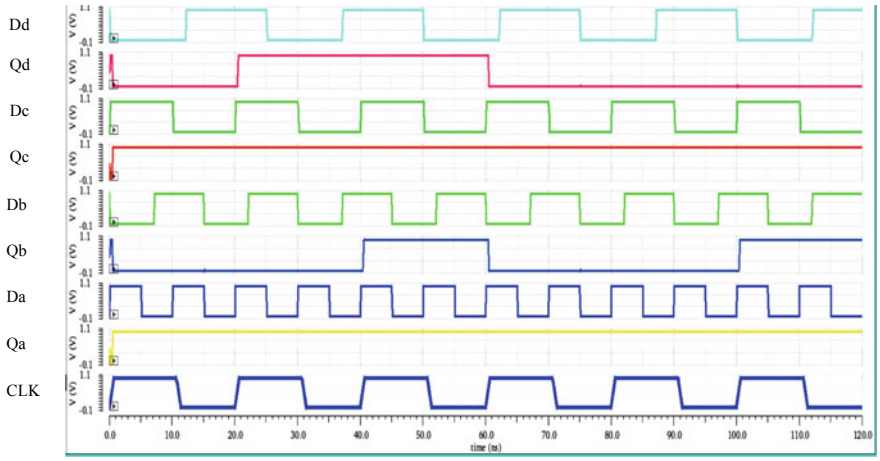


Fig. 9 Simulation waveform of proposed PIPO shift register circuit

its conventional circuit. As the supply voltage is increasing, the power dissipation also increases as shown in Fig. 11a–c.

The delay of the proposed shift registers has been calculated for different supply voltages in the range of 0.6–1.2 V and has been plotted and compared with its

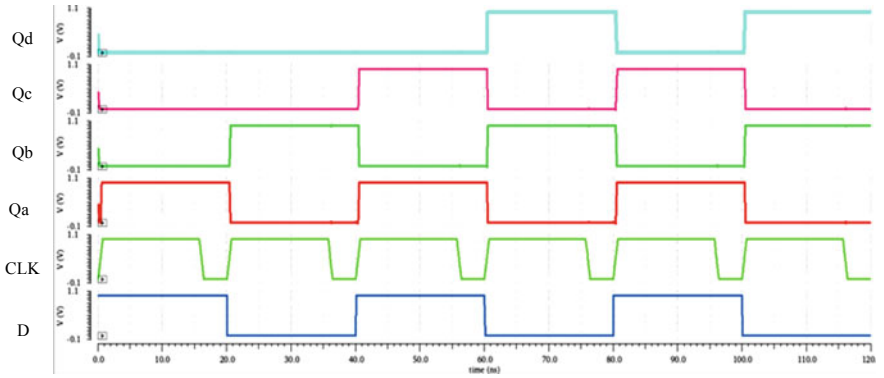


Fig. 10 Simulation waveform of proposed SIPO shift register circuit

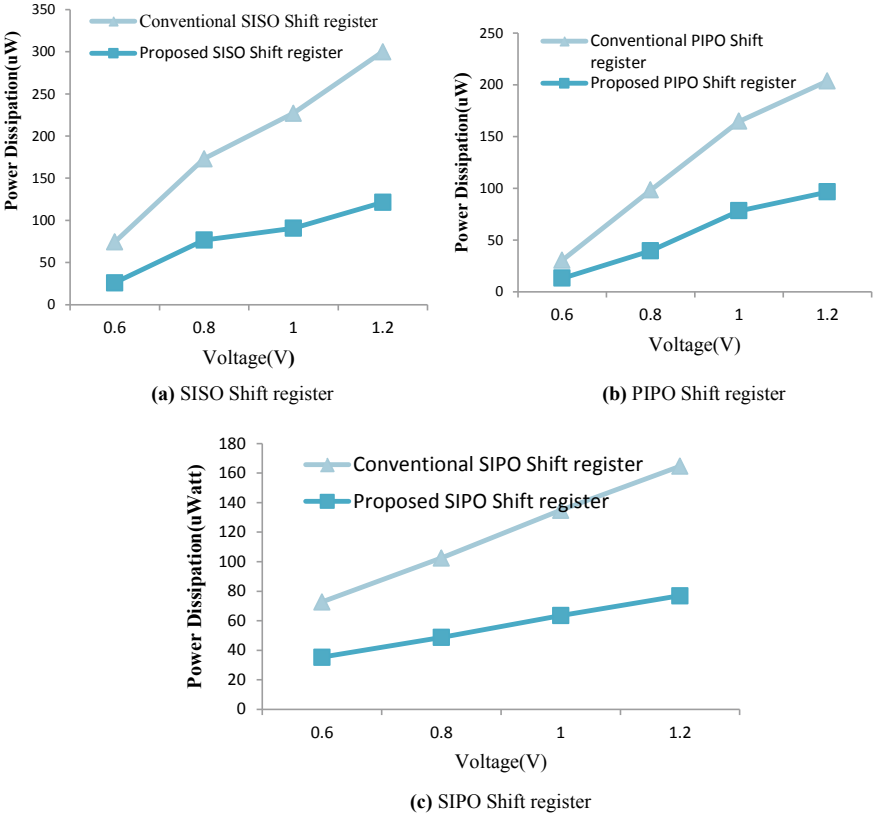
Table 6 Comparative table for power dissipation (μW) of shift registers at various voltage (V)

Voltage (V)	Power in proposed shift registers (μW)			Power in conventional shift registers (μW)		
	SISO	PIPO	SIPO	SISO	PIPO	SIPO
0.6	26.02	13.16	35.29	48.45	17.38	37.47
0.8	76.68	39.63	48.76	96.47	58.76	53.76
1.0	90.76	78.27	63.48	136.37	86.48	71.37
1.2	121.48	96.48	76.97	178.45	107.16	87.68

Table 7 Comparative table for delay (ns) of shift registers at various voltage (V)

Voltage (V)	Delay in proposed shift register (ns)			Delay in conventional shift register (ns)		
	SISO	P IPO	SIPO	SISO	PIPO	SIPO
0.6	20.45	24.43	40.15	32.76	30.84	47.26
0.8	17.68	18.63	29.76	28.36	23.86	39.29
1.0	12.47	12.47	20.15	21.64	17.13	26.02
1.2	7.36	8.78	12.69	16.46	14.89	16.23

conventional circuits. As the supply voltage is increased, the delay is increasing as shown in Fig. 12a–c. The proposed shift registers perform better shift registers implemented using conventional flip flop even at NTV. Overall PDP is also found to be improved.



(a) SISO Shift register

(b) PIPO Shift register

(c) SIPO Shift register

Fig. 11 **a**–c Comparison of power dissipation with supply voltage variations

5 Layout Design

The Cadence Virtuoso XL layout editor software has been used for layout designing. The compact layout area is calculated as 89.249 μm^2 of the reference 18T SPC flip flop which has been implemented on 45 nm technology and is shown in Fig. 13. The layout area is calculated as 1131.458 μm^2 of the proposed PIPO shift register which has been implemented on 45 nm technology and is shown in Fig. 14.

6 Conclusion

This paper explores the application of contention free single-phase clocked flip flop in shift registers. The flip flop structure which has been presented in the paper is

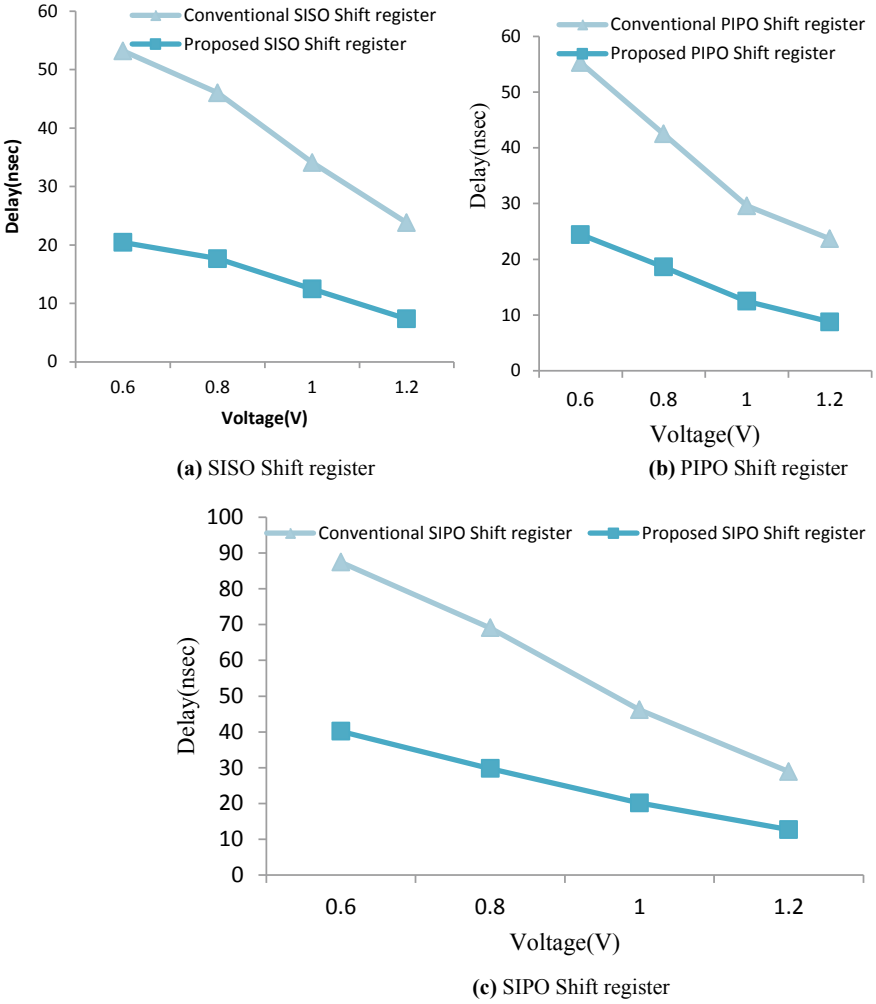


Fig. 12 **a–c** Comparison of delay with supply voltage variations

quite simple and robust in nature and can be used to reduce the energy consumption as well as power dissipation of modern digital VLSI design and application in nanotechnology. The 18 T SPC flip flop (reference circuit) is compared with the conventional flip flop topologies circuits on the basis of power dissipation, delay, PDP and transistor count. Simulation results reveal that for all the supply voltages variation the 18 T SPC FF has better power consumption due to single-phase clocked flip flop as well as due to the better performance at NTV region. This reference circuit has been verified at different supply voltages and different technologies, i.e., at 45, 65 and 90 nm on Cadence Virtuoso tool.

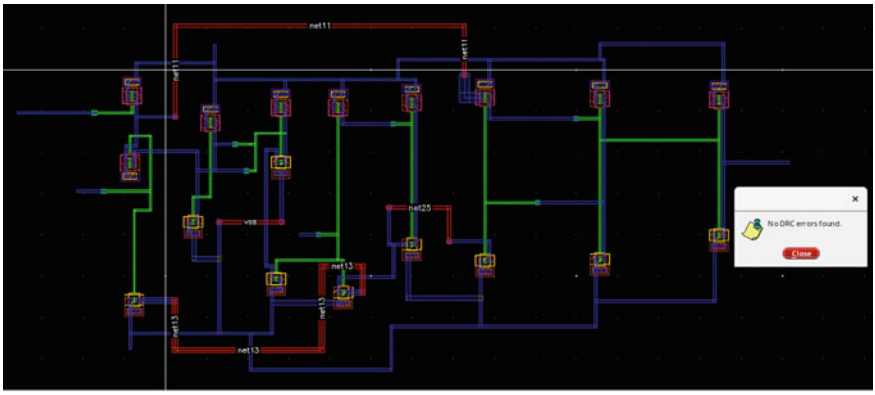


Fig. 13 Simulation layout of 18 T SPC flip flop

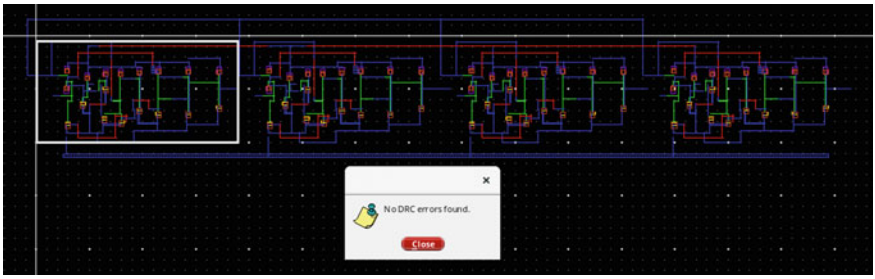


Fig. 14 Simulation layout of proposed PIPO shift register

Three 4-bit shift registers SISO, PIPO and SIPO topologies using 18 T SPC flip flop have been designed, and the simulation performance parameters are compared with its conventional counterpart. It has been observed that the overall power consumption has been reduced (28–38)%. Its robustness has been established by observing the effects of supply voltage variation on power and delay. The simulations are done on Cadence Virtuoso tool using 45 nm technology at 1 V using 100 MHz clock. By the results, it can be concluded that 18 T SPC flip flop provides significant improvement in the implemented shift registers thereby opening the avenues for several low-power applications.

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FPGA-Based Display Driver Design with Remote Terminal Unit (RTU) Support Using MODBUS

Y. M. Ashoka Raja, Prashant K. Shah, and Anand D. Darji

1 Introduction

In recent years, data display devices are becoming more and more prevalent, and remote data displacing is in booming demand. Remote display is a kind of display system where the display under consideration is used to show the information/data remotely. To update display with new message or data no need to reprogram, it will be updated as soon as memory is updated with new data. These remote display devices play critical role in many sectors of the industrial applications. Remote data accessibility is in high demand in several industries [1]. Also, these remote display devices are primary thing in many institute, organisation and public utility places [2]. These remote displays can be used to convey important information at large group of people at a time.

The conventional wired display boards are controlled by MCUs. To change the information being displayed, we need to change the MCUs program again and again and size of the display is also limited. With the recent advancements of the technology, it is possible to fix these issues. In the proposed work, it aims to design, development and implementation of the FPGA based VGA display driver for both image and font display capability. This device is also enabled to receive and update the display with the new data sent from remote device. The proposed work used implementation of master and slave protocol to establish remote terminal support. This proposed work demonstrates designing of PL + PS based remote displaying system with MODBUS RTU support.

MODBUS over serial line protocol; is widely adapted, loyalty free, openly published protocol, which is developed for industrial applications as it provides reliable and easy communication between the devices connected in the same network [3]. Hence, the proposed work aims bring in this MODBUS protocol as an RTU in

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https://doi.org/10.1007/978-981-16-2761-3_45

to the loop. VGA standard is the widely used, common interface such as embedded systems, automobile infotainment system, ATMs, security system or video players. Therefore, VGA monitor controller that could be the logic circuit to regulate the VGA interface, may be simply realised using FPGA technology with a low cost and high flexibility [4].

2 Related Work

In Ref. [5], author talks about the embedded web server-based remote data monitoring and controlling. The data to be displayed on the display depends upon the data updated by the remote device on the server. Web server-based systems are backboned by the support of internet service provider. In the implementation of [5], it uses ZYNQ 7000 APSOC board, it also uses VGA standard to drive the display. Remote data acquisition and accessibility are in high demand in industries. Human beings are replaced by sensing devices that will acquire data and send the data back to the base station remotely. At base station, it is possible to monitor data remote and take action accordingly. The implementation web server-based remote display in [1] includes the master and slave implementation. In implementation, master device is placed in the main office or at the base station of the industry which has display device. It uses ARM based Raspberry pi, which includes the porting Linux OS into master device. Slave devices can be placed in any one or more units of industry. The number of slave units used for the implementation depends on the number of units in the industry which requires remote monitoring. This slave is based on PIC microcontroller. In Refs. [2, 6, 7] talks about MCU-based remote display systems based on the GSM. In the GSM-based display system, it has GSM interfaced master device which can send data to the multiple slaves, each slave has GSM modules to receive the data, decode and send to display. This microcontroller with GSM-based remote display system can be used at the colleges and universities for displaying day-to-day information at regular intervals, besides this can also be used at other public places like schools, railway stations, gardens, etc. With the implementation and use of various AT commands, it is possible to control the data onto the display device. This technology is used to monitor/update the remote display devices and hence, for conveying the information through a data sent from authenticated master device. In these MCU based system, to increase the display size more numbers of drivers are needed. To make the display multilingual, the MCU based system becomes more completed as it requires many encoding and decoding technique [2]. References [8, 9] talk about the FPGA-based VGA display driver implementation using hardware description language. In [10] also author has taken the implementation of the FPGA-based VGA display design as a part of the work, which talks about principle of VGA display control and implementation of the same using Verilog. These papers describe the VGA timing analysis for different resolutions, algorithm to generate VGA signals, realisation of VGA using FPGA, timing parameters, etc., were discussed. The other

works of note can also be found in Refs. [3, 11, 12] which talks about the design and development of MODBUS-based communication system.

3 Proposed System

The proposed system includes the design and implementation of the master and slave configuration. The design, development and implementation of slave device require the interfacing of major peripheral viz. VGA driver interface, memory interfaces (VGA buffer memory and secondary memory) and serial communication interfaces. All these peripherals are implemented and tested as standalone system before doing integrated system testing. The master device function is to send the encoded RTU frames which carries information such as salve ID, function code, actual data and checksum for the entire message. This actual data of the frame carries the information related to display update data. Figure 1 shows the proposed system block design, and Fig. 2 shows the typical MODBUS RTU frame.

ZYBO and ZED boards are largely used as prototyping boards due to its speed, feature rich and ready to use nature. In the proposed work, ZYBO development board from digilent is used as master device and ZED board is used as slave device. Use of the Modbus protocol allows to connect up to 247 slaves (with RS 485), where each slave is addressed with its unique address [13, 14]. The proposed system uses RS 232 as physical interface for MODBUS protocol implementation. Each slave device will have implemented slave part of Modbus protocol, which includes decoding of frames and performing successive operation based on the received function code.

With FPGA, the display data will be handled by the hardware and eventually it reduces the software overhead and also the hardware is reconfigurable, this will be the

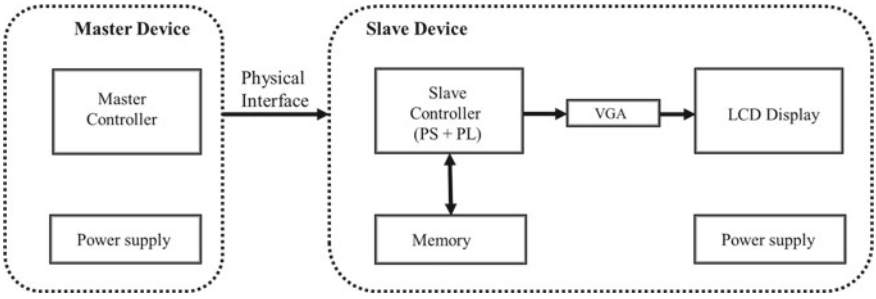

Fig. 1 Proposed system block diagram

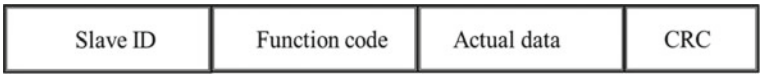

Fig. 2 Typical RTU frame

added advantage which makes it possible to quickly change the display for any others, with redesigned drivers for the newly selected display. Requirement of memory for the chosen display (for buffering and secondary storage of data) is provided through memory interfaces. The required driver for the VGA protocol will be implemented in the FPGA with its timing analysis corresponding to the selected screen resolution (640 × 480). For the secondary storage of the data, SD card will be interfaced to the system device through SD mode.

3.1 Memory Interfaces

The implementation of the proposed work requires two types of memories viz. temporary memory such as RAM for VGA data buffering and secondary memory such as SD card or EEPROM to store images or fonts.

VGA Buffer memory

Since the proposed display driver design is VGA based system, it requires the buffer memory to keep the data ready before sending it to the display, which should also satisfy persistence of human eyes. The amount of RAM required by the VGA display is directly proportional to the chosen screen resolution. Below tabulated, Table 1 shows the RAM requirement analysis for different resolutions (resolution indicates the total number of pixels in the screen in Horizontal pixel × Vertical pixels format) and colour depths.

Block RAM available in the FPGA can be configured to implement the required VGA display buffer memory. ZED board can offer around 610 kBytes of Block RAM. With reduced size of 256 × 256 pixels, it is possible to test the VGA display having 16 bits/pixel colour depth. In order to implement the Block RAM, BMG IP

Table 1 RAM requirement analysis for different resolutions and colour depths

Display	Colour depth and memory requirement (in bytes)				
Resolution	1 bits/pixel (Mono)	2 bits/pixel (4 shades)	4 bits/pixel (16 shades)	8 bits/pixel (256 colours)	16 bits/pixel (65 K colours)
1280 × 1024	16,840	327,680	655,360	1,310,720	2,621,440
1280 × 800	128,000	256,000	512,000	1,024,000	2,048,000
1024 × 768	98,304	196,608	393,216	786,432	1,572,864
800 × 600	60,000	120,000	240,000	480,000	960,000
800 × 480	48,000	96,000	192,000	384,000	768,000
640 × 480	38,400	76,800	153,600	307,200	614,400
480 × 272	16,320	32,640	65,280	130,560	261,120
320 × 240	9,600	19,200	38,400	76,800	153,600
128 × 64	1,024	2,048	4,096	8,192	16,384

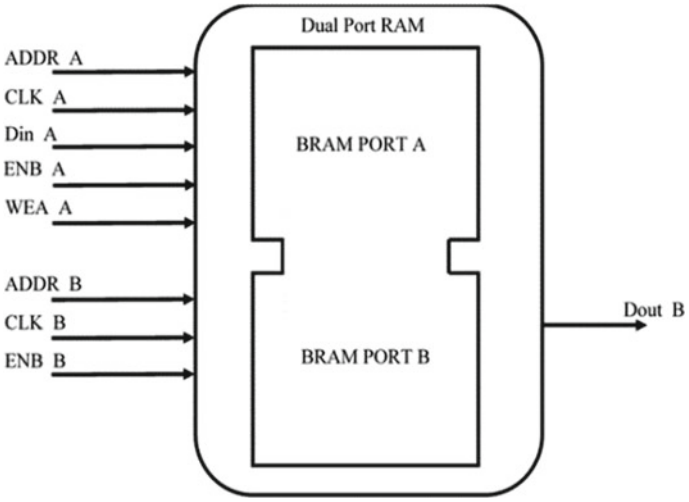

Fig. 3 Dual port RAM with IO ports

core (from Xilinx) is used in dual port configuration. Figure 3 shows the dual port RAM IO configuration for the block RAM. Port A is used for the write operation, and port B is used for the read operation. Both port share common clock and other pins of both the ports were controlled by PS section.

SD memory interfacing with BRAM integration

In the proposed system, the secondary memory such as SD card is required to store the data such as images, font table, etc. Since the system has RTU support, based on the data received, the slave can decode the data and using the available data in the secondary memory, it can send appropriate data to display. SD card is an ultra-small flash memory card designed to provide high-capacity memory in a small size. The system under consideration is tested with up to 8 GB of memory with class 10 memory card. The micro SD card supports two types of communication protocols, i.e. SD and SPI bus mode. With ZED board, SD card is interfaced in SD mode, which also gives better performance than the SPI mode.

In order to implement proposed work, it mainly requires SD card read operation. Serial terminal is used for debugging purpose. The read data will be sent to the block RAM using AXI interface. Figure 4 shows the integrated flow chart for the SD card with block RAM design. This design is tested as standalone design before using in the final integration.

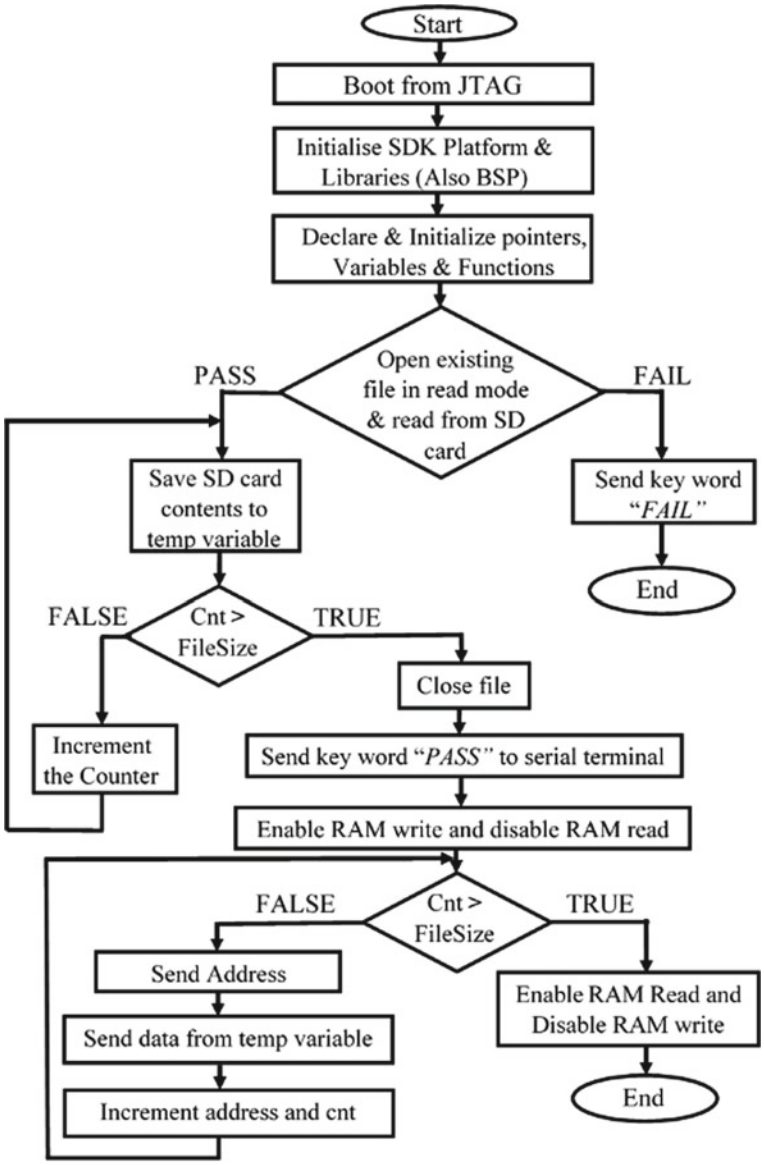

Fig. 4 Flow chart for integration of block RAM and SD card memory

3.2 Display Controller Design

VGA can provide an easy methodology to attach a system with a monitor for showing information or images, or even to interact with the system by the user. VGA monitor controller that could be the logic circuit to regulate the VGA interface may be simply

realised using FPGA technology with a low cost and high flexibility using hardware description language [4, 9]. Note that because of Block RAM limitation the screen size is reduced to 256 × 256 size, so that it can be implemented and tested on FPGA with lower BRAM capacities. To save 256 × 256-pixel image with 16 bits/pixel, we need 132Kbytes of BRAM (256 * 256 * 2).

For the current design, VGA timing is selected to be 640 × 480. For the vertical sync design, total 521 vertical pixels are considered (In a line). Among them 480 pixels corresponds to the active area, 10 and 29 pixels correspond to front and back pouch, respectively. Two pixels are dedicated to the VS pulse width. For the horizontal sync design, total 800 horizontal pixels are considered. Among them 640 pixels corresponds to the active area, 16 and 48 pixels correspond to front and back pouch, respectively. 96 pixels are dedicated to the HS pulse width. This design uses 25 MHz clock with 60 Hz refresh frequency.

Display Image

The usage of the images to convey information by display devices, language will not be a barrier. Also human brain can process images much more speeder than the reading the text. Thus, images are more powerful to convey crucial information to the people of any kind, literate or illiterate, and there will be no barrier of language. In order to implement the VGA controller on FPGA, three modules were designed and integrated with block RAM. First module is designed to generate all the required VGA timings viz. Horizontal Count (HC), Vertical Count (VC), Horizontal Sync Pulse (HS) and Vertical Sync Pulse (VS), which will have the inputs viz. pixel clock and reset. The second module is designed to generate all the required address for the Block RAM module, and these addresses are generated based on the inputs from module one using HC and VC. The third module is the main module which will send all the required outputs to drive the VGA display, i.e. HS, VS and RGB colours.

Display Font

Displaying text is one of the add-on functionality in the display driver design. In order to implement font displaying capability in the VGA display, font table has been developed which will be stored as look up table in the FPGA LUT memory. The design goals to display ASCII text character on the VGA display.

Figure 5 shows the typical example for the bit map generated for the ASCII font B. Similarly for each character 32 × 16 bit mapping is created. Hence, with 32 pixels wide and 16-pixel height, it will give total of 600-character location, i.e. 480 pixels divided by 16 rows per character gives total 30 lines and 640 pixels divided by 32 columns per character gives 20 lines, hence 30 × 20 = 600 locations (with small sized font in loop). This will ensure that all the pixels in the 640 × 480 area are mapped into any one of the pixel from 600 tiles. This size of the font being displayed can also be controlled by controlling address passed to fetch the font.

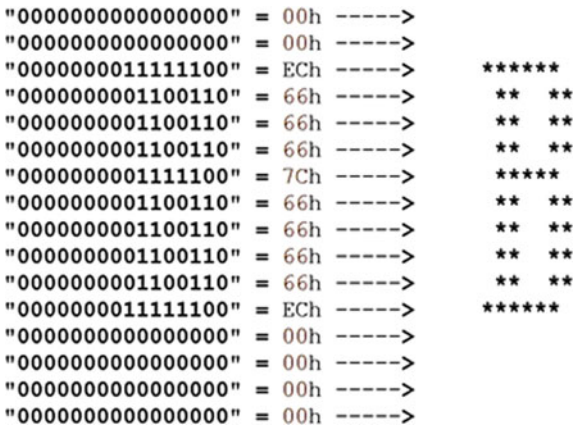

Fig. 5 Bit mapping for alphabet B

3.3 Network Protocol for RTU Support

To obtain the RTU support for the proposed system, MODBUS over serial line protocol is proposed to be implemented. MODBUS serial line communication protocol is a Master/Slave based protocol. This protocol stays at level two, i.e. data link layer of the OSI model. Master device always initiates the MODBUS communication. Slave device (up to 247 slaves can be connected) will not transmit data without a request from the master device, and do not communicate with each other slaves of the network. The MODBUS application protocol defines a simple protocol data unit (PDU) which is independent of the underlying hardware communication layer. The MODBUS over serial line defines two transmission modes, i.e. The ASCII mode and the RTU mode. This transmission mode (also serial port settings) must be the same for all devices on a MODBUS serial line. In the proposed work, MODBUS over serial line is used in RTU transmission mode.

Figure 6 shows the designed and implemented MODBUS over serial line PDU which consist of slave ID, function code, actual data and the CRC data. The slave ID address field contains the 8-bit data, i.e. it contains two hexadecimal digits. The function code contains the action to be performed, i.e. it contains the control information which will be decoded by the slave device to take necessary action on the received actual data. Function code is also 8-bit code. The actual data length can vary but in the current design it is chosen to be 16 bit to 32 bit wide. Out of 8 bytes, last

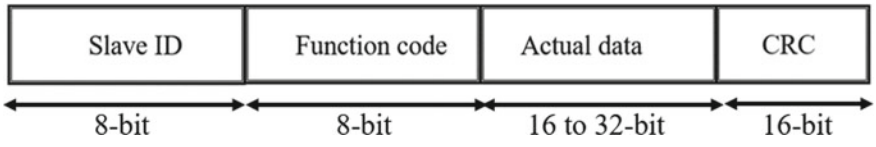

Fig. 6 Designed and implemented MODBUS PDU

two bytes were added to the frame after sixteen-bit CRC calculation on the slave ID, function code and actual data, all together. The cyclical redundancy checking data is 2 bytes: containing a sixteen-bit binary value. This CRC value is calculated by the Zybo board (which is a master) and appends it to the message. The slave device, i.e. ZED board that receives MODBUS PDU, again calculates the CRC during receipt of the frame and compares this recalculated value to the actual value it received in the CRC field.

4 Integrated Display Driver with RTU Support

To convey the proof of concept, the implementation includes the integration of VGA modules with memory modules, both block RAM and SD card along with Modbus over serial line protocol. This also includes the design of algorithms for master and slave devices. The pre-designed and tested VGA display driver is loaded in the slave FPGA device. This slave device also integrated with the slave code which can handle the RTU packets received from the master. Besides these, the designed slave also has the PS + PL interface and RTU packet decoding part in it. This slave is also interfaced with secondary memory, i.e. SD card. This memory holds the data to be displayed on the VGA display based on the decoded data which is received from the master device. This SD card consists of various image data files stored in the form of binary file. When slave is powered, it checks for the data from master, in case no data from master or master device is OFF then slave will be displaying the default image at default location on the VGA display screen. This default image conveys the user that slave has not received the RTU data from the master. Once the master data is availed at the slave, it will decode the data and based upon this information it will update the VGA screen with new image along with its X and Y coordinates (i.e. the location at which the image to be displayed). Similarly, for VGA font display design, the master device is required to send the RTU frame which should consist of tile number and ASCII character to be updated on that tile along with other mandated sub parts of the frame.

Master device is responsible for sending the RTU frames. This frame includes the major message parts such as slave ID, function code, actual data and check sum data. The actual data consist of which image to display (or font to be displayed in case of font display) on the VGA screen and coordinates, i.e. X and Y locations (Tile number in case of font display) at which the image to be updated. In the current master design, this information was sent in a fixed interval so that the design gets tested. The slave device will decode this X and Y location (or tiles information) and also decodes the image (or font) to be updated on the screen and performs the successive operation at the remote slave side.

Figure 7 shows the experimental setup and board connections, respectively, for the implemented design. VGA display is connected to the slave device, ZED board is used as slave device, and ZYBO board is used as master device. These master and slave devices are connected through the RS-232 hardware; a common ground is

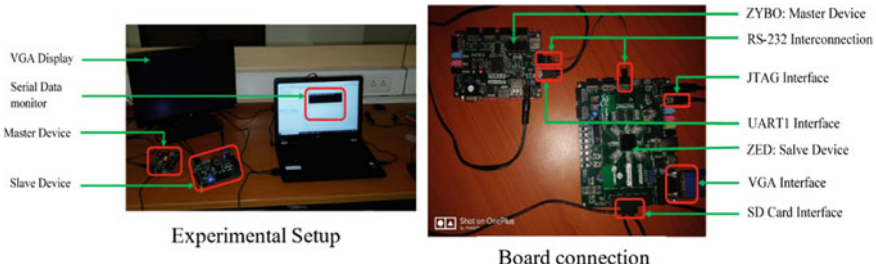

Fig. 7 Experimental setup and board connection

connected between these two to ensure both are at same reference potential point. UART1 peripheral is used for the serial monitoring of the data, and this terminal displays the data sent from the master.

5 Result and Discussion

In order to test the design, binary converted data of various images are loaded into the SD card. Based on the data received from the master device, slave will update the display. User-defined function codes are added to the MODBUS PDU to differentiate various functionality. Figure 8 shows the initial testing of the integrated VGA modules

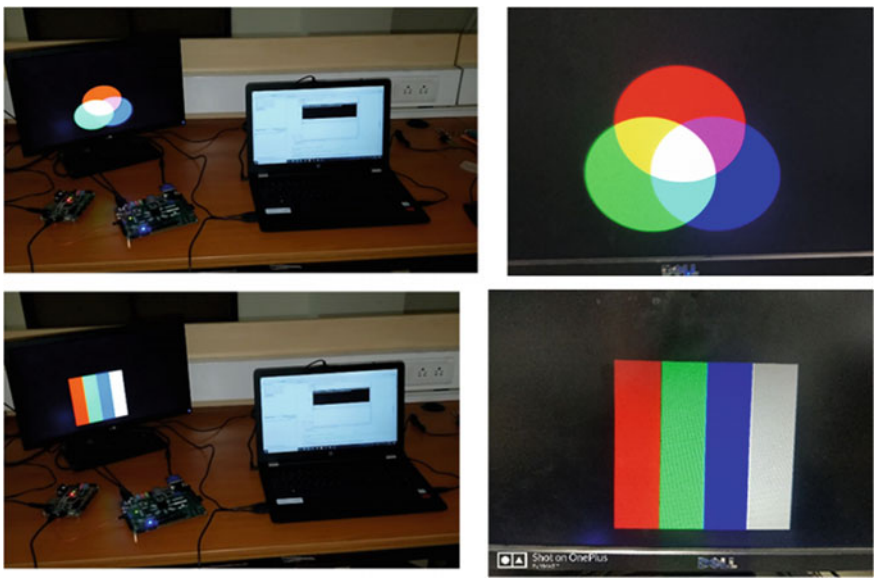

Fig. 8 Integrated VGA Module testing with basic RGB colours

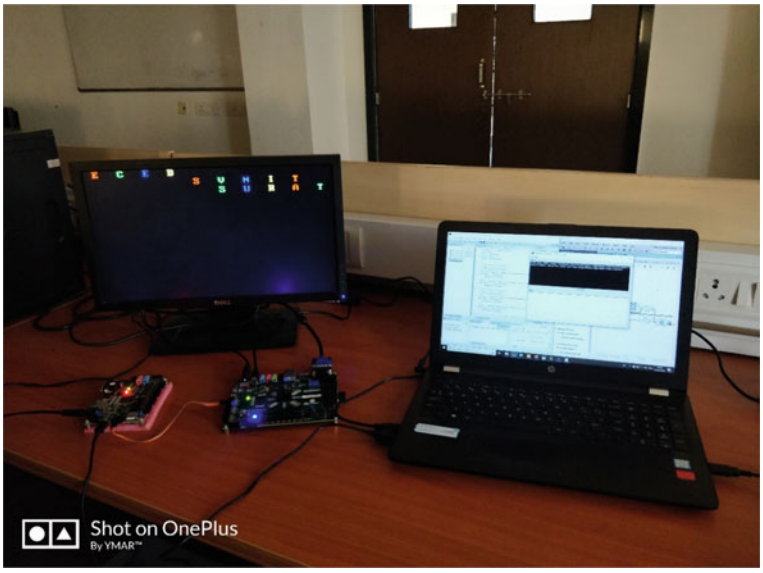

Fig. 9 Integrated system testing to display font with RTU in loop

using basic RGB colours.

When there is no data from RTU, slave display will show "Nothing to Display" which is also the default image. Once the data received, slave will update the display with new image in the new coordinates. Figure 9 shows such one of the simulated scenario to display default image in the integrated system testing with RTU in loop. This image is popped in the current scenario by making slave to go through clod start, hence initially slave will display default image until it will start receiving the frames from the master device. Once the data received, slave will update the display with new image in the new coordinates. Figure 9 shows the integrated system testing, in here master is programmed to send MODBUS PDU frame with regular intervals, where in the slave will decode this frame and decide which image to display on the VGA screen and fetch the corresponding data from the secondary memory, i.e. SD card and update the block RAM memory. The received RTU frame PDU also consist coordinates at which the decoded image to be displayed on the screen.

Figure 10 shows the results of the integrated system testing for font display with RTU in loop, and here the font table is stored in FPGA LUT memory. The master is designed to send the character string "ECED SVNIT SURAT". Note that each character in this string sent from the master will have tiles information in the sent MODBUS PDU. The slave is designed to identify and decode the coordinates of the font in the received MODBUS PDU, at which the new font to be updated. In here, it also possible to control the colour of each tile being displayed. The expected output is verified with the actual results and found to be satisfactory.

It is also possible to store the font table in the SD memory and avoid the dependence on the limited FPGA memories (LUTs). Figure 11 shows the results of the integrated

Fig. 10 Integrated system testing to display image with RTU in loop

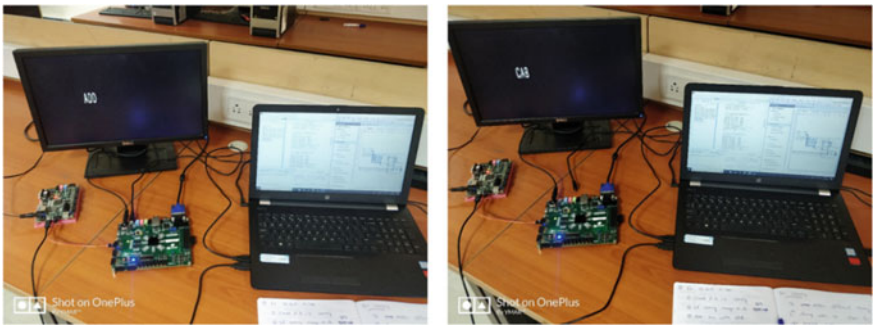

Fig. 11 Font display testing with font table stored in the SD card

font display testing where the font table is stored in SD card, where the master is designed to send the character string "ADD" and "CAB". The slave will decode the ASCII character received from the master and update the display. With this method, it requires very little modification in the design to display any language fonts.

Table 2 shows the comparison of various methods with respect to the various parameters.

6 Conclusion

The proposed paper work strives to implement the proof of concept for the new remote data displaying solution with design of actual system (Including display driver) from de novo. The proposed system has been designed with FPGA-based VGA display driver for both font and image display and integrated with MODBUS over serial line protocol, which intern gives the RTU support to the system. For the

Table 2 Comparison of various methods

	MCU based System	Embedded web server based system	Proposed system
Need of service provider	GSM Service provider is the back bone of the entire system	Internet service provider is required continuously for the operation	With serial communication no need of service provider
Flexibility	Limited functionality and flexibility in the software implementation and there is no hardware reconfiguration [6, 7]	With FPGA in loop offer both the performance of hardware and flexibility of software computing [5]	With FPGA in loop offer both the performance of hardware and flexibility of software computing [5]. (Implemented with PL and PS based integrated system)
Execution	Works in sequential mode only	With FPGA in loop Parallel execution is possible	Allotted parallel execution to PL part and sequential execution to PS part
Communication	GSM based wireless communication [6, 7]	Embedded web server based communication [5]	Open source and generic MODBUS protocol is chosen for the implementation [3]. Allows both **serial (Implemented)** and TCP/IP based communication
Display size	Constrained by display size. Display multiplexing is possible; however, it will lead to more drivers and MCUs	With FPGA in loop hardware can be customised to selected display, however, it is also limited by the memory of device under consideration	With FPGA in loop hardware can be customised to selected display, however, it is also limited by the memory of device under consideration
Retrofit option	Constrained by the MCU as it does not allows customised hardware logic implementation	Flexible in terms of customised hardware logic implementation and hence retrofitting [5]	Flexible in terms of customised hardware logic implementation and hence retrofitting and MODBUS has higher extending compatibility [3]

master and slave configuration design of system, ZYBO and ZED boards are used for implementation, respectively. The implementation of PS and PL based design allow the paralleling processing design to be allocated to PL part and sequential execution is allocated to PS part of the design. The use of FPGA in the system design gives the great advantage with respect to both the performance of hardware and flexibility of software computing besides being custom logic implementable.

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Dual-Band Pentagonal-Shape Hybrid Rectangular Dielectric Resonator Antenna for C-Band Application

Pinku Ranjan, Mihir Patil, and Anand Sharma

1 Introduction

These days wideband antenna is a needed in the society, due to multiple modern wireless applications emerging every day. There is a dire need to develop wideband antennas which can support multiple numbers of operations simultaneously [1]. Non-resonant antennas have been in use since a very long time. Because of their non-resonating structure, they can be used to receive a broad range of frequency. Even they possess a very strong candidature for wideband antennas, due to non-efficient design and very big size, they have not yet been put to practice as a wideband antenna.

In contrast, printed antenna can easily be used as a wideband antenna, due to its very small size and high efficiency even at higher frequencies. Proper optimization of the patch and the ground's dimensions can lead to wide impedance bandwidth. Various techniques are developed so as to attain large impedance bandwidth while keeping the size as small as possible. DR (dielectric resonator) can be placed over the radiating patch, and proper optimization of the dimensions of the DR with different feeding mechanisms can increase the impedance bandwidth of the antenna. In [2], the mathematical analysis of DR is shown with a microstrip slot and a microstrip line.

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Changes in the dielectric constant of the DR are also reported for further enhancement of the bandwidth. In [3], a multi-segment DR is proposed, where the thickness and the dielectric constant of both the segments are adjusted in a way to match the impedance of the DR to the microstrip line. This ensures the transfer of maximum power to the DR and hence helps in achieving an efficient antenna design. In [4], an Archimedean spiral slot is used to excite the rectangular DR and hence increase the bandwidth of the antenna.

Dual polarization is achieved in [5], and this helps in reduction in interference between nearby frequency by allotting different polarization to the waves and hence help to increase the handling capacity of the antenna by about 2–3 folds. Conducting loops are placed near the DR for generating circular polarization. 51% of circular polarization is achieved in the overall bandwidth. Similarly, in [6] a circularly polarized antenna is proposed with a stair-shaped DR fed with an open-ended ground plane. Introduction of the open-ended ground plane led to much better impedance matching and increment in the axial ratio bandwidth.

To further reduce the height of the antenna, an increase in impedance bandwidth was sought by using a printed antenna itself. Various numerical methods were implemented for different designs of the ground and the patch. Thus, in [7] a bow tie configuration is implemented to increase the bandwidth. Two patches are implemented in the design, but the novelty is that one is placed above the substrate and the other placed below the substrate. Gain greater than 2 dB is achieved in the whole band with an omnidirectional radiation pattern. In [8], a kind of similar bow tie pattern is shown with a balun integrated into the design, to help the antenna in impedance matching over a very large bandwidth. The dimensions of the balun are adjusted to further enhance the impedance bandwidth to 47%. In [9], the antenna is fed with coplanar strip lines. There are two rectangular arms on both the side of the substrate, and the arms below the substrate are bigger than their other counterpart. Both the top arms are connected to the bottom arms by shorting; this is done by drilling a hole through the substrate. Thus, this helps in the enhancement of the impedance bandwidth of the antenna. Also, in [10] the impedance bandwidth is increased by using CPW (Co-Planar Waveguide) feeding structure.

2 Antenna Geometry

The radiating patch on the top surface of the antenna and the ground both are made up of PEC (perfect electric conductor). The substrate is made up of FR4 epoxy, with the dimensions of $30 \times 30 \times 1.6$ mm^3. The top view and the bottom view of the antenna are shown in Figs. 1 and 2, respectively (all the dimensions shown in the figures are in mm). The length of the feed line on the top surface is 3 mm $\times$ 24 mm. Keeping 22 mm $\times$ 15 mm as the center point, a pentagon and a triangle are drawn. The dimension of the regular pentagon and the regular triangle is 8.28 and 8.66 mm. The pentagon is united with the feed line, while the triangle is subtracted from the united structure. The ground plane is made by subtracting a small cuboid with the

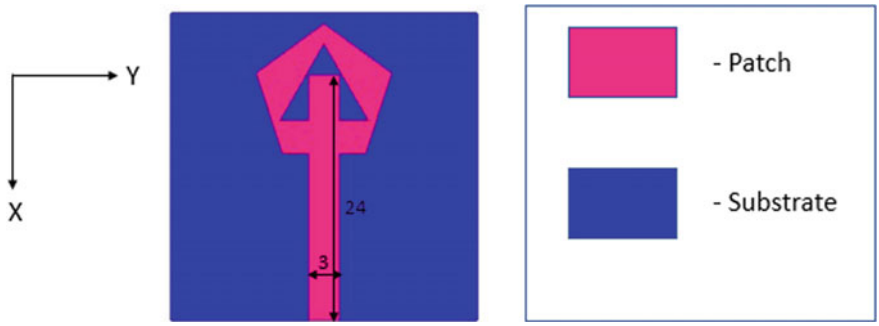

Fig. 1 Top view of the pentagonal patch of the proposed antenna

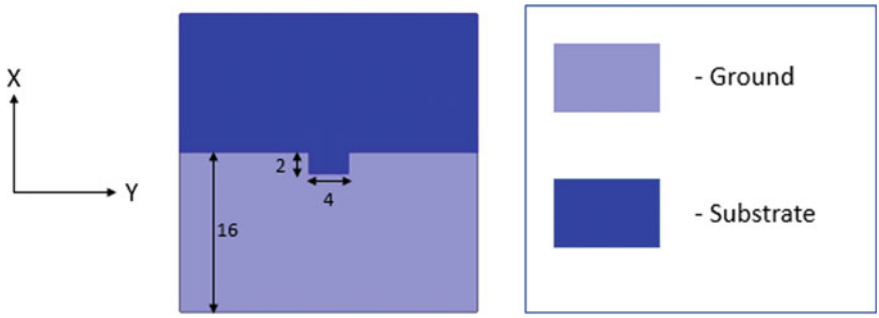

Fig. 2 Bottom view of the proposed antenna

dimension of 2 mm × 4 mm from a cuboid of dimension 16 mm × 30 mm. The height of both the ground plane and the patch is 0.035 mm. Over the radiating patch, a DR (dielectric resonator) is kept along with optimizing the size to 13 × 13 × 6 mm^3. The reason for selecting cuboidal DR is due to its two parameters (height/length and width/length). Both of these parameters can be independently controlled to make changes in the impedance bandwidth of the antenna. This enables the designer to make extra iterations in the design to achieve the best antenna characteristics. The cross-sectional view of the antenna is shown in Fig. 3.

3 Results and Discussion

All the simulations are done in HFSS 13.0. The step size is 0.01 GHz. The maximum number of passes is 6, while maximum delta *S* taken is 0.02.

In Fig. 4, S-parameter of the antenna is shown. The antenna is a dual-band antenna as it resonates in 3.72–5.8 GHz and 6.38–8 GHz. Hence, it promises a total impedance bandwidth of 3.7 GHz. It resonates at 4.42 and 7.63 GHz.

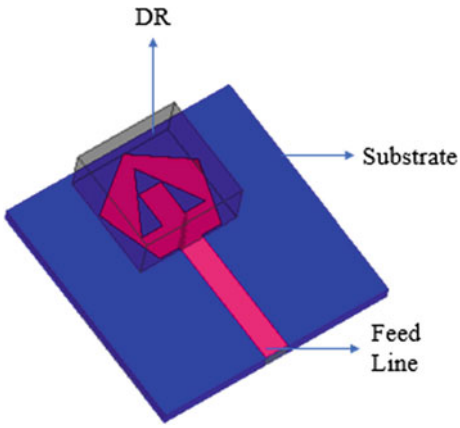

Fig. 3 Cross-sectional view of the proposed antenna

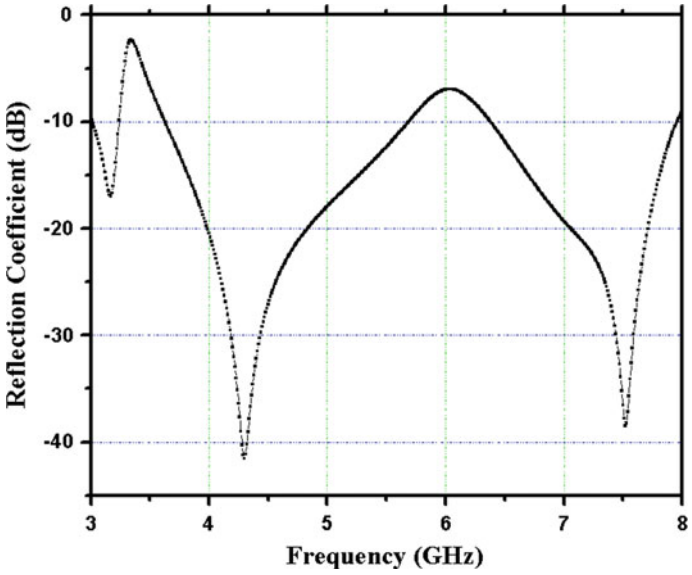

Fig. 4 S-parameter of the proposed Antenna

The antenna promises radiation efficiency of greater than 95% in the whole impedance bandwidth, while the directivity achieved is greater than 3 dBi at frequency 4.42 GHz.

Figure 5 shows the gain plot. The antenna promises gain of greater than 3 dBi in the first band. Also, the simulated far-field parameters show gain greater than 2 dB at the other band.

Figure 6 shows the 3D polar plot of the proposed antenna. The antenna promises

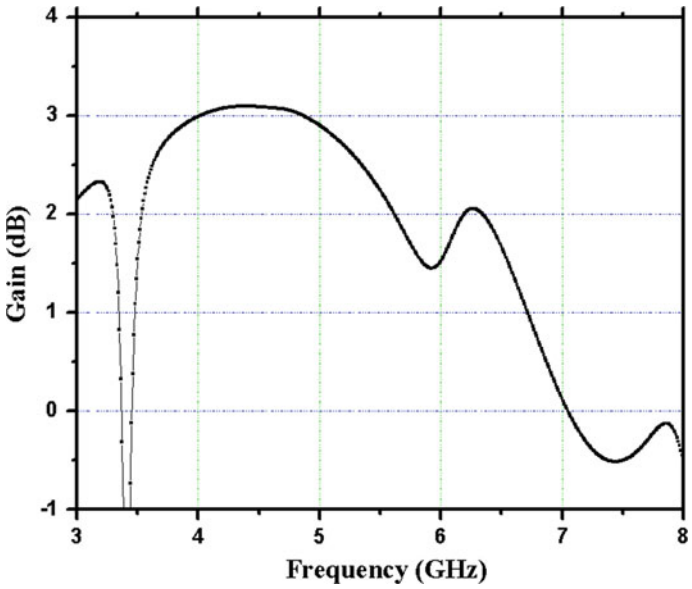

Fig. 5 Gain versus frequency plot of the proposed antenna

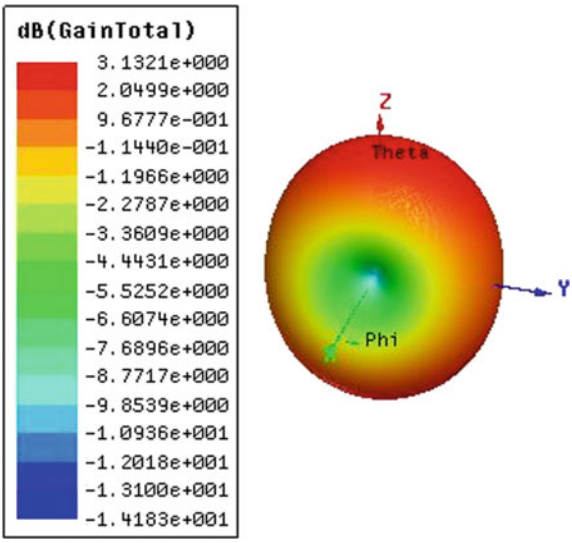

Fig. 6 3D plot of the proposed antenna

omnidirectional radiation pattern, with a maximum gain of 3.13 dB at theta = 0 deg and phi = 0 deg.

Figure 7a, b represents E-plane & H-plane radiation pattern at frequency 4.42 GHz,

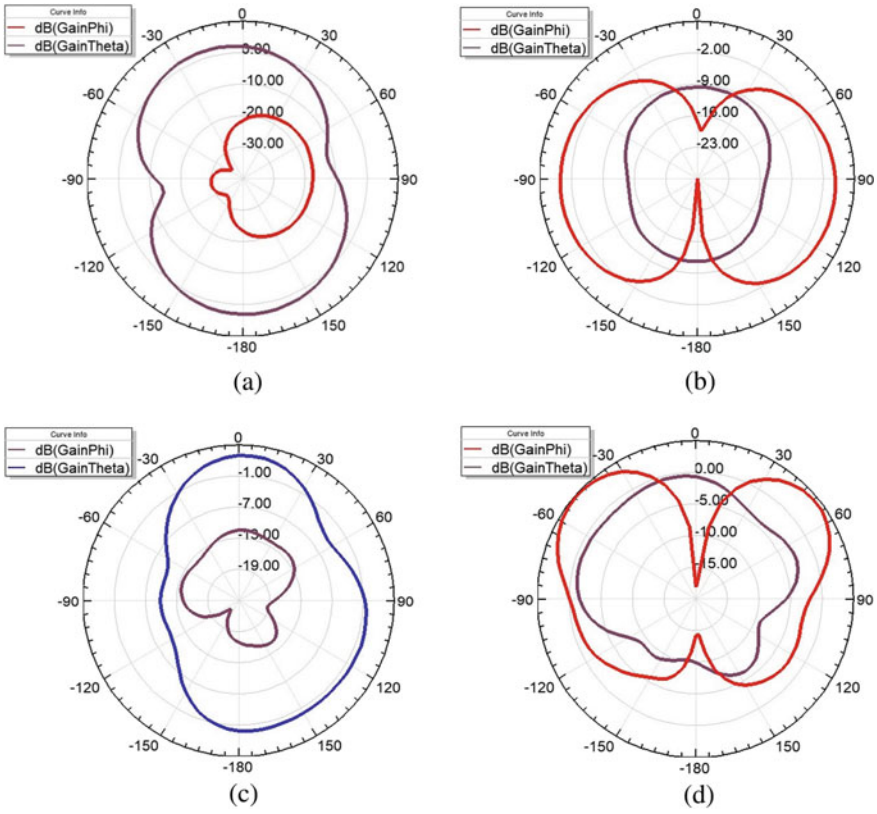

Fig. 7 E-plane and H-plane 2D radiation pattern

respectively, b, d represents E-plane & H-plane radiation pattern at frequency 7.63 GHz, respectively, of the proposed antenna.

4 Conclusion

A wideband antenna is designed for C-Band application; it has an impedance bandwidth of 3.77 GHz. It is a dual-band antenna as it resonates at 4.42 and 7.63 GHz. The antenna promises a gain of greater than 3 dB, with an omnidirectional radiation pattern. It also has a radiation efficiency of greater than 95% in the whole impedance bandwidth. The major advantage of the design is its ability to operate in Sub-6-GHz and C-Band, thus enabling multiple wireless applications.

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Performance Evaluation of Various Precipitation Algorithms Over the Indian Subcontinent Region

P. Giri Prasad, P. Anil Kumar, and S. Varadarajan

1 Introduction

The economy of the India is highly dependent on the agriculture. The yield of the agriculture can be predicted based on the amount of rainfall received. The greater part of the subcontinent receives 60–80% of annual rainfall during south-west monsoon and has great impact on our economy [1]. Hence accurate prediction of rainfall is very significant for agricultural production. Due to limited number of rain gauges and sparsely distributed weather RADARs over the Indian subcontinent region, accurate estimation and forecasting of rainfall over the surface region become quite complex. Hence, there arises a necessity for the satellite network for the accurate estimation of rainfall over both the land surface and ocean regions. Satellite plays a crucial role in hydrological modeling and climatological studies. The precise measurement and prediction of rainfall rate both in time resolution and spatial resolution can be achieved with the help of high-resolution satellites. Hence, Researchers have started to make use of these satellite data for estimations of rainfall at high precision all over the world [2–4]. A wide number of algorithms are available in the literature for the estimation of rainfall over the Indian regions at high temporal and spatial resolutions [5, 6]. A large number of techniques are available for rainfall estimation which uses various sensors data and each has its own advantages and limitations. The available

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techniques for the prediction of rainfall in the literature are based on VIS/IR, IR-TB, IR-WV bands of the geostationary satellite data. The temporal resolution of the geostationary satellites is 30-min interval. In general, a variety of sensors are placed on the satellite which has the data in the bands of visible, water vapor, and thermal infrared band. Most of satellite-based rainfall estimates are based on TIR data, which gives the data about the brightness temperature of cloud top height. The Cloud Top Brightness Temperature (CTBT) has a direct relation to the type of clouds, and it plays a significant role in identifying the rain bearing clouds. Clouds with a low CTBT produce convective rainfall and have an indirect relation with precipitation rates over the surface because the TIR measurements cannot penetrate into the clouds [7].

Threshold-based techniques are used to discriminate the rainy pixels from the non-rainy pixels. If the value of CTBT is less than or equal to 235 K, then the pixel is treated as a rainy pixel. If the CTBT values cross 235 K, then the pixel is considered as a non-rainy pixel [8, 9]. Clouds are classified based on the CTBT values. The clouds with the same CTBT precipitate different amount of rainfall based on the other external atmospheric parameters. Hence the TIR-based methods fail to estimate the precipitation accurately. Also, this method fails to classify the thin cirrus clouds based on the CTBT value, which has no relation with the rainfall [10].

The CTBT estimated from the TIR band fails to estimate the vertical structure and composition of the clouds. The vertical profile of the cloud has a direct relation to rainfall [11]. The advantage of using TIR measurements is the availability of its high temporal resolution. The main limitations of the infrared-based algorithms are its inability to discriminate the rain/non-rainy pixels. Unlike TIR measurements, the microwave (MW) measurements provide physical connection with rain and hydrometeors since they penetrate through clouds but suffer with poorer temporal and spatial resolutions (lower orbiting satellites gives less coverage). Hence, there is a need to merge TIR measurements and MW measurements for better estimates of precipitation which gives rise to hybrid algorithms.

The estimation accuracy of the rainfall can be improved by merging the algorithms on the two individual datasets [2]. Moreover, estimation of rainfall using multispectral band provides better accuracy than using single TIR band. The WV band images provide brightness temperature with respect to the vertical moisture content in the atmosphere. If Water Vapor Brightness Temperature (WVBT) is low, it indicates there is a high probability for precipitation. If the value of the WVBT is high, then there is low chance of precipitation. Hence WVBT plays a crucial role along with the TIR band for better the estimation of precipitation [12].

Table 1 Characteristics of the Kalpana-1 VHRR data

Band name	Wavelength (μm)	Resolution (km)
Visible	0.55–0.75	2
TIR	10.5–12.5	8
WV	5.7–7.1	8

2 Data Used in the Work

2.1 Kalpana-1 Data

Kalpana-1 is an Indian geostationary satellite launched by ISRO on 12th Sept 2002. The sensors placed on the Kalpana-1 satellite operate in three different wavelengths. The VHRR sensor operates in three different bands namely VIS, TIR and WV. The spatial resolution of the WV, TIR and VIS band is 8 km, 8 km, and 2 km, respectively. The characteristics of the onboard sensor for the Kalpana-1 satellite are shown in Table 1.

2.2 TMPA-3B42v7

The TMPA consists of three products, namely 3B42 which collects data three-hourly, 3B42 derived which collects data daily, and 3B43 products which accumulate data monthly. The TMPA interpolates precipitation estimates from both the rain gauge analyses and satellite systems for improving the spatial resolution. The spatial resolution of the TMPA is 0.25° which merges data from the multiple satellites. In the present study, 3B42 data was employed to analyze the duration and intensity of the rainfall over the Indian subcontinent (http://mirador.gsfc.nasa.gov).

2.3 GSMaP Data

GSMaP was initiated by the Japan Science and Technology Agency in 2002 to produce a global precipitation product with very high spatial and temporal resolution. This product has the data from Microwave sensor and an infrared sensor which is onboard of a geostationary satellite. The temporal resolution of the GSMap is hourly and daily. The spatial resolution of the GSMap is 0.01° (http://sharaku.eorc.jaxa.jp/GSMaP_crest/html/data.html).

2.4 Automatic Weather Station (AWS) Rain Gauge Data

The AWS maintained by the ISRO is a minimized, particular, rough, amazing and ease framework and housed in a portable, self-contained package. It procures point data with three hour duration. It collects various atmospheric parameters such as precipitation from rain gauge, humidity, relative humidity at 2 m level, Atmospheric temperature, Atmospheric pressure, wind speed and wind direction. In the present study, AWS data is used for validation of the rainfall estimation algorithm.

3 Methodology

Estimation of rainfall intensity and place of occurrence is quite unpredictable and hence the precipitation estimation within a spatial grid occupies a predominant role (i.e. determination of rainy and non-rainy pixel). Clouds such as convective (cumulonimbus, nimbostratus, stratocumulus) and non-convective clouds (cirrus, altostratus, stratus) are classified based on the thermal IR and WV channels in the Kalpana [13, 14]. The present technique comprises two steps. In the first step, the rainy pixels are discriminated from the non-rainy pixels. In the second step, the precipitation rates are evaluated for the rainy pixels based on nonlinear power relation method [15].

In the present technique, convective and non-convective clouds are separated based on segmentation and Hard Threshold technique. The gray level values of the TIR and WV band are converted into brightness temperature with the help of standard predefined Lookup table for the Kalpana satellite. Based on the brightness temperature of these bands, a pixel is considered as a rainy pixel if it satisfies the following criteria:

(i) Brightness Temperature of TIR band (BT TIR) < 250 K and
(ii) Brightness Temperature of TIR band (BT TIR)—Brightness Temperature of WV band (BT WV) < 19 K.

In the present algorithm, precipitation rates are computed-based convective cloud information and the relation between them is nonlinear power relation. Figure 1 depicts the flowchart for the present algorithm. The intensity and magnitude of the rainfall are evaluated for every half an hour and at each spatial grid point. The procedure is repeated over the entire day to get the accumulated rainfall on daily basis. Monthly rain is calculated by cumulatively adding the daily rains over the month duration. Validations are made over land and ocean for heavy rainfall days using two global rainfall products (TMPA-3B42 v7 and GSMAP data) along with available AWS data provided by Indian Meteorological Department (IMD). The comparisons are done over $0.25° \times 0.25°$ grid spatial resolution. In order to validate the Kalpana-1 data with global rainfall data products, Kalpana-1 data are regridded to $0.25° \times 0.25°$ spatial resolution.

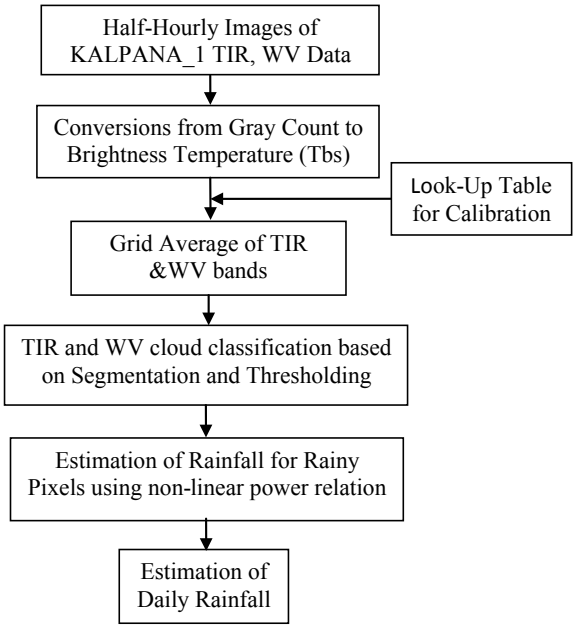

Fig. 1 Flowchart for the proposed algorithm

3.1 Selection of Categorical Statistics

To estimate the performance of the present algorithm, the categorical statistics used in this work are Probability of Non-Detection (POND), Probability of Detection (POD), False Alarm Rate (FAR), BIAS, and accuracy (ACC). These parameters are evaluated regional-wise at a spatial resolution of 0.25°. The Contingency matrix of Global rainfall Product and Observed (TMPA-3B42 V7) data is tabulated in Table 2.

Hits (h) is defined as the number of pixels for which are correctly classified as rainy pixel in both the selected global rainfall data set and the TMPA-3B42 V7. False alarm (f) is defined as the number of misclassified pixels such as the rainy pixel is recognized as a non-rainy pixel and vice versa. Misses (m) are defined as the number of rainy pixels which are not detected by the global rainfall data but are detected by the TMPA-3B42 V7.

Correct negatives (z) are defined as the number of non-rainy pixels correctly classified by both the selected global rainfall data and the TMPA-3B42 V7 [8, 14].

Table 2 Contingency matrix of selected rainfall data and observed (TMPA-3B42V7)

		Observed (TMPA-3B42 V7)	
		Occurrence of rain	Non-occurrence of rain
Rainfall data set	Occurrence of rain	h	F
	Non-occurrence of rain	m	Z

Depending on the contingency matrix, various categorical statistics are calculated as follows:

$$\text{BIAS} = \frac{f+h}{m+h} \tag{1}$$

$$\text{POD} = \frac{h}{m+h} \tag{2}$$

$$\text{POND} = \frac{z}{z+f} \tag{3}$$

$$\text{ACC} = \frac{(h+z)}{(h+m+f+z)} \tag{4}$$

$$\text{FAR} = \frac{f}{f+h} \tag{5}$$

BIAS is defined as the ratio of the number of correctly identified rainy pixels by selected rainfall dataset to the total number of rainy pixels present in TMPA-3B42 V7. The value of the BIAS indicates whether the selected rainfall dataset has overestimated/underestimated the number of rainy pixels available in TMPA-3B42 V7. A BIAS value more than 1.0 demonstrates that chosen precipitation dataset has more number rainy pixels compared to demonstrates that the rainfall dataset overestimates compared to TMPA-3B42 V7, while a BIAS of less than 1 demonstrates that the selected rainfall dataset underestimates the number of rainy pixels compared to TMPA-3B42 V7. The POD is characterized as the proportion of the number of correct rainy pixels detected by selected rainfall dataset to the total number of rainy pixels present in TMPA-3B42 V7. POD is a measure of the algorithm accuracy for detecting the rainy pixels. A POD of unity value indicates that the selected rainfall dataset correctly identified all the rainy pixels. POND is characterized as the proportion of the number of correctly identified non-rainy pixels by selected rainfall dataset to the total number of non-rainy pixels present in the selected rainfall dataset. ACC is the acronym for accuracy and is defined by the ratio of the correctly detected pixels whether it is rainy or non-rainy to the total number of pixels. The value of the accuracy lies between 0 and 100%. The value of the ACC has a direct relation to the POD and POND. As the POD, POND value increases; the value of ACC increases. FAR is defined as the proportion of the number of rainy pixels wrongly detected by selected Rainfall dataset to the total number of rainy pixels detected by that selected Rainfall dataset. The lower the FAR the better the Rainfall dataset.

4 Results and Discussions

The validation of the present technique was examined over the Indian sub-continent and oceanic regions during heavy rainfall events of 2015 and 2016. The performance of the algorithm is cross verified with TRMM-3B42 values and validated with rain-gauges. The present algorithm was tested under different conditions, and the results are presented here. The rainfall derived using the present technique was validated with TMPA-3B42 V7 and IMD daily rainfall.

4.1 Case Study-I (27th July, 2015)

For evaluation of the present technique, a random date was chosen from the southwest monsoon. The rainfall was evaluated on 27th July using the present technique, and the results are compared with the TMPA 3B42 V7, GSMAP, and IMD. Figure 2a–d is the daily accumulated rainfalls collected from the TMPA 3B42 V7, Kalpana, GSMAP, and IMD, respectively.

The Categorical Statistics evaluated on this day was tabulated in Table 3. From table, it is observed that a bias of 1.2029 indicates that Kalpana-1 rainfall data overestimates with respect to TMPA-3B42 V7, whereas a bias of 0.7857 indicates that GSMAP rainfall data underestimates with respect to TMPA-3B42 V7. The categorical statistics are evaluated for the standard Arkin's method which is based on

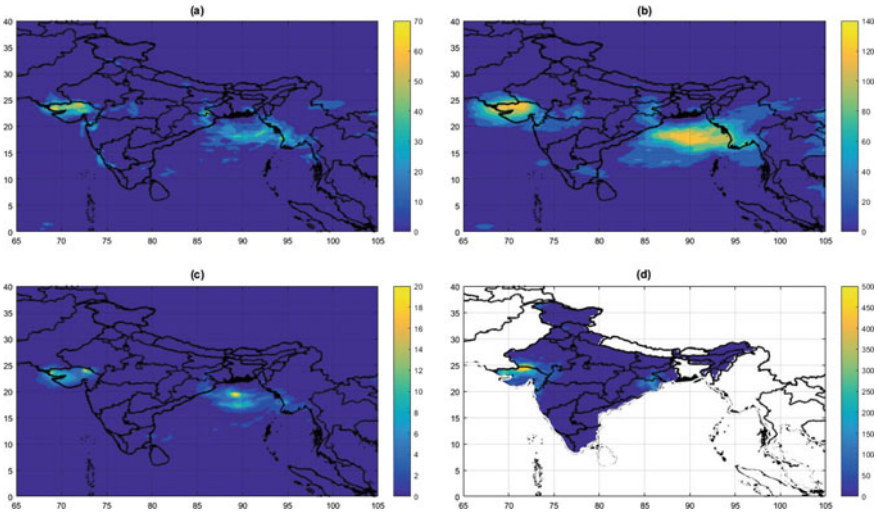

Fig. 2 Daily gathered rainfall (in mm) using **a** TMPA-3B42V7; **b** Kalpana-I; **c** GSMAP; **d** IMD on 27th July, 2015

Table 3 Categorical statistics for case study-I

	Kalpana-1 versus TMPA-3B42 V7	GSMAP versus TMPA-3B42 V7	Arkin's technique versus TMPA-3B42 V7
Correlation coefficient	0.8072	0.7592	0.6573
BIAS	1.2029	0.8313	1.320
POD	0.7991	0.6930	0.7121
POND	0.8760	0.8230	0.9011
ACC	0.7346	0.6894	0.6383
FAR	0.2265	0.3281	0.1723
RMSE (rain in mm)	16.6690	20.3676	24.7854

the thresholding technique. In this technique, a pixel is treated as rainy pixel if the brightness temperature of IR band is less than 235 K.

4.2 Case Study-II (09th November, 2015)

9th November 2015 was chosen as a second case during the northeast monsoon. The rainfall was evaluated on 9th November 2015 using the present technique, and the results are compared with the TMPA 3B42 V7, GSMAP, and IMD. Figure 3a–d is the daily accumulated rainfalls collected from the TMPA 3B42 V7, Kalpana, GSMAP [16], and IMD, respectively. From the figure one can observe the convective clouds

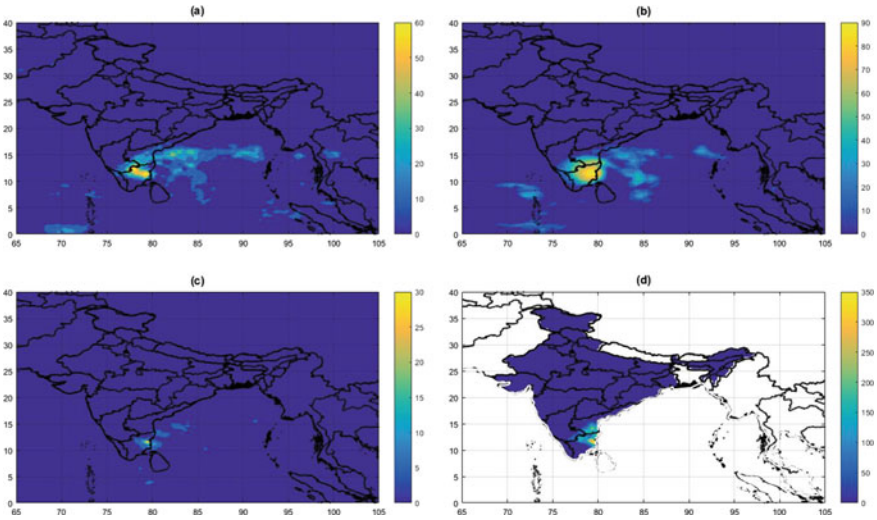

Fig. 3 Daily gathered Rainfall (in mm) using **a** TMPA-3B42V7; **b** Kalpana-I; **c** GSMAP; **d** IMD on 9th November, 2015

Table 4 Categorical statistics for case study-II

	Kalpana-1 versus TMPA-3B42 V7	GSMAP versus TMPA-3B42 V7	Arkin's technique versus TMPA-3B42 V7
Correlation coefficient	0.7094	0.6644	0.6726
BIAS	1.0192	0.8762	0.7854
POD	0.8482	0.7692	0.7564
POND	0.9594	0.9045	0.9723
ACC	0.8009	0.7665	0.7352
FAR	0.0909	0.2664	0.1732
RMSE (rain in mm)	5.2408	6.8845	9.7723

over Tamil Nadu and adjoining Districts of Andhra Pradesh. A low pressure area was formed in the south Bay of Bengal on 8th November, which converted into a deep depression. This deep depression was associated with strong winds and remained practically stationary very close to the coast of Tamil Nadu. This caused very heavy rainfall at a few places with isolated extremely heavy rainfall over Tamil Nadu and adjoining Districts of Andhra Pradesh.

From Table 4, it is observed that a bias of 1.0192 indicates that Kalpana-1 rainfall data overestimates with respect to TMPA-3B42 V7, whereas a bias of 0.8762 indicates that GSMAP rainfall data underestimates with respect to TMPA-3B42 V7.

4.3 Case Study-III (1st December, 2015)

1st December was chosen as a third case for evaluation of the present technique. The rainfall was evaluated on 1st December 2015 using the present technique, and the results are compared with the TMPA 3B42 V7, GSMAP, and IMD. Figure 4a–d is the daily accumulated rainfalls collected from the TMPA 3B42 V7, Kalpana, GSMAP, and IMD, respectively. In quick succession, two troughs of low pressure were developed over Southeast Bay of Bengal during last week of November which move westwards toward Tamil Nadu coast and result in very heavy rainfall at Tamil Nadu and adjoining Districts of Andhra Pradesh.

From Table 5, it is observed that a bias of 1.0924 indicates that Kalpana-1 rainfall data overestimates with respect to TMPA-3B42 V7, whereas a bias of 0.9027 indicates that GSMAP rainfall data underestimates with respect to TMPA-3B42 V7.

4.4 Case Study-IV (07th July, 2016)

For the present case, the daily rainfall on 07th July 2016 has been examined using the present technique. Figure 5a–d is the daily accumulated rainfalls collected from the

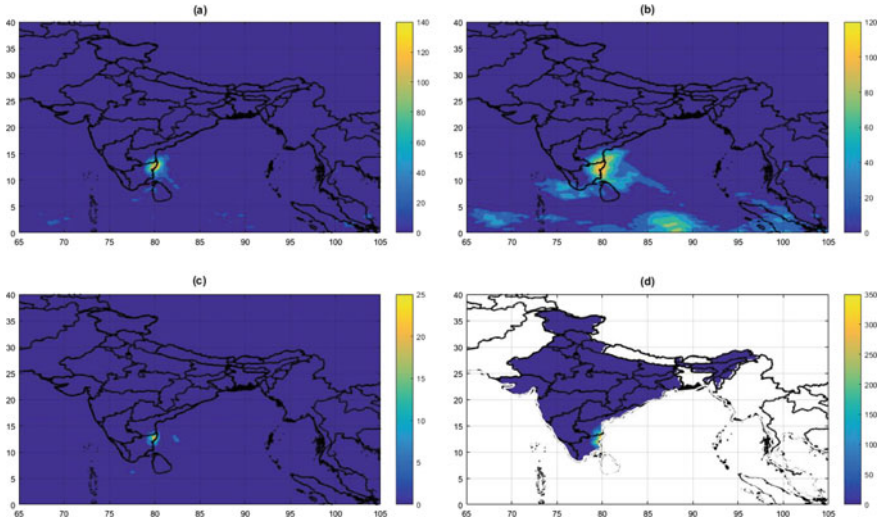

Fig. 4 Daily gathered Rainfall (in mm) using **a** TMPA-3B42V7; **b** Kalpana-I; **c** GSMAP; **d** IMD on 01st December, 2015

Table 5 Categorical statistics for case study-III

	Kalpana-1 versus TMPA-3B42 V7	GSMAP versus TMPA-3B42 V7	Arkin's technique versus TMPA-3B42 V7
Correlation coefficient	0.7346	0.7135	0.6845
BIAS	1.0924	0.9027	0.8754
POD	0.8582	0.8162	0.7785
POND	0.9415	0.8776	0.9526
ACC	0.8884	0.8717	0.8490
FAR	0.1712	0.2741	0.1265
RMSE (rain in mm)	9.5310	12.8229	16.8523

TMPA 3B42 V7, Kalpana, GSMAP, and IMD, respectively. A deep depression was formed over Madhya Pradesh which results in heavy rainfall in and around Madhya Pradesh.

From Table 6, it is observed that a bias of 1.2313 indicates that Kalpana-1 rainfall data overestimates with respect to TMPA-3B42 V7, whereas a bias of 0.8545 indicates that GSMAP rainfall data underestimates with respect to TMPA-3B42 V7.

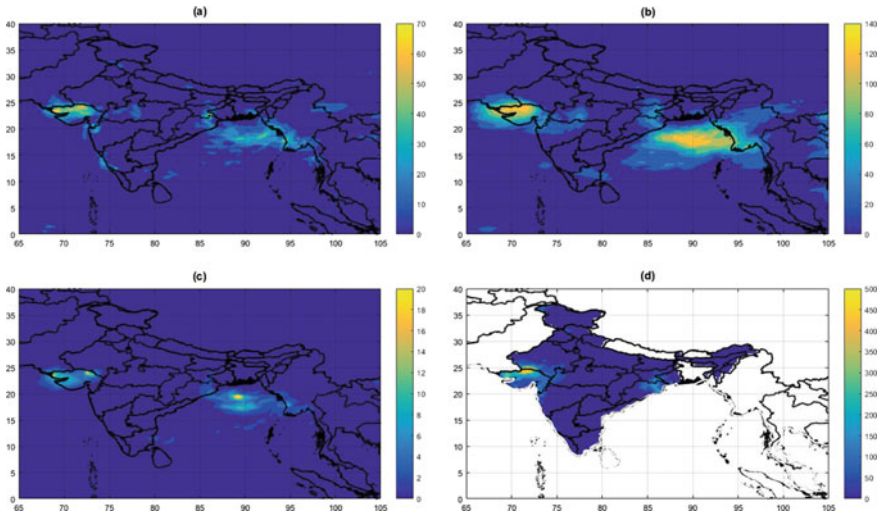

Fig. 5 Daily gathered rainfall (in mm) using **a** TMPA-3B42V7; **b** Kalpana-I; **c** GSMAP; **d** IMD on 07th July, 2015

Table 6 Categorical statistics for case study-IV

	Kalpana-1 versus TMPA-3B42 V7	GSMAP versus TMPA-3B42 V7	Arkin's technique versus TMPA-3B42 V7
Correlation coefficient	0.7238	0.6716	0.6535
BIAS	1.2313	0.8545	0.7620
POD	0.7955	0.7177	0.6920
POND	0.7869	0.6439	0.8012
ACC	0.7529	0.7079	0.7215
FAR	0.2601	0.3603	0.1925
RMSE (rain in mm)	21.5205	24.5904	29.4560

4.5 Validation of AWS Data

For the above cases, the rainfall derived from the present algorithm (Kalpana-1) and TMPA-3B42 V7 is compared with available AWS data. Based on the availability of AWS stations, IMD provides regridded daily rainfall data with a spatial resolution of 0.25° × 0.25°. Hence the regridded Kalpana rainfall data, TMPA-3B42 V7 and GSMAP Rainfall data can be compared with a spatial resolution of 0.25° × 0.25°.

IMD provides Rainfall data from latitude 6.5 to 38.5 and longitude from 66.5 to 100 with a spatial resolution of 0.25°. Some pixels are assigned with NaN (No data) which represents the location is in ocean. IMD provides rain data for 4964 data points. For these available data points, comparison has been done for the above satellite rainfall datasets.

Case I: (July, 27, 2015)

	Kalpana-1 versus IMD	TMPA-3B42 V7 versus IMD	GSMAP versus IMD
Correlation coefficient	0.8421	0.8377	0.6937
RMSE (rain in mm)	40.7091	51.9198	58.5332

Case II: (November, 09, 2015)

	Kalpana-1 versus IMD	TMPA-3B42 V7 versus IMD	GSMAP versus IMD
Correlation coefficient	0.8757	0.8624	0.8475
RMSE (rain in mm)	16.9031	21.5172	26.5358

Case III: (December, 01, 2015)

	Kalpana-1 versus IMD	TMPA-3B42 V7 versus IMD	GSMAP versus IMD
Correlation coefficient	0.8804	0.9364	0.9252
RMSE (rain in mm)	13.2148	16.4420	21.1799

Case IV: (July, 07, 2016)

	Kalpana-1 versus IMD	TMPA-3B42 V7 versus IMD	GSMAP versus IMD
Correlation coefficient	0.7043	0.7496	0.6810
RMSE (rain in mm)	26.4889	32.6634	36.5618

5 Conclusions

The present study evaluates the performance of the present rainfall estimation method with the other SRE algorithms such as TMPA-3B42v7 and GSMap Rainfall product during heavy rainfall events. The results show that the present algorithm is well suited with TMPA-3B42v7, GSMAP, and available IMD data. From the aforementioned results, it is observed that the Arkin's algorithm has less FAR and more POND compared to present technique. The proposed technique shows better performance in terms of accuracy, POD, RMSE, and BIAS compared to the existing Arkin's method. Also from the results, it is observed while comparing with IMD data, the

present technique has great improvement in RMSE compared to TMPA-3B42v7 and GSMAP. From the results, it is clear that the RMSE is less for case II and case III compared to Case I and Case IV. This shows that the satellite rainfall estimation algorithms are well suited for coastal regions when compared with semiarid desert regions. From the aforementioned results, the proposed method surpasses the results obtained by TMPA-3B42v7 and GSMAP Rainfall products.

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A FSS- and Metasurface-Loaded Dual-Polarized High-Gain Waveguide Array

Avinash Chandra, Kalpesh S. Dakhode, and Hemprasad Yashwant Patil

1 Introduction

Please note that the first paragraph of a section or subsection is not indented. The first waveguide has many advantages in satellite communications and radars because they are capable of handling more power, higher gain and moderate manufacturing cost. With the recent development of RF technology, demands of advanced multiband antennas have risen rapidly over past few years. Generally slotted array waveguides and reflectors array are used for this purpose because these structures have simple feeding mechanisms, to sustain a very high power, negligible losses, moderate gain and simple fabrication procedure. These things attracted to the various researchers from last seven decades. The past work mainly concentrated on calculation of full wave analysis of waveguide aperture and slotted antenna [1].

A changes in the waveguide-based technology when, in last decade Marques et al. [2] proposed propagation of waves in a hollow metallic waveguide, periodically embedded with stop-band resonators. The equivalent circuit model of resonators had been presented by Baena et al. [3, 4] in the year 2005. Chandra and Das, in 2016, published a work on multiband slot antenna with improved radiation behaviors [5, 6]. In 2017, the superstrate-loaded polarization reconfigurable array has been presented by Chandra et al. The metasurface has been inserted in waveguide to obtain the circular polarization in both bands. The next year in 2018, Chandra and Das [7] have analyzed a two-element dual-band dual-polarized high-gain slot array with improved radiation parameters.

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In this communication, a FSS and metasurface-loaded dual-polarized waveguide array has been presented. An octal shape SRR has dual-band dual-polarized behavior with improved gain of 2 dBi. The proposed antenna has dual-band nature; it shows CP in first band and linear vertical polarization in the second band. The designed array is useful for radar and satellite communication.

2 Dual-Band Dual-Polarized Array

The geometrical view of designed radiator is depicted in Fig. 1a. Geometrical view

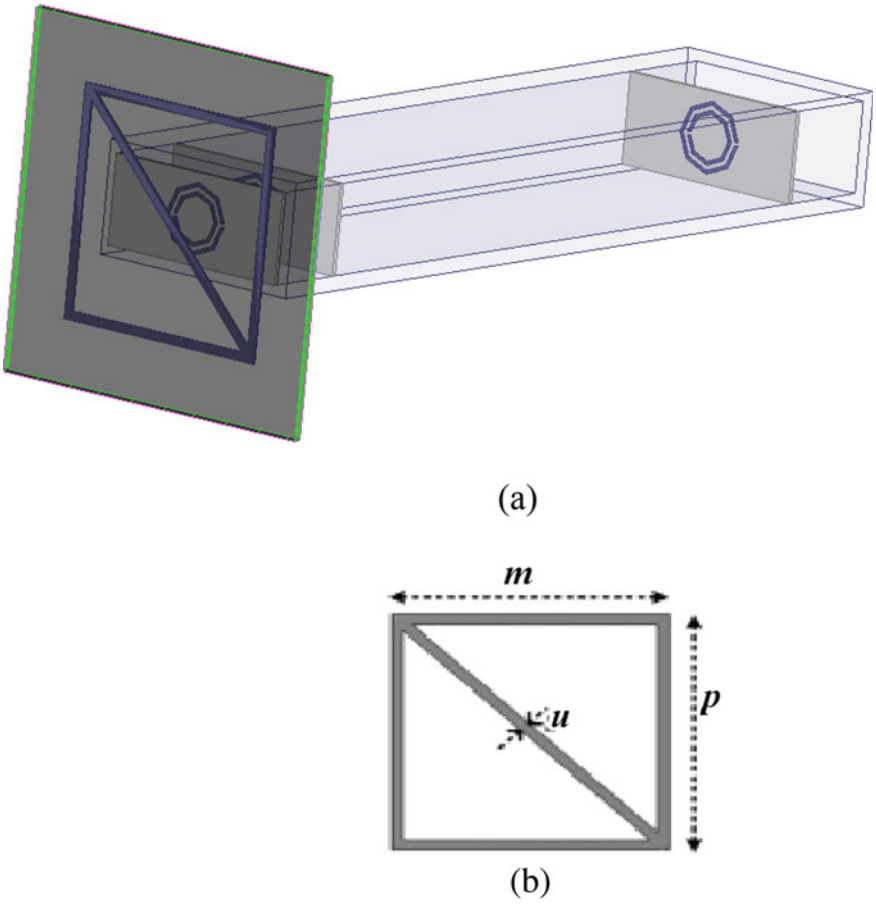

Fig. 1 Presented dual-polarized aperture array. **a** Three-dimensional view of presented array. **b** Metasurface. Cell; $u = 1.08$ mm, $m = 25$ mm and $n = 25$ mm (distance between aperture and FSS is 5.1 mm)

of metasurface is depicted in Fig. 1b.

The shape has been processed on the expansive mass of a waveguide having geometrical restriction and wide divider measurements 10.16 and 22.86 mm, separately. The FSS of octal shape having equal sides has been taken to structure the array. Rogers RT Duriod 5880 with thickness 0.508 mm with relative permittivity 2.2 has been taken for designing the metasurface and FSS. The optimized separation between FSS and the aperture is 5.1 mm.

3 Scattering and Radiation Behavior

The S11 of presented FSS-loaded array is depicted in Fig. 2. The presented three-element array has dual-band behavior. It has more than 10-dB impedance bandwidth ranges from 8.5 to 11.05 GHz. The proposed array resonates at 2 different frequencies at 9.5 GHz and 11.05 GHz, respectively. The 3-dB axial ratio of metasurface-loaded dual-band radiator is depicted in Fig. 3. It revealed that axial ratio (AR) bandwidths range from 9.3 to 9.7 GHz. Figure 4 shows that the field vectors movement in clockwise (for positive *z*-direction) direction. So, the presented radiator has left-handed circularly polarization nature in the first band.

The Co and cross-pol normalized power pattern of the proposed array has been depicted on both orthogonal plane (yz and xz) as shown in Fig. 5. The depicted array is dual-polarized. In the first band, it shows circular polarization, while in the other band, it shows linear polarization. The presented FSS-loaded array is left-handed circularly polarized in the lower band. Figure 5a and b shows that LHCP components are 20–30 dB higher of RHCP components at boresight directions.

The Co and cross-pol normalized power pattern of the proposed array has been depicted on both orthogonal plane (yz and xz) as shown in Fig. 5. The depicted array is dual-polarized. In the first band it shows circular polarization, while in other

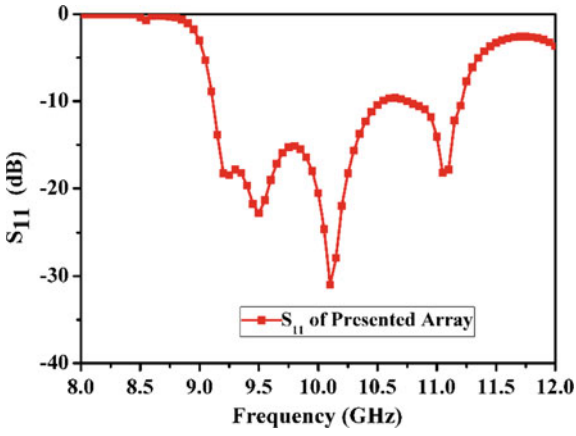

Fig. 2 S-parameter of array

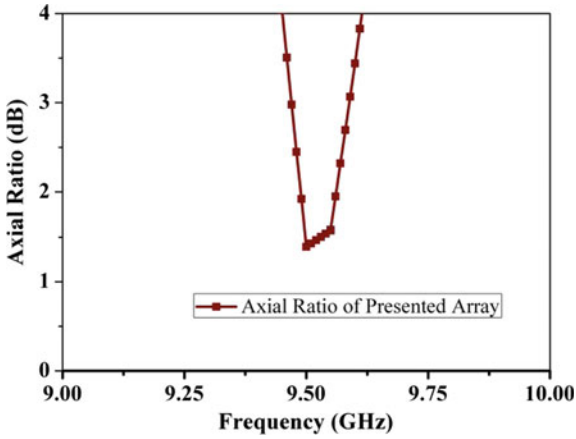

Fig. 3 Axial ratio of designed radiator in first band

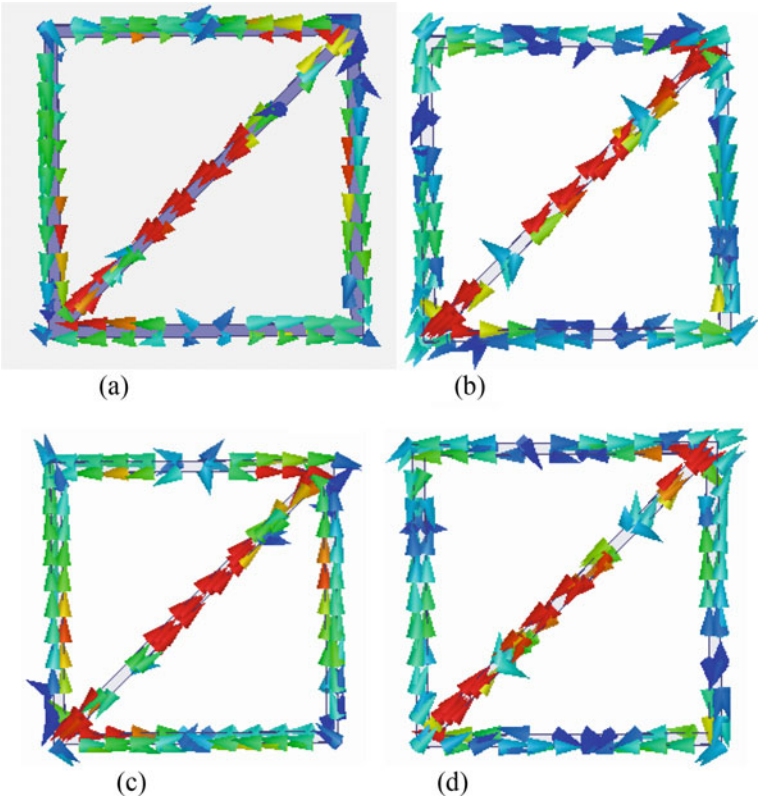

Fig. 4 E-field rotation at various time instants

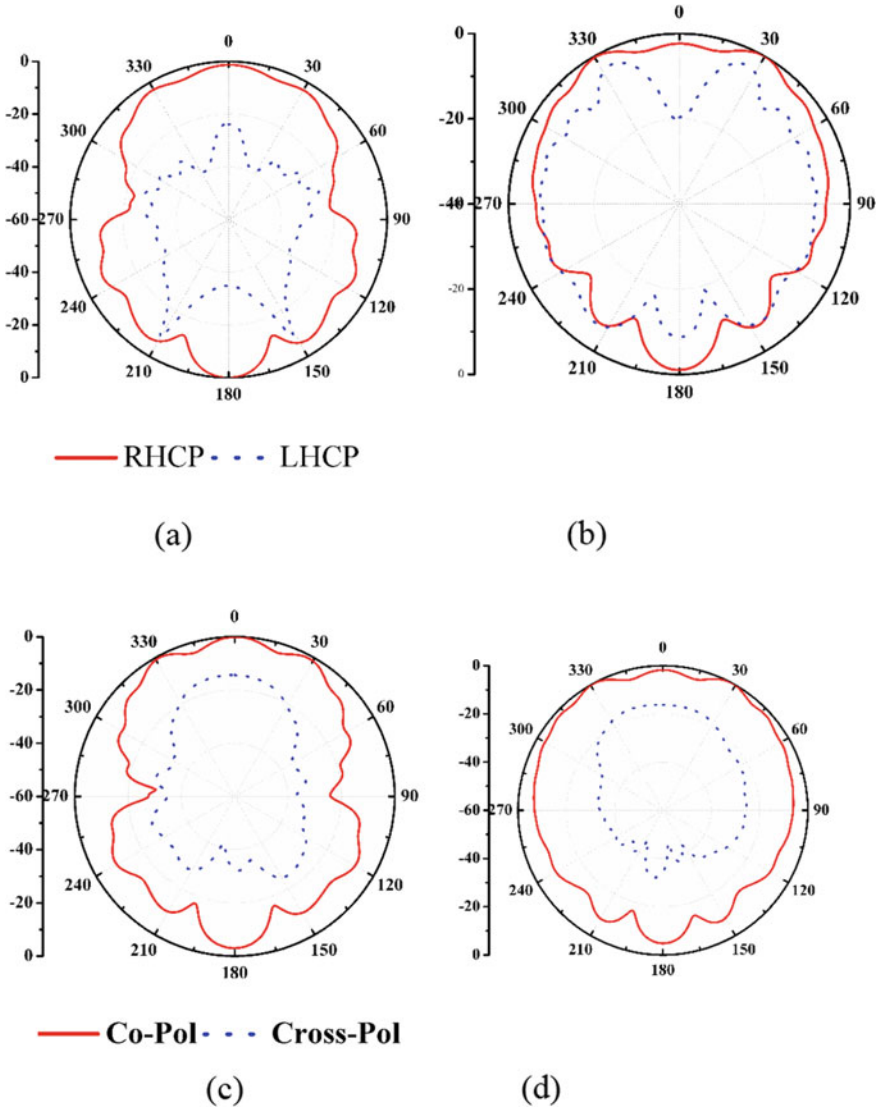

Fig. 5 Normalized power pattern of presented array **a** at 9.5 GHz in xz, **b** at yz-plane and 11.5 GHz **c** at xz **d** at yz-plane

band linear polarization. The presented FSS-loaded array is left-handed circularly polarized in the lower band. Figure 5a and b shows that LHCP components are 20–30 dB higher of RHCP components at boresight directions.

Total gain plot of the dual-polarized array is shown in Fig. 6. Gain of presented array has been also plotted at the resonant frequency. Figure 6 concludes that the gain

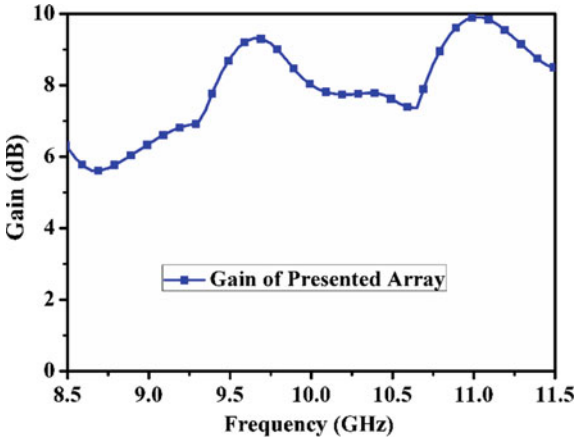

Fig. 6 Gain of presented radiator

of metasurface-loaded array at two distinct matching frequency is 6.5 and 8 dBi. The insertion of metasurface and FSS improves the gain of overall array by 1.5–3 dBi.

4 Conclusion

A FSS and metasurface embedded high-gain dual-band dual-polarized array has been proposed in this article. A three octal shape SRR are kept in the E-plane of waveguide. The array has been analyzed using HFSS (version 15).The presented antenna shows circular polarization in the first band, while linear vertical polarization is observed in higher (second) band. The gain of presented FSS and metasurface-loaded array is 2–3 dB greater than the traditional waveguide aperture arrays.

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Design and Implementation of Direct Memory Access & Compression in PSoC5LP

Athira Gopinath, Chandni Arun, and Aravind Hanumanthaiah

1 Introduction

A reliable streaming of sensor data is very critical for a disaster management application like forest fire detection and landslide early warning system. It becomes challenging especially when it is deployed in a remote location [1, 2]. The size of the data has to be accounted when transmitted through a communication module, since the bandwidth of the module is fixed. Also, there can be data loss, when the CPU of the processor is allocated with several processing tasks on complex signal processing algorithms. This is because the microcontroller executes the code in the sequentially and ADC need to wait until the microcontroller reads the value from the output register of ADC. Since every data is very crucial in disaster management, we cannot afford to lose data. The selection of an embedded processor or a controller plays a significant role in designing an efficient system. Conventionally, general processors [3] are used in most of the applications due its low cost, ease of implementation, and availability. Some of the high-end processors has DMA features and can run at high speed.

PSoC series is likewise an alternative that simplify large portion of novel preference which is further useful for researchers, designers, developers, and engineers to facilitate their works. It is designed in such a way that both hardware designing besides the product of software development is applicable. Some more com-

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plicated applications related to anti-aliasing filter, ADC, DMA implementation, and along with different communication modes which can be simply designed and reconstructed according to the changes in the operations.

PSoC5LP is selected and used in this work to design and implement the ADC, DMA, compression, and UART. In order to prevent the data loss, DMA [4] is considered in the design and implementation. Direct Memory Access (DMA) helps to transfer the data from source to the destination without the intervention of CPU. It is a highly recommended to reduce the size of data to be transmitted.

In Fig. 1, it explains the basic block diagram of a real-time system. The data sensed by the sensor will be fed to the ADC register. The ADC will convert the analog signals to digital values. The digital values will be fetched by the DMA. Data will undergone compression and sent to the network. When it is received by receiver, the data get decompressed back and fed to the visualization unit. In this paper, it describes the role of DMA to reduce the workload handled by the CPU. This focuses mainly on implementation of DMA on PSoC5LP along with the implementation of compression algorithm which is handled by CPU, thus to understand how the tasks can be improvised by comparing the performance with and without having the intervention of DMA.

Section 2 explains the related works; Sect. 3 described the processor descriptions. In Sect. 4, it details the implementation of DMA in PSoC 5LP, and Sect. 5 conveys the steps to need to follow for the implementation DMA in PSoC5LP. Data compression algorithm is explained in Sect. 6. Section 7 gives the discussion of the work. Section 8 concludes the paper work.

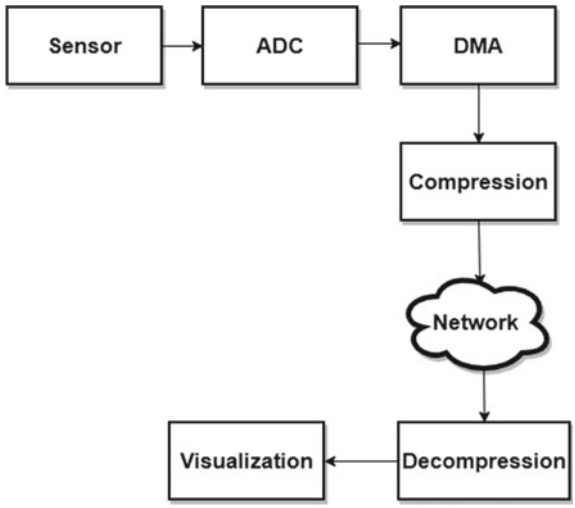

Fig. 1 Basic block diagram of a remote monitoring system

2 Related Works

Soheila Gharavi [5] et.al designed a five-stage parametric DWT and 1024- FFT with digital filters in PSoC5LP and compares it with the FPGA, ASIC, and DSP chip in terms of power efficiency. With this work, the paper proved that PSoC5LP are more flexible in designing, highly accurate with complex algorithms, good providence in hardware overhead, and efficient utilization of power.

Tuyen Phong Truong [6] et.al proposed a re-configurable hardware development stage for power broad-field remote sensor systems. Here, the work is designed and implemented using a configurable hardware architecture for isolated sensing structures based on PSoC and long-range (LoRa) technology. This paper highlights the evaluation of the functional claims and efficiency utilization of the design.

Mishra [7] et al. described a comparative study of nine popular IoT prototyping development platforms and also analysis based on the seven aspects of IoT application prototyping in terms of computational power, cost, reliability, learning curve, OS support and ease of programming, and time to market.

Krauss et al. [8] inquired into the feasibility of using the Arduino platform in real-time feedback control. This paper also checks the digital communication delay in the performance of the system by using a combination of serial echo tests and Bode plots. It gives additional information on to set the Arduino's timer for fast PWM and achieve a virtual ground for bipolar and A/D conversion.

Oza [9]et.al designed and developed a robotic hand with the aid of Arduino UNO board with two phases. The first phase includes the movement of the movements of fingers using glove, and the second phase will concentrated on the movement of the wrist. The design includes a flex sensor which is attached to the fingers. The configuration of the flex sensor attached to the finger, and the angle calculation for the rotation servo motor will be the trickiest part of this work.

Mohiddin [10] et al. proposed a sensor grid system using PSoC. Routing is achieved by incorporating CYFI RF module to transmit the data. Since the PSoC integrates all the programmable digital/analog and microcontroller blocks, all the signal processing tasks can be performed in to an individual chip which will results in a miniature footprint for the main hub. Also the sensor networks can be build and tested in different topology.

3 Differences Between a Conventional SoC and PSoC

3.1 Programmable System on Chip

System on a chip (SoC) is an integrated chip which usually has a microcontroller with analog and digital blocks which can be programmed on the same fabric.

Programmable system on chip [11] from Cypress Semiconductor is a popular SoC family used for industrial applications. Similar to an SoC, PSoC also has a

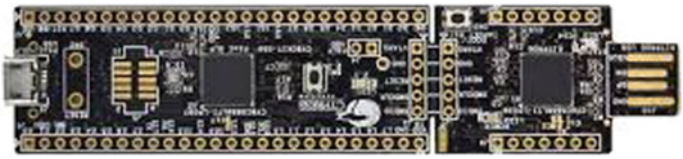

Fig. 2 PSoC5LP[12]

microcontroller-coupled digital and analog blocks. But, the PSoC platform offers the GUI and API to program the analog and digital blocks. This feature is discussed in the paper which eases out the development process.

Due to its high flexibility, performing complex task and its energy efficiency will make the PSoC platform to do best in commercial markets.

PSoC5LP: For our work, PSoC5LP based development board is used to implement DMA and compression technique. PSoC5LP in Fig. 2 shows the PSoC architecture that has a 32 bit ARM Cortex-M3 processor with a DMA controller which can clock the speed up to 80MHz. Enabling excessive less power beside industry's expanded voltage domain, whereas analog and digital programmable blocks implement characteristic functions and also flexible enough to perform routing attributed to analog and digital function to either pins. It has a 24 channel Direct Memory Access which helps to reduce the burden over CPU. PSoC5LP kit is shown in Fig. 2.

DMA implementation is possible in high-end series of PSoC family. This feature is integrated in such way that the designers can easily do the implementation by giving the inputs to the DMA wizards. DMA wizard will generate a code and based on that will help to reduce the manual error occurred during the programming and also saves the time required to complete the coding part. PSoC5LP family of devices has better performance in terms of speed while processing, low-power operations, feature compatibility, and quality functions to execute the applications.

4 Implementation of DMA in PSoC5LP

A peripheral to memory, DMA implementation approach is designed and developed, in which the data is taken from ADC and passed to a memory array bypassing the CPU. This will help reduce the CPU interventions and can be allocated to the ALU for other functions rather than collecting the data from the ADC [13]. For the implementation of DMA in PSoC 5LP, the source and destination address should be specified. In this case, ADC will be the source and memory array will be the destination. When the ADC completes its conversion, the EOC signal will initiate the DMA. It will enable the DMA to pass a channel request. On each DMA request, the DMA will fetch the data from the ADC output register and write that to the destination memory address. Further, it will increment the destination memory address and also decrements the transfer count after each burst. This will happen until the transfer

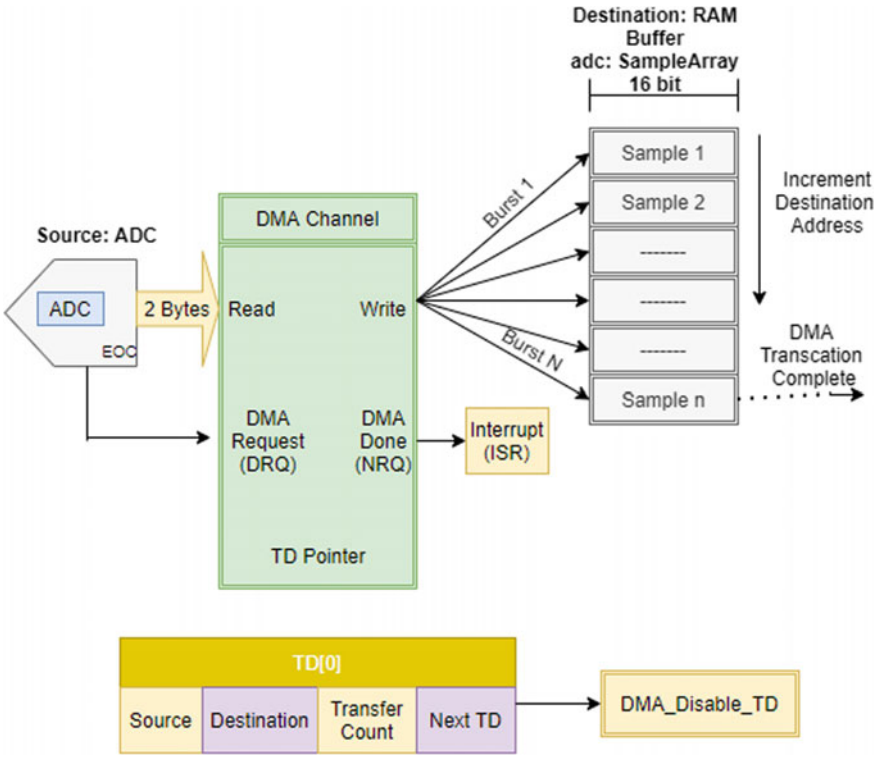

Fig. 3 Architecture of DMA

count is decrements to zero. Once the transfer counter decrements to 0, which will produce a transaction finished signal at the NRQ terminal of the DMA component, which triggers the ISR_DMA_Done interrupt. Figure 3 depicts the architecture of peripheral to memory DMA.

5 Start the DMA Wizard

5.1 Selection of DMA Channel Wizard

(i) Select the DMA channel to be designed in Fig. 4.

- Give name to the PSoC project creator
- Name the DMA component in the project

(ii) Select the DMA transfer global settings in Fig. 5

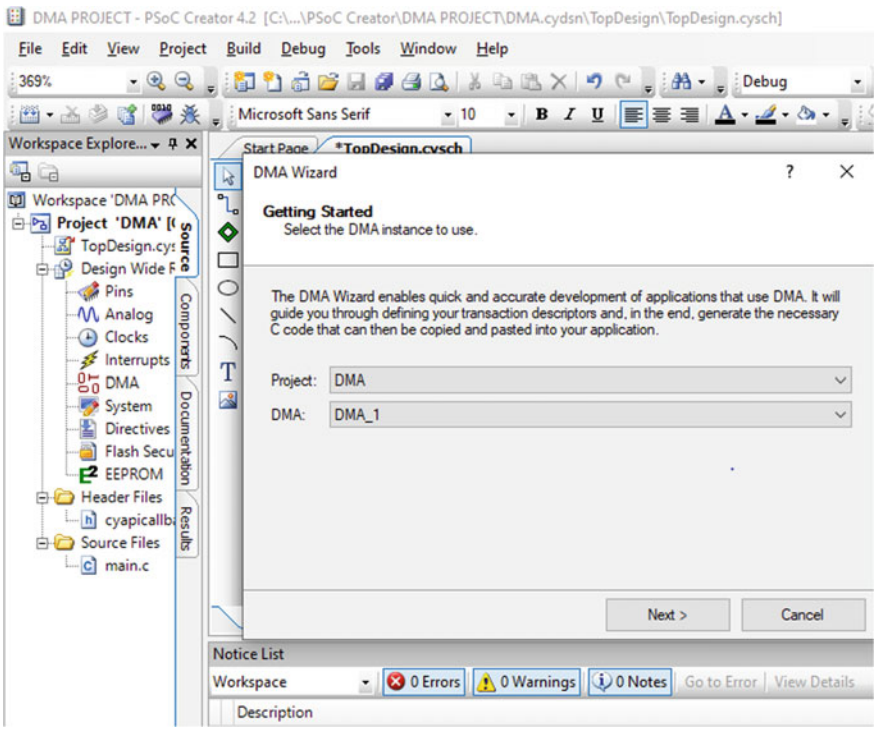

Fig. 4 Select DMA channel

- The upper 16 bits of the source address and destination address is designed in channel configuration register, respectively.
- Bytes per burst are defined as number of bytes to be carried in a single burst while transferring the data.
- Burst will decide whether a single burst depends upon the separate request. Therefore, each burst obtains a request.
- There are 1–128 number of transaction descriptors which are correlated with the DMA channel.
- Single chain or loop refers as what 'Next TD' for the last TD in the chain. If single chain, the next TD is DMA_DISABLE_TD (0xFE). If loop, it is the first TD.

(iii) Characterize transaction descriptors for the DMA channel in Fig. 6

(iv) Duplicate the code created by the DMA wizard in Fig. 7

- Once the configuration of DMA channels and TD are finished, the wizard will create code for the DMA channel. This code comprises the DMA channel and the TDs configuration, and it is generated in a window in the DMA wizard dialog [14]. The working of DMA in PSoC5LP is depicted as flowchart in Fig. 8.

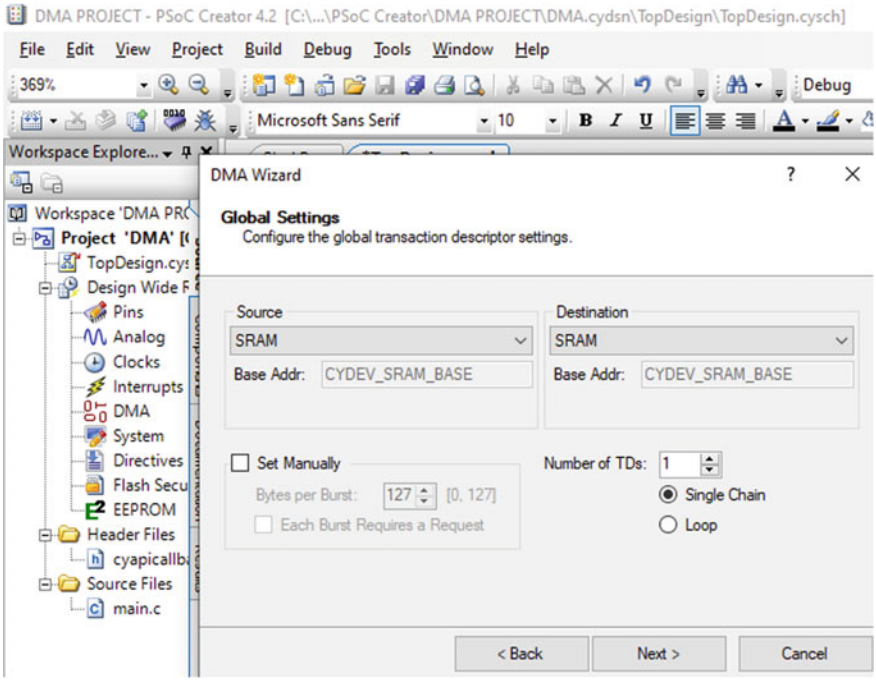

Fig. 5 Global settings

6 Implementation of Compression Algorithm

The compression [15] of data can reduce the data storage required for an optimized system for monitoring, analyzing, and detecting the events. It will help to increase the storage capacity, transfer speed, and bring down the hardware requirements for storage and bandwidth required for the transmission. The compression methods can be of two types, which are lossless compression and lossy compression. In this paper, lossless compression approach is adopted to compress the data collected from the sensor because the data loss is not acceptable in this work. A combination of delta and run length encoding is used as lossless compression techniques [16] to reduce the data points required to store and transmit. The blocks involved in the compression are shown in Fig. 9.

The data compression is selected based on the type of data used for transmission. It is one among the important factors which affect the compression ratio. In this application, accelerometer data are considered. The accelerometer shows a large variation when it capture any vibrations or caused due any sort of inclination. Based on these studies, delta encoding is best suited for the smooth data points. In order to minimize the repeated data points, the run length encoding is applied after the

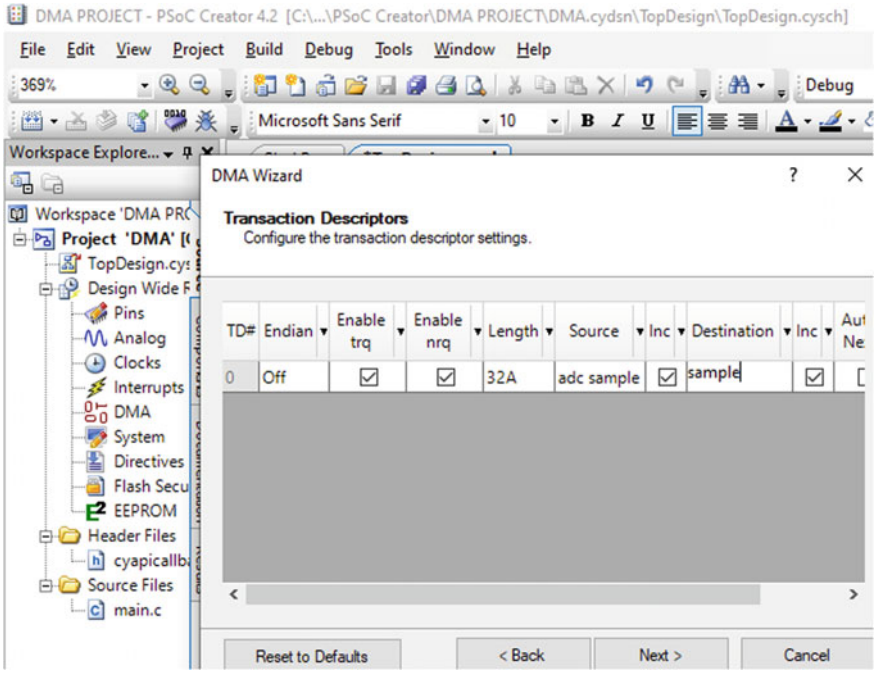

Fig. 6 Add transaction descriptors

delta encoding. Both encoding algorithms will help to enhance the data compression ratio by reducing the data size to be transmitted. Also these two are simplest lossless algorithm which will reduce the complexity of the entire process.

6.1 Delta Encoding

Delta encoding is a kind of simplest compression algorithm used to reduce the number of bits stored and transmitted. It is mostly preferable for the smooth data like slow varying data which gives small differences between the consecutive data points [17]. In delta-encoded algorithm, it will store and transmit the delta values instead of the original values. The encoded file contains the first data sample as such in the original data file and differences of the consecutive data samples. The delta encoding find its application in software revision control system, transverse file variations, enhancing HTTP working and systematic Web page storage. Figure 10 shows the working of delta encoding with an example.

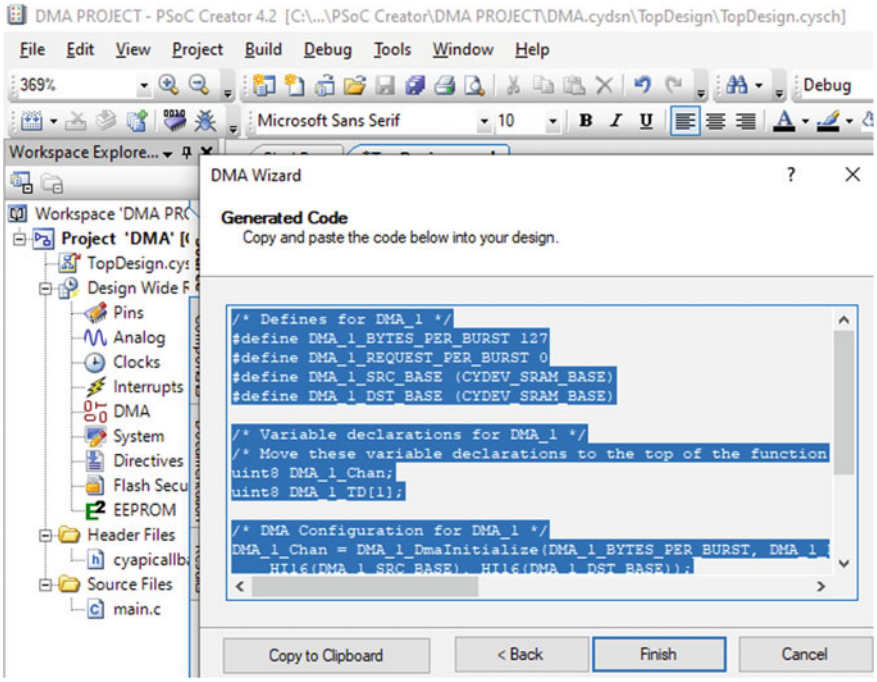

Fig. 7 Generated code

6.2 *Run Length Encoding*

Run length encoding method is a common lossless method adopted mostly in the data files having the repeated data points. In the RLE encoded file [18], it will replace the repeated data points with the count of repetition and copy of the data point itself. Thus, it reduces the data to be stored and transmitted. It will give prominent compression ratio only if it contains the repeated data points. Otherwise it can give a low compression ratio, or sometimes the compressed file size [19] is even more than the size of the original file. RLE is widely used in TIFF and PDF files. Figure 11 shows the working of RLE encoding with an example.

6.3 *Delta and Run Length Encoding*

In the combination of delta and RLE encoding approach [20], primarily the data samples are passed through the delta encoder and the delta encoded data samples are fed to the input RLE encoder [21]. The benefit of using combined algorithms is that the compression ratio can be effectively increased without any complex efforts. The

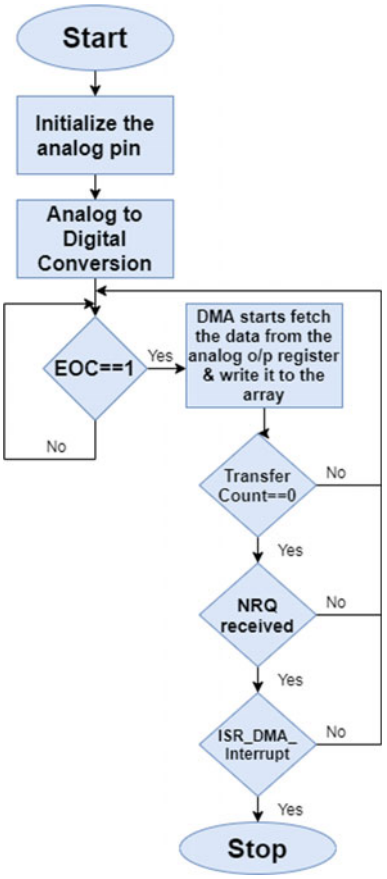

Fig. 8 Flowchart of DMA implementation in PSoC5LP

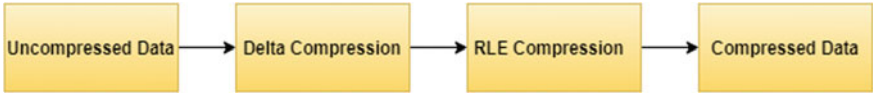

Fig. 9 Basic block diagram of lossless compression

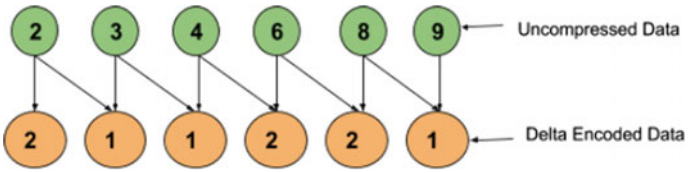

Fig. 10 Delta encoding

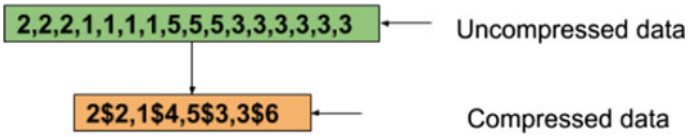

Fig. 11 Run length encoding

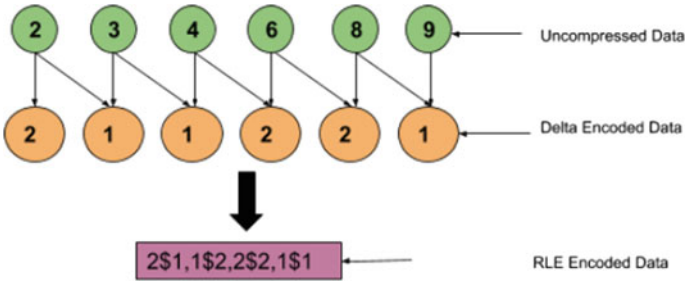

Fig. 12 Delta run length encoding

accelerometer data is fed through the delta encoder, which will take of the differences between the consecutive number. In accelerometer data, the data points are almost smooth except when it detects any events. But the number of data points is still same as that of the original file with the delta values of the consecutive data points. In order to reduce the number of data points, the delta encoded values are fed to the RLE encoder. Since the data is almost smooth, the delta encoded file contains more repeated delta values. When these repeated data fed to the RLE encoder, this will definitely increase the compression ratio by replacing the repeated delta values with its count of the repeating delta points and copy of the delta point. Delta RLE encoded data are shown in Fig. 12. The algorithm provides a data compression of almost 50% of the original data size.

7 Discussion

This work mainly focuses implementation of DMA feature and compression technique in the data acquisition system and explore the advantages of using DMA for fetching the ADC data rather than the conventional way. In a conventional system, the ADC values are directly given to the CPU for data processing, and then, the processed data is transmitted using an appropriate communication protocol. Here, the CPU performs most of the task from the data acquisition, processing and transmitting. This will increase the CPU overhead, especially when the sampling rate of the data is high. The DMA reduces the CPU overhead which will help the CPU to do other tasks. Also, it will avoid the data loss that can occur due to high sampling

rates. The DMA fetches the data from the register, while the CPU performs data compression.

The compressed data is sent using the UART communication protocol. Since the research mainly looking into the remote sensing, that requires a huge amount of data to be transmitted for analysis. Each communication module have constraints to transmit the size of data. This is solved by implementing the compression techniques in the CPU code that reduces the size of the data

The development boards like Arduino is not fast enough and also does not have robust and dynamic DMA features as PSoC.

8 Conclusion

This paper shows the implementation of DMA and compression techniques in PSoC5LP. The DMA enables the parallel processing, while CPU compresses the sensor data, DMA acquires the data from the sensor. Thus, the system can avoid the delay that usually occurs due to the sequential execution of code in the CPU. This system can be beneficial in the applications that has high sampling rate.

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Security of Medical Images Using DWT and SVD Watermarking Technique

Kumari Suniti Singh and Harsh Vikram Singh

1 Introduction

Advancement of multimedia technology in addition to communication technology boosts the capacity of handling medical information and also sharing it to remote areas, but also some risks are introduced for electronic patient records and therefore requires secure information management systems [1]. To avoid the risk and secure, the medical images between the exchange process security techniques must be able to provide confidentiality, authenticity, and integrity of a medical image [2]. Confidentiality shows that only the approved clients can able to get the transmitted image. Integrity shows the image received is uncontrollable by any unapproved user. Whereas, authenticity ensures image origination from the specified source and is associated with the patient specified. So, these requirements must be fulfilled to accomplish secure and reliable medical image transmission. Cryptography and watermarking techniques are mainly used to secure medical images [2]. Whereas, the watermarking technique is most widely used in data hiding and security. Digital watermarking mainly refers to directly embedding the information into some carrier. The cryptography approach utilizes hashing functions, symmetrical encryption, and digital signatures to provide security [2]. Whereas, security can be achieved by using robust and fragile watermarking techniques. Robust watermarks are able to resist common signal processing and attack [2]. Unlike robust watermarking, fragile watermarking cannot be able to resist signal processing attacks and tampering. So, to utilize the effect of both methods, i.e., cryptography and watermarking, crypto-watermarking algorithms are developed and utilized. There are different types of

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crypto-watermarking techniques that have been proposed. These techniques can be classified into reversible, irreversible, and region based. Region based is further classified into a region of interest (ROI) and region of non-interest (RONI) [3]. While hiding the information into ROI section, there is a necessity of care to avoid the degradation of image. Also, any tampering must be avoided to recover the original data in order to attain correct diagnosis and if needed for retransmission [3]. The recovery data has been embedded inside the RONI region. Digital watermarking can be classified as a carrier and its method of representation. Digital watermarks could be taken as video watermarks, audio watermarks, image watermarks, and text watermarks [4]. In recent years, the application of watermarking has been increased significantly and different methods are used for the security of medical images so far. Some most frequently applied methods are classified and described hereafter. Al-Haj et al. [2] proposed a region-based multi-algorithm using various watermarking techniques in both domains (i.e., frequency and spatial). To assure confidentiality and authenticity, RONI is also used in this proposed method by using DWT and SVD techniques. Eswaraiah and Sreenivasa Reddy [3] proposed a watermarking technique, which is block based and fragile to circumvent the distortion inside ROI and assures the integrity of it. In this method, image has been partitioned into ROI pixels, RONI pixels, and border pixels. So, the data to be recovered has been embedded into RONI. Navas et al. [5] proposed an electronic patient report (EPR) hiding technique using integer wavelet transform. The proposed method shows the result in terms of higher PSNR and high EPR with weighted peak signal to noise ratio (WPSNR). Roy et al. [6] give a brief review about different aspects of biomedical image security and different methods to provide medical image security. Jero et al. [7] proposed a method using DWT and SVD. DWT decomposes the image, and SVD embeds the data into decomposed ECG signal. In this, the embedding of information has been gained by replacing the singular value (SV) of a decomposed image by SV of the secret information. Different evaluation matrices have been used to measure the performance of applied algorithms. Kaw et al. [8] proposed reversible and high capacity data hiding technique to secure embedded EPR available in the image using OPR, which denotes optimal pixel repetition. Each pixel of the host image is altered using OPR into 2 * 2 blocks to ensure reversibility of pixels in a 2 * 2 blocks to attain altered values. In this, a lookup table is generated corresponding to 16 possible pixel values. İn this [9], a secure, robust and lossless image watermarking using DWT and DCT is given, which provides the privacy of patient data. DWT is applied to partition the image into sub-bands (i.e., LL, LH, HL, and HH). After decomposing the image, DCT has been applied on the HH frequency component. The adaptive scaling factor is computed, and mean is calculated. The scaling factor is multiplied with watermarked co-efficient to obtain new watermark co-efficient. Then, new watermark co-efficient is added. At the end, inverse DCT is used to attain watermarked image. Memon et al. [10] proposed a hybrid watermarking method using embedding a watermark in RONI region for achieving image security. Firstly, the information separated is inserted into RONI so that it can be used later in the procedure of recovery of the host image. This method evaluates WPSNR for equality measure. Kumar et al. [11] provide a spread spectrum watermark algorithm using DWT. This algorithm has been

used to embed watermarks like patient records, source of identification, and digital signatures of doctors in binary format to secure the image information. The results show the performance of algorithm as to gain factor, watermark size, and level of decomposition of sub-bands.

The rest of the paper is arranged as: Different Security Techniques used for medical images is given in Sect. 2. Methodology used for image security is presented in Sect. 3. Results have been demonstrated in Sect. 4, and conclusion is presented in Sect. 5.

2 Different Security Techniques Used for Medical Images

The recent advancement in communication technology has increased the quality of health care services. Telemedicine makes possible the exchange of medical information among the doctors and hospitals situated across the entire world. However, telemedicine has also some drawback since it gives ease for intruders to interrupt and tamper the medical data because of exchange on public networks. Hence, the securities of medical images are necessary for correct diagnosis and to avoid any kind of tampering. To assure secured exchange of medical images, three criteria must be fulfilled: confidentiality, integrity, and authenticity [12]. Presently cryptography and watermarking are most frequently used to furnish these security measures [13, 14]. Watermarking has been performed in three common steps like watermark generation, watermark embedding, and watermark extraction as given in Fig. 1.

Watermarking scheme uses different domain such as spatial domain and frequency domain. Spatial domain is simple and straight forward to use but not robust and also faces difficulty in surviving attacks [6, 15]. Transform domain or frequency domain is robust in nature, and information is embedded in transform co-efficient. Whereas, transform domain is robust in nature and information is embedded in transform co-efficients. Transform domain uses different wavelet transform: discrete wavelet transform (DWT), discrete cosine transform (DCT), singular value decomposition (SVD), etc. Each transform has its specific property. If more robustness is required,

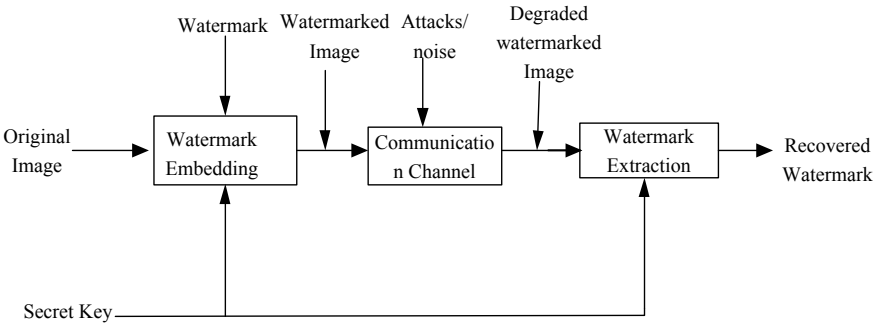

Fig. 1 Block diagram of digital watermarking

DWT is most appropriate among the three transforms. Whereas, for more fragility, DCT is the best suitable method [15]. Digital watermarking can be also classified into two groups: reversible watermarking and robust watermarking.

2.1 Discrete Wavelet Transform

DWT has achieved very good attention in the image processing research work because of multimedia image representation capabilities. It is the most widely used for image decomposition. It gives approximation and detail coefficients. Which can be written as LL, LH, HL, and HH [16]. Where LL represents approximation and LH, HL, HH represents (horizontal, vertical, and diagonal, respectively) detail coefficients. LL is low-frequency component of an image which contains most of the energy in the image. The decomposition level can be increased according to the need of an application. Three-level DWT decomposition is given in Fig. 2.

The 2D-DWT of an image $I(p, q)$ of size $P \times Q$ can be calculated as Eqs. (1) and (2) [17].

$$w_{\varphi}(j_0, s, t) = \frac{1}{\sqrt{PQ}} \sum_{p=0}^{P-1} \sum_{q=0}^{Q-1} I(p, q)\, \varphi_{j_0,s,t}(p, q) \tag{1}$$

$$w_{\psi}(j, s, t) = \frac{1}{\sqrt{PQ}} \sum_{p=0}^{P-1} \sum_{q=0}^{Q-1} I(p, q)\, \psi^{i}_{j,s,t}(p, q) \tag{2}$$

where $i = \{H, V, D\}$, j_0 is starting scale, $w\varphi(j_0, s, t)$ gives approximation coefficients, and $w^{i}_{\psi}(j, s, t)$ gives detail coefficients for $j \geq j_0$.

Inverse 2D-IDWT is obtained by Eq. (3).

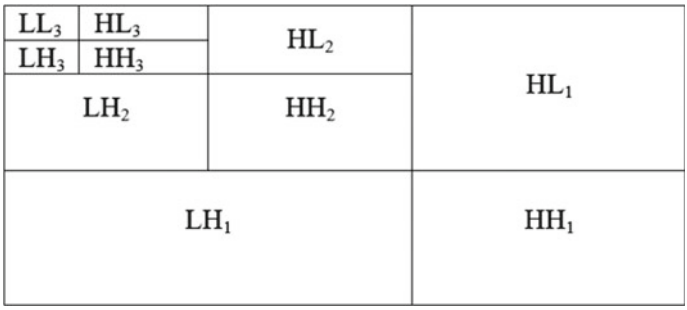

Fig. 2 Three-level image decomposition using DWT

$$I(p,q) = \frac{1}{\sqrt{PQ}} \sum_{s} \sum_{t} w_{\varphi}(j_0, s, t)\, \varphi_{j_0,s,t}(p,q) + \frac{1}{\sqrt{PQ}} \sum_{i=H,V,D} \sum_{j=j_0}^{\infty} \sum_{s} \sum_{t} w_{\psi}^{i}(j,s,t)\, \psi_{j,s,t}^{i}(p,q) \tag{3}$$

where $\varphi_{j_0,s,t}(p,q)$ and $\psi_{j,s,t}(p,q)$ represent discrete variable functions for $p = 0, 1, 2, \ldots, P-1$ and $q = 0, 1, 2, \ldots, Q-1$.

2.2 Singular Value Decomposition

SVD is a widely used tool for mathematical solutions for image processing and signal processing application. It is used frequently in filtering, compression, and noise estimation calculations [18, 19]. It gives a factorized form of rectangular matrix either it is real or complex. It gives a product of matrices of rectangular matrix with different characteristics, which helps in image processing in transform domain [20]. Let M be a matrix of corresponding image with m rows and n columns, then SVD of M be given as Eqs. (4) and (5).

$$M = U * S * V^T \tag{4}$$

$$M = [U_1, U_2, \ldots, U_m] \times \begin{bmatrix} \lambda_1 & - & - & - & 0 \\ | & \backslash & & & | \\ | & & \backslash & & | \\ | & & & \backslash & | \\ 0 & - & - & - & \lambda_m \end{bmatrix} \times [V_1, V_2, \ldots, V_n] \tag{5}$$

where S, U, V denote diagonal matrix and the orthogonal matrices, respectively. S matrix is formed by λ_i Eigen elements, which is called singular values. $\lambda_1 \geq \lambda_2 \geq \cdots \lambda_r = \lambda_{r+1} = \cdots = \lambda_n = 0$. r denotes the rank of matrix S. Right singular vectors and left singular vectors are given by first r columns of V and first r columns of U, respectively.

Matrix M can also be written as Eq. (6),

$$M = \sum_{i=0}^{r} \lambda_i * u_i * v_i^T \tag{6}$$

SVD contains the majority of image energy in its singular values. SV also provides good stability of an image [21].

2.3 *Medical Imaging Security Requirements*

In medical image security, various aspects are considered to properly secure the image. Basic security requirements are given below [15, 16]:

Privacy concern: Medical images are highly sensitive data that are used in diagnosis purposes. So, this is important to secure it from any unauthorized access and misuse to gain any kind of profit from it. At the time of using any technique, privacy concerns should be kept in mind [17].
Assured reliability: Medical images are very important for a correct diagnosis of any disease. So, accurate images are required for this purpose. Therefore, the practical implementation of any healthcare system without confidence in its reliability should not be deployed.
Maintaining authenticity: The received medical image should be authenticating and belongs to the specified patient and be received from a specified source [17].
Integrity measure: In a health monitoring system, continuous monitoring of images needs integrity for reliable results. Incomplete information may lead to difficulty in diagnosis [18].

3 Proposed Image Watermarking Technique

In the proposed method, we have applied a hybrid DWT-SVD based model as given in Fig. 3. The hybrid technique provides an imperceptible and robust algorithm, which

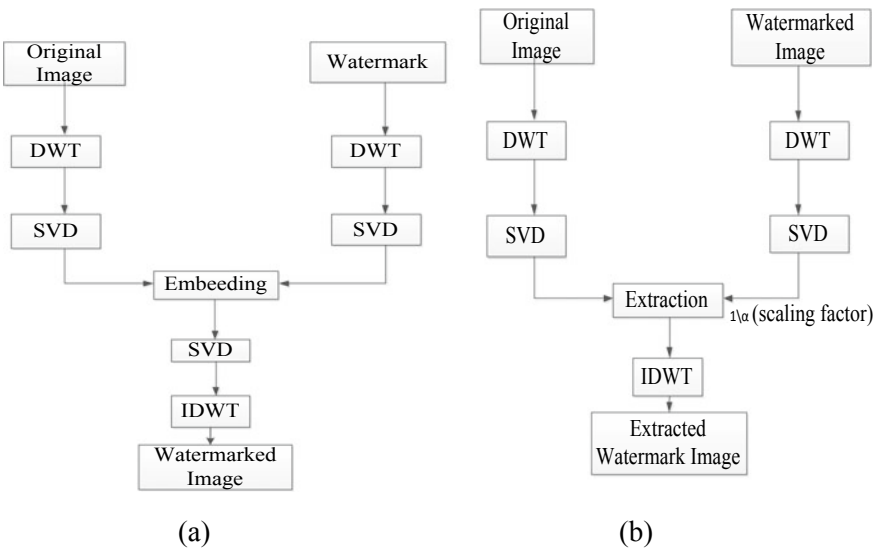

Fig. 3 Proposed model **a** watermark embedding, **b** watermark extraction

can sustain against various attacks. The methods of embedding and extraction have been given below:

Watermark embedding:

1. Host image I have been decomposed into 4 sub-bands, i.e., LL, LH, HL, and HH by using level 1 DWT transform.
2. Now SVD has been applied on LL sub-band as,

$$I_{\mathrm{LL}} = USV^{'} \tag{7}$$

3. A watermark image W is taken and decomposed at level 1 using DWT again as LL_1, LH_1, HL_1, and HH_1.
4. Now SVD has been applied on LL_1 as,

$$W_{\mathrm{LL}_1} = U_1 S_1 V_1^{'} \tag{8}$$

5. Embedding is performed by altering the singular values of LL sub-bands and further SVD is applied on modified singular values using scale factor α as,

$$S + \alpha S_1 = S_w \tag{9}$$

6. Modified DWT co-efficient of image is obtained by

$$I_{\mathrm{LL}}^{*} = US_w V^{'} \tag{10}$$

7. Now inverse DWT (IDWT) of level 1 has been applied on non-modified sub-bands and on the modified band (W_{LL1}) of image I to recover the watermark.

Watermark extraction:

1. Decomposition is applied on watermarked image using level 1 DWT, which gives 4 sub-bands as LL_2, LH_2, HL_2, and HH_2.
2. Now SVD has been applied on LL_2 as,

$$W_{\mathrm{LL}_2} = U_2 S_2 V_2^{'} \tag{11}$$

3. Modification in the singular values of LL_2 sub-bands has been done as,

$$(S_2 - S) \backslash \alpha = S_w^{*} \tag{12}$$

4. After that SVD has been applied on modified singular values as,

$$W_{\mathrm{LL}_1}^{*} = US_w^{*} V_1^{'} \tag{13}$$

5. Now inverse DWT (IDWT) is applied on non-modified sub-bands LH1, HL1, HH1 and $W_{\mathrm{LL}_1}^{*}$ to extract the watermark.

4 Results

The proposed algorithm is applied to grayscale images, size taken as 256 × 256. Also, a Grayscale image of size 128 × 128 is used as watermark for embedding and extraction using the proposed algorithm. The results are given in Fig. 4 and Table 1, which are analyzed based on PSNR and Structural Similarity Index (SSIM) parameters as below.

(a) PSNR: It is used frequently for the measure of the quality of the watermarked image. PSNR can be given as [22, 23],

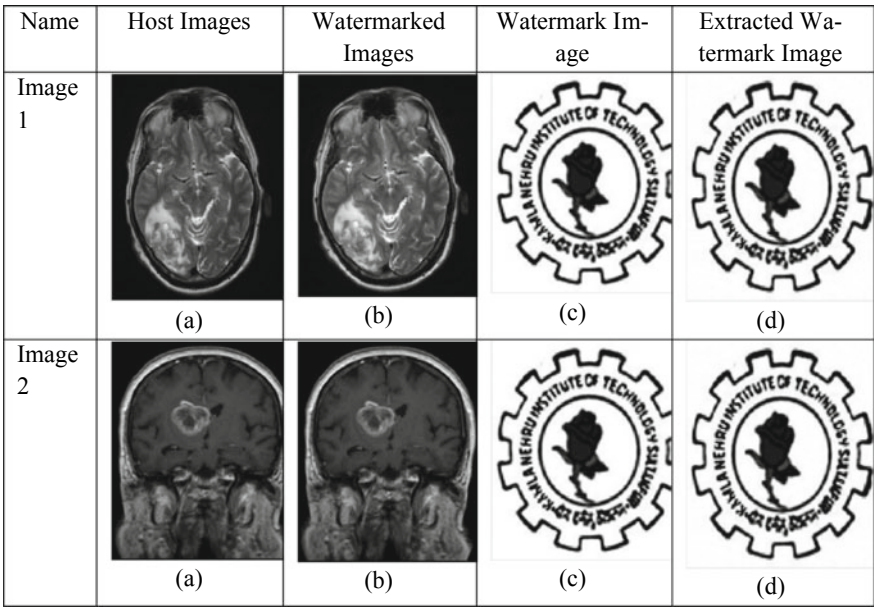

Fig. 4 Results of proposed algorithm. **a** Host images; **b** watermarked images; **c** watermark image; **d** extracted watermark image

Table 1 Comparison of PSNR and SSIM values at different scale factors using the proposed algorithm

Sr. No.	Original image	Scale factor	PSNR (dB)	SSIM
1	Image 1	0.01	47.489	0.998
		0.03	37.887	0.996
		0.05	33.467	0.995
2	Image 2	0.01	47.363	0.995
		0.03	37.911	0.991
		0.05	33.448	0.980

Table 2 PSNR and SSIM values at different watermark size using scale factor 0.01

Watermark size	Original image	PSNR (dB)	SSIM
32 × 32	Image 1	64.189	1.000
	Image 2	74.420	0.998
64 × 64	Image 1	51.562	0.999
	Image 2	51.205	0.996
128 × 128	Image 1	47.489	0.998
	Image 2	47.363	0.995

$$\text{PSNR}_{db} = 10 \log_{10} \left\{ \frac{255^2}{\text{MSE}} \right\} db \tag{14}$$

where MSE denotes Mean Square Error.

(b) SSIM: It gives a similarity measure between the original and watermarked image. SSIM is defined as [24],

$$\text{SSIM} = \frac{(2\mu_x\mu_y + c_1)(2\sigma_{xy} + c_2)}{(\mu_x^2 + \mu_y^2 + c_1)(\sigma_x^2 + \sigma_y^2 + c_2)} \tag{15}$$

where μ, σ, σ_{xy} shows mean, variance, covariance of an image, respectively, and c_1, c_2 gives stabilizing constants. The SSIM values of an image vary between 0 and 1. The SSIM value of similar images is near to 1.

From Table 2, we can observe that as the size of watermark increases, the corresponding PSNR value of the image decreases. The change in values occurs because of embedding more pixels in the original image, which results in an increase in MSE and a decrease in PSNR. PSNR is also calculated and compared by performing different attacks on a watermarked image using scale factor 0.01 as given in Table 3.

Table 3 Comparison of PSNR values after introducing attacks to watermarked image

Watermark size	Attacks	Watermarked image	PSNR between watermark image and extracted image (before attack)	PSNR between watermark image and extracted image (after attack)
128 × 128	Gaussian noise	Image 1	27.129	23.059
		Image 2	30.496	19.568
128 × 128	Salt and pepper noise	Image 1	27.129	22.984
		Image 2	30.496	26.827

5 Conclusion

Security and secrecy of the medical image data are one of the main concerns these days. Without using proper measures of security, it is not practical to deploy it in any remote healthcare system. Medical images may suffer from various issues like noise artifacts, poor contrast, etc. Medical images contain significant information of a specified and any tampering of image data causes difficulty in diagnosis because of tampering doctor would not be able to identify the diseases. Several methods are used to secure the medical images. In this paper, we used DWT- and SVD-based model to secure the image. The performance of the algorithm is evaluated by using different performance evaluation parameters. The result above shows that this method gives a good PSNR value and secures the medical images efficiently with good perceptual quality and also withstand against several attacks. Further, this method can be utilized by adding other transform techniques. Also, this technique can have extended for the use of colored medical images.

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Designing Multimodal Cognitive Model of Emotion Recognition Using Voice and EEG Signal

Ram Avtar Jaswal, Sunil Dhingra, and Javalkar Dinesh Kumar

1 Introduction

Emotion plays a major role to recognize human behaviour and identify health conditions of human, but emotions recognition is very challenging and difficult tasks in several respects. One of the major difficulties is that it is very hard to correlate signal patterns with a convinced emotional state in an accurate way. Moreover, emotion-relevant signal patterns may sometimes differ from person to person in different situation and environment.

Emotions are the feeling such as hate, anger, love, fear, trust, panic, etc., aroused from visual, audio stimuli or from any physiological activity and can be classified into two types on their origin primary (aroused in response of an event) and secondary (follows the effect due to primary emotions). Emotions play a vital role in humans to communicate with each other and can be expressed through facial expressions mainly. Through facial expression, one can communicate irrespective of the language they speak.

The major function of emotion is to give information to the individual about their interaction with the world. Robert Plutchik created a wheel of emotions which consisted of 8 basic emotions with its basic opposite

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Basic emotion	Basic opposite
Joy	Sadness
Trust	Disgust
Fear	Anger
Surprise	Anticipation
Sadness	Joy
Disgust	Trust
Anger	Fear
Anticipation	Surprise

Types of emotions: There are two types of emotions called positive emotions and negative emotions.

1.1 Negative Emotions

Negative emotions are those emotions that make you feel sad and helpless and can demoralize you which are given below.

Negative emotions
Sadness
Anxiety
Anger
Guilt
Shame/embarrassment

1.2 Positive Emotions

Positive emotions are emotions other than negative, i.e. they do not have any negative feeling towards their origin which are given below.

Positive emotions
Joy
Gratitude
Serenity
Pride
Amusement

(continued)

(continued)

Positive emotions
Inspiration
Love

1.3 Emotion-Based Intelligent Systems

Emotion-based intelligent systems have been used in different fields like e-health and e-learning. Smart city and smart home are based on computer-based intelligent emotion recognition and have great prospective in online gaming, customers' feedback assessment and in case of mental health monitoring. Researchers are now working to find accurate human emotions in order to maintain mental health problem, because in a healthcare system, patient's mental and physical states can be observed in real time with the help of emotion recognition method. The objective of emotion detection is to design and implement intelligent systems with HCI in different applications and appliances of defence. The emotion recognition can also be applied to find the state of soldiers, pilots and to enhance driving safety measure by monitoring the emotional state of the driver to prevent dangerous driving in public transportation.

1.4 Effects of Emotions on Human Behaviour

Behaviour is defined by how one acts and reacts to the things that he/she faces, which is further dependent on the mood of the individual which changes with time. One's mood is completely dependent on the state of mind of the person which is further dependent on the emotions that a person is going through at that particular time. Emotions also affect the choice one made in his/her life, for example, considering a person feeling frustrated because of not qualifying a test for the third time might make him give up hope and loose morale further he might give up and stop preparing for that test in the future.

1.5 Relation of Emotion and Cognition

There are many-sided connections among discernment and feeling, a few scientists accepted that feeling cannot happen without comprehension. The significant type of perception associated with feeling is the evaluation of the importance of improvements for the person. Regardless of whether comprehension is important to feeling stays an unsettled issue.

1.6 Detection of Emotions

Detection of emotion is what we do in our daily life without knowing it. Emotions of humans can be detected either verbally through emotional words or by intonation, facial expressions and body postures. Most of times humans do it through judging one's facial expressions mainly. There are computational methods that are developed for emotion recognition to train machines in doing so. There are several methods on which currently research is going on such as Emotional Recognition Questionnaire, heart rate variability, facial expressions, speech signal, EEG, EMG, ECG, EOG, keystroke dynamics and mouse pointer movement.

1.7 Affective Computing

Full of feeling figuring is a rising examination field that means to empower canny frameworks to perceive and decipher human feelings with the assistance of HCI, AI, intellectual science, neuroscience and neuropsychology. Full of feeling processing is the arrangement of strategies and acknowledgment of feelings from information in various modalities. Full of feeling figuring research for the most part comprises of opinion investigation with intellectual abilities to acknowledgment of feelings by applying various classifiers and highlights. Over the previous decades, AI analysts have endeavoured numerous issues to perceive, decipher and express feelings and conclusions.

2 Proposed Work and Methodology

The described methodology to design cognitive model is based on multiple bio signal and voice signal is composed of the following steps:

Bio Signal: A bio signal is every signal in active being that can be measured continuously and monitored. The term bio signal is used to refer bioelectrical signals, but it may denote both electrical and nonelectrical signals. Bio signals (EEG, ECG, Voice, EMG, EOG, etc.) are distinct, time domain continuous signal with scattered energy distribution.
Signal Acquisition: Signals can be acquired by placing electrodes on skin (EEG, EMG, ECG or EOG) or voice with any external microphone (transducer that converts voice into electrical signals) for different defined protocols or emotions.
Signal Pre-Processing: The acquired signal is contaminated with noises called artefacts (EMG, ECG, EOG in case of EEG, external sound signals in case of voice and power line noise); these are unwanted signals captured during the acquisition process. In order to extract some useful information from the acquired signal, we must remove these noises from them with the process called pre-processing. In

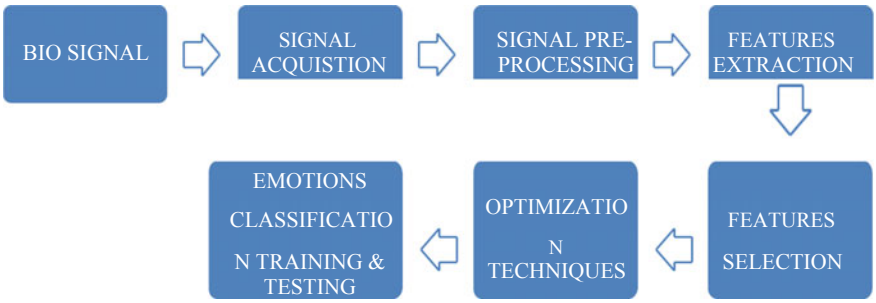

Fig. 1 A block diagram flow of the described methodology is shown below

pre-processing, bio signal is passed through filters to remove the noises, power line noise is removed by applying a filters, whereas noises in voice signal can be removed with hardware (secondary noise cancellation microphone).

Features Extraction: After pre-processing, features extraction of a signal can be done using wavelet transform or Hilbert–Huang transform or Fourier transform or short-time Fourier transform, etc. The time domain features are the basic statistical features such as nasty, median, standard deviation, power and RMS. Frequency domain features are power spectral density (PSD), cepstral coefficients, etc. Feature extraction is done to reduce the dimensionality.

Features Selection with Optimization Techniques: Classifiers are essentially machine learning algorithms that learn imperative information from features extracted from signals and then make grouping on the basis of these features. After extracting features, optimization of features can be done using optimization algorithms such as genetic algorithm (GA), particle swarm optimization (PSO) and ant colony optimization (ACO), grey wolf optimization (GWO), etc. This process is done to further decrease the dimensions. After optimization of features, classification is done using classifiers such as linear-discriminant analysis (LDA), support vector machine (SVM), nearest-neighbour classifier (kNN), neural network, CNN, etc.

Emotions Classification: Classifier is first trained with sample data/signal of known emotions/class and when classifier is trained, prediction of emotions can be done by feeding classifier with unknown class of signal/data and accuracy of classifier can be calculated (Figs. 1 and 2).

3 Literature Review

3.1 Previous Emotions Study Based on EEG

In 'Feature Extraction and Selection for Emotion Recognition commencing EEG', authors Robert Jenke et al. reviewed feature-extraction and feature-selection methods

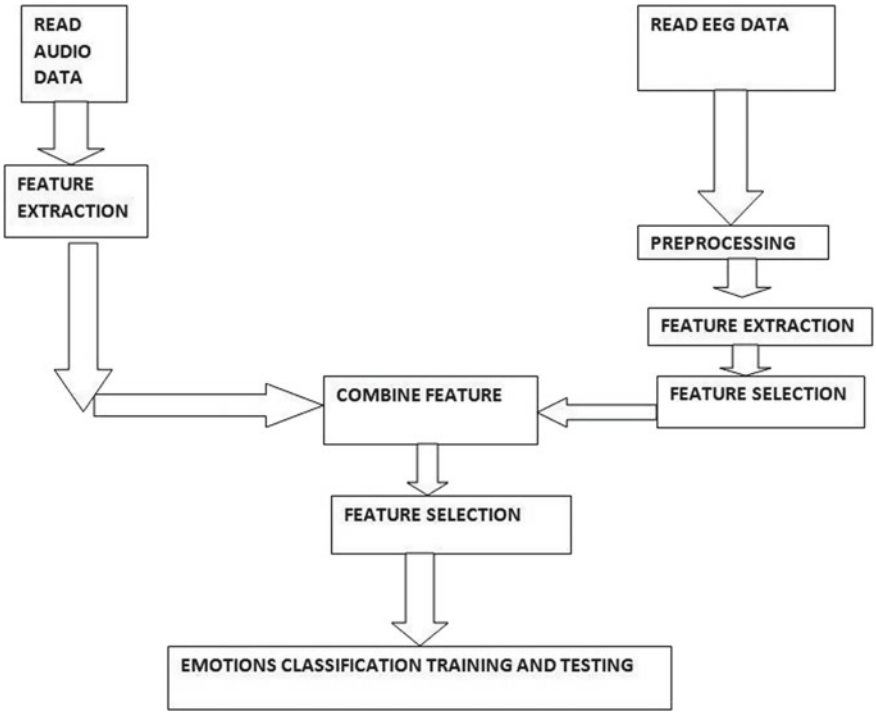

Fig. 2 A block diagram flow of the described methodology to detect emotions

used in more than thirty studies. Feature extraction methods used are fast Fourier transform (FFT), power spectral density (PSD), short-time Fourier transform (STFT), discrete wavelet transform (DWT), empirical mode decomposition (EMD), Higuchi Box Counting, etc., and feature selection methods such as Relief F, effect size-based univariate feature selection, effect size-based multivariate feature selection method, etc. Optimization of channels is also done instruction to find the best optimal channel for taken into consideration. To study results that feature extraction methods such as HHS, HOC and HOS have better accuracy, whereas multivariate feature selection methods are better than the univariate feature selection method. Also the parietal and centre-parietal lobes have optimal channels for feature extraction.

In another work, 'Human Emotion Recognition and Analysis to Response Audio Music with Brain Signals' authors Adnan Mehmood Bhatti et al. classified emotions such as happy, sad, love and anger using single electrode of different age group (15–25, 26–35 and 36–50 yrs) aroused by auditory stimuli (Rap, Rock, Metal, etc.) using time, frequency and wavelet (time–frequency) sorts. The classifiers used are nearest neighbour (kNN), support vector machine (SVM) and artificial neural network (ANN) with highest accuracy achieved 98% in 26–35 age group by ANN (MLP).

In 'Emotion Sorting from EEG Signals using Time–Frequency-DWT Features and ANN', authors Adrian Qi-Xiang Ang et al. achieved classification accuracy of 81.8% using ANN as a classifier for two emotions, happy and sad, with two electrodes (channels) using time domain, frequency domain feature and wavelet coefficients and IAPS are used as visual stimuli to evoke emotions. The features used are power, nasty, standard deviation, maximum frequency amplitude and DWT coefficients.

In another work, authors M. Sreeshakthy et al. reviewed the different feature extraction techniques in 'A Survey on Emotion Classification From EEG Signal Using Various Techniques and Performance Analysis' such as DWT, HOC, STFT and PCA used for EEG analysis. In emotion recognition, the highest accuracy achieved is 84.6% using wavelet transform feature extraction with RBF and SVM used as a classifier.

In evolutionary computation algorithms for feature selection of EEG-based emotion recognition using mobile sensors, authors Bahareh Nakisa et al. proposed a new framework for optimization of features using evolutionary computation algorithms and tested it on two public datasets (MAHNOB and DEAP 32 channel) and one new dataset attained with emotive insight (5 channel). The dataset was preprocessed using filters and independent component analysis (ICA), and then, a total of 45 features were extracted with time–frequency domain features. A comparison of five feature selection algorithms, namely ant colony optimization (ACO), genetic algorithm (GA), simulated annealing (SA), particle swarm optimization (PSO) and differential evolution (DE) is shown on the basis of time taken and accuracy from which GA achieved highest accuracy of 97.119% in 79 h on MAHNOB dataset with feed forward neural network (PNN).

Weinreich et al. [1] measured deviations of alpha frequency band in front lobe by using 16-channel EEG signals from 20 female and 8 male participants.

Hidalgo-Munoz et al. [2] studied EEG signals of 26 females during surveillance emotional images from IAPS. In this study, feelings were observed affording to the valence–arousal model by using used spectral turbulence (ST). Outcomes show that the left activist lobe has weighty activity during emotion elicitation.

Koelstra and Patras et al. recorded EEG signals from partakers conferring to the valence–arousal model by showing video staples in order to arouse emotions. In this study, PSD of EEG sub-bands was premeditated and active divisions were spotted from face videos of participants. Then, combinations of many features were applied. Hidden Markov model and Gentle Boost remained used as the classifiers. They showed that the blend of face videos and EEG signals enhanced the accuracy.

Lee et al. proposed an emotion recognition system established on fuzzy logic control. They used video staples to prompt emotions and recorded EEG signals from 12 contestants and extracted vibrant features from emotional states and 3D fuzzy GIST and 3D fuzzy tensor to extract brain.

Choppin1 has examined EEG signals to identify emotion, in order to precise their spirits. In toting, this revision has used NN to classify the EEG signals, and attained a precise cataloguing rate for different samples of about 64%, for three emotion classes and partial training datasets.

Musha et al. [3] explored EEG signals to recognize human emotions and mined cross-parallel coefficients between the EEG signal from dissimilar locations and calculated an 'emotion matrix' to transform factors into a four-element vector resembles to four basic emotions. The statistics in the vector signifying the strong particular emotion is found in the EEG signals. This study has evaluated the average accuracy range from 54.5 to 67.7% for each of four emotional states.

Heraz et al. [4] established model to envisage emotional states during learning. The best grouping accuracy was 82.27% for eight emotional states, using KNN (k-nearest neighbours) as a classifier and the bounties of four EEG components as features.

Chanel et al. [5] re-counted an average accuracy of 63% by using EEG signal with time–frequency data as sorts and SVM as a classifier to describe EEG signals into emotive states.

3.2 Previous Emotions Study Based on Speech

In 'Discourse feeling acknowledgment dependent on highlight determination and extraordinary learning machine choice tree', creators Zhen-Tao Liu et al. proposed outrageous learning machine (ELM) choice tree for discourse feeling acknowledgment. In the feeling arrangement, a choice tree is built for discourse feeling acknowledgment by contrasting the estimation of disarray degree among six sorts of fundamental feelings (i.e. nonpartisan, furious, shock, upbeat, dread and misery), in which ELM is embraced as the twofold classifier. They utilized Chinese discourse database from foundation of robotization of Chinese institute of sciences (CASIA) and showed that the proposition accomplished 89.6% acknowledgment rate overall.

In 'Discourse feeling acknowledgment: Features and order models', creators Lijiang Chen et al. proposed three-level discourse feeling acknowledgment model to group six discourse feelings, including bitterness, outrage, shock, dread, joy and sicken. Right off the bat, they extricated the highlights of the discourse signal including vitality, zero intersection rate, vitality times zero intersection rate, pitch, range centroid, range cut-off recurrence, relationship thickness, Mel-recurrence groups vitality. In this paper, they are embraced to plan four relative trials with Fisher + bolster vector machine (SVM), head part investigation (PCA) + SVM, Fisher + fake neural system (ANN) and PCA + ANN for grouping. They demonstrated that include a decrease in utilizing the Fisher standard is better than PCA.

In 'Discourse feeling acknowledgment Using Fourier Parameters', creators Kunxia Wang et al. proposed another Fourier boundary model for speaker-autonomous discourse feeling acknowledgment. Mel-recurrence cepstral coefficient (MFCC) and Fourier boundary highlights were separated for speaker-autonomous feeling acknowledgment. Fourier boundary highlights were assessed for speaker-autonomous feeling acknowledgment by utilizing support vector machine (SVM) and a Bayesian classifier. The examination demonstrated that Fourier parameter highlights are viable in describing and perceiving feelings in discourse signals.

In 'Discourse feeling acknowledgment utilizing concealed Markov models', creators Lay New, Say Wei Foo, Liyanage C. De Silva et al. proposed arrangement of enthusiastic condition of articulations. The framework utilizes brief timeframe LFPC for highlight extraction for feeling acknowledgment. Brief timeframe LFPC speaks to the vitality appropriation of the sign in recurrence groups. Ghostly examination shows that conveyance of vitality is subject to feeling classes and coefficients additionally give significant data on the basic recurrence of discourse. The outcomes show that normal exactness of 77.1% and best precision of 89% can be accomplished in grouping the feelings exclusively. The outcomes show better precision of 65.8% as contrasted and accomplished by human evaluation. The outcome additionally shows that the proposed framework with brief timeframe LFPC as the pointers of enthusiastic states and HMM as the classifier do fill in as a reasonable methodology for the arrangement of feelings acknowledgment of discourse.

In 'Review on speech feeling acknowledgment: Features, groupings schemes, and databases', Moataz ElAyadi, Mohamed S. Kamel, Fakhri Karray et al. proposed that discourse feeling acknowledgment framework has been given and three significant issues have been examined: the highlights used to describe various conditions of feelings, the characterization strategies and significant plan measures of enthusiastic discourse databases. There are a few ends drawn from this examination. The first is high arrangement correctnesses that have been gotten for order of feelings.

The normal grouping precision of discourse feeling acknowledgment frameworks is under 80% in a large portion of the proposed strategies. Now and again, for example, it is as low as half. For speaker-subordinate arrangement, the normal exactness surpassed 90%. Numerous classifiers have been gone after for discourse feeling acknowledgment, for example, HMM, GMM, ANN and SVM. In any case, it is hard to choose which classifier performs best for this errand. There are additionally utilized distinctive element determination strategies to locate the best highlights for this undertaking. In numerous databases, it is troublesome in any event, for human subjects to decide the feeling as human acknowledgment precision was 67%.

In 'Programmed discourse feeling acknowledgment utilizing balance ghostly features', Siqing Wua, Tiago H. Falk, and Wai-Yip Chan present novel MSFs for the acknowledgment of feelings in speech. The proposed highlights are separated from ST portrayal by methods for unearthly measures and straight expectation boundaries. The MSFs assessed by Berlin database to group feelings, transient unearthly highlights and prosodic highlights are removed to benchmark the proposed highlights. The proposed highlights are filled in as joined with MSFs to accomplish 91.6% generally speaking acknowledgment precision. In a LOSO cross-approval test, the MSFs give better execution, when speaker standardization is applied; MFCC joined with prosodic highlights beat MSFs joined with prosodic highlights. MFCC highlights are appeared to convey the best outcomes in the relapse tests (Table 1).

Table 1 Findings of emotion recognition approaches and their accuracy

S.No.	Authors	Signal/technique/approach	Accuracy (%)	Findings/outcome
1	Adrian Qi-Xiang Ang	EEG, time–frequency-DWT features and ANN	81.78	Wavelet coefficients and IAPS are used as visual stimuli to evoke emotions
2	M. Sreeshakthy	EEG, DWT, HOC, STFT, PCA with RBF and SVM used as a classifier	84.6	Outcome indicated that proposed work effectively extracted EEG analysis in emotion recognition the highest accuracy achieved
3	Bahareh Nakisa	EEG, ant colony optimization (ACO), genetic algorithm (GA), simulated annealing (SA), particle swarm optimization (PSO) and differential evolution (DE)	97.1	A comparison of five feature selection algorithms is shown on the basis of time taken and accuracy from which GA achieved highest accuracy on MAHNOB dataset with feed forward neural network (PNN)
4	Zhen-Tao Liu	Voice signal, extreme learning machine (ELM)	89.6%	Emotion as decision tree is erected for speech emotion recognition and ELM is assumed as the binary-classifier
5	Lijiang Chen	Voice signal, support vector machine (SVM), principal-component-analysis (PCA), artificial neural network (ANN)	86.2	Proposed model as feature reduction using Fisher norm is better than PCA
6	Kunxia Wang	Speech, Mel-frequency cepstral coefficient (MFCC), support vector machine (SVM)	85.2	Fourier parameter sorts are effective in characterizing and identifying emotions in speech signals

(continued)

Table 1 (continued)

S.No.	Authors	Signal/technique/approach	Accuracy (%)	Findings/outcome
7	Panagiotis Tzirakis	Speech, long short-term memory (LSTM)	61.35	Future model achieves state-of-the-art results, with esteem to concordance parallel factor for both arousal and valence
8	Lay New	Speech, LFPC and HMM	89	LFPC as the pointers of emotional states and HMM as the classifier do oblige as a feasible approach for the sorting of emotions recognition speech
9	Moataz ElAyadi	Speech, HMM, GMM, ANN, and SVM	90	Employed altered feature collection techniques to find the best structures for emotions recognition of speech
10	Siqing Wua	Speech, MFCC combined with prosodic features outperform MSFs	91.6	Proposed features are served as combined with MSFs to achieve overall recognition accuracy
11	Adnan Mehmood Bhatti	EEG, KNN, SVM, ANN	91.0	Emotion recognition and exploration in retort to audio music with best accuracy
12	Heraz	EEG, KNN	82.27	The best classification accuracy achieved for eight emotional shapes, using KNN (k-nearest neighbours) as a classifier

4 Conclusion and Future Scope

Emotion recognition is becoming very popular and important field to mend the interaction between human and machine as convolution of human emotion makes the acquirement assignment more difficult. Researchers are proposed to imprisonment

emotion through uni-modal instrument such as voice, facial expression, bio signals (EEG, ECG, EMG and EOG). This paper attempts to represent different techniques that can be used to recognize emotions using speech and EEG brain signals separately. Though emotion and speech recognition are two individual research field, we can design a cognitive model of emotion recognition by using voice and EEG signal with high accuracy by attempting to emerge with the new techniques, which comprise of emotion and speech together for detecting emotions of human being and classify emotions more accurately.

Besides, the possibility of multimodal feeling acknowledgment has expanded the precision pace of the discovery of the machine with different learning methods. Still numerous viewpoints here to take a shot at to improve and make a powerful framework will identify and order feelings all the more precisely. We attempted to investigate the important works, their strategies and adequacy of the different techniques and the extent of the improvement of the exactness in human feeling identification.

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Butler Matrix Design for Smart Antenna in X-Band Applications

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1 Introduction

In wireless communication, beamforming technique is used to cover the desired direction for the coverage of intended user in modern mobile needs. For this kind of application, an antenna was designed by using Rogers RT Duriod 5880 substrate to cover X-band frequencies [1]. 5G will be the next wireless technology for communication with high data rate, high capacity and will tackle energy efficient operation in the near future [2]. To design an individual antenna is easy, but data rate will be low. The present/next technology requires high data rate, which depends on the multiple antenna systems called multiple input multiple output (MIMO) [3, 4].

5G technology will resolve almost all drawbacks of 4G technology in future and will provide data rate up to three times of 4G, and the main advantage of 5G is that mobile device with 4G can be upgraded to accommodate 5G antennas [5]. In wireless communication systems, it is required to separate the desired signal from the interference signal. By reducing the multipath and channel interference, smart antennas will provide high capacity of signal transmission in wireless communications [6–9].

The design of butler matrix is one type of passive beamforming network which consist of N input and output ports and N input and output antenna elements to produce N principal orthogonal beams at different directions. The operation of butler matrix design can be understood as: Firstly, radio frequency (RF) signal will get excitation from the input ports, after that signal will go to the output port through the feeding array elements. The signal will propagate equally with a constant phase between them, and beam radiation will generate at a certain angle [10–12].

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2 Butler Matrix Design for Beamforming

In this paper, 4 × 4 butler matrix design is proposed for X-band applications. Figure 1 shows the front and back views of the proposed 4 × 4 butler matrix design. In this design, four 90^0 hybrid couplers, 2-crossovers, and 2-phase shifters are used. This design is used to feed 4-microstrip patch antennas. The radiation direction of beam is point out with respect to each input ports in such a way, so that user can select the desired main beam by feeding any inputs [13, 14]. Computer simulation tool (CST) software is used for the design and simulation results. The optimized dimensions of the butler matrix design are given in Table 1.

The proposed 4 × 4 butler matrix is designed, as a passive network by using the Rogers RT duriod substrate, having dielectric constant of 2.2, dielectric loss of 0.0009, and thickness of 0.79 mm. RF signal can excite to any input ports (port one, port two, port three and port four or all) with equal amplitude and phase difference.

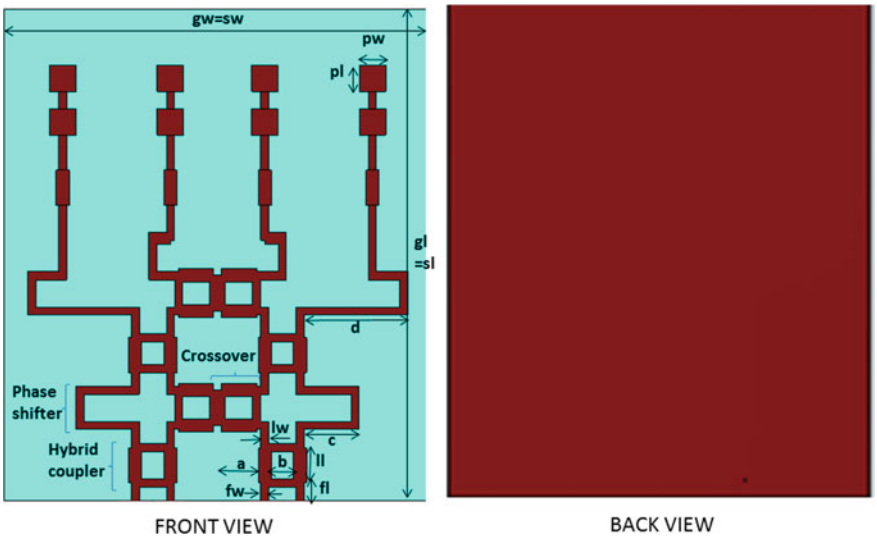

Fig. 1 Schematic views of the proposed 4 × 4 Butler matrix design

Table 1 Optimized dimensional values (mm)

Parameter	sw	sl	gw	gl	a	b	c
Value (mm)	130	150	130	150	14.4	10.7	18
Parameter	d	fw	fl	pw	pl	ll	lw
Value (mm)	34	2.4	5.4	8	8	10.7	3.94

If all the input ports are excited, then the butler matrix can work as a beamforming network.

At the center frequency, butler matrix provides four outputs with equal power levels and equal phases. The direction of main radiation beam can be changed by exciting the desired input port. Narrow beam can be developed using this design for different directions and can select the strong signal from the available signals. Return loss has minimum influence on the working frequency due to its microstrip discontinuities.

For impedance matching and high antenna gain, the optimized patch dimensions and inter element space very careful and in this design. It is observed that the phase differences received at 10 GHz frequency are very closer to the theoretical model (45°, 135°) with a quite tolerable phase errors from 9° to 12°.

Hybrid coupler structure plays a vital role in butler matrix, which divides the input signal into two output signals with equal amplitude and provides 90° phase shift to the operating frequency. The main line of hybrid coupler is connected to the secondary line with two quarter wavelengths ($\lambda/4$) long sections. Hybrid coupler provides input at port one, output at port two, isolation at the port three, and matched load termination at port four [15].

In realization of butler matrix design, crossover is the main problem because crossover is used to bypass the superimposed of signals at crossings. At the port, hybrid coupler in cascading is required for the enhancement of the isolation between the input ports. If every adjacent port is isolated, then designing of crossover is complete. Reference line L is smaller than each line by definite amount of $\triangle L$ to introduce a phase shift θ and is given by Eq. 1 [16].

$$\triangle L = \frac{\theta * \lambda_g}{360^\circ} \tag{1}$$

where, λ_g is guided wavelength.

The microstrip line of 50 Ω can be designed with 45° phase shift. In microwave networks, phase shifters are used, and phase delays of transmission lines are given by Eq. 2:

$$\phi = k_z l \tag{2}$$

where ϕ is phase delay, k_z is propagation constant and l is length of the line.

Equal lengths and unequal widths of two delay lines can be used to provide phase difference and is given by Eq. 3:

$$\triangle\phi = (k_{z2} - k_{z1})\, l \tag{3}$$

where, k_{z1} and k_{z2} are propagation constants.

Performance of 4 × 4 butler matrix in terms of beamformimg can be obtained by the proposed matrix by connecting it to the four patch antenna arrays [17–19]. The scan sensitivity and main beam direction are given in Eq. 4 [20]:

$$d \sin\theta + \sqrt{(\eta_l)} = \frac{c}{f} = \lambda \tag{4}$$

where d is the space between elements, ι is transmission line length to join the elements, and θ is the angle of beam, pointing which is measured from the broadside direction.

Series feed linear antenna array factor can be written in Eqs. 5 and 6 as:

$$AF = \frac{\sin\left(N\pi d_x\left(u - u_0\right)\right)}{\sin\left(\pi d_x\left(u - u_0\right)\right)} \tag{5}$$

and,

$$u = \sin(\theta), u_o = \sin(\theta_o) \tag{6}$$

where dx is the space between the elements and N denotes the number of elements.

Voltage radiation pattern and array factor of elements both can be combined to provide normalized power radiation of total elements and is given by Eq. 7 as:

$$P_{\text{rad}} = 20\log\left(|E/AF)\right| \tag{7}$$

The presented series feed array antenna and hybrid coupler are designed on a single layer. It results in integrated structure with high efficiency. The microstrip series feed patch antenna array is designed to increase the operating bandwidth and for reducing the XPR (cross-polarization) radiation. The electric field can be expressed by Eqs. 8 and 9 as [21]:

$$\overrightarrow{E} = E_o\left(j\alpha\overrightarrow{a_x} + \overrightarrow{a_y}\right) \tag{8}$$

$$\overrightarrow{E} = E_o\left(-j\alpha\overrightarrow{a_x} + \overrightarrow{a_y}\right) \tag{9}$$

where α is the residual axial ratio.

For good radiations, a planar array must have characteristics of beam steering and side lobe suppression. Applications of series fed antenna have beamsteering and multibeam capability for multi-frequency operations. Variety of butler matrix is available in literatures [22–27].

3 Results and Discussion

To fed the proposed 4×4 butler matrix, 50 Ω microstrip feed line is used, and it resonates at -10 dB return loss for the operating band of 9.4–10.6 GHz. Simulated results of return loss and isolations at different ports are shown in Figs. 2 and 3. It is also observed that $S_{11} = S_{34} = S_{42} = -10$ dB, $S_{13} = S_{21} = S_{44} = -23$ dB, $S_{23} = S_{31} = -24$ dB, $S_{41} = S_{33} = -8$ dB, $S_{12} = S_{43} = -11$ dB, $S_{14} = S_{22} = -9$ dB and

Table 2 Different inputs with their respective beam angles

References	Input 1 (°)	Input 2 (°)	Input 3 (°)	Input 4 (°)
[23]	−45	135	−135	45
[27]	−15	45	−45	15
Proposed design	−15	45	−45	15

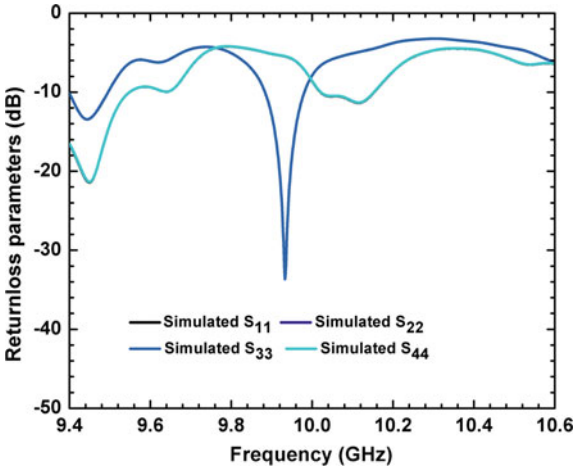

Fig. 2 Return loss parameters of 4 × 4 Butler matrix

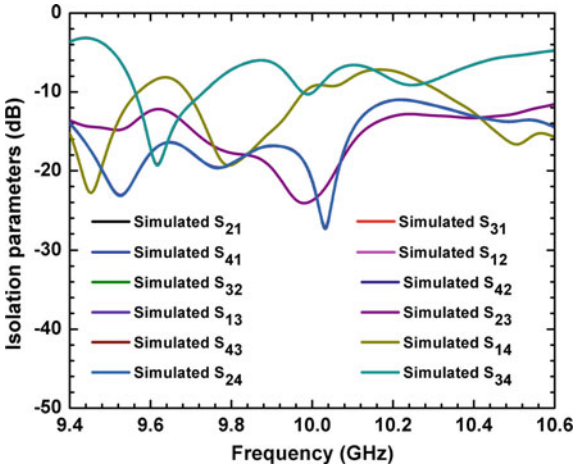

Fig. 3 Isolation parameters of 4 × 4 Butler matrix

$S_{24} = S_{32} = -21$ dB at 10 GHz. Table 2 gives the comparison of proposed design with existing designs for different inputs with their respective beam angles.

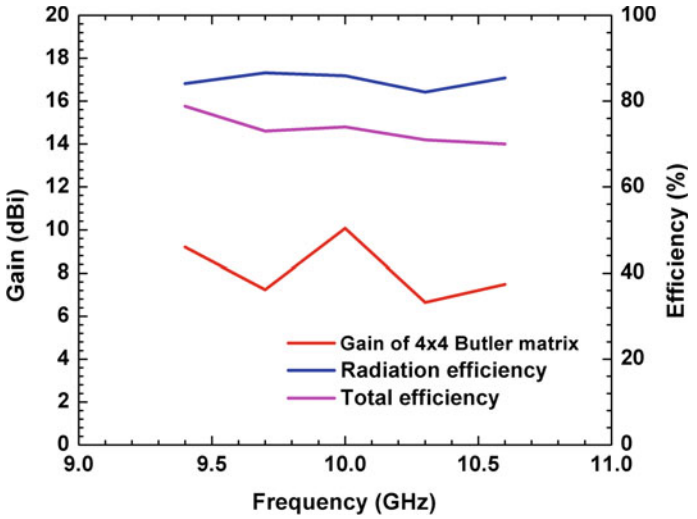

Fig. 4 Gain and efficiency of the 4 × 4 Butler matrix

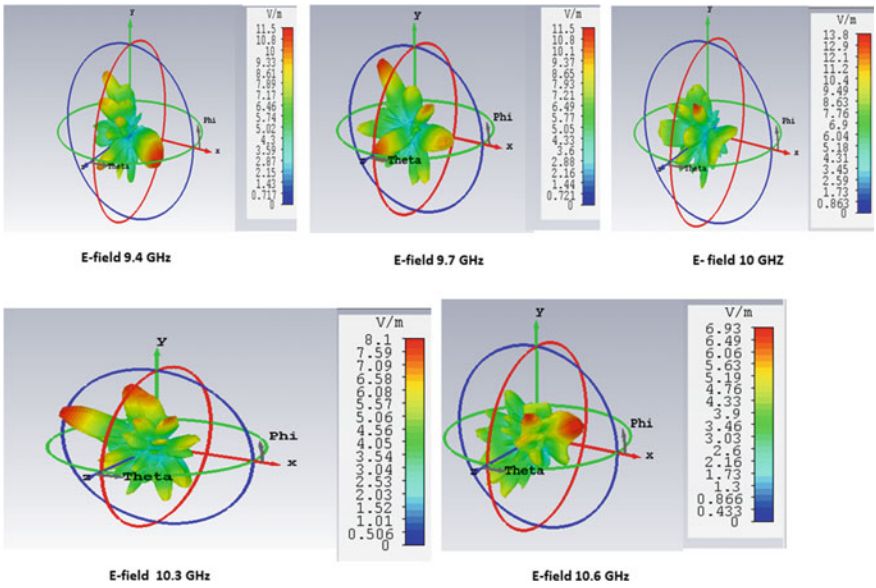

Fig. 5 3D E-field patterns at different frequencies

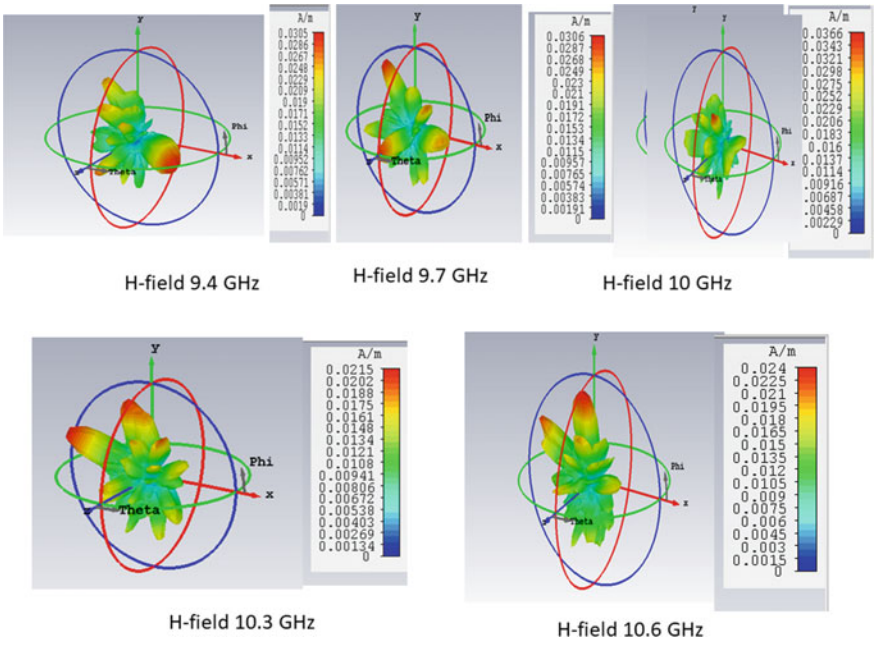

Fig. 6 3D H-field patterns at different frequencies

The variation in gain can be obtained between 7.49 and 10.08 dBi in the operating frequency range of 9.4–10.6 GHz. The radiation efficiency in the band varies from 82 to 87%. The total efficiency in the operating band is more than the 67% for the 4×4 butler matrix. All the gains and efficiencies are plotted in Fig. 4. Maximum gain is 10.08 dBi at 10 GHz resonant frequency, and maximum radiation efficiency is 86.58%.

The 3D E-field patterns for different frequencies in the operating band are given in Fig. 5 with their individual scales. These far-field radiation patterns are obtained using CST-MWS software. Different main lobe magnitudes at these frequencies are 11.5 V/m, 11.5 V/m, 13.8 V/m, 8.1 V/m, and 6.93 V/m at 9.4 GHz, 9.7 GHz, 10 GHz, 10.3 GHz, and at 10.6 GHz, respectively.

Similarly, different 3D H-field patterns are shown in Fig. 6 with their individual scales. Different main lobe magnitudes are 0.0305 A/m, 0.0306 A/m, 0.0366 A/m, and 0.0215 A/m, and 0.024 A/m, at 9.4 GHz, 9.7 GHz, 10 GHz, 10.3 GHz, and at 10.6 GHz, respectively. From E-field and H-field patterns, it has been observed that the beamforming have been done in these patterns.

Table 3 Comparison of proposed design with existing designs

References	Frequency band (GHz)	Butler matrix of size	Size of substrate	Return loss (dB)	Gain	Substrate	Isolation (dB)	Application
[24]	9–11	4 × 4	$7.1 \times 4.5\,cm^2$	−10	–	RT/Duroid 5880	10	X-band
[25]	8.25–8.3	4 × 4	$53.7 \times 46.7\,mm^2$	−34	–	RT/Duroid 5880	10	X-band
[26]	10	3 × 3	$197 \times 50\,mm^2$	−14	10.5 dBi	Rogers 5880	30	X-band
Proposed design	9.4–10.6	4 × 4	$150 \times 130 \times 0.79\,mm^3$	−10	10.08 dBi	RT Duriod 5880	20	X-band

4 Conclusion

To steer the beam in different directions, a design of 4 × 4 butler matrix with wide band has been designed, which is operating in the frequency range from 9.4 to 10.6 GHz. At 10 GHz frequency, gain is 10.08 dBi, and radiation efficiency is 85.93%. Designed butler matrix has been implemented very easily and having the dimension of the substrate as $150 \times 130 \times 0.79\,\text{mm}^3$ for 2:1 VSWR. The design has small volume, light weight, and low cost, which makes this proposed design suitable for the beamforming applications. This design can be converted into 8 × 8 Butler matrix for the coverage of the appropriate directions.

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On Body Antenna for WiMAX and WLAN-Band Operations

Ankur Utsav and Ritesh Kumar Badhai

1 Introduction

In the present scenario of high-speed data communication, antenna is playing an important role as a transmitter as well as the receiver. In the present scenario of communication, on body antenna is becoming great thrust among the researchers as it is applicable in biomedical applications for a diagnosis like MRI, FMRI, biomedical telemetry, ECG, EMG, breast cancer detection, and brain tumors, etc. [1–6]. These days WBAN is very important band as it is dealing with the data communication related to body and its surroundings. Also, body antenna is in great demand among military applications and satellite communications [7]. In lieu of development, different researchers have given their ideas and analysis for the on-body antenna at different frequencies of operation. Initially, a single-band wearable antenna is presented by different researchers. Some of them are working for any of the bands namely ISM, WiMAX, WLAN, UWB, etc. [8–11].

Again, the concept of reconfigurability in on body antenna is used among the researcher such that the antenna can be capable of working at any of two different bands. To achieve this, the concept of the slot, PIN diode, etc., is used. The overall gain is found to be in a better range and showing optimal operation throughout range [12, 13].

After the development of a single band antenna with a reconfigurable concept, different researchers have suggested their work on dual-band wearable antenna [14–18]. The dual-band antenna with co planar patch [18] is working for 2.45 and 5 GHz bands of frequency, the concept of arraying is also used and an overall gain of 3 dBi is

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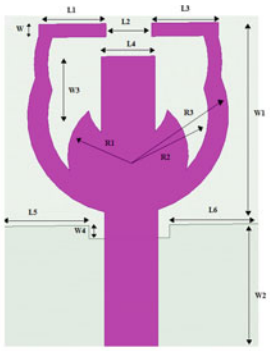
reported. The reported antenna was printed on a fabric substrate and its comparative analysis with FR4 is also studied. But the work is outshined with little bandwidth and bigger size. In [19], a flexible dielectric resonator with dual-band operating (WiMAX and WLAN) is proposed. The antenna is showing a better gain of 5.4 dBi with a size of 40 × 40 mm^2. Analysis of human phantom with different dielectric values for skin, fat, and muscles is undertaken. The overall size is of the antenna is bigger. In [20], a triple-band antenna is proposed having notch at Wimax band WLAN band and X band. WLAN band has a set standard of IEEE 801.11 used for Wi-fi in general communication works and its covering frequency range is from 5.1 to 5.9 GHz. X band can be used for satellite communications.

Throughout different works proposed by different researchers very little work is proposed for the duality function of WiMAX and X-band. As it is better known than WiMAX, having its IEEE standard as 802.16a which is an innovative technology having a better bandwidth of 2–11 GHz and is largely operated for high-rate broadband internet service [21]. Also, WLAN band is used in communication ranges from 5.1 to 5.9 GHz having main applications in military usage, Wi-fi and RADAR technology [22].

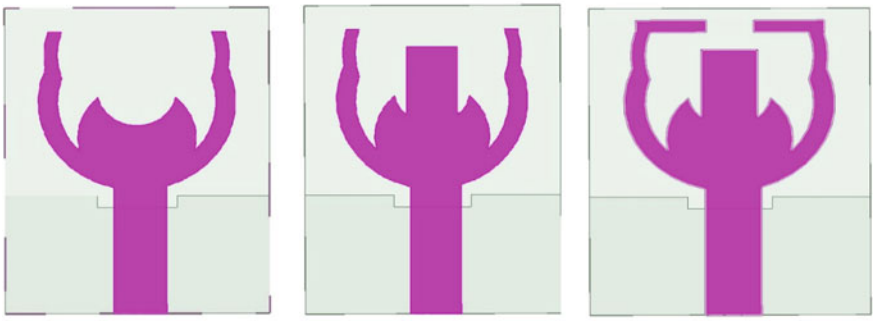
In the present work, a modified arm vase-based shaped monopole patch antenna with compact dimensions of 26 × 20 mm^2 is shown. The rectangular slot is taken out from ground plane at the backside of the feedline for impedance matching and second mode generation. The concept of DGS is also implemented for improvement in the matching in the lower frequency. The proposed antenna is resonating at WiMAX and WLAN-band. The present antenna is fulfilling all the basic requirements to be operated for WiMAX and WLAN-band. The proposed antenna exhibits a better gain of 3.9 dBi in free space and 3.2 dBi with body phantom at the resonating frequencies and having a bandwidth of 3.1–3.6 GHz for WiMAX and 4.8–8 GHz for WLAN-band in free space.

2 Antenna Design and Study

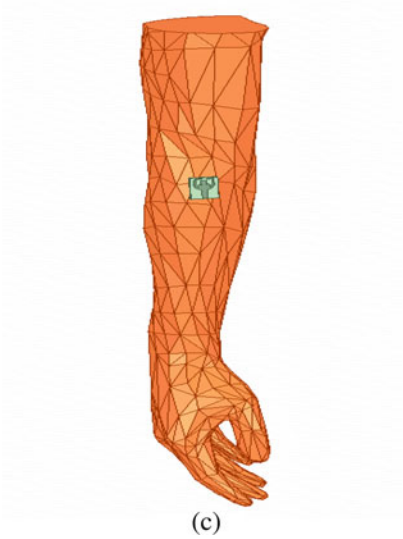
The defined antenna dimensions are depicted in Fig. 1a. The substrate of $\varepsilon_r = 4.4$, $\tan\delta = 0.02$ with a thickness of 1.6 mm named glass epoxy FR4 material is used. For the simulation purpose, we had used ANYSIS HFSS 17.2 simulation tool. Two circles having a radius of 8 and 6 mm are being connected with the center space of 2 mm for radiating patch with dual-wideband characteristics. The discussed antenna is having its excitation with a 50 Ω micro-strip transmission line having a length of 21 mm and a width of 4.0 mm, which is further connected to a circular structure of radius 4 mm. This patch consists of two arms having width 2 mm which is formed by subtracting two circles of 8 and 6 mm, respectively. And last at the arms of the patch two more rectangles are added with length 6 mm and width 1 mm for the second band. A small rectangle with length 6 mm and width 1 mm ground in the backside of the patch is taken for getting the anticipated frequency range. A perfection in bandwidth and better impedance matching is seen. The detail of the obtained antenna is described



(a)



(b)



(c)

Fig. 1 **a** Design of the projected antenna, **b** the parasitic study of final projected antenna, **c** realization of the projected antenna in simulated space on the human hand

Table 1 Details of the projected antenna design

L1 = 5	L6 = 7	W4 = 1
L2 = 3.30	W = 1	R1 = 4
L3 = 5	W1 = 16	R2 = 6
L4 = 4	W2 = 10	R3 = 8
L5 = 7	W3 = 6.5	All dimensions are in mm

in Table 1 and the final proposed antenna is shown in Fig. 1a. The Parametric study of three antenna is also shown in Fig. 1b and its implementation on the human hand phantom is shown in Fig. 1c.

3 Results and Discussions

In Fig. 2 shows a comparative graph of the simulated reflection coefficient in air and with the human hand. From the reflection coefficient graph, it can be observed that the simulated results of the projected antenna are resonating at lower resonating frequency 3.3 (3.0–3.5 GHz) and higher resonating frequency 5.5 GHz (4.7–8 GHz) with a bandwidth of and 3.95 GHz, respectively. For human phantom, the lower resonating frequency is achieved at 3.35 (3.0–3.5 GHz) and the higher resonating band is achieved at 5.56 (4.9–8.0 GHz) with a bandwidth of 3.4 and 3.2 GHz for dual operating bands in free space and presence of male human arm, respectively,

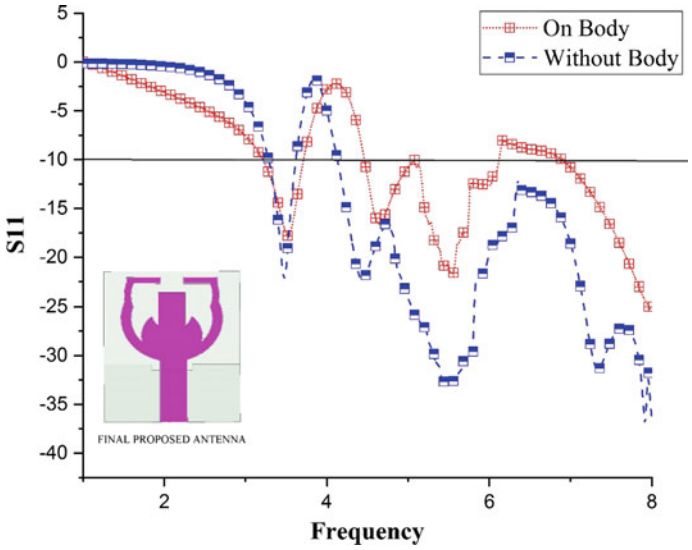


Fig. 2 Simulated reflection coefficient (S_{11}) in free space and on the human arm body

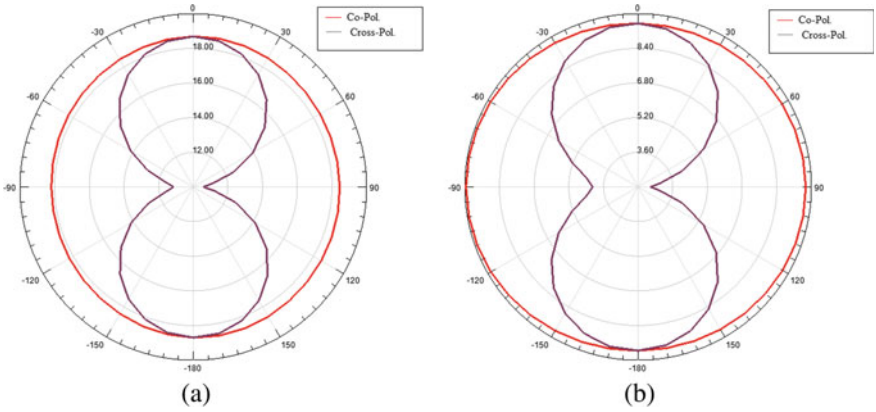


Fig. 3 Simulated normalized radiation pattern of the projected antenna **a** 3.3 GHz and, **b** 5.5 GHz

satisfying both the desired bands WiMAX and WLAN band. All the results are in close agreement with each other. We examine that on body results are shifted a bit higher side because the reduction in the permittivity of the human body with frequency. Resonant frequency is inversely proportional to permittivity.

In Fig. 3, graph for the simulated 2D radiation pattern of the projected antenna in air at two frequencies (3.3 and 5.5 GHz) for YZ-plane (E-plane) is shown. Figure 4 depicts Co and Cross-polar normalized graph of the antenna's radiation pattern.

In Fig. 4, SAR variation in human body hand at two operating frequencies 3.3 and 5.5 GHz is shown. SAR is very important parameter for antennas for Body applications as it gives a range of power permitted for 1 kg of human mass tissue. According to FCC/IC, the allowed SAR value to 1.6 W/kg averaged over 1 g of human tissue. SAR in EM energy can be projected from the applied electric field in the tissue as:

$$\mathrm{SAR} = \frac{1}{V}\int \frac{\sigma(r)\{E(r)\}^2}{\rho(r)}\mathrm{d}r$$

where V = volume of the section,
σ = conductivity of the sample,
E = RMS value of electrical field,
ρ = sample's density.

In the present work as evident from Fig. 5 that SAR is in under the allowed values and its highest range is found to be 0.12 W/kg for 3.3 GHz and 0.299 W/kg for 5.5 GHz.

In this paragraph study of current density is illustrated, as it is well known that current density is very important parameter for antenna designing. It gives the measure of electric current for a unit area of cross-section. The surface current distributions of the projected antenna at 3.3 and 5.5 GHz are shown in Fig. 5. It can be

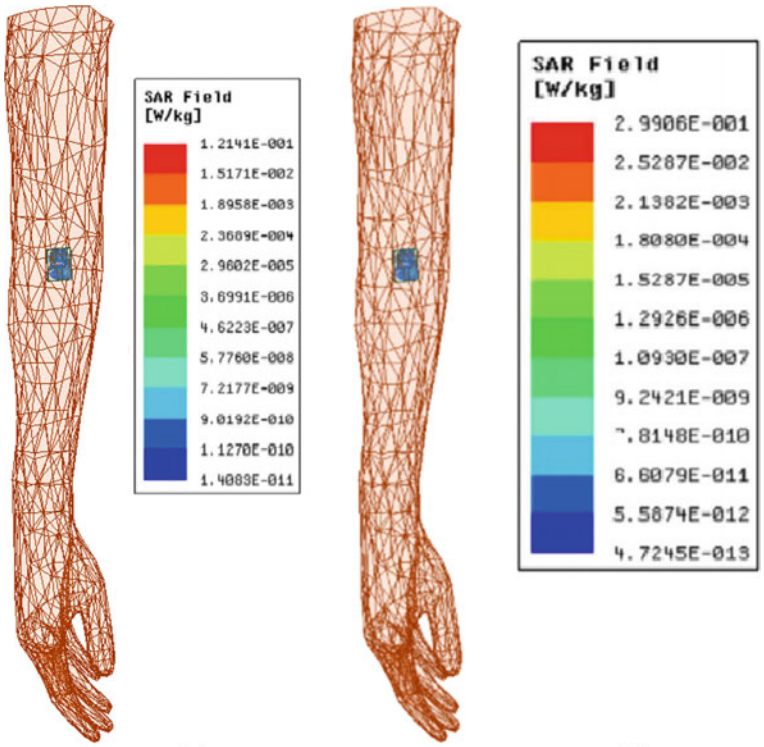


Fig. 4 SAR differences on human male arm at **a** 3.3 GHz and **b** 5.5 GHz

observed that at lower resonance most of the current distributed over the radiating patch and the ground plane. For the advanced resonance frequency, current is leading at the upper I-shaped strip of the ground level. Table 2 consists of various antenna parameters of the proposed antenna and Table 3 consist comparison of proposed antenna parameters with different papers.

4 Conclusion

This is a paper which describes a new, compact and effective designed printed antenna which is operated at dual bands covering Wimax and WLAN. It was found that the projected antenna was perfect for body applications with desired SAR values. During the simulation process, we found that our antenna is having a very improved return loss which confirms a better impedance matching. Two wide bands which were obtained are from 3.0 to 3.5 GHz (WiMax) and from 4.7 to 8 GHz (covering WLAN-Band). This printed antenna can be effectively used for communicational

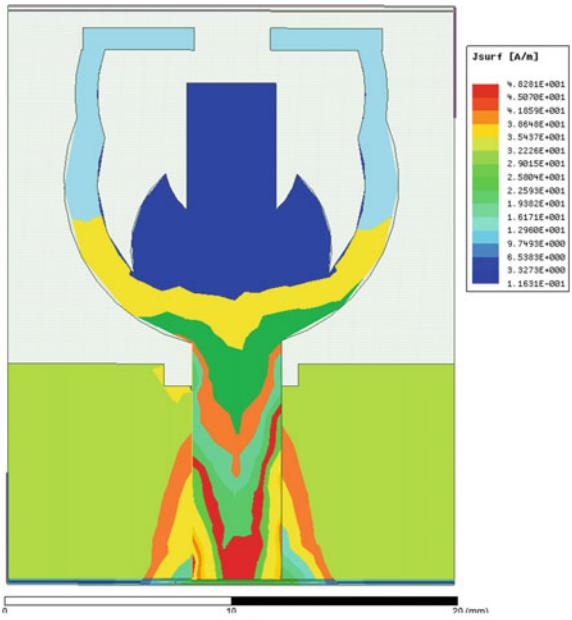


Fig. 5 Surface current density of projected antenna at **a** 3.3 GHz and, **b** 5.5 GHz

Table 2 Comparison of various antenna parameters without body and with the body

Antenna parameters	Without body	With body
Minimum reflection coefficient (S_{11})	− 21, − 33 dB	− 19, − 21 dB
Resonating frequency	3.3, 5.5 GHz	3.34, 5.56 GHz
Maximum gain	3.9 dBi	3.2 dBi
Band width	500 MHz (the first band covering Wimax band) 3.4 GHz (the second band covering WLAN band)	440 MHz (first band covering Wimax band) 3.2 GHz (the second band covering WLAN band)
Efficiency (%)	87	85

Table 3 Comparison of proposed antenna parameters with different papers

References	Antenna parameters				
	Bandwidth (GHz)	Operating band	Gain (dBi)	SAR (W/kg^2)	Size (mm^3)
[8]	7.5	UWB	–	–	30 × 30 × 0.5
[21]	0.2	WLAN and WiMAX	5	–	44 × 44 × 1
[22]	0.24	ISM	1.81	0.0288	8 × 9 × 1.5
Proposed antenna	0.500 (first band)	WiMAX and WLAN	3.9	0.12 (first band)	26 × 22 × 1.6
	3.4 (second band)			0.299 (second band)	

purposes in home and offices by Wi-fi, for cellular communications, for medical data communication in air and on human body. The small size with dimensions 20 mm length and 26 mm width and its improved results makes the projected antenna a unique one. DGS concept is used for better and improved second band. For the simulation Ansys HFSS software is used. We can use this projected antenna for smart watches and other wearable devices (Tables 2 and 3).

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Performance Analysis of Gate-Stack Nanoscaled Recessed-S/D SOI-MOSFET for Analog Applications

Nilesh Anand Srivastava, Anjali Priya, and Ram Awadh Mishra

1 Introduction

Nowadays, semiconductor devices have become the backbone of modern communication systems with the development of low-power and high-performance integrated-circuits (ICs). Further, these ICs are advancing day by day with the continuous growth of complementary-metal–oxide–semiconductor (CMOS) technology for low power analog applications [1, 2]. Moreover, the heart of these high-density ICs is a MOSFET, as each IC is accommodated with billions of MOS-devices [3, 4]. So, this is a prime concern that the MOS-transistors should exhibit significant characteristics for successful integration with an IC. To attain high-density and high-speed ICs, the miniaturization of CMOS transistors is taking place from the past two decades [4, 5]. However, the hyper scaling tends in MOS-transistors beyond 100 nm node have deteriorated the performance of the device and results in various short-channel-effects (SCEs), such as mobility-degradation; hot-carrier-effects (HCE); gate-induced-drain-leakage (GIDL); drain-induced-barrier-lowering (DIBL); etc. [5, 6]. These detrimental changes in nanoscaled MOS-devices may lead to threshold-voltage roll-off and hence leakage in the subthreshold-regime [7].

Various suggestions have been reported in earlier researches' to overcome these unwanted effects in short-dimension MOSFETs. Like, multi-metal-gate (MMG: dual-/triple-metal) [8, 10] and multi-gate (MG: double-/triple-/gate-all-around

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(GAA)) [11] FETs have been suggested to enhance the gate controllability over channel. However, the gate-all-around structures suffer from various misalignment issues and have higher fabrication complexity. Further, the silicon-on-insulator (SOI) technology [12] (FinFET-SOI [13], Fully-/Partially-Depleted SOI [14–16], Junction-less-transistors [17]) has replaced bulk Si-substrates and results in very low off-state leakage with improved short-channel behavior. Similarly, different performance enhancement techniques, like, source/drain engineering [18]; high-k/low-k gate-stack (GS) [19]; hetero-dielectric (HD) [20] have also been suggested in earlier state-of-the-art to improve the device immunity in nanoscale regime.

Moreover, as per the recent reports, FD SOI MOSFETs offer significant immunity over SCEs with lesser process complexity than Fin-shaped FETs [21–23]. Also, FD SOI technology exhibits un-doped channel concept due to its thinness and follows the Moore's law altogether [24, 25]. The first theoretical potential model of FD SOI-MOSFET was proposed by Young [21]. Further, Suzuki et al. had modified with the inclusive effects of SOI-thickness [22]. Next, Cheng et al. had concluded that dynamic threshold and back-bias technique could be two alternatives to improve the analog and radiofrequency (RF) performance of nanoscaled-SOI MOSFETs [23].

Further-more to overcome the issue of DIBL significantly, the multi-metal-gate technique has been employed in FD SOI-MOSFETs [24, 25]. In which, multi-metal gates of different work-functions are arranged side-by-side to reduce the DIBL effects in a much-controlled manner. The dual work-function metal gates offer a step-like potential profile [24]. Kumar et al. had theoretically investigated FD SOI performance with dual-metal-gates (DMG) [24]. In continuation, Srivastava et al. has extensively studied the concept of separated metal-gates with dielectric modulation and source-engineering [10, 25].

However, FD SOI-MOSFETs with ultra-thin-body (UTB) may lead to the larger series-resistance due to ultra-thin regions of S/D. Moreover, Zhang et al. had suggested that this could be further overcome by the use of recessed-S/D (Re-S/D) technology [26] and Sivilicic et al. had given the theoretical justifications for the same [27]. In next, the methodology of Re-S/D technique also employed with multi-metal-based SOI-MOSFETs [28, 29]. However, technology scaling in the nanometres regime also reduces the oxide thickness, which increases the current and speed. Also, the thin oxides may lead to the carriers-tunnelling through gate-oxide and hence cause of gate-oxide leakage current. This leakage may further be reduced by using high-k oxide-material such as HfO_2 (Hafnium Dioxide) stacked with SiO_2 (silicon-dioxide) [19]. However, less attention has been made to utilize the technique of gate-stack in the design of triple-metal gate-engineered Re-S/D SOI-MOSFET.

This paper presents the performance investigation of short-channel GS-TMG: Re-S/D FD SOI MOSFET for the first time. The results assure that the concept of gate-stack can further improve the performance of triple-metal gate-engineered Re-S/D FD SOI MOSFET. This paper has been organized in the following sections. The device structure and process flow are discussed in Sect. 2, and the simulation platform and model definition has been described in Sect. 3. Next, the numerical simulation results of the proposed FD SOI MOSFET have been extensively analyzed in Sect. 4. Finally, the overall work is concluded in Sect. 5.

2 Device Design Strategies and Process Flow

The studied device structure of GS-TMG: Re-S/D FD SOI n-MOSFET is shown in Fig. 1, and the device parameters and their specifications are listed in Table 1. The device is initially designed at 45 nm technology node with three different work-function metal gates (L_{M1}: $\phi_{M1\text{-Aurum}} = 4.8$ eV; L_{M2}: $\phi_{M2\text{-Molybdenum}} = 4.6$ eV; L_{M3}: $\phi_{M3\text{-Titanium}} = 4.4$ eV) of length 15 nm each ($L_g = L_{M1} + L_{M2} + L_{M3}$). This arrangement is suitable to enhance the gate control over the channel and screen-off the changes due to higher drain-bias. Next, the high-k spacer is placed to overcome the fringing-field effects at gate edge. Also, the device is composed of high-k (HfO_2)/low-k (SiO_2) dielectric-gate-stack ($\varepsilon_{r:high\text{-}k} = 32$ and $\varepsilon_{r:low\text{-}k} = 3.9$), such that a thin layer of low-k dielectric is deposited prior to the high-k. Gate-stack engineering will help to overcome the issues of off-state and gate-oxide leakage. All other design parameters and doping levels are mentioned in Table 1.

The process flow of the device mentioned above is also feasible with less complex fabrication steps as compared to Fin-shaped FETs. The process feasibility can be discussed in the following steps. Step 1: Pattering of Silicon-wafer [10]; Step 2: Formation of UNI-BOND technique based SOI substrate [15]; Step 3: Preparation of Re-S/D junctions [18]; Step 4: Implantation of source/drain regions [15, 18]; Step 5: Stacked-oxide growth [10]; Step 6: Metal-Gates ($M_1/M_2/M_3$) deposition [18]; Step 7: Side-spacer growth/Etch/Contact Formation; Step 8: Lift-off/Device Test.

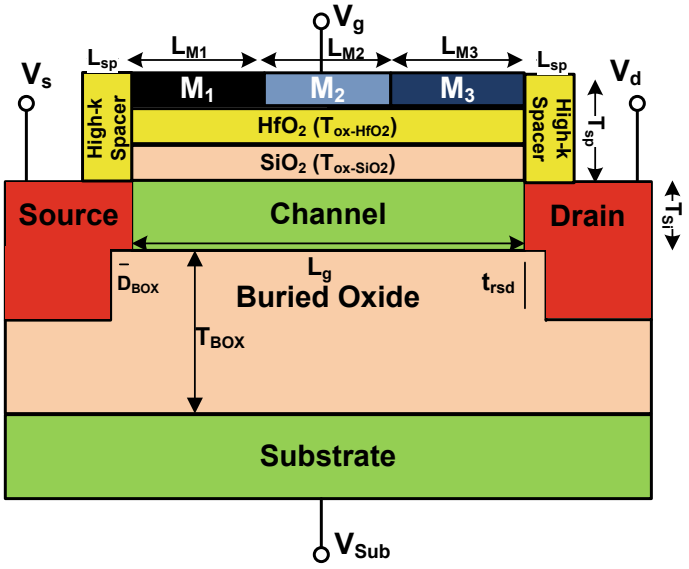

Fig. 1 Studied and simulated design of gate-stack TMG: Recessed-S/D FD SOI-MOSFET

Table 1 Device design parameters and specifications

Parameter	Symbol	Value	Unit
Channel length	L_g	45	nm
High-k oxide-thickness	$T_{ox\text{-}HfO_2}$	1	nm
Low-k oxide-thickness	$T_{ox\text{-}SiO_2}$	1	nm
High-k spacer length	L_{sp}	10	nm
High-k spacer-thickness	T_{sp}	3	nm
BOX-thickness	T_{BOX}	50	nm
Si-film thickness	T_{si}	12	nm
Re-S/D thickness	T_{rsd}	20	nm
BOX overlap Re-S/D thickness	D_{BOX}	3	nm
Metal-gates length-ratio	–	1:1:1	–
Doping (source/drain)	$N_{S/D}$	1×10^{20}	cm^{-3}
Doping (substrate)	P_{Sub}	1×10^{16}	cm^{-3}

3 Simulation Methodology

The design and simulation of studied FD SOI n-MOSFET have been performed using Silvaco-TCAD (ATLAS™) [30]. For the accurate analysis, different numerical models have been included at the simulation platform [28]. As SRH (Shockley–Read–Hall) model is taken to access the life-time of majority-carriers (generation/recombination). Next, to add the effects of mobility degradation due to temperature, Lombardi-mobility, and CVT (constant-voltage-and-temperature) models are considered. Also, the FLDMOB model (field-dependent-mobility) has been utilized to monitor the impact of transversal-field in nanoscaled-MOS design. To investigate thermal behaviour lat.temp (lattice-temperature) model has also been considered here. Further, the Gummel-Newton model and drift–diffusion are taken for the study of switching (on/off) behavior of the device. Furthermore, this is necessary to adopt the quantum-potential models at 45 nm node. So, for the analysis, QME (Quantum–Mechanical-effect) and BQP (Bohm-Quantum-Potential) models has also been taken into consideration. The analyzed simulation results are discussed in Sect. 4.

4 Performance Investigation of Gate-Stack TMG: SOI-MOSFET in Re-S/D Technology

This section represents the short-channel electrical performance of the proposed SOI-MOSFET. Figure 2 represents the drain-current versus gate-voltage (I_d vs. V_{gs}) characteristics of the proposed MOSFET and referenced state-of-the-art [28] at $T = 300$ K. It is observed that the proposed GS technique in TMG: SOI MOSFET helps to reduce off-state-leakage significantly in comparison to SOI-MOSFET [28].

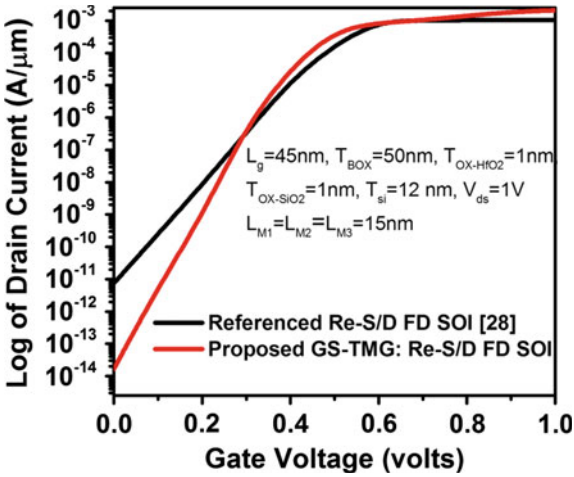

Fig. 2 The plot of drain-current (I_d) with variation in gate-voltage (V_{gs}) for proposed and reference FD SOI-MOSFET [28]

The suggested and referenced FD SOI offers off-state (I_{off}) of 0.169 fA and 7.5 pA and on-current (I_{on}) of 2.13 mA and 1.12 mA, respectively. This corresponds to the higher switching performance ($I_{on}/I_{off} = 10^{11}$) in the case of proposed GS: TMG SOI MOSFET than the referenced device ($I_{on}/I_{off} = 10^{9}$) at $L_g = 45$ nm. This is due to the reduced off-state gate tunneling in gate-stack FD SOI-MOSFET.

Also, the metal-gate-engineering will offer step-like potential-profile, which helps to increase the control of gate over the channel and the considerable reduction in drain-electric-field penetrations at higher V_{DS}, i.e., lesser DIBL effect. Similarly, the output drain characteristic (I_d vs. V_{ds}) of the devices is shown in Fig. 3. It is inferred from the plot that the proposed MOSFET results in improved current behavior than reference FD SOI MOSFET [28]. Also, the variation of subthreshold-slope (SS) at different BOX oxide thickness and $L = 45$ nm is shown in Fig. 4. It is found

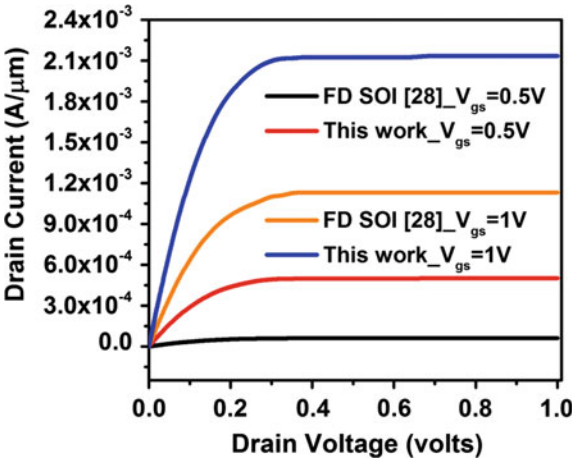

Fig. 3 The plot of drain-current (I_d) with variation drain voltage (V_{ds}) at different V_{gs} for proposed and reference FD SOI-MOSFET [28]

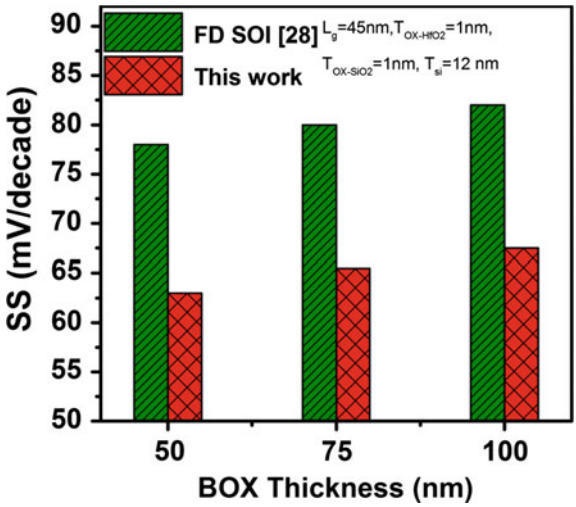

Fig. 4 The plot of subthreshold-slope at different BOX thickness (50–100 nm) at $L = 45$ nm for proposed and reference FD SOI-MOSFET [28]

that the proposed device offers a lesser value of subthreshold-slope as compared to referenced device [28]. This is due to the lesser off-state leakage in case of proposed FD SOI as compare to referenced device.

Next, the DIBL effect due to change in T_{BOX} (50–100 nm) and channel-length (30–60 nm) is monitored on the basis of TCAD-simulations for the proposed device. The result of TCAD simulation for the analysis of DIBL with variation in drain bias from $V_{ds} = 0.5$ V to $V_{ds} = 1$ V is drawn in Fig. 5. A noticeable reduction is seen, as the proposed MOSFET exhibits very less value of DIBL even at $L_g = 30$ nm. This

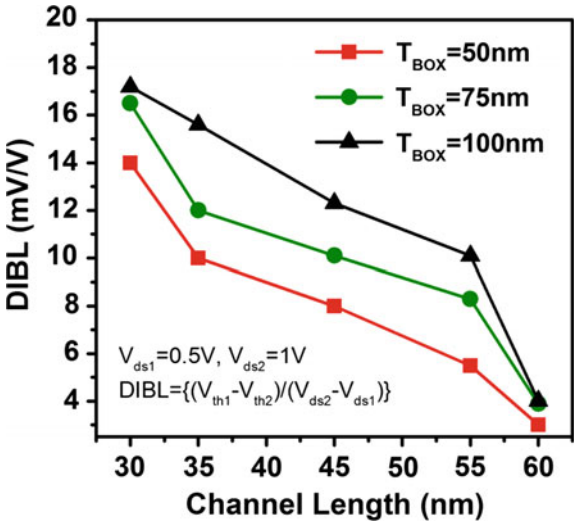

Fig. 5 The plot of DIBL at different channel length for proposed SOI-MOSFET

performance is due to the suggested technique of high-k stack in Re-S/D; gate/spacer engineered nanoscaled SOI-MOSFET.

4.1 Impact of Temperature on Gate-Stack TMG: SOI-MOSFET in Re-S/D Technology

This section discusses the impact of temperature variation on DC and analog behaviour of studied nanoscaled gate-stack SOI-MOSFET. Here, firstly the effect of change in operating temperature on drain-current performance is taken under study. Figure 6 shows the I_d versus V_{gs} plot of the studied device with change in device temperature over the range 200–400 K. It is clear from the analysis that the off-current and on-current both take a shift when the operating temperature increases. The increment in I_{off} at higher temperature is due to the effect of thermal generation/ionization and reduction in I_{on} may be due to the scattering phenomenon [23]. However, these changes are minimal in the case of the studied device, and the resulting current behavior is acceptable even at $T = 400$ K.

Next, the exact analysis of I_{off} with variation in device temperature and T_{BOX} is shown in Fig. 7. The device represents better off-state behavior and optimum drain current even at 400 K. Similarly, the calculated switching ratio (I_{on}/I_{off}) ratio at different operating temperature dictates that I_{on}/I_{off} ratio of the device has been reduced from 10^{12} to 10^{9} with the increase in temperature from 200 to 400 K. So, the analysis itself explains that the MOSFET could be further analyzed for low-power circuit applications.

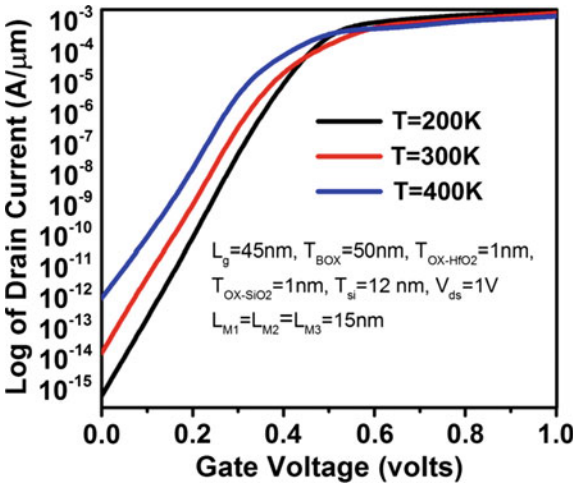

Fig. 6 Impact of temperature on drain current (I_d vs. V_{gs} characteristics) for the proposed SOI-MOSFET at $T =$ 200–400 K and $L_g = 45$ nm

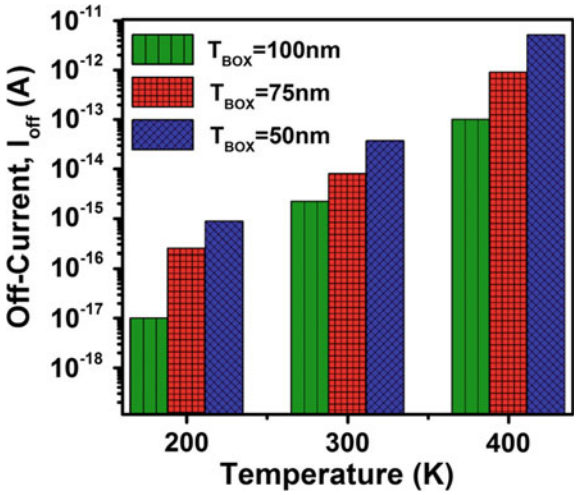

Fig. 7 Impact of temperature on sub-threshold leakage-current (I_{off}) for the proposed SOI-MOSFET with variation in T_{BOX} = 50–100 nm at $L_g = 45$ nm

4.2 Impact of Temperature on Analog Performance

The analog performance study of proposed nanoscaled SOI-MOSFET at different temperatures is discussed here. Here, TCAD simulations have been performed for the analysis of transconductance, $g_m = \partial I_d/\partial V_{gs}$, output-conductance, $g_d = \partial I_d/\partial V_{ds}$, and transconductance-efficiency-factor, TEF $= g_m/I_d$. Figure 8 represents the analysis of transconductance versus gate voltage with variation in temperature from 200 to 400 K at $L_g = 45$ nm. One can observe from the plot that the device exhibits better transconductance behavior. As, the device offers transconductance of 4.07 mS at $T = 300$ K and approximately increases (decreases) by 11% (21%) at $T = 200$ K (400 K). So, the device will offer higher gain even at $T = 400$ K.

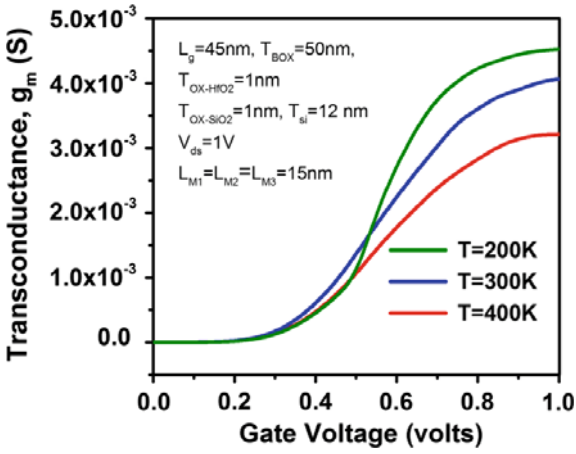

Fig. 8 Temperature-dependent transconductance analysis of studied SOI-MOSFET with variation in V_{gs} at T = 200–400 K and $L_g = 45$ nm

Similarly, the plot of *TEF* versus V_{gs} is drawn in Fig. 9. *TEF* value represents the effectiveness of drain-current and transconductance with the thermal behavior of device-to-circuit co-designs. The ratio of transconductance and drain-current defines TEF. Also, the value of *TEF* must be lower in the strong-inversion regime and higher in weak-inversion. A similar trend is seen in the case of the proposed device. Moreover, less deterioration is recorded when temperature varied from 200 to 400 K. So, the device can also be suggested for high-gain analog applications in highly linear and thermal stable mode. In continuation, the analysis of output conductance versus V_{ds} at $T = 200$–400 K and $L_g = 45$ nm is drawn in Fig. 10. In order to achieve the higher gain in analog ICs, g_d must be as low as possible. One can find from the plot that as the drain-voltage is applied, g_d starts decreasing after $V_{ds} = 0.2$ V, 0.24 V

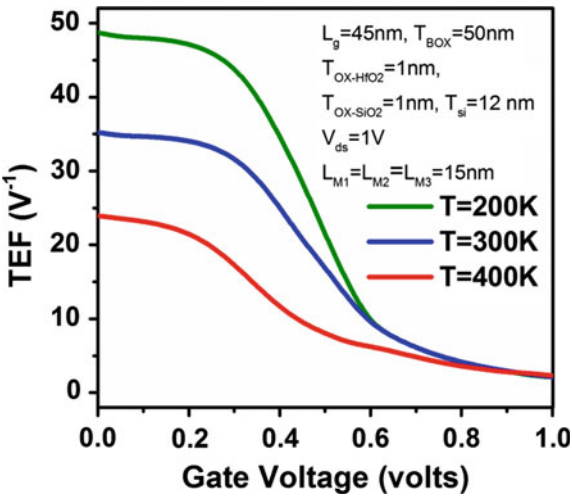

Fig. 9 Temperature-dependent analysis of transconductance-efficiency-factor (TEF) with variation in V_{gs} at $T = 200$–400 K and $L_g = 45$ nm

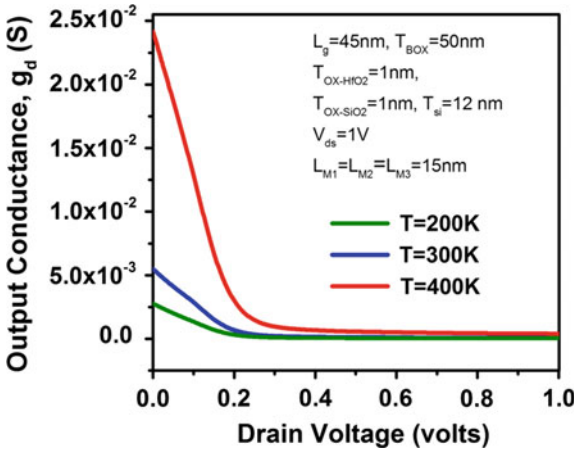

Fig. 10 Impact of temperature on output conductance with variation in V_{ds} at $T = 200$–400 K and $L_g = 45$ nm

Table 2 Performance parameters of GS-TMG: Re-S/D FD SOI FDSOI MOSFET at $L = 45$ nm, $T_{BOX} = 50$ nm and $T =$ 200–400 K

Parameters	Temperature		
	$T = 200$ K	$T = 300$ K	$T = 400$ K
I_{off} (A)	6.67×10^{-16}	1.69×10^{-14}	1.05×10^{-12}
I_{on} (A)	2.33×10^{-3}	2.13×10^{-3}	1.7×10^{-3}
Switching ratio (I_{on}/I_{off})	3.49×10^{12}	1.26×10^{11}	1.61×10^{9}
DIBL (mV/V)	8.2	8.9	15.5
g_m (mS)	4.53	4.07	3.21
TEF (V^{-1})	48.74	35.21	23.95
g_d (mS)	0.004	0.007	0.041

and 0.28 V at $T = 200$ K, 300 K and 400 K respectively. Moreover, the increase in g_d is considerable even at $T = 400$ K.

The overall analysis of the aforementioned SOI-MOSFET with variation in temperature is listed in Table 2. It is worth to mention that the high-k oxide-stack multi-metal-gate engineering technique is advantageous in recessed-S/D technology-based SOI-MOSFETs. Hence, this analysis itself dictates the device applicability in low-power thermally-stable analog-circuit and systems.

5 Conclusion

This paper investigates the impact of high-k gate-stack and metal-gate engineering on the performance of recessed-S/D technology-based FD SOI-MOSFET. The studied device exhibits enhanced short-channel immunity with improved temperature sensitivity at $L_g = 45$ nm. As the device offers $I_{off} = 0.169$ fA (1.05 pA) and $I_{on} = 2.13$ mA (1.7 mA) at $T = 300$ K (400 K) and $L = 45$ nm. This results in I_{on}/I_{off}-ratio of 10^{11} (10^{10}) at $T = 300$ K (400 K), which is significant to off-flow the subthreshold-leakage in nanoscaled-MOS devices. Next, the higher value of transconductance enables the device application in high gain analog amplifiers. Similarly, the device signifies the better *TEF* value of 35.21 V^{-1} at $T = 300$ K and decreases (increases) at $T = 400$ K (200 K) in weak-inversion regime. The resulting value of *TEF* dictates the device applicability in highly-linear ICs with improved thermal stability. Further, the device also offers the lower value of output-conductance at $T = 300$ K and $L = 45$ nm, which is desired for higher intrinsic-gain. So, the studied MOS-device could be suggested as an alternative for low- power analog circuits in the near future.

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A Novel Compact 360° Azimuth Scanning Antenna Array for L-Band Applications

Sanjana Paul, Pallepogu Prasanna Kumar, and Prerna Saxena

1 Introduction

Scanning antenna arrays play a significant role in different applications like satellite communications, telecommunication, UAV (unmanned aerial vehicles), etc. The scanning procedure generally involves the use of antenna arrays or a single antenna structure. The antenna arrays are preferred over single element structure because of their accuracy, and with modern wireless application in longer range enforced systems, the high gain scanning antenna array is employed [1]. The scanning antenna array involves beam steering in desired directions. The different array configurations as per geometry are linear, planar, and circular. Planar scanning involves scanning in azimuth plane and elevation plane. The general trend is that azimuth plane scanning is used more than the elevation plane scanning due to widespread applications.

There are beam forming networks as well as beam steering techniques which are used for scanning purposes, but beam steering is more preferred due to its simpler designs with reduced computational complexity [2]. The beam steering can be exercised either electronically [3] or mechanically. The electronic and mechanical beam steering methods involve almost equal computational complexity, but the mechanical beam steering structure escalates the pay load of the system, while the electronic beam steering circuitry aids in bringing down the load on the system. The electronic beam steering uses more of the digital circuitry which are elements of comparatively smaller dimensions.

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We have proposed a circular antenna array for beam steering applications in the L-band (1.52–1.72 GHz). The L-band ranges from 1 to 2 GHz with 30–15 cm wavelength range. The applications of this band are wide spread like radars, global positioning systems (GPS), radio, telecommunications, and aircraft surveillance. This band has lower bandwidth on account of its shorter frequency range. This particular band was chosen because of its special properties like not suffering from large signal loss as encountered by high frequencies when delivered over copper coaxial cables, being less tractable to interventions in the channel and providing a devoted link [4]. These usable properties make this band suitable to be incorporated in remote surveillance and operations governance frameworks. The beam steering technique is employed in this band so as to aid in better radar structures involving efficient scanning mechanisms with reduced computational complexity.

The antenna array employs microstrip patch antennas as elements. The motivation behind choosing a microstip element is the ease of fabrication, low-cost, low-profile, and light-weight structure [5, 6]. Slots are used to expand the bandwidth of the antenna element [7, 8], and hence, the element we have proposed has a slotted patch structure. This proposed antenna array is employed for 360° scanning in the azimuth plane with a minimalistic structural configuration.

As per the state-of-the-art designs, there exist different techniques for planar scanning like the usage of high-impedance surface multi-beam antenna grounded on surface-wave, ferrite loaded circular waveguide antenna, hybrid phased array, and pattern reconfigurable antennas [9]. In a hybrid inclined and interlaced active phased array, exercising an electrical elevation scanning and mechanical azimuth scanning devised to receive signals at (12.25–12.75 GHz) and transmit signals at (14.0–14.5 GHz) employing a radiation element which is a type of waveguide antenna supporting dual polarizations. It achieves 15–75° elevation scanning and 0–360° azimuth scanning and a gain loss of maximum 4.0 dB [10]. In a ferrite loaded circular waveguide antenna, packed with a concentric ferrite cylinder which is axially magnetized, it exhibits an azimuth scan range of 360° and an elevation scan range of 60° [11]. In a method, high-impedance surface multi-beam antenna which is grounded on surface wave exhibiting full azimuth coverage is used for scanning which has 28 feeding ports employing 7 in each beam forming network (BFN) which employs leaky-wave principle and surface-wave excitation. The proposed antenna has widened scanning range and comparatively compact size, and it features single layer configuration which is low profile and low cost [12].

In a pattern reconfigurable antenna, at a fixed resonance frequency of 2.4 GHz, the boresight and conical radiation patterns can be reconfigured which is advantageous when operating at boresight mode in the azimuth plane exhibiting adaptive polarization scanning over 360° with 6.05 dBi gain and 86.7% efficiency measured in the boresight mode, corresponding to conical mode gain and efficiency of 4.39 dBi and 82.4%, respectively [13]. For a cylindrical active frequency-selective surface (AFSS) and a planar feed array (with elevation plane beam scanning by a reference antenna which is an array fed metallic reflector) which is analyzed at S-band (2.4–2.5 GHz) has 360° sweeping beam in azimuth and +16°/15° beam steering in elevation giving a maximum gain of 9.2 dBi [14]. In [15], a p-i-n diode switch controlling a group of

shorting vias connected to six parasitic elements, and a radiating patch comprised in a single patch element operating from 5.1 to 5.9 GHz. It achieves 360° beam scanning, 10 dBi gain, 42° azimuth beam-width, and 97° elevation beam-width. In a cylindrical approach for L-band with operational precision at 1.45 GHz, the antenna elements are arranged along each of subarray along the length of the cylindrical shape for elevation scanning and those along the circumference for azimuth scanning. There are 24 subarrays with 6 antenna elements each summing up to a structure with 144 antenna elements [16].

The existing antenna array design technology has to be improvised so as to give out efficient beam steering capability overcoming the limitations of bulk of the end product, environmental factors, smart power consumption, and satisfying the space requirements of vehicular and mobile installations. Hence, the preference of low-profile antennas employed in the structure is well justified. In our design, we concentrate on full axis azimuth scanning with microstrip patch element array. A circular array with antenna elements steered electronically serves the purpose.

The state-of-the-art employs phase shifters as a major module of the beam steering circuitry which is basically used for higher frequency ranges and is being used for lower frequency bands too. The involvement of phase shifters involves the use of bulky circuitry for its feed and control purposes [17]. The beam steering circuit has to be made less bulky and minimalistic, and hence, we have to avoid the implementation of phase shifters. The wide angle scanning arrays have come into picture in the recent years [18, 19]. The proposed antenna array is also a wide scanning antenna array. Our aim is to propose a 360° azimuth scanning antenna array along with its electronic steering circuit setup which has a compact size. The rest of the paper is organized as follows. Section 2 presents the proposed antenna array design, power divider design, and power divider embedded antenna array designs. In Sect. 3, the proposed beam steering circuit is presented along with its simulation results followed by conclusion in Sect. 4.

2 Design Process

The analysis, design and simulation of the proposed antenna element, antenna array, and power divider are carried out using ANSYS HFSS (High-Frequency Structure Simulator).

2.1 Antenna Array Design

The design of the proposed inset-fed microstrip patch element is given in Fig. 1a. The design parameters are W_p (width of the patch) = 61 mm, L_p (length of the patch) = 45.5 mm, h_p (height of the patch) = 0.035 mm, W_s (width of the substrate) = 80 mm, L_s (length of the substrate) = 80 mm, h_s (height of the sub-

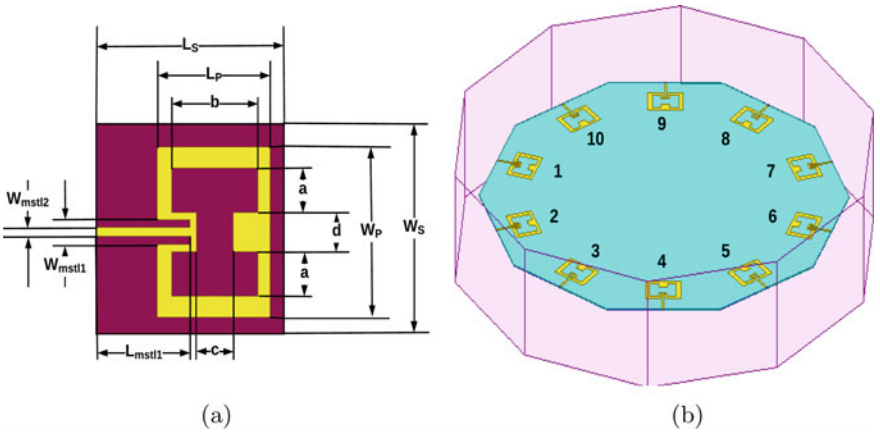

Fig. 1 Proposed **a** antenna design **b** antenna array design

strate) = 1.6 mm, W_{mstl1} (width of the microstrip transmission line) = 3 mm, L_{mstl1} (length of the microstrip transmission line) = 40 mm, and W_{mstl2} (width of the inset feed) = 9 mm. To enhance the bandwidth, an I-shaped slot is incorporated in the patch. The slot dimensions are $a = 15$ mm, $b = 35$ mm, $c = 15$ mm, $d = 15$ mm.

The substrate is FR-4 Epoxy which has $\varepsilon_r = 4.4$ and $\tan\delta = 0.02$.

The design equations are given as [20]:

$$W_p = \frac{c}{2f_r\sqrt{\frac{\varepsilon_r+1}{2}}} \tag{1}$$

$$\varepsilon_{\text{reff}} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\frac{1}{\sqrt{1+\frac{12h_s}{W_p}}} \tag{2}$$

$$\Delta L_p = 0.412h_s\frac{\varepsilon_{\text{reff}}+3}{\varepsilon_{\text{reff}}-0.258}\frac{\frac{W_p}{h_s}+0.264}{\frac{W_p}{h_s}+0.8} \tag{3}$$

$$L_p = \frac{c}{2f_r\sqrt{\varepsilon_{\text{reff}}}} - 2\Delta L_p \tag{4}$$

$$W_s = W_p + 12h_s \tag{5}$$

$$L_s = L_p + 12h_s \tag{6}$$

Ten antenna elements are used and are arranged in circular-decagon configuration with spacing between the elements as $\frac{\lambda}{2}$. The spacing is 84.9 mm, and radius is 319 mm as indicated in Fig. 1b.

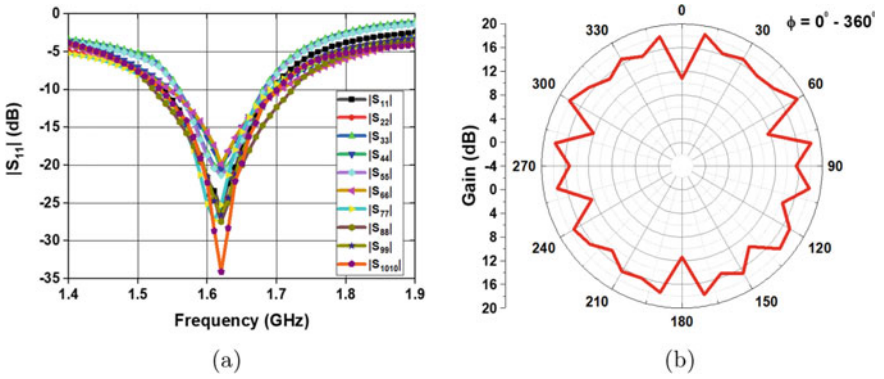

Fig. 2 **a** $|S_{11}|$ of antenna array; **b** gain of proposed antenna array

The obtained $|S_{11}|$ at design frequency is -34.0668 dB as given in Fig. 2a. The maximum azimuth gain obtained is 18.68 dB. The simulation results of the gain obtained on exciting the entire array are given in Fig. 2b.

2.2 *Power Divider Design*

For designing the array feed network, we have used power dividers. The proposed power divider has dimensions $a = 3.2$ mm, $b = 25.2$ mm, $c = 31.6$ mm, $d = 10$ mm, $e = 48$ mm, $f = 28$ mm, $g = 1.6$ mm, $h = 38$ mm, and the design is given in Fig. 3a. The power divider gave $|S_{11}|$ of -23.89 dB and S_{21} and S_{31} of -3.2 dB, and the simulated S parameter graph is given in Fig. 3b.

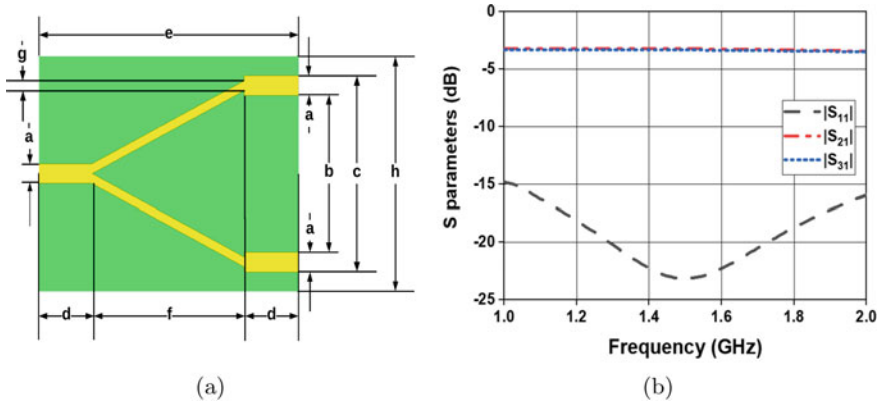

Fig. 3 **a** Proposed power divider; **b** *S* parameters of power divider

Parametric studies are carried out on the initial power divider, and the different power divider designs proposed are given in Fig. 4. The design with the best compatibility for the antenna array in case of dimensions and $|S_{11}|$ is chosen, and it is design (b).

2.3 *Antenna Array Integrated with Power Divider*

The optimization of the antenna array feeding network aids in improving the quality of the array framework in case of efficient feeding network as well as reduced complexity. The proposed power divider is embedded on the antenna array and simulated so as to know the variation on the $|S_{11}|$ of antenna array and bandwidth. The proposed 1:2 power divider results in 5 antenna pairs as given in Fig. 5a. The $|S_{11}|$ is −20.4348 dB, and the bandwidth obtained is 140 MHz as given in Fig. 5b.

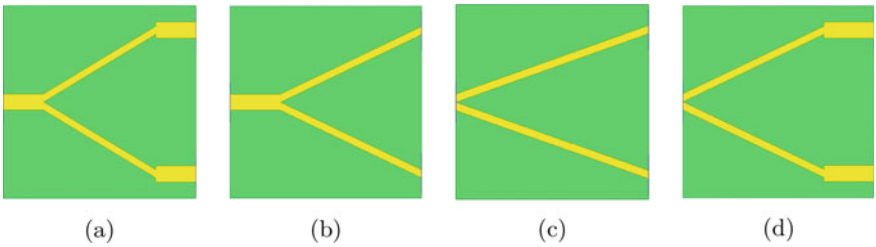

Fig. 4 Power divider designs

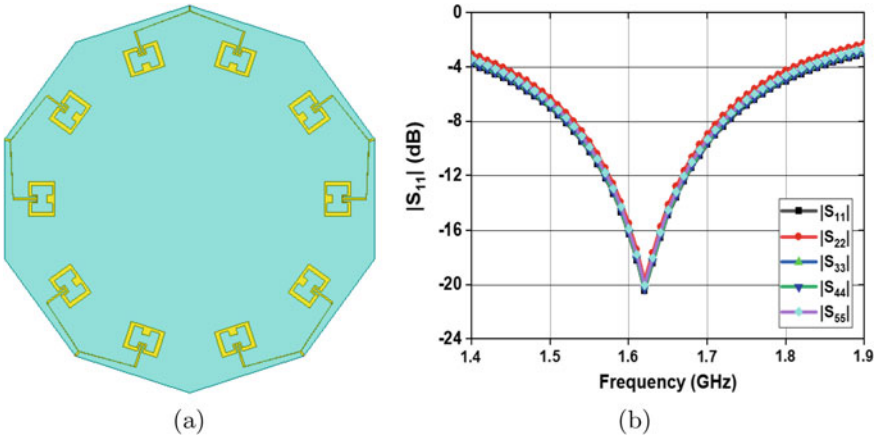

Fig. 5 **a** Proposed power divider incorporated in the antenna array; **b** $|S_{11}|$ of proposed power divider integrated antenna array

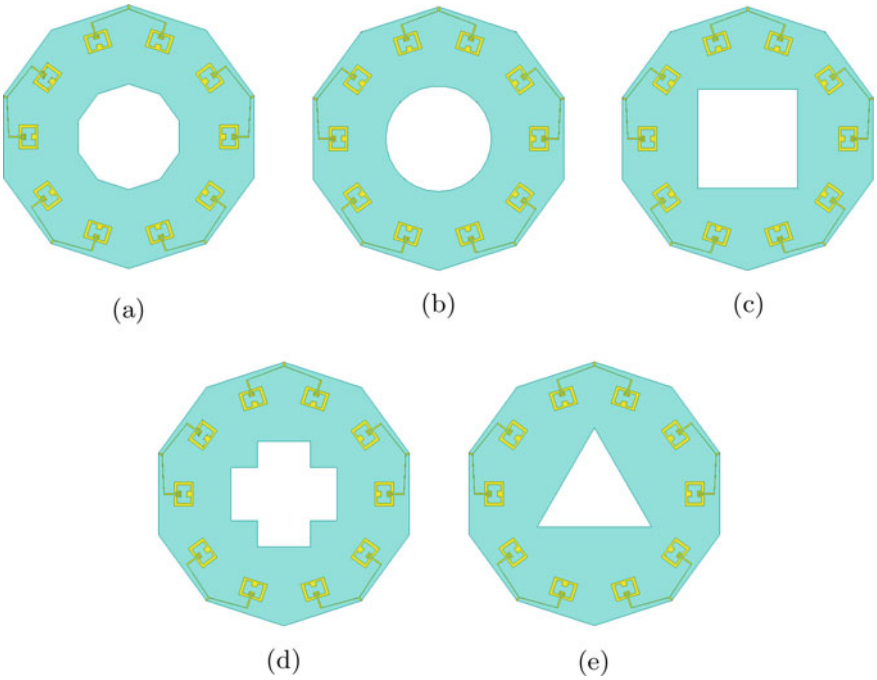

Fig. 6 Power divider integrated antenna array with **a** decagon (mirror) slot; **b** circular slot; **c** square slot; **d** plus slot; **e** triangle slot

The different slots introduced are a decagon (mirror) slot as given in Fig. 6a with radius 200.8 mm, a circular slot as given in Fig. 6b with radius of 200.8 mm, a square slot as given in Fig. 6c with side of 133.4 mm, a plus slot as given in Fig. 6d with cross lengths of 66.7 mm and 133.4 mm, and a triangle slot as given in Fig. 6e with side of 182.6 mm.

The resemblance of the configuration of each slot to the configuration of the antenna array plays a key role, and we can see that as the slot starts to resemble the array configuration, we observed that the bandwidth improves and that the resonating frequency also starts approaching that of the proposed antenna array. The bandwidth and $|S_{11}|$ values obtained for the slotted arrays can be observed as given in Fig. 7a for decagon (mirror) slot, Fig. 7b for circular slot, Fig. 7c for square slot, Fig. 7d for plus slot, and Fig. 7e for triangle slot.

The decagon (mirror) slotted power divider integrated array was found to be better than the others exhibiting $|S_{11}|$ of -20.89 dB and maximum bandwidth of 160 MHz. The comparison table between different power dividers embedded arrays is given in Table 1.

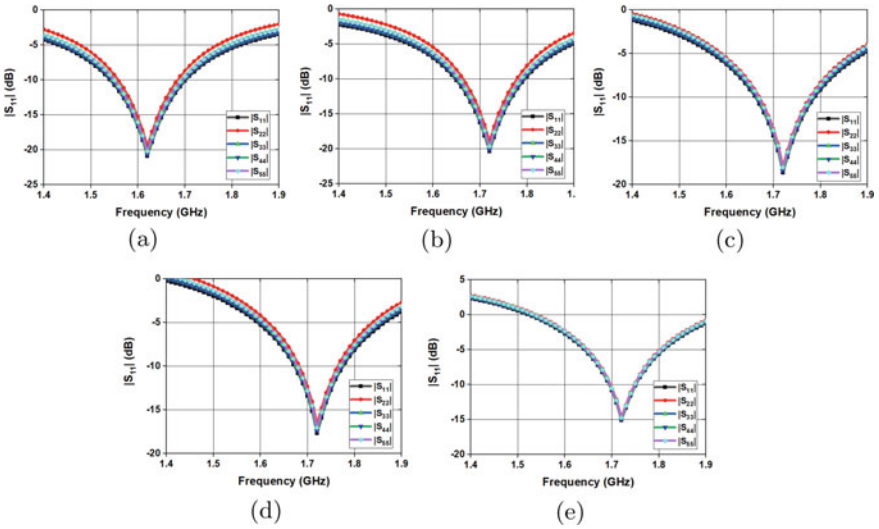

Fig. 7 $|S_{11}|$ for **a** decagon slotted array; **b** circular slotted array; **c** square slotted array; **d** plus slotted array; **e** triangle slotted array

Table 1 Comparison of power divider embedded arrays with and without slots

Type of slot	$\lvert S_{11}\rvert$ (dB)	Bandwidth (MHz)	Resonating frequency (GHz)
No slot	−20.43	140	1.62
Decagon	−20.89	160	1.62
Circular	−20.38	140	1.72
Square	−18.65	120	1.72
Plus	−17.67	90	1.72
Triangle	−15.12	60	1.72

3 Results and Discussion

The 360° beam steering in azimuth plane is demonstrated in simulation on exciting antenna pairs sequentially. The five sequential radiation patterns on exciting each antenna pairs are given in Fig. 8.

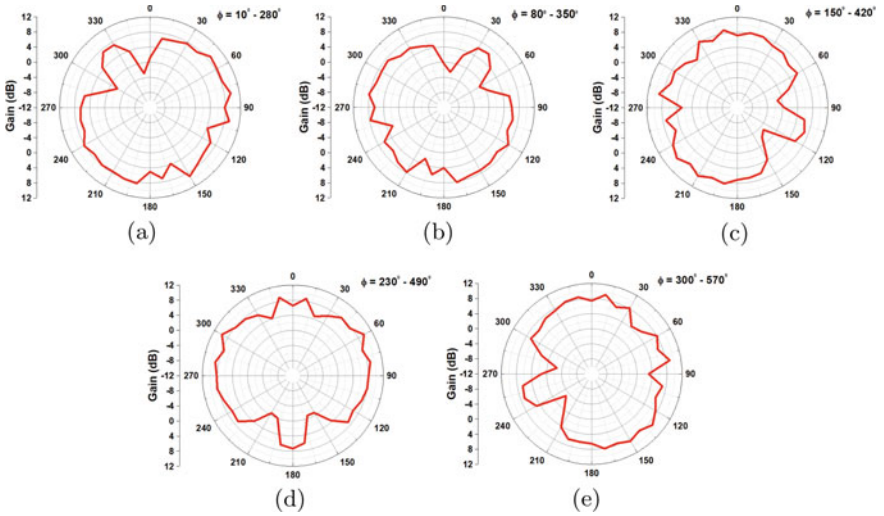

Fig. 8 Gain on exciting antenna elements **a** 1 and 2; **b** 3 and 4; **c** 5 and 6; **d** 7 and 8; **e** 9 and 10

3.1 Beam Steering Circuit

The proposed beam steering circuit is given in the block diagram in Fig. 9. It has an RF section with the antenna array, SP5T RF switch, and RF detector modules; a digital control section with microcontroller comprising of the comparator and ADC (analog to digital converter) modules and a display section.

The 10 antenna elements are divided into 5 pairs. Each pair has a radiation pattern and a radiated power value. These 5 pairs are activated using an SP5T RF Switch which sends the RF input power received by it to each RF pair input based on the control line input given using microcontroller. All 5 radiated power values are saved

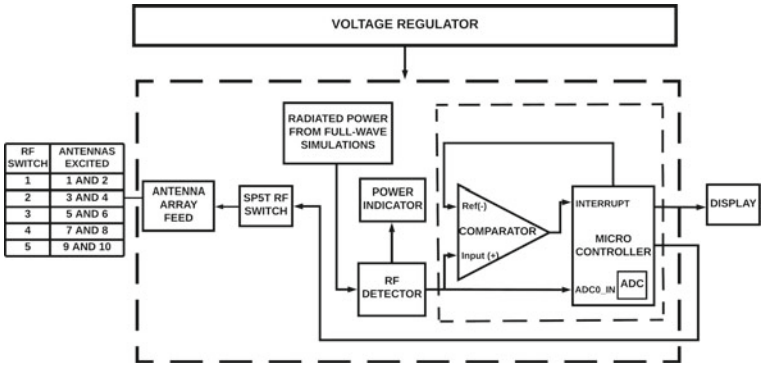

Fig. 9 Block diagram of proposed beam steering circuit

Table 2 Beam steering sequence

RF pair excited	Azimuth angle (ϕ) range (°)	Radiated power (dB)
RF pair 1	10–280	15.56
RF pair 2	80–350	16.12
RF pair 3	150–420	19.44
RF pair 4	230–490	20.33
RF pair 5	300–570	19
Entire array	0–360	17.59

in the microcontroller registers. The microcontroller gives input for the RF switch to select the first RF pair to feed it, and the output is given to the RF detector IC, and this is demonstrated using the potentiometers. The input received by the RF detector is converted to DC voltage and is fed to the microcontroller's ADC input. There is a maximum power value saved in a register of the microcontroller after converting it to a voltage value. The reference of the comparator is the saved maximum power value (which is the voltage converted value). If the input voltage given to the comparator is greater than the reference voltage, then the input value which was also fed at the ADC is used to update the maximum power value to a new value (which is also a voltage value). This new maximum value is converted to power and is displayed on an LCD display. The current power and maximum power are displayed. This is one cycle. Then the next power value is read by the RF detector, and the above cycle is repeated. The maximum power values are updated in the further cycles. This is done for all 5 power values. Each cycle occurs in a difference of 5s. The time delay can be varied according to our convenience.

The software simulation is done using PROTEUS 8, and the microcontroller programming is done via MPLABX IDE. The software simulation circuit is demonstrated using the PIC16F877A microcontroller, LM044l LCD using the ADC units of the controller, the RF power detector module, and SP5T RF switch module. We have used sub-circuit model to define the RF SP5T switch board and RF power detection and input board. The sub-circuit for RF detector (LT-5534) is a simple potentiometer connection between the Rx pin and VOUTx pin ($x = 1, 2, 3, 4, 5$). The sub-circuit for the SP5T RF (ADRF5250) switch is a 3:8 decoder with 5 digital to analog converter (DAC) modules at the outputs of 3:8 decoder. The simulation circuit is given in Fig. 10. The sub-circuits for the RF detection and input module and the SP5T RF switch are given in Figs. 11a and b, respectively.

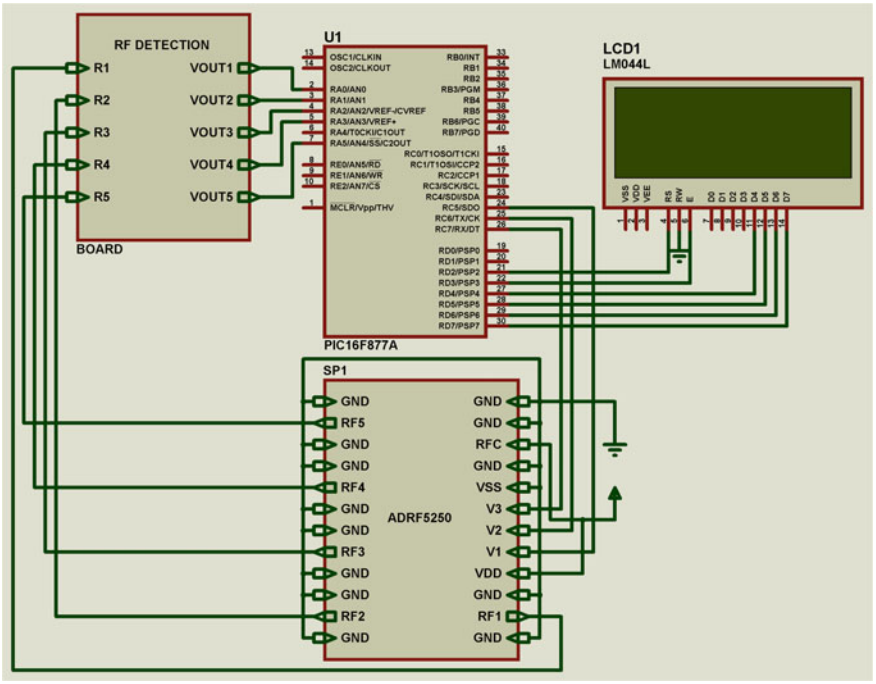

Fig. 10 Simulation circuit of the proposed beamsteering network

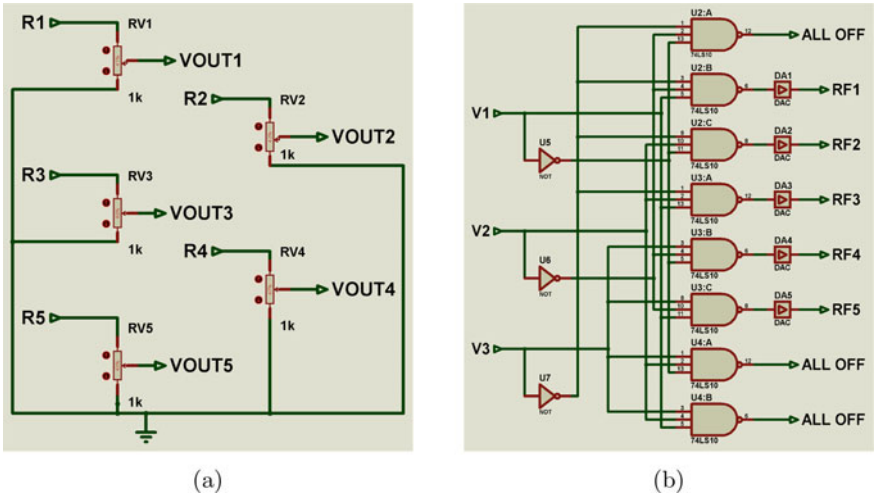

Fig. 11 Sub-circuit for **a** RF detection and input module; **b** RF SP5T switch module

Table 3 Comparison of the proposed antenna array with state-of-the-art designs

References	Frequency range (GHz)	No. of elements and array configuration	Type of antenna	Maximum bandwidth (MHz)	$\|S_{11}\|$ (dB)
[9]	1–2	81 (9 × 9) Multiscale	Annular slot	40	−16.7
[10]	12–15	384 (32 × 12) stair	Slotted waveguide	250	−38.13
[11]	8–12	1 NA	Circular waveguide	360	−29.43
[12]	23–27	625(25 × 25) square	Microstrip patch	2000	−31
[13]	2.37–2.46	1 NA	Shorted microstrip patch	90	NA
[14]	2.4–2.5	8 Linear	Dipole	100	−45
[15]	5.1–5.9	1 NA	Reconfigurable	660	−21
[16]	1–2	144 (24 × 6) cylinder	Bowtie	360	−25.1
This work	1–2	10 circular decagon	Microstrip patch	470	−34.067

4 Conclusion

A 360° azimuth scanning antenna array for electronic beam steering applications in L-band (1.52–1.72 GHz) was designed starting with microstrip patch element giving $|S_{11}|$ of −21.65 dB, VSWR of 1.44, and a gain of 10.99 dB. The antenna element array with 10 elements placed in a circular-decagon configuration at an element spacing of 84.9 mm and array radius of 319 mm gave $|S_{11}|$ of −34.0668 dB and gain of 18.68 dB. The power divider fed antenna array and the proposed beam steering were demonstrated in simulation by exciting antennas in pairs giving radiated powers of 15.56 dB, 16.12 dB, 19.44 dB, 20.33 dB, and 19 dB, respectively, on exciting pairs 1, 2, 3, 4, and 5, respectively as shown in Table 2. The comparison shown in Table 3 shows that the proposed beam steering array is novel, compact, and has wide bandwidth, making it suitable for L-band applications.

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Analysis of Image Segmentation Algorithms for Infrared Images

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1 Introduction

IR sensors deal with a broad range of wireless applications. The key areas are night vision, temperature monitoring, climate monitor, pressure control, pedestrian recognition, indoor appliances, blood glucose control, security surveillance, fire detection, and may more [1–3]. The infrared electromagnetic spectrum is broadly classified into three categories: far IR region, mid IR region, and near IR region as shown in Table 1.

Object segmentation is the first step in pattern recognition. Object recognition in visible images is efficient and popular than IR image segmentation. An IR imaging sensor offers higher visibility in contrast to visible digital sensors in dark surroundings. Recently, IR imaging cameras have established extensive use in many applications. The essential step in IR object recognition and pattern recognition is segmentation of image, which separate out desired objects from the dark surroundings [4, 5].

Basically in visible image, much information is used for segmentation such as gray-level, texture information, color, etc. But in case of IR images, temperature variation is the limited information available for segmentation [1]. IR images facing problem of low SNR [2, 3, 6], moving object detection [7], and clutter [6, 7]. Comparing with color image, IR image has characteristics such as: (i) segmentation in absence of light, (ii) no shading problem, (iii) intrinsic variations are improved, and (iv) segmentation at large distance with diverse climate conditions [5, 8].

In this paper, we carry a study of image segmentation on IR images with basic algorithms and their comparisons. The sample images of human, animal, and object have been captured using SeekThermal IR sensor. Section 1 has an introduction of IR image sensors with applications. Section 2 introduces basic image segmentation algorithms; Sect. 3 has comparison of image segmentation algorithms and results. Finally, conclusion is made in Sect. 4 of the paper.

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Table 1 IR sensor range in electromagnetic spectrum

Range	IR region	Application
3000 nm to 1 mm	Far-IR region	Thermal imaging
1400–3000 nm	Mid-IR region	Heat sensing
700–1400 nm	Near-IR region	IR sensors, fiber optic

2 Image Segmentation Algorithms

2.1 Ostu Method

Nobuyuki Otsu [9] proposed a popular image segmentation method known as Ostu thresholding. This method assumes bimodal histogram of image with two classes of intensity, object pixels, and background pixels. This method calculates minimum intra-class variance for optimal threshold that separates object pixels and background pixels.

Algorithm 1 Ostu Algorithm

Input: IR Image
Output: Binary Image

1: Calculate histogram with probabilities of each gray-level value.
2: Locate opening class means and opening class probability.
3: Walk throughout all probable thresholds highest intensity.
4: Revise means and class probability.
5: Calculate variance between object-class and background-class.
6: Optimal threshold subjected to the highest value of variance among object-class and background-class.
7: Stop.

Ostu thresholding method is fast, and on the other hand, it assume bimodal histogram and illumination should be uniform.

2.2 Max Entropy Method

Maximum entropy method [10] is analogous to Otsu thresholding method. Here, rather than calculating minimum intra-class variance, the maximum inter-class entropy is calculated. This method includes prior knowledge about object to be segmented [11]. Entropy determines the ambiguity of an event. Entropy is calculated by Eq. 1.

$$E = -\sum_{x=0}^{L-1} p \times \log_2(p) \tag{1}$$

p is the probability of gray-level value (L) in image.

2.3 Triangle Method

The geometry-based method for image segmentation is proposed by Zack et al. [12] known as triangle method. This method presupposes a highest mode close to one end and look for the other end of the histogram. This algorithm is efficient subjected to the object pixels construct a frail peak in the gray-level histogram of an image.

2.4 Percentile Method

Doyle [13] proposed method for selecting the threshold value based on percentage of object and background pixels. If it is known in prior that object is brighter or darker than surrounding with some percentage (p), then threshold is calculated in a way that p object pixels are under this gray-level value.

3 Comparison of Image Segmentation Algorithms

Before we describe the comparison of image segmentation algorithms in details, we initial introduce the IR sensor used for this study. Figure 1a shows the SeekThermal 206 × 156 Thermal Sensor, model: Compact [16], and Fig. 1b shows example image captured from this camera in grayscale mode.

3.1 Experiments and Results

The experimental study is carried out on IR images (human, animal, and object) taken from SeekThermal IR sensor. Four image segmentation algorithms Ostu, Max Entropy, Triangle, and Percentile have been studied. The flowchart is shown in Fig. 2.

The IR images of human, animal, and object have been captured using SeekThermal IR sensor. The image is converted into gray level, and the noise has been removed using median filter in preprocessing step, after thresholding has been applied on filtered images. Finally, segmented area has been marked by red color. The process is summarized in Fig. 3. The segmentation efficiency is evaluated using parameters

(a) (b)

Fig. 1 IR imaging camera SeekThermal used for study. **a** IR sensor (compact); **b** grayscale image from IR sensor

Fig. 2 Flowchart of the IR image thresholding algorithm

recall, precision, Jaccard similarity index, dice similarity index, and absolute error rate. The details about evaluation parameters have been discussed in Sect. 3.2.

These algorithms were implemented in OpenCV java library and ImageJ software.

3.2 Evaluations

To validate results, recall, precision [3, 17], Jaccard similarity index (JSI) [2], dice similarity index (DSI) [2], and absolute error rate (a_{er}) [2] are used. Let A(O) represents number of object pixels segmented by the method and let A(T) total number of actual object pixels that was physically segmented. The recall is given as in Eq. 2.

$$\text{Recall} = \frac{A(O \cap T)}{A(T)} \tag{2}$$

The precision is given as in Eq. 3.

$$\text{Precision} = \frac{A(O \cap T)}{A(O)} \tag{3}$$

JSI(G_t, S_i) represents Jaccard similarity index for ground truth and segmented image. For better segmentation result, it is high and lower for it weak segmentation result. It is given by Eq. 4.

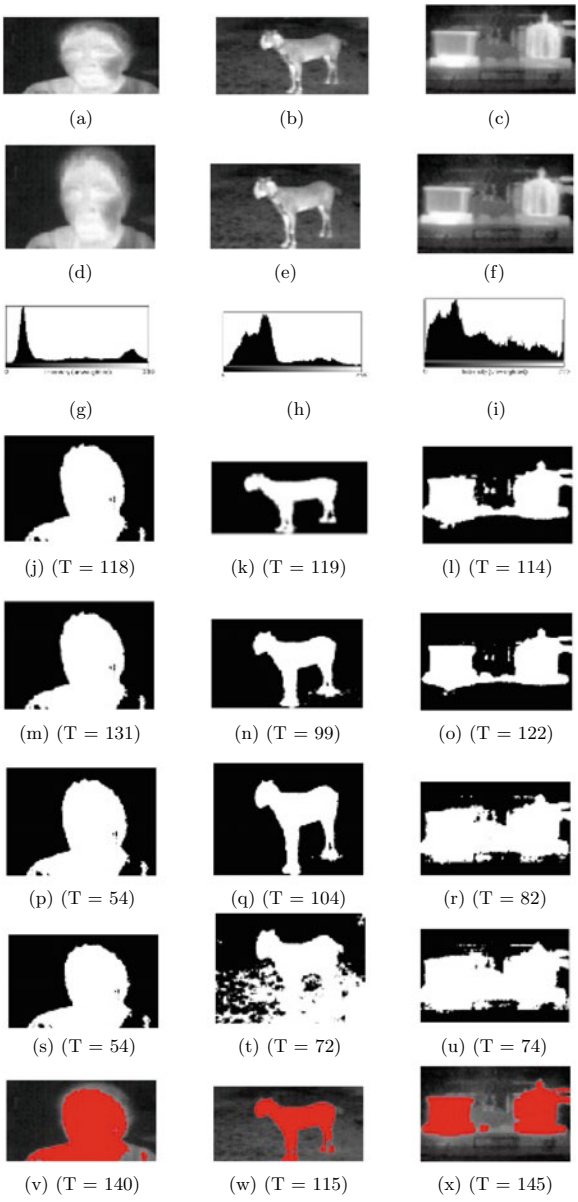

Fig. 3 Segmentation output. Figures **a**–**c** input images. Figures **d**–**f** preprocessing result. Figures **g**–**i** histogram of input images. Figures **j**–**l** segmentation results with Ostu method. Figures **m**–**o** segmentation results with max entropy method. Figures **p**–**r** segmentation results with triangle method. Figures **s**–**u** segmentation results with percentile method. Figures **v**–**x** segmentation results with ground truth (*T* represents threshold value)

Table 2 Results for thresholding algorithms

Method	Parameter	Object	Human	Animal
Ostu method	Precision	0.73	0.88	0.96
	Recall	1	1	1
	JSI	0.73	0.88	0.96
	DSI	0.85	0.94	0.98
	a_{er}	8.92	4.73	0.67
Max Entropy method	Precision	0.72	0.95	0.85
	Recall	1	1	1
	JSI	0.72	0.95	0.85
	DSI	0.84	0.97	0.92
	a_{er}	9.69	1.90	3.13
Triangle method	Precision	0.51	0.70	0.89
	Recall	1	1	1
	JSI	0.51	0.70	0.89
	DSI	0.68	0.83	0.94
	a_{er}	23.27	14.85	2.32
Percentile method	Precision	0.49	0.70	0.36
	Recall	1	1	1
	JSI	0.49	0.70	0.36
	DSI	0.80	0.24	1.93
	a_{er}	25.28	14.85	31.61

$$\mathrm{JSI}(G_t, S_i) = \left| \frac{G_t \cap S_i}{G_t \cup S_i} \right| \tag{4}$$

Dice similarity index (DSI) is as like as JSI and lies between 0 and 1. DSI is represented as in Eq. 5.

$$\mathrm{DSI}(G_t, S_i) = 2 \times \frac{|G_t \cap S_i|}{|G_t|\,|S_i|} \tag{5}$$

Absolute error rate (a_{er}) is ratio of absolute error (n_{er}) to total pixels of image ($M \times N$). It is given by Eq. 6.

$$\text{Absolute Error Rate } (a_{er}) = \frac{\text{Absolute Error } (n_{er})}{M \times N} \times 100 \tag{6}$$

Table 2 shows the comparison of results for thresholding algorithms. It shows that the global Ostu and Max Entropy shows good results with IR images.

4 Conclusion

This paper presents study of basic thresholding algorithms for IR images. It aims to analyze performance of thresholding algorithms for IR images. The input images object, human, and animal have been captured using SeekThermal IR sensor for study. This study is based on image thresholding of object, human, and animal IR images. The result shows that Ostu method outperforms best for IR image segmentation. By modifications in these methods will be used in future to reorganization of objects. This dataset under study is unique and limited. We proposed to develop a public dataset.

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Low-Area, High-Throughput Field-Programmable Gate Array Implementation of Microprocessor Without Interlocked Pipeline Stages

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1 Introduction

The processor architecture for microprocessors without interlocked stages (MIPS) developed by MIPS Technologies and Imagination Technologies has recently evolved from a 32-bit version to a 64-bit version. Compared with ARM processors, the MIPS core is compact, requires a smaller die size, and consumes less power, all while offering multi-threading capabilities, which increases its functionality. MIPS processors are often used in applications involving consumer audio devices, such as audio players, set-top boxes, DVD recorders and players, and digital displays, which are typically implemented with a multifunction system on chip.

Given that low power and high speed are important goals in these applications, reduced instruction set computer (RISC) architectures are preferred. The instructions are simple in RISC, and each instruction requires a similar number of clock cycles, making it easy to pipeline the instructions, thereby obtaining high throughput. Field-programmable gate arrays (FPGAs) are also popular as platforms for pre-silicon prototyping to accelerate verification and software development. Thus, exploiting low-area FPGAs to accelerate the implementation of MIPS processors is of significant importance.

Numerous research efforts have focused on MIPS architecture in the past. In 2019, Indira et al. implemented a 32-bit MIPS processor and targeted the same on a Xilinx Virtex 7 FPGA [1]. They also discussed possible pipeline hazards and the associated remedies. In 2017, Rashidah et al. proposed a simulator for the RISC-16 instruction set [2] that was based on visual basic programming and five pipeline stages. In 2016, Husainali et al. proposed a three-stage, 32-bit pipelined processor [3] that they designed in Verilog and implemented on a Xilinx Virtex 7 FPGA using Xilinx ISE

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software. In 2018, Mangalwedhe et al. proposed a low-power RISC processor [4] that they designed in Verilog. They used clock gating to reduce the dynamic power consumption and implemented the design on a Spartan 6 FPGA.

In 2014, Rakesh et al. proposed a novel architecture for a 17-bit address RISC processor [5]. They implemented their Harvard architecture-based design on a Xilinx FPGA. In the present work, we use high-level synthesis (HLS) to design a MIPS core and implement it on a Xilinx Virtex 7 FPGA target, and we compare this implementation with previous implementations. In the proposed design, we use multiple HLS directives to reduce the area and increase the speed. The results of the proposed FPGA are clearly superior to those of previous FPGAs.

The rest of the paper is organized as follows: Sect. 2 introduces HLS, and Sect. 3 presents the architecture of the MIPS processor that we designed and explains the method used in the proposed design. In Sect. 4, we discuss the techniques used to optimize the synthesis results. Specifically, we discuss in detail the HLS directives used during the design process, which lead to the optimal synthesis between design and the target FPGA. Section 5 presents the results of the simulation and synthesis and compares the results with those of other works for the same application. Finally, Sect. 6 concludes the paper.

2 High-Level Synthesis

HLS is gaining popularity in the design community as a method that ensures continued verification in the design flow and increasing the level of abstraction that designers can use to describe the design behavior. This method of code generation is free from errors and is faster than manual register transfer language (RTL) coding [6]. HLS tools like Vivado HLS [7] and MATLAB HDL [8] coder are commonly used in the design community to design and prototype algorithms that target different application areas, such as image processing, computer vision, and microprocessors. The code complexity is reduced by almost an order of magnitude, and reuse of behavioral IPs across projects is simplified by using modeling techniques in HLS, such as transaction-level modeling [9].

For modern system on chip designs, especially those containing embedded processors running firmware, the use of high-level programming languages in the automated HLS process enables designers and architects to explore area, power, and throughput trade-offs using different hardware–software boundaries. The industrial focus on HLS tools gained importance with the enhancements to RTL-based synthesis tools and flows. Proprietary tools were introduced by major chip design houses, such as Motorola [10], IBM [11], Philips [12], and Siemens [13]. Major electronic design automation (EDA) companies have also commercialized their HLS tools in the past few years. In 1995, Synopsys introduced the behavioral compiler [14] that generates synthesizable RTL implementations from C code and connects with downstream synthesis tools. Mentor Graphics came out with Catapult HLS [15], and Cadence introduced Stratus HLS [16].

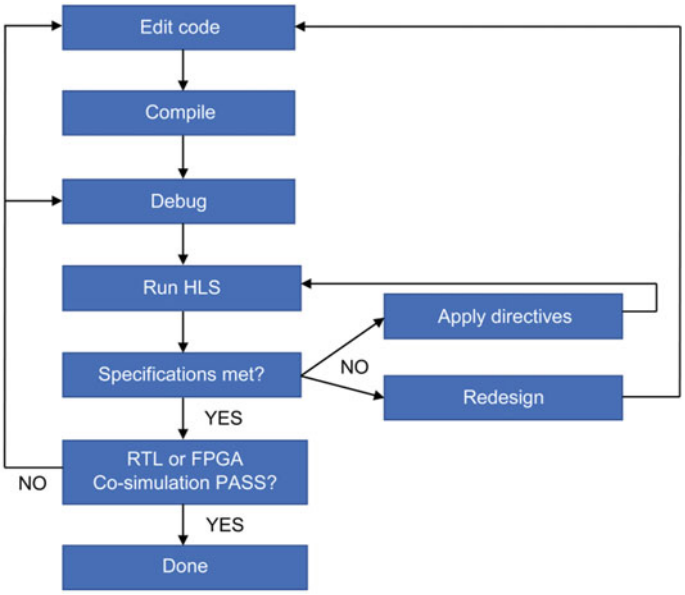

Fig. 1 High-level synthesis flow for very large scale integration designs

Figure 1 shows a typical HLS flow for very large scale integration (VLSI) designs. The HLS tool extracts all the parallelism that is accessible from the input description and schedules the operations. The next step includes allocating and sharing the necessary resources and optimization to minimize the area and improve performance. During these intermediate transform stages, different optimization directives can be applied to guide the HLS tool to meet the design specifications for decreasing area, increasing speed, and reducing power consumption. Within the HLS flow, tools typically perform the following functions: compile the specifications, allocate hardware resources (functional units, storage components, buses, etc.), schedule the operations to clock cycles, bind the operations to functional units, bind variables to storage elements, and bind transfers to buses.

Although the overall design cycle time during algorithm development may increase, the subsequent design implementation cycles are quicker, so the time to market is reduced. As seen in Fig. 1, not satisfying the desired specifications may trigger multiple iterations for HLS directives in the design flow.

3 Architecture of MIPS Processor

The primary goal in VLSI design has always been to reduce the power consumption of devices (specially mobile), such as laptops, mobile phones, and tablets, so that they would support real-time applications in video, image processing, telecom,

networking, etc. Different types of integrated circuits provide different complex signal processing units to fulfill the various demands of complex use cases such as mathematical computations. When it comes to real-time operation of these integrated circuit designs, speed and power dissipation are the major bottlenecks. Thus, the major aim here is to obtain computational speed and decrease power consumption.

To satisfy this requirement, the MIPS processor was proposed by MIPS Technologies in the 1980s. To date, six versions of the MIPS have been released (denoted I–VI), with the current version (VI) having been released in 2017. Earlier versions had only 32-bit support, but the later versions support 64 bits. The MIPS architecture is also known as load-store architecture because, except for memory access, all instructions operate on registers. The salient feature of a MIPS core is its use of the RISC architecture with a non-interlocked five-stage pipelining technique to reduce delay [17].

Pipelining has proven to be more efficient than traditional sequential architecture because of that fact that CPU becomes idle during instruction cycles that include other services such as read and write to memory and storage or input–output devices. This is clearly evident from Tables 1 and 2, which show the fetch, decode, and execute cycle with and without the pipelining for multiple instructions, and the associated throughput.

All MIPS instructions are 32 bit long. The instruction set is a compiler-based encoding of the machine instructions (i.e., code generation efficiency is used to choose alternative instructions). Multiple simple instruction sections are packed together into an instruction word. To do several operations simultaneously in pipelining, the simultaneous implementation of devices such as memory, integer units, and other units is essential. Pipelining involves five stages: fetch, decode, execute, memory, and write back.

- Fetch: In this stage, we fetched the instruction from the memory based on the address provided in the program counter (PC). Incrementing by four to the

Table 1 Instruction execution without pipeline; the throughput is two instructions per clock cycle

	Cycle 1	Cycle 2	Cycle 3	Cycle 4	Cycle 5	Cycle 6
Instruction 1	Fetch	Decode	Execute			
Instruction 2				Fetch	Decode	Execute

Table 2 Instructions execution with pipeline; the throughput is four instructions every six clock cycles

	Cycle 1	Cycle 2	Cycle 3	Cycle 4	Cycle 5	Cycle 6
Instruction 1	Fetch	Decode	Execute			
Instruction 2		Fetch	Decode	Execute		
Instruction 3			Fetch	Decode	Execute	
Instruction 4				Fetch	Decode	Execute

previous instruction address may update the PC. Alternately, it can be updated by a branch address provided by conditional or unconditional branch instructions. The instruction is fetched from the memory and relayed on to the next stage:

$$\text{PC} \leq (\text{PC} + 4),$$
$$\text{PC} \leq \text{Branch address}.$$

- Decode: In instruction decode, the opcode is decoded by the decoder unit. The register bank is also present in this stage to find the effective address. When in indirect-addressing mode, two clock cycles are required. For different addressing modes, operands are identified through the register bank and handed to the next stage for computation.
- Execute: All logical and arithmetic operations are performed in this stage. The operation performed on the data are dependent on the control signals generated in the decode stage for each instruction [2]. The integer unit consists of the arithmetic logic unit (ALU), shifter, and multiplier devices. In addition, the effective addresses used for load and store operations are computed.
- Memory: All memory related instructions are executed in this stage. Depending on the control signals, instructions such as load and store are performed to read and write the data.
- Write back: The registers are updated in this stage. The corresponding data are updated in the register array located in decode stage. The data may be coming from a memory location or another register.

MIPS cores have three types of instructions: I-type, J-type, and R-type (see Table 3). The six most significant bits for all types specify the opcode to select the type of instruction. R instructions are used when all the values used by the corresponding instruction are used from registers. I instructions are used when the instruction operates on a register and an intermediate value. Immediate values may be up to 16 bits long; larger number values cannot be manipulated by immediate instructions. J instructions are used for jumps; it has the most bits available for an immediate value to be stored because addresses are typically large numbers.

Table 3 Instruction types for MIPS architecture

R-type instructions					
Op (6 bits)	Rs (5 bits)	Rt (5 bits)	Rd (5 bits)	Shamt (5 bits)	funct (6 bits)
I-type instructions					
Op (6 bits)	Rs (5 bits)	Rt (5 bits)	Address/immediate (16 bits)		
J-type instructions					
Op (6 bits)	Target address (26 bits)				

4 Design Methodology

The end-to-end processor model for the MIPS core was created by using Simulink with MATLAB function blocks. Figures 2, 3, and 4 show the top-level CPU (Controller + Memory), MIPS datapath, and controller, respectively. The design is optimized by applying directives such as loop unroll and pipelining (three stages). An instruction parser operates within the datapath and consisted of the opcode, source register, destination register, immediate operand, and jump address. The parser is directly linked to a sign extend block and a jump calculator block. A 32-bit register file is also available which consists of one write port and two read ports. The ALU RESULT consists of three inputs: ALU control, Scr A, and Scr B, and this block performs four major operations on the input: addition, subtraction, AND, and OR

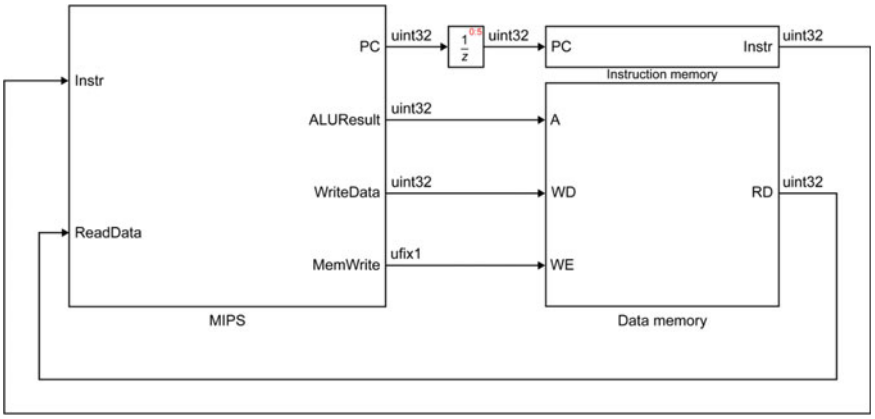

Fig. 2 Top-level implementation of processor system with memory

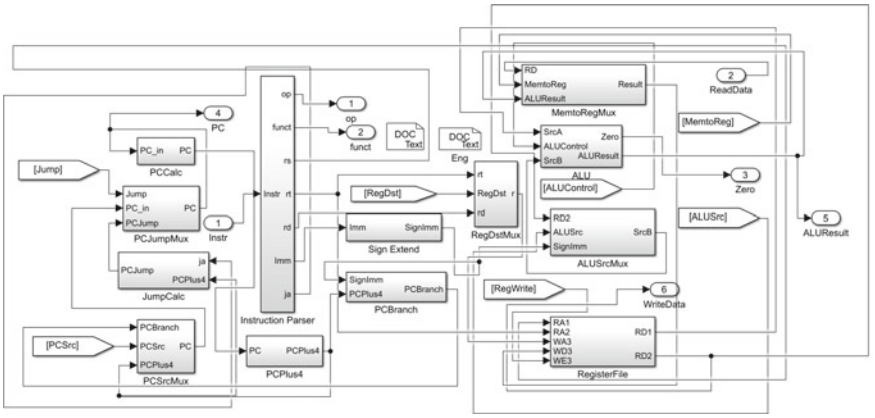

Fig. 3 MIPS data path model

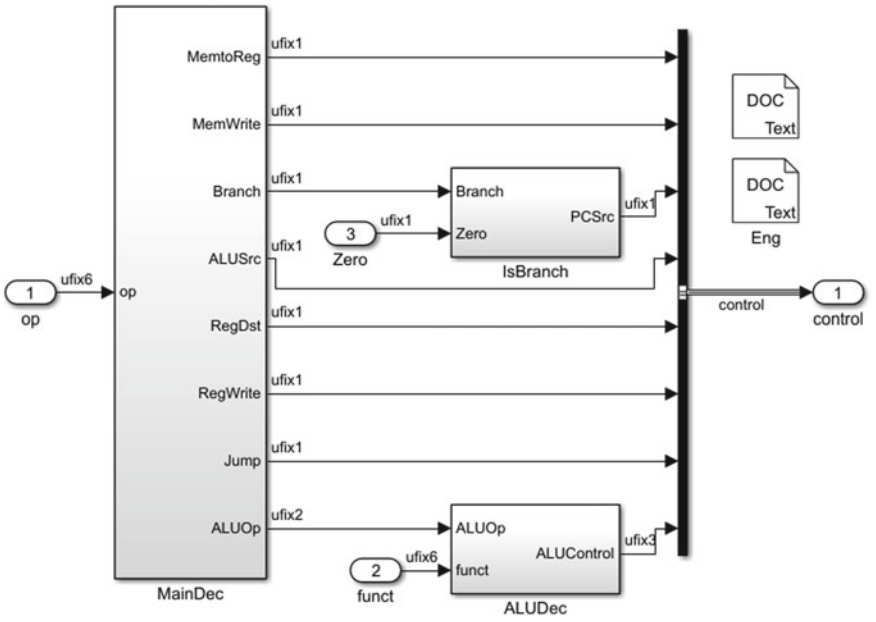

Fig. 4 MIPS controller

between the Scr operands A and B. The register file provides Scr A, and the Scr B output data are obtained from the sign extended immediate value. The three-bit ALU control specifies the operation to perform on operands while the ALU generates a 32-bit result and a zero flag (to indicate if ALU Result = zero). The ALU Scr multiplexer is used to handle the R-type instructions, which write the ALU Result to the register file. Therefore, we add this multiplexer to select between Read Data and ALU Result and call the output as "Result." This multiplexer was controlled by the signal "Mem to Reg," which is zero for R-type instructions to choose Result from the ALU Result, and unity for lw to choose Read Data. After the base implementation is created, we use the HLS tool MATLAB HDL coder to convert the MIPS core to synthesizable Verilog code and subsequently run it through FPGA synthesis using Xilinx Vivado.

As a second step, we apply the following HLS directives to optimize the results of the MATLAB HDL coder:

(A) Pipeline. The HLS directive allows the concurrent execution of operations by reducing the initiation interval for a loop or function, so a trade-off exists between area and speed. To optimize this CPU design implementation, we apply a pipeline directive with an initiation interval of two for all loops in the design.

(B) Loop unroll allows the loop iterations to run in parallel by creating multiple copies of the same loop body in the generated RTL. This directive helps to increase the throughput by making the loops either partially or fully unrolled.

Table 4 Resource use for FPGA implementation; maximum synthesis frequency = 420.028 MHz, power = 0.0233 W; LUT: lookup table, IOBs: input–output blocks, BUFG: global clock buffer

Resource	Resources used	Total resources
Slice registers	43	408,000
Slice LUTs	178	204,000
Fully used FF pairs	41	178
Number of bonded IOBs	47	600
Number of BUFG	1	32

For the proposed application of the MIPS controller and datapath, we use the partial unroll directive to improve design performance, which incurs a minor trade-off on resource usage. An unroll factor of two is used in the implementation.

Section 5 presents detailed implementation results for the base implementation and the implementation after application of the HLS directives.

5 Results

5.1 Simulation Results

After generating the RTL code, we performed an RTL simulation for the design using a non-synthesizable Verilog test bench in xSim software. The simulation results were identical to the simulation results obtained using a high-level simulation in Simulink.

5.2 Results of FPGA Implementation

We implemented the generated RTL from the HLS model on a Xilinx Virtex 7 FPGA board (7vx330tffg1157-3). Table 4 summarizes the implementation results for the target FPGA device.

5.3 Comparison of Results

As can be seen from Tables 4 and 5, although the proposed implementation operates at almost the same operating frequency as that of Indira et al. [1], its resource usage is 40–50% less. In addition, the proposed implementation is about fourfold faster than that proposed by Rakesh et al. [5], with almost the same resource use. These

Table 5 Comparison of FPGA implementation results

Metric	Proposed implementation	Indira et al. [1]	Rakesh et al. [5]
Slice registers	43	81	56
Slice LUTs	178	321	203
Fully used flip flops	41	81	43
Bonded IOBs	47	71	51
BUFG	1	2	1
Power (W)	0.021	0.0233	1.318
Maximum frequency (MHz)	404.1	420.028	100

improvements are attributed to the use of HLS directives in the proposed implementation, which produces better results in terms of both area and speed of operation (i.e., synthesis frequency).

6 Conclusion

Over the past few years, MIPS processor architectures have evolved as an important choice for multiple computing applications, such as communication and information processing. Being built from a RISC architecture, MIPS are friendly for pipelining instructions and thus provide faster throughput for targeted applications. Additionally, to reduce time to market for VLSI designs, FPGAs have also become popular as platforms for pre-silicon software development and accelerated verification. Therefore, the optimal FPGA implementation of MIPS cores is vital for obtaining optimized designs.

This paper proposes a resource optimal, high-throughput implementation of a MIPS core on a Virtex 7 FPGA. The proposed design was created using Simulink and was implemented using the MATLAB HDL coder and Xilinx Vivado. The design targeted Virtex 7 so that the results could be compared directly with those of other studies. We optimized the targeted implementation for performance and resource usage using appropriate HLS directives for pipelining and loop unrolling. After applying the directives, the final implementation results proved superior in terms of throughput and target area on the FPGA. The results of FPGA synthesis clearly indicate that the proposed implementation is superior to previous implementations, despite having exactly the same design specifications. The implementation results can be further improved using one or more HLS directives, which will be explored in future work.

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A Low Power 3-Stage Ring Voltage Controlled Oscillator with Wide Tuning Range and Active Load

Nitin Kumar, Manoj Kumar, Vikram Singh, Dhruv Aditya Mittal, and Priyamvada

1 Introduction

In the present scenario, high-speed and low power consumption are always desired for electronic appliances. Power-hungry devices, due to their large size demand more attention from the designer. The progressive downscaling of CMOS technology has contributed to reducing size, costs and commenced to a new era of low power portable electronic devices (PEDs). Battery operated low power PEDs are widely used in the communication system [1]. Modern communication systems comprise filters, low noise amplifiers (LNA), phase-locked loops (PLL) and mixtures. The performance of a PLL system is derived by its output key circuit of voltage-controlled oscillator (VCO) and this PLL is widely used in synchronization, clock generation, data retrieval circuits and in wireless transceiver system [2–4].

The architectural block diagram of a closed-loop feedback controlled PLL system is shown in Fig. 1, which also consists of a phase frequency detector (PFD), a charge pump (CP), a loop filter and a frequency divider in feedback path. In a PLL system, most of the power is consumed by VCO. The significant design challenge of RVCO is to obtain a tunable wide-ranging frequency spectrum, low power dissipation and minimum layout area. The energy consumed by a PLL system can also be reduced by reducing the power dissipation of VCO circuit.

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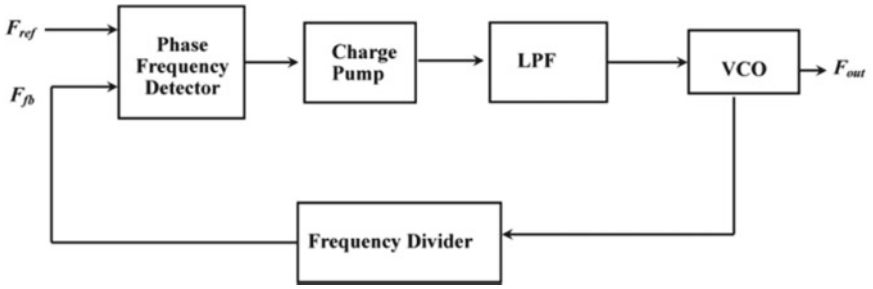

Fig. 1 Architecture of a closed-loop PLL system

1.1 Topologies and Background of RVCO

Two broadly classified topologies for a VCO are either by using an inductor-capacitor (LC) tank or by using a ring topology. An LC VCO provides better performance in terms of enhanced phase noise which is an advantage for the high frequency of operations. However, they suffer from a large layout area and limited tuning range [5, 6]. On the contrary, a ring VCO offers wide tuning range, high frequency operations, and low power consumption with an easy integration which provides small chip-area. The ring VCO provides low resolution and slightly higher phase noise performance [7, 8], but they are preferred to save chip-area. In a ring-VCO, the architecture of the delay cell can either be a single or a differential ended. A differential ended RVCO can have both even and odd number of delay stages, depending upon the type differential topology and design specifications. Differential ended RVCO provides excellent immunity to diminish bulk and power supply injected phase noise [9, 10]. The number of delay stages must be odd in a single-ended RVCO. Unit voltage gain with a net phase shift of 360° are the two main requirements of a ring VCO circuit in order to provide sustained oscillations at the output [11]. In a ring oscillator, the output oscillation frequency can be derived as [12]

$$f_{\text{out}} = \frac{1}{2Nt_{\text{d}}} \tag{1}$$

where, f_{out} is the output oscillation frequency, t_{d} is the average propagation-delay of a delay cell and N is the number of delay cells. Single-ended RVCO provides a compact layout area, low power dissipation, wide tuning range but it has acceptable phase noise [13]. In a RVCO phase noise is affected by temperature, power supply, control voltage, frequency, power dissipation, and the number of delay cells. The phase noise of single-ended RVCO can be expressed as [14]

$$L_{\min}(\Delta f) = \frac{8}{3\eta} \cdot \frac{kT}{P_{\text{diss}}} \frac{V_{\text{dd}}}{V_{\text{cr}}} \cdot \frac{f_{\text{out}}^2}{\Delta f^2} \tag{2}$$

where Δf is the offset frequency from the center output frequency f_{out}, V_{cr} is the characteristic voltage of the device, T is absolute temperature, k is Boltzmann constant and η is the proportionality constant. As depicted from (2), phase noise performance depends on the number of cells. Phase noise performance is degraded as the supply voltage increases for the specified power dissipation and frequency. Single-ended RVCO is selected to achieve low power dissipation, small area and acceptable phase noise performance. Depending upon the different application, various RVCO is mentioned in the literature such as current starved delay cell [15], delay stage with active load [16], delay stage with active inductor [17], shunt-shunt feedback delay stage [18], delay stage with inductive composite load [19], delay stage with source capacitive current amplifier [20] but all these RVCO designs either suffer from high power dissipation and delivers small tuning range with high phase noise performance. In this paper, three-stage single-ended RVCO based on active load is proposed to obtain, wide tuning range with low power dissipation, low phase noise and high FoM.

This paper is organized as follows: The design description and working of the proposed RVCO structure is presented in Sect. 2. Section 3 reports the results of output frequencies, phase noise and power consumptions for VCO-I, VCO-II, VCO-III and its performance comparison with earlier reported work. Finally, the conclusion of the paper is given in Sect. 4.

2 Design Description of Proposed RVCO

In a RVCO, output frequency begins when the V_{dd} is higher than a specified threshold level. At a constant V_{dd} supply, the output oscillation frequency (f_{out}) depends on delay stages associated with the closed-loop and the time delay of each delay stage. The delay time for fixed delay stages can be changed by modulating the control voltage (V_{cnt}) of RVCO.

Schematic of the single-ended proposed delay cells with NMOS AL (VCO-I), PMOS AL (VCO-II), and CMOS AL (VCO-III) is manifested in Fig. 2. In this design, the NMOS transistor MN_2 form input for the loop, whereas PMOS transistor MP_1 is utilized to pre-charge the output node whose gate-voltage is controlled by transistor MN_1 using controlled voltage (V_{cnt}) input. Two NMOS transistors MN_3, MN_4 and one PMOS transistors MP_2, are employed as a resistive loads. These resistive loads i.e., MN_3 and MN_4 are in parallel with load capacitance and discharge the output node. The ac equivalent model of CMOS active load based proposed delay stage is displayed in Fig. 3.

The output frequency of a VCO can be modulated with the shift in the control voltage (V_{cnt}), used at the gate terminals of MN_1, MN_3, MN_4 and MP_2 transistors. In NMOS based active load VCO-I, when the V_{cnt} is raised, MN_1 transistor is 'ON' gives the low resistance. The charging time through MP_1 of the output node is increased. Simultaneously MN_3 and MN_4 transistors are also 'ON' which provide low resistance and discharge the output node. The net charging time constant of

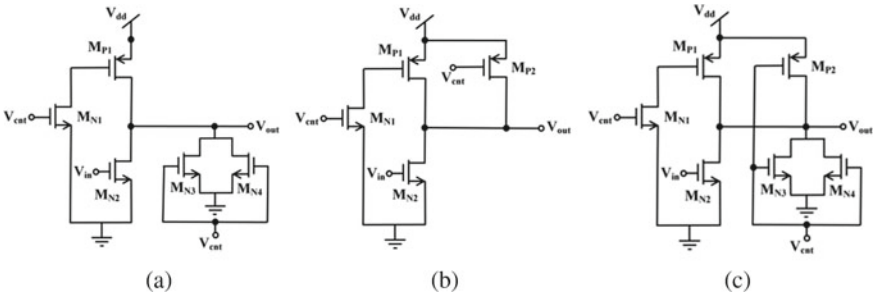

Fig. 2 VCO delay cell with: **a** NMOS AL only (VCO-I), **b** PMOS AL only (VCO-II) and **c** CMOS AL (VCO-III)

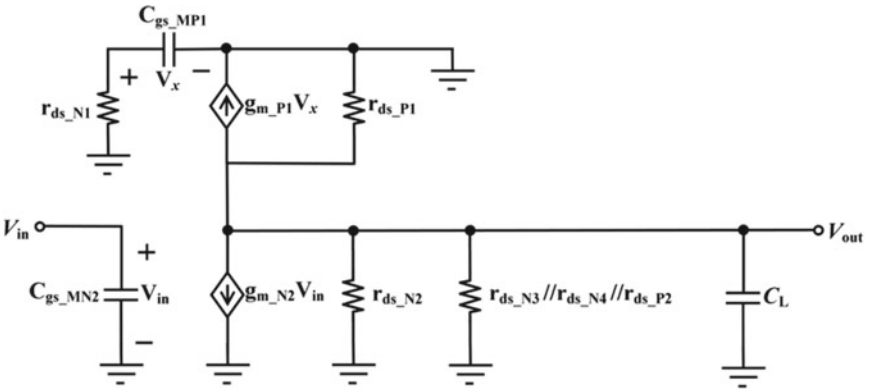

Fig. 3 AC equivalent small-signal model of CMOS active load VCO delay cell

the circuit is increased. As a result, the output frequency of the proposed VCO is decreased. In PMOS based active load VCO-II, V_{cnt} is initially low then the output node charges faster through MP_1 and MP_2 transistor. The time constant of the circuit is reduced, resulting high output frequency. As V_{cnt} is increasing, the output node charge only through MP_1 transistor, the time constant of the delay stage increases, output frequency decreases consequently. The proposed VCO-II provides the high frequency range as compared to VCO-I because of smaller time delay constant. In CMOS based active load VCO-III, when the V_{cnt} is increased, the output node charges through MP_1 and MP_2 transistor. Simultaneously MN_3 and MN_4 transistors discharge the output node. The net charging time constant of the circuit is expanded. As a result, the output frequency of the proposed VCO is reduced. Schematic of the proposed three-stage RVCO is shown in Fig. 4, and the respective dimensions for each MOS device used are presented in Table 1.

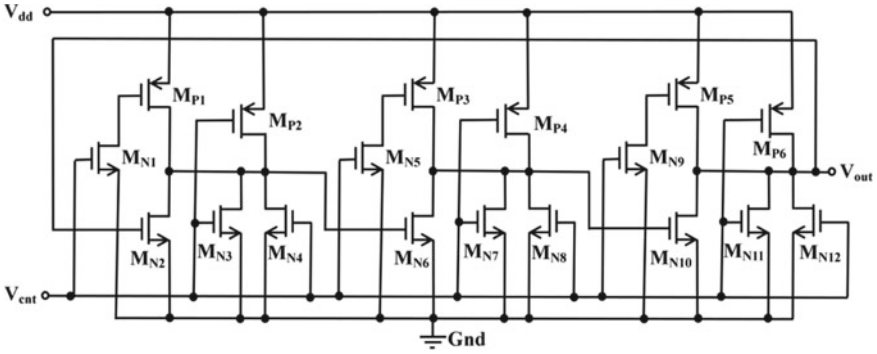

Fig. 4 Complete circuit of CMOS active load VCO

Table 1 Width of proposed delay stages for $L = 180$ nm

Transistors	M_{P1}	M_{P2}	M_{N1}	M_{N2}	M_{N3}	M_{N4}
Channel width (μm)	2.0	1.0	2.0	2.0	2.0	2.0

3 Results and Discussion

The proposed three-stage RVCOs based on the NMOS AL (VCO-I), PMOS AL (VCO-II), and CMOS AL (VCO-III) are simulated in 180 nm CMOS process with V_{dd} of 1.8 V. Tables 2, 3 and 4 demonstrate the simulation results of the proposed VCO-I, VCO-II and VCO-III. The output frequency range of VCO-I, VCO-II and VCO-III circuit varies from 6.540–3.764 GHz, 10.113–8.215 GHz and 7.115–5.179 GHz with a tuning range of 53.88%, 20.73% and 31.49%, respectively. For these achieved frequency ranges, the power dissipation is varying from 2.028 to 2.278 mW, 2.747–2.448 mW and 2.747–2.542 mW, respectively, with the variation of V_{cnt} from 0.1 V to 0.8 V and 0.2 V to 0.7 V. Figure 5a shows the change in power dissipation with V_{cnt}. As the control voltage of VCO-I, VCO-II and VCO-III

Table 2 Results of proposed RVCO with NMOS load only (VCO-I), at different values of V_{cnt}

V_{cnt} (V)	f_{out} (GHz)	P_{diss} (mW)	*PN* (dBc/Hz)
0.1	6.540	2.028	− 91.54
0.2	6.134	2.030	− 84.40
0.3	6.088	2.031	− 93.20
0.4	6.084	2.107	− 99.36
0.5	5.900	2.041	− 100.90
0.6	5.647	2.082	− 101.18
0.7	4.990	2.165	− 100.75
0.8	3.764	2.278	− 102.789

Table 3 Results of proposed RVCO with PMOS load only (VCO-II), at different values of V_{cnt}

V_{cnt} (V)	f_{out} (GHz)	P_{diss} (mW)	*PN* (dBc/Hz)
0.2	10.115	2.747	− 81.702
0.3	9.567	2.576	− 91.144
0.4	9.274	2.650	− 95.705
0.5	8.983	2.441	− 96.017
0.6	8.551	2.428	− 95.545
0.7	8.215	2.448	− 94.903

Table 4 Results of proposed RVCO with CMOS load (VCO-III) at different values of V_{cnt}

V_{cnt} (V)	f_{out} (GHz)	P_{diss} (mW)	PN (dBc/Hz)
0.2	7.115	2.747	− 85.453
0.3	6.735	2.704	− 94.889
0.4	6.515	2.651	− 99.994
0.5	6.258	2.428	− 100.732
0.6	5.813	2.448	− 100.519
0.7	5.179	2.542	− 99.552

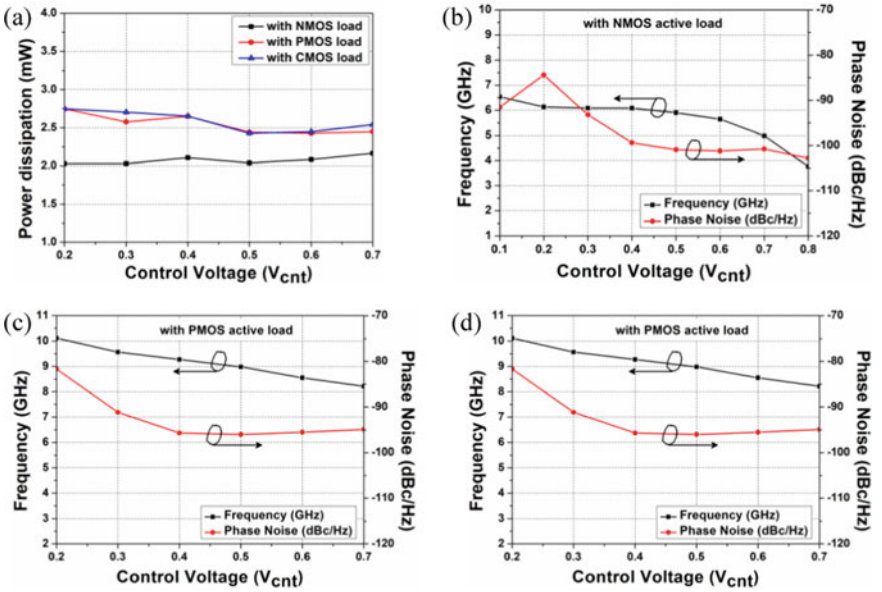

Fig. 5 **a** Variation in power dissipation with V_{cnt}; **b** variation in frequency and phase-noise with V_{cnt} for (VCO-I), **c** for (VCO-II) and **d** for (VCO-III)

is increased, the power dissipation of VCO-I is increased, whereas that of VCO-II and VCO-III are decreased.

Figure 5b–d shows the variation in the frequency and phase noise of VCO-I, VCO-II and VCO-III increases with V_{cnt}. The proposed VCO-I, VCO-II and VCO-III designs achieve − 99.36, − 95.70, and − 99.99 dBc/Hz phase noise at 1 MHz offset from 6.084, 9.274 and 6.515 GHz center frequency, respectively.

In contrast, Fig. 6 exhibits the simulated output voltage waveform of RVCO for VCO-I, and Fig. 7 presents the phase noise performance of VCO-I at V_{cnt} equal to 0.4 V and 0.5 V, respectively. Table 5 shows the effect of temperature on output

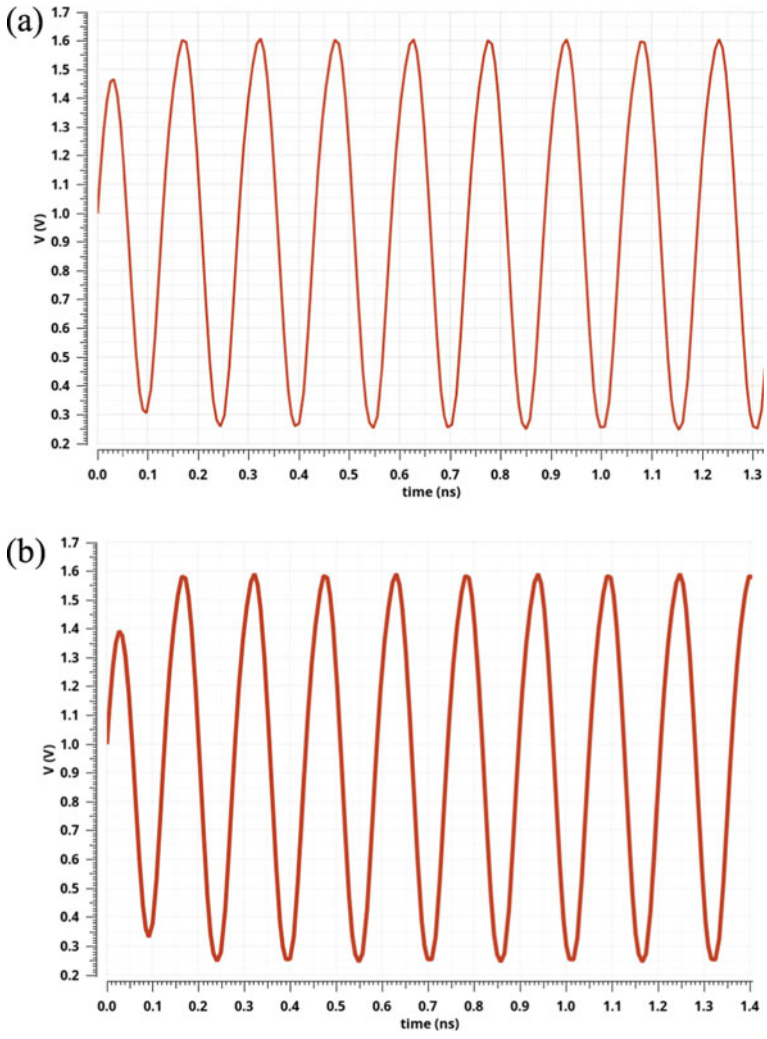

Fig. 6 Output waveform of VCO-I **a** at V_{cnt} of 400 mV **b** at V_{cnt} of 500 mV

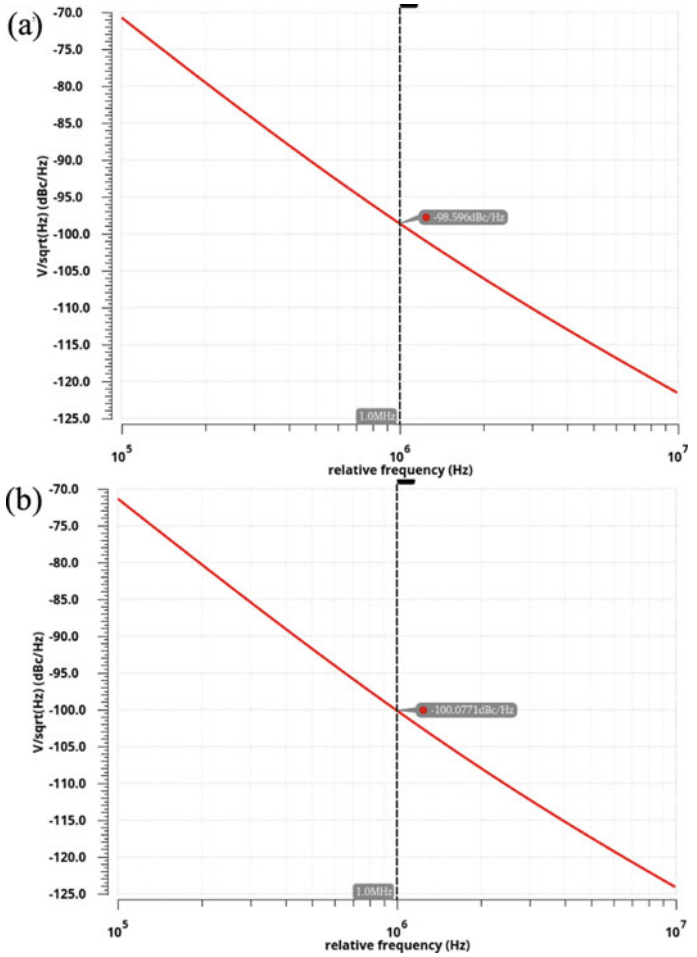

Fig. 7 Phase noise of proposed VCO-I **a** at V_{cnt} of 400 mV **b** at V_{cnt} of 500 mV

Table 5 Temperature effect on frequency response of VCO-I, VCO-II, and VCO-III

T (°C)	f_{out} (GHz) of VCO-I		f_{out} (GHz) of VCO-II		f_{out} (GHz) of VCO-II	
	$V_{cnt} = 0.4$ V	$V_{cnt} = 0.5$ V	$V_{cnt} = 0.4$ V	$V_{cnt} = 0.5$ V	$V_{cnt} = 0.4$ V	$V_{cnt} = 0.5$ V
− 50	6.533	6.508	9.856	9.608	6.892	6.709
− 25	6.386	6.339	9.661	9.396	6.758	6.557
0.0	6.240	6.178	9.482	9.195	6.635	6.410
25	6.105	6.008	9.288	8.991	6.518	6.268
50	5.971	5.846	9.121	8.792	6.407	6.129

frequency of RVCOs. As temperature increases, the output frequency of proposed VCO-I, VCO-II and VCO-III decreases. The FoM is extensively used for estimating the VCO performance based on the single-tuning frequency is expressed as [21]

$$\mathrm{FoM} = 10\log\left[\left(\frac{f_o}{\Delta f}\right)^2 \frac{1}{P_{\mathrm{diss(mW)}} L(\Delta f)}\right] \tag{3}$$

The calculated FoM of VCO-I, VCO-II and VCO-III is − 171.7 dBc/Hz, − 160.8 dBc/Hz and − 171.9 dBc/Hz, respectively. Figure of merit described by Eq. (3) can be increased by reducing power dissipation, phase noise and increasing output oscillation frequency. The phase noise seems to control the FoM uniformly, whereas frequency has more impact on FoM. Consequently, an increase of frequency could be an increase in power dissipation and the net results are an improved FoM. The proposed RVCO designs occupy the layout area of 18.39 µm × 8.385 µm. Achieved results of proposed RVCO designs compared with existing work, as shown in Table 6 and it has been depicted that the power dissipated by the proposed VCO circuits is less as compared to the existing literature in [3, 5, 17–21]. The results of proposed VCO-I, VCO-II and VCO-III show improved performance in terms of power, frequency, phase noise and FoM (Fig. 8).

Table 6 Performance comparisons of existing VCOs

Ref.	Tech. (nm)	V_{dd} (V)	f_{out} (GHz)	TR (%)	P_{diss} (mW)	PN (dBc/Hz) at 1 MHz	FoM (dBc/Hz)
[3]	180	2.0	0.523–2.11	49.4	14.8	− 103.3[a]	–
[5]	180	1.8	4.9–5.9	18.5	8.1	− 86.7	− 149.7
[16]	180	1.8	6.687–6.395	7.26	1.84–2.20	− 76.20	− 149.4
	180	1.8	5.726–6.142	7.01	1.97–2.17	− 73.42	− 145.5
[17]	180	1.8	3.25–4.2	25.5	7	− 92.3	− 154.8
[18]	180	1.8	2.5–5.2	74	17	− 90.1	− 148.9
[19]	130	1.2	6.3–13.9	77	5.1	− 81.5	173.4
[20]	180	2.0	4.3–6.1	34.61	80	− 85	− 140
[21]	180	1.8	3.125	18	12.6	− 91	− 149.1
TW VCO-I	180	1.8	6.540–3.764	53.88	2.028–2.278	− 99.36	− 171.7
TW VCO-II			10.115–8.215	20.73	2.747–2.448	− 95.70	− 160.81
TW VCO-III			7.115–5.179	31.49	2.747–2.542	− 99.99	− 171.9

TW This work
[a] @600 kHz

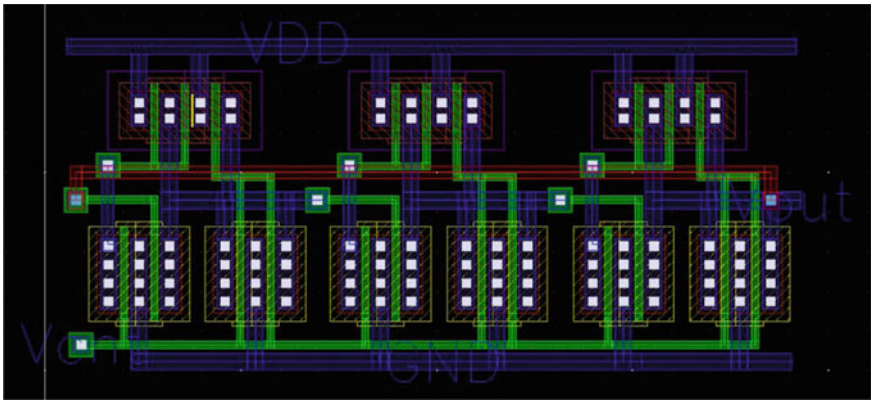

Fig. 8 Layout of the proposed RVCO design (VCO-III)

4 Conclusion

In this work, single-ended three-stage RVCOs based on the NMOS active-load (VCO-I), PMOS active-load (VCO-II), and CMOS active-load (VCO-III) have been presented. The proposed RVCOs are designed and simulated 180 nm TSMC CMOS process with V_{dd} of 1.8 V. The proposed VCO-I, VCO-II and VCO-III for the frequency range 6.540–3.764 GHz, 10.113–8.215 GHz and 7.115–5.179 GHz dissipates the power of 2.028–2.278 mW, 2.747–2.448 mW and 2.747–2.542 mW, respectively. The proposed VCO-I, VCO-II and VCO-III circuits exhibit − 99.36 dBc/Hz, − 95.70 dBc/Hz, and − 99.99 dBc/Hz phase noise at 1 MHz offset from 6.084, 9.274 and 6.515 GHz center frequency. The corresponding figure of merit (FoM) is − 171.7 dBc/Hz, − 160.8 dBc/Hz and − 171.9 dBc/Hz, respectively. The proposed design occupies the layout area of 18.39 μm × 8.385 μm. The performance of proposed RVCOs is compared with previous reported VCOs shows advantages of high frequency, high FoM, low phase noise and low power dissipation.

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865–867 MHz 180 nm Transmitter with Direct BPSK Modulation for Wireless Sensor Application

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1 Introduction

The advancement in technology, low voltage, low power, designs is getting significant concerns in Radio Frequency (RF) front-end systems, such as IEEE 802.11b standards [1–3]. In remote locations, the power supply is limited; for which low voltage and low power RF devices are in demand. RF front-end consists of an RF transceiver module which can transmit as well as receive signals. The transceiver sub-circuits include filter, mixer, power amplifier (PA), low-noise amplifier (LNA), and voltage control oscillator (VCO). The transmitter/receiver can be designed either using (i) direct conversion or (ii) indirect conversion architectures. The indirect conversion architectures are of three types: (i) Zero-IF, (ii) Complex-IF and (iii) High (real) IF architectures. The direct conversion transmitter architectures are of two types: (i) I/Q modulator-based transmitters and (ii) VCO-based transmitters. The VCO-based transmitter is also called as a direct modulation transmitter consisting of a VCO, RF Mixer, and PA. It has several advantages like low cost and relatively simpler architecture. It can operate within the bandwidth at the desired frequency and do not generates IF signals. This eliminates the requirement of IF filters and hence distortion is minimum [4, 5]. The disadvantage is that its output spectrum is corrupted due to leakage through the VCO signal to the PA. This problem can be rectified by improving isolation between VCO and PA.

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The RF mixer and PA are the most power-hungry blocks in a direct modulation transmitter. The performance of these blocks can affect the overall performance of the transmitter. Thus, proper design considerations are to be taken, while designing RF mixer and PA blocks. The Gilbert cell-based RF mixer has several advantages like good conversion gain and port-to-port isolation which can provide better isolation between VCO and PA. It has been used as a modulator, which performs modulation as well as for up-conversion of the input signal. Whereas in PA design, there is a trade-off between power-added efficiency (PAE) and linearity. Higher the PAE, less power is drawn from the battery.

Many direct modulation BPSK transmitters have been reported in the past [6–9]. The direct-digital RF-modulator (DDRM) architecture reported in [6] has a modulator constructed with two digital-to-RF converters (DRFCs). Jerng et al. [7] proposed a wideband delta-sigma digital-RF-modulator for high data rate transmitter consisting of oversampled and Q delta-sigma digital modulators and a quadrature digital-RF converter with integrated RF bandpass filter. Lee et al. [8] reported a direct modulation BPSK transmitter consisting of an RF mixer with a 65 GHz LC-VCO oscillator implemented using SiGeBiCMOS technology. Trotta et al. [9] designed a 79 GHz SiGeBipolar spread-spectrum transmitter for radar systems.

In this work, Gilbert cell-based BPSK modulated direct modulation transmitter has been designed for 865–867 MHz frequency band. DTMOS transistors have been used in the transconductance stage of the Gilbert cell due to its significant current driving capability, low-voltage operations, and low-leakage current. Tank circuit-based cross-coupled LC-VCO having a central frequency (f_c) of 866 MHz has been designed for RF mixing and modulation. The inductor-less class-AB PA has been designed for power amplification of the BPSK modulated signal before transmitting it through an antenna. Rest of the paper is as follows: in Sect. 2, the basic architecture of the transmitter has been discussed. Sub-modules and the overall result of the transmitter are presented in Sect. 3. Finally, Sect. 4 presents the conclusion of the work done.

2 Proposed Work

The simplified block diagram of the direct conversion transmitter is shown in Fig. 1. The off-chip non-return-to-zero (NRZ) data and VCO generated 866 MHz (0° and 180°) signals are applied to the input of the RF mixer. The RF mixer is designed using the Gilbert cell to achieve higher isolation between VCO and PA. The RF mixer together with combiner circuit forms BPSK modulator. The PA amplifies the BPSK modulated signal, which is transmitted through the antenna. The integrated block diagram has been shown in Fig. 5.

2.1 BPSK Modulator

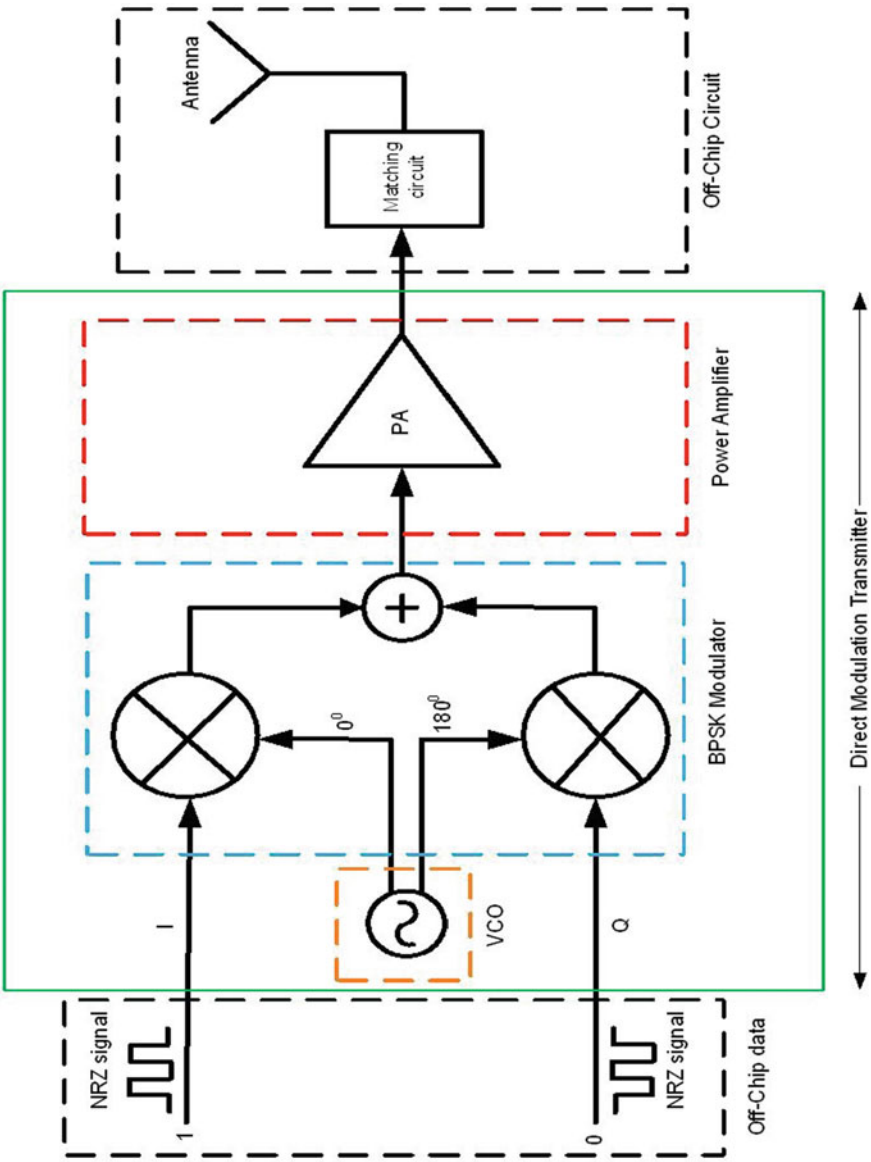

Fig. 1 General block diagram of the transmitter

Figure 2 shows the Gilbert cell-based BPSK modulator. It has three stages; (i) Transconductance stage, (ii) Switching stage, and (iii) Load stage. In the proposed modulator design, the current mirror transistors M_1 and M_2 are used for biasing. The NRZ data is applied to the input pins IN_1 and IN_2. Further, DTMOS transistors (M_3 and M_4) are used instead of conventional MOS transistors in the transconductance stage which improves gain of the RF mixer. The VCO signal is applied to the input pins LO+ and LO−. The mixing of the LO and the input signal (IN) takes place in the switching stage consisting of transistors M_5–M_8. The output is taken from the resistive loads R_4 and R_5 which are fed to the combiner circuit transistors M_9–M_{13} to provide output BPSK modulated signal. Table 1 shows the parameter values of the BPSK modulator.

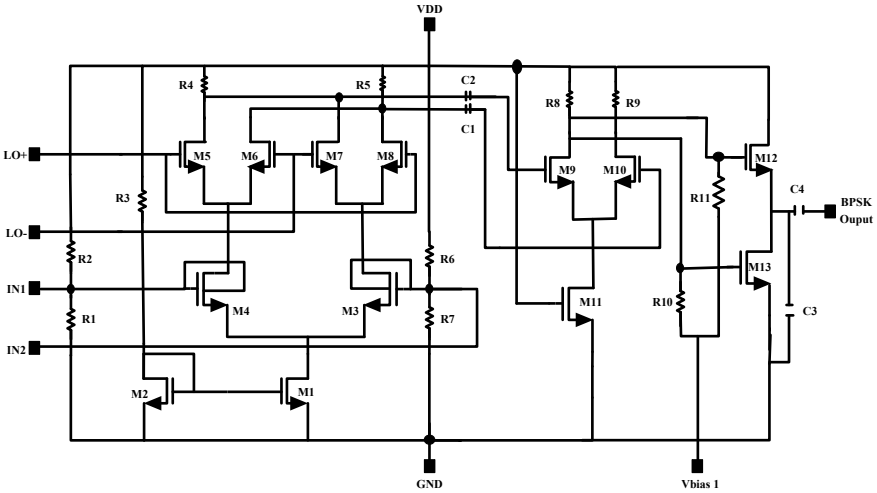

Fig. 2 Proposed BPSK modulator schematic

Table 1 Device parameters

S. No.	Parameters	Values
1	M_1, M_2	10 μm/0.18 μm
2	M_3, M_4	10 μm/0.18 μm
3	M_5, M_6, M_7, M_8	1 μm/0.18 μm
4	M_9, M_{10}	4 μm/0.18 μm
5	M_{11}	80 μm/0.18 μm
6	M_{12}, M_{13}	50 μm/0.18 μm
7	R_1, R_2, R_6, R_7, R_8, R_9, R_{10}, R_{11}	1 kΩ
8	R_3, R_4, R_5	300 Ω
9	C_1, C_2, C_3, C_4	0.1 nF

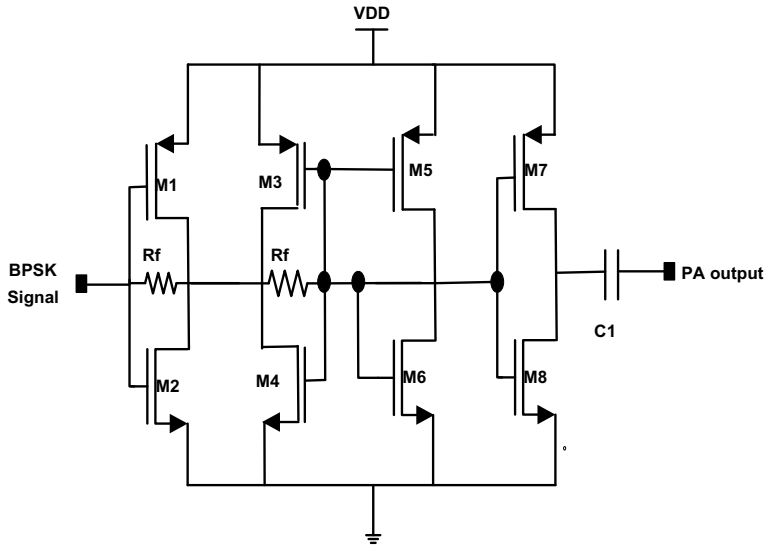

Fig. 3 Schematic of power amplifier [10]

Table 2 Device parameters

S. No.	Parameters	Values
1	M_1, M_2, M_3, M_4	100 μm/0.34 μm
2	M_5, M_6	50 μm/0.34 μm, 25 μm/0.34 μm
3	M_7, M_8	100 μm/0.34 μm
4	R_f	500 Ω
5	C_1	10 pF

2.2 Power Amplifier

Power amplifier schematic is shown in Fig. 3. It is consists of three stages; (i) Driver stage, (ii) Gain stage, and (iii) output stage. Driver stage consists of transistors M_1–M_4. The gain stage has transistor M_5 with a diode-connected load M_6. Class-AB push–pull amplifier consisting of transistors M_7 and M_8 has been used at the output stage. Proper sizing of the transistors M_7 and M_8 are needed to minimize the second-order effect (IIP3). R_f (resistive feedback resistance) is chosen to optimize the gains in the desired frequency band. Table 2 shows the device parameters.

2.3 Voltage Control Oscillator (VCO)

A low-phase noise VCO has been designed as shown in Fig. 4. The oscillation core

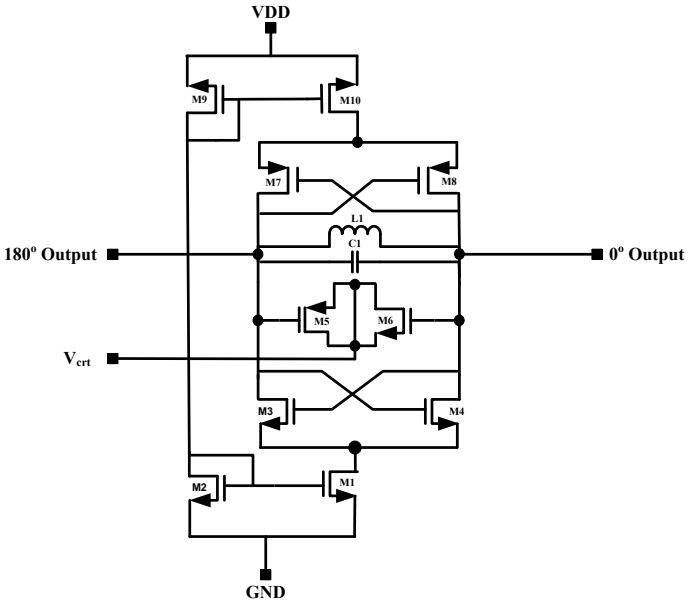

Fig. 4 Schematic of VCO

Table 3 Device parameters

S. No.	Parameters	Values
1	M_1, M_2, M_3, M_4	1 μm/0.18 μm
2	M_5, M_6, M_7, M_8, M_9, M_{10}	3 μm/0.18 μm
3	L_1	4 nH
4	C_1	9 pF

consists of inductor L1, and capacitor C1 determines the oscillation frequency. The cross-coupled topology consists of complimentary PMOS and NMOS transistors M_7, M_8 and M_3, M_4, respectively, which are used to generate negative feedback resistance for the lost compensation of the oscillation core [11, 12]. The tail current mirror consists of transistors M_1, M_2 and M_9, M_{10} are used to balance the output impedance of the VCO. Device parameters are shown in Table 3 (Fig. 5).

3 Results and Discussion

The BPSK transmitter for Sub-Gigahertz band (865–867 MHz) has been implemented in 0.18 μm UMC technology with a supply voltage of 1.8 V. The 866 MHz frequency of oscillation and it's magnified image are shown in Fig. 6a and b, respectively. The output BPSK modulated signal with input data is shown in Fig. 7. Figure 8

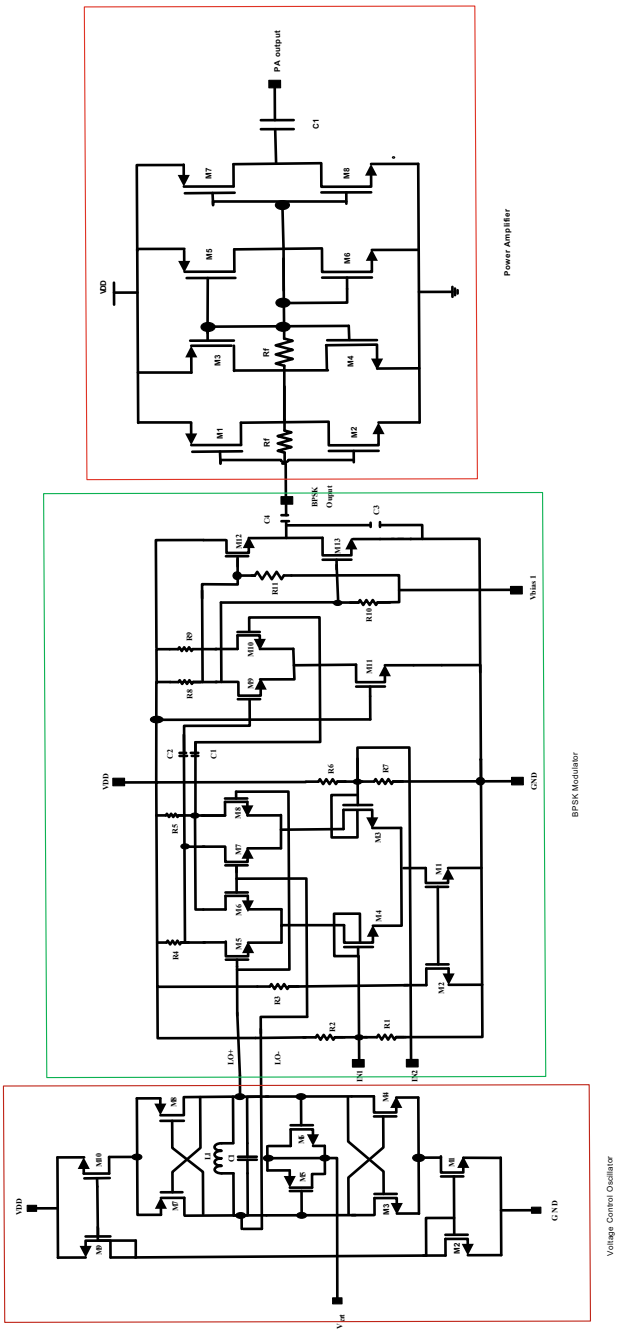

Fig. 5 Integrated diagram of a BPSK direct modulation transmitter

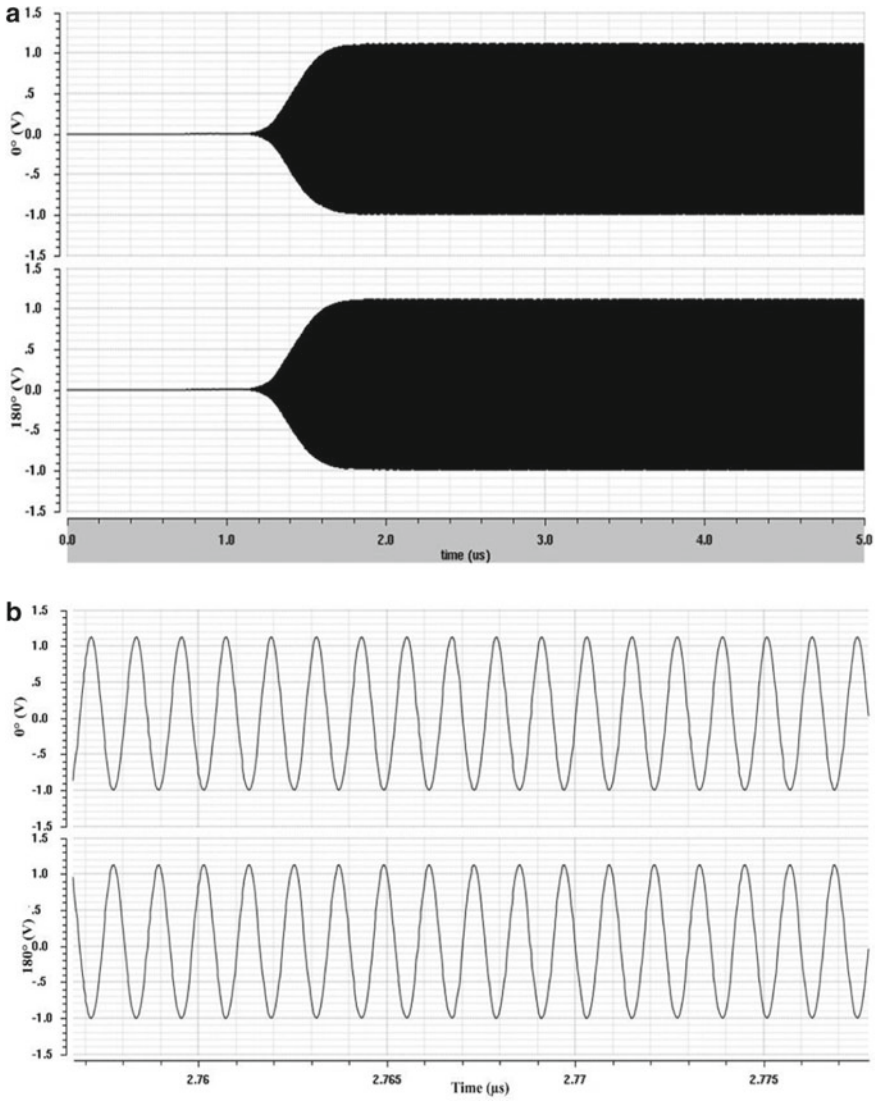

Fig. 6 **a** VCO output @ 866 MHz. **b** VCO magnified output @ 866 MHz

shows the phase noise of the VCO. The conversion gain of the Gilbert cell is 7.65 dB as shown in Fig. 9. PSS and PAC analysis calculate the linearity of the Gilbert cell to be 18.17 dBm as shown in Fig. 10. Power amplifier output power, 1-dB compression output and PAE, is showed in Figs. 11, 12, and 13, respectively. Figures 14 and 15 express LO-IF and LO-RF port-to-port isolation of the transmitter, respectively. Total power consumption of the integrated BPSK transmitter is 98.47 mW.

It is observed from Table 4 that though the circuit reported in [13] consumes lower

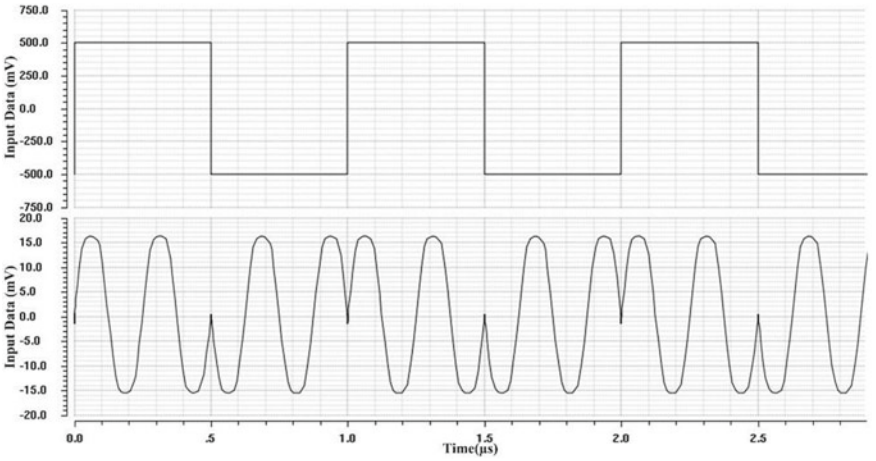

Fig. 7 BPSK modulated output with input data (input data rate 1 Mbps)

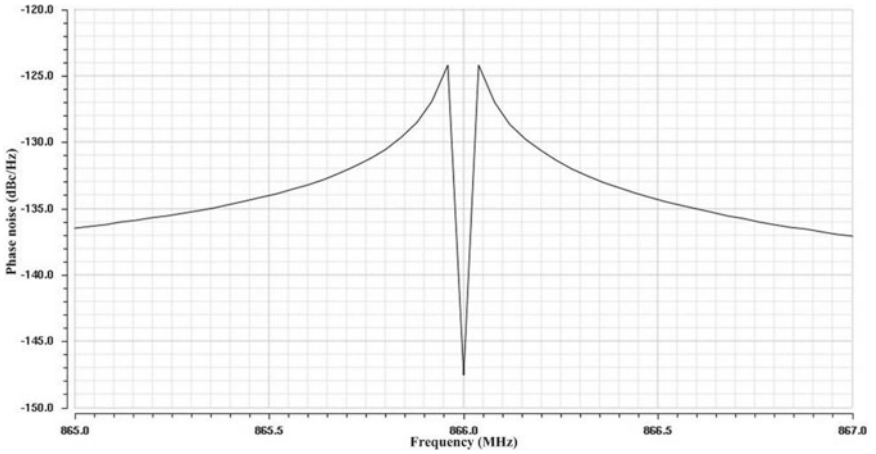

Fig. 8 Phase noise of VCO is − 148.23 dBc/Hz

power due to low-supply voltage, but the proposed circuit offers better linearity in comparison with it. The circuit reported in [14] consumes almost the same power; however, the proposed circuit offers better PAE (39.12%) and better phase noise of VCO (− 148.23 dBc/Hz) @ 866 MHz.

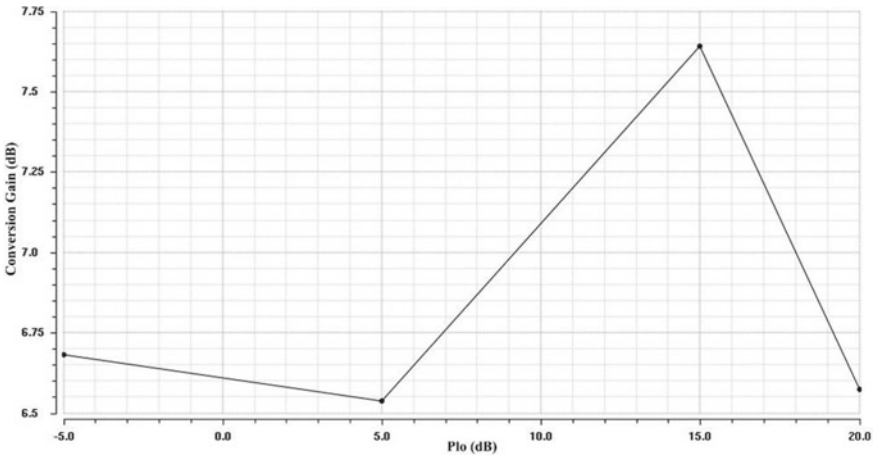

Fig. 9 Conversion gain of Gilbert cell is 7.65 dB

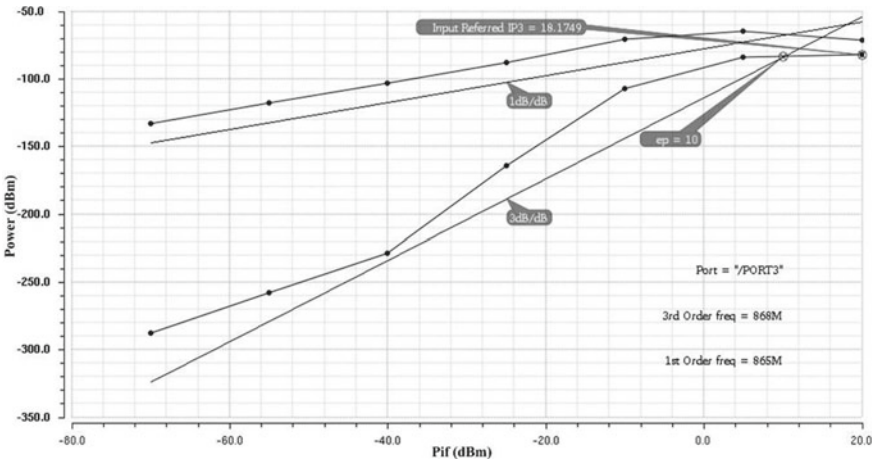

Fig. 10 Linearity of the Gilbert cell is 18.17 dBm

4 Conclusion

A 1.8 V direct BPSK modulation transmitter has been designed for 865–867 MHz frequency band. Gilbert cell does up-conversion and modulation. Thus, the complexity of the design reduces and also provides better port isolation between VCO and PA. The phase noise of the VCO is − 148.23 dBc/Hz, which is quite good. In the PA design, there is a trade-off between efficiency and linearity. Higher the efficiency less power is drawn from the battery. The PAE of the power amplifier is

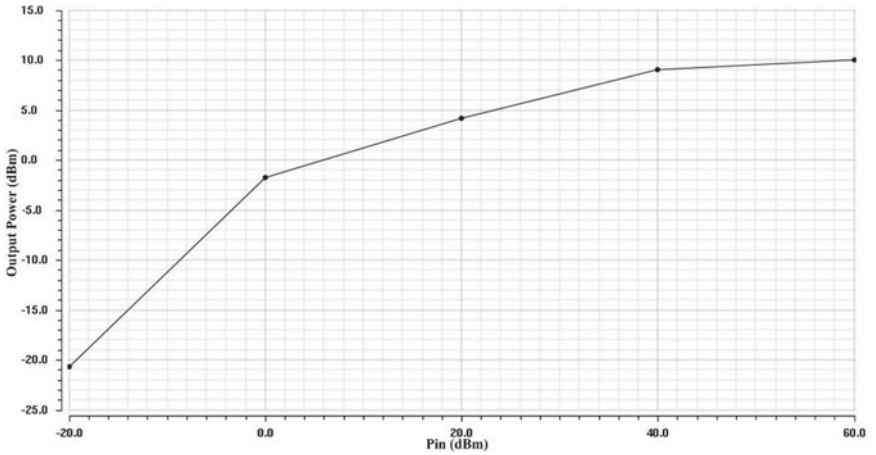

Fig. 11 Output power of PA is 9.9 dBm

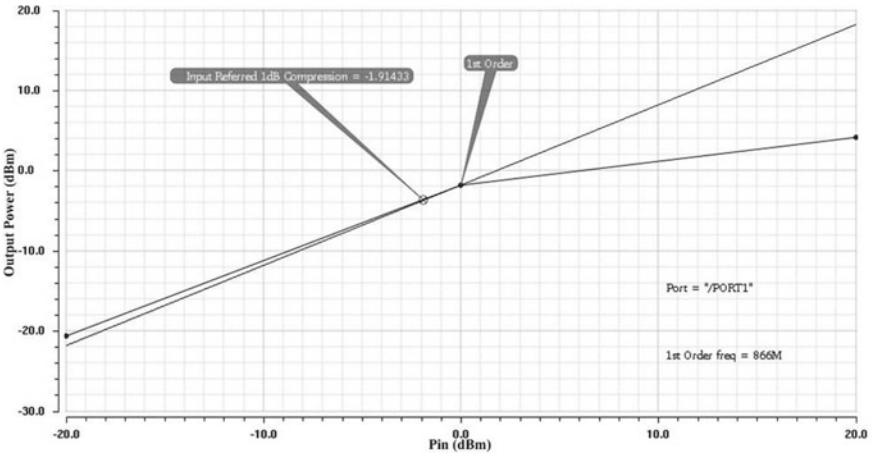

Fig. 12 1-dB compression of PA (− 1.91 dBm)

39.12%. The output power of the PA is 9.9 dBm. Thus, the overall design is suitable for battery-operated independent devices for unlicensed frequency band, i.e., 865–867 MHz.

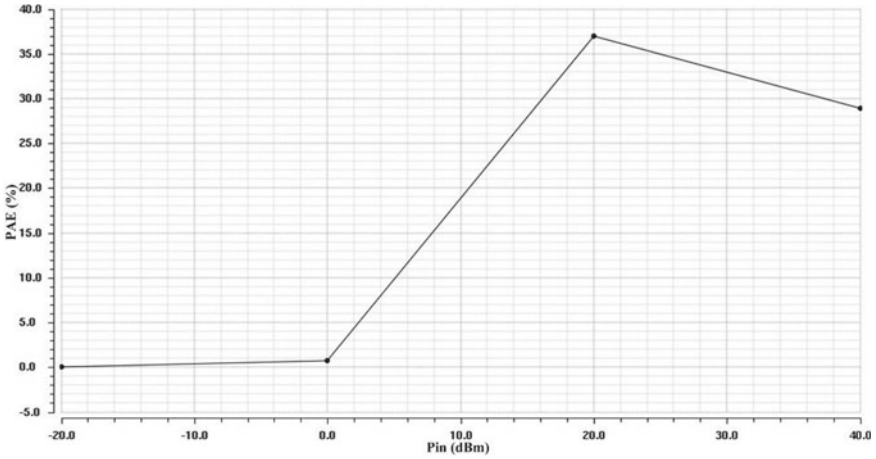

Fig. 13 PAE of PA is 39.12%

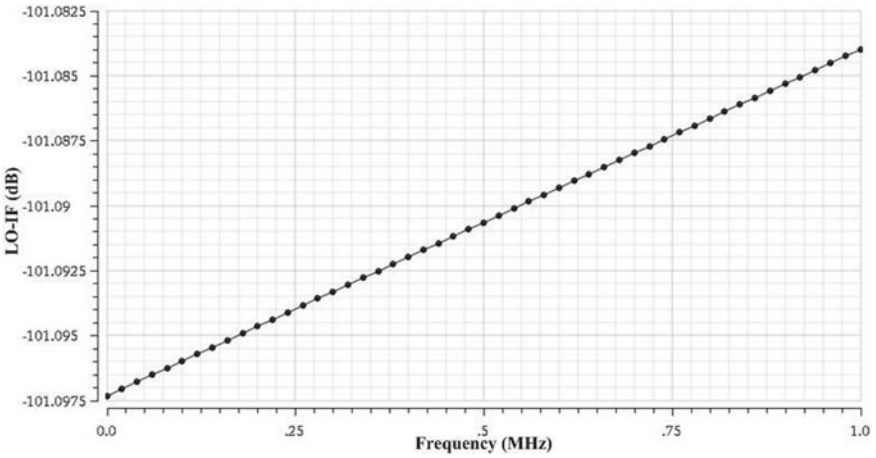

Fig. 14 LO-IF isolation of the transmitter

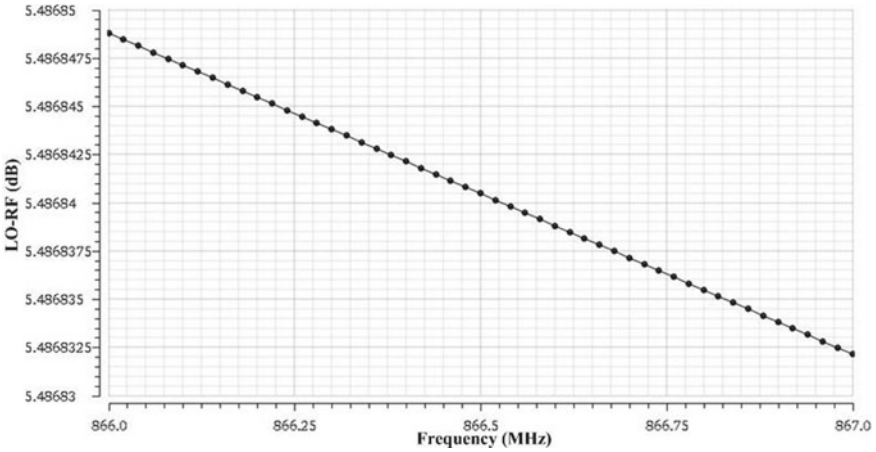

Fig. 15 LO-RF isolation of the transmitter

Table 4 Comparison table

S.No.	Parameters	[13]	[14]	This work
1	Technology (180 nm)	UMC	UMC	UMC
2	Supply voltage (V)	1.25	1.8	1.8
3	Frequency band (MHz)	900	755–933	865–867
4	Modulation type	BPSK	BPSK	BPSK
5	Data rate (Mbps)	N/A	N/A	1
4	Power consumption (mW)	50	95.8	98.47
5	Conversion gain (dB)	16	N/A	7.65
6	Linearity (dBm)	12	N/A	18.17
7	1-dB compression (dBm)	− 2	N/A	− 1.91
8	Output power of PA (dBm)	N/A	N/A	9.9
9	PAE of PA (%)	N/A	25.5%	39.12%
10	Phase noise of VCO (dBc/Hz) @ 866 MHz	N/A	− 120.7	− 148.23

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Improving the Charging System at Urban Places for Electric Vehicle

Amit Sharma and Abhishek Mishra

1 Introduction

Studies indicate the increase in greenhouse and other gases, which are bringing the climatic changes [1, 2]. Big cities are producing more air pollution due to number of industries and vehicles, which are causing hazardous environment and many diseases like chronic obstructive pulmonary disease (COPD), lung cancer, and acute lower respiratory infections in children. [2, 3]. Many agencies are working to reduce the pollution by using steps like (i) generation of power from renewable sources [4] (ii) inspiring the use of electrical vehicles [5–7]. Commercial agencies are working to make more efficient electrical vehicles or they have already launched in the market like Eve, Zytel, Little Electric Cars, or Tesla Motors. With the soring price of petrol and diesel, electric vehicles are going to play significant role in public transport.

Figure 1 shows the actual data of electric vehicles by different agencies such as IEA [8, 9], and Paris declaration [10] with the help of clean energy ministerial to decrease the rise in global temperature [11]. Keeping this in mind, the future electric vehicles will be furnished with intelligent charging system as residential charging system will be the right place to charge, as domestic charging stations will be limited. Most convenient method used is plug and charge (PC) method in which batteries start charging as soon as they are provided with supply current.

PC method suffers with some drawbacks as the electricity rates may vary during night and day; however, user does not look for this and start charging their vehicles whether the rates are expensive at that time, and follow the same routine every day. During night, this charging practice creates a peak demand of power and the grid gets collapse.

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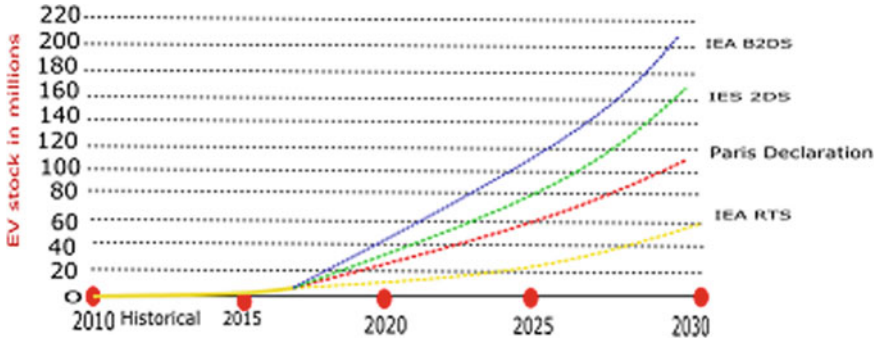

Fig. 1 EVs future deployment scenarios

Some major problem associated with this method is that the price is higher during high demand of power when most of the EVs will get charged. Due to this, grid will bear extra burden as the EVs are increasing every year. Good infrastructure, large capital, and operating expenses are required to support and satisfy the needs of future energy demand.

The problem in the traditional method is solved by using the different methods like the cheapest (TC), economical starting (EC), the low price, (LP) and the last time (LT) schemes. These methods should be deployed with intelligent charger to speed up the charging process thereby reducing the cost. The set of strategies for battery charging have been discussed, and the result obtained are compared with the traditional method to examine the durability and fragility of each one.

2 Related Work

The recent development in the field of EVs has widen the topic of research and their need in the future. Some authors have worked and deduced various method to reduce the electricity cost. Wi et al. [12] presented algorithm based charging of electric vehicle, which uses PV cells and makes system cost effective. Their result showed reduction in 7 to 14% of cost as compared to plug and charge method. Makkonen et al. [13] proposed a system in which charging head both energy management system and the energy storage. They provided a gateway for the mobile energy storage, but they did not compared their result with the traditional method. Tikka et al. [14] deduced a smart charging system in order to minimize the charges. They conducted the charging on a charging testbed. They test the charging of the vehicle at home for a week, compared their result with plug and charge method, and found a reduction in electricity bill.

Gharbaoui et al. [15] presented a system in which scatter communication infrastructure can be utilized. In this, the data of the energy requirements can be exchanged and thereby reducing the charging time.

Valdivia et al. [16] presented a method using particle swarm optimization in plug-in hybrid electric vehicles. They performed the simulation for 24 h for different scenario. They compared their result with other algorithms like GSA, FA and found the better result. Ma et al. [17] presented a strategy of dispersed charging control, which was designed for large number of electric vehicles. The aim is to increase the efficiency of charging by promoting the electricity tariffs of overnight thereby reducing the overall cost. In this, the test was conducted on two-battery capacity.

Mets et al. [18] presented two charging strategies in which local and global iterative strategies were compared. In this, the aim was to reduce the peak power demand. In this, PHEVs from 150 houses were taken, and the test was conducted for 24 h. All specifications were same of each vehicle, and the maximum charging rate was 4.6 kWh. Results show the reduction in peak power loads from 9 to 40%. Gan et al. [19] presented a protocol in which EVs charging schedule is managed, the aim is to arrange the EVs charge as per the electricity demand. They performed the simulations for one day by taking average residential load in the particular area of South California. Cheng et al. [20] presented a strategy by charging the EVs at off-peak hours and thus improving the charging process, they used PSO algorithm and compared the result with an uncontrolled recharge approach.

In this part, we can find there are many works, which tell us about how the growing number of EVs affect the electricity demand. Sharma et al. [21] presented the effects of charging in scattered unbalanced system at urban places, then they analyzed the result with smart charging schemes and found that the uncontrolled charging have the adverse effect on the grid. Acha et al. [22] presented a system in which two types of vehicles were used that are PHEVs and PEVs and suggested a cost-effective exchange between scattered network, power markets, and electric vehicles.

Quian et al. [23] proposed a methodology and a model of electricity demand of electric vehicle, and they compared on the following criteria of uncontrolled off-peak domestic charging, uncontrolled domestic charging, and uncontrolled off-peak domestic. Result suggested that there will be 18% increase in power demand, and they also considered various parameters like arrival time of vehicle and state of charge of vehicles to prepare the statistical model. Last, but not least, we have also accounted the real pricing of electricity for all around the day and over the full year [24].

The authors have proposed many ideas, yet there is a scope for improving the charging and the charging time of the electric vehicle. The various strategies can be formed for the EVs for better charging and charging time on 24 h format.

3 Our Proposal: Improving EVs Charge Strategies

The traditional method is plug and charge, i.e., the charging of battery start as soon as we provide them a plug point with proper power supply. However, this method is ineffective, as it does not consider many parameter like energy efficiency, cost, power demand, and current battery level. We can take this traditional method for our comparative study.

A. Electric factor

The main objective of this paper is to propose new strategies for efficient charging and compare the result obtained with the traditional method of charging, taking into account, various factors like battery status and time available to complete the process of charging. Smart chargers can be of used in any of the one approaches to enhance the charging process at residential homes.

As per the standard IEC 62196 [25], four charging modes are designed for EVs, which are as follows:

- **Mode 1,** this is the most used method for electric vehicle charging at residential houses. In this, 230 V and a current of 16 A is used to charge the batteries. The process may last up to eight hrs. Hence, this method is considered slow method, mode 1 is the most common method used.
- **Mode 2** is the fast charging mode as compared to mode 1, current up to 32 A is supported in this method. Due to high current the charging time is reduced to 4 to 6 h hence, this mode is also called as semi fast mode.
- **Mode 3** this is the fast charging method and current between 32 and 250 A is supported, generally in a mode EVs take less than one hour to recharge their battery level.
- **Mode 4** in this mode current up to 400 A is supported and is also known as ultra-fast charging method. It is an important method as it comprehensively reduces the charging time of the EV batteries. The heat developed might be an issue because many of the battery could not withstand the large amount of current.

The electricity pricing is also to be considered, as the prices are different during day and night in many countries for example United States, Canada, UK, France, Portugal, Spain, Finland, and Latvia [23, 26–29]. We can easily distinguish between high and low price time slots for the charging of EVs.

B. Recharging Methods Proposed

In this proposed work, we have already said that four methods will be discussed which will enhance the charging process with efficient recharges. We assumed that system has smart charging point; communication can be easily done among vehicles and Internet connectivity.

Assume 'T' to be taken as the time period in which electric vehicle would be recharged (arrival and departure), and 'R' is the time period that EV needs to fully recharge its battery, '$P(h)$' is the price of the electricity at that particular hour, 'ch' is the denotation at which the electricity price is the cheapest, and 'Lt' denotes the time at which electric vehicle leaves the parking area, and 'st' and 'ed' represent the starting and ending time of the battery charging. These all parameters are given in the Table 1.

The proposed method are discussed below:

- **The Cheapest (TC)**—This strategy of charging will allocate 'st' for the 'ch' in between of 'R'. For this charging process, the charging period is governed by

Table 1 Different charging parameters

Parameters	Definition	Values
T	Time taken by the vehicle to be recharged	12 h
R	Total time in which EV get fully charged	06 h
$P(h)$	Price of the electricity at that hour	0.152 Euro/kWh
ch	Time in which electricity price is the cheapest	4 AM
Lt	Time when the vehicle leaves the parking lot	7 AM
St	Starting charging time of battery	22 PM
ed	Ending charging time of battery	7 AM

Eq. 1. Electric vehicles will be fully charged only when $\left(\text{ch} + \frac{R}{2}\right) < Lt$

$$\left[\left(\text{ch} - \frac{R}{2}\right) \ldots \left(\text{ch} + \frac{R}{2}\right)\right] \tag{1}$$

- **Economical Starting (EC)**—this strategy of charging will start charging the EVs as soon as the electricity price becomes 'ch' (st = ch), the process will be governed by Eq. 2, and vehicle will be fully charged only when $(\text{ch} + R) > Lt$ is met.

$$[\text{ch} \ldots (\text{ch} + R)] \tag{2}$$

- **Low Price (LP)**—In this strategy, electric vehicle will charge their when the off-peak period begins. This charging strategy is considered for nighttime charges, this strategy is governed by Eq. 3. We consider negative variations in the price of electricity to calculate max $(\Delta P\,(h))$, i.e. when the price of the electricity drops.

$$[\max(P(h)) :: \max(P(h) + R)] \tag{3}$$

- **Last Time (LT)**—In this strategy electric vehicle, will recharge its battery during last part of 'R'. Charging process will finish just before the vehicle is about to leave the parking lot. This process is regardless of the electricity fee. If $T < R$, then LT will be acting like the traditional P&C method. This method is governed by Eq. (4).

$$[(Lt - R) \ldots Lt] \tag{4}$$

Let us take an example for EV Volkswagen Golf having a capacity of 24.2 kWh, at 7:00 p.m. Vehicle reaches at charging which is mode 1 of charging and leaves at 7 a.m. (i.e., $T = 12$; Lt = 7). When the vehicle reaches the charging point, the level of the battery is 75%. As per the data, 2 h are required to recharge the battery completely ($R = 2$). Figure 2 shows the graph having fares of EVs on Y-axis and hours on the X-axis. Taking the traditional method, the vehicle will automatically at 7:00 p.m. (St

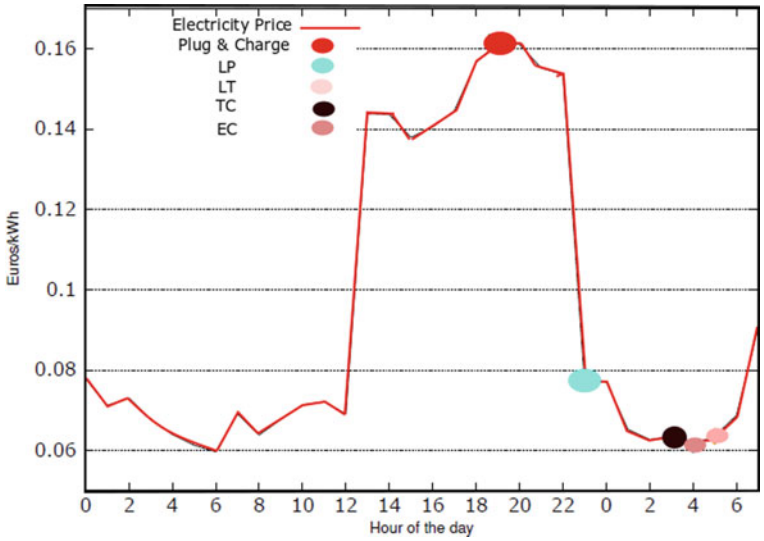

Fig. 2 Illustrated figure, which includes electricity, price (January 2018), and recharging point for different strategy [24]

$= 19 = 7$ p.m.). At this time, it is seen from the graph that the electricity price is the highest.

In the cheapest method, charging of the vehicle will, i.e., at 3 a.m., and the vehicle requires 2 h to complete the charging as this is the most economical period for vehicle charging (3 a.m.–5 a.m.). $([(4-1)\ldots4+1)]$, according to Eq. (1).

In the economical starting method, the vehicle will start charging when the price of the electricity is minimum, i.e., at 4 a.m. and will complete at 6 a.m. $([4\ .\ (4+2)]$, according to Eq. (2)).

In low price method, the vehicle will start recharging at 23 p.m., as during this time the drop in price negligible and off-peak period also begins. The charging process would be [23…1] as per Eq. (3) (Table 2).

The last method is last time in which we utilize the last time, which is left for the charging, i.e., the charging will start at 5 a.m. and will remain till 7 a.m., after that the vehicle will leave the parking lot, $([(7-2).0.7]$, according to Eq. (4).

4 Simulation Environment

The simulation was done on three different environment and as per the average battery level. The aim is to analyze the methods under various energy requirements. The scenarios are:

Table 2 EVs during 2016 [28]

Make and model	Battery capacity (kWh)	Market share (%)
Nissan leaf	24	16.2
Citroen C-zero	15	15.5
Renault Zoe	22	12.6
BMW i3	22	10.6
Renault Kangoo	33	10.3
Nissan NV 200	24	9.6
Smart fortwo	17.6	4.8
Volkswagen Golf	24.2	4.3

- **Regular demand**, in which battery level of vehicle follow a Gaussian distribution with a mean (μ) of 72 and 10% standard deviation (σ). The data is analyzed after single day use of electric vehicle, as per Qian et al. [23].
- **Soaring demand**, in which battery level of vehicle follow a Gaussian distribution with a mean (μ) of 50 and 10% standard deviation (σ).
- **Additional demand**, this is a different scenario in which battery level of vehicle follow a Gaussian distribution with a mean (μ) of 25 and 10% standard deviation (σ).

The battery capacity level is also considered in this part, for the battery with less capacity will require less time, and the battery with larger capacity will require larger time to charge. By simulating with the help of above charging methods, various results have been shown. We use Monte Carlo method [30] for the various vehicle included. Table 3 shows various parameter used in the simulations.

More details are discussed and explained below.

- **Total number of vehicles**. A total number 365000 EVs data was collected, i.e., 1000 vehicles per day for the entire year.

Table 3 Regular demand

Metrics	P & C	TC	EC	LP	LT
Megawatts charged	2.42	2.32	1.85	2.32	2.38
Electricity price (€/vehicle per year)	349.72	139.28	104.15	161.3	148.79
Price diff. compared to P&C (%)	–	− 60.17	− 70.22	− 53.88	− 57.46
Recharged energy (average %)	27.97	27.97	22.08	27.78	27.98
Net battery level (average %)	99.9	99.62	94.3	99.7	99.9
#EVs battery level < 75%	635	635	27,180	870	635
#EVs battery level < 50%	0				
#EVs battery level < 25%	0				
Battery level at starting (average %)	71.9				

- **Vehicle's appearances model**. In this, we have to see when the vehicle is arriving at the place to be charged. As per the traditional method, it will start charging at that instant. To make it realistic, the vehicle follows a Gaussian distribution with μ equal to 1080 min and σ equal to 60 min. Usually vehicles reach at the residential house from 4 to 9 p.m. Many values have taken from the previous works [19–23].
- **Journey duration model**, which tells the appropriate travel time until reaching the recharging point. Weibull distribution is followed by these values [30–35] with $\alpha = 45$ min, $\beta = 1.8$, and $\gamma =$ zero. Most of the journey time requires 45 min or less than that.
- **Recharging time model**. This parameter tells the maximum time, which is required by the EVs to charge their battery. This follow a Gaussian distribution mean (μ) of 700 and 150 min of standard deviation (σ). Most of the vehicles are parked for an average time of 9–14 h per day.
- **Battery measure model**. In this, it tells us about the level of charging left when it reaches to the charging point. We discussed about three kind of scenario (regular demand, soaring demand, and additional demand). It follows a Gaussian distribution with different parameters (μ is 70, 50, and 25%), and σ is 10%.
- **Power at charging point**. Since we are interested for the charging of EVs at houses, so it has to follow Mode I, in which batteries will be charged at 230 V and 16 A.
- **Energy dissipation by heat**. Batteries suffer from heat loss during the charging process. These losses are correlated to current and voltages, i.e., low battery charging encounters less loss as compared to larger batteries. We have assumed that 10% of the energy is wasted during charging.

5 Results

In this part, results from the scenarios are discussed above and described. The performance of different charging methods are also analyzed under different conditions.

A. ***First scenario: Regular Demand***

As per Quian et al. [26], after a day use, the level of a battery of a vehicle remains at 72%, so for this scenario, we consider the average battery level to be 71.90 before charging.

Table 3 shows various output obtained from the regular demand scenario. As we see that energy charged is similar to all methods except the EC method. If we see the electricity cost, we can easily distinguish the difference per vehicle (104–349€). If we are using this scenario the cost, saving is about 54–70%

B. ***Second scenario: Soaring demand***

In this second scenario, we considered the soaring demand as vehicle would start charging when the initial value of the battery level is 50%. As per Qian et al. [26],

Table 4 Soaring demand

Metrics	P & C	TC	EC	LP	LT
Megawatts charged	4.31	4.07	2.84	4.09	4.23
Electricity price (€/vehicle per year)	605.42	251.18	163.87	267.43	278.06
Price diff. compared to P&C (%)	–	− 58.51	− 72.93	− 55.83	− 54.07
Recharged energy (average %)	49.66	47.80	33.79	48.48	49.66
Net battery level (average %)	99.84	97.97	83.96	98.65	99.84
#EVs battery level < 75%	1000	506	120,072	7227	1000
#EVs battery level < 50%	506	506	18,774	788	506
#EVs battery level < 25%	0				
Battery level at starting (average %)	50.18				

this level battery shows that it has not been recharged for almost two days. Table 4 is the output obtained by this scenario.

As we see in the table that the energy charged by the vehicle for all the methods are almost the same, although the consumption of energy is doubled as compared to regular demand scenario because the battery level in the starting was reduced as compared to regular demand. Again, EC method fails to meet the required levels as most of the vehicles are waiting for the price of energy to be cheapest. If we look the difference in price in all the methods, we can see a remarkable difference in all the prices in Table 4. The cost of saving also ranges from 54.07 up to 72.93%. When we see the final level of the battery, we can see the levels are almost same except EC method, which is 83.96%. We can see that all vehicles finished their charging on proper time even when they started with battery level less than 50%. Some of the vehicles could not meet the final level of battery as given in Table 4. EC method is showing some defect as it is showing deficiency to meet the required level.

In this scenario, the last time gives the best performance in terms of battery charging level and cost saving.

C. *Third scenario: Additional Demand*

In this, we analyzed the scenario in which additional demand of energy is required to charge a vehicle, battery level is very low, i.e., 25%.This is the extreme condition which is being discussed.

When we compare the result among all the methods, energy consumed by the vehicle is higher in this scenario. If we compare it to regular demand scenario, energy required is 160% more. Even the EC method work worse for this scenario as vehicle only reach 67% of the battery level. The savings of the price is seen from this method if we compare to our traditional method. The savings of 46–75% can be obtained. In this scenario, there were insignificantly number of vehicles that were not able to full charge their battery. The EC method was not able to fulfill its criterion as seen in Table 5. However, it is impossible to find additional demand for

Table 5 Additional demand

Metrics	P & C	TC	EC	LP	LT
Megawatts charged	6.43	5.92	3.55	5.91	6.34
Electricity price (€/vehicle per year)	855.5	390.8	212	371	454
Price diff. compared to P&C (%)	–	− 4.3	− 75.2	− 56.53	− 46.9
Recharged energy (average %)	74	69.7	42.4	70	74
Net battery level (average %)	99.5	94.5	67.5	95	99.5
#EVs battery level < 75%	1730	17,000	206,700	29,700	1730
#EVs battery level < 50%	1000	1000	10,000.	1000	530
#EVs battery level < 25%	530	530	17,000	650	
Battery level at starting (average %)	25				

so many vehicles. Last time methods performs good in this scenario as it gives good performance, battery level, and cost savings.

6 Conclusions

EV demand is increasing day by day, as the technology is changing; we have to eventually change the methods of charging the batteries thereby reducing the cost of recharging the EVs.

The traditional method is mostly used to charge the batteries, and it is not very efficient, as it does not consider any quantity to boost the efficiency of the charging process. We have to consider various parameter like battery level, price of electricity, load on grid, etc. We proposed four charging methods, which seeks to maximize the battery charging by reducing the time of charging and its cost.

Number of vehicle data was analyzed for regular demand, soaring demand, and additional demand scenario. All the scenarios have been studied, and we can see improvement in various parameters in percentage. We can clearly see the difference in megawatts charged in these four methods, and we can also the price difference when we are using these four methods. There has been difference of time while achieving the net battery level.

This case study can also be implemented in India as the demand of EVs are increasing day by day. Looking into the fact of this demand, the need of infrastructure and proper charging points is the need of an hour, and with this increase of EVs, there will be a burden on the grid due to the battery charging, and this will be the next problem, which can be easily solved by using these methods. By utilizing the flexible electricity prices and the method of charging proposed above, we can tremendously reduce the infrastructure cost and charging points, as we will be utilizing the residential charging points and at last reducing the load on the grid.

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Reduction of Mutual Coupling in Dual Band Antenna Array Using Novel Metamaterial Structure

B. Siva Chaitanya, P. Prasanna Kumar, and Prerna Saxena

1 Introduction

Nowadays, due to advancements in wireless communications demand for compactness has increased. Microstrip patch antenna has an advantage of low profile and compactness. Due to the demand in wireless communications, we need antennas that operate at different frequencies. Designing antennas at each frequency in a single device occupies more space and violates the condition of compactness. So an antenna that operates at multiple frequencies is required. Today, devices have more than one antenna embedded inside them. Such antennas are called array antennas. Array antennas have advantages like high gain and controlled radiation pattern. In array, antenna mutual coupling is inevitable. It degrades the performance of the system by disturbing radiation patterns. So coupling is a serious phenomenon and should be taken care of for the proper functioning of antenna arrays.

To overcome the effect of mutual coupling in array, many techniques have been implemented. In [1], meander structure is used to minimise the coupling effect, but antenna dimensions are very large. The isolation between antennas is −34.3 dB by usage of ML slot in [2]. In [3], split ring resonators are used but the isolation at 2.4 GHz is only −24 dB. *C*-shaped DGS(Defective Ground Structure) is used to reduce coupling but size of antenna is more with high-mutual coupling at desired frequencies in [4]. In [5] *H*-shaped DGS used, the dimensions of antenna are very

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large. The length of antenna is more in [6] with moderate coupling reduction between antennas. In [7, 8] EBGs (Electro Band Gap) are used, but the reduction in coupling is limited. In [9, 10], the number of decoupling elements used are very high which occupies more space. In [11], isolation between antennas is limited.

Nevertheless, these methods limit the space available for other components of the device and interrupt antenna pattern. Metamaterials have evolved as a new area of research in electromagnetics. Recent advances in modelling of electromagnetic metamaterials make this an appropriate approach for controlling the performance of the antenna. Several researches are reported for reduction of coupling using metamaterials. In [12], the isolation between antenna arrays at 2.4 GHz is very low. The coupling between antennas is high and accounts to −20 dB and −25 dB at lower frequency and higher frequency, respectively in [13]. The size of dual band antennas is large and distance between them is also more in [14, 15]. In [16] the single band antenna dimensions and spacing between array elemtes is high.

A novel dual band antenna is proposed in this paper, and the use of metamaterial structure reduces coupling. The paper continues as follows: Sect. 2 describes the dual band microstrip patch antenna design in array and its simulation results of $|S_{11}|$ and gain. Section 3 discusses the design of metamaterial unit cell with its simulation parameters. In Sect. 4 parametric analysis for placement of metamaterial unit cell in antenna array are carried out. In Sect. 5 results of array loaded with metamaterial are presented. Section 6 concludes this work.

2 Proposed Antenna Design

The proposed structure of dual band microstrip patch antenna is shown in Fig. 1. It is designed on FR-4 substrate with thickness 1.588 mm, dielectric constant and loss tangent of 4.4 and 0.02, respectively. It has ground plane and radiating patch made of copper on bottom side and top side of substrate, respectively. The dimensions of dual band antenna are as follows: $W_s = 35$ mm, $L_s = 35$ mm, $W_p = 14$ mm, $L_p = 4.5$ mm, $W_f = 15.6$ mm, $L_f = 3$ mm, $g = 1$ mm.

The dimensions of the proposed meander structure in the antenna are follows: $W_{sl} = 0.5$ mm, $V_{sl1} = 12.5$ mm, $V_{sl2} = 6$ mm, $H_{sl1} = 1.5$ mm, $H_{sl2} = 2$ mm, $P_{ms} = 7.875$ mm.

The dimensions of the proposed DGS are as follows: $W_{gs1} = 2$ mm, $W_{gs2} = 5$ mm, $L_{gs1} = 28$ mm, $L_{gs2} = 4.5$ mm, $L_{gs3} = 2$ mm, $P_{gs1} = 9$ mm, $P_{gs2} = 3.5$ mm.

The S-parameters and gain of dual band antenna are shown in Figs. 2 and 3, respectively. It has resonance at 2.38 GHz and 5.82 GHz having $|S_{11}| - 34.88$ dB and −33.24 dB respectively, with bandwidth of 40 MHz and 150 MHz respectively. The gain of proposed antenna at 2.4 GHz is 2.44 dB and at 5.8 GHz is 2.54 dB.

The antenna array configuration is depicted in Fig. 4. The antennas are separated by distance of 35 mm from port to port and having distance of 7 mm between ground slots.

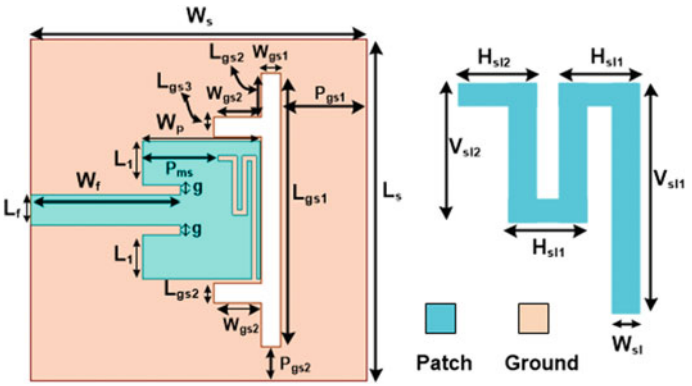

Fig. 1 Proposed dual band antenna

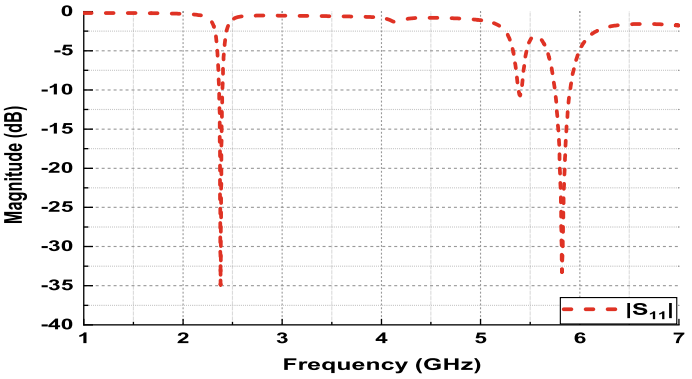

Fig. 2 Reflection coefficient versus frequency of dual band antenna

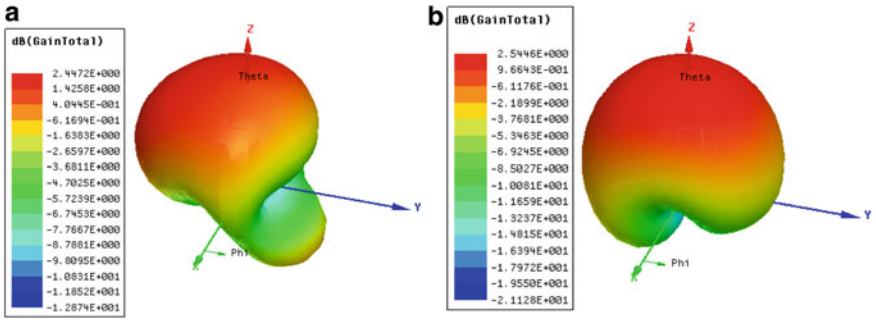

Fig. 3 Proposed antenna: **a** Gain at 2.4 GHz, and **b** Gain at 5.8 GHz

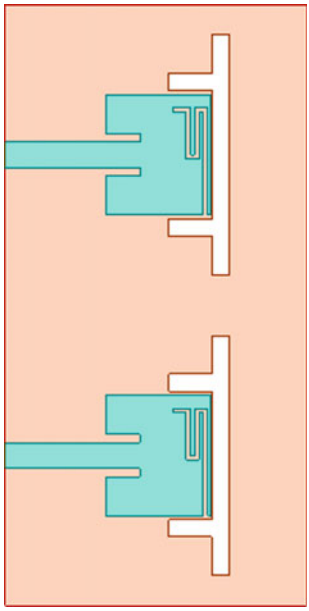

Fig. 4 1×2 array configuration

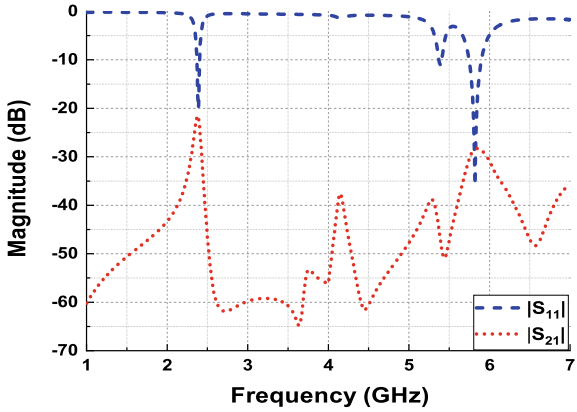

Fig. 5 Magnitude of *S*-parameters of antenna array

When antennas are placed in array, mutual coupling becomes inevitable. The coupling is mainly due to surface waves of antennas that propagate along substrate. To reduce the effect of these waves on antenna performance, decoupling units should be incorporated between them. These decoupling units acts as stop band at desired frequencies and blocks the surface waves motion and avoid performance degradation of other antennas in array. The array configuration's *S*-parameters are given in Fig. 5. It has resonance at 2.38 GHz and 5.82 GHz, having $|S_{21}| - 23.26$ dB and -28.71 dB at 2.4 GHz and 5.8 GHz respectively, with bandwidth of 30 MHz and 150 MHz respectively. The field distribution of array antenna is shown in Fig. 6.

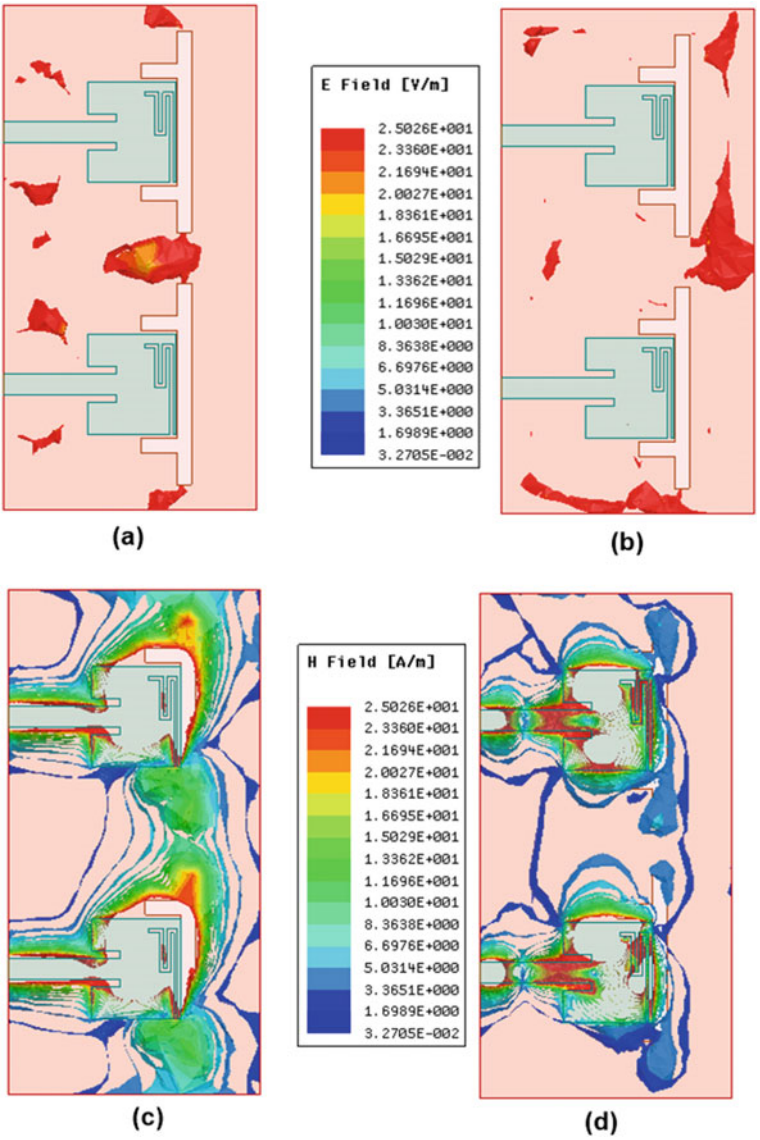

Fig. 6 **a** *E*-field at 2.4 GHz, **b** *E*-field at 5.8 GHz, **c** *H*-field at 2.4 GHz, and **d** *H*-field at 5.8 GHz

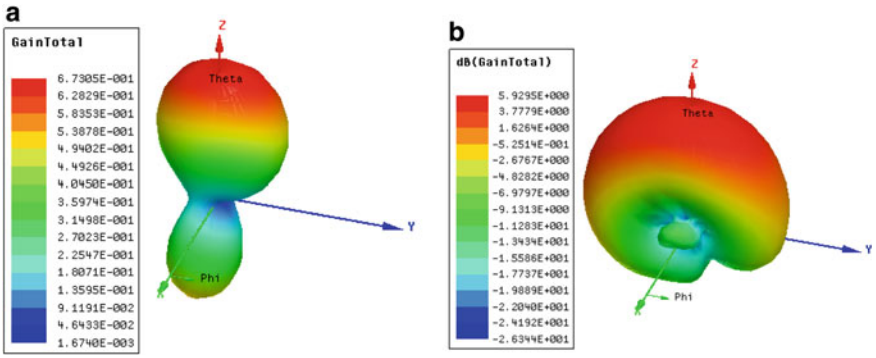

Fig. 7 Proposed antenna array: **a** Gain at 2.4 GHz, and **b** Gain at 5.8 GHz

The dual band antenna array has gain of 0.67 dB at 2.4 GHz and 5.92 dB at 5.8 GHz as shown in Fig. 7.

It can be seen clearly that the majority of coupling between antennas in the array are due to H-field. For the purpose, μ negative metamaterial is proposed.

3 Proposed Metamaterial Unit Cell

A metamaterial having negative permeability operating at desired bands, i.e. 2.4 and 5.8 GHz is designed and its simulation setup is shown in Fig. 8.

This cell is designed on FR-4 substrate with relative permittivity 4.4 and loss tangent 0.02. The thickness of substrate is 1.588 mm with area 7.1×7.1 mm^2.

Unit cell has boundary conditions as follows: it has PEC (Perfect Electric conductor) boundary along yz plane, PMC (Perfect Magnetic Conductor) boundary along xz plane. The top view of unit cell is shown in Fig. 9. The metamaterial unit cell has the

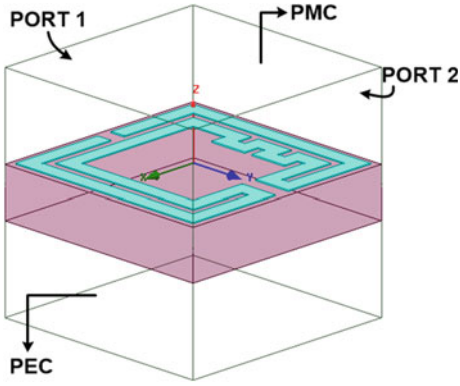

Fig. 8 Simulation setup of proposed metamaterial unit cell

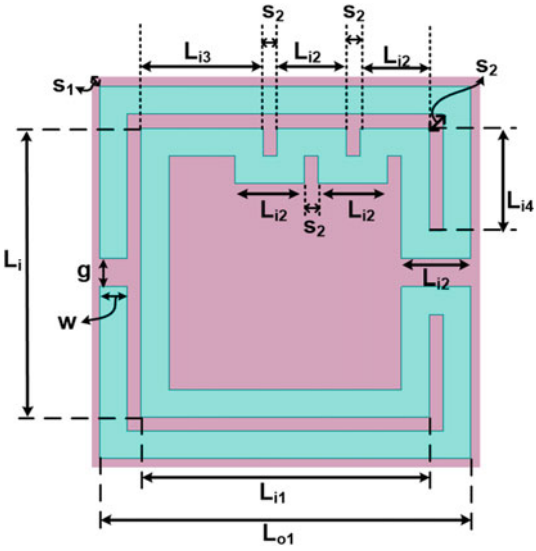

Fig. 9 Proposed metamaterial unit cell

dimensions as follows: $L_{o1} = 6.7$ mm, $L_{o2} = 3.1$ mm, $L_i = 5.2$ mm, $L_{i3} = 2.2$ mm, $L_{i4} = 1.85$ mm, $S_1 = 0.2$ mm, $S_2 = 0.25$ mm, $W = 0.5$ mm, $g = 0.5$ mm.

The metamaterial parameters are retrieved using a standard extraction procedure [17]. The steps are summarised below:

1. S-parameters are defined from (1, 2).

$$S_{11} = \frac{\rho_1(1 - e^{j2Nkd})}{1 - \rho_1^2 e^{j2Nkd}} \tag{1}$$

$$S_{21} = \frac{(1 - \rho_1^2)e^{jNkd}}{1 - \rho_1^2 e^{jNkd}} \tag{2}$$

   where, k is wave number, d is thickness of the metamaterial unit cell, and N is refractive index.
2. Determine the material impedance, z, as follows

$$z = \pm\sqrt{\frac{(1 + S_{11})^2 - S_{21}^2}{(1 - S_{11})^2 - S_{21}^2}} \tag{3}$$

3. Determine the term e^{jkNd} by taking $\rho_1 = (z - 1/z + 1)$

$$x = e^{jkNd} = \frac{S_{21}}{1 - S_{11}(z - 1/z + 1)} \tag{4}$$

4. Determine the complex refractive index

$$N = [\mathrm{Im}(\ln(x)) + 2\pi m - j\mathrm{Re}(\ln(x))]/kd \tag{5}$$

5. Determine the material parameters, ϵ_r and μ_r

$$\epsilon_{\mathrm{eff}} = N/z, \quad \mu_{\mathrm{eff}} = N * z \tag{6}$$

The *S*-parameters and extracted permeability for the proposed metamaterial unit cell are shown in Figs. 10 and 11, respectively.

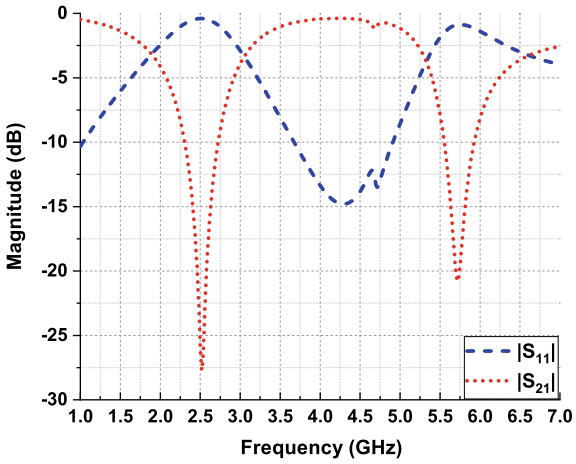

Fig. 10 Magnitude of *S*-parameters of metamaterial unit cell

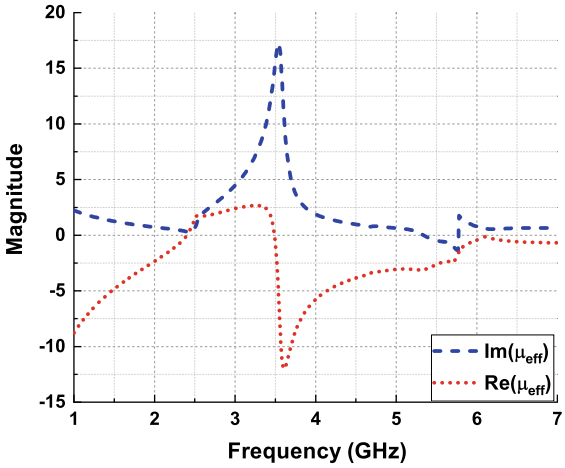

Fig. 11 Extracted effective permeability of the proposed metamaterial unit cell

4 Parametric Analysis for Placement of Metamaterial Unit Cells

In this section, we analyse the placement of metamaterial unit cells in array antenna to reduce the mutual coupling.

4.1 Case-0

In Fig. 12, antenna array elements having coupling effect at edges due to H-field.

So, to reduce the coupling effect metamaterial cell has to be placed in the antenna array.

4.2 Case-1

In Fig. 13, it can be seen that the coupling between antennas at 5.8 GHz is reduced by placement of metamaterial unit cells at left edge because the field gets coupled to unit cell.

But there is effect of coupling between antennas elements at right edge.

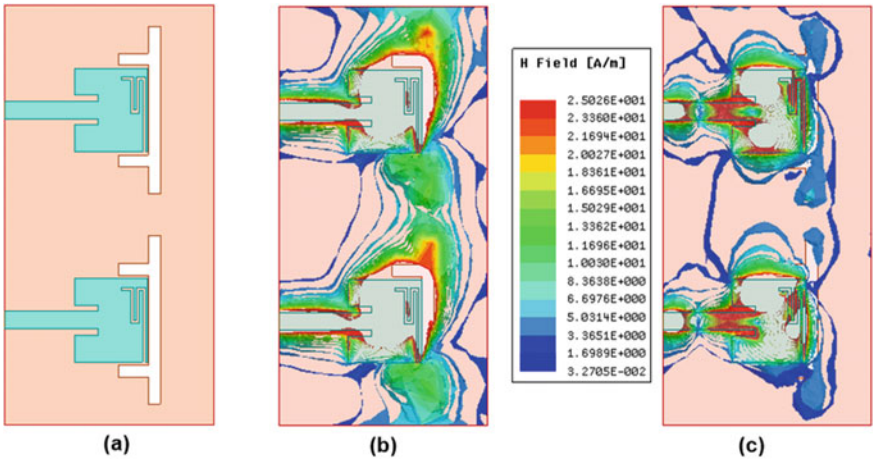

Fig. 12 **a** Array antenna, **b** H-field at 2.4 GHz, and **c** H-field at 5.8 GHz

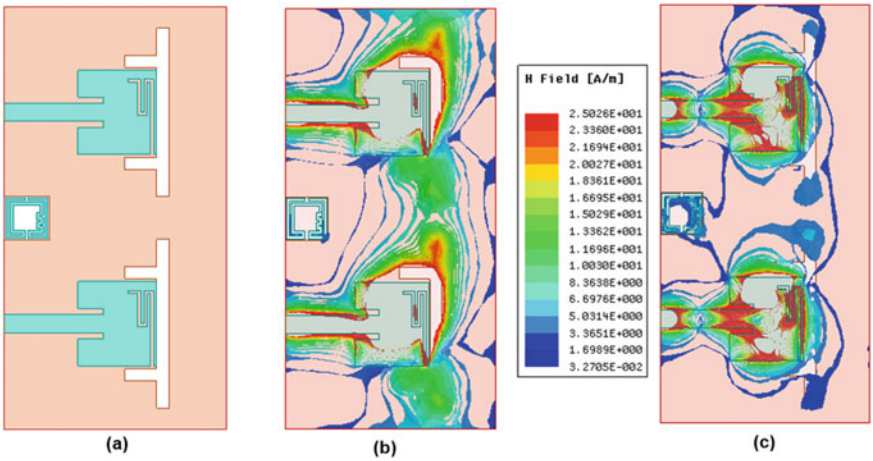

Fig. 13 **a** Array antenna loaded with one unit cell, **b** *H*-field at 2.4 GHz, and **c** *H*-field at 5.8 GHz

4.3 Case-2

In Fig. 14, it can be seen that the coupling between antennas at 2.4 GHz is reduced by placement of metamaterial unit cells at right edge because the field gets coupled to unit cell. But there is effect of coupling between antennas elements at middle.

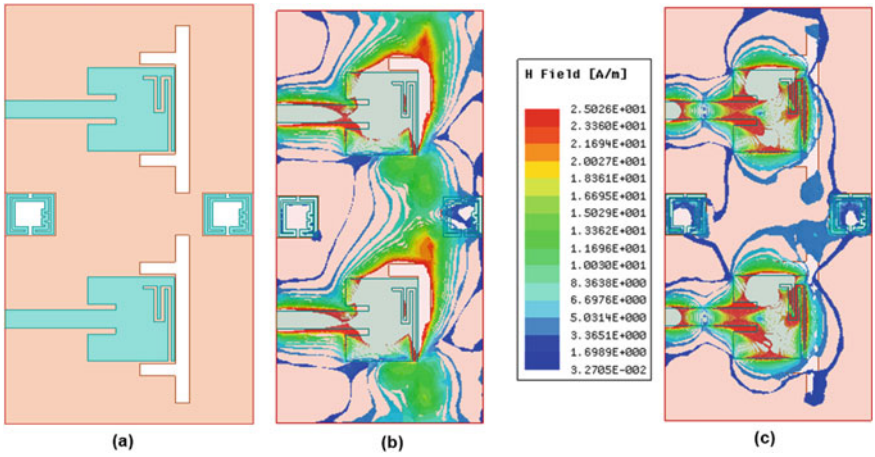

Fig. 14 **a** Array antenna loaded with two unit cell, **b** *H*-field at 2.4 GHz, and **c** *H*-field at 5.8 GHz

4.4 Case-3

In Fig. 15, it can be seen that the coupling between antennas at 2.4 GHz is reduced by placement of metamaterial unit cells at middle because the field gets coupled to unit cell.

To further decrease the effect of coupling, more number of metamaterial unit cells has to be incorporated in the array.

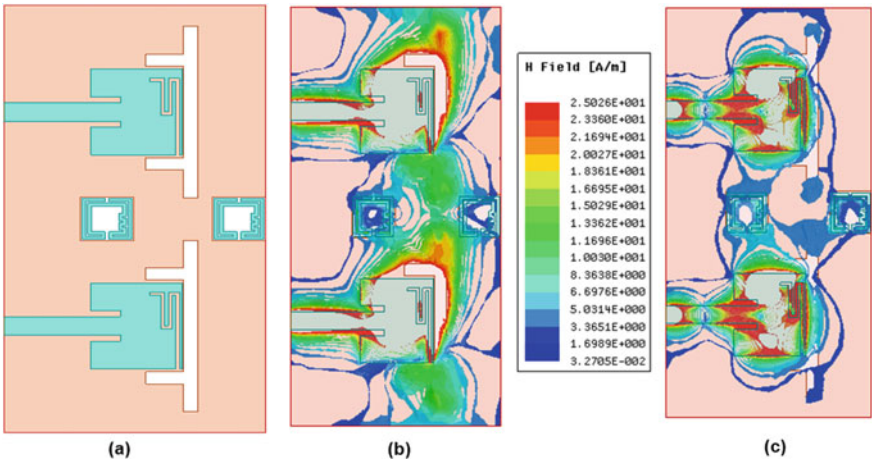

Fig. 15 **a** Array antenna loaded with two unit cell, **b** *H*-field at 2.4 GHz, and **c** *H*-field at 5.8 GHz

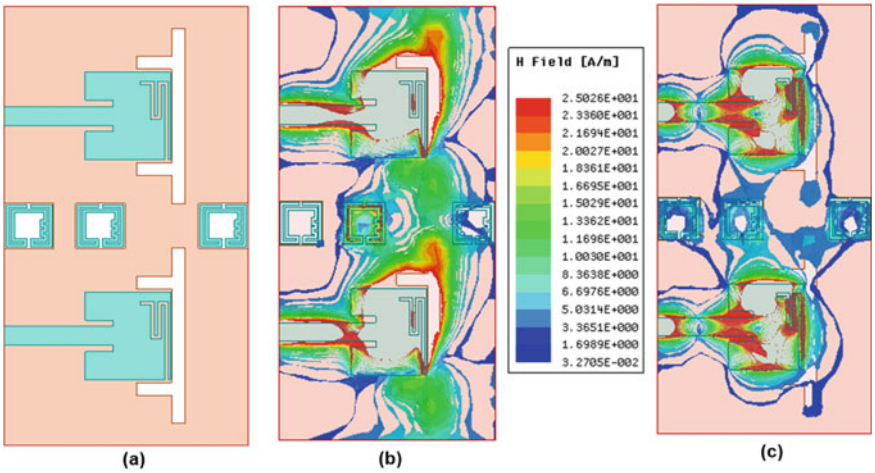

Fig. 16 **a** Array antenna loaded with three unit cell, **b** *H*-field at 2.4 GHz, and **c** *H*-field at 5.8 GHz

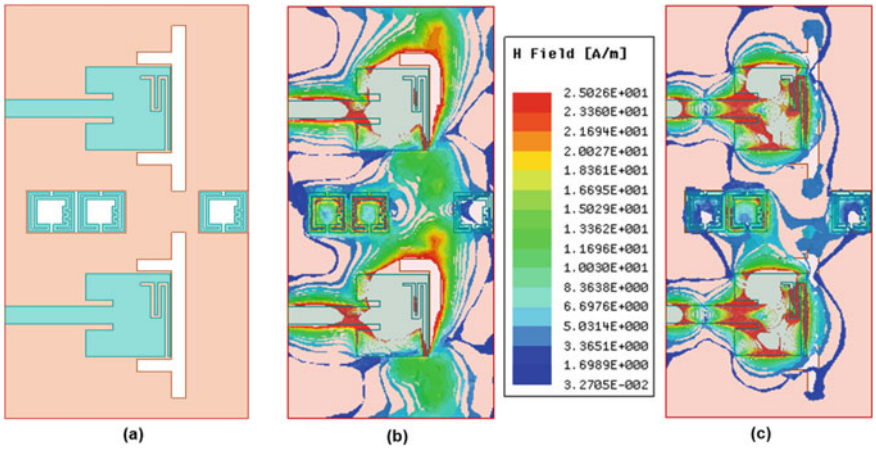

Fig. 17 **a** Array antenna loaded with three unit cell, **b** *H*-field at 2.4 GHz, and **c** H-field at 5.8 GHz

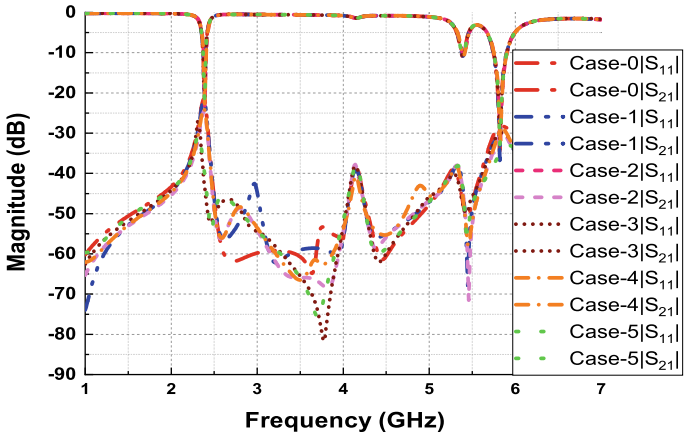

Fig. 18 Comparison of *S*-parameters for various cases

4.5 Case-4

In Fig. 16, it can be seen that the coupling between antennas at 2.4 GHz is increased by placement of metamaterial unit cells at left edge.

To decrease the effect of coupling metamaterial unit cells has to be placed at a definite position.

4.6 Case-5

In Fig. 17, it can be seen that the coupling between antennas at 2.4 and 5.8 GHz is decreased by optimum placement of metamaterial unit cells.

By parametrically placing of metamaterial cells in antenna array coupling at 2.4 and 5.8 GHz is reduced.

Figure 18 gives us information about *s*-parameters of different cases. From Fig. 18, Case-5 has better isolation values.

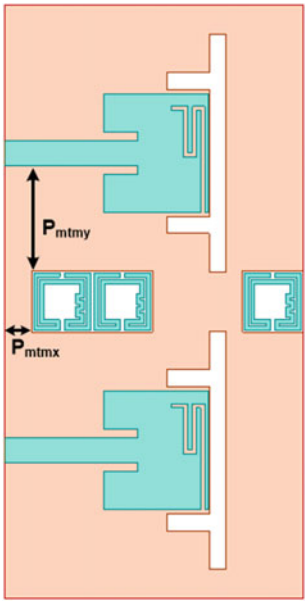

Fig. 19 Dual band array loaded with proposed metamaterial having $P_{mtmx} = 3.15$ mm, $P_{mtmy} = 12.45$ mm

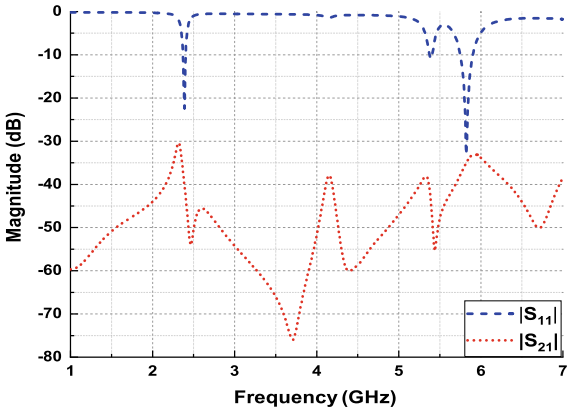

Fig. 20 *S*-parameters of dual band array loaded with proposed metamaterial

5 Results and Discussion

The proposed dual band antenna is placed in array and designed metamaterial unit cells are placed between array elements is shown in Fig. 19.

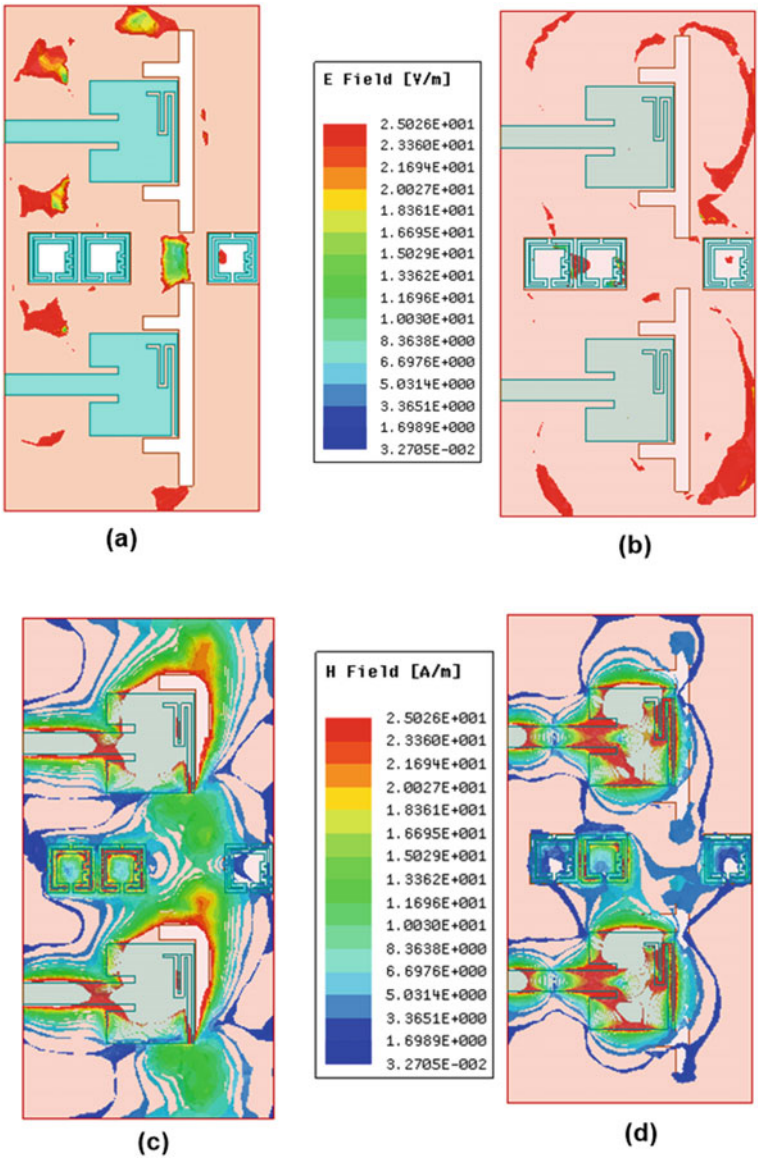

Fig. 21 **a** *E*-field at 2.4 GHz, **b** *E*-field at 5.8 GHz, **c** *H*-field at 2.4 GHz, and **d** *H*-field at 5.8 GHz

Antenna array is loaded with μ negative metamaterial unit cells in middle. Figure 20 represents S-parameters.

The value of $|S_{21}|$ at 2.4 GHz is −42.29 dB and 5.8 GHz is −35.86 dB.

Therefore, by placing metamaterial unit cells between array elements, the coupling between antennas is decreased by −19 dB at 2.4 GHz and −7 dB at 5.8 GHz. This can been seen from field distribution in Fig. 21.

The proposed metamaterial loaded dual band array antenna exhibits a gain of 2.39 dB at 2.4 GHz and 6 dB at 5.8 GHz, as depicted in Fig. 22.

The proposed antenna array loaded with metamaterial is compared with different state-of-the-art approaches and represented in Table 1. It can be observed that the designed μ negative metamaterial unit cell in array antennas has better isolation enhancement with minimum distance between antenna elements.

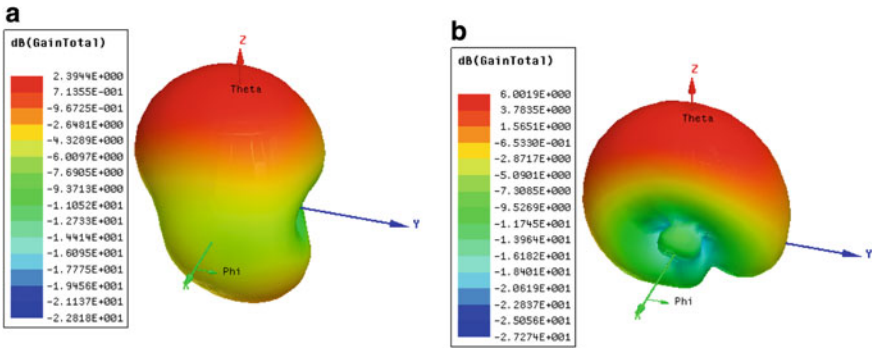

Fig. 22 Gain at **a** 2.4 GHz, and **b** 5.8 GHz

Table 1 Performance summary and comparison with the state-of-the-art designs

References	Resonant frequency (GHz)	Array size (mm^2)	Edge to edge distance (λ)	Isolation (dB)
[12]	2.4	56 × 117	0.128	−18
				−15
[13]	2.4 and 5.8	52 × 60	0.112 ($\lambda_{2.4}$)	<−20
[14]	2.4 and 5.8	52 × 60	0.112 ($\lambda_{2.4}$)	−38 and −30
[15]	2.4 and 5.4	N.A	N.A	−35 and −42
[16]	5.3	40 × 72	0.38	−45
This work	2.4 and 5.8	35 × 70	0.056 ($\lambda_{2.4}$)	−42 and −36

6 Conclusion

In this paper, a novel dual band antenna array operating at 2.4 and 5.8 GHz was designed. A novel metamaterial with negative permeability was proposed to minimise the effect of mutual coupling at 2.4 and 5.8 GHz. The proposed design reduces coupling by −19 dB and −7 dB at lower frequency and higher frequency, respectively. The *S*-parameters and gain of the antenna array without metamaterial and with metamaterial has been described. The proposed metamaterial loaded dual band antenna array is of compact size and has good isolation as compared to the state-of-the-art and can be used in applications where compactness is required.

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Audio Watermarking Scheme for Ownership Verification Using ANN Based Optimal Quantization Strategy

Hanan S. Alshanbari

1 Introduction

Today, digital audio signals have become a very popular form of human communication medium. With few clicks, one can send audio message to a friend, who is far away. Simplicity and compact size of audio signals has increased its popularity for human communication. Audio signal can be classified on the basis of channel used [1]; for example: mono, stereo, etc. Also, they can be classified on the basis of formats [2, 3]; for example: wav, mp3, ogg, etc. Audio signals are recorded as the variation of air pressure through a microphone, which further converted it into a digital signal via sampling and quantization process [4]. It is quite obvious that higher value of sampling and quantization leads to a better audio quality.

The security of this audio signal from an unauthorized access/use can be ensured via encryption/watermarking. The main difference between these two techniques is that encryption keeps the signal secure by making it imperceptible [5], whereas in watermarking, signal remains perceptible but secured [6, 7]. In watermarking, secret information is stored into the original audio signal, which can be verified later for ownership check as well as host authentication [7]. There are many categorizations of audio watermarking [7, 8], like: blind/non-blind, robust/fragile/semi fragile, spatial/transform domain, etc. Blind watermarking means only watermarked signal is required with secret key for watermark extraction/authentication process. On the other hand, non-blind watermarking required several other data (original host/original watermark) for successful extraction. Blind approach is always preferable because of its independence working without external data.

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Robust watermarking provides the robust nature to the watermark, whereas fragile watermarking provides fragile nature [7, 8]. Robust watermarking is used for ownership verification, and fragile is used for content authentication. Usually, transformed domain approached is more preferred for robust watermarking due to its ability to locate high-energy component for watermark insertion. On the other hand, fragile uses time domain (like LSB substitution) and provide tamper detection with low time complexity.

Transform domain approach is well suited for ownership verification as inserted watermark does not get destroyed even in case of intentional/unintentional attack: like cropping, compression, etc. [9, 10]. One of the main challenges with robust watermarking is to get an optimal trade-off between imperceptibility and robustness of the scheme [10]. The iterative approach and soft computing approach always increases the time complexity of watermarking scheme many folds [11, 12].

The proposed work is trying to obtain this trade-off in a faster way by incorporating the ANN for relationship learning. ANN is known for its pattern recognition ability, and same is used in this work to learn audio signal's unique and respective quantization factor. Once learning is done, the ANN is used to predict the value for new audio signals.

2 Literature Review

There are various types of audio watermarking scheme that have been proposed by various researchers and have different objectives, such as content authentication [13], tamper detection [14], tamper recovery [15], and ownership verification [16–18]. As the proposed work is for the ownership verification, this literature review provides a comprehensive insight of robust audio watermarking techniques.

Bhat et al. [10] proposed an adaptive quantization strategy for audio watermarking using the L2 norm of DWT-SVD (discrete wavelet transformed—singular value decomposition) signal's singular values. The method worked well, but the issue was that it was not able to give optimal values of quantization factor in order to obtained best trade-off between imperceptibility and robustness. The method proposed by Lei et al. [11] incorporated the optimization strategy (differential evolution) in SVD domain for optimal embedding, and obtained result was also good. The main limitation of their work was its high time complexity as evolutionary algorithms are prone to take more time in watermarking optimization due to its iterative nature.

Su et al. [12] proposed another robust audio watermarking scheme with scaling factor optimization. This method used heuristics approach for guaranteed SNR value. The results were good, but time complexity was again high due to involvement of heuristics approach. Xiang et al. [16] proposed a spread spectrum and discrete cosine transform (DCT)-based audio watermarking approach. The PN sequences were used as a watermark, and same was hidden into the audio signal after its segmentation using DCT transform in order to locate energy dense regions of audio signal. The correlation coefficients were used to check the hidden watermarks after different

attacks. The performance was good, but the output (bits per second) was low (84 bps).

Hwang et al. [17] proposed a quantization index modulation (QIM)-based adaptive watermarking strategy for stereo audio signals. This scheme used the ratio of singular values for the QIM based embedding, which was a new methodology for embedding. This obtained result and watermarked audio output were quite good. The use of adaptive quantization improved the performance even further. The main limitation was use of same adaptive formula for every audio signal, which restricts the optimization of quantization index. Bhat et al. [18] proposed another watermarking scheme for copyright protection of audio signals. This scheme [18] used the Euclidean norm of SVD transformed signal's singular values for watermark insertion. Insertion was done by quantizing the norms. After norms quantization, scheme re-calculates singular values and replaced the same in original audio signal. The invariant nature of singular values helped in getting very good result against different attacks. The manual calculation of quantization factor was main drawback, which limits the performance of scheme.

The proposed work carries forwards the concept proposed by Ref. [18]. In addition, it proposes a way to check the performance of audio watermarking scheme in terms of both imperceptibility and robustness simultaneously by incorporating the objective function variation with respect to quantization factor. Also, to obtain an optimal performance in a speedy manner, a trained ANN (with 100 audio samples) has been used for quantization factor prediction.

3 Proposed Audio Watermarking Scheme

The work carried out in this study can be divided into three main sections: watermark embedding, watermark extraction, and finding of the optimal quantization factor. The same is explained in Sects. 3.1, 3.2, and 3.3.

3.1 Watermark Embedding

Following steps are followed during the watermark embedding:

1. Read the 1D audio signal (mono) and resize it to 230,400 samples.
2. Segment the audio signal into the size of 225 samples of each.
3. Convert each segment into 2D matrix (M) of 15 × 15.
4. Calculate the SVD of each 2D matrix such as Eq. (1)

$$M = U \times S \times V^T \tag{1}$$

5. Calculate the norm of each singular matrix (S) using Eq. (2), which have "n" singular values (SV)

$$\text{norm} = \sqrt{\left(\sum_{i=1}^{n} (\text{SV})_i^2\right)} \tag{2}$$

6. Calculate a decision factor (DF) for each matrix using Eq. (3) and set a value of μ (quantization factor). Here, the bracket represents floor value.

$$\text{DF} = \left\lfloor \frac{\text{norm}}{\mu} + \frac{1}{2} \right\rfloor \tag{3}$$

7. Read the binary image watermark (32×32) and convert it into 1D watermark (W), so that 1 bit can be inserted into each segment
8. Follow the following decision conditions (if else: a, b, c) to find out the new norms (norm_{new}) for each matrix segment

   a. **if** (mod(DF, 2) "is equal to" W(segment))

$$\text{norm}_{\text{new}} = \text{DF} \times \mu \tag{4}$$

   b. **else if** (mod(DF, 2) "is not equal to" W(segment)) && (DF "is equal to" floor(norm/μ))

$$\text{norm}_{\text{new}} = (\text{DF} + 1) \times \mu \tag{5}$$

   c. **else if** (mod(DF, 2) "is not equal to" W(segment)) && (DF "is not equal to" floor(norm/μ))

$$\text{norm}_{\text{new}} = (\text{DF} - 1) \times \mu \tag{6}$$

9. Calculate new singular values (SV_{new}) using Eq. (7)

$$\text{SV}_{\text{new}} = \frac{\text{norm}_{\text{new}}}{\text{norm}} \times \text{SV} \tag{7}$$

10. Use SV_{new} with original U and V matrix to obtain watermarked 2D segments.
11. Convert 2D watermarked segments into 1D segments and add them to get watermarked audio signal.

3.2 Watermark Extraction

The watermarked audio signal may have gone through attacks and that is why watermarked audio and attacked watermarked audio (available for extraction) might be different from each other. Following steps are followed during the watermark extraction process:

1. Read the attacked watermarked audio signal and convert each 225 samples into 2D matrix (as done in Sect. 3.1 with original audio signal)
2. Calculate "norm" of each matrix segment using Eq. (2).
3. Use Eq. (8) to extract the binary watermark (W_{ext}) bit from each matrix segment.

$$W_{\text{ext}}(\text{segment}) = \text{mod}\left(\left\lfloor \frac{\text{norm}}{\mu} + \frac{1}{2}, \right\rfloor 2\right) \tag{8}$$

4. Convert the extracted 1D watermark bits into 2D in order to obtain extracted watermark image.

3.3 Finding of the Optimal Quantization Factor Using ANN

On the basis of experimental analysis and on the basis of past research works [11, 12], it can be inferred that higher quantization factor leads to low imperceptibility and high robustness. On the other hand, lower quantization factor leads to high imperceptibility and low robustness. As both the parameters, imperceptibility, and robustness are inversely related to each other, there is a need to find the optimal value of quantization factor for each audio signal.

A single optimal value cannot be used for different audio signal as used in Ref. [18]. The reason of the same is that every audio signal contains different type of components in it. Singular values are quite robust in nature, and therefore, they are likely to have a strong connection with audio signals.

With reference to above discussion, an ANN has been prepared that tries to map the relation between singular values and quantization factor. A total of 100 audio signals are used to generate the singular values, and iterative method is used to generate the best quantization factor for each audio signal. In iterative method, one needs to check performance of scheme over range on different quantization factors. A range of 0.1–1 is used for testing on the basis of previous literature [18]. An objective function (Eq. 9) is created to evaluate the performance.

$$\text{Objective function} = \text{imperceptibility} + \frac{\sum_{i=1}^{n}(\text{robustenss})_i}{\text{number of attacks } (n)} \tag{9}$$

Here, imperceptibility is defined as correlation between watermarked and original host audio. Robustness is defined as correlation between original watermark and

extracted watermark. If "n" numbers of attacks are considered, then average robustness is calculated as sum of all robustness divided by number of attacks (as shown in Eq. 9). The mathematical formula of correlation is shown in Eq. (10).

$$\text{Correlation}(X,\ Y) = \frac{\sum_{i=1}^{\text{length}} \left(X_i - \overline{X}\right)\left(Y_i - \overline{Y}\right)}{\sqrt{\sum_{i=1}^{\text{length}} (X_i - \overline{X})^2 \sum_{i=1}^{\text{length}} (X_i - \overline{X})^2}} \tag{10}$$

A correlation value of one signifies that the signals are exactly similar to each other, whereas value of zero signifies they are not at all same.

In addition, bit error rate (BER) is also used to check the performance of scheme in the presence of attacks. The BER is defined by Eq. (11)

$$\text{BER} = \frac{\text{no of incorrect bits}}{\text{total bits}} \times 100 \tag{11}$$

4 Results and Discussion

The simulation was done on MATLAB with a computer having a Core-i5 processor and 32 GB of RAM. All the audio signals used in this study were sampled at 44.1 kHz, 16-bit depth, and .wav files. The audio signals have been taken from Refs. [19, 20]. The host was resized to 230,400 samples before the watermark insertion process. The watermark of size 32×32 was used during the embedding. The watermark used for embedding was of binary nature, taken from Ref. [21]. A total of 225 samples of host have been taken in one segment and used for the insertion of 1 bit of watermark. The watermark along with an audio host is shown in Fig. 1.

Six attacks were considered in this work on the watermarked audio signal. The same is describing in Table 1.

Tables 2, 3, and 4 show the imperceptibility, robustness (average), and objective

Fig. 1 **a** Sample audio signal and **b** watermark

Table 1 Attacks names and descriptions

Attack name	Attack description
A-1	Resample to 22.05 kHz and again to 44.1 kHz
A-2	Butterworth filter with cut off frequency (fc) = 11.025
A-3	Additive white Gaussian noise (AWGN) addition 10 dB
A-4	8 bit quantization of audio signal
A-5	OGG based 75% audio compression
A-6	OGG based 50% audio compression

Table 2 Variation of imperceptibility (I), average robustness (R), and objective function (O) with respect to quantization factor (Q) of audio sample-1

I	0.995	**0.983**	0.969	0.928	0.868	0.815	0.766	0.736	0.705	0.645
R	0.853	**0.996**	0.989	0.945	1	1	1	1	1	1
O	1.849	**1.979**	1.958	1.873	1.868	1.815	1.766	1.736	1.705	1.645
Q	0.1	**0.2**	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0

Table 3 Variation of imperceptibility (I), average robustness (R), and objective function (O) with respect to quantization factor (Q) of audio sample-2

I	0.999	0.997	0.993	**0.988**	0.981	0.976	0.966	0.957	0.945	0.933
R	0.679	0.853	0.945	**0.991**	0.992	0.977	0.969	0.957	0.947	0.936
O	1.679	1.850	1.939	**1.980**	1.974	1.953	1.935	1.915	1.892	1.870
Q	0.1	0.2	0.3	**0.4**	0.5	0.6	0.7	0.8	0.9	1.0

Table 4 Variation of imperceptibility (I), average robustness (R), and objective function (O) with respect to quantization factor (Q) of audio sample-3

I	0.999	0.997	0.993	0.986	**0.978**	0.968	0.959	0.949	0.938	0.927
R	0.633	0.826	0.889	0.922	**0.937**	0.926	0.916	0.908	0.905	0.950
O	1.632	1.823	1.882	1.908	**1.915**	1.895	1.875	1.858	1.844	1.877
Q	0.1	0.2	0.3	0.4	**0.5**	0.6	0.7	0.8	0.9	1.0

function variation of three different audio signals with respect to different quantization factors. It can be clearly seen from Tables 2, 3, and 4 that the maximum objective function values are achieved on different quantization factor value for different audio signals. This concludes that the use of same quantization factor for every audio signal's watermarking is not a wise choice because it will result into either poor imperceptibility or robustness. So there is a need to find optimal quantization factor, which can maximize both; imperceptibility as well as robustness.

The iterative method can give the value of optimal quantization factor but takes a good amount of time to find the same. So an ANN approach has been develop, which can find the optimal value in quite lesser time.

4.1 ANN Approach to Obtain the Optimal Quantization Factor

Randomly, 140 samples are selected from the dataset [19, 20] and further divided into 100 training and 40 testing samples. A training dataset has been prepared with the help of 100 training samples in following manner (one after another):

1. Audio signal is fed to the embedding function (as explained in Sect. 3.1), and watermarked signal is obtained
2. Imperceptibility is calculated (as explained in Sect. 3.3)
3. Watermarked audio signals are attacked (simultaneously), and six attacked audio signals are generated
4. Six watermarks are extracted from six attacked sample (as explained in Sect. 3.2)
5. Average robustness is calculated (as explained in Sect. 3.3)
6. Objective function is calculated (as explained in Sect. 3.3)
7. Step 1–6 are repeated for quantization factor value of 0.1–1 with an increment of 0.1
8. Best scaling factor (single value) that gives maximum value of objective function and audio signal's norms (1024 values, as explained in Sect. 3.1) are stored as training dataset.

At the end of above-mentioned iterative procedure, input matrix of 100×1024 and output matrix of 100×1 is obtained, which is used to train the ANN shown in Fig. 2.

After the training, 40 new audio signals are also prepared via iterative method. The norms of these 40 audio signals are also fed to the trained ANN for prediction. Both outputs (predicted by ANN and obtained by iterative method) are compared for difference. The mean difference for 40 predictions turn out to be only 0.0583, which is a quite low value. It signifies that ANN can predict the optimal quantization factor with quite a good accuracy.

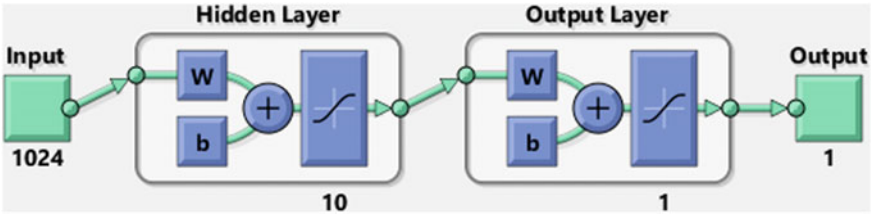

Fig. 2 Designed ANN architecture

Table 5 Run time comparison of proposed ANN method with iterative method

Run time (iterative method) in seconds	Run time (ANN method) in seconds
20.601	0.327

The importance of ANN use over iterative method can also be understood by the reduction in the run time (on same computer) to generate optimal value for one audio signal. The same is shown in Table 5. Clearly, ANN is around 60 times faster than iterative method.

The feature comparison between Bhat et al. [18] and proposed work is given in Table 6 to justify the importance of proposed work.

Table 7 shows the results obtained after the ANN based optimization for two test

Table 6 Feature comparison with Bhat et al. [18]

Features	Bhat et al. [18]	Proposed
Embedding method	Mean quantization of singular value norms	Optimal mean quantization of singular value norms
Selection of quantization factor (μ)	Manual	Automatic (by ANN)
Data payload (bps)	196	196
Inclusion of imperceptibility and robustness variation with μ	No	Yes

Table 7 Extracted watermark from attacked audio signal after ANN based optimization

Attack	AS-1 (imperceptibility = 0.9895)	AS-2 (imperceptibility = 0.9819)
	Extracted watermark Robustness (Correlation, BER)	Extracted watermark Robustness (Correlation, BER)
A-1	 (1, 0)	 (0.9886, 0.3906)
A-2	 (1, 0)	 (0.9971, 0.0977)
A-3	 (0.922, 2.6367)	 (0.9943, 0.1953)
A-4	 (1, 0)	 (1, 0)
A-5	 (1, 0)	 (1, 0)
A-6	 (0.9971, 0.0977)	 (1, 0)

audio signals (AS-1, AS-2). The watermark is able to sustain even A-3 attack, which is quite strong in nature.

5 Conclusion

An optimal mean quantization audio watermarking scheme was developed in this work that used ANN for the optimal quantization factor calculation. The scheme used norm of singular values for watermark insertion due to its robust nature toward attacks. ANN based quantization factor predictor has been designed to get an optimal trade-off between imperceptibility and robustness. This insured faster (around 60 times) result and provided best possible trade-off between imperceptibility and robustness for tested audio hosts. In future, more attacks will be incorporated to make the scheme even more effective. The attacks intensity can be made strong to check the limitations of scheme. Further, optimal segmentation length will be investigated to increase the payload without increasing the sampling frequency of audio signals. ANN based quality assured audio watermarking will also be investigated in future.

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Design, Optimization, and Critical Analysis of Hybrid Frequency Selective Surface in the Range of 1–18 GHz

Sunil Jorwal, Varun Chaudhary, Ravi Yadav, and Ravi Panwar

1 Introduction

Frequency selective surfaces (FSSs) are found important in a vast number of applications due to their filtering characteristics [1]. FSS is generally a two-dimensional periodic resonator patch and a metal plane separated by a dielectric substrate. Some basic periodic resonators used are rectangular, square, circular, polygon shaped structures because of their capability to generate a magnetic response in the microwave frequency range [2–4]. Recently, to meet the demand of multiband, the possibility of proposing the fractal FSSs attracted a lot of attention.

The polarization state is one of the strongest and essential characteristics of electromagnetic (EM) waves [5]. The polarization state of wave propagation can be controlled in various telecommunication applications such as remote sensing and fiber-optic communication [6]. Currently, Faraday rotation, Brewster angle effect, and birefringent crystals such classic approaches are widely applied in polarization control [7]. Unfortunately, in some cases, the methods of controlling polarization are suffered from heavy and bulky structures. To mitigate such problems, several designs have been proposed in recent decades.

The term fractal involves similar patterns reoccurring progressively at smaller scales, and the term fractal was first coined by Mandelbrot [8]. The fractals have the unique characteristics of self-similarity, and space-filling in their geometrical structures that result in multiband resonating frequencies [5]. The fractal shapes can be developed using the iterative transformational methodology, which includes scaling, copying, and translation of the geometry. Researchers have proposed a few widely reported geometries, i.e., Sierpinski gasket, Sierpinski triangle, and Minkowski fractal loop, etc., for various EM applications [9].

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Khosronejad et al. proposed transpolarizing structures of two linearly polarized converters which are having the cascaded connection of the unit cells. The polarization converters were rotated by 90° polarization from the normal direction of polarization. Jhiang et al. have proposed multiband absorber based on fractal circular structure exhibits three resonating peaks at 2.1, 4.3, and 11.8 GHz with absorptivity of 98, 99, and 99.5%. The Sierpinski nanocarpet operated in a wide wavelength range from 400 to 700 nm and polarization-insensitive in the range of incident angles (0–90°) [10]. The broadband perfect polarization convertor of the asymmetric double split-ring resonator has a polarization conversion ratio of 99% with the fractional bandwidth of 35% [11]. Amiri et al. have proposed fractal metamaterial absorber of $20 \times 20 \times 1.7$ mm^3 exhibited absorption ratio over 90% at 2, 5, and 12.5 GHz with the bandwidth of 0.85 GHz, 1.0 GHz, and 0.9 GHz, respectively.

In this paper, the Minkowski (MSK) loop fractal which is having simple iterative methodology has been modified to create a wideband polarization convertor. The proposed FSS achieves multiband resonant frequency and broadband polarization. Furthermore, a detailed analysis of polarization conversion of the structure has been demonstrated, and calculation of the polarization conversion ratio (PCR) with co-and cross-polarization reflections has also been done. To understand the physical mechanism behind the broadband conversion efficiency, the surface current distributions are illustrated at all three resonant frequencies. The constitutive electromagnetic properties of the structure are retrieved to understand the metamaterial behavior of the proposed FSS.

2 Design and Analysis of the Structure

The Minkowski loop fractal inspired hybrid FSS geometry has been obtained after a self-similar structure repetitive growing procedure, which is shown in Fig. 1. The front view of the proposed unit cell is illustrated in Fig. 1a, in which a new kind of hybrid fractal FSS geometry with Jerusalem cross and H-shape geometry has impinged over a 2.0-mm thick FR-4 substrate (relative dielectric constant $\varepsilon_r = 4.4$ and loss tangent of 0.02). The proposed FSS is backed with a perfect electric conductor (PEC). The PEC and substrate are separated by an air gap ($\varepsilon_r = 1$) of 2.0 mm as shown in Fig. 1b. FSS is made up of copper strips having the conductivity of 5.8×10^7 S/m, and a thickness of 0.035 mm. The structure is designed using a simulation software named as computer simulation technology (CST), microwave studio. The incident wave propagates in the z-direction and the periodic boundary conditions are used along the x and y-axis. The parametric optimization of the proposed geometry has been performed using CST microwave studio. The periodicity (a) of the proposed unit cell is 13 mm and other optimal geometrical design variables are illustrated in Table 1.

Figure 2 shows the reflection coefficient spectra versus frequency under the normal incidence in the frequency range of 1–18 GHz. The reflection spectra clearly show three peaks at discrete bands, located at 3.9 GHz (S-band), 9.9 GHz (X-band),

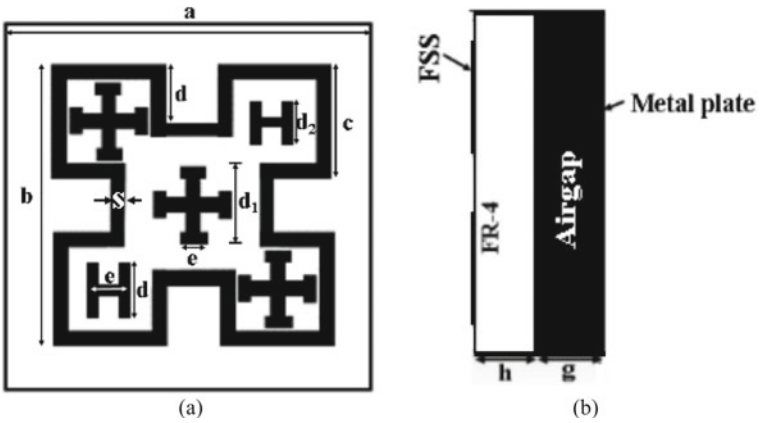

Fig. 1 **a** Front view of proposed FSS unit cell and **b** side view of the polarization converter structure

Table 1 Optimized geometrical design variables of the proposed FSS configuration

Parameter	Value (mm)	Parameter	Value (mm)
S	0.5	d1	3
a	13	d2	1.5
b	10	e	1
c	4	g	2
d	2	h	2

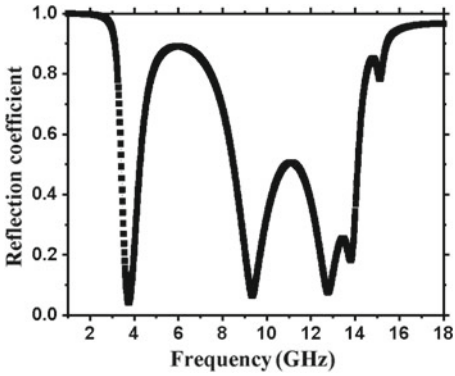

Fig. 2 Reflection coefficient of the proposed FSS in the range of 1–18 GHz

and 13.3 GHz (Ku-band), having reflection coefficient of −28.4, −24.1, and −22.4 dB with −10 dB bandwidth of 0.6 GHz, 1.1 GHz, and 1.8 GHz, respectively. To verify conversion properties, full-wave simulation is carried out with CST microwave Studio. The cross-polarization and co-polarization are defined as $R_{xy} = \left|E_{xr}/E_{yi}\right|$

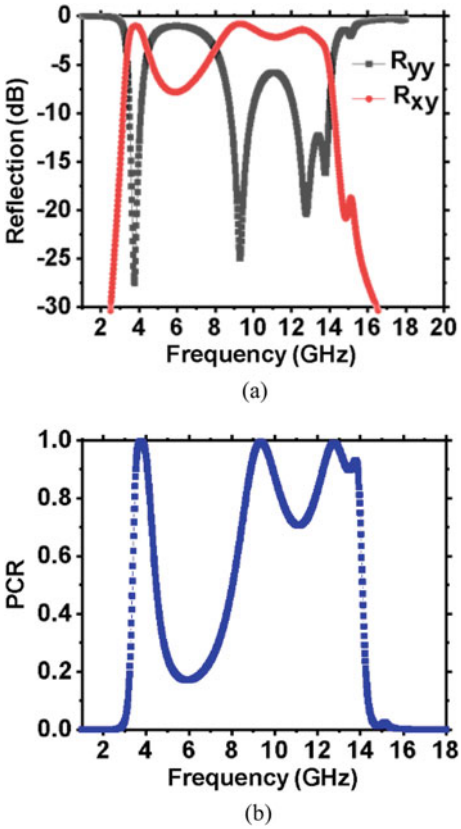

Fig. 3 Simulated **a** co-and cross-polarization reflection and **b** Polarization conversion ratio in the frequency range of 1–18 GHz

and $R_{yy} = \left|E_{yr}/E_{yi}\right|$ for y-polarized incidence wave [12]. Furthermore, the polarization conversion ratio (PCR) is defined as PCR $= \left|R_{xy}\right|^2/\left(\left|R_{xy}\right|^2 + \left|R_{yy}\right|^2\right)$ [12]. Figure 3 shows the graphical representation of simulated reflection spectra and PCR versus frequency. As shown in Fig. 3a, the cross-polarization reflection (R_{xy}) nearby approaches to −2.0 dB at 3.9 GHz, 9.9 GHz and 13.3 GHz, while the co-polarization reflection (R_{yy}) is reduced to more than 20 dB, respectively. Therefore, the value of PCR is more than 99% at all three resonating frequencies, as depicted in Fig. 3b. The above result shows that a perfect polarization rotation of almost 90° is attained in the defined frequency range for both x and y-polarized incident electromagnetic waves.

According to the theory of impedance matching, the normalized wave impedance of a fractal FSS can be modified to match the free space impedance. The normalized wave impedance can be calculated as [13]:

$$Z(\omega) = \sqrt{\frac{(1 + S_{11}(\omega))^2 - S_{11}^2(\omega)}{(1 + S_{11}(\omega))^2 - S_{11}^2(\omega)}} \tag{1}$$

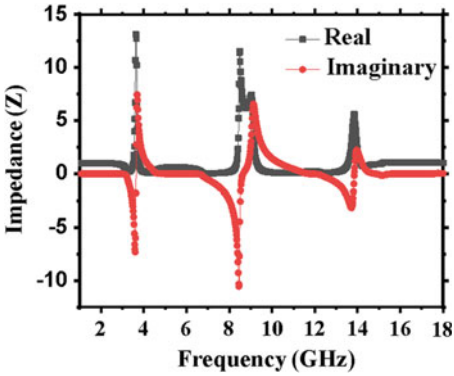

Fig. 4 Real and imaginary normalized input impedance (Z) in the range of 1–18 GHz

Figure 4 represents the normalized impedance of the optimized structure versus frequency demonstrating three resonance frequencies of 3.8, 10.4, and 16.1 GHz. To comprehend the physical nature of the structure, effective parameters are extracted. The electromagnetic structure parameters, i.e., effective dielectric permittivity (ε_{eff}) and effective magnetic permeability (μ_{eff}) in the range of 1–18 GHz are illustrated in Fig. 5a, b. The real part of effective permittivity at three resonance frequencies is very high which results in strong electric resonance as shown in Fig. 5a, and the real part of the effective permeability at resonance frequencies (3.9, 9.9, and 13.3 GHz) is 13.4, 12.1, and 6.7 which depict the strong magnetic resonance at all three reflection peaks. The electromagnetic properties have been extracted out with the help of full-wave simulation.

To better understand the physics of three resonant frequencies, the surface current distribution has been monitored. The surface current distribution at three resonant frequencies is shown in Fig. 6. As we can see, the high currents are concentrated on the outer ring of Minkowski (MSK) fractal and a small amount of current flows through the inner part of MSK fractal loop shown in Fig. 6a. The direction of current along the outer MSK loop on the top layer is opposite to that in the inside part of the MSK loop, which can be examined as the magnetic dipole resonances. Figure 6b, c have similar electric dipoles that are excited on the inner layer and highly concentrated at the outer layer. In Fig. 6c, the surface current indicating the focus on the outer part of MSK fractal loop as well as the high current is distributed on Jerusalem cross and H-shaped FSS as compare to lower resonance frequencies. From these figures, we examine that the lower polarization conversion band is mostly attributed to the fundamentals. Whereas the higher frequency band has been formed by the fundamental and multi resonances excited on inner and outer MSK fractal loop structure.

Table 2 provides a relative analysis of the proposed structure with other open literature approaches with no. of bands, thickness, and polarization conversion ratio. In comparison, it has been evident that the PCR of the proposed structure is defined as greater than 99% in the given reflection spectra. From Table 2, it is to be noted that

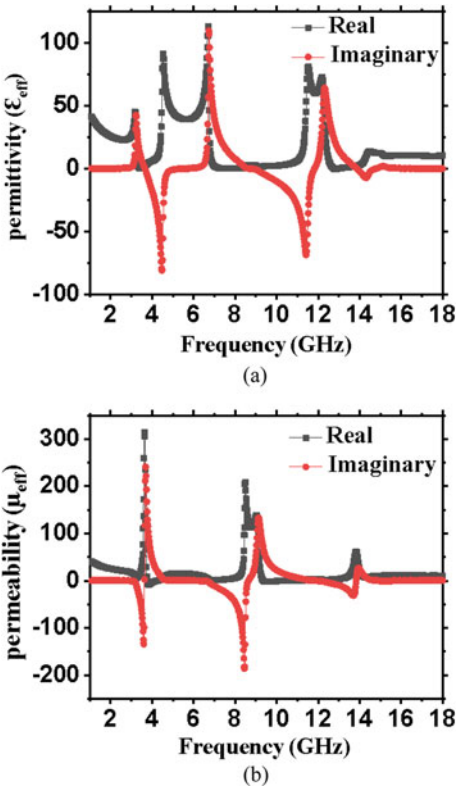

Fig. 5 Extracted electromagnetic properties **a** effective permittivity (ε_{eff}) **b** permeability (μ_{eff})

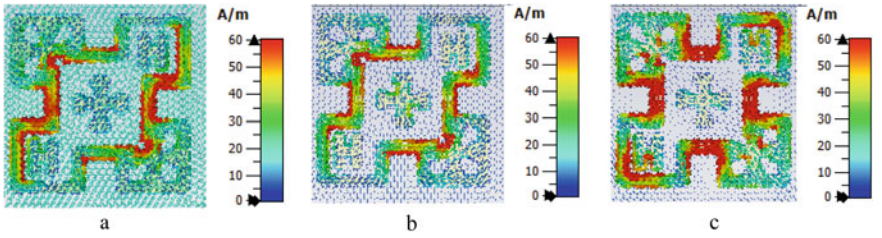

Fig. 6 Surface current distribution at **a** 3.9 GHz, **b** 9.9 GHz, and **c** 13.3 GHz

the proposed structure provides the maximum PCR with three different resonating bands, while comparing to other relevant reported work.

Table 2 Comparative analysis of proposed and other reported works

References	FSS shape	Thickness (mm)	Number of bands	PCR (%)
[14]	Strip-loaded half elliptical rings	1.5	1	98
[15]	Metal square rings	5.1	1	>88
[12]	Double arrow-shaped structure	2.1	1	>90
Proposed structure	Hybrid Minkowski fractal	2.0	3	>99

3 Conclusion

The hybrid fractal FSS is successfully designed and analyzed in the range of 1–18 GHz. The structure is composed of an asymmetric hybrid Minkowski unit cell coupled with Jerusalem cross and H-shaped geometry. The simulated result shows three resonance peaks at 3.9, 9.9, and 13.3 GHz, high-efficiency cross-polarization reflection, and very low-co-polarization reflection are achieved. A unique response with three resonating frequency is achieved below −10 dB in frequency bands at S, X, and Ku-bands. The electromagnetic properties have been extracted out with the help of full-wave simulations. Excellent broadband polarization conversion properties have been observed, and such polarization converter is of excellent applications in polarization-controlled devices.

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Analysis of Transient Fault Detection Models

T. Shunbaga Pradeepa and S. Uma Maheswari

1 Introduction

In today's fast-moving world, everyone expects everything to be working perfect. If any failure occurs, immediate alternative solution is the need or the failure should be intimated earlier to have precautions and safe everything. Mitra and McCluskey [1] analysed the concurrent error detection techniques by duplication and parity check and have simulated it for various bench mark circuits. Matakias et al. [2] soft and timing errors are detected in CMOS IC using sense amplifier circuit with the concept of pre-evaluation and detecting the error. The circuit proposed in [2] overcomes the duplication, triplication and provides a feasible solution to detect faults quickly. Ernst et al. [3] proposed a new model RAZOR for detection and correction of failures in digital circuits. Multiple fault detection is an important factor in evaluating faults in digital circuits. To handle multiple errors, a time dilation technique was discussed by Valadimas [4] which detects and corrects fault within one clock cycle. Quinn et al. [5] tested and proved that DWC techniques are robust to single-event upset and single-event transients especially in microcontrollers. Nicolaidis [6] discussed the various double sampling architectures and observed the error detection, failure prediction, power reduction and increase in speed. Thus, from the survey, it is observed that various fault detecting models are available and each have its own merits and demerits. Ahmady et al. [7] have introduced a new technique utilizing dynamic flip flop conversion along with dynamic clock to improve the performance with respect to critical paths. Choudhury et al. [8] described a technique to mask timing error using time borrowing. In [9], transient faults in flip flops and latches are monitored

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early using moving time window method. As early fault detection is of most urge few of the fault models are analysed in this paper. The paper is organized as follows. Section 1 introduction where the previous works are compared. In Sect. 2 the fault models are discussed. In Sect. 3 the results obtained along with the observations are discussed. Lastly, the conclusion is in Sect. 4.

2 Fault Detection Models

There are various fault detection models available as suggested by Camponogara Viera in [10]. In this section, fault models such as duplication with comparison (DWC), time redundancy (TR), RAZOR-II, Transition detector with time borrowing (TDTB), double sampling with time-borrowing (DSTB), transient fault monitoring scheme (TFMS) are discussed.

2.1 DWC

Figure 1 represents the duplication with comparison structure. It consists of 2 blocks, where one block is the actual and another block is the copy of the actual block. They are compared with a xor gate.

If both blocks maintain the same data, then it means that there is no error. If any one block is corrupted with any transient fault occurrence then it results in an error. This helps in identifying the fault. In this model, only faults can be detected.

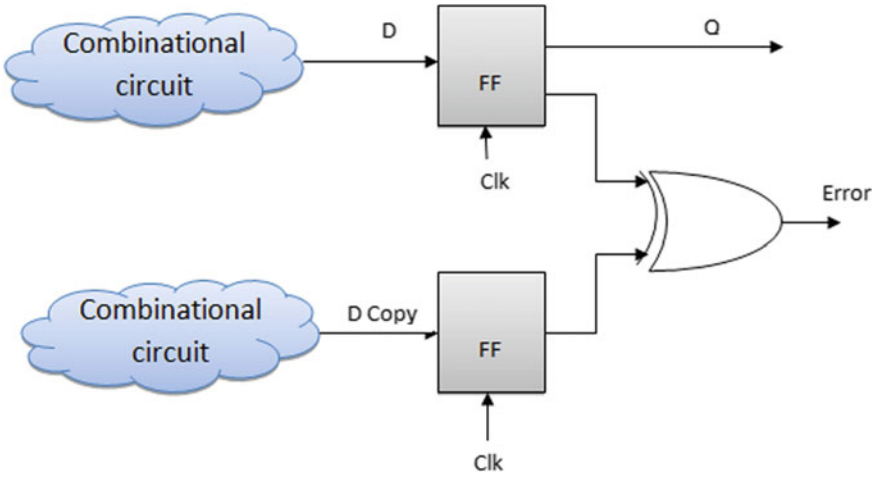

Fig. 1 Duplication with comparison structure

2.2 TR

Time redundancy model in Fig. 2 helps in detecting the transient faults. The actual circuit data is stored in the flip flop. The time delayed data is also stored in another flip flop. The same logic is computed in both the circuits but at two different times. Both the results are compared and if they are different then error is generated.

The clk signals are given such that same data is compared to find the error. If there is no change, then error signal is deactivated.

2.3 Razor-II

The Razor II model is shown in Fig. 3. In this model, the output of the circuit is stored in the latch. There is a transition detection module which helps in finding the transient fault. The role of pulsed clock generator is to generate a short pulse to disable the detector after rising edge for a short interval of time.

2.4 TDTB

The transition detector with time as in Fig. 4 is yet another model used to detect the transient fault. The model has two latches, one working with positive clock and other working in the negative clock. There is a transition detector which helps in detecting the transition of clock edges.

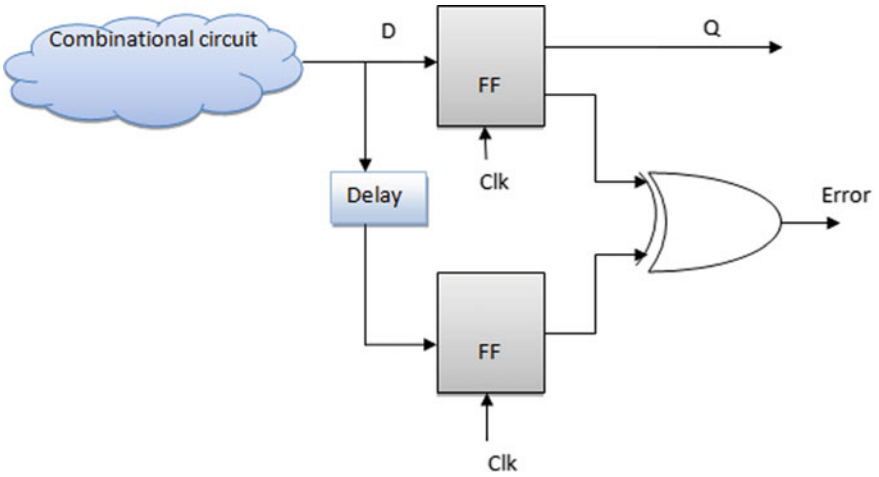

Fig. 2 Time redundancy model

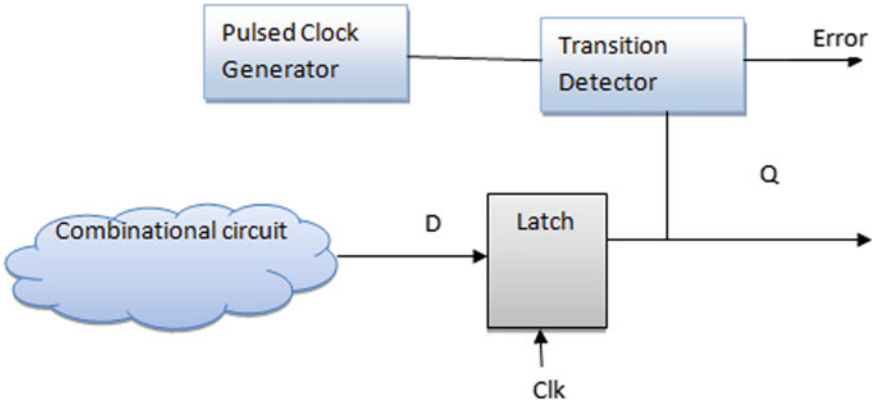

Fig. 3 Razor II model

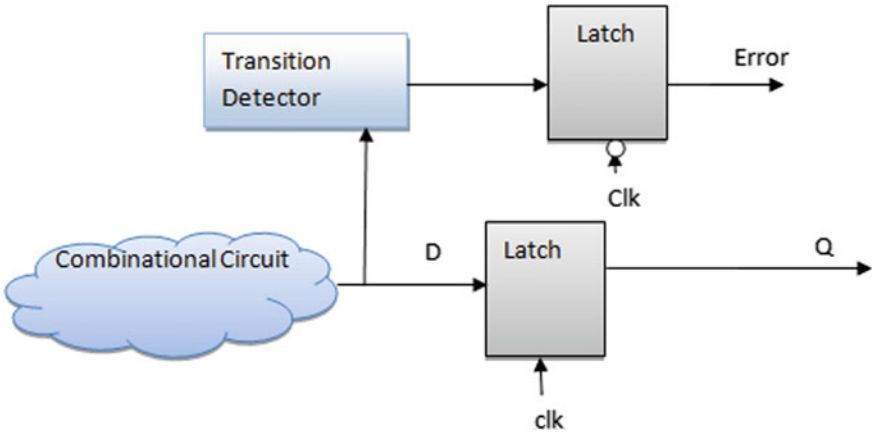

Fig. 4 Transition detector with time borrowing model

2.5 DSTB

Figure 5 which is as like RAZOR II has a latch and a flip flop. The outputs are connected to a xor gate. The signal has to be stable before the logic low of the clk because the error signal is generated during the low state of clk.

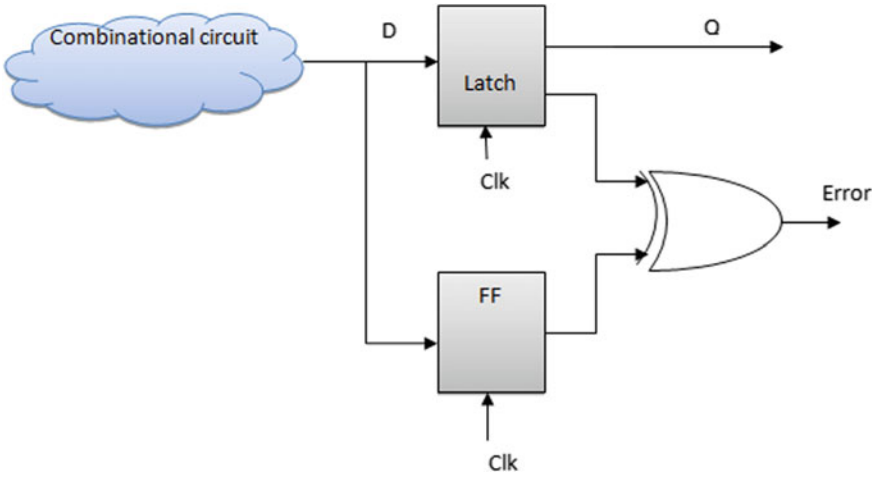

Fig. 5 Double sampling with time-borrowing model

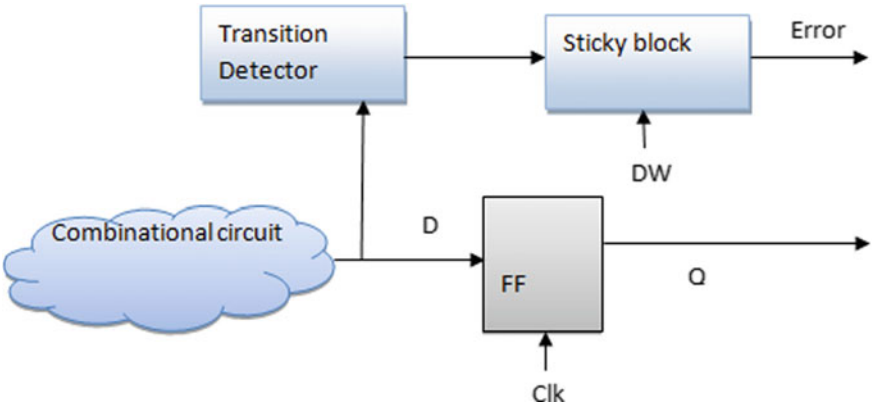

Fig. 6 Transient fault monitoring scheme model

2.6 TFMS

TFMS in Fig. 6 has a transition detector detecting the transition faults. There is another block called sticky block which helps to check whether the fault is within the scanning window or not. Based on that the error signal will be generated.

3 Results and Discussion

All the circuits were designed and simulated using the Microwind tool using the 45 nm technology file. Figure 7 represents the duplication with comparison circuit diagram with possible input combinations. There are 2 cases.

Case 1: No fault injection,
Case 2: Transient Fault injection.

In case 1, the actual input and duplicate input will be the same, where no error is detected. In case 2, transient faults are injected and as a result input and it's duplicate are different, so error is detected.

Figure 8 represents the fault detection of DWC. It is observed from figure that multiple transient faults are injected and errors are detected and few errors are missed. It is observed that this circuit has missed detection of transient fault for fault width less than or equal to Tclk/2, where Tclk is the input clock period. The power consumed is also observed.

Figure 9 shows the time redundancy circuit and its fault detection. Similar to the above circuit, both cases are simulated and results are observed. It is found that in this circuit also transient fault error detection were missed. The power seems to be less when compared to the earlier circuit.

Razor II circuit is shown in Fig. 10 and its simulated results are shown in Fig. 11. Similar to the above circuit, both cases are simulated and results are observed. It is found that in this circuit all the injected transient faults were detected as error without missing. The power seems to be reduced when compared to the other circuits.

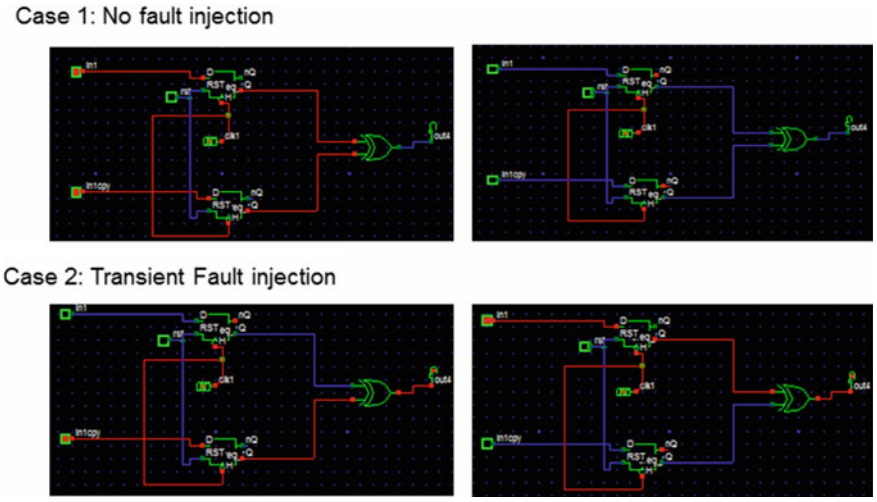

Fig. 7 Duplication with comparison circuit diagram

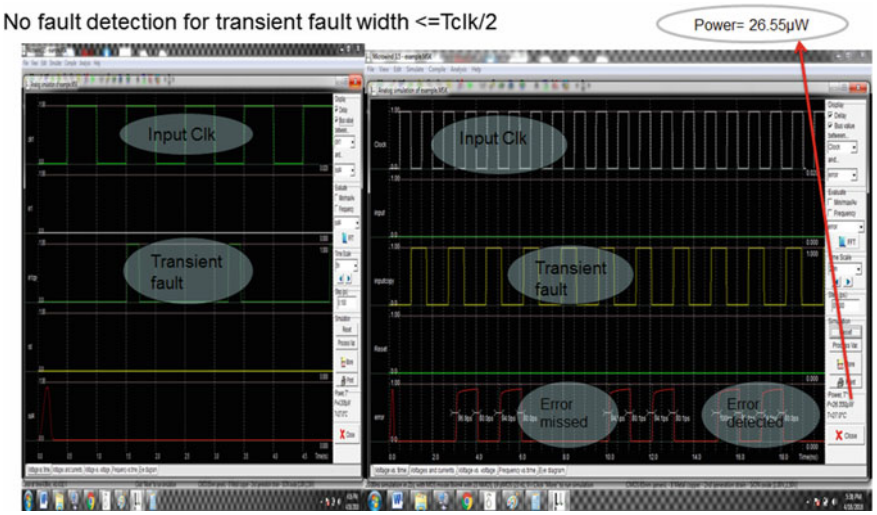

Fig. 8 Fault detection of DWC

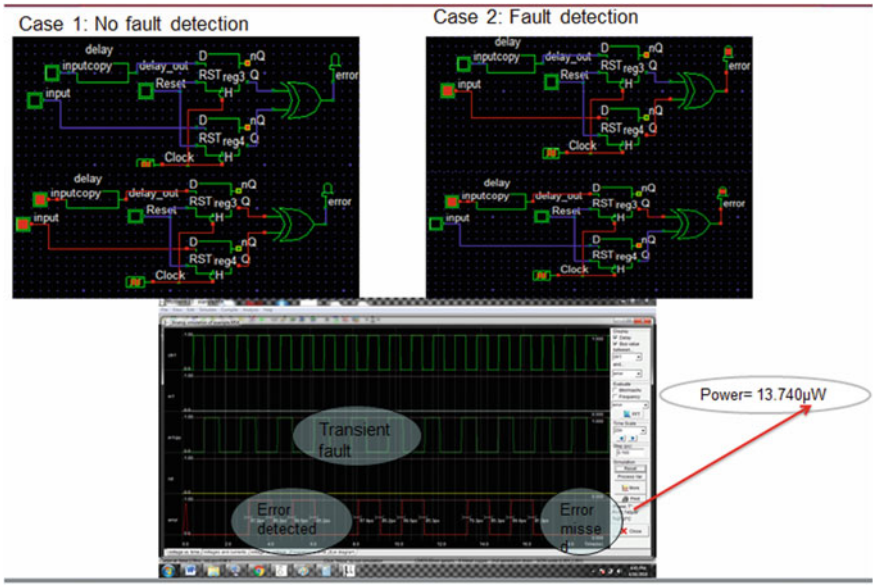

Fig. 9 Time redundancy circuit and fault detection

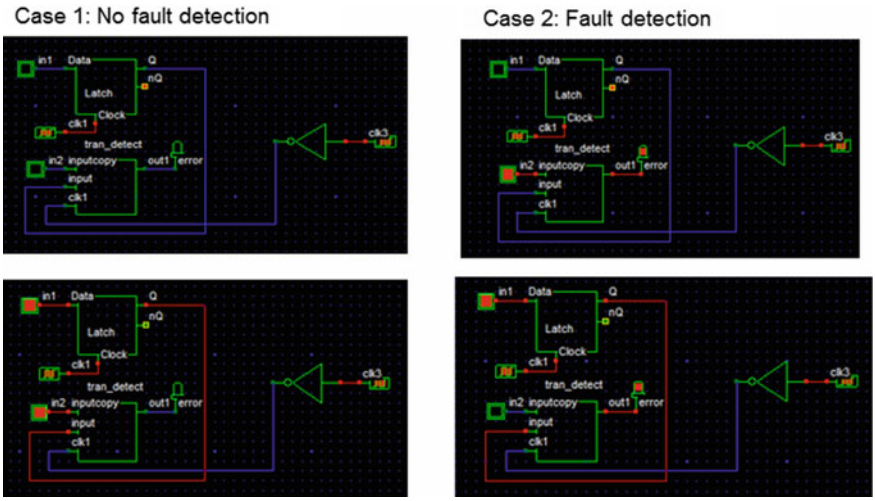

Fig. 10 Razor II circuit diagram

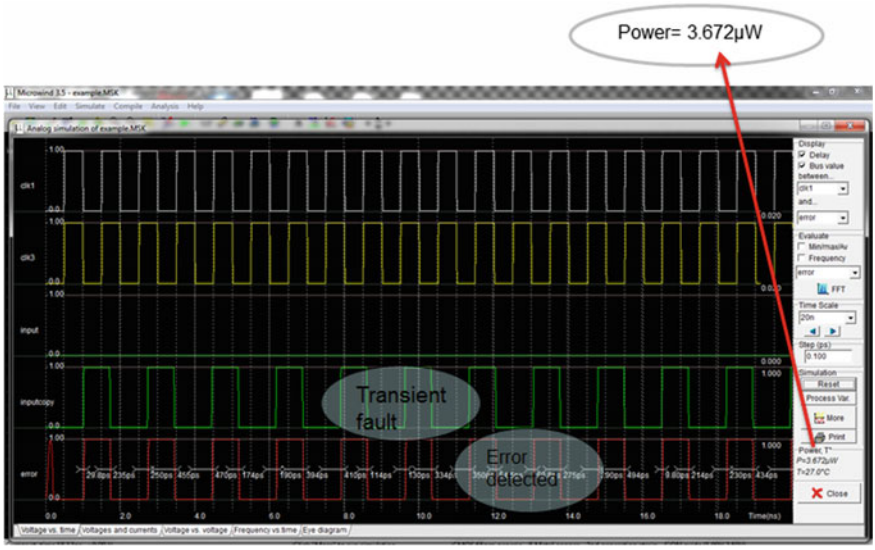

Fig. 11 Razor II output

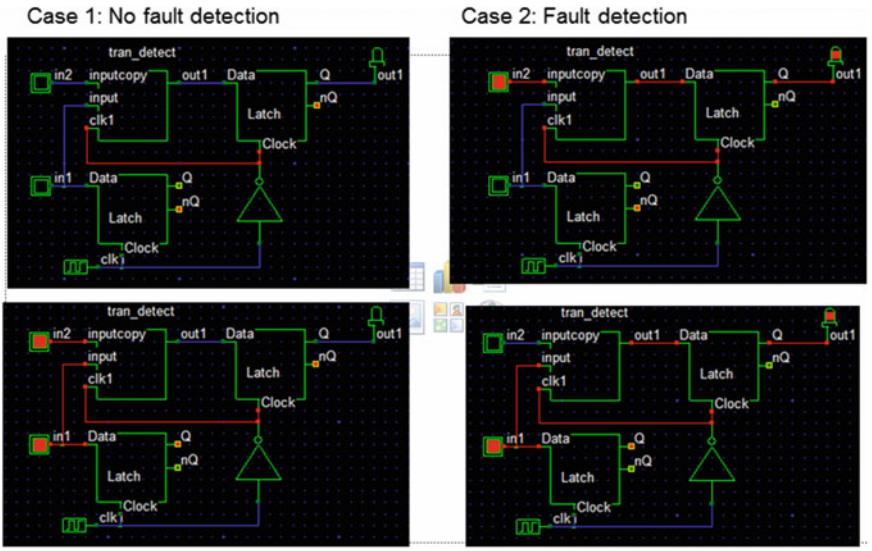

Fig. 12 Transition detector with time borrowing circuit

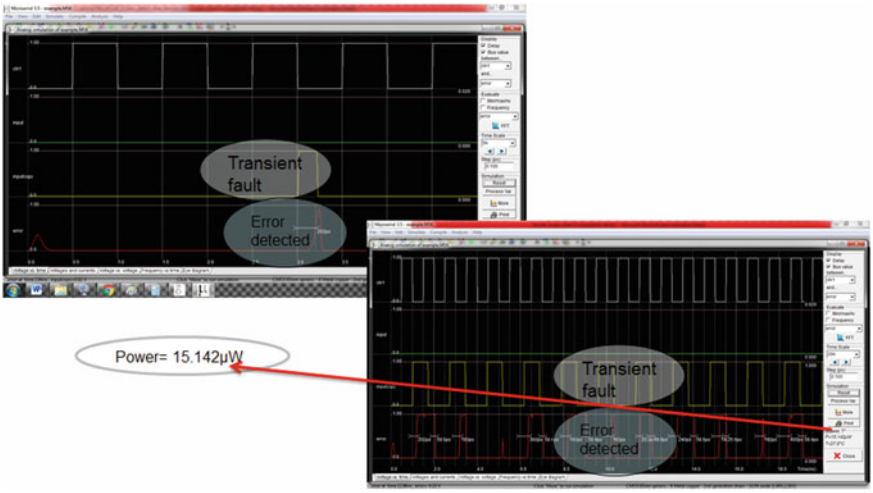

Fig. 13 Transition detector with time borrowing output

Transition detector with time borrowing is the circuit shown in Fig. 12 and its simulation result is shown in Fig. 13. In this circuit, the injected faults were detected but very few error were missed. The power is quite less compared to time redundancy circuit.

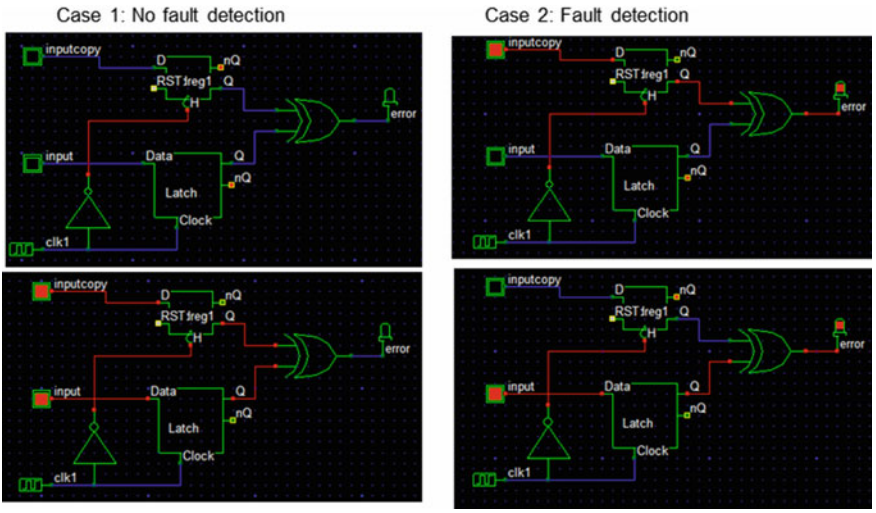

Fig. 14 Double sampling with time borrowing circuit diagram

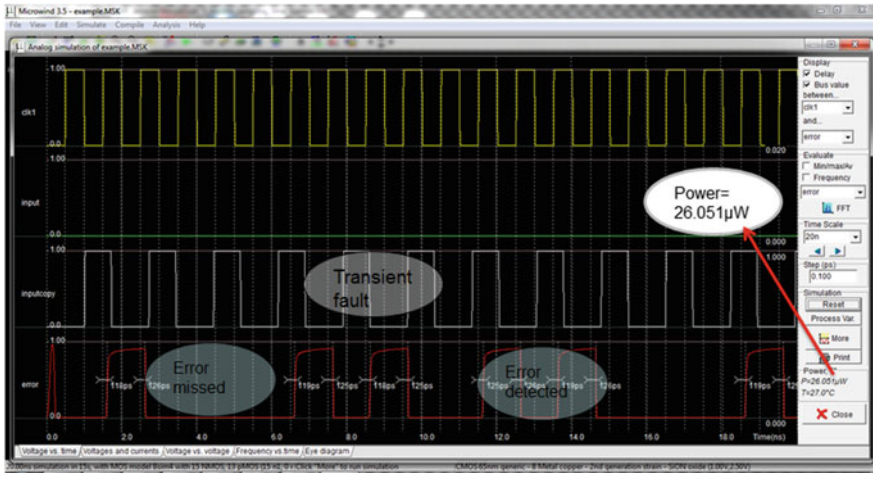

Fig. 15 Double sampling with time borrowing output

Figure 14 represents the double sampling with time borrowing circuit and its simulation result is shown in Fig. 15. In this circuit, the injected faults were detected and few errors were missed. The power is quite moderate.

Figure 16 represents the transient fault monitoring scheme circuit. Its simulation result is shown in Fig. 17. Similar to Razor II circuit, this circuit detected all injected faults as errors. The accuracy is good, but the power consumption is very high compared to other circuits.

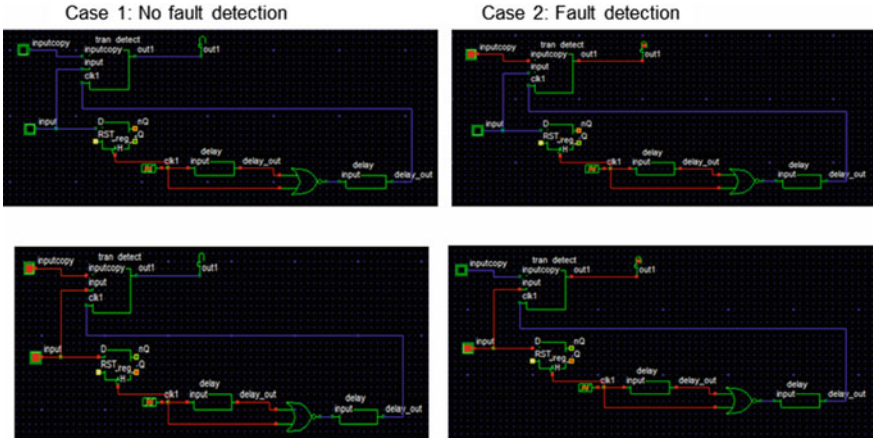

Fig. 16 Transient fault monitoring scheme circuit

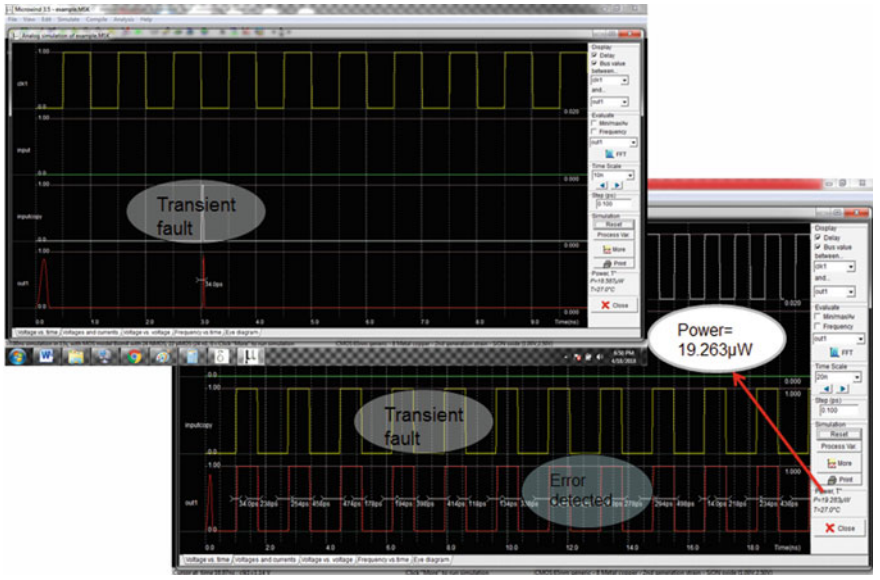

Fig. 17 Transient fault monitoring scheme output

The circuits were simulated with various scenarios like change in transient pulse width, amplitude, and time period. The scenarios are selected with 2 different pulse widths namely w1 ns and w2 ns, 2 different amplitudes v1 volt and v2 volt. Scenario 1 has been tested with fault width of w1 ns and amplitude of v1 volt. The scenario 2 has the same fault width w1 ns as like scenario 1 but with different amplitude of v2 volt. Scenario 3 is tested with fault width w2 ns and amplitude as like that of

Table 1 Summary of power

S. No.	Fault model	Power (uW)			
		Scenario1	Scenario2	Scenario3	Scenario4
1	DWC	11.74	40.97	12.73	26.55
2	TR	13.74	33.84	29.26	23.28
3	RAZOR II	1.23	30.289	3.672	28.582
4	TDTB	15.142	40.501	12.436	40.317
5	DSTB	10.963	35.582	32.211	26.051
6	TFMS	6.984	46.589	19.263	44.831

Table 2 Summary of efficiency

S. No.	Fault model	Efficiency (%)			
		Scenario1	Scenario2	Scenario3	Scenario4
1	DWC	55	73	75	100
2	TR	55	73	88	100
3	RAZOR II	100	100	100	100
4	TDTB	82	82	100	100
5	DSTB	55	73	88	100
6	TFMS	100	100	100	100

scenario 2 which is v2 volt. The last scenario 4 is tested with w2 ns pulse width and amplitude of v1 volt.

The summary of power under various scenarios are tabulated in Table 1. The power is expressed in uw (micro Watt). The efficiency based on the detection of faults are summarized in Table 2.

Figure 18 summarizes the power analysis of all circuits under 4 scenarios. It is found that the 1st, 2nd, 3rd scenarios the Razor II circuits have low-power consumption, whereas for 4th scenario time redundancy circuit has less power.

The efficiency produced in detecting the transient fault errors are summarized in Fig. 19. From this, it is observed that Razor II and transient fault monitoring scheme (TFMS) has detected all the faults in all scenarios. The other circuits have detected all the faults in 4th scenario, whereas they have missed few faults in 1st, 2nd, 3rd scenarios. TR and DSTB have the same efficiency in all the scenarios.

4 Conclusion

This paper discussed on the various fault models such as DWC, TR, RAZOR-II, TDTB, DSTB, TFMS. The transient fault of different amplitude, frequency, duty cycle was injected into all the circuits. The fault detection, correction of errors, was

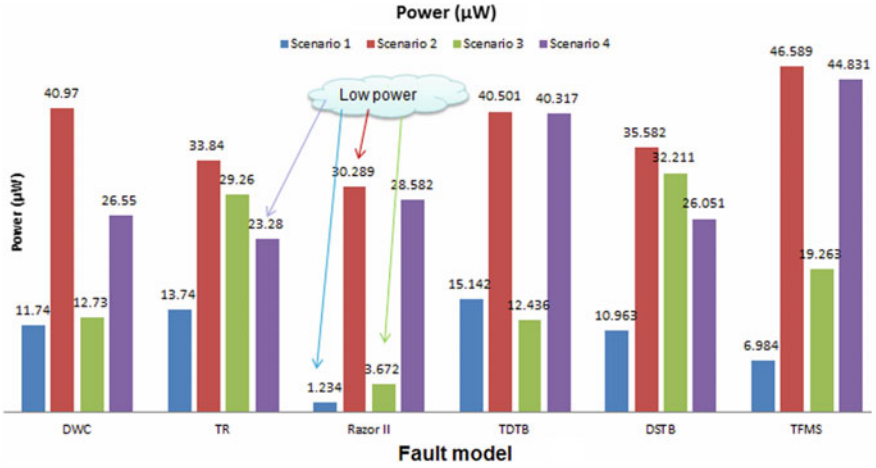

Fig. 18 Power analysis

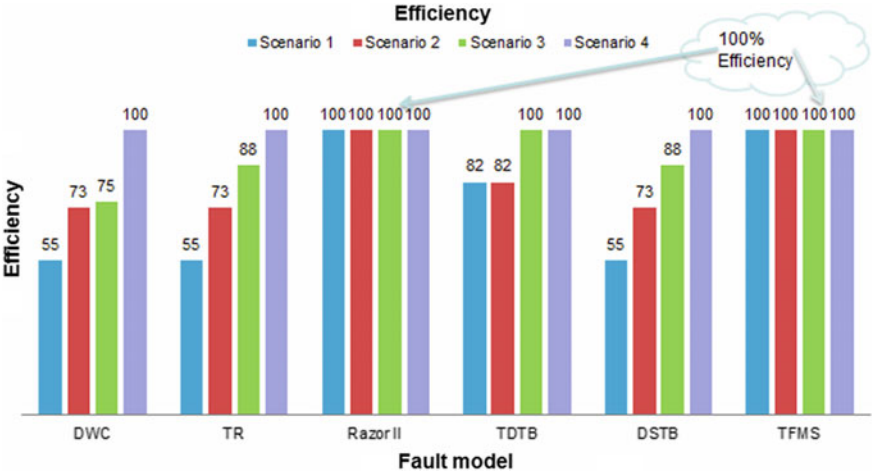

Fig. 19 Efficiency analysis

observed. It is observed that transient fault detection is accurate in RAZOR II and TFMS models, whereas RAZOR II model consumes less power. Thus, this model can be employed in any fault detection at faster time with better efficiency consuming less power. This work can be extended by increasing the test scenarios and including the correction mechanism using suitable correcting circuits.

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Deep Learning-Based Modulation Classification of Communication Signals

Vaibhav Tiwari, Girish Chandra Tripathi, and Meenakshi Rawat

1 Introduction

Deep learning has found its applicability in the industrial and research domain due to its enormous capabilities [1]. Moreover, to solve the fundamental problem of communication that is the reproduction of message signals approximately or precisely at the receiver using machine learning does not achieve much success due to the limitation in the processing capability of the available devices. Now the availability of highly efficient Field-programmable gate arrays (FPGAs), Graphics processing unit (GPU), and other RF components has enabled us with the freedom to push the limits of data processing which has allowed to replace traditional modulation identification techniques. The modulation classification [2] is a massive challenge in the military and civilian applications for interceptive threat analysis and aversion, interference management, and spectrum management. Moreover, the motive of this approach should be to identify friend and foe signals in the real-time basis to classify them and take appropriate actions; therefore, such scenario requires a complex and robust algorithm which is at the same time compact and adaptive, to be able to quickly adapt to myriad systems and find real-time applications. More precisely, in a highly congested spectrum of radio waves, to carefully know about the RF signatures and better understand the RF spectrum utilization and security threat detection, is what has been accomplished herein.

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Lecture Notes in Electrical Engineering 777,
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An artificial intelligence-based modulation classification system for a particular scenario consists of three steps; the first one is obtaining/synthesizing the dataset as simulative as possible to the application environments. The second step is signal preprocessing or data engineering [3]. Finally, the third step involves classification algorithms. Data engineering contains tasks like recognition of various data components and tweaking them, i.e., modifying the parameters to obtain maximum distinction between them depending upon the method that is been applied, thus maximum accuracy. In the third step, an artificial neural network (ANN) is applied [4]. The classification of the modulated signals has been investigated in [5–10]. This paper provides significant insights and improvements on the existing literature on modulation classification with changes in the dataset manipulation techniques. We have used the results obtained in [11] as a baseline, which has been vastly improved over here. This paper is organized as follows: Sect. 2 describes the data preprocessing technique used to process the data before applying it. Section 3 presents the deep neural network architecture and its improvement. The results are shown in Sect. 4. The conclusion is presented in Sect. 5.

2 Data Preprocessing

Data preprocessing is an essential step since the collected data may have odd data combinations, missing values, etc. Such data may cause problems and confusing results. Therefore, the interpretation and quality of data are first and foremost before running any analysis. Firstly, a synthetic dataset, obtained [11] with GNU Radio, consists of eleven modulations with variable SNRs. The dataset has moderate local oscillator drift, weak fading, and several SNR increments. Every sample is presented using two vectors; each of them has 128 elements. We identify the raw features and make a battery of more features such as that concatenates the essential features that are as follows.

1. Raw time series as given (two channels)
2. First derivative in time (two channels)
3. Integral in time (two channels)
4. Combinations of 1, 2, and 3 (more channels).

This dataset consists of radio signals modulated using different modulation techniques and different signal-to-noise ratios. The dataset has been divided into labels and signal vectors. Signal vectors have 162,060 pairs of arrays with 128 values, each signifying in-phase (I) and quadrature (Q) signals in time series format. Thus, the resulting dimension of the signal vectors or input to the neural network is (162,060, 2128). The labels are then encoded in binary form using one-hot encoding. The signal vectors are kept in four forms, namely raw data, Fourier transform, integral, and derivatives per channel, as shown in Fig. 1. We have attempted different neural network architectures to classify the signals based on the modulation technique that is used. The performance of the networks has been compared across signal-to-noise

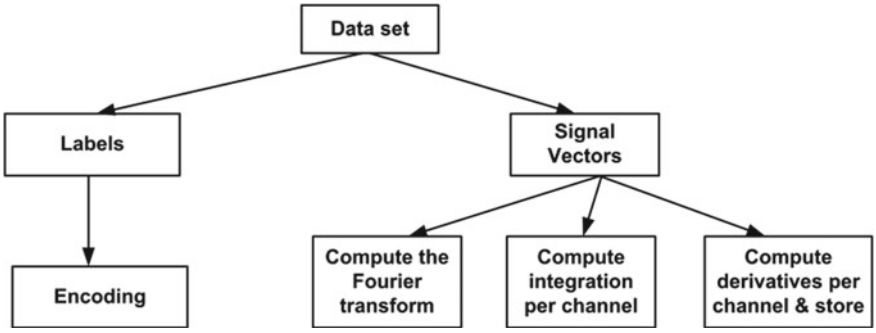

Fig. 1 Data preprocessing

ratios ranging from −20 to +18 dB. The negative signal-to-noise ratios signify that the original signal is still identifiable, even with such high noise, and thus opens quite a possibility to reduce noise since it can be traced, but that is beyond the scope here.

3 Deep Neural Network Architectures

Deep neural networks are fundamentally a collection of weights and biases that add up and decide whether or not the neuron must be triggered via an activation function. Every layer is a linearly functioning system, triggered by a nonlinear (not essentially but in our case) function, which makes the whole system highly nonlinear. We investigated the performance of three different types of neural network architectures for the modulation classification problem.

3.1 Convolutional Neural Network (ConvNet/CNN)

A convolutional neural network (ConvNet/CNN) is a deep learning architecture which takes input in more than one dimension, and assigns learnable weights and biases to various aspects/objects in the data. Thus, it can differentiate between multiple aspects/objects and consequently differentiate between classes of input. The preprocessing required in a ConvNet is much lower as compared to other classification algorithms. In contrast, earlier, methods filtered data aspects manually. With enough training, ConvNets can learn these filters/characteristics. We have treated the input with dimensions, 2×128. The architecture is shown in Fig. 2. Being a convolution-based network, it can deal with all dimensions; thus, the input is reshaped to $1 \times 2 \times 128$ and convolved $64 \times 2 \times 128$, and then batch normalization (BN) is carried out by keeping the dimensions intact. Afterward, we have used a convolution, and BN is layered; hence, there is no change in dimensions of the parameters.

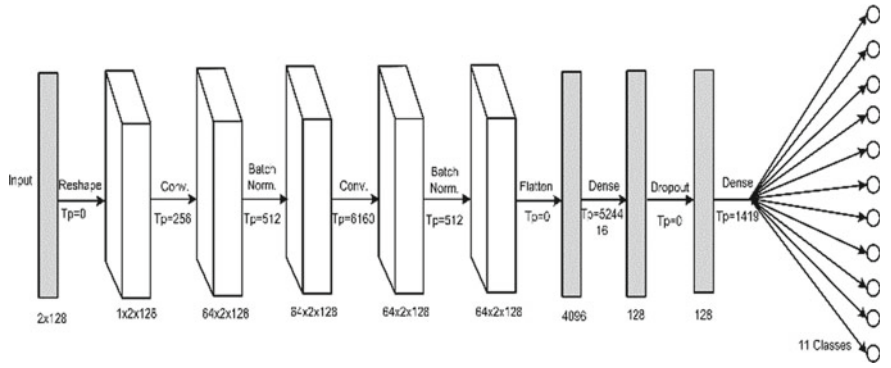

Fig. 2 CNN architecture for modulation classification

A flattening layer is then applied with zero training parameters (tp), and thus after flattening, the dimensions become 4096 ($64 \times 2 \times 128$); then, to reduce the dimensions of the output further, a dense layer is applied, and the dimensions of the output become 128. To avoid over-fitting, dropout is applied, and finally, a dense layer is applied to get eleven classes. The training and testing accuracy of CNN is depicted in Fig. 3. The final training and validation accuracies of ConvNet are 60.35% and 60.46%, respectively, at ten epochs.

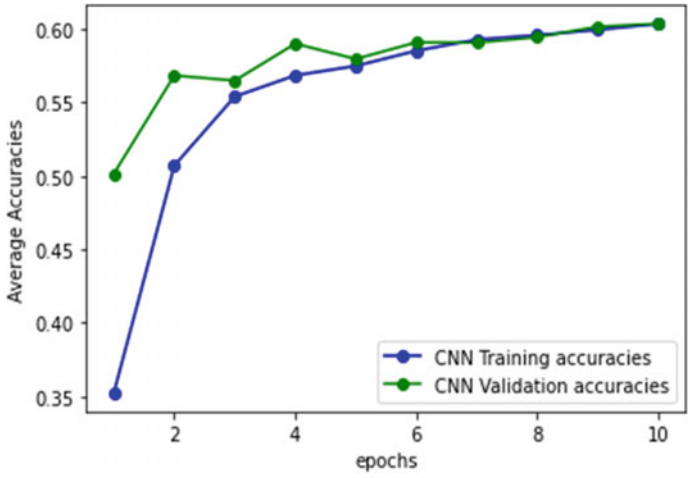

Fig. 3 CNN validation and training accuracy

3.2 *Fully Connected Neural Network (FCNN)*

The second architecture using a fully connected neural network (FCNN) architecture has been proposed. Figure 4 shows FCNN architecture where all the layers are fully connected, as the name suggests. Since the input data to the network was two-dimensional, a flatten layer is applied to reduce it to one dimension as we cannot process two dimensions without convolutional layers. Then, the parameters are reduced successively by two densing layers from 256 to 128 to 64 parameters, respectively. Then, we have used BN that is subtracting the mean from each observation and dividing by the square root of variance. The BN has the advantage since it decreases the internal covariate shift. Afterward, a dense layer is used to reduce the parameters to 32. To avoid over-fitting or to overtrain, the dropout layer is applied. Now since the classification has to be done in eleven classes, one denser layer is applied to reduce thirty-two parameters into eleven categories. Moreover, the training of DNN becomes complex since the distribution of each layer's inputs changes during the training process, and since parameters of the former layers modified. This reduces the training by needing lower learning rates and cautious parameter initialization, which makes it extremely difficult to train models with saturating nonlinearities. This phenomenon is known as internal covariate shift (ICS) [12]. This variation progresses to a constant shift in the fundamental training problem and is thus thought to have a negative effect on the training process. This problem can be addressed by normalizing the inputs to the layer. Moreover, the BN favors the reduction of ICS, and this is the prime advantage of BN. Figure 5 shows training and validation accuracies of the FCNN, where we can see the highest training accuracy is 64.2%, and validation accuracy is 63.06% at thirty epochs.

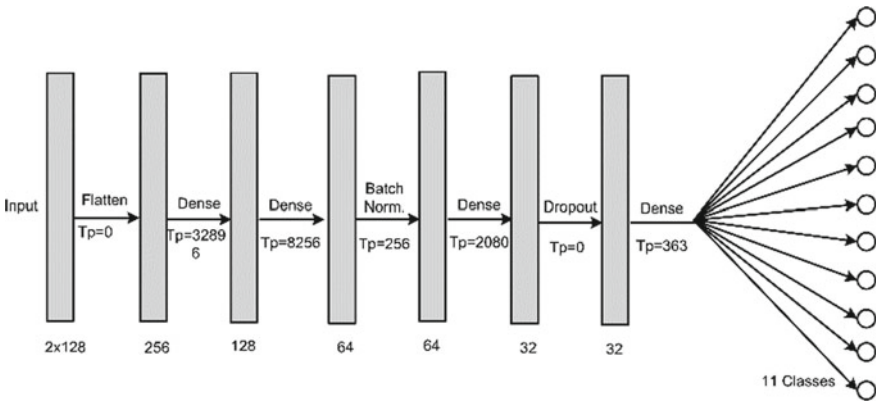

Fig. 4 Fully connected neural network architecture

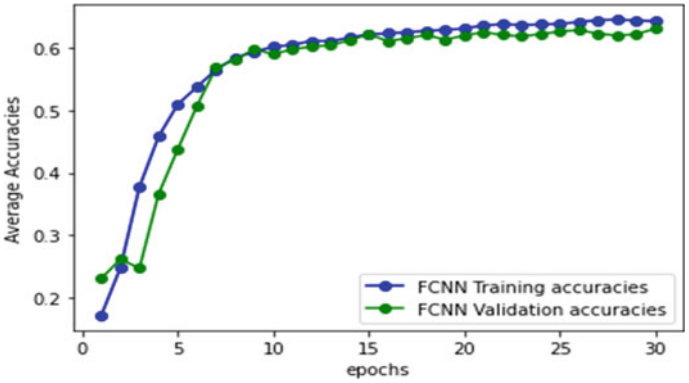

Fig. 5 FCNN validation and training accuracy

3.3 Inception Convolutional Neural Network (ICNN/IncNet)

Like CNN in the case of inception convolutional neural network (ICNN), the input with dimensions of 2×128 is reshaped to $1 \times 2 \times 128$. In parallel simultaneously, the reshaped input is passed to four ConvNets, and one Max pooling layer, the shape of all the four outputs, has dimensions $1 \times 2 \times 128$. All of the four outputs are convolved again to get four outputs, three of which are $1 \times 2 \times 64$, the other with the dimension of $1 \times 2 \times 128$, the three with $1 \times 2 \times 64$ dimensions came from previous convolutional layers, and the one shaped as $1 \times 2 \times 128$ came from the Max pooling layer. All of the four outputs of dimensions $1 \times 2 \times 128$ and $1 \times 2 \times 64$ are now normalized by BN layers. Therefore, the dimensions remain unchanged. All the four outputs from the BN layers are simply concatenated to yield an output of dimensions, $1 \times 2 \times 320$ [$1 \times 2 \times (128 + 3 * 64)$]. The flattened and dropout layers yield an output of 640 nodes. Then after four dense layers, the output nodes are obtained as 360, 120, and 84, respectively, and finally, eleven classes are required (Fig. 6). The validation and training accuracies are shown in Fig. 7. From Fig. 7, we can see that the validation and the training accuracies are 64.03% and 69.51%, respectively, at 16 epochs only. Since the ConvNets, when kept parallel with each other couple up, thus they become faster while maintaining the depth of the network at minimal, although the computational expense increases but the accuracy increases likewise [13].

4 Results

In this section, we have compared the classification accuracies with different NN architectures to find the best performance.

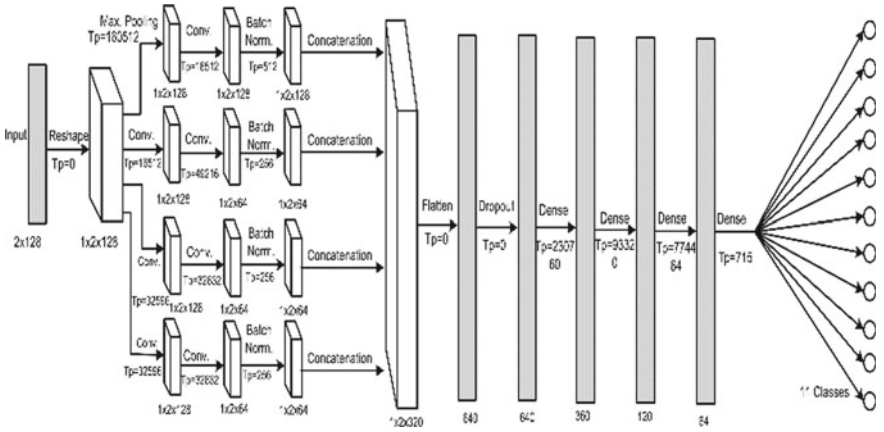

Fig. 6 Inception neural network architecture

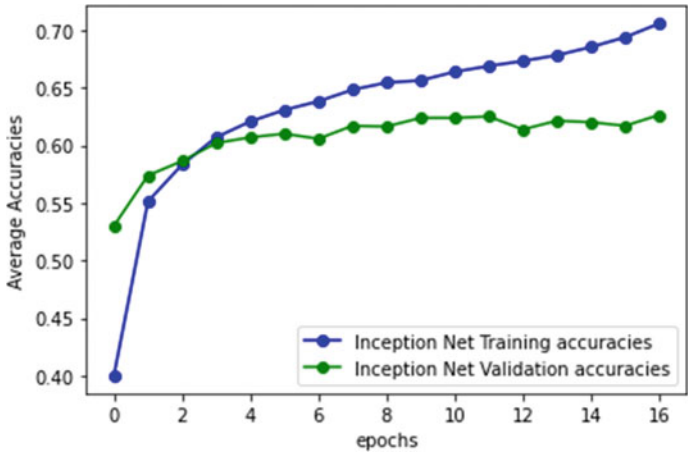

Fig. 7 ICNN training and validation accuracy

4.1 Fully Connected Layers

The confusion matrix summarizes the results for the fully connected network for the whole data, shown in Fig. 8, which shows that the networks confuse between 8PSK and QPSK because of the similarities they hold in the modulation type. The accuracy peaks around 90% for SNRs of −2 dB and above, which is considerably more accurate than [11], and the architecture we have used is much simpler as compared to the architectures used in [11]. Yet, as can be seen in Fig. 9, the accuracy has been improved**.** Along with the fully connected layer, we have also used residual net, convolutional long short-term deep neural network (CLDNN), inception layer

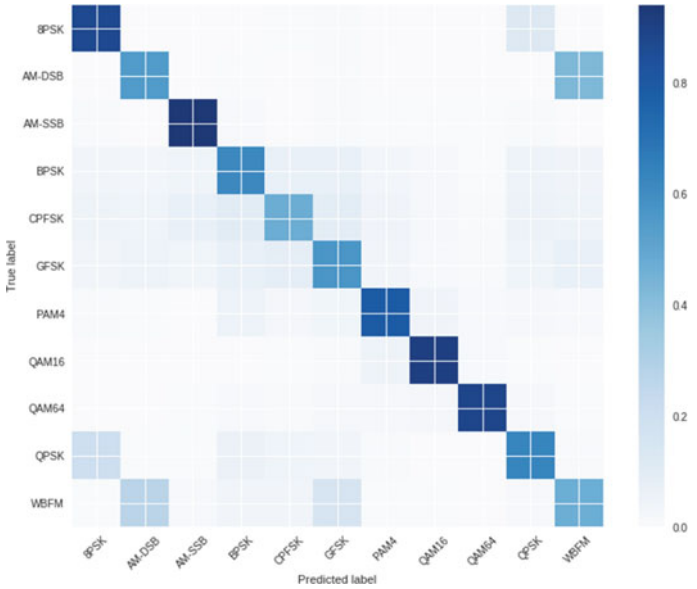

Fig. 8 FCNN classification confusion matrix

without batch normalization, and convolutional neural network (CNN-2) without batch normalization for comparison purposes. From Fig. 9, we can see that the accuracy of FCNN has been increasing with the increase in SNR.

4.2 Convolutional Neural Net with Batch Normalization

The results for the convolutional neural net has been summarized below and can be seen in the confusion matrix in Fig. 10. The confusion between QPSK and 8PSK is evident because of the similarities they hold in the modulation type. For comparison purposes along with the convolutional neural net with batch normalization layers, we have also used residual net, convolutional long short-term deep neural network (CLDNN), convolutional neural net without batch normalization, and another convolutional neural network with batch normalization. The comparison has been made in Fig. 11, which shows that using CNN with batch normalization increases the classification accuracy.

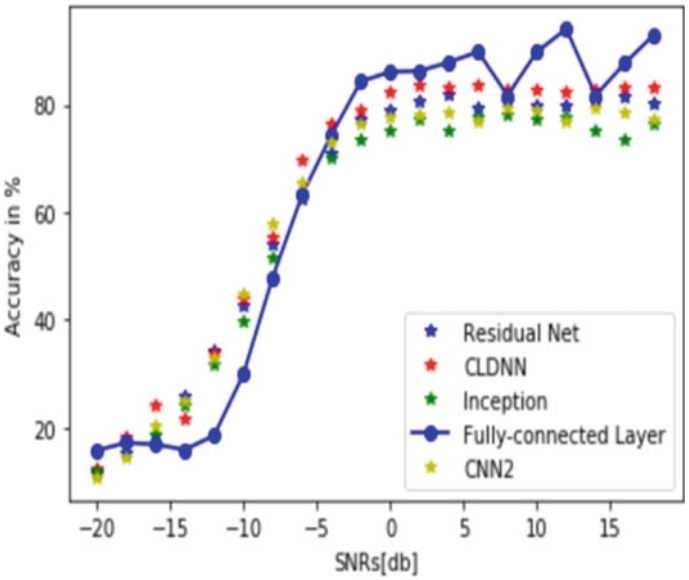

Fig. 9 FCNN classification results compared with other networks

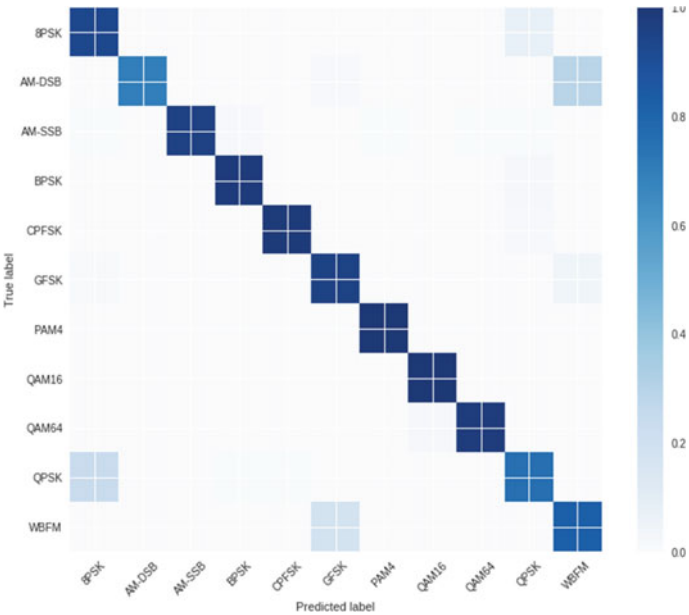

Fig. 10 CNN classification confusion matrix

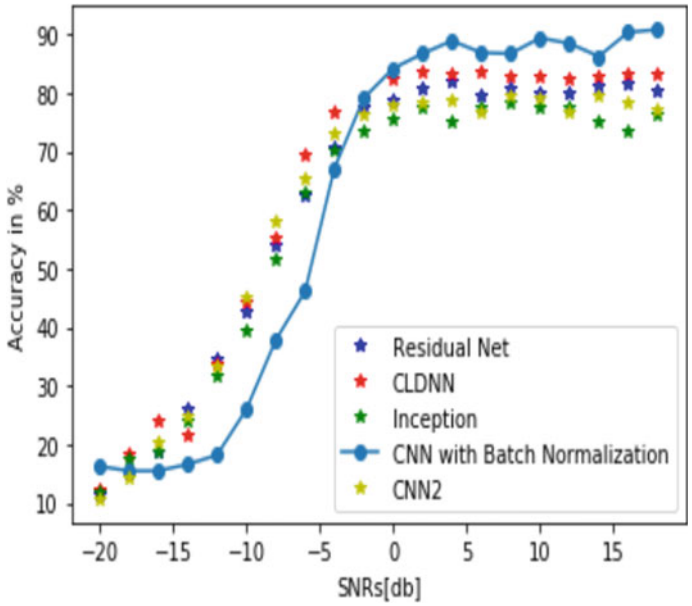

Fig. 11 CNN classification results compared with other networks

4.3 Inception Convolutional Neural Network

The confusion matrix obtained using the inception convolutional neural network is shown in Fig. 12. The confusion between the 8PSK and the QPSK is due to the similarity in the modulation format. For comparison purposes and the inception convolutional neural net with batch normalization layers, we have also used residual net, convolutional long short-term deep neural network (CLDNN), and convolutional neural net without batch normalization. The comparison has been given in Fig. 13.

Table 1 shows the average accuracies of the FCNN and ICNN, overall the SNR values. Table 1 shows that the inception model is marginally better than the FCNN for the raw data. Other than the raw data, various other concatenations between different data streams like Raw + FFT, Raw + Derivative + FFT have also been checked. The ICNN performs better than FCNN for raw data. Table 2 shows various accuracies at zero SNR using CNN and ICNN, and the ICNN shows an accuracy of 86.05% for raw data. Table 3 shows the best achievable accuracies by the two networks at positive SNRs.

Table 4 shows the comparison of the proposed method with other methods. As can be seen, the proposed method has more accuracy when compared to other methods.

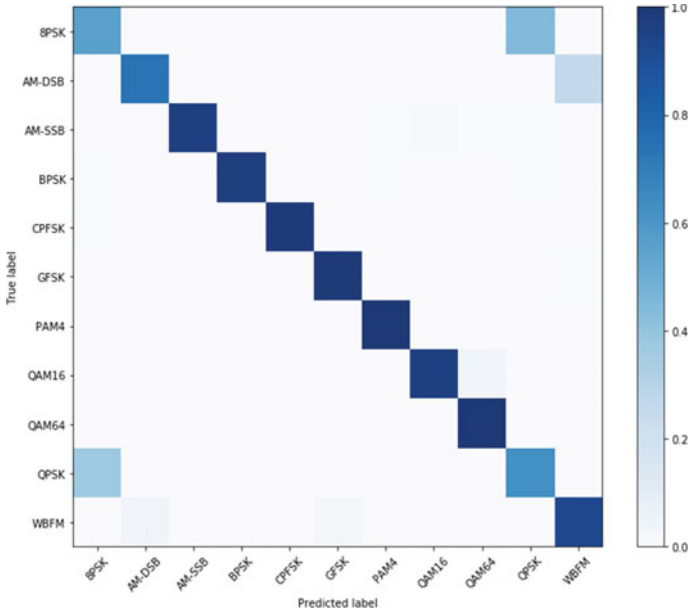

Fig. 12 ICNN classification confusion matrix

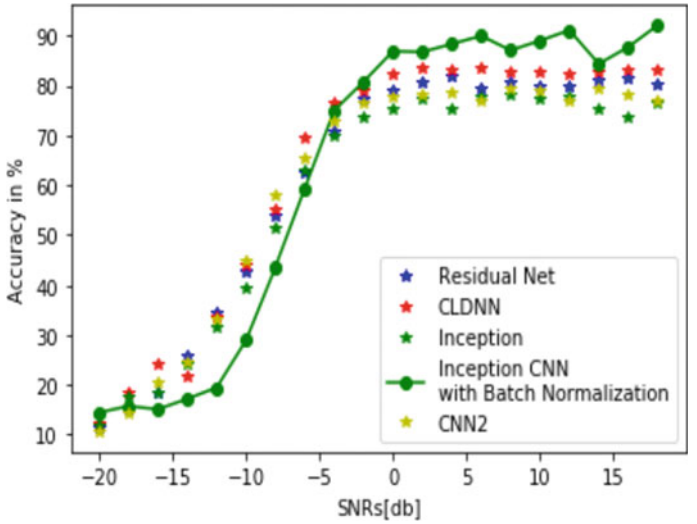

Fig. 13 ICNN classification results compared with other networks

Table 1 Average accuracies as compared between the fully connected and inception model

Features	Fully connected	Inception model with CNN
Raw data	61.68	62.10
Derivative	48.07	15.22
Raw and FFT	60.44	60.63
Raw, derivative, and FFT	58.49	61.24

Table 2 Accuracies as compared between the fully connected and inception model at zero SNR

Features	Fully connected	Inception model with CNN
Raw data	83.69	86.05
Derivative	63.43	15.62
Raw and FFT	81.49	83.28
Raw, derivative, and FFT	70.02	85.21

Table 3 Best accuracies as compared between the fully connected and inception model at positive SNRs

Features	Fully connected	Inception model with CNN
Raw data	93.57	93.10
Derivative	76.35	17.31
Raw and FFT	87.19	88.56
Raw, derivative, and FFT	82.04	92.19

Table 4 Comparison of accuracies with other methods

Work	Methods used	Best accuracy (%)
[14]	CNN-IQ, CNN-IQFOC, LSTM-IQ, and LSTM-IQFOC	~87
[15]	CLDNN and LSTM	92
This work	FCNN and ICNN	93.57

5 Conclusion

Based on the different classification schemes for the raw data, highest accuracy obtained for ICNN at various SNRs is 93.10%, and that obtained by the FCNN is 93.57%, whereas that obtained by the baseline model, i.e., the CNN, is comparatively low at just 60%. Using the radio classification method, we have demonstrated that it can effectively learn to classify modulation techniques using domain-specific trigger functions and layer configurations. BN significantly improves the classification accuracies. We require zero knowledge of the modulation technique for training the networks and identification of modulation schemes.

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Biomedical Watermaking Using Arnold Transformation

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1 Introduction

Digital technology has several advantages such as data copying and transmission without any information losses, etc. We can easily send and receive the message. In engineering, signal plays a very important role [9–11, 21]. Telemedicine is a combination of information technology and telecommunication. It is also used in the case of an emergency. Using this technique, information can be easily transferred, and it also allows communication between medical staffs and patient relatives. One of the main activities that medical image management involves is the exchange of data between two hospitals located at different places. And it demands high security and good quality of images after data transmission. Digital image watermarking is a way to secure medical images from data hiding and copying data. Watermarking techniques are used in biomedical IP protection [20] and software protection [13]. A watermark can contain some information. This information can be about the origin, status, or recipient [4, 6, 7, 14, 23]. Multi-resolution signal decomposition also used for watermarking of the digital images [8]. Discrete Wavelet Transform (DWT) and Singular Value Decomposition (SVD) are used for image watermarking [12]. Cao et al. [2] use the modern reversible data hiding for watermarking. Tsai et al. [24] use a new algorithm which utilizes the wavelet multi-resolution structure for the construction of the image frequency components. It is used to hide secret information in the form of binary data in the image signal that can be extracted later to prove the ownership, content authentication, copy control, transaction tracking and device control [16]. Measurement standards such as capacity, robustness, PSNR, RMSE and

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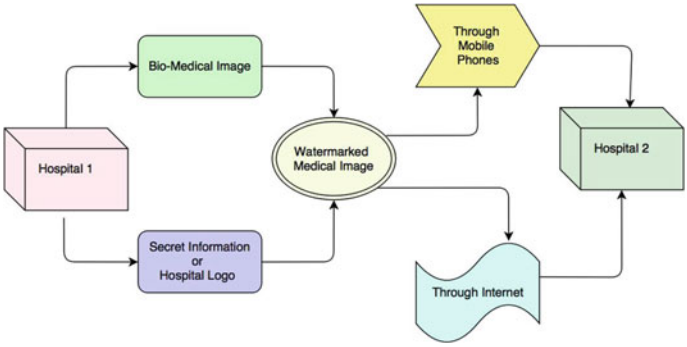

Fig. 1 Transmission of medical images between hospitals

blindness are used to test the effectiveness of the technique. There are two types of watermarking. It is as follows:

1. Visible watermarking
2. Invisible watermarking.

This technique can be applied on RGB images as well, for coloured images, we need to apply this technique separately on red, green and blue layer. In this technique, a host medical image is classified into sub-bands using Discrete Wavelet Transform, and then Arnold Transform is applied on watermark image. Here, Arnold Transform is applied to scramble the image.

In this paper, Sect. 2 demonstrates the challenges in the medical images. In Sect. 3, we have discussed the various kind of attacks. Section 4 describes the proposed method. We have discussed the pros and cons of our proposed technique in Sect. 5. Future work has been mentioned in Sect. 6 (Fig. 1).

2 Challenges in Medical Imaging

From last so many years, watermarking has given security many advantages in this era. Among the most important is the insertion of signature into the data. It is an essential aspect as security and authenticity are concerned. Modification of even a single pixel in the medical image may affect the overall information present in the image. So, it may influence the diagnosis, and consequently, this might threaten the health or even the life of the patient. Therefore, it is crucial to approach watermarking in the area of medical imaging quite distinctly compared to the other fields of interest. Watermarking of medical images [18] can boost security and authenticity, and it can enhance the everyday operation in medical practice [19].

- **Proof of Ownership and Identification** Watermarking is used to prove ownership. Hiding a security key or any pseudorandom number in the form of message

signal or image signal (that represent owner identification) in the original image using some transform technique such as DWT, DCT. Watermark embedding in the original image can change some bits of the original image but does not affect its applications because the watermark is embedded only in Region of Not Interest (RONI) [1, 15]. Watermarks are indistinguishable and inseparable from the information in which they are embedded.

- **Copy Control** When we publish any paper or any information on the Internet, we cannot have a relationship with every possible person who will view and read that information because the Internet is open for anyone. Due to modern digital technology, anyone can copy without any information loss.
- **Transacation Tracking** Digital technology gives many advantages; it provides the user to translate information in digital format. It is easy to replicate the digital information format without any information loss. To stop illegal use of this advantage, watermark (Secret Key) is embedded in original information. Watermarking gives the advantage to track its origin.

3 Categories of Attacks

Today, many types of attacks exist to affect the quality of the image and to track some critical information of the image. For this, they try to modify watermark or try to get the secret key so that authorized person cannot prove their ownership. This section includes the following attacks.

1. **Forgery Attacks** The main aim of this attack is to crack the security key in the watermarking scheme. After finding this key, they remove embedded watermark or embed any other watermark. This attack is also called as an unauthorized embedding or cryptographic attacks. In this attack, attackers try to modify the images by inserting new watermark. Copy attack is also an example of this attack. They intend to destroy the ownership information from the image.
2. **Geometrical Attack** In this attack, attackers try to manipulate the image in such a manner that an authorized person cannot detect the watermark. They aim to get information about the image. Some of the examples of geometrical attacks are rotation attack, cropping attack, shearing attack, etc. They try to shift image pixels, rotate the image by some degree, or scale image without any visual changes in images.
3. **Removal Attack** The main aim of this attack is to remove the watermark and crack some information about the image. This attack includes compression attack, mean filter, median filter, average filter, compression attack, collusion attack, etc. Their main aim is to remove the embedded watermark and to get valuable information from this image. This attack is so affecting, such that attackers are near to destroy the watermark from watermarked image.
4. **Passive Attack** This also one of the unauthorized attack. Attacker's main goal is to detect the embedded watermark that supposed to be recognized by only

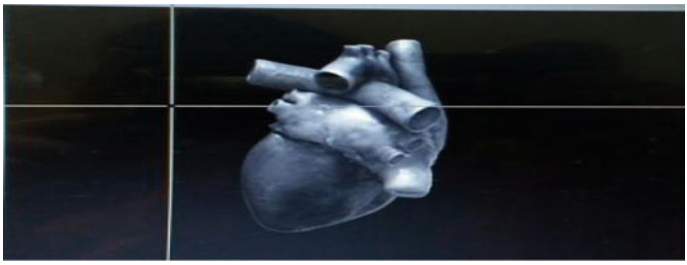

Fig. 2 Pick a point to select the ROI of a square shape. Size of ROI should be less than 1/4 of the original image

authorized personnel. Attackers may be interested in modifying the watermark or may not be.

5. **Noise Attack** This attack can be made using the MATLAB function. This includes Gaussian attack, blurred image attack, salt and pepper attack and contrast attack. Salt and pepper is a kind of attack in which as a noise white and black dots present in the image. Blurred image attack is implemented on the image to reduce the quality of the image. That can be done using many local factors. Contrast attack is kind of attack in which contrast of the image is changed to affect both watermark and original host image.

4 The Proposed Technique

In this section, the watermark embedding and watermark extraction method are discussed. Watermark is embedded as an image signal in the original image signal using Discrete Wavelet Transform and Arnold Transform. In this section, we will discuss how to select ROI for watermarking in medical images.

4.1 Selection of ROI

Watermark is not embedded in the whole image. A small region of an image is selected for watermarking. Biomedical images are so sensitive, and embedding in the entire image is not acceptable because the change in a single bit that carries information can occur a big problem in the diagnosis process. So, watermarking is done only in Region of Not Interest(RONI) that have no critical information. ROI and RONI can be selected based on size or intensity. But the selection of RONI is more complicated than ROI. Here, in this method, ROI is chosen based on size and location, and the rest region is RONI (Fig. 2).

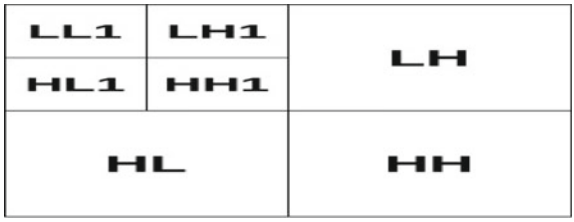

Fig. 3 Wavelet transform

4.2 Discrete Wavelet Transform

The most popular transforms are the Discrete Wavelet Transform (DWT), Discrete Cosine Transform (DCT) and Arnold Transform. Here, we embedded watermark in transform domain. We used a Discrete Wavelet Transform. This Wavelet Transform has multi-resolution characteristics due to which hierarchical or nested embedding is more efficient in case of DWT. The main property of the Wavelet Transform is to process data at various scales or multi-resolution. The basic idea of wavelet transform is to split image signal into two parts, high frequencies and low frequencies. The fundamental concept of wavelet transform is that transformation should allow change only in a time extension, not in the shape of the data signal. Wavelet Transform is good at a time resolution of high frequency [25]. In this method, the image signal is split into four non-overlapping sub-bands of different frequencies: LL (low-frequency components), and LH, HL, HH are high-frequency sub-bands. LL sub-band is again divided into four bands; then high-frequency component HL1 is selected for watermarking embedding. Because LL band is most sensitive to human eyes, so embedding in LL1 sub-band can occur unacceptable problems in biomedical images. So the best way for watermarking is to choose a high-frequency band. But HH1 band includes edges and textures of the images, so it also fails the property of watermarking embedding. The most appropriate band for watermark embedding is the HL band; it is horizontal sub-band. Here, we chose HL1 sub-band for watermark embedding (Fig. 3).

$$y_{i-1}^{\mathrm{LOW}}(k) = \sum_{n}^{\infty} x_i(n) l(2k - n) \tag{1}$$

and

$$y_{i-1}^{\mathrm{HIGH}}(k) = \sum_{n}^{\infty} x_i(n) h(2k - n) \tag{2}$$

where $i = I0, \ldots, I, I + 1$. $I0$ represents the lowest resolution index and $I + 1$ represents the highest resolution index.

4.3 Arnold Transform

Arnold Transform is also one of the most famous transform. It is used to scramble images, so that scrambled watermark image can be embedded in original image. Arnold Transform is based on the transformation of the image. It provides a method to hide data in scramble form. It is a reversible method. Using Inverse Arnold Transform, We can reconstruct image again. Human eyes are not sensitive to this transform. It changes every pixel of the image many times. It is robust to many geometrical attacks and noise attacks, such as compression, rotation, cropping, median attack, mean attack, Gaussian noise attack, salt and paper noise attacks [22]. The basic formulation of Arnold Transform is

$$\begin{bmatrix} X \\ Y \end{bmatrix} = \begin{bmatrix} 2 & 1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} x \\ y \end{bmatrix} \bmod N \tag{3}$$

This transformation is called two dimensions Arnold Transform. Where N is the total number of pixels in the image. $(x, y) = (0, 1, 2, 3, \ldots, N)$ are pixels coordinates of image, and $(X, Y) = (0, 1, 2, 3, \ldots, N)$ are pixels coordinates of scrambled image after Arnold Transform. After solving this matrix formula, we get this relation:

$$X = 2x + y \tag{4}$$

$$Y = x + y \tag{5}$$

The cycle of Arnold Scrambling (T) depends on the size of the image.

4.4 Singular Value Decomposition (SVD)

SVD-based watermarking technique is mostly used in the case of small distraction to an image. In this technique, the watermark is embedded into singular values. SVD-based watermarking is robust to several attacks such as geometrical attacks: cropping, rescaling, rotations and compression. However, it fails in noise attacks like Gaussian attacks with high variance. Watermark can be embedded directly into the singular value of the host medical image or host image is subdivided into small blocks using any technique. Precise amounts of the watermark are embedded in those blocks. The basic idea of SVD is given by this formula

$$\begin{bmatrix} U & S & V \end{bmatrix} = \text{svd}(I) \tag{6}$$

where S represents singular values of an image, U and V represent the unitary matrix of image, and T denotes the matrix transposition. If the size of the medical image is $M \times N$, then the size of S will be $M \times N$ and U, V will be of size $N \times N$.

$$I = \mathrm{USV}^T \tag{7}$$

Using Eq. (7), we can get back the host signal (Figs. 4 and 5).

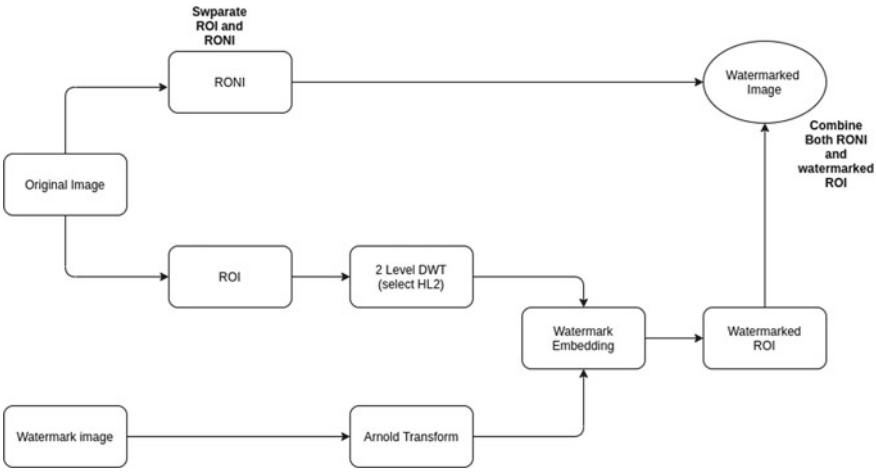

Fig. 4 Watermark embedding for grayscaled image

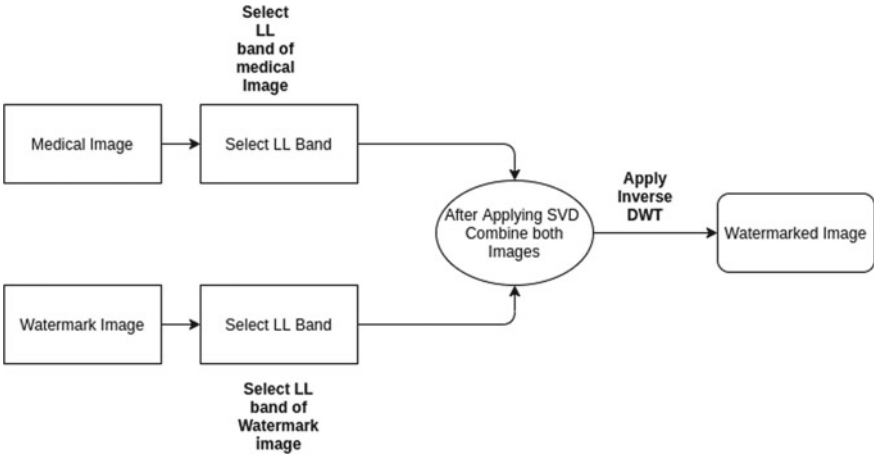

Fig. 5 Watermark embedding for coloured image

4.5 Watermark Embedding

Steps for watermark embedding are shown in flow charts separately for grayscaled image and coloured image. Grayscaled algorithm also can be applied for the coloured image, but for this, we need to use this algorithm separately for red, green and blue level. Here in this article, our focus is mainly on the grayscaled image. So, results from the discussion will be only for a grayscaled image.

1. Watermarking for grayscale image
   - Select ROI and RONI from the cover medical image.
   - Apply DWT using 'haar' wavelet on selected ROI. Select HL1 for watermark embedding.
   - Watermark image size should be 1/4 of selected ROI.
   - Apply Arnold Transform on watermark image using a secret key to get scrambled watermark.
   - Combine ROI after DWT and scrambled watermark using strength coefficient.
   - Apply inverse DWT to get watermarked image [17].
2. Watermarking for the coloured image
   - Apply DWT using 'haar' wavelet on secret watermark image. Select LL band for watermark embedding [3].
   - Apply the SVD technique on both images.
   - Embed singular value of watermark in the singular value of a medical image.
   - Perform inverse SVD.
   - Apply inverse DWT to get watermarked image [5].

4.6 Watermark Extraction

After watermark embedding, it is required to extract the embedded data from the watermarked image to prove ownership and in many more other applications. Extraction algorithm also discussed separately for grayscaled image and coloured image. The original image is required for this process (Figs. 6 and 7).

1. Watermark Extraction in a Grayscale Image
   - Select ROI and RONI from watermarked medical image.
   - Apply DWT using 'haar' wavelet on selected ROI. Select HL1 for watermark embedding.
   - Apply extraction formula to get scrambled watermark image.
   - Inverse Apply Arnold Transform on watermark image using the same secret key to get original watermark.
   - Add ROI after DWT and scrambled watermark using strength coefficient.

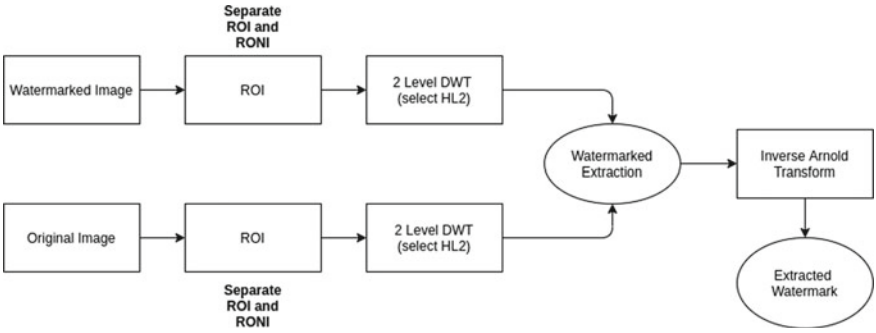

Fig. 6 Watermark extraction for grayscaled image

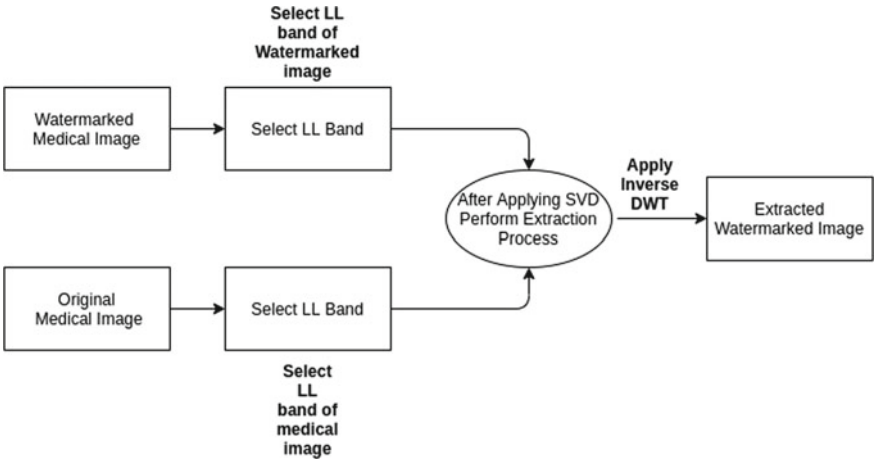

Fig. 7 Watermark extraction for the coloured image

2. Watermark Extraction in Coloured Image
   - Apply DWT using 'haar' wavelet on the host medical image. Select LL band for watermark embedding.
   - Apply the SVD technique on both images.
   - Perform extraction algorithm.
   - perform inverse SVD.
   - Apply inverse DWT transform to get back embedded watermark image [5].

5 Experimental Results

In this section, we have tested our proposed method with some of the art-of-the-method for different biomedical images under separate attacks. We have taken the images (sized = 256 × 256), and we have performed on the MATLAB platform. The parameters we have considered are as follows.

5.1 Parameter of Comparison

RMSE This is calculated to compare two images. This can be calculated using this formula

$$\text{RMSE} = \frac{\sum_{r=1,c=1}^{R,C}[\text{Im1}(r,c) - \text{Im2}(r,c)]^2}{R * C} \tag{8}$$

PSNR PSNR computes the peak signal-noise ratio between two signal. Here, in this method, it computes between two images. It is calculated to measure the quality of images. Higher PSNR represents a good quality watermarked image.

$$\text{PSNR} = 10 \log \left(\frac{R^2}{\text{RMSE}} \right) \tag{9}$$

where R is maximum fluctuation in the image. It is also called as the maximum pixel value in image, and RMSE is root mean square error.

WPSNR It computes the weighted peak signal to noise ratio between two images. It is used to measure the quality of the image (Figs. 8, 9 and 10; Tables 1, 2, 3 and 4).

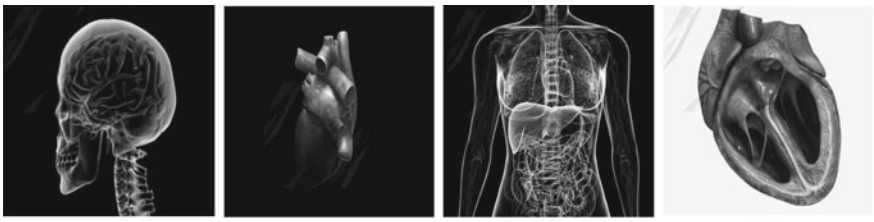

Fig. 8 Tested images

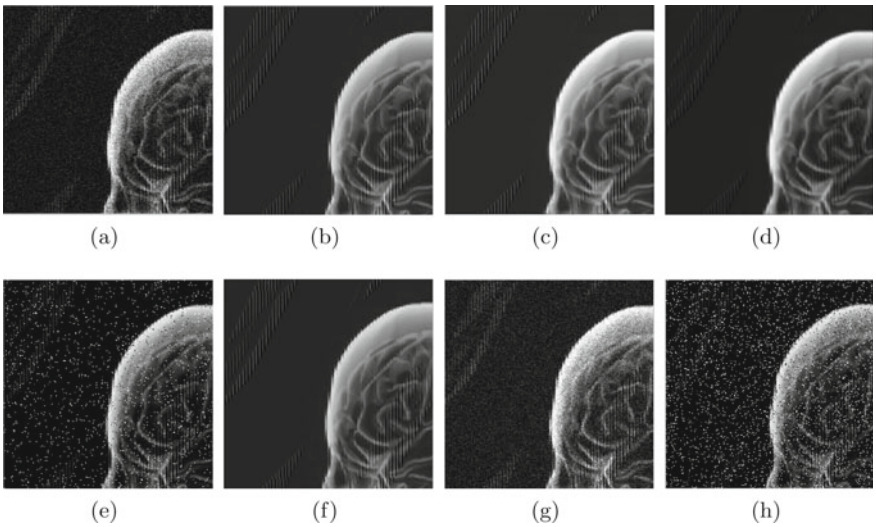

Fig. 9 Different attacks on watermarked image1

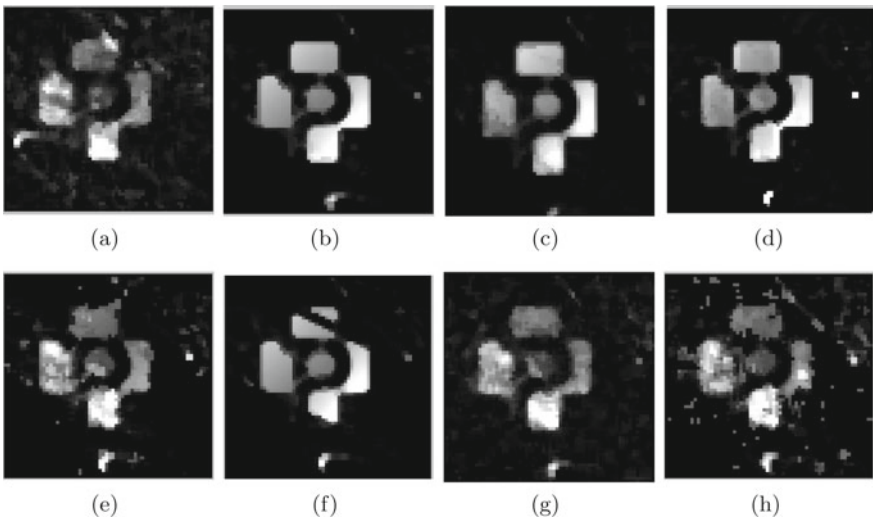

Fig. 10 Extraction of watermarks at different attacks on image1

Table 1 Attacks with their quantitative parameters for input image1

Parameter	Gaussian	Cropping	Median	Mean	Salt and pepper $v = 0.05$	t rotation	Gaussian	Salt and pepper $v = 0.1$
PSNR	59.8619	58.8542	59.1014	58.7957	59.1850	58.9906	59.0904	58.3628
MSE	0.5736	0.7965	0.7630	0.7877	0.7999	0.6825	0.8712	0.8779
WPSNR	17.5670	16.4389	16.6230	16.4167	16.9007	16.6052	16.7534	16.3616
PSNR2	31.9566	16.4389	31.7368	31.7681	31.9790	31.9833	31.9689	31.7112

Table 2 Attacks with their quantitative parameters for input image2

Parameter	Gaussian	Cropping	Median	Mean	Salt and pepper $v = 0.05$	t rotation	Gaussian	Salt and pepper $v = 0.1$
PSNR	59.2313	58.7900	59.0736	58.6911	59.2074	58.9404	59.5762	58.7893
MSE	0.7030	0.7850	0.7865	0.8000	0.6645	0.7020	0.6462	0.7254
WPSNR	16.9454	16.3973	16.6031	16.3810	16.9770	16.5876	17.2609	16.6873
PSNR2	29.1478	29.1674	29.1628	29.1004	29.1878	29.0949	29.1674	29.1878

Table 3 Attacks with their quantitative parameters for input image3

Parameter	Gaussian	Cropping	Median	Mean	Salt and pepper $v = 0.05$	t rotation	Gaussian	Salt and pepper $v = 0.1$
PSNR	59.3534	58.9116	58.9754	58.8214	59.1258	59.3413	59.2582	59.0909
MSE	0.78050	0.8027	0.7986	0.8551	0.8085	0.6825	0.8827	0.8980
WPSNR	16.9749	16.5522	16.5507	16.6352	16.9407	16.6052	16.9749	16.9954
PSNR2	22.5024	22.7727	22.8597	22.7659	22.7385	22.3268	22.8974	22.4701

Table 4 Attacks with their quantitative parameters for input image4

Parameter	Gaussian	Cropping	Median	Mean	Salt and pepper $v = 0.05$	t rotation	Gaussian	Salt and pepper $v = 0.1$
PSNR	59.6324	58.9336	58.9240	58.8500	59.4379	58.4789	59.6606	59.2702
MSE	0.7596	0.7972	0.7942	0.8024	0.7468	0.6642	0.7024	0.7625
WPSNR	17.3503	16.5286	16.4461	16.5153	17.1086	16.2466	17.3602	16.3616
PSNR2	30.7533	30.7129	30.7912	30.6382	30.5649	30.3788	31.4631	30.8512

6 Conclusions

In the medical industry, for the transmission of the medical image between hospitals, the security of the image is essential. Security has become the most desired factor in modern days. This problem can be solved using robust digital watermarking technology. This paper provides us with a unique method of protecting biomedical images from several attacks that have been already discussed. This method RONI of original medical image is used for watermark embedding. Size of ROI and RONI is selected based on size. ROI should not be greater than 25% of the original image. In this technique, quality of medical images is not being destroyed by embedded watermark image. In the extraction process, the watermark can be extracted with high PSNR value. To measure the quality of extracted watermark, we calculated peak signal to noise ratio (PSNR), root mean square error (RMSE) and weighted peak to noise ratio (WPSNR) for more than 100 images. It is giving us a PSNR value up to 59.86 dB, RMSE value less than 0.7965 and WPSNR value up to 17.567 dB. These results show that our watermarking technique can be beneficial in the field of the healthcare industry. This watermarking technique provides us with security that is necessary for medical images. However, this watermarking method fails the shear attack. Our future work is to make this algorithm more robust.

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Review of Antenna Array for 5G Technology Using mmWave Massive MIMO

Kailash V. Karad and Vaibhav S. Hendre

1 Introduction

In today's world, high data rate is prime requirement for any user and any application to be run on OS (operating system). The necessity [1] of high-data-rate transmission is increased drastically because of large number of users and services available in the market. MmWave [2] is viewed as foremost recurrence possibility in 5G may tender extremely towering transmission rate at cellular communication [3]. Massive MIMO is identified like full dimension MIMO, very large multiuser MIMO, hyper-MIMO or a big number antenna structure which clearly indicates use of large number of antennas at Base Station (BS).

In contrast with usual MIMO, large number of antennas are proposed in massive MIMO which concentrates energy intended for smaller regions, radiation efficiency, low level of interference, user throughput, etc. Also, it enlarges cell range or coverage more effectively for higher frequency bands in mmWave as large number of operational antennas, i.e., antenna array can be packed with a small footprint for high power directivity and helps in propagation for worse conditions of it [4]. Antenna arrays at the transmitter are intelligent to adjust radiation patterns with the time as well as frequency referred as spatial beamforming. Antenna arrays are able to do the spatial filtering also. Mainly, it focuses in space [5] at random point for signal whose environment supports multipath propagation as shown in Fig. 1.

The amalgamation of 5G for mmWave spectrum at base station and mobile phone requires highly directional antenna with beamforming [6]. Nowadays many mobile service providers use spectrum of sub 3 GHz. Although, increase in service demand is not able to fulfill the requirement of user, and the solution to this problem comes out from a band of millimeter wave frequency. This band specifically ranges from 30 to 300 GHz as shown in Fig. 2.

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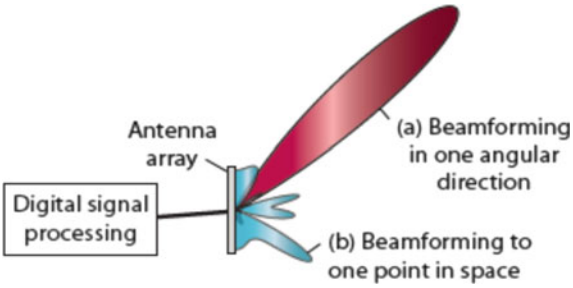


Fig. 1 Antenna array beam formation [5]

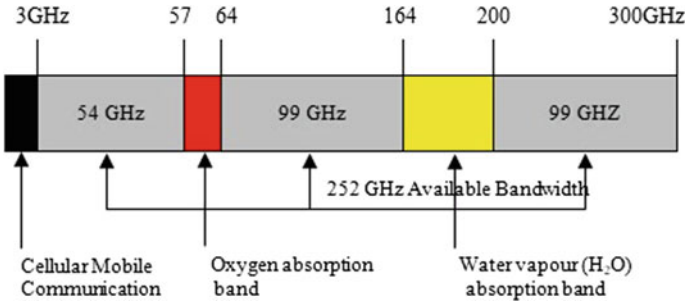


Fig. 2 Millimeter wave band allocation [7]

With this mmWave frequency, 57–64 GHz band as well as 164–200 GHz are found as absorption band for oxygen and water vapor, respectively, which are not appropriate to have propagation because of attenuation from water vapors (mainly occurs by 180 GHz). In short, over the entire mmWave band, 252 GHz spectrum is available for mobile broadband communication [6, 7]. The frequency band 57–67 GHz is unlicensed V band whereas 71–76 GHz and 81–86 GHz is lightly licensed E band. This band offers bandwidth in terms of gigahertz. E band supports transmission distance up to 500–700 m whereas V band supports up to several kilometers due to oxygen and rain attenuation, respectively. This helps to minimize inter-cell interference. MmWave have small wavelength which in turn results into use of antennas in large scale manner we referred the term as massive MIMO which is best suited at the base stations (BS) of macro cell and small cells. In brief, it is improving the value of directivity, spatial gain, cell coverage, frequency reuse and reduction in the value of path loss which is major impact for mmWave. Ultimately, this will save the setting up time of a BS, space required for it and always for which we think that is cost, will also get reduced [8].

Mainly in case of antenna arrays, geometrical configuration (placing of antennas), individual antenna pattern, array factor, mutual coupling and impedance plays vital role for system performance [9]. Accordingly, geometrical configuration of array in 5G for massive MIMO should be explored and evaluated. This may have rectangular, hexagonal, circular or cylindrical configuration of antenna array which could be

premeditated by requisites of number of antenna elements, operating frequency, radiation pattern, directivity (gain), beamwidth, mutual coupling, return loss and effect of all this on area coverage, signal strength of received signal, SINR (signal to noise and interference ratio), throughput, spectral efficiency and the channel capacity must be analyzed. The exploration may through one or many frequencies like 6 GHz, 28 GHz, 38 GHz or 60 GHz from mmWave frequency band and evaluation through different types of antenna elements with desired number of it; likewise microstrip patch, slot, dipole, lens, yagi-uda and many more.

2 Observations About mmWave Bands

2.1 Less Propagation

Misinterpretation about the mmWave is that, higher frequencies propagate less than smaller frequencies at free space as path loss (PL) is deliberated among two antennas (isotropic in nature) for definite frequency or with the help of dipoles.

2.2 Shorter Wavelengths

It is proved [7], shorter wavelengths (higher frequencies) propagates longer than longer wavelengths (lower frequencies) because of narrower beams which are more directional at higher frequencies. This helps to lessen interference, moreover strengthening spatial multiplexing along with access capabilities at cell site.

2.3 Penetration

Penetration of Millimeter wave through solid material is weak (e.g. bricks, concrete) compared to lower frequency signal. At the same time, penetration through wood, cardboard and plastic is good for mmWave communication.

2.4 Attenuation

The key achievement of mmWave band is that, human body or metal objects are less penetrating but they are acting as a good reflector for the frequency of 28 GHz and attenuate more in heavy rain.

2.5 Power

Normally, when wavelength is short, then more power is distributed by particles in the signal transmission path and misalignment of beams leads to criticism which needs to be resolve.

Basically, mmWave supports high frequency which results into more path loss during transmission and reception of signal. This can be resolved by using beamforming gain with the massive antenna array structure. As the frequency in mmWave is high, i.e., wavelength is very small, so it is possible to pack antenna arrays into a smaller physical size. This will help us to improve the spectral efficiency as well as bandwidth as multiple antennas will be used for transmission and reception purpose which will provide separate path for it. The received power P_r in a wireless system is given by;

$$P_r = \frac{P_t G_t G_r \lambda^2}{(4\pi)^2 r^2} \tag{1}$$

where P_t symbolize transmitted power, G_t and G_r termed as transmitting and Receiving antenna gain, whereas r is separation distance of transmitting and receiving antenna or range and λ as signal wavelength. The path loss may be setup easily from Eq. (1). From a single base station of macro cell by means of massive antenna array, all the small cells residing in the same macro cell will get serve as shown in Fig. 3. This will help to improve the small cell mobile user's data rate and minimizes path loss, power requirement at base station. On the way to get better antenna array gain, phase shifting of each antenna can be implemented by using phase shifter. This will improve the signal transmission and reception intended to achieve high directivity and gain. Implementation of this leads to highly directed beams referred as a hybrid beamforming and gain of this is depend on the size and dimension of antenna array [10].

The existing technology of 4G (LTE or LTE—advanced) with MIMO employed combination of 2–4 compact antennas in signal transmission as well as reception.

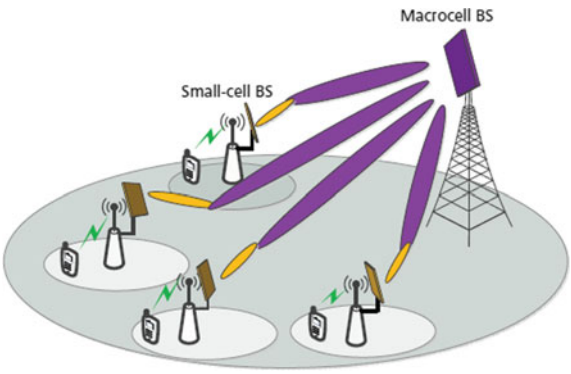


Fig. 3 mmWave massive MIMO structure for 5G implementation [8]

In 5G, it is proposed to make use of more than 100 antennas (preferably 128) with massive architecture. This will lead to improve the cell capacity, data rates, enhancement in signal to noise ratio by offering highly directional beam antenna [11].

3 Antenna Array for mmWave Band

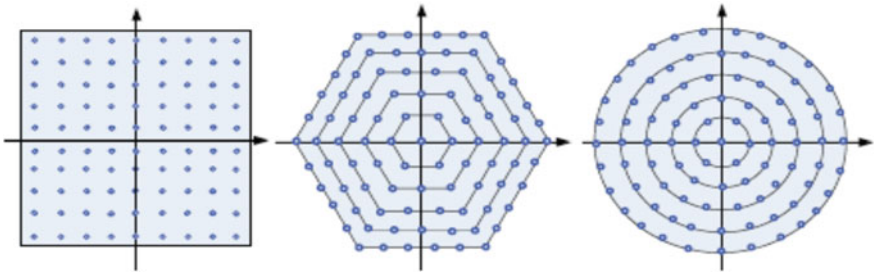
As discussed earlier, for minimization of path loss and coverage improvement; directional antennas and beam formation with steering capability is very important at mmWave frequencies. In this section we are going to focus on antenna array construction, simulation methods and parameter measurements with comparative results of it.

3.1 Planner Type Array

The work [12] is mainly deals with three types of planner array, viz. uniform rectangular, hexagonal and circular planner array. These are also referred as, URPA, UHPA and UCPA as given in Fig. 4.

Author designed and simulated the structure of above three antenna array with inter-element spacing of $\lambda/2$ considering the frequency 30 GHz and beyond. Attained results are summarized in Table 1.

Looking at the observations of Table 1, all three antenna configurations have almost same value of gain and beamwidth. Overall, the performance of UHPA is good considering geometrical area and HPBW which helps to fit into compact size because of smaller area. This also proves that, though the operating frequency lies in mmWave band, there is no effect on use of planner antenna array system.



(a) Rectangular array (b) Hexagonal array (c) Circular array

Fig. 4 Planner array configuration in 2D [12]

Table 1 Physical dimension and measured parameters for planner antenna arrays

Parameter/type of array	URPA	UHPA	UCPA
Antenna elements	90	91	91
Geometric area	22.5 λ^2	16.24 λ^2	19.64 λ^2
Maximum gain (dB)	42.39	42.63	43.00
HPBW (3 dB)	11.300	10.150	10.820
SLL (dB)	−12.90	−18.86	−17.65

3.2 Lens Antenna Array

In [10] lens antennas for static and mobile user with variation in the size of lens antennas are proposed. This resulted into high directivity and gain compared to non-lens types of antennas. Utmost use of lens at the place of usual phase shifter lessens computational difficulties in beamforming design with power consumption. Here, lens performs the role of virtual phase shifter (passive in nature) which focuses incident EM wave in assured region. It performs important role when used in combination with antenna array. It focuses on signal power to achieve towering directivity (gain) and this power is directed into sub-area covered by array antenna.

A lens with antenna array is referred as *N* element lens antenna. Here, two types of lens antennas are designed, simulated (using HFSS), and fabricated at operating frequency of 28 GHz, inter-element spacing of 10 mm with the hyperbolic lens (made of polyethylene) having dielectric constant $\varepsilon_r = 2.2$ in a vertically polarized manner. The comparative of antenna array parameters are described with Table 2.

From above geometrical configuration, author compared the performance of SULA and MULA with no lens antenna arrays and found improvement in the directivity, gain, half power beamwidth (HPBW). Specifically, SULA attained gain value of 25 dB (more around 17 dB) and MULA attained gain of 12.5 dB with the small value of HPBW as ±6.5° in comparison with no lens. In broad view manner, it is clear that making use of lens with antenna array (lens antenna) helps to improve the value of directivity, gain, narrower of beamwidth and beam switching either with static user or mobile user.

Table 2 Types of lens antenna array with different parameters

Type	Geometry	Patch size	Position of lens	Beam switching	Application
SULA	Cube $1 \times 1, 2 \times 2, 1 \times 4$	50 mm × 50 mm × 60 mm	Behind the patch	Not necessary	Static user
MULA	Square $1 \times 4, 4 \times 4$	3.05 mm × 3.05 mm	In front of patch	Necessary	Mobile user

Table 3 Summary of antenna array architectures with different shapes

Type of array	Element spacing	Gain variation w.r.t. main lobe	Gain variation w.r.t. side lobe
8 × 8 rectangular	λ × 2	3–5 dB	More
64 circular	λ/ 2, 3 λ/2, 5 λ/2, and 7 λ/2 as diameter	Not changed	Less
61 hexagonal	λ/2	Not changed	More
16 crisscross	Vertically 2 elements adjacent to each other	3–5 dB	Less

3.3 Antenna Array with Various Shapes

Author [13] proposed four designs of array typically; rectangular, circular, hexagonal and crisscross shape. Firstly, 8 × 8 rectangular array where spacing between elements is kept as λ × 2 to form a square grid along x and y directions. Secondly, 64 circular arrays with 16 elements in each four concentric circles having diameter $\lambda/2, 3\lambda/2, 5\lambda/2,$ and $7\lambda/2$ are selected correspondingly. Thirdly, hexagonal array with 61 elements at a spacing of λ/2 is chosen between adjacent two elements. Lastly, 16 crisscross shape arrays arranged vertically to each other with two 8-elements linear array. Thus, the circular type array hits perfectly in outdoor propagation of mmWave as it covers larger area through which it obtains high gain and directivity compared to other array structure. The summary of all these antenna types is presented in Table 3.

3.4 Patch Array

In [14], use of 57–64 GHz unlicensed band for 5G communication is proposed because of increased outside emanation power level. The author has designed and simulated (in CST) antenna array structure for desired frequency. Formulae for designed structure are taken as follows;

$$\frac{w}{h} \geq 1 \tag{2}$$

$$\varepsilon_{\text{reff}} = \left(\frac{\varepsilon_r + 1}{2}\right) + \left(\frac{\varepsilon_r - 1}{2}\right) \times \left(\sqrt{\left[1 + 12\frac{h}{w}\right]}\right) \tag{3}$$

Fringing effect leads enhancement in patch length by ΔL given as;

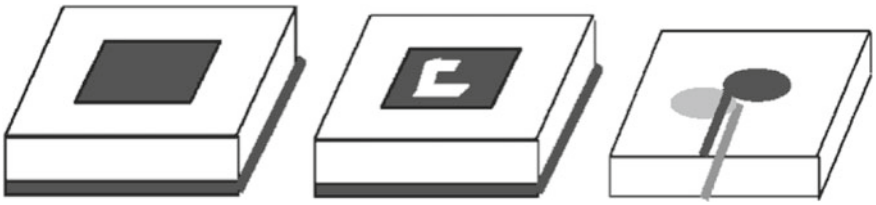
$$\Delta L = (0.412 \times h) \times \left[\frac{(\varepsilon_{\text{reff}} + 0.3)\left(\frac{w}{h} + 0.264\right)}{(\varepsilon_{\text{reff}} - 0258)\left(\frac{w}{h} + 0.8\right)}\right] \tag{4}$$

$$L_{\text{eff}} = \frac{c}{2f_r \times \sqrt{\varepsilon_{\text{reff}}}} - 2\Delta L \tag{5}$$

The substrate material RT Duroid 5880 (thickness = 0.508 mm) is opted with dielectric constant $\varepsilon_r = 2.2$ for the frequency band of 57–64 GHz resonating around 60 GHz. The schematic of entire patch antennas are shown in Fig. 5.

Antenna having cut in slot as in Fig. 5b gives larger bandwidth with respect to S_{11} characteristic for the said spectrum compared to other shapes. With this conclusion, author designed and fabricated the same structure of antenna arrays with same material specifications. The summary of all antenna parameters with geometry is listed in Table 4 (Fig. 6).

The best suited structure is slot array (1 × 10) when compared with other structures of Table 4 as the value of gain (15.3 dB) is highest and beamwidth (half power beamwidth—10.2°) is narrower exclusive of SLL (side lobe level).



(a) rectangular patch (b) broadband patch (c) elliptical patch

Fig. 5 Microstrip patch antenna element types [14]

Table 4 Comparison of microstrip antenna arrays for different parameters

Array structure	Geometry	Area (mm^2)	Beamwidth (in o)	SLL (in dB)	Gain (in dBi)
Comb-line array		4 × 21	17.0	−4.6	9.9
Probe fed comb-line array		5 × 38	11.6	−10.3	16.3
Linear series fed array		5 × 27	17.1	−11.4	12.0
Probe fed array (1 × 10)		5 × 27.5	10.3	−13.2	15.2
Slot array (1 × 10)		5 × 27.5	10.2	−13.6	15.3

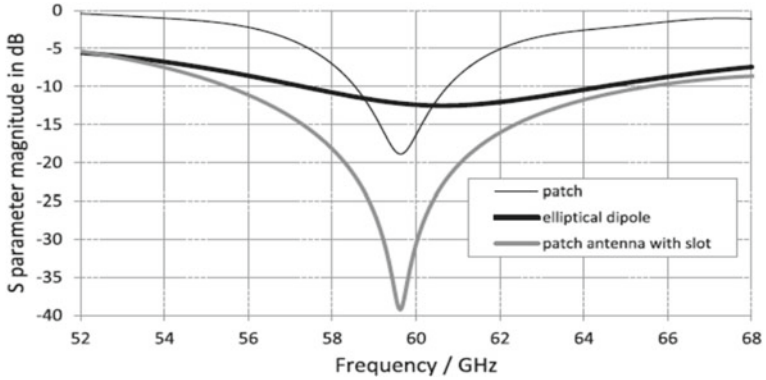


Fig. 6 Plot of S_{11} against frequency

3.5 Patch Type 2 × 2 Array

Author [11] designed a patch antenna at a frequency of 29 GHz for a mobile handset with two 2 × 2 antenna array. The orientation of arrays is kept as orthogonal to achieve spatial diversity and polarization diversity. Author design and simulated the said work into Altair FEKO 3D electromagnetic simulation software. In order to obtain flexibility in operation of antenna configuration, it is recommended that each array can be excited at a time or both at the same time.

3.6 Antenna Array (128 Elements) Simulation Analysis

An array of 128 elements are considered [15] for radio propagation simulation in outdoor urban area environment at a frequency of 28, 38 and 60 GHz of mmWave band. By means of ICS Telecom EV software, coverage analysis of basic coverage, signal-to-noise and interference ratio (SNIR) along with throughput is performed. Total 21 transmitters are used to cover an area of 1.352 km^2 by considering seven points of base station with each having sector of 120°.

Results of Table 5 are very indicative for mmWave frequencies specifically 28, 38 and 60 GHz in the use of 5G technology with respect to area coverage, value of SNIR and throughput.

Table 5 Summary of simulation analysis for coverage, SNIR and throughput

Frequency (GHz)	Area coverage value (%)/(dBm)	SNIR coverage value (%)		Throughput coverage value (%)
		For 10–15 dB	For 16–90 dB	For 124,470–134,710 kbps
28	35.10 (−116 to −107)	0.47	98.71	80.99
38	30.31 (−126 to −117)	1.56	98.20	58.03
60	26.20 (−126 to −117)	2.58	54.00	24.33

4 Applications of mmWave

Today, use of massive MIMO becomes a prominent in view of mmWave applications to support 5G technology. Many applications, technologies have been opened because of usage proposed in mmWave frequency bands. A few are considered here as follows.

4.1 IOT (Internet of Things)

This is a recent trend going on in industries which enabled communication among device to device (D2D) and/or one machine to others with the help of sensors. This involves communication of multiple devices simultaneously in a real-time manner. To have communication between all these, efficient antennas are required along with high speed and large amount of bandwidth. This shows the way to make use of mmWave frequency for such applications. The power consumption and connectivity of all these devices is also a main concern which can be limited by mmWave frequencies [3, 9].

4.2 Vehicular

Nowadays many vehicle safety applications are developed which keeps control on the speed of vehicle, road directions, remotely opening and closing of doors and windows, etc. This needs number of sensor to be active all time, but still there is limitation on sensor range. To increase the range of sensor for generating high data rate use of compact size antenna with automated vehicle is possible which is certainly gifted by mmWave communication.

4.3 Medical

In medical field, imaging is one of the important part for diagnosis of different layers of skin or tissues of the body. The mmWave provides ability to display and measure various parameters associated with human body because of its smaller wavelength. To do imaging with high level resolution, mmWave probes such as co-axial as well as waveguide with integrated structure of antenna into device are preferable.

4.4 Massive MIMO

At present, cellular communication uses MIMO having antenna elements as less than or equal to eight. In 5G, use of mmWave will lead to enhancement in the number of antenna elements from MIMO to massive MIMO which enables count greater than eight to thousands. This will show the way of achieving high speed communication, high gain and highly directive patterns.

5 Discussion

In this paper, we focused on the part of mmWave band for 5G through massive MIMO challenges, advantages and its key features. The frequency from 3 to 300 GHz is primarily pledged for enhancement in data rate, cell capacity, bandwidth, spectral efficiency and throughput by adopting antenna array structure at the transmitter or receiver site. Also, different antenna array structures have been studied like uniform rectangular, circular, hexagonal, cylindrical, elliptical, crisscross with the configuration of 1×4, 1×10, 2×2, 4×4, 8×8, 90, 91 or 128 elements. The concept of lens antenna at 28 GHz for static and mobile user (SULA and MULA) is also innovative approach to fulfil the user's requirement of high data rate with lesser power. The authorization for researchers to do work in mmWave frequency band for 5G applications can be understood from simulation of radio propagation model at 28, 38 and 60 GHz. This shows the improvement in cell area coverage, overall throughput and SINR.

Thus, in broad manner, antenna elements in large number with beamswitching-assisted improvement in gain (directivity), SNIR, and narrowing beamwidth with reduced side lobes.

6 Conclusion

As on today, all over the world, research is going on to increase the data rate with the innovative technologies which has forced to make use of mmWave frequency band. These technologies are preparing the base for 5G mobile network services incorporated with massive MIMO. Most of the work from 5G services' point of view has been initiated for the mmWave frequency band, typically at 28, 38 and 60 GHz. The frequency band 57–64 GHz is unlicensed V band whereas 71–76 GHz and 81–86 GHz E-band is lightly licensed which is advantageous and inspiring to researchers in near future. The design of antenna array for mmWave frequency band is a challenging because of its smaller wavelength, but at the same time, it is offering features like larger bandwidth, less power requirement, physically compact or small in size to set up a base station with massive number of antennas, cell coverage and thereby throughput, etc.

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Cattle Health Monitoring and Tracking System

R. Boopathi Rani, Dilshad Wahab, George Benedict Dung Dung, and Meruva Reddy Sai Seshadri

1 Introduction

The basic idea of the project is to help the farmer to treat the cattle which is having some disease before the situation of the cattle reaches the last stage, thus preventing the loss of cattle. The method that we are planning to use to detect whether the cattle is having any disease or not is to measure the various common parameters and compare them to healthy cattle. Any animal with any disease will show variations in the heart rate, temperature and sleep patterns when compared to healthy cattle. The idea is to create a wireless body area network device to measure the heart rate, the body temperature and sleep patterns of the cattle hence finding it out whether the cattle are healthy or not and inform the farmer. This will help the farmer to treat the infected cattle hence preventing the spread of the disease to other animals and hence saving the infected animal.

The subject or animal that we are considered for the project is cow or horse since dairy industry owns a very large percentage of the animal husbandry and is a major source of income for farmers other than their farming and poultry and horse because the same system tests can be run on a horse.

1.1 Applications

- The project is aimed to detect the infected cattle and resulting in the required treatment to cure the disease.

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- To reduce the loss to the farmer caused due to the death of the infected cattle and even due to spreading of the disease.
- To increase the gain out of the animal husbandry by maintaining healthy cattle, hence increasing the production rate.

2 Literature Review

There are different kinds of diseases affecting animals. It is essential to find the animal's health and monitoring its health condition. Lovett et al. proposed monitoring using infrared thermography. It was used to find the foot to mouth disease in the cow [1]. Handcock et al. proposed GPS collars for finding the location of the animal. They also used a wireless sensor network (WSN) and satellite remote sensing technique to find the animal location and its behaviour [2]. Nadimi et al. proposed monitoring the animal presence and pasture time using Zigbee-based WSN [3]. Hopster et al. proposed a heart rate monitoring system during different time instants and situations to know the stress response of an animal. For the recording of heart rate, surface electrocardiograms (ECG) are often used [4]. Pavan Sikkha et al. mentioned in their paper about the way how wireless technologies can be used for animal tracking, but their paper lacked any kind of health parameter measurements for animals subjected under tracking [5]. Tim Wark, et al. proposed a system for animal control and tracking, but the system is very expensive and utilizes costly sensor and technologies [6]. The papers [7, 8] were referenced to create a smart sensor network for the various sensors involved. Stewart et al., proposed a system to evaluate stress in dairy cows using infrared thermography, and these non-invasive measures were kept in mind while designing the system [9]. If we analyse the proposed systems, those are complicated, inconvenient or costly.

Considering the practical difficulties, the simple system is proposed in this paper which is also at affordable price. The proposed system monitors the health of a cattle and informs the farmer when the parameters deviate from the normal values. This system monitors the temperature, heart rate and sleeping pattern. The normal values for these parameters are given in Table 1. The proposed system continuously monitors these parameters and informs the farmer when the deviation is found significant, i.e., when the animal is restless, diseased and also too tired.

Table 1 Recommended optimal values

Optimal temperature range	98–104 °F
Optimal heart rate range	48–84 beats per min
Optimal sleep duration	3.9 h per day

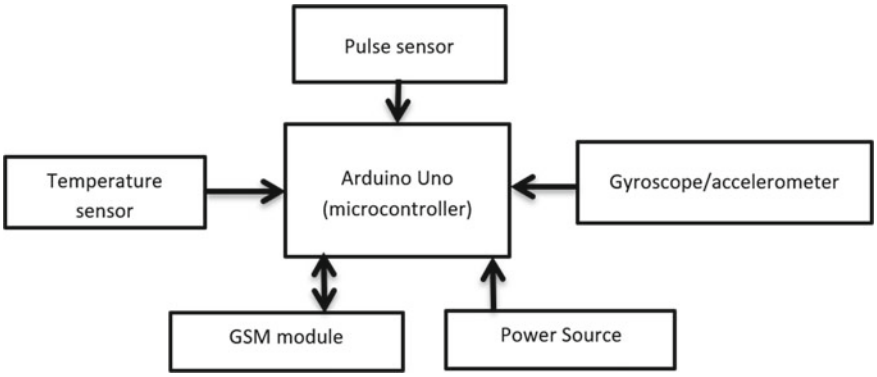

Fig. 1 Basic block diagram of the proposed system

3 Hardware Details

The input from all the sensors in the health tracker will be taken in by the microcontroller. And if any variation or irregularities in the readings are noted, then the owner of the cattle will be intimated about these changes so that proper action could be taken. This process of informing is done by the GSM network module. The block diagram of the system is shown in Fig. 1. This system uses Arduino UNO microcontroller board, Pulse Rate Amped sensor, MLX90614 temperature sensor, MPU6050 (gyroscope and accelerometer) and GSM Module (Adafruit FONA 808 module).

Various software used:

1. Arduino software IDE
2. MATLAB.

Programing language used was C and Embedded C.
Various interfaces involved:

1. MLX90614 temperature sensor uses the I2C protocol.
2. Pulse Rate Amped sensor uses Serial communication.
3. MPU6050 gyroscope and accelerometer use Serial communication.
4. GSM Module (Adafruit FONA 808 module) uses Serial communication.

4 System Modelling and Design

An embedded system is a blend of hardware and software and possibly other mechanical parts designed to perform a definite function. Theoretically, sensors send raw data to the microcontroller. The microcontroller converts the raw data to the required readings and an SMS is sent to mobile phone with the help of a GSM modem using AT commands. Figure 2 shows the proposed system implementation model.

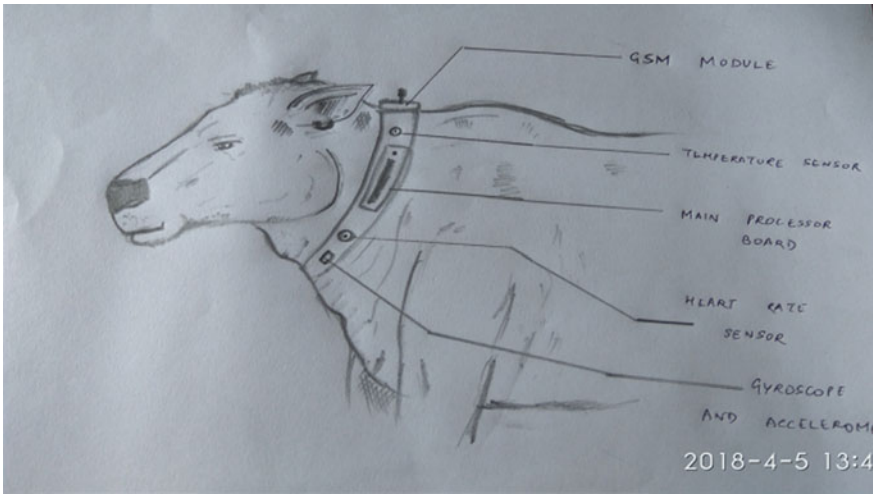

Fig. 2 Implementation model

The project is aimed to detect the infected cattle and resulting in the required treatment to cure the disease. A wireless body area network device is created to measure the heart rate, body temperature and sleep patterns of the livestock using the appropriate sensors (Pulse Rate Amped sensor, MLX90614 temperature sensor, MPU6050 gyroscope and accelerometer) which help to detect the health of the cattle and hence report back any fluctuations in the readings taken to the farmer using GSM Module (Adafruit FONA 808 module). The main interfacing board used for this is Arduino Uno programming board.

5 Implementation and Results

Non-contact temperature measurement is carried out using an infrared thermometer MLX90614. Figure 3 shows the temperature sensor interface and its output. Plug-and-play heart-rate sensor is used to count the pulses. This is used to measure the heart rate of cattle. Figure 4 shows the heart rate sensor interface and its output. The gyro module is MPU6050 chip which communicates with the microcontroller board through I2C serial communication via the serial clock and data. Figure 5 shows the gyro module interface and its output. GSM SIM808 is used in this system. Figure 6 shows GSM interface and measured parameters such as latitude, longitude, the temperature in Fahrenheit and heart rate.

The testing of the integrated system was done, and the results of all the sensors were obtained. All the sensors were working properly and the results were sent to a mobile phone through the GSM Module. The integrated system is shown in Fig. 7. This can be designed as a belt and put on the neck of a cattle as shown in Fig. 2.

Fig. 3 Temperature sensor interfacing and results on serial monitor

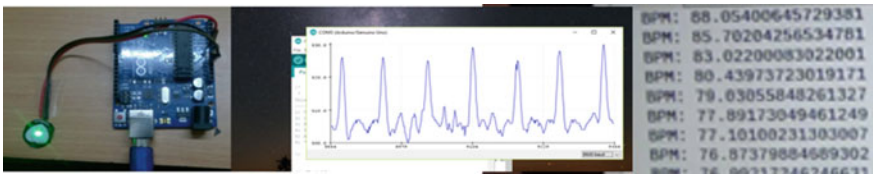

Fig. 4 Heart rate sensor interfacing, its results on the serial plotter and on the serial monitor

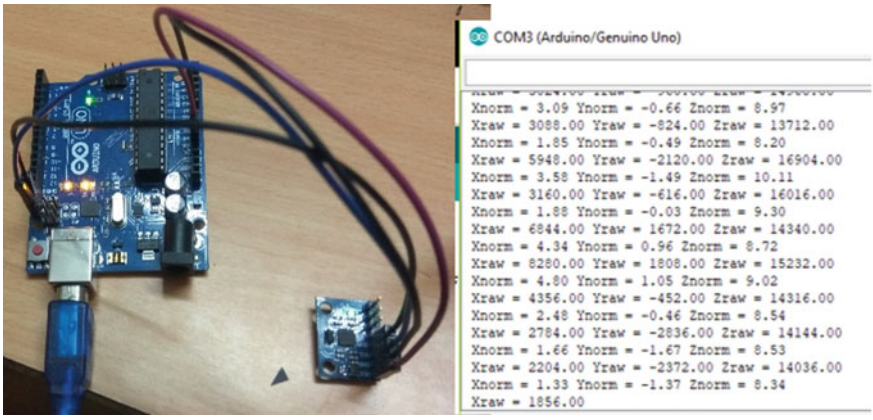

Fig. 5 Gyroscope and accelerometer interfacing and its results on the serial monitor

6 Conclusion

This paper presents a proposed system which is a wireless body area network device to measure the heart rate, body temperature and sleep patterns of the livestock using the appropriate sensors. This helps to detect the health of the cattle and hence report back any fluctuations in the readings taken to the farmer using GSM Module. The main

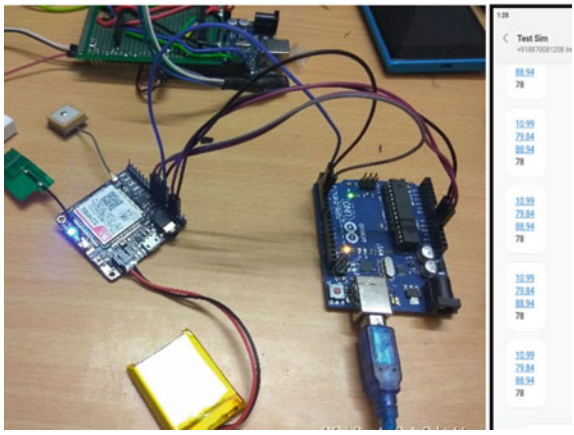

Fig. 6 GSM module interfacing and output

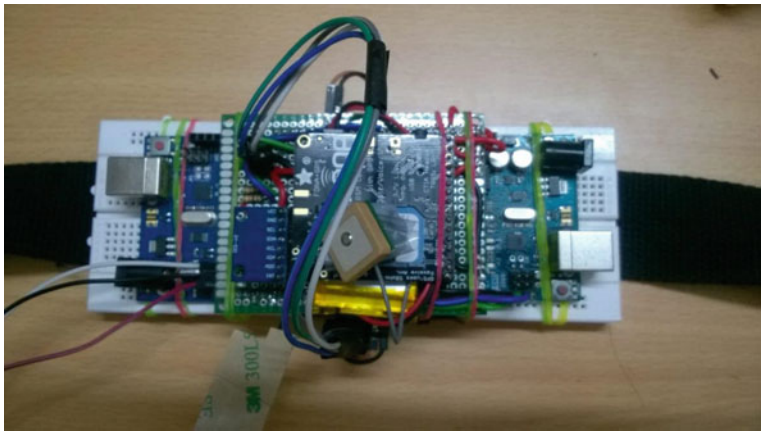

Fig. 7 The integrated system

interfacing board used for this is Arduino Uno programming board. The Arduino code for sending messages from the GSM module is written, and the same is done for all the three sensors. This proposed system can be successfully used to increase the yield and health index of cattle coming from the animal husbandry sector hence improving the GDP by a very large fraction. It will not only help the farmers but the vets could use this efficiently to track the health of the cattle.

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Utilization and Selection of Best SU Act as Relay via Cooperative NOMA (CNOMA)-Based CRNs for Next-Generation (5G) Communications

Ashok Kumar, Mani Shekhar Gupta, Krishan Kumar, and Sumit Kumar

1 Introduction

In a couple of years, Non-Orthogonal Multiple Access (NOMA) being the center of attraction for the researcher to facilitate multiple users in powdered form on the same time/frequency bands to improve the spectral efficiency of 5G communication over orthodox Orthogonal Multiple Access (OMA) in CRNs [4, 6, 8, 13].

Usually, the signal received at the destination through direct and indirect path is combined with the utilization of space diversity to mitigate various impairment [9, 11] of channel. Relays are used to create an indirect route. These relays are dedicated and user-oriented. The relays which standalone and not been selected by among users are known as dedicated relays. Outage probability of two users and relay selection by two-stage techniques are examined through a dedicated relays Cooperative NOMA (CNOMA) [2, 7, 14]. However, in the ad hoc network, installation of dedicated relays is robust and sophisticated. The user-oriented relays are utilized among users. In this case, users are being used as relays to improve the reliability of transmission for weaker channel gains user because more energetic gain users decode the other users signal through Successive Interference Cancellation (SIC) [3, 12]. Moreover, in relay processing, all available users can participate and enhanced processing complexity on SIC and through the grouping of (far and near) users with near user act as a relay for away user [1, 5].

The left of the paper is sorted as Sect. 2 presents a CNOMA-based CRNs system model. The examination of performance is to be done in Sect. 3. Sections 4 and 5 illustrate the discussion of results and conclusion, respectively.

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2 System Model

Taking a downlink underlay, NOMA-based CRNs with a base station (BS) which unicast/multicast the multiplexed signal to a primary user (PU) and a bunch of (N) secondary users (SUs) in the first slot, respectively. During the second slot of time, all SUs have decoded their signals utilizing Successive Interference Cancellation (SIC). Best SU (n^*) is being selected which further act as a relay to retransmits the remaining signal to PU. Both the signal is reached to PU (from BS as well as best SU), and the best signal is to be selected through selection combining techniques (Fig. 1).

In first slot of time, the multiplexed signal at BS is defined as $x_b = a_p x_p + a_{s_n} x_{s_n}$ aired to PU and multiple SUs with unit power, where x_p and x_{s_n} are signal of PU and N SUs, respectively. a_p and a_{s_n} are the corresponding power coefficient with $a_{s_n} < a_p$ and $a_{s_n}^2 + a_p^2 = 1$, i.e. $n \in (1, 2, \ldots N)$. Thus, the signal observed at PU and n SUs is expressed as

$$y_{b,p} = \sqrt{P_{\text{BS}}} x_b h_{b,p} + w_{b,p} \tag{1}$$

$$y_{b,s_n} = \sqrt{P_{\text{BS}}} x_b h_{b,s_n} + w_{b,s_n} \tag{2}$$

where P_{BS} mentions the BS power, $h_{b,i}$ and $w_{b,i}$ interprets the channel coefficients and Gaussian noise [10, 15] between a BS and node i, i.e. $i \in (p, s_n)$, respectively.

Therefore, the received Signal-to-Interference-plus-Noise-Ratio (SINR) at PU is written as

$$\gamma_{b,p} = \frac{\rho a_p^2 \left|h_{b,p}\right|^2}{\rho a_{s_n}^2 \left|h_{b,p}\right|^2 + 1}. \tag{3}$$

Meanwhile, SUs are decoding the high priority, i.e. PU signal first with integration of SIC at n SUs to detect PU signal is expressed as

$$\gamma_{b,p \to s_n} = \frac{\rho a_p^2 \left|h_{b,s_n}\right|^2}{\rho a_{s_n}^2 \left|h_{b,s_n}\right|^2 + 1}, \tag{4}$$

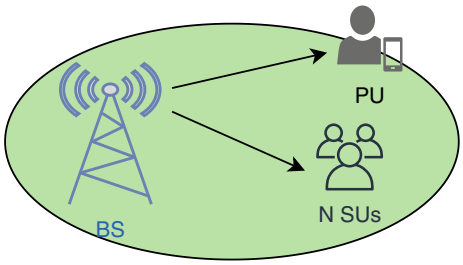

Fig. 1 System model

and the SINR at n SUs can be derived as

$$\gamma_{b,s_n} = \rho a_{s_n}^2 \left|h_{b,s_n}\right|^2. \tag{5}$$

where $\rho \simeq \frac{P_{\mathrm{BS}}}{N_0} \simeq \frac{P_{S_n}}{N_0}$ is assumed without loss of generality.

In second phase, after decoding all SUs signal, then the best SU, i.e. (s_{n^*}) reencode and retransmit the remaining signal, i.e. $x_{s_{n^*}} = a_p x_p$ to PU. Thus, the signal observed at PU comprised as

$$y_{s_{n^*},p} = \sqrt{P_{S_n}} h_{s_{n^*},p} x_{s_{n^*}} + w_{s_{n^*},p} \tag{6}$$

and the corresponding SINR is represented as

$$\gamma_{s_{n^*},p} = \rho a_p^2 \left|h_{s_{n^*},p}\right|^2. \tag{7}$$

The best relay or SU selection is to be completed by

$$s_{n^*} = \arg\max(\gamma_{b,s_n}) \tag{8}$$

3 Performance Evalution

3.1 Outage Probability of SUs

The SUs outage probability mathematically expressed as

$$P_{\mathrm{out},s} = P\left(\gamma_{b,p\to s_n} < \tau_p\right) + P\left(\gamma_{b,p\to s_n} \geq \tau_p, \gamma_{b,s_n} < \tau_{s_n}\right) \tag{9}$$

where $\tau_p = 2^{2C_{\mathrm{out},p}} - 1$ and $\tau_{s_n} = 2^{C_{\mathrm{out},s_n}} - 1$ denote threshold SINR correspondingly associated with $2C_{\mathrm{out},p}$ and C_{out,s_n} outage capacities of PU and n SUs, respectively.

Substituting all given values into (9) and rearranged as

$$P_{\mathrm{out},s} = P\left(\frac{\rho a_p^2 \left|h_{b,s_n}\right|^2}{\rho a_s^2 \left|h_{b,s_n}\right|^2 + 1} < \tau_p\right) + P\left(\frac{\rho a_p^2 \left|h_{b,s_n}\right|^2}{\rho a_s^2 \left|h_{b,s_n}\right|^2 + 1} \geq \tau_p,\ \rho a_s^2 \left|h_{b,s_n}\right|^2 < \tau_{s_n}\right)$$

After simplification, the expression is rearranged as

$$= P\left(\left|h_{b,s_n}\right|^2 < \frac{\theta}{\rho}\right) + P\left(\left|h_{b,s_n}\right|^2 \geq \frac{\theta}{\rho},\ \left|h_{b,s_n}\right|^2 < \frac{\phi}{\rho}\right)$$

where $\theta = \frac{\tau_p}{a_p^2 - \tau_p a_{s_n}^2}$ and $\phi = \frac{\tau_{sn}}{a_{sn}^2}$.

The above expression is concluded as

$$P_{\text{out},s_n} = P\left(\left|h_{b,s_n}\right|^2 < \frac{\eta}{\rho}\right) \tag{10}$$

where $\eta = \max(\theta,\ \phi)$.

The pdf of $f_{\left|h_{b,s_n}\right|^2}$ due to order statistics can be given as

$$f_{\left|h_{b,s_n}\right|^2}(x) = \frac{N!}{(N-n)!(n-1)!} f_{\left|h_{b,s}\right|^2}(x) \times \left(F_{\left|h_{b,s}\right|^2}(x)\right)^{n-1} \times \left(1 - F_{\left|h_{b,s}\right|^2}(x)\right)^{N-n}$$

Further it can be simplified as

$$f_{\left|h_{b,s_n}\right|^2}(x) = \frac{N!}{(N-n)!(n-1)!} \frac{1}{\lambda_{b,s}} \sum_{k=0}^{n-1} \binom{n-1}{k} (-1)^k \, \mathrm{e}^{\frac{-x(N-n+k+1)}{\lambda_{b,s}}} \tag{11}$$

From (10) and (11) provides

$$P_{\text{out},s} = \frac{N!}{(N-n)!(n-1)!} \frac{1}{\lambda_{b,s}} \sum_{k=0}^{n-1} \binom{n-1}{k} (-1)^k \int_0^{\frac{\eta}{\rho}} \mathrm{e}^{\frac{-x(N-n+k+1)}{\lambda_{b,s}}} \mathrm{d}x$$

After solving above expression gives outage probability of SUs as

$$P_{\text{out},s} = \frac{N!}{(N-n)!(n-1)!} \sum_{k=0}^{n-1} \binom{n-1}{k} (-1)^k \left(\frac{1 - \mathrm{e}^{\frac{-\eta(N-n+k+1)}{\rho\lambda_{b,s}}}}{N-n+k+1}\right) \tag{12}$$

3.2 *Outage Probability of PU*

The outage probability of a PU is being calculated through

$$P_{\text{out},p} = P_{\text{out,dir}} \times P_{\text{out,indir}} \tag{13}$$

Taking

$$P_{\text{out,dir}} = P\left(\gamma_{b,p} < \tau_p\right)$$
$$= P\left(\frac{\rho a_p^2 \left|h_{b,p}\right|^2}{\rho a_{s_n}^2 \left|h_{b,p}\right|^2 + 1} < \tau_p\right)$$
$$= P\left(\left|h_{b,p}\right|^2 < \frac{\theta}{\rho}\right)$$

$$P_{\text{out,dir}} = 1 - \mathrm{e}^{\frac{-\theta}{\rho}} \tag{14}$$

now taking

$$P_{\text{out,indir}} = P\left\{\min\left(\gamma_{b,p\to s_{n^*}},\ \gamma_{s_{n^*},p}\right) < \tau_p\right\}$$

Generally, it can be written as

$$= \prod_{n=1}^{N} P\left\{\min\left(\gamma_{b,p\to s_n},\ \gamma_{s_n,p}\right) < \tau_p\right\}$$
$$= \prod_{n=1}^{N} \left[1 - P\left\{\min\left(\gamma_{b,p\to s_n},\ \gamma_{s_n,p}\right) < \tau_p\right\}\right]$$

$$= \prod_{n=1}^{N} \left[1 - P\left(\gamma_{b,p\to s_n} \geq \tau_p\right) P\left(\gamma_{s_n,p} \geq \tau_p\right)\right] \tag{15}$$

Substituting provided values into (15), gets

$$= \prod_{n=1}^{N} \left[1 - P\left(\frac{\rho a_p^2 \left|h_{b,s_n}\right|^2}{\rho a_{s_n}^2 \left|h_{b,s_n}\right|^2 + 1} \geq \tau_p\right) P\left(\rho a_p^2 \left|h_{s_{n^*},p}\right|^2 \geq \tau_p\right)\right]$$
$$= \prod_{n=1}^{N} \left[1 - P\left(\left|h_{b,s_n}\right|^2 < \frac{\theta_n}{\rho}\right) P\left(\left|h_{s_n,p}\right|^2 < \frac{\Phi_n}{\rho}\right)\right]$$

Therefore,

$$P_{\text{out,indir}} = \prod_{n=1}^{N} \left[1 - \mathrm{e}^{\frac{-\theta_n}{\rho}} \times \mathrm{e}^{\frac{-\Phi_n}{\rho}}\right] \tag{16}$$

where $\Phi_n = \frac{\tau_p}{a_p^2}$, pdf of $P\left(\left|h_{b,s_n}\right|^2 < \frac{\theta_n}{\rho}\right) = \mathrm{e}^{\frac{-\theta_n}{\rho}}$ and $P\left(\left|h_{s_n,p}\right|^2 < \frac{\Phi_n}{\rho}\right) = \mathrm{e}^{\frac{-\Phi_n}{\rho}}$, respectively.

Substituting (14) and (16) into (13), gets outage probability of a PU as

$$P_{\text{out},p} = \prod_{n=1}^{N} \left[1 - \mathrm{e}^{\frac{-(\theta_n + \Phi_n)}{\rho}}\right] \times \left[1 - \mathrm{e}^{\frac{-\theta}{\rho}}\right] \tag{17}$$

3.3 Outage Capacity of SUs

From (12) can be simplified for an SU is to be expressed as

$$P_{\text{out},s} = 1 - \mathrm{e}^{\frac{-\eta}{\rho\lambda_{b,s}}} \tag{18}$$

At high ρ, assumed $\mathrm{e}^x = 1 + x$ the expression can be modified as

$$P_{\text{out},s} = \frac{\eta}{\rho\lambda_{b,s}}$$

The outage capacity of SUs depends on the value of τ_{s_n}, so that

$$\begin{aligned} P_{\text{out},s} &= \frac{\frac{\tau_{s_n}}{a_{s_n}^2}}{\rho\lambda_{b,s}} \\ P_{\text{out},s} \times \rho\lambda_{b,s} &= \frac{\tau_{s_n}}{a_{s_n}^2} \\ P_{\text{out},s} \times \rho\lambda_{b,s} a_{s_n}^2 &= 2^{C_{\text{out},s_n}} - 1 \end{aligned}$$

Therefore, outage capacity of SUs is written as

$$C_{\text{out},s_n} = \log_2\left(1 + P_{\text{out},s}\rho\lambda_{b,s}a_{s_n}^2\right) \tag{19}$$

3.4 Outage Capacity of PU

Similarly, from (17), expression can be rewritten as

$$P_{\text{out},p} = \prod_{n=1}^{N} \frac{\theta_n}{\rho} \tag{20}$$

where letting $\left[1 - \mathrm{e}^{\frac{-\theta}{\rho}}\right] = 1$, $\mathrm{e}^x = 1 + x$ and $\theta_n \gg \Phi_n$ at high ρ.

For simplicity taking $n = 1$, the expression can be defined as

$$P_{\text{out},p} = \frac{\tau_p}{\left(a_p^2 - \tau_p a_{s_n}^2\right)\rho}$$

where $\theta_n = \frac{\tau_p}{a_p^2 - \tau_p a_{s_n}^2}$.

$$\rho a_p^2 P_{\text{out},p} = \tau_p \left(1 + \rho a_{s_n}^2 P_{\text{out},p}\right)$$
$$\frac{\rho a_p^2 P_{\text{out},p}}{1 + \rho a_{s_n}^2 P_{\text{out},p}} = 2^{2C_{\text{out},p}} - 1$$

Thus, the outage capacity of a PU for $n = 1$ is to be illustrated as

$$C_{\text{out},p} = \frac{1}{2}\log_2\left(1 + \frac{\rho a_p^2 P_{\text{out},p}}{1 + \rho a_{s_n}^2 P_{\text{out},p}}\right) \tag{21}$$

Now, outage sum capacity of given system is to be represented as

$$C_{\text{out,sum}} = C_{\text{out},p} + C_{\text{out},s_n} \tag{22}$$

4 Results and Discussion

BS and PU lie at center (0, 0) and edge (1, 1) of the cell simultaneously, and N SUs are distributed in between them. The channel gain $\lambda_{j,k} = d_{j,k}^{-\xi}$ with $\xi = 3$ and $d_{j,k}$ defines the path loss factor for urban areas and normalized distance between (j, k) nodes, respectively. Taking $C_{\text{out},p} = C_{\text{out},s_n} = 0.5$ bps/Hz along with associated $a_p^2 = 0.86$ and $a_{s_n}^2 = 0.14$ coefficients.

Figure 2 shows the comparison between proposed CNOMA and orthodox OMA through DF technique of relaying in given CRNs. The related figure depicts the analyses results which are equal to the simulated solutions. Simultaneously, the proposed CNOMA provides outstanding behavior over OMA which is being offered in Fig. 2. Outage behavior of PU and SUs is continuously enhanced and reduced with the rising value of ρ, respectively. The intersection point on outage probabilities curves of SUs and PU represents the approximate assignment powers to SUs (14%) and PU (86%) at ($\rho = 10$ dB) of the total system power, respectively. Therefore, PU behaves well than SU and OMA also, as given in Fig. 2.

The outage sum capacity of CNOMA and OMA has been depicted through Fig. 3 w.r.t. different values of ρ. Moreover, outage capacity of PU under CNOMA is gradually enhanced initially then becomes constant along ρ due to presence of noise

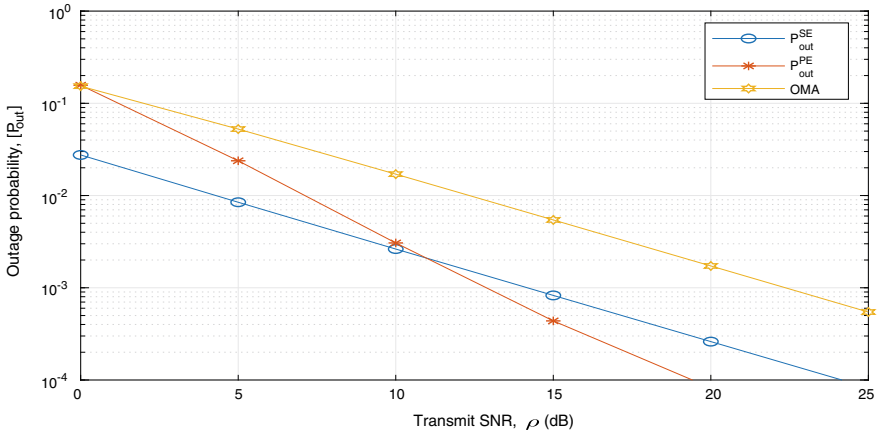

Fig. 2 Impact of outage on the proposed CNOMA and OMA in DF technique with power allocation coefficients, $a_p^2 = 0.86$ and $a_{s_n}^2 = 0.14$ and target rates, $C_{\text{out},p} = C_{\text{out},s_n} = 0.5$ bps/Hz for PE and SE, respectively

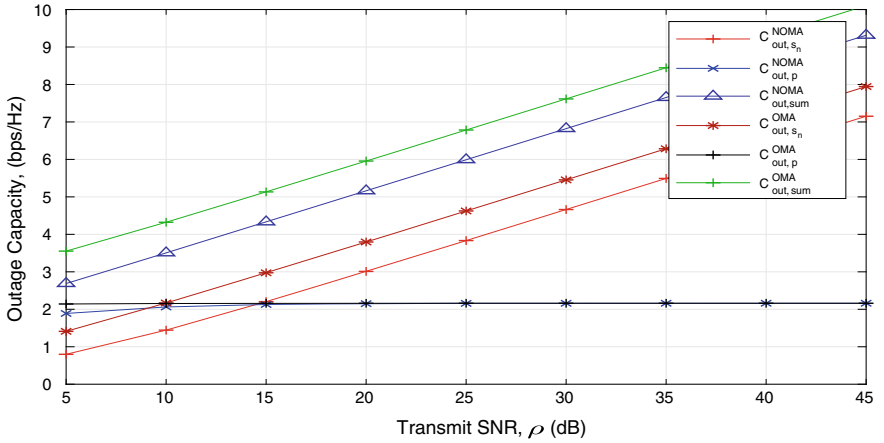

Fig. 3 Comparing impact on outage capacities of CNOMA and OMA with $a_p^2 = 0.86$, $a_{s_n}^2 = 0.14$ and $C_{\text{out},p} = C_{\text{out},s_n} = 0.5$ bps/Hz for PE and SE, respectively

in the denominator as compared to OMA. The outage capacities of both PU and SUs increase along ρ under CNOMA but behaves much better than the existing orthodox OMA technique, as shown in Fig. 3. Thus, the outage sum capacity of CNOMA shows outstanding behavior over OMA.

5 Conclusion

This paper concludes that the outage probabilities and capacities of SUs, as well as a PU for the given CNOMA, outperform over orthodox OMA with implementing DF relaying technique in CRNs, respectively. The closed-form solutions of outage capacity and probabilities are also discussed along with the comparison of sum capacity of the system as mentioned earlier to OMA technique through simulation results.

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Performance Comparison of FinFET-Based Different Current Mirror Topologies

Monika and Poornima Mittal

1 Introduction

The current mirror (CM) is an accomplished and significant part of analog circuits. It produces a mirror image of an input current at a high impedance output node [1]. A current mirror can be find in various applications such as active load, current amplifier, current source, biasing in operational transconductance amplifiers (OTAs), operational amplifiers (Op-amps), operational mirrored amplifiers, analog filters, current conveyors, current-feedback op-amps, digital-to-analog converters, and analog-to-digital converters, etc. [2–4]. Thus, CM plays a crucial role in these integrated circuits. Performance criteria of current mirrors which are also essential are bandwidth, input/output compliance voltage, output resistance, input resistance and accuracy [1]. One of the current mirror's parameter i.e. accuracy can be defined as how much a precise copy of input current mirrored to the output and it can be given as a ratio which is called percentage error ratio (PER), whereas, the input/output compliance voltage is represented as the minimum voltage at the output of a current source while it attempts to produce the desired matched current.

Utmost performance requirement of the current mirror includes a high accuracy which is essential for many applications like bio amplifiers, implantable micro stimulators and biomedical circuits [4]. However, Bluetooth filters, operational amplifiers, universal bi-quad filters and biomedical circuits require low compliance voltage CMs and used in low-voltage applications [5]. Current mirrors that have high output resistance and low input resistance are used to minimize the loading effect, and this proficiency can be used to improve power supply rejection ratio, DC gain and common-mode rejection ratio which is a crucial factor for differential input pairs [1,

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6]. Further, current mirrors with high bandwidth required in high-speed circuits such as high-speed current-mode amplifiers, current steering digital-to-analog converters, current conveyors, etc. [2, 7]. Many CMs have been reported earlier in the literature with improvements of different parameters. Low compliance voltage has achieved in low-voltage cascode CM, high swing cascode current mirror, etc. [8, 9]. Whereas, higher output resistance has seen in active feedback CM, regulated cascode CM, self-cascode MOSFET CM, etc. [1, 10].

Due to the three-dimensional (3-D) structure of FinFET, it has superior control over the drain–source channel and leakage current which is the main reason behind short channel effects (SCEs). Also, using near-intrinsic channel doping can be further improving threshold voltage variation which provoked due to random dopant fluctuations [11, 12]. Various digital applications like multiplexers are designed in the literature and compared with CMOS technology [13, 14]. Still, there are much advancement which enhanced in layout and technology of CMOS logic, pass transistors logic, etc., and all these techniques are used with different technology node for low power and low-voltage applications [15–17]. Therefore, in this paper, different CM topologies based on FinFET are designed and analyzed in terms of accuracy, output compliance voltage and output resistance.

This paper is arranged in a total of four sections with the current introduction as Sect. 1. Further, schematics and characteristics of different current mirrors are discussed in Sect. 2, whereas the analysis results are illustrated in Sect. 3. Finally, important outcomes are summarized in Sect. 4.

2 Schematic Diversity for Current Mirror

In this section, figure of merit (FoMs) of CM, i.e., percentage error ratio (PER), output compliance voltage and output resistance will be discussed. The PER is given as

$$\frac{I_{\text{out}} - I_{\text{in}}}{I_{\text{in}}} \times 100\% \tag{1}$$

Reciprocal of output current's derivative gives output resistance. The voltage where the output current is similar to input current is called as output compliance voltage. For better performance, it should be low because it gives a higher compliance range. The voltage $V_{\text{DG-OUT}} = 0\,\text{V}$ will maintain the output transistor in saturation. Thus, for accurate mirroring behavior, output voltage should be

$$V_{\text{OUT}} = V_{\text{CV}} = V_{\text{GS-OUT}} = V_{\text{DS-OUT}} \tag{2}$$

where V_{CV} is output compliance voltage, and $V_{\text{GS-OUT}}$ and $V_{\text{DS-OUT}}$ represent gate–source voltage and drain–source voltage of output leg of circuit, respectively.

The basic topology of CM based on FinFET is shown in Fig. 1a, wherein the

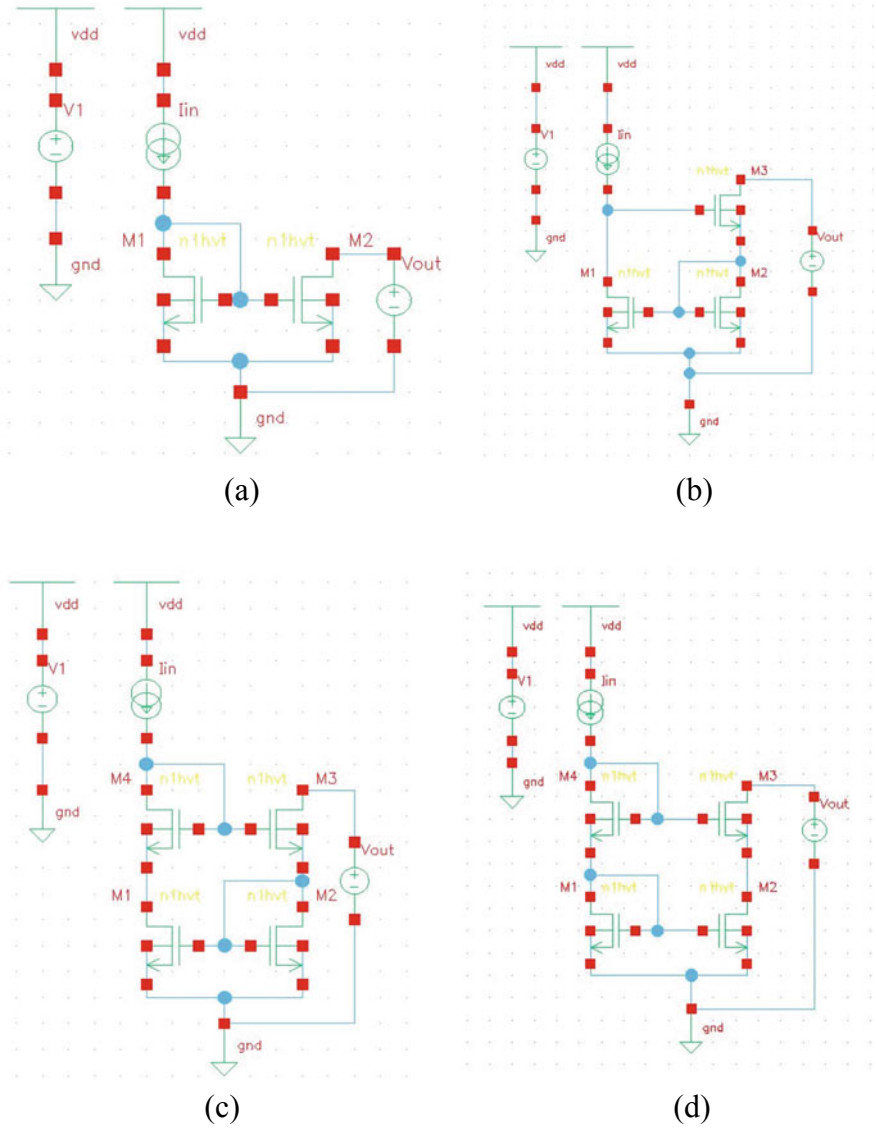

Fig. 1 Topologies of basic current mirror; **a** Conventional, **b** Wilson, **c** Improved Wilson and **d** Cascode

channel current for both transistor M1 and M2 is equal, if the gate–source voltage of two matched FinFET devices is equal. Here, transistor M1 acts as the reference transistor and M2 as the mirroring transistor. To carry out the current mirroring (i.e., $I_{d1} = I_{d2}$), both the transistors must remain in saturation, and their lengths should also match ($L1 = L2$). The conventional current mirror can be achieved from two

transistors in which one transistor has diode connection and the second transistor is current sourced by a diode-connected transistor. The diode connection provides basic gate–source voltage to the output transistor. When the aspect ratio of M2 is greater than M1, then CM amplifies the input current [1].

Further, the output current (M2's drain current) is comparable to the input current (M1's drain current), if M1 and M2 run in the saturation region. Similar to MOSFET-based current mirror, in FinFET CM, the circuit will work as an amplifier if the aspect ratio of M2 is greater than M1. The transistor should work in a saturation region to exhibit a good current source. Though a better matching accuracy is achieved for conventional CM, a lower output resistance is obtained. Hence, here trade-off can be seen between accuracy and output resistance. For further increased accuracy, we move toward different CM topology, which is called Wilson CM (Fig. 1b). Wilson current mirror circuit derived using three FinFETs and gives copied value of input current at output side. In this architecture, transistor M3 provides a shunt-series type negative current feedback which gives higher output resistance than conventional CM. Here, it is observed as a drawback that Wilson current mirror generates large input and output voltage while it should be minimum:

$$V_{o\ \min} = V_{\mathrm{Th}} + 2V_{\mathrm{DS\ sat}} \tag{3}$$

$$V_{i\ \min} = 2V_{\mathrm{Th}} + 2V_{\mathrm{DS\ sat}} \tag{4}$$

Also, it is noticed that the V_{DS} of M1 and M2 are not equal as a result of channel length modulation, which should be equal. This drawback is going to be the cause of erroneous current gain. To fix this, balanced Wilson CM is designed by Wilson [18], as shown in Fig. 1c, and Schlotzhauer and Viswanathian [19] used it as a four MOSFET current mirror. And it is labeled as improved Wilson current mirror by Hart and Baker [20]. The key idea for enhancing the accuracy in improved Wilson CM is to add diode-connected transistor (M4) in the input branch to even up the drain–source voltage of the primary current mirror pair [1]. By doing so, it is found that output resistance, compliance voltage and input resistance are similar to Wilson current mirror. The output resistance for these two current mirrors is given as

$$r_{\mathrm{out}} \approx \frac{g_{m1} r_{o1} g_{m3} r_{o3}}{g_{m2}} \tag{5}$$

It has been realized that using more numbers of transistors results in enhanced performance of the current mirror and also a higher number of transistors causes' increased parasitic capacitance. For better accuracy and performance, cascode current mirror is structured as demonstrated in Fig. 1d [1]. Cascoding both branches of the conventional current mirror will generate the Cascode current mirror. V_{BS} of transistor M3 and M4 is used for calculating the input and output resistance. M3 and M4 are used to balance the V_{DS} of M1 and M2. Due to cascoding current mirroring, accuracy can be seen here. Hence, the channel length modulation effect

and imbalance of input–output voltage do not affect the current gain. Errors which produced during process variation, can't be changed and hence they can be improved using perfect layout of design and matched design. For efficient matching and high r_{ds}, M1 and M2 are optimized, and for a broad range of transconductance, M3 and M4 are sized. Its output resistance is given as

$$r_{out} = r_{03} + r_{02}(1 + r_{03}(g_{m3} + g_{mb3})) \tag{6}$$

Its output compliance voltage is $2V_{DS,sat} + V_{Th}$. It is observed that Wilson and improved Wilson current mirror's compliance voltage are identical to cascode current mirror, and it is increased by V_{th}, which is higher than the minimum voltage. Further improvement in performance and resistance can be developed by using double cascode current mirror. The nearest value of output resistance for double cascode CM is given as $(g_m r_0)^2\, r_0$, and also, it leads to higher voltage headroom. Despite its better higher output resistance, larger bandwidth and higher accuracy, the higher voltage headroom cannot be ignored because of modern low voltage application [1].

3 Simulation Results

Here, characteristics of all basic topologies of current mirror circuits, using the Cadence Virtuoso simulation tool at 18 nm FinFET, have been plotted. For comparison, all topologies carried out with similar conditions. With V_{dd} of 1 V, input current source with 10 μA and DC output voltage source of 1 V, all the circuits have been simulated. Here, the fin length of FinFET is 18 nm. In DC analysis, input current I_{in} is varied over a range of 0–500 μA, and the output voltage V_{out} swept for 0–5 V.

Figure 2a shows current transfer characteristics for all topologies, and their percentage error ratio (PER) is presented in Fig. 2b. It is examined from the plot that the mirroring accuracy of a Wilson and improved Wilson is quite poor and better accuracy is found in conventional CM and cascode CM. Here, the matching accuracy is found improved for a very low voltage range but after a certain range it is started to degrade. I_{out} versus V_{out} characteristics are displayed in Fig. 2c. It is observed that lower output compliance voltage (at $i_{IN} = 10$ μA) is seen in conventional CM and it gets worse in Wilson CM. Figure 2d shows frequency versus output resistance curves (at $i_{in} = 10$ μA) for these current mirrors. It is observed in FinFET-based CMs, and output resistance decreases at the cost of increased accuracy. Table 1 shows the compared data of all these current mirrors, and it shows that accuracy is obtained at the cost of lower output resistance.

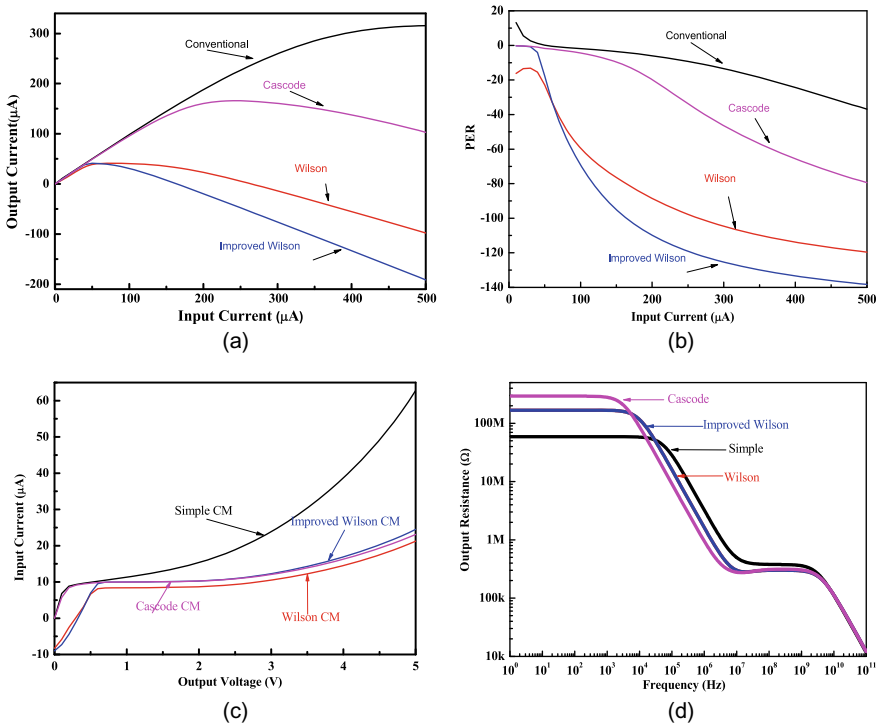

Fig. 2 Comparative results for current mirrors, **a** basic current mirror's input–output current characteristics, **b** percentage error ratio (PER) curves, **c** I_{out} versus V_{out} plot at $i_{in} = 10\ \mu A$, **d** frequency versus output resistance curves at $i_{in} = 10\ \mu A$

Table 1 Comparative data for basic current mirror topologies

S. No.	Parameter	Conventional	Wilson	Improved Wilson	Cascode
1	Mirroring_accuracy[a]	Great	Good	Poor	Poor
2	% Error ratio (PER)[b]	13.17	−16.17	−0.189	−0.19
3	$V_{out,min}$[a](V)	0.4–0.6	2.7–2.9	0.6–1.2	0.7–1.2
4	Output resistance[b] (MΩ)	58.9	168	168	293

[a]I_{in} range = 0–500 μA
[b]At $I_{in} = 10\ \mu A$

4 Conclusion

Detailed current mirrors topologies and simulations have been done on Cadence Virtuoso in 18 nm FinFET technology node. All current mirrors parameters defined plot have been shown, and their analyzed data tabulated. It has been detected that major accuracy has seen in a simple current mirror and cascode CM, while higher

output resistance has been obtained from Wilson and improved Wilson CM. It has been also concluded that FinFET CM is only suitable for low current range, and for higher current, it contributes a lot mismatch. Further, it is noticed that in CMOS current mirror the accuracy is dependent on the number of transistors such as transistor is increased in the structure the accuracy is found more improved. But this kind of trend is not seen in FinFET CM.

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Two-Element Composite Dielectric Resonator-Based MIMO Antenna for WLAN and WiMAX Application

Shivani Anand, Gagandeep Bharti, and Anand Sharma

1 Introduction

The MIMO technique in the present time is used considerably for wireless communication. It will be used in future technology because of its several benefits. MIMO technology uses multiple antennas for wireless point [1]. MIMO technology plays an important role in achieving high data level, and optimizing performance for most advanced wireless communication network, a substantial improvement in channel capacity may be accomplished without the need for extra bandwidth or more transmitting power by installing such a MIMO system [2]. Ishimiya first identified and demonstrated the principle of MIMO DRA [3]. In recent year, DRA have gained a lot of interest due to their high efficiency, small size, easy excitation, and large impedence bandwidth. DRA has also shown good performance in MIMO [4]. The first candidate identified as the dielectric resonator antenna (DRA) was cylindrical dielectric resonator antenna (CDRA) in 1983 [5]. The compact and multiband DRA for mobile portable device for WiFi, LTE, and WiMAX available as two dielectric resonator are used, but there are large ground size and high mutual coupling value especially the higher band [6]. Wireless LAN (WLAN) is a wireless computer network that connects two or more computer used for wireless communication which can establish a local area network (LAN) in a restricted area such as a home, school, computer laboratory and office. The proposed 8-port diversity antenna is suitable for WLAN application in the frequency range between 5.6 and 5.9 GHz [7]. WiMAX is

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a wireless broadband networking technology based around the IEEE802.16 standard that requires high-speed data around a wide area, WiMAX stand for worldwide interoperability for microwave access, and it is a point to multipoint wireless networking system. A CDRA with circular ring patch fed is proposed which is perfect for the WiMAX, WLAN, 3G, and Amateur Satellite [8]. LTE band 22 is a part of the FDD (frequency division duplex) LTE spectrum that has different uplink and downlink frequency where lower band frequency range is (698–966 MHz), middle band range is (1.42–2.69 GHz), and higher band range is (3.4–3.8 GHz) [9].

2 Layout of Antenna

The layout of proposed antenna is shown in Fig. 2 which is drawn by the dimension of $50 \times 100\,\text{mm}^2$. The substrate is FR4 with thickness 1.6 mm and dielectric constant 4.4 alumina (Al_2O_3) based material is used for ring dielectric resonator. The ring DRA is placed above the substrate. In the middle of the ring, DR was placed a second ring DR of Teflon material which is 6.00 mm length, and third cylinder-shaped DR was placed on the top of it. Figure 1 show a circle is cut on the ground plane, and a small circle is placed in that severed circle just below the ring DR to generate circular polarization and the gun shaped microstrip feed line is mounted on the lower surface of the ground, and all dimension of proposed antenna is given in Table 1 and geometry in (Figs. 2 and 3).

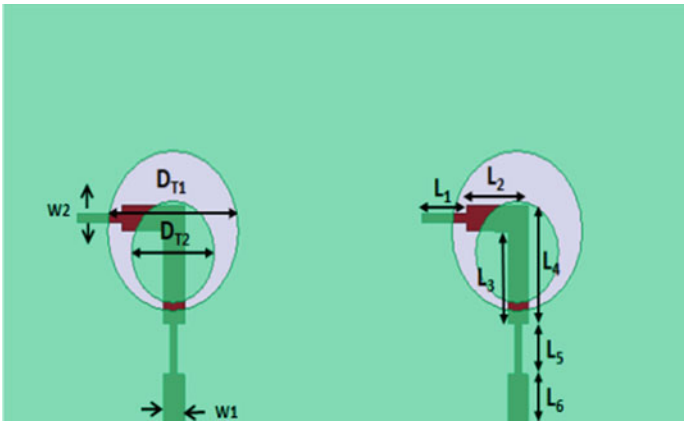

Fig. 1 Layout of antenna: the ground plane

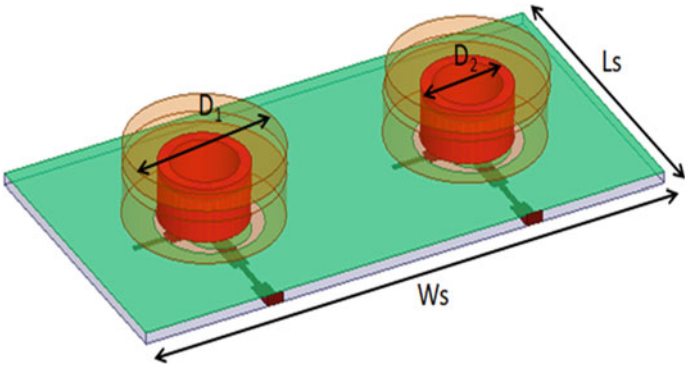

Fig. 2 Layout of antenna: front view

Table 1 Antenna dimension

Symbol	Value (mm)	Symbol	Value (mm)
L_S	50.0	L_4	14.00
W_S	100.0	$L_5 = L_6 = H_2$	6.00
H	1.60	H_1	2.50
D_1	28.00	W_1	3.00
D_2	12.00	G_1	1.50
L_1	6.5	G_2	7.50
L_2	9.00	D_{T1}	19
L_3	11.00	D_{T2}	12
L_4	14.00	W_2	1.00

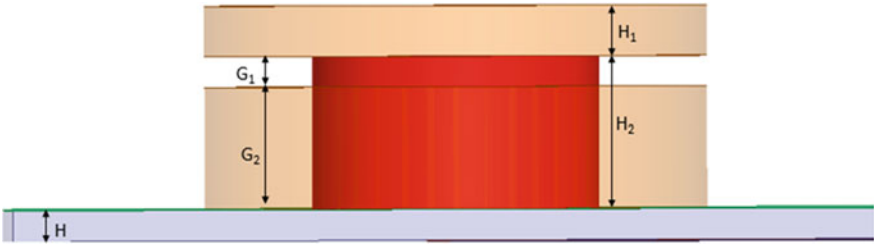

Fig. 3 Layout of antenna: side view

3 Evolution of Antenna

The proposed antenna is designed step by step and the proposed antenna with different configuration is studied step by step. Circle-shaped slot in infinite ground plane

cut and a second small circle in middle of circle and microstrip feed line are used to enhance the isolation, and ring dielectric resonator are used to enhance impedence bandwidth. Stimulation and antenna analysis has been done through HFSS software [10]. Figure 4 shows the evolution of antenna, the first antenna (a) introduced gun-shaped microstrip feed line and a circle shaped slot. It achieves better performance in band return loss $|S_{11}| < -20$ dB; (b) shows that the cylinder DR is placed on top of the substrate which provides better isolation; (c) displays that the cylinder DR is replaced in a ring DRA that generates a band where frequency range is 5.2–5.9 GHz; (d) the proposed antenna produces dual orthogonal mode in composite DRA that enable to achieve dual frequency operation 3.1–4.1 GHz and 5.2–5.9 GHz. Figure 5 displays the impedence bandwidth $|S_{11}/S_{22}|$ changes for different condition, first of which show without DRA that achieve only one band, the band that has come does not appear in any application. Second is with cylindrical DRA for that good isolation is not obtained. Third is a ring-shaped DRA that generates one band, and this band is standard WLAN band. Fourth presented proposed antenna achieves two band 3.1–4.1 GHz and 5.2–5.9 GHz that is useful for WLAN, WiMAX, and Amateur satellite application [8]. Figure 6 illustrates that the variance of the isolation between the two antenna ports in four different conditions (1) shows the without DRA, (2) is with cylindrical DRA, (3) is a ring-shaped DRA, and (4) is presented proposed antenna. The use of DGS in the two-port radiator structure has been said to increase the efficiency of the isolation performance in the lower frequency band up to 20 dB. Similarly isolation in the upper band has been enhanced by taking replica of the modified semi-circle-shaped aperture more than 30 dB.

Figure 7a shows the result of the average gain is more than 4 dB. In radiation

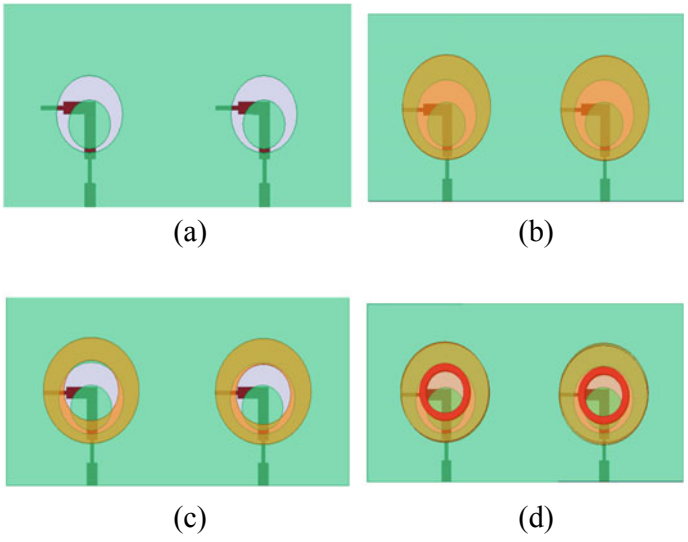

Fig. 4 Evolution of proposed antenna

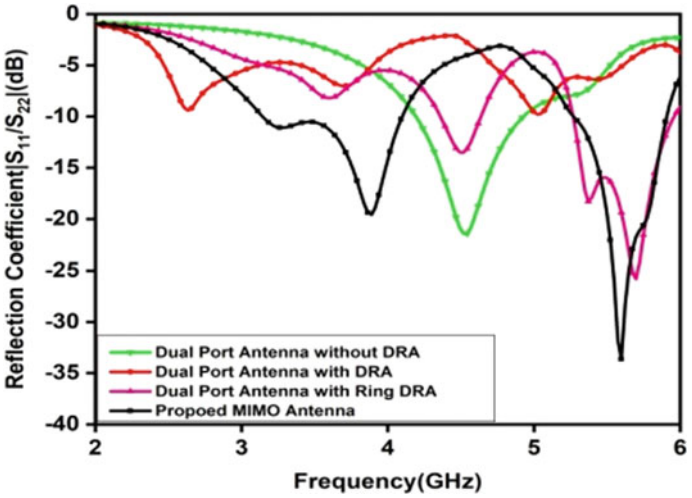

Fig. 5 Evolution of proposed antenna impedance bandwidth (dB)

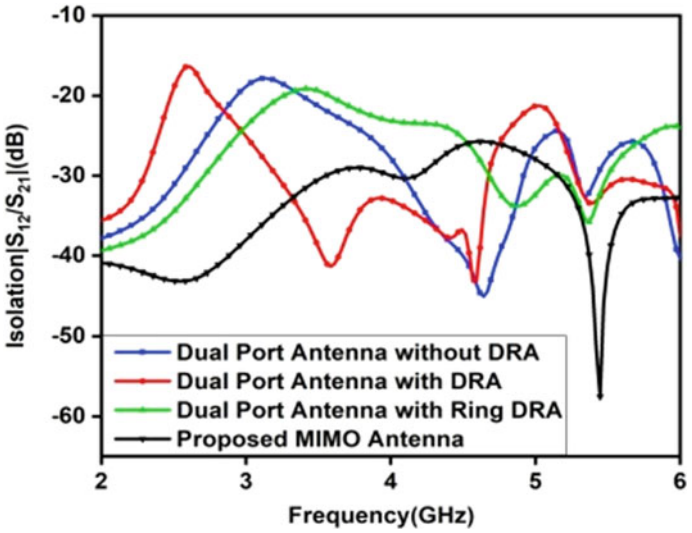

Fig. 6 Evolution of proposed antenna mutual coupling

efficiency, the radiation efficiency is higher than 92%. Figure 7b shows that axial ratio is (circularly polarized) frequency AR $\leq$ 3 dB bandwidth is (3.1–3.3 GHz).

Figure 8a the simulated impedance bandwidth $|S_{11}| \leq -20$ obtained from (3.1–4.1) GHz and (5.2–5.9) GHz. Figure 8b all the ports cover the frequency band between 3.1–4.1 GHz and 5.2–5.9 GHz. Improved isolation (better than 20 dB).

Figure 9a, b displays the composite ring DR two resonance peak electric field

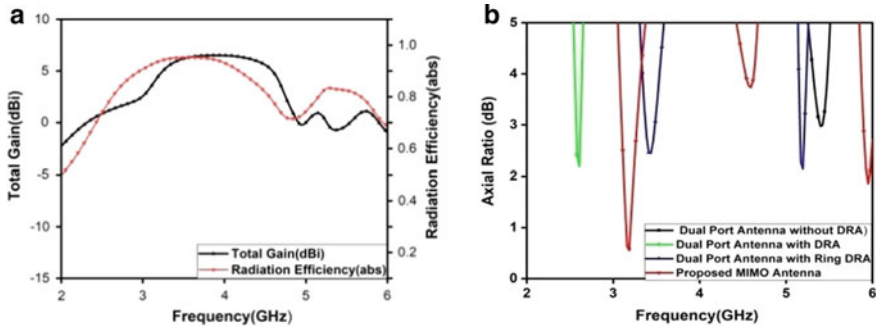

Fig. 7 **a** Antenna gain and antenna efficiency of proposed antenna. **b** axial ratio

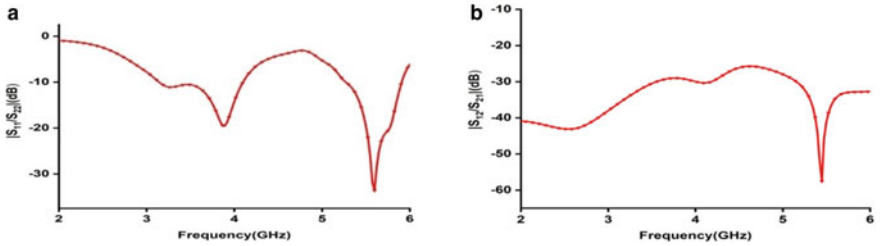

Fig. 8 **a** Simulated reflection coefficient $|S_{11}/S_{22}|$ dB. **b** Simulated isolation $|S_{12}/S_{21}|$ dB

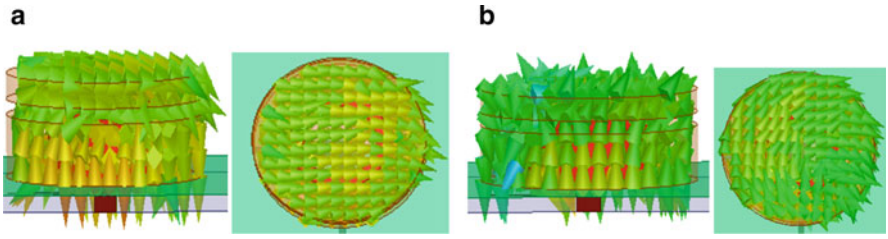

Fig. 9 **a** Near-field distribution on cylindrical. **b** DRA in equatorial plane and meridian plane at 3.88 and 5.59 GHz

distribution at 3.88 and 5.59 GHz which is created due to the generation of orthogonal mode within the composite ring DRA, shows the top view of cylindrical DRA is absorbingly the horizontal *E*-field line on top of DRA, and shows the side view of composite ring DRA is vertical *E*-field line on side view DRA.

Figure 10a, b depicts the current distribution at 3.88 and 5.59 GHz; it shows maximum current at the feed line. Figure 11 show radiation pattern in *XY*-plane at ($\phi = 0°$) and ($\theta = 0°$) due to port 1 and port 2. Radiation pattern of proposed antenna in *E*-plane and *H*-plane at different resonant frequency is shown in Fig. 11 in *XY* plane radiation pattern calculate the strength of the EM waves (Table 2).

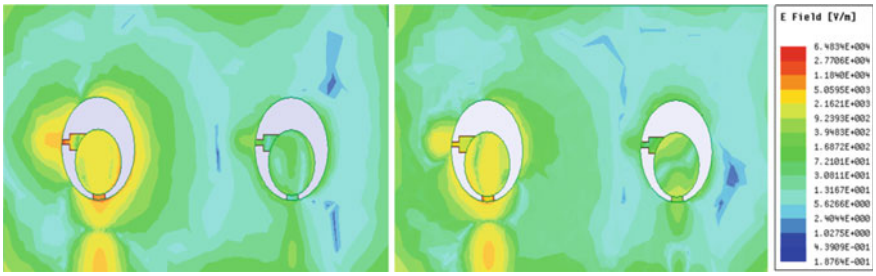

Fig. 10 Behavior of surface current distribution of the antenna at 3.88 and 5.59 GHz

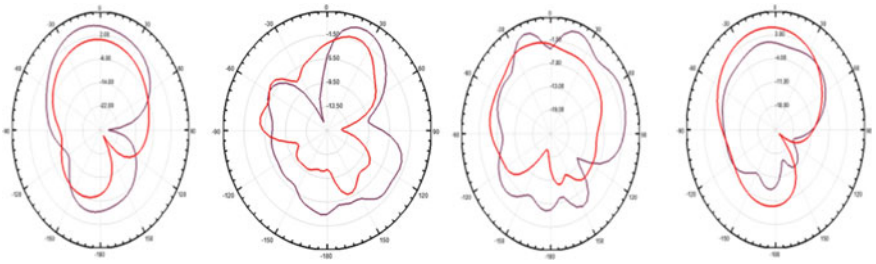

Fig. 11 Radiation patterns of antenna at 3.88 and 5.59 GHz

Table 2 Comparison of proposed multi-input multi-output antenna with other two-port MIMO antenna on the basis of isolation, antenna shape, feed line, and application

References	DRA shape	Feed	Frequency range (GHz)	Application	Isolation
[11]	Cylindrical DRA	Microstrip feed line	2.2–2.3, 2.5–3.2, 4.8–7.8	WLAN, WiMAX LTE	<−20
[1]	Cylindrical DRA	Microstrip feed line	2.4–2.8, 5.3–5.8	WLAN	<−20
[12]	Rectangular DRA	Metallic strip feed line	3.3, 5.2	WiMAX, WLAN	<−16
[7]	Cylindrical DRA	Microstrip feed line	5.6–5.9	WLAN	<−20
[13]	Ring-shape DRA	Aperture	2.3–2.9, 3.4–4.0	WLAN, WiMAX	<−20
[14]	Ring-shape DRA	*U*-shape metallic feed line	3.3–3.6 GHz, 5.2–5.8 GHz	WiMAX, WLAN	<−18
Proposed antenna	Composite ring shape	Microstrip	3.1–4.1, 5.2–5.9	WLAN, WiMAX	<−30

4 Conclusion

In this article, a composite DR based MIMO is designed for WLAN standard (5.6–5.9 GHz), WiMAX (3.3–3.6 GHz), LTE higher band (3.4–3.8 GHz), and Amateur satellite (5.6/5.8 GHz) application. Dual bandwidth is achieved by composite ring DRA and semi-circle slot in infinite ground plane that achieves dual frequency band 3.1–4.1 GHz and 5.2–5.9 GHz, and CP range is 3.1–3.3 GHz. Total gain and radiation efficiency of this MIMO antenna are 4 dB and 92%, respectively. The proposed antenna can bea used in applications of upper frequency band of WLAN, WiMAX, LTE, and uplink/downlink of Amateur satellite (5.6/5.8 GHz).

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Heat Flow Modeling of Breast Tumor

Jaswantsing Rajput, Anil Nandgaonkar, Sanjay Nalbalwar, and Abhay Wagh

1 Introduction

Cancer causes cells to divide uncontrollably. It also prevents them from dying at a natural point in their life cycle. Breast cancer and lung cancer in women have been on the rise in the last four decades. The incidence of breast cancer alone is 11.6% worldwide [1]. Breast cancer incidence rates have gone up slightly, by about 0.3% per year, since 2004. However, the survival of patients after treatment has improved since the mid-1970s for all of the most common cancers. In addition to surgery, there are many other options available to treat breast cancer. Effective use of radiofrequency (RF) waves on tumor position is widely used, while treating breast cancer. Hyperthermia treatment (HT) along with chemotherapy or radiotherapy is beneficial for the treatment of breast cancer. Hyperthermia causes breast tumors to shrink and make them easier to remove surgically [2]. Combined treatment is a major contributor to the decline in breast cancer mortality. Between 1989 and 2017, the death rates of breast cancer patients have been dropped by 40% [3]. This steepest decline in cancer deaths occurred for breast cancer, because of improvements in the focusing techniques of RF waves, microwaves, and ultrasound waves used in radiotherapy. The use of fully developed, and advanced antenna beamforming techniques for hyperthermia therapies have played a significant role in reducing the mortality rate of breast cancer patients. Many scientists worldwide are working for the development of highly advanced wireless technique for the application of RF energy on tumors [4]. The selection of frequency, antenna array, focusing technique, and treatment time is dependent on the tumor stage and site. When treating hyperthermia, it is important to keep the temperature of the tumor above 42 °C and the temperature

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of the surroundings to 37 °C. For effective control of temperature, and heat in the tumor site, tissue characteristics of tumor site and surroundings should be studied properly to avoid hotspots on healthy tissues [5].

Before HT, investigations are carried out using a computerized tomography (CT) scan to find the detailed location, size, depth, and other dimensions of the tumor. These parameters are used for the proper selection of treatment period, RF energy amplitude, phase, focusing methodology, types of antennae array required for HT of tumors [6]. Different types of antenna applicators, antennae arrays are used according to the stage, site location, and size of the tumor. Microstrip array antennas, Lucite cone applicators, are widely used in local HT and superficial HT [7, 8]. The best results are obtained when three-dimensional focusing methodology is used for breast tumors treatment, at microwave frequency [9, 10]. The temperature of the tumor and surrounding tissue is measured using thermometer probes. Its constant monitoring is essential to maintain flow of radiation power inside the tumors avoids excessive heating of tumor and surrounding tissues. Figure 1 shows a simple module of RF energy focusing on breast tumors. Two tumors inside the breast are treated by hyperthermia using RF energy. For achieving the highest focusing on tumor, perfect electromagnetic coupling, and avoid reflection of RF power, water bolus is used for microwave hyperthermia.

The simulation of electrostatic breast model is performed and the discretization of the entire model into small finite elements has been done with finite element method (FEM) on COMSOL Multi-Physics Solver Simulator. In the 2D electrostatic modeling, database for breast tissue characteristics [11, 12] is considered, and two tumors of 5 mm size are inserted into the electrostatic model of breast having a

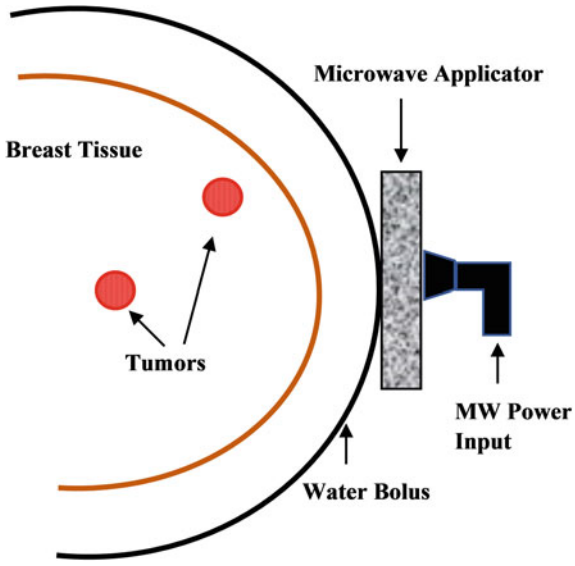

Fig. 1 Focusing of RF energy on breast tumors

diameter of 160 mm. Section 2 describes this detailed modeling. All results are described in Sect. 3. The concluding remarks are discussed in Sect. 4.

2 Heat Flow Modeling of Breast Tumor

The flow of heat due to thermal conduction is expressed by (1),

$$f = -k\nabla T \tag{1}$$

where f—heat flux vector, k—thermal conductivity coefficient, and $-\nabla T$—vector quantity.

To obtain optimum focusing results, we have studied the flow of heat between control volumes inside the breast tumor tissue and the tumor's surroundings inside the breast. In the modeling, the contribution from intrinsic radiative heat transfer processes is considered as negligible. Heat flows inside the tumor or normal tissue by two mechanisms: conduction, which means the inner temperature gradient, which drives the heat flow, and another way is through convection of thermal energy by the perfusing blood. In 1948, Pennes [13] described the relationship between thermal heat transfer and blood perfusion for healthy tissue (2), and tumor domain (3), which has been used for heat flow modeling. The computational time is optimized for a higher amount of heat flow inside the tumors [14]. Convection is the transfer of thermal energy through a fluid due to the fluid's bulk motion, and radiation is the transmission of RF energy in the form of RF waves. These two boundary conditions are solved by FEM. The FEM is used to solve numerical approximations of the equation with a close boundary conditions for radiation and convection.

$$\rho_1 c_1 \frac{\partial T_1}{\partial t} = \nabla(k_1 \nabla T_1) - \omega_{b1} c_{b1}(T_1 - T_b) + Q_{m1} + \alpha P \tag{2}$$

$$\rho_2 c_2 \frac{\partial T_2}{\partial t} = \nabla(k_2 \nabla T_2) - \omega_{b2} c_{b2}(T_2 - T_b) + Q_{m2} \tag{3}$$

where, tissue density, specific heat, and thermal conductivity of breast tissue are denoted by ρ, c, and k, respectively. $T_1 T_2$ and T_b denotes the temperature of the tumor, normal tissue, and blood, respectively. c_b and ω_b denotes blood perfusion rate, and temperature, and Q_m, α, and P denotes metabolic heat per unit volume, correction parameter, and dissipated power per unit volume, respectively. The change in magnitude of electric flux density, electric field intensity around the breast tumor surface, and distribution of heat flux density in breast model has been described in Sect. 3.

3 Results and Discussion

Heat flow modeling for optimum and deeply penetrated focusing of RF energy on breast tumor tissue has been carried out using an electrostatic model. This model attains maximum focusing of RF energy on tumor tissue and keeps surrounding tissue safe. From the obtained results of electrostatic modeling of breast tumors, it is clear that the magnitude of focusing RF power is more at tumor site only, that has been shown in terms of electric field distribution around the tumor surface, and the magnitude of electric flux density inside the tumor surface in Figs. 2 and 3, respectively.

For achieving higher accuracy, the flow of heat should be maximum, deeply penetrated inside the breast tumor than surrounding tissues of the breast tumor. The outcomes of this modeling give optimistic temperature distribution inside the breast tumor. This modeling gives higher and deep penetration of RF energy inside the breast tumors. The distribution of heat flux density plot in Fig. 4 shows the maximum amount of heat dissipation around the tumors, whereas its minimum inside the other area of the breast.

The optimum and deep temperature distribution around the tumor inside the breast have been shown with the help of temperature gradient distribution plot in Fig. 5, and the temperature distribution plot in Fig. 6.

The temperature gradient plot in Fig. 5 shows the highest concentration of temperature around the tumors, and the equipotential line plot for the same has been shown in Fig. 6. Simulation results obtained for the different known boundary conditions

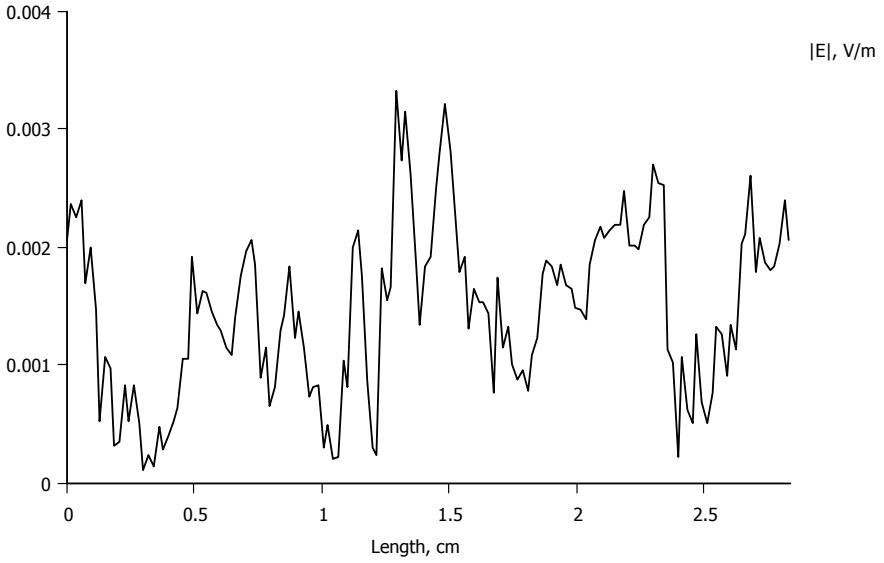

Fig. 2 Variations of electric field intensity around the tumor

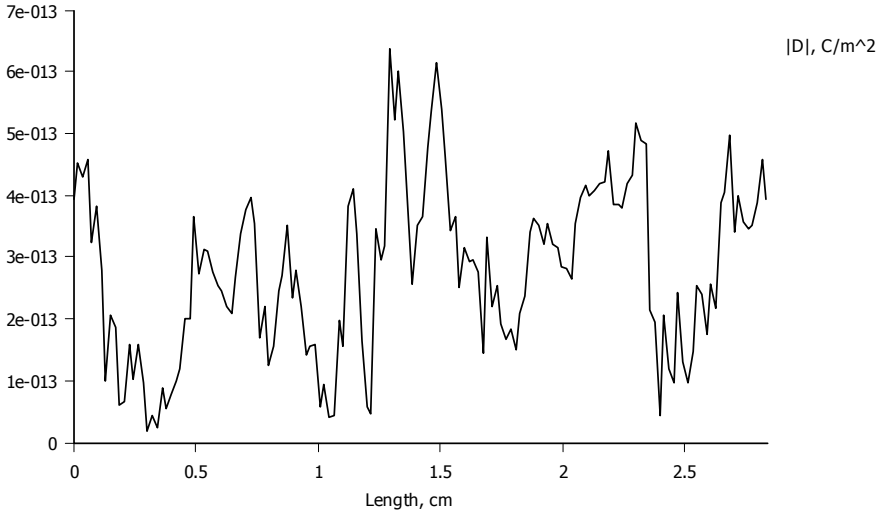

Fig. 3 Variations of electric flux density inside the tumor

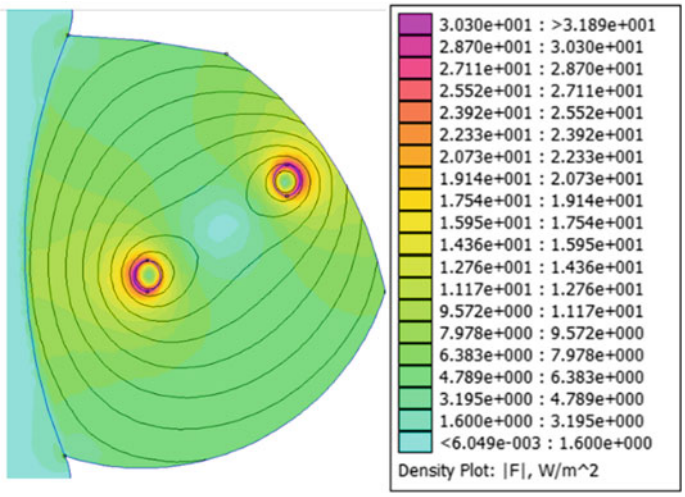

Fig. 4 Distribution of heat flux density in breast model

show that optimum focusing of radiation power around the tumor inside the breast has been given higher efficiency of hyperthermia treatment. The simulation results are useful for the improvement of hyperthermia treatment of breast cancer patients, with minimal damage to normal cells. The stored electric field intensity magnitude around the first and second tumor surface is shown in Figs. 7 and 8, respectively. The obtained results show that the stored energy inside these two breast tumors in

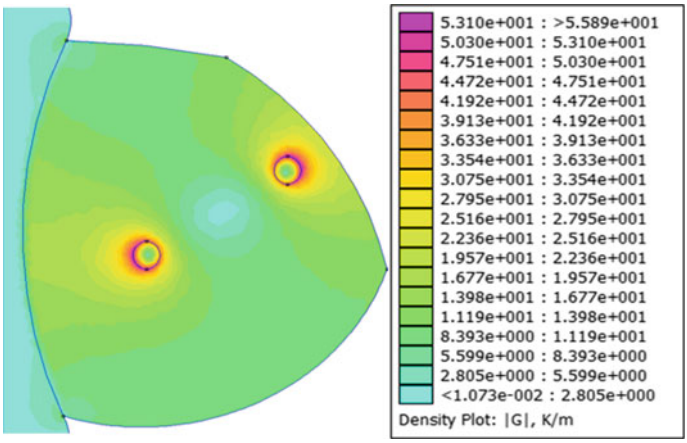

Fig. 5 Temperature gradient

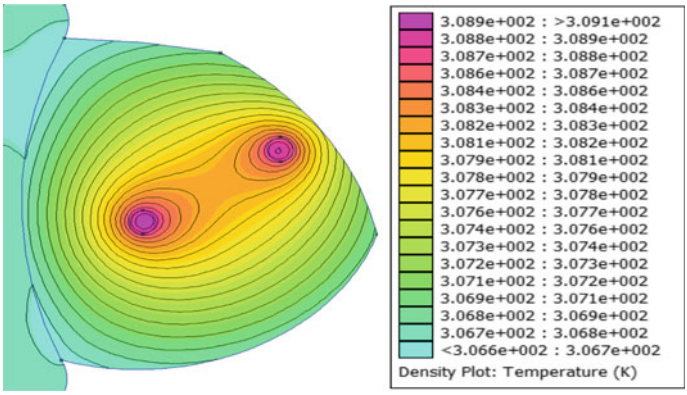

Fig. 6 Two tumors with temperature distribution

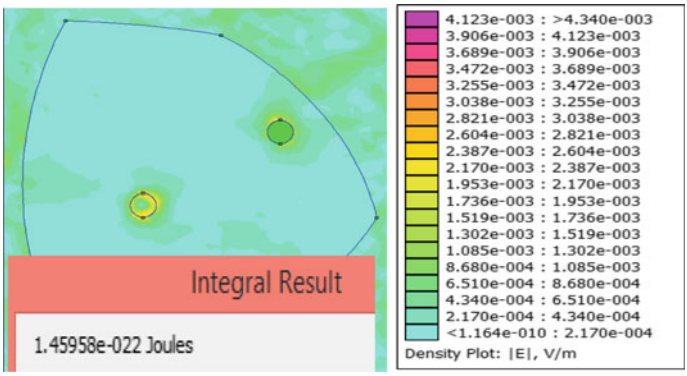

Fig. 7 Stored electric field intensity magnitude around the first tumor surface

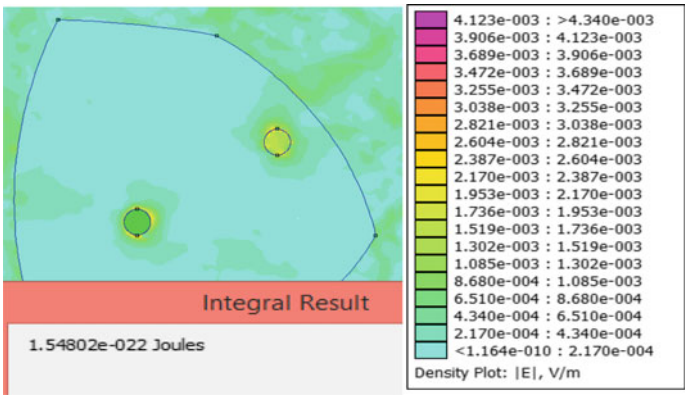

Fig. 8 Stored electric field intensity magnitude around the second tumor surface

terms of specific heat distribution is 1.45958×10^{-22} J/(kg K) and 1.54802×10^{-22} J/(kg K), respectively.

4 Conclusion

This article concludes with an optimistic outcome of heat low modeling useful for the HT of breast tumors. We simulate the bio-heat equation for the known boundary conditions. The optimum distribution of heat flow density and intensity inside the tumor has also been demonstrated successfully. Hyperthermia treatment can be optimized concerning the heat application method and tumor site, to avoid hotspots on healthy tissues around the tumor. It can also be used for extensive parametric studies to achieve higher accuracy and stability of various treatment parameters.

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Performance Analysis of Fusion Methods for the Multimodal Fusion of CT/MRI, MRI/PET and PET/CT Brain Images

Twinkle and Barjinder Singh Saini

1 Introduction

In the present era of technology, medical images hold prime importance for the assessment of various disorders and medical diseases. Many imaging modalities have been used for capturing such images. These include computed tomography (CT), magnetic resonance imaging (MRI), positron emission tomography (PET), single-photon emission computed tomography (SPECT), ultrasonography (USG), X-rays, etc. "MRI, CT and USG images are the structural and therapeutic images which afford lofty resolution images" [1]. "Whereas PET, SPECT and functional MRI images are functional therapeutic images which afford low-spatial resolution images with functional information" [1]. CT image can only display bone structures accurately. And, on the other hand, MRI image can only display normal or pathological soft tissues. Therefore, a single imaging modality is not sufficient to analyze a disorder perfectly because of lack of good quality and less relevant information content.

"Image fusion can manage the image quality problem as fusion process collects all the useful information from many images and present it in a combined image called fused image of higher intensity and higher quality" [2].

Hence, multimodal medical image fusion has become the valuable assistant amongst the medical experts for the need of the hour. When images from different imaging modalities are fused together, the resulting fused image is high in visual quality and rich in diagnostic information.

As defined in [3], "Multi-modal image fusion is the process of registering and combining multiple images from single or multiple imaging modalities to improve the imaging quality and reduce randomness and redundancy in order to increase the clinical applicability of medical images for diagnosis and assessment of medical problems" [3] (Fig. 1).

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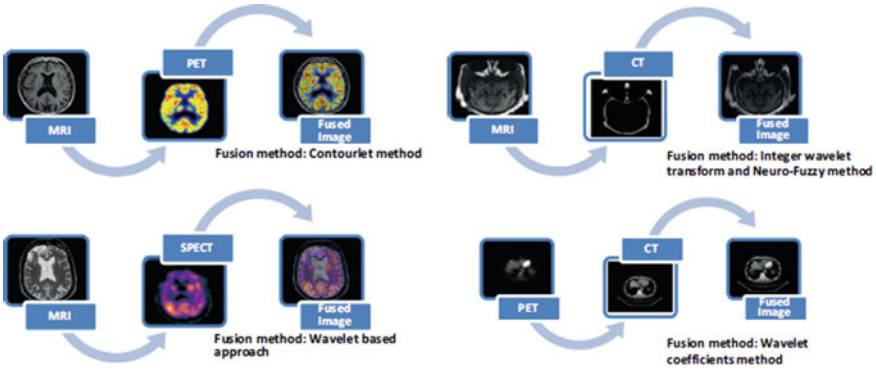

Fig. 1 Multimodal medical image fusion [4]

Image fusion is basically performed at three basic levels such as pixel-level, feature-level and decision-level [5]. "As compared to feature and decision-level, pixel-level methods are more suitable for medical imaging as they can preserve spatial details in fused images" [5]. If we talk about the multimodal image fusion specifically, it makes use of pixel-level fusion concept. Medical image fusion has many application domains or target organs like brain, breast, lungs, liver, prostate, etc.

In 2014, A. P. James and B. V. Dasarathy stated that, "Brain is one of the important organs that have been subjected to a wide range of medical image analysis and research" [3]. "The imaging studies reveal several important pieces of information about the brain that are otherwise not visible to human sensory mechanisms" [3]. Many types of imaging modalities have been used so far to study brain like CT, MRI, PET, SPECT, EEG, etc. The paper is primarily focused on CT, MRI, PET images of brain for carrying out the fusion process.

2 Literature Review

This section deals in portraying the work related to the field of medical image fusion, more specifically about fusion methods that has already been published in the past. Secondly, the section will put forth the conclusions drawn from the reviewed literature.

2.1 Related Work

Many researchers have carried out image fusion by the use of variety of fusion methods. In 2010 [6], image fusion algorithm had been presented for medical images

which is based on multi-wavelets and regional variance. This work had proved that "fusion based on multiple wavelets has better performance than single wavelet-based fusion" [6]. Later on, in 2010 in the work entitled [7], "Multimodal medical image fusion based on IHS and PCA", researchers indicated that IHS transform and PCA in conjunction with each other can preserve more spatial features and functional information with no color distortion for the fusion of PET and MRI brain images[7].

In 2011, Tan and Huang [8] had illustrated the concept of pixel-level fusion of medical images. Alka Srivastava and her fellow researchers presented that "image fusion method based on stationary wavelet transform (SWT) is better than principal component analysis (PCA) and discrete wavelet transform (DWT) because DWT is time invariant in transform domain and PCA results in blurring problems" [9]. PCA-DWT-based fusion methods have been widely proposed for the purpose of image fusion by many researchers [1, 9–11].

In 2014, V Jagruti presented in her research work about the idea of image fusion using discrete wavelet transforms [12]. In 2015, Agarwal and Bedi [13] proposed the hybrid technique using wavelet and curvelet transforms for the fusion of MRI and CT images. The main purpose behind the research study was feature enhancement in medical diagnosis.

In the year 2016, El-Gamal et al. [4] had very well described the entire process of fusion, image registration and categories of fusion methods. Also, Hajma and Sarma in their work entitled, "A Novel Multi-Focus Image Fusion Algorithm Using Stationary Wavelet Transform" [14], highlighted a new novel fusion method SWT that can be used for image fusion. SWT had also been used for the fusion of global and local features of images for the content-based image retrieval in [15]. SWT is combined with DWT and proposed for the fusion of images [16]. Many variants of wavelet transforms were widely discussed in the literature for performing fusion like multimodal fusion, multi-focus fusion or medical image fusion [17–21].

In the year 2017, B. Rajalingam and R. Priya suggested that PCA-DWT hybrid technique offers superior performance when compared to other traditional techniques in the image fusion of CT, MRI and SPECT images [1]. In order to improve the amount of information present in source images, Murthy and Kusuma [22] in their work entitled "Fusion of Medical Image Using STSVD" proposed the use of shearlet transform with singular value decomposition (SVD) to fuse PET and MRI images [22].

Also, S. Masood and his team presented a detailed review study of various image fusion methods [23]. Later on, S. Chavan along with his fellows introduced a new type of fusion technique rotated wavelet transform for CT and MRI images in order to extract the edge-related information from the source images [24]. In the same year, H. M. El-Hoseny et al., in the work entitled [25] "Medical image fusion techniques based on combined discrete transform domains," underlined the various transform domain fusion methods useful in performing medical image fusion [25].

In 2018, S. Singh and his fellow researchers [26] gave a cascaded fusion technique based on NSST and ripplet transforms for the fusion of CT/MRI images. They concluded that proposed fusion method resulted in better quality of fused images by overcoming the problem of shift invariance [26]. Also in the same year, Y. Na et al.

had proposed a novel fusion algorithm for the fusion of CT and MRI images based on guided filter (GF) where they had shown that the proposed fusion method results in more information content with clear edge details in medical images [27].

In the year 2019, Huang et al. [28] came up with another fusion algorithm which includes pulse coupled neural network (PCNN) and shuffled frog leap algorithm (SFLA) for the fusion of CT & SPECT brain images with an improved quality of fused images. The fusion method gave better precision and spatial resolution [28]. Also, in the year 2019, Yin [29] along with his fellow researchers worked upon proposing new fusion algorithm comprising non-subsampled shearlet transform (NSST) and parameter adaptive pulse-coupled neural network (PA-PCNN) model that resulted in superior performance and improved visual quality [29].

Later in 2019, Saboori and Birjandtalab [30] in their work entitled "PET–MRI image fusion using adaptive filter based on spectral and spatial discrepancy" proposed a fusion technique that incorporates adaptive filtering for the fusion of functional and structural information obtained from PET and MRI images, respectively [30]. It was shown that by the use of adaptive filter-based image fusion method, the structural and spectral characteristics of fused images were improved during the fusion of MRI and PET images [30].

In January 2020, Yadav and Yadav [31] published their work entitled as "Image fusion using hybrid methods in multimodality medical images", wherein they have reviewed various fusion methods involved in image fusion particularly focused on the use of wavelet transform, independent component analysis (ICA) and principal component analysis (PCA) for the purpose of reducing data dimensions and denoising [31]. They have mainly focused on three commonly used modalities, i.e., CT, MRI and PET. Also, they have well documented the future prospects of fusion methods or techniques for performing medical image fusion [31].

2.2 Inferences from Literature

From the reviewed literature, it was inferred that fusion methods such as simple average method or select maximum or select minimum method were easy to apply on images, but on the other hand, they produced images that possess low visual quality, blurring effects and poor edge information. So, it was decided to explore only the pixel-based methods based on addition and subtraction, respectively.

Also, it was found that multi-scale transforms when used for image fusion lead to fusion artifacts that may hamper the pathological information as well. Although researchers are more focused on using deep learning techniques in image fusion because of improved performance, but these techniques have many limitations such as complex framework which is time-consuming, lack of training data, requirement of professional labeling by medical experts which increases the workload, need of high performance computer hardware, etc.

On the other hand, it was deduced that there is a lack of fusion method that could be entirely be used for the fusion of CT/MRI, MRI/PET and PET/CT brain

images. The past research had only proposed the fusion techniques in general. Those fusion methods were not specific to a target organ. So, this paper is entirely focused on exploring the already available fusion approaches (as described in Sect. 3) and then finding out the best outperforming fusion method for the fusion of CT/MRI, MRI/PET and PET/CT brain images.

The basis of choosing CT, MRI and PET imaging modalities was only because of the fact that they are the most common imaging modalities used by the medical experts for brain as the target organ. Also, the image datasets of these imaging modalities are widely available on "The Whole Brain Atlas" [32] database contributed by Keith A. Johnson and Alex Becker.

3 Fusion Approaches

This section describes all the explored fusion methods for the multimodal fusion of CT/MRI, MRI/PET and PET/CT brain images.

3.1 Pixel-Based Methods (PBM)

"The pixel-based fusion methods include all those techniques that operate directly on the pixels of the image" [4]. Some sort of operation is performed on the pixels of the input images that modify their pixel values. After that, these images are fused together to generate the final fused image. Examples of such methods are arithmetic operations such as addition, subtraction, multiplication, division and logical operations, etc.

Here, two types of pixel-based methods: PBM-Addition and PBM-Subtraction have been explored. PBM-addition and PBM-subtraction are illustrated by Eqs. (1) and (2), respectively.

$$F(i, j) = I1(i, j) + I2(i, j) \quad \forall i, j \tag{1}$$

$$F(i, j) = I1(i, j) - I2(i, j) \quad \forall i, j \tag{2}$$

In the above equations, $F(i,j)$ represents the pixels of fused image; $I1(i,j)$ and $I2(i, j)$ represent the pixels of image from first and second imaging modalities, respectively. Also, "i" and "j" represent the number of rows and columns in the matrix representation of these images, and size of each image is taken as "$i \times j$".

In order to generate fused images using pixel-based methods, the input images must possess the same size.

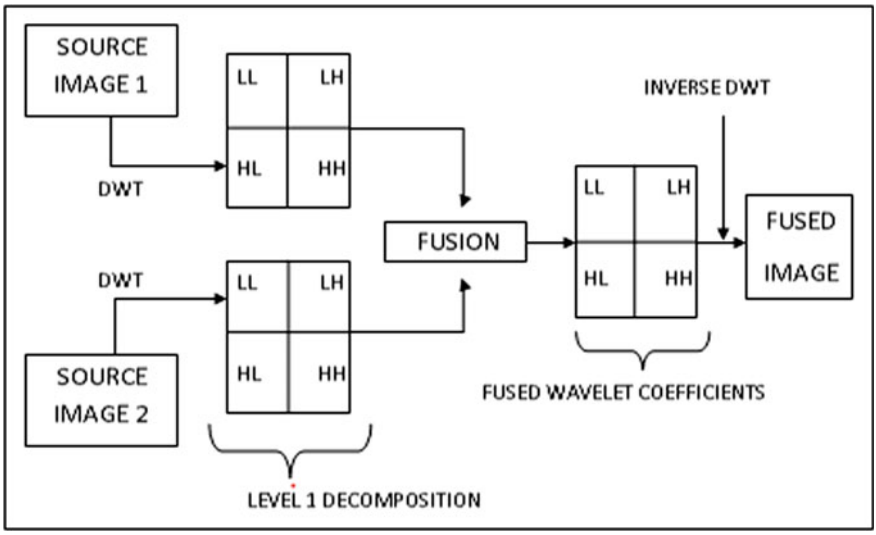

Fig. 2 DWT-based image fusion [12]

3.2 Discrete Wavelet Transform (DWT)

Discrete wavelet transform is a type of multi-scale fusion method. "Such methods are collection of those fusion techniques which work upon by representing each input image in a multi-scale manner" [4]. It includes the process of low pass or high pass filtering along with subsampling the parts of the image. "The discrete wavelets transform (DWT) allows the image decomposition in different kinds of coefficients preserving the image information" [33].

In DWT-based image fusion, at first, DWT is applied to the source images in order to obtain the wavelet coefficients. After that, an appropriate fusion rule is used. Finally, the use of inverse DWT is carried out for the reconstruction of final-fused image. This fusion based on DWT is depicted in Fig. 2.

3.3 Principal Component Analysis (PCA)

Principal component analysis comes under the category of sub-scale fusion methods. These fusion methods incorporate those statistical techniques that work upon correlation, taking it as a major factor into consideration.

In this fusion technique, "a high-dimensional input image is divided into various subspaces or regions" [4]. After this, important subspaces of the input images, often called as principal components, are evaluated. Later on, these components

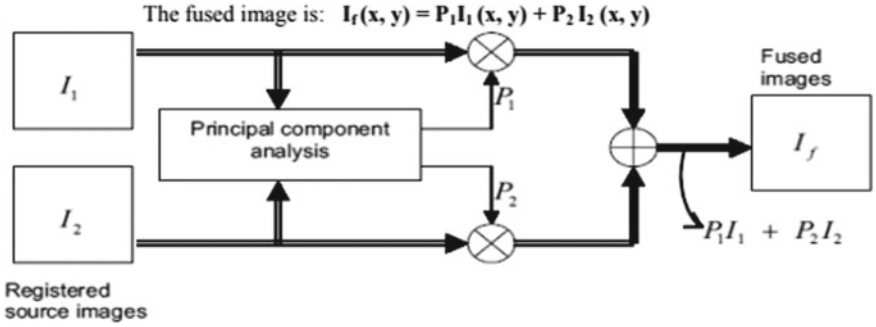

Fig. 3 PCA-based image fusion [13]

are combined together to generate the final resultant fused image. The procedure for fusion of images based on PCA is well demonstrated in Fig. 3.

3.4 Stationary Wavelet Transform (SWT)

As we know, Discrete Wavelet Transform (DWT) is not time invariant transform. Therefore, SWT method is developed to overcome the demerits of the DWT. Here in, the method of the down-sampling is suppressed so that SWT becomes translation invariant. SWT does not include down-sampling in the analysis filter bank and up-sampling in the inverse transform. The process of image fusion based on SWT is illustrated in Fig. 4.

In SWT-based image fusion, at first, SWT is applied to the source images *I*1 and *I*2 in order to obtain the wavelet coefficients. Once the wavelet coefficients are obtained for each of the source images, an appropriate fusion rule is used to fuse/combine them together. Then, the wavelet coefficients are generated for the fused image. Later, inverse discrete SWT is used for the reconstruction of final fused image from its wavelet coefficients. In this way, the final fused image is generated in SWT-based fusion process.

All these fusion methods were coded in MATLAB, and fusion was performed for CT/MRI, MRI/PET and PET/CT brain images. Then, the obtained fused images were evaluated based upon the image quality assessment metrics to find out the best fusion method. The simulation results and image quality metrics obtained for each fusion category are presented in the next section of this paper.

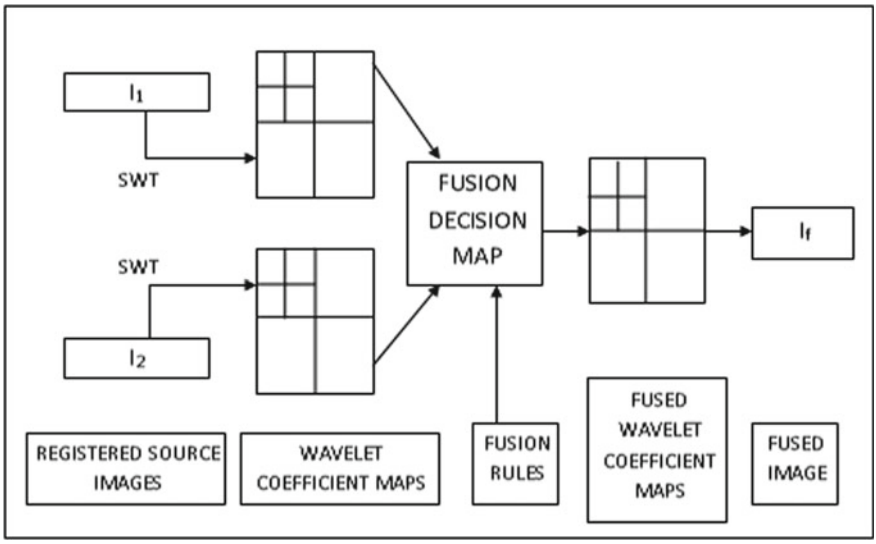

Fig. 4 SWT-based image fusion [14]

4 Experimental Results and Discussions

Experiments have been performed over three different imaging modalities of brain images: CT, MRI and PET. A total of 60 images of brain with/without diseases of three modalities were obtained from "The Whole Brain Atlas" [32] database.

All the simulations were carried out using MATLAB R2016a. The fused images obtained after fusion based on different fusion methods such as PBM, DWT, PCA and SWT have been presented in Figs. 5, 6, 7 and 8.

4.1 Fusion Based on Pixel-Based Methods (PBM)

Figure 5 illustrates the fusion of CT/MRI, MRI/PET and PET/CT brain images using pixel-based methods, namely PBM Addition and PBM Subtraction.

Figure 5a is illustrating the fusion of MRI (Image 1) and CT (Image 2) brain images using pixel-based methods. The third image and fourth image are showing the resultant fused images obtained after using PBM (addition) and PBM (subtraction) as the fusion method, respectively.

Similarly, Fig. 5b is illustrating the fusion of MRI (Image 1) and PET (Image 2) brain images using pixel-based methods. The third image and fourth image are showing the resultant fused image obtained after using PBM (addition) and PBM (subtraction) as the fusion method, respectively.

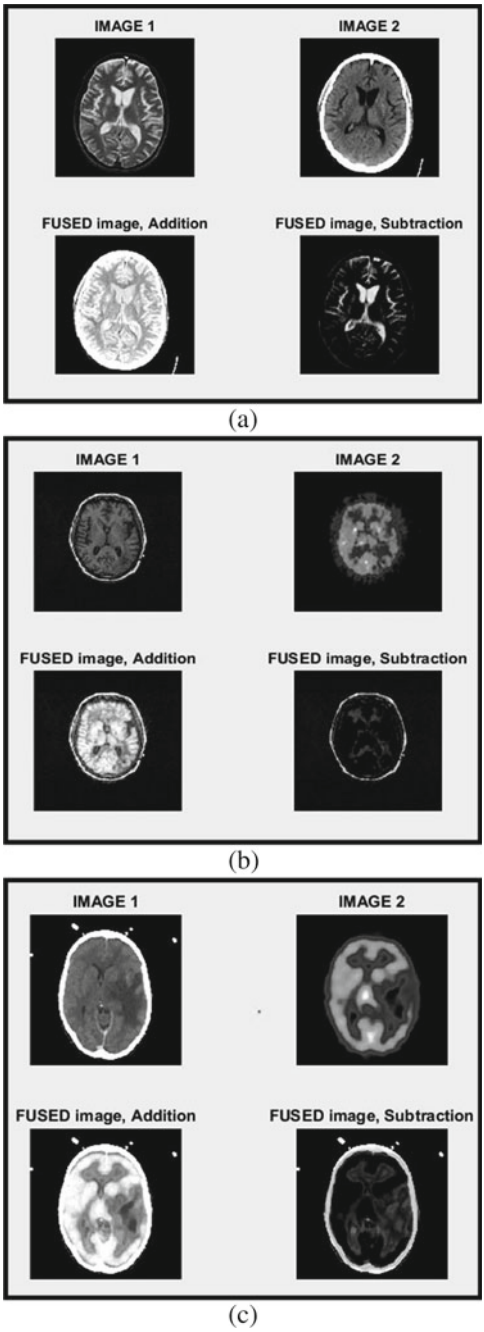

Fig. 5 Fusion based on pixel-based methods for **a** MRI and CT brain images. **b** MRI and PET brain images. **c** CT and PET brain images

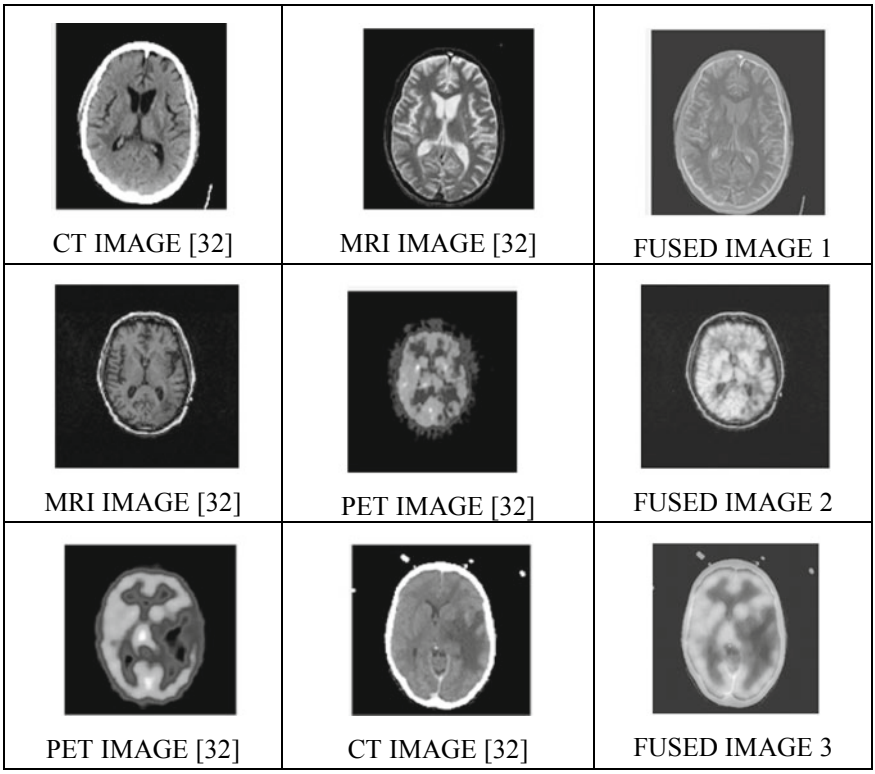

Fig. 6 Fusion based on DWT

Figure 5c is showing the fusion of CT (Image 1) and PET (Image 2) brain images using pixel-based methods. The third image and fourth image are showing the resultant fused image obtained after using PBM (addition) and PBM (subtraction) as the fusion method, respectively.

4.2 Fusion Based on Discrete Wavelet Transform (DWT)

Figure 6 is showing input source images and obtained fused images in the fusion of CT/MRI, MRI/PET and PET/CT brain images using DWT as fusion method.

In the first row of Fig. 6, MRI and CT brain images are shown which are fused together to generate the fused image 1. Second row illustrates the fusion of MRI and PET brain images to generate fused image 2. Similarly, PET and CT brain images are depicted in the third row which results in generating fused image 3.

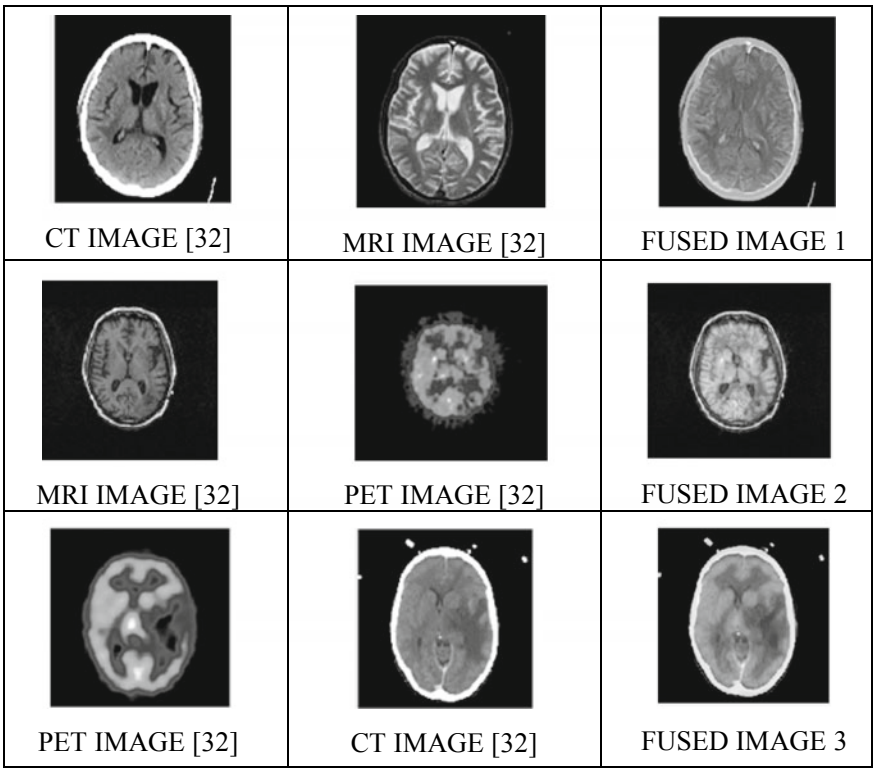

Fig. 7 Fusion based on PCA

4.3 Fusion Based on Principal Component Analysis (PCA)

Figure 7 illustrates the fusion of CT/MRI, MRI/PET and PET/CT brain images using PCA as fusion method. In the first row of Fig. 7, CT and MRI brain images are shown which are fused together to generate the fused image 1. Second row illustrates the fusion of PET and MRI brain images to generate fused image 2. Similarly, PET and CT brain images are depicted in the third row which results in generating fused image 3.

4.4 Fusion Based on Stationary Wavelet Transform (SWT)

Figure 8 illustrates the fusion of CT/MRI, MRI/PET and PET/CT brain images using SWT as fusion method. In the first row of Fig. 8, CT and MRI brain images are shown which are fused together to generate the fused image 1. Second row illustrates the fusion of PET and MRI brain images to generate fused image 2. Similarly, PET and

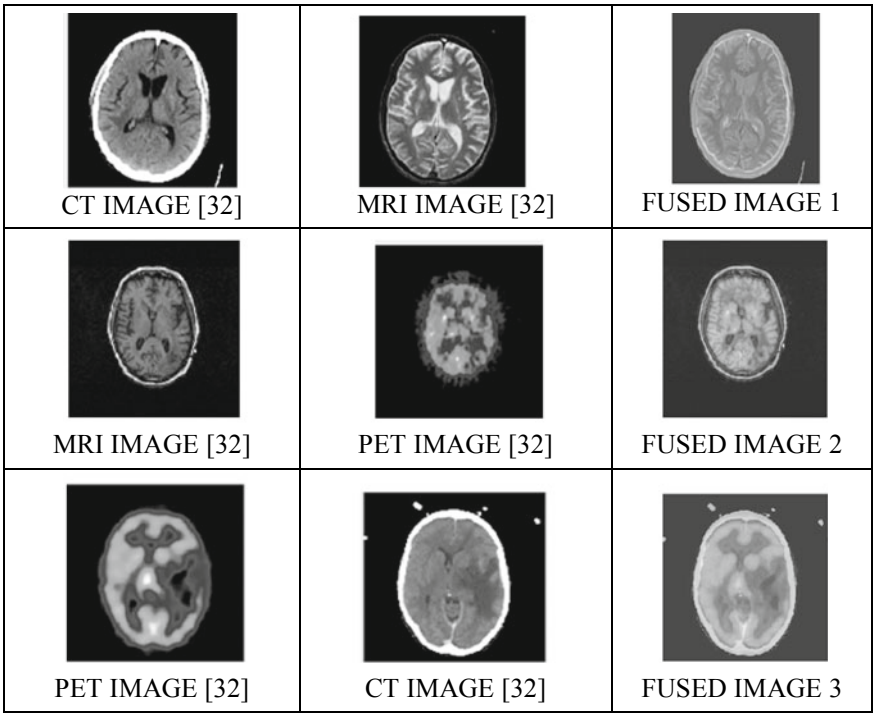

Fig. 8 Fusion based on SWT

CT brain images are depicted in the third row which results in generating fused image 3.

5 Image Quality Assessment Parameters

In order to quantify the quality of generated fused images, various image quality assessment parameters have been used in this paper. These parameters include entropy, structural similarity index metric (SSIM), peak signal-to-noise ratio (PSNR) and root mean square error (RMSE). These parameters are widely used by the researchers in analyzing the quality and information content of the images. These metrics have been discussed in detail below.

5.1 Entropy

Basically, Entropy measures the information content present in an image. "It is the most important quantitative measures in image fusion" [9]. More is the entropy value of fused image, more is the information present in an image and more beneficial it is for the medical experts in diagnosis.

In order to find the amount of information content embedded in images, entropies of IM1 (Image from first imaging modality) and IM2 (Image from second imaging modality and IMF (Fused image) were calculated.

5.2 Structural Similarity Index Metric (SSIM)

Structural similarity index metric refers to the parameter that measures the similarity between two images. SSIM is in the range of 0 (no similarity) to 1 (perfectly similar). SSIM values were calculated between IM1 (Image from first imaging modality) and IMF (Fused image) and between IM2 (Image from 2nd imaging modality) and IMF (Fused image) for analyzing the similarity between fused image and input images.

5.3 Peak Signal-to-Noise Ratio (PSNR)

This parameter calculates the ratio of signal power to noise power. Higher value of PSNR means higher signal power, lower noise power and hence better quality of reconstructed image [9].

In this paper, PSNR values were calculated for IM1 (Image from first imaging modality) and IMF (Fused image) and IM2 (Image from second imaging modality) and IMF (Fused image), respectively, in order to know about the quality of fused images with respect to original source images, i.e., how much useful information content is transferred from source images to the fused image.

5.4 Root Mean Square Error (RMSE)

"RMSE is computed as the root mean square error of the corresponding pixels in the reference image and the fused image" [34]. Less RMSE value is always desired in any fusion process because we expect the fused images to be full of useful information content and constituting no noise or errors. RMSE values were calculated for IM1 (Image from first imaging modality) and IMF (Fused image) and IM2 (Image from second imaging modality) and IMF (Fused image).

6 Comparative Analysis of Fusion Methods

The explored fusion methods that were used for performing the fusion of CT/MRI, MRI/PET and PET/CT brain images include

1. Pixel-based methods (PBM)
2. Discrete wavelet transform (DWT)
3. Principal component analysis (PCA)
4. Stationary wavelet transform (SWT).

After obtaining the resultant fused images for each fusion method, at first stage, the values for all the image quality assessment parameters were obtained during the fusion of all 60 brain images and considering all the four fusion methods. Then, average values of all image quality assessment parameters were calculated which are tabulated in Tables 1, 2 and 3 in the fusion of CT/MRI, MRI/PET and PET/CT brain images corresponding to all fusion methods such as PBM, DWT, PCA and SWT.

In Tables 1, 2 and 3, fusion methods are shown in the rows on extreme left, whereas the image quality assessment parameters are presented in columns. IM1 means image 1(Image from first imaging modality); IM2 means image 2 (Image from second imaging modality), and IMF means generated fused image. At first, entropies of all three types of images are tabulated like entropy of image 1; entropy of image 2; entropy of fused image, obtained for each of the fusion method. Then, SSIM values are presented between image 1 and fused image and image 2 and fused image, respectively. Similarly, PSNR and RMSE values are tabulated for image 1 and fused image and then for image 2 and fused image in the next columns.

Table 1 is showing the average values of all image quality assessment parameters that have been obtained corresponding to different fusion methods in the fusion of CT/MRI brain images. It is inferred from the table that average value of entropy of fused image is highest, i.e., 4.6379 when PCA is used as the fusion method.

The least entropy value, i.e., 2.2091 was found in SWT-based fusion. On the other hand, if we focus on SSIM values, then it is well depicted in the table that mean values of SSIM calculated between IM1 and IMF and IM2 and IMF are highest in PCA-based fusion, whereas SSIM values were lowest in case of fusion based on SWT. In PCA-based fusion, values were more close to 1 (SSIM = 1 means perfectly similar images) as desired.

Also, average PSNR value calculated for IM1 and IMF was the highest and least using PCA and SWT fusion methods, respectively. DWT- and SWT-based fusion gave the highest and least PSNR values in case of IM2 and IMF. The average RMSE value (between IM1 and IMF) was least for PCA-based fusion and highest for SWT-based fusion. Whereas, average RMSE (between IM2 and IMF) value was least and highest for DWT and SWT fusion methods, respectively.

Table 2 is depicting the average values of all image quality assessment parameters that have been obtained corresponding to different fusion methods in the fusion of MRI/PET brain image. It is inferred from the table that average value of entropy of

Table 1 Image quality metrics obtained for different fusion methods for fusion of CT/MRI brain images

Fusion method CT/MRI	ENTROPY			SSIM		PSNR		RMSE	
	IM1	IM2	IMF	IM1 and IMF	IM2 and IMF	IM1 and IMF	IM2 and IMF	IM1 and IMF	IM2 and IMF
PBM	3.468	4.9956	3.7009	0.6711	0.5665	13.28	9.55	3153.81	7405.12
DWT	3.468	4.9956	2.4508	0.7370	0.7291	16.79	16.779	1362.97	1367.04
PCA	3.468	4.9956	4.6379	0.7709	0.7458	20.7	14.32	555.16	2409.87
SWT	3.468	4.9956	2.2091	0.3046	0.2407	5.04	4.77	22,277.04	21,304.45

Table 2 Image quality metrics obtained for different fusion methods for fusion of MRI/PET brain images

Fusion method MRI/PET	Entropy			SSIM		PSNR		RMSE	
	IM1	IM2	IMF	IM1 and IMF	IM2 and IMF	IM1 and IMF	IM2 and IMF	IM1 and IMF	IM2 and IMF
PBM	5.3419	3.7614	4.2357	0.7139	0.4062	12.82	8.22	3581.63	10,105.05
DWT	5.3419	3.7614	1.39	0.6244	0.6891	15.98	15.69	1748.28	1768
PCA	5.3419	3.7614	5.4008	0.6834	0.6894	16.09	15.96	1579.03	1760.46
SWT	5.3419	3.7614	5.2718	0.6767	0.6896	15.91	15.61	1669.32	1796.97

Table 3 Image quality metrics obtained for different fusion methods for fusion of PET/CT brain images

Fusion method PET/CT	ENTROPY			SSIM		PSNR		RMSE	
	IM1	IM2	IMF	IM1 and IMF	IM2 and IMF	IM1 and IMF	IM2 and IMF	IM1 and IMF	IM2 and IMF
PBM	3.6297	4.2682	3.3268	0.7954	0.6024	13.81	10.02	2723.39	6572.38
DWT	3.6297	4.2682	1.2878	0.8490	0.7076	17.20	17.06	1241.98	1284.01
PCA	3.6297	4.2682	4.1334	0.9453	0.7085	22.02	14.36	410.16	2401.82
SWT	3.6297	4.2682	1.4110	0.5935	0.5628	7.94	6.15	19,608.83	15,929.22

fused image is highest, i.e., 5.4008 when PCA is used as the fusion method. The least entropy value, i.e., 1.39 was found in DWT-based fusion.

If we focus on SSIM values, then it is well inferred from the table that mean values of SSIM calculated between IM1 and IMF and IM2 and IMF are highest in PBM and SWT-based fusion, respectively. The least values for SSIM have been obtained in case of fusion based on DWT (IM1 and IMF) and PBM (IM2 and IMF). Almost similar SSIM values have been obtained for DWT, PCA and SWT fusion methods (in case of IM2 and IMF).

Also, the average values of PSNR calculated for IM1 and IMF and IM2 and IMF were the highest and least using PCA and PBM fusion methods, respectively. On the other hand, average RMSE values calculated between IM1 and IMF and IM2 and IMF were least obtained for PCA fusion method and highest obtained for PBM fusion method.

Table 3 is depicting the average values of all image quality assessment parameters that have been obtained corresponding to different fusion methods in the fusion of PET/CT brain images.

It is inferred from the table that average value of entropy of fused image is highest, i.e., 4.1334 when PCA is used as the fusion method. The least entropy value, i.e., 1.2878 was found in DWT-based fusion. Talking about SSIM values, then it is well inferred from the table that mean values of SSIM calculated between IM1 and IMF and IM2 and IMF were highest in PCA-based fusion. The least values for SSIM have been obtained in case of fusion based on PBM (IM1 and IMF) and SWT (IM2 and IMF) fusion methods.

Also, the average values of PSNR calculated for IM1 and IMF were highest and least using PCA and SWT fusion methods, respectively. Whereas, for PSNR calculated for IM2 and IMF, DWT and SWT fusion methods gave the highest and least average values. On the other hand, average RMSE values calculated between IM1 and IMF and IM2 and IMF were least for PCA and DWT fusion methods, respectively. Fusion based on SWT gave the highest average value of RMSE in both the cases.

The average values obtained for all the image quality assessment metrics (tabulated in Tables 1, 2 and 3) during fusion of CT/MRI, MRI/PET and PET/CT brain images versus different fusion methods such as PBM, DWT, PCA and SWT have been plotted in Figs. 9, 10, 11 and 12. These plots will help in finding out the

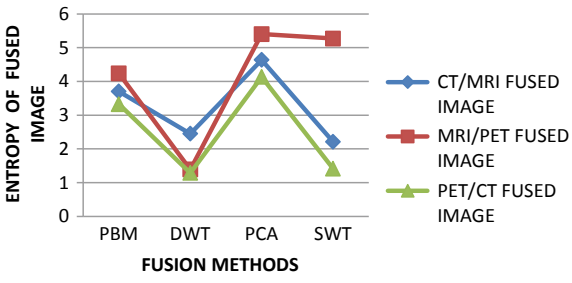

Fig. 9 Plot showing entropy of fused image versus fusion methods for fusion of CT/MRI, MRI/PET and PET/CT brain images

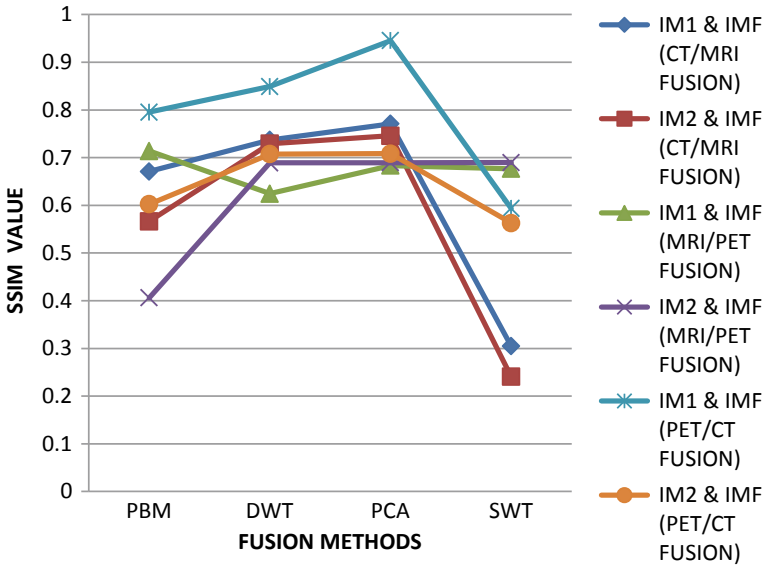

Fig. 10 Plot showing SSIM values (IM1 and IMF) and (IM2 and IMF) versus fusion methods for fusion of CT/MRI, MRI/PET and PET/CT brain images

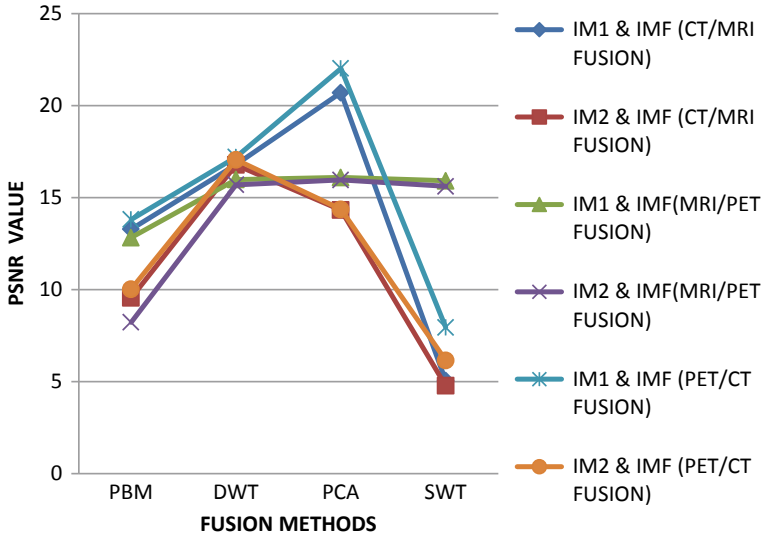

Fig. 11 Plot showing PSNR values (IM1 and IMF) and (IM2 and IMF) versus fusion methods for fusion of CT/MRI, MRI/PET and PET/CT brain images

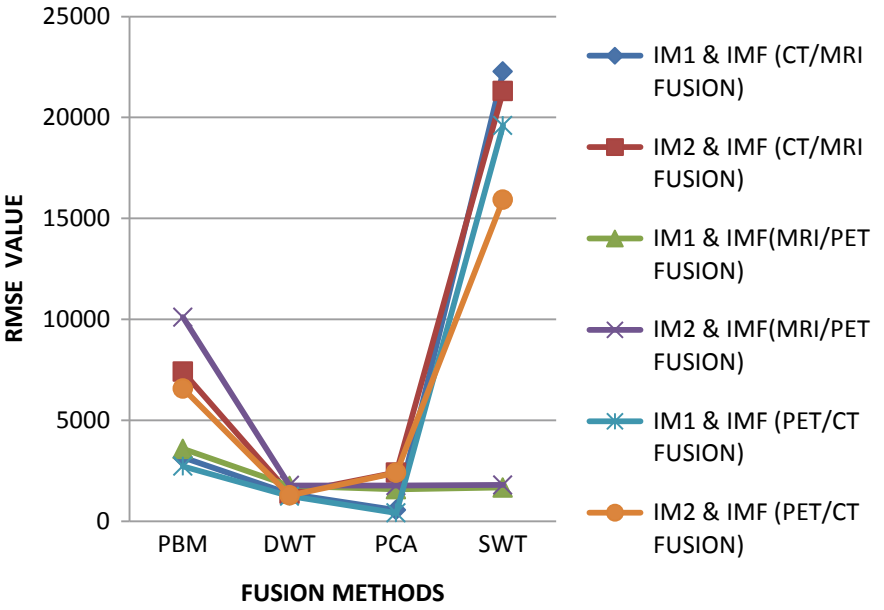

Fig. 12 Plot showing RMSE values (IM1 and IMF) and (IM2 and IMF) versus fusion methods for fusion of CT/MRI, MRI/PET and PET/CT brain images

best outperforming fusion method amongst all the fusion methods for the fusion of CT/MRI, MRI/PET and PET/CT brain images.

Figure 9 infers that the average value of entropy of fused images obtained in fusion of CT/MRI, MRI/PET and PET/CT brain images is highest, when PCA is used as the fusion method compared to other fusion methods such as PBM, DWT and SWT.

It has been deduced from Fig. 9 that the fusion based on PCA has resulted in an average increase of entropy of fused images by 74.84% in CT/MRI fusion; 106.18% in MRI/PET fusion and 146.05% in PET/CT fusion of brain images when compared to fusion methods such as PBM, DWT and PCA.

Figure 10 infers that the average values of SSIM calculated between fused images (IMF) and input images (IM1, IM2) were overall found to be highest using PCA fusion method.

Overall, PCA-based fusion has resulted in an average increase of SSIM values by 68.05% in CT/MRI fusion; 9.19% in MRI/PET fusion and 22.53% in PET/CT fusion, when compared to other fusion methods such as PBM, DWT and SWT.

Figure 11 infers that PCA-based fusion gave the highest average values of PSNR calculated between fused images (IMF) and input images (IM1, IM2) when compared to other methods such as PBM, DWT and SWT. This was found equally true in all the three cases, i.e., for the fusion of CT/MRI, MRI/PET and PET/CT brain images. Overall, it has been deduced from Fig. 11 that PCA-based fusion has resulted in an average increase of PSNR values by 104.91% in CT/MRI fusion of brain images;

18.40% in MRI/PET fusion of brain images and 72.35% in PET/CT fusion of brain images, when compared to other fusion methods such as PBM, DWT and SWT.

Figure 12 infers that the average values of RMSE calculated between fused images (IMF) and input images (IM1, IM2) were overall found to be least when PCA is used as the fusion method for the fusion of CT/MRI, MRI/PET and PET/CT brain images. It was observed that PCA-based fusion resulted in an average decrease in RMSE values by 52.17%; 28.09% and 50.17% in fusion of CT/MRI, MRI/PET and PET/CT brain images, respectively.

7 Conclusion

It is clearly concluded from the obtained results that are tabulated in Tables 1, 2 and 3 and from Figs. 9, 10, 11 and 12 that PCA is the best fusion method amongst all explored fusion methods such as PBM, DWT and SWT for the fusion of CT/MRI, MRI/PET and PET/CT brain images. Not only, the resultant fused images obtained using PCA fusion method were best in terms of visual quality, but also these fused images gave the best results for all the image quality assessment parameters.

In CT/MRI fusion of brain images, PCA has resulted in an average percentage increase of entropy by 74.84%; SSIM values by 68.05%; PSNR values by 104.91% and RMSE values have been reduced on average by 52.17%.

Similarly, in MRI/PET fusion of brain images, average percentage improvement of 106.18%, 9.19%, 18.40% was observed in entropy, SSIM and PSNR, respectively, using PCA fusion method. Also, RMSE value was reduced by 28.09% on average using PCA as fusion method when compared to other methods.

In PET/CT fusion of brain images, PCA-based fusion gave the best results with an average increase of entropy by 146.05%; SSIM values by 22.53%; PSNR values by 72.35% and RMSE values were decreased on average by 50.17%, when compared to other fusion methods like PBM, DWT and SWT.

Hence, it has been justified that multimodal fusion of CT/MRI, MRI/PET and PET/CT brain images is best performed using PCA as the fusion method. The resulting fused images are rich in information content, less noisy and possess reduced redundancy. These images will aid the medical experts in knowing the state of the patient more accurately in short span of time. Instead of analyzing the individual images of different imaging modalities one by one, the expert can just focus on one single fused image.

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Performance Analysis of Task Scheduling Heuristics in Fog Environment

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1 Introduction

In distributed computing, resources are interconnected with each other, and these resources are providing huge computational power which can be thought of as cloud. Cloud computing brings revolution and provides a new way to access devices that can quickly provide services [1]. Devices connected with internet connectivity which transmit data to higher-level devices in the network are termed as IoT devices. IoT devices contain sensors, actuators, vehicles that are generating data. IoT devices are growing rapidly, and they are producing an immense amount of data. It is impossible for standalone IoT devices to efficiently perform the computation. A standalone system has limitations in their functionalities for processing but cloud computing provides abundant resources for computation. In some cases, IoT gadgets require a fast reaction, and delay in response from a cloud is not desirable. To overcome this scenario of latency communication, fog computing is used to assist the cloud computing [2–6]. This resides between client and cloud which process requests from the client and processing of the request are performed at fog and necessary data forward to cloud for storage [1, 7, 8]. In a fog computing environment, task scheduling is a significant issue that requires resources for execution. Allocation of resources for scheduling of tasks is a critical issue. Efficient resource management is required for scheduling of tasks which provide minimum task execution time [1, 8, 9]. The

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objective of scheduling is to find an optimal assignment of tasks to machines. How to execute a task in a fog environment is a big technical challenge. Which task should be executed on which node is a big concern [10, 11]. What heuristics can be used in for optimal task execution? To address this challenge, various authors have proposed strategies for task scheduling. [9] Proposed an adaptive double fitness genetic task scheduling (ADGTS) algorithm for task scheduling in fog computing. A security-aware task scheduling in a fog environment has been described in [12]. Ni et al. [13] also describe a scheduling heuristic for fog computing. In this work, we studied the scheduling of tasks in a fog environment and performance evaluation of various task scheduling heuristics is carried out.

2 Task State Transition in Fog Environment

The task execution in a fog environment can pass through in many states, i.e., IoT device, fog computing administrator, fog scheduler, blocked, executor, finish state, and finally in cloud storage state. Figure 1 is illustrated all the states involved in the completion of one task. Initially, the task is generated by IoT devices. The fog computing administrator is responsible for submitting the task. It also collects the requirement for task execution from IoT devices. Tasks arriving at the fog scheduler is put in the global task queue. The fog scheduler checks the workload and resource availability of each node and forwards the task to the node that satisfies the task requirement. If the fog scheduler is busy, then the arriving task will be blocked from entering into execution else it is put in the global queue. Undertakings that are desiring execution in the fog scheduler are separated into two types viz. newly arrived tasks

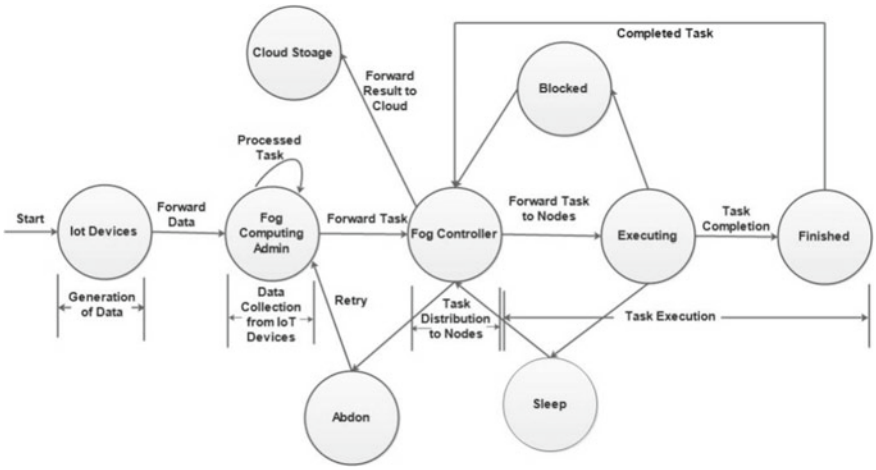

Fig. 1 Fog computing architecture

and squirted tasks, i.e., tasks that are aborted, while new tasks, i.e., tasks that have not any service from time of arrival. To recognize these two kinds of tasks, it maintains two queues, one for new tasks that are arrived in fog but not scheduled and the second queue for squirted tasks. The new queue keeps tasks in the order of arrival, while the squirted queue keeps tasks based on the size of CPU consumption. The task having the littlest CPU utilization is put at the head of a queue while the assignment having the biggest CPU utilization is put at the tail of the queue. The task in the task queue is scheduled first, and then squirted queue tasks are sent to scheduling. Once a task is completed execution, it releases resources, and these resources become available for other unscheduled tasks. If the required resource is not available for the task then it is put in the blocked state. Task which is using CPU cycles belongs to the executor state. Task enters into the finished state after total execution. Finished task came back to the user through the fog scheduler. After complete execution of the task, the fog scheduler forwards results to cloud storage. In cloud storage state, it has stored the processed result from the fog computing environment.

3 Task Scheduling Heuristic Description

In fast come first service (FCFS) task scheduling, the task is selected for execution in the order of submission. If sufficient resources are not available, then the scheduler waits until the resource becomes available. In random scheduling, the task for execution is randomly selected from a set of tasks that are submitted but started for execution. No task is preferred, but tasks submitted earlier have a higher probability to be started for a given time instant [14]. In the earliest deadline first (EDF), tasks are selected according to the deadline in the earliest deadline first heuristic. The deadline and priority of tasks are inversely proportional to each other. In Min-Min algorithm, it commences with a set of a task which is not scheduled. It then determines the completion time of all tasks on all available machines [15]. The task is selected such that it has the least completion time on the respective machine. The task which is scheduled on a machine is expelled from a set of tasks and then this methodology is repeated for unscheduled tasks [14]. In Max–Min algorithm, it starts to execute with a set of a task which is not scheduled. It then determines the completion time of all tasks on all available machines. Task having the most extreme finishing time is selected and scheduled on the respective machine. The task which is scheduled on a machine is expelled from a set of tasks, and then this methodology is repeated for unscheduled tasks [2, 16].

4 Performance Assessment

Table 1 demonstrates the evaluation set up to quantify the performance of our model.

Table 1 Simulation parameters

Simulator tool	iFogSim
Number of nodes	10
Task ETC	Between 1 and 10 (Random distribution)
Task arrival	Poisson distribution
Simulation starts at	100 tasks
Simulation end at	500 tasks

We considered two parameters viz. makespan and flowtime time to measure performance. We have developed a simulation model in iFogSim [17]. Each simulation ends when 500 tasks execution gets completed. We considered ten computing nodes for simulation each having diverse computing capacity. The arrival of tasks is modeled as a Poisson random process. We have evaluated the performance using Max–Min, Min–Min, FCFS, Random, and EDF heuristics.

Makespan is defined as a maximum of completion time for any task. Figure 2 shows the number of tasks versus makespan. The x-axis shows a number of tasks, while the y-axis shows the makespan. It is found from the figure that with the increase in the number of tasks, and the makespan additionally gets increased. Max–Min, Min–Min, EDF, Random, and FCFS heuristics are applied for task scheduling by fog scheduler. From the comparison, it is observed that scheduling task using Max–Min and Min–Min heuristic gives better results as thought about EDF, Random, and FCFS heuristics.

Figure 3 shows a comparison of flowtime versus a number of tasks. It is observed flowtime increases with the number of tasks. The horizontal axis demonstrates a number of tasks and the vertical axis demonstrates flowtime. Performance analysis is carried out between Max–Min, Min–Min, EDF, Random, and FCFS heuristics.

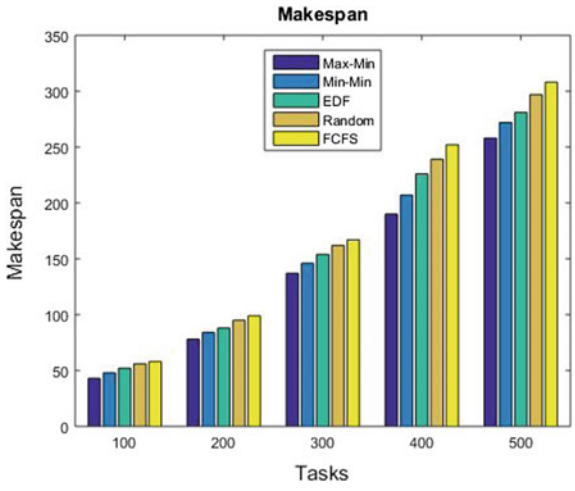

Fig. 2 Makespan comparison

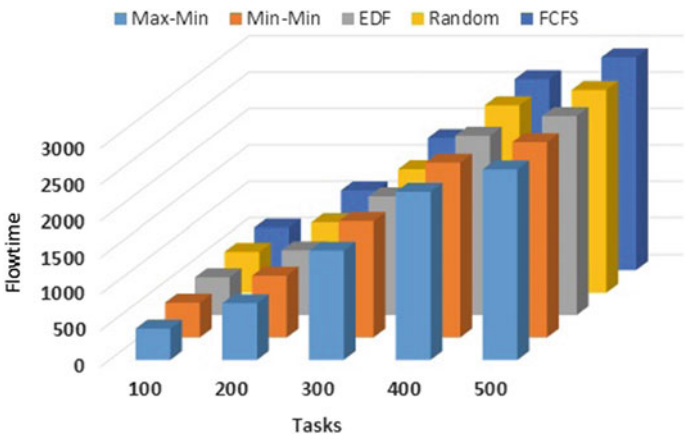

Fig. 3 Flowtime comparison

The simulation results show that scheduling of tasks using Max–Min heuristic gives better outcomes as thought about Min–Min, EDF, Random, and FCFS heuristics.

Figure 4 shows the average execution time and task with real performance. As the no. of tasks increases, we observe a consistent increase in average execution time. As the higher the number of tasks, more resource is used, increasing the total execution time. Performance evaluation is carried out using Max–Min, Min-Min, EDF, Random, and FCFS heuristics. The x-axis indicates a number of tasks, and the y-axis indicated the average execution time. From the comparison, it is observed that if tasks are scheduled using the Max–Min heuristic, then it gives better results as thought about Min-Min, EDF, Random, and FCFS heuristics.

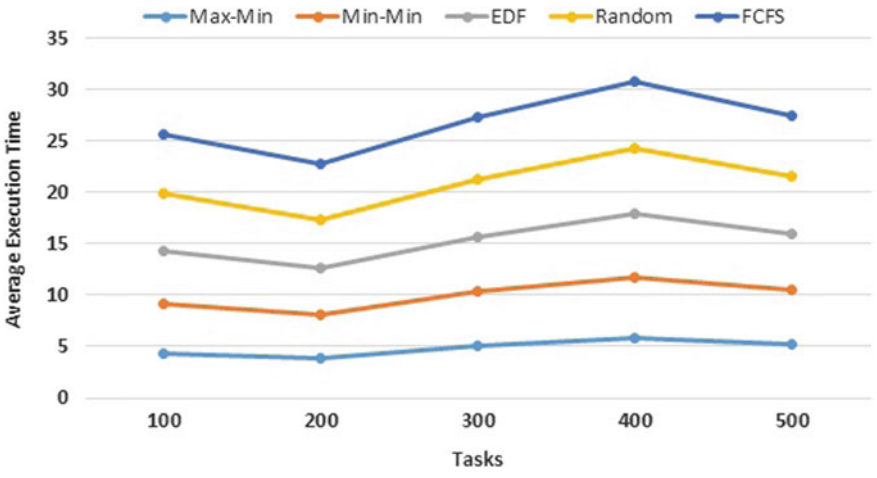

Fig. 4 Average execution time comparison

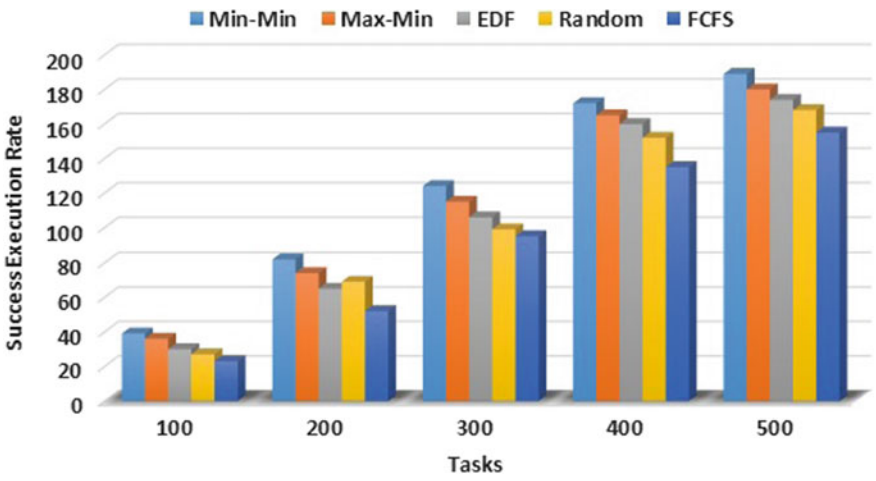

Fig. 5 Success execution rate comparison

If the task completes execution within a given deadline, then it is called as successfully executed. The effect of success execution rate on the number of tasks is shown in Fig. 5. The horizontal axis demonstrates the number of tasks, and the vertical axis demonstrates success execution rate. Comparison results clearly indicate that Min-Min heuristics complete more number of tasks within the deadline as contrasted with Max–Min, EDF, Random, and FCFS heuristics.

5 Conclusion

The present research article aims to present the performance analysis of task scheduling heuristics in fog computing environment. The heuristics are executed in a heterogeneous fog environment. Here, it evaluated the performance using Max–Min, Min–Min, FCFS, Random, and EDF heuristics based on parameters viz. makespan, flowtime, average execution time, and success execution rate. From the performance evaluation, it has observed that Max–Min gives better performance in minimizing makespan, flowtime and average execution time, while Min-Min heuristic gives better performance in success execution rate.

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Multi Hop DTN Routing Algorithm for Maritime Networks

Nidhi Sonkar, Sudhakar Pandey, and Sanjay Kumar

1 Introduction

Now a day's, people want to access internet in ship also, while traveling but, currently in ship internet is access directly by satellite links in which 20 MBPS connection rate of satellite to ship connection and ship to user connection rates up to 432 kbps [1]. It is found that satellite connection is too expensive for frequently use. To resolve this problem, researchers are finding the way to expand the internet connection from land to sea so that people can use internet access in low cost. Triton [2] is a project which aim is to extend the wireless network from land to sea. Triton used the WiMAX IEEE and 802.16 m techniques that can gives the wide range of communication about 50 km. Triton used these features for long range communication from shore to ship and ship to ship wireless links. But the ships are continuing moving and in sea density is very low, the result becomes frequent disconnection between nodes. Therefore, the topology of networks changes every time. In this type of network, where low density, intermittent connectivity and highly dynamic networks delay in communication occurs. In such type of issues, delay tolerant networks can resolve the problems in maritime networks [3].

Delay tolerant networks (DTNs) enable communication in the environment where intermittent connectivity, high-error rate, long delay or no communication between source and destination exist [4]. DTNs use store-carry-forward technique to overcome intermittent connectivity for transmission. If there is no connectivity exist between two nodes, source node stores messages in buffer until the destination has been reached [5]. In maritime networks, if no connectivity exist between two ships, one ship stores the data until the link has been found. In this way, delay tolerant network finds applicable in maritime networks. For DTNs, many routing algorithms have been proposed by authors [6]. Multi copy-based routing epidemic routing [7] is

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initially proposed routing algorithm in which when any two nodes come in the contact they share all the messages to each other so that both can have all the messages. The advantages of this technique are high-delivery rate with minimum latency. But the major drawback of this scheme is it uses high amount of buffer space, bandwidth and energy. Therefore, spray and wait [8], and multi period spray and wait [9] schemes have been proposed which limit the number of copies with high-delivery rate. In single-copy-based routing scheme, PROPHET [10] routing has been proposed, in which history of encountering of node is considered for prediction of future movement of node. For example, if a node visited several locations multiple times it is likely to be visit the same location in future. MaxProp [11] is other single-copy-based routing algorithm in which author set the priority of schedule of both message dropping and transmitting to other nodes. This routing scheme achieves better performance when limited resources are available. But these techniques give high-delivery delay and unsatisfactory delivery rate when applying in maritime networks [12].

2 Related Works

There are multiple protocols for routing proposed by authors for maritime mess networks, which are optimized link state routing (OLSR) [13], Ad hoc on demand distance vector routing (AODV) [14] and Ad hoc on demand multipath distance vector (AOMDV) [15]. These all routing protocols are compared in [16]. These routing protocols are good performer when the density is high but in the maritime networks density cannot be good; therefore, they are failed in maritime networks. When the problem of low density occurs delay tolerant networks come in every researchers mind. Multiple routing protocols have been proposed in DTN. We can divide all protocols in two categories. First one is multi copy-based routing protocols, in this category the protocols lied are epidemic [17] spray and wait [8], and multi period spray and wait [9]. Second category is single-copy-based routing protocols, in this category many protocols are implemented which are, PROPHET [10], MaxProp [11], etc.

But, these routing protocols give unsatisfactory results when applying in maritime networks as discussed in [12]. High end-to-end delay and less delivery ratio are the problem of existing routing protocols. Therefore, we are proposing new routing protocols for maritime networks to overcome the existing problem. Our scheme takes less information about networks and finds the probability to select relay node to transfer data from source to destination. By probability of node that they can transfer data in minimum time, we can decrease the end-to-end delay and increase the delivery probability of data in maritime networks by using the features of delay tolerant networks.

3 Proposed Methodology

Let us consider the set of all ships available in sea is Sh, such that, $\mathrm{Sh} = \{\mathrm{sh}|\ \mathrm{sh} \in \mathrm{Sh}\}$ and nodes in land side L is defined as $L = \{l|l \in L\}$. The ships are moving in different locations with different velocities. We assume that time of contact between the ships is sufficient to make decision to selection of node and the transfer of messages from one ship to other. The ships which come in contact are implicitly assumed to become aware of the arrival instance and the speed as well as direction of propagation of the contact ship. Moreover, the computation time taken by the host node for bundle relaying decision is negligible (Fig. 1).

Based on the above mentioned assumptions, our goal is to develop a routing algorithm which has a single copy of message in which the delay in expected delivery will be minimum we proposed same routing scheme for vehicles in [19]. For ease of understanding, we list the main auxiliary variables as abbreviation in Table 1.

In this methodology, when a ship contact to other ship or node in the land they share information to each other. The information includes speed of ship and arrival time. Here, we consider the node that start transmission is S. Thus, S has the information about the speed v_i and arrival time of ith ship. S releases a single packet that is placed in the front of its queue with a probability Pr. If packet B is forwarded to the ith ship, it will be delivered to destination D at the instant $d_\mathrm{i} = t_\mathrm{i} + \frac{D_\mathrm{sd}}{v_\mathrm{i}}$. If packet B is forwarded to the $(i+1)$th ship, it will be delivered to destination D at the instant $d_{i+1} = t_{i+1} + \frac{D_\mathrm{sd}}{v_{i+1}}$. Thus, the best opportunity to forward message arises whenever:

$$d_{i+1} \langle d_i \Rightarrow I_{i+1} + \frac{D_\mathrm{sd}}{v_{i+1}} < \frac{D_\mathrm{sd}}{v_i} \tag{1}$$

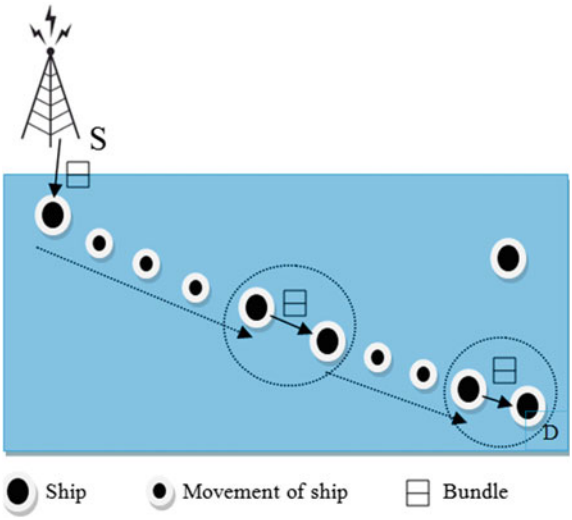

Fig. 1 Proposed methodology in maritime networks

Table 1 Details of auxiliary variables

Variables	Details
Sh	Set of ships
L	Set of nodes in land
Pr	Probability to release messages
C	Coverage range of node
S	Source node
D	Destination node
D_{sd}	Distance between source and destination
d_{i}	Instance of delivery to D for ith ship
v_{i}	Velocity of ith ship
$I_{\text{i+1}}$	$(i + 1)$th ship inter arrival time
t_{i}	Time of arrival of ith ship

According to Eq. (1) not only does $(i + 1)$th ship, has to arrive S before one has reached D but also has to reach D before one does [18, 19]. In proposed routing scheme, we first direct transfer the message to the node that arise first in the range of communication by direct delivery method. After that decision will be taken for each contact for transmission. We choose the node that come in the contact of node that is going to transfer the message according to the direction of the node. That means, we select the node that is going to the direction of destination so that we can reduce the delay in transmission. We cannot select the ship that has zero velocity in the direction of destination. Thus, expected delivery time can be reduce by following this procedure. The connection that satisfies Eq. (1) is the best connection among all. The algorithms for proposed routing scheme and selection of best node are as follows.

Algorithm 1: Multi Hop routing Algorithm
For each ship sh $\in$ Sh and stationary node that is in land l $\in L$, working as host do

1. For any node that comes in the communication first deliver the message by direct delivery method.
2. Drop a message to the forwarder from the front of the message queue.
3. Find the destination of the message.
4. Find list of all Useable Connections.
5. Call Best node Computation algorithm.
6. Deliver message to the best node.

In Algorithm 1, we choose the list of connection that direction is same as destination of the transmitting message. In the present context, this connection is called as valid connections. We cannot choose other connections for message transfer because the direction is not same as destination if we choose those connections only delivery delay will be increase. A node from the valid connection is called as best node and that node will be choose for message transmission. In proposed scheme, a best node

is called in terms of minimum delivery time that is the node that deliver message to the destination with minimum time as we discussed in Eq. 1. Below, we discuss the algorithm for best node computation.

Algorithm 2: Best Node Computation
For a given list of connection and destination location of the dequeued messages.

1. Get information about node like arrival time and speed
2. Calculate exit time $t_e = t_i + t_c$
3. While $t_{current} < t_e$
4. For each connection
5. Calculate estimate time $estTime = t_i + \frac{dist}{speed}$
6. If $estTime < minTime$
7. $minTime = estTime$
8. Update connection list
9. Return base connection.

4 Simulation and Results

ONE simulator abbreviated as, opportunistic networking environment simulator is designed especially for routing in delay tolerant networks [20]. We are using ONE simulator for simulation of proposed routing scheme in maritime networks to evaluate performance that proposed routing scheme is better than existing algorithms. The parameters used in multi hop DTN routing algorithm for maritime networks are given in Table 2.

We have simulated the proposed routing scheme to study the performance of proposed methodology with existing techniques in order to compare proposed multi hop algorithm for maritime networks with existing DTNs routing algorithms. The results of simulation are shown as follows: In Fig. 2, we can see the impact of number of ships in delivery probability, when we increase the number of ships delivery probability also increases. But network of sea is sparse network, we cannot make it a dense network. Therefore, we take maximum of 50 ships in the sea and the delivery

Table 2 Parameters

Parameter	Value
Transmit range	1 km
Buffer size	20–100 MB
Number of ships	10–50
Message TTL	300 min
Message size	100 b
Simulation time	10,000 s
Movement model	Map based movement

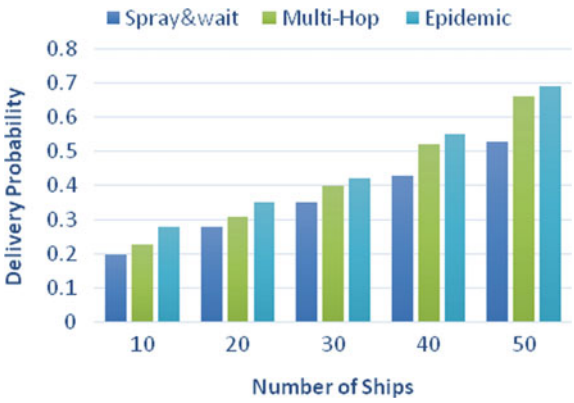

Fig. 2 Impact of number of ships in delivery probability

probability is also satisfactory as compare to other algorithms in less number of ships also except epidemic routing algorithm. The reason of increasing delivery probability is, when more number of ships available in sea opportunity of meeting ships to each other will increase and amount will be less of losing the bundle.

In Fig. 3, we can see the impact of number of ships in average end to end delay. When number of ships increases the delay is decreasing, the reason behind this decrease is we can find the ship which can transfer faster than others if we have more number of ships. Our proposed routing algorithm have the less end-to-end delay as compare to others because we use probabilistic scheme to find the ship which can deliver the data in minimum time our main work of proposed algorithm is make the delay minimum.

In Fig. 4, the impact of increasing buffer size in delivery probability is shown. We can see that when the buffer size is increasing delivery probability also increasing because, when the two ships are far away from each other, one should store the data till the other ship not come in the contact of other. So buffer space plays the major role in this problem. Therefore, we can say that the delivery probability will be increase if we increase the size of buffer. In Fig. 5, we can see that the average end-to-end delay in decreasing when we increase the buffer size the reason behind this decrease

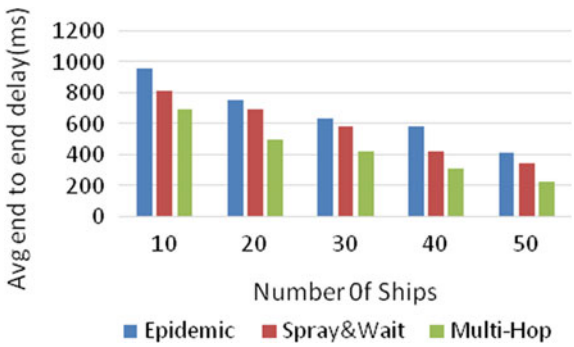

Fig. 3 Impact of number of ships in average end to end delay

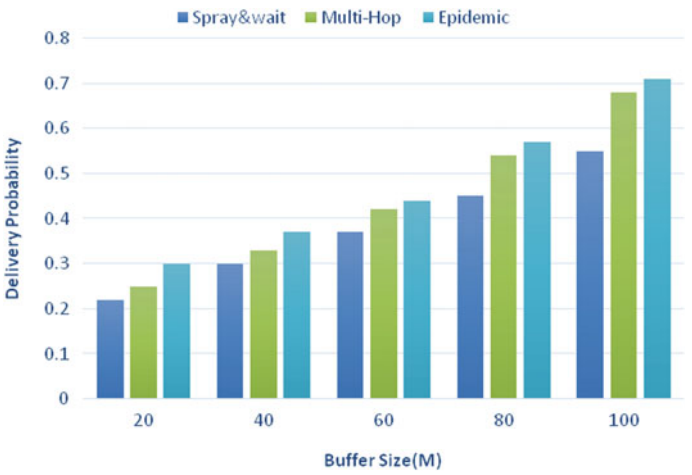

Fig. 4 Impact of buffer size in delivery probability

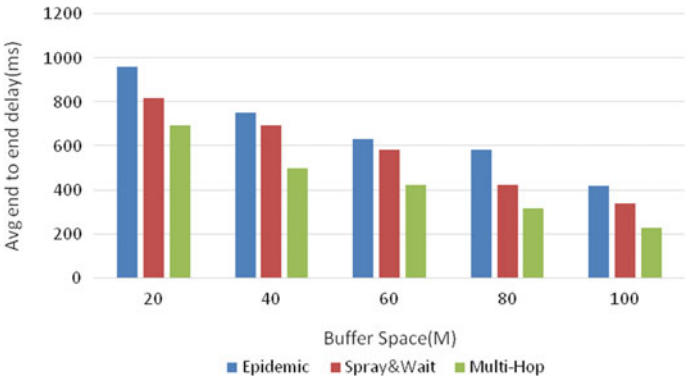

Fig. 5 Impact of buffer size in average end-to-end delay

in end-to-end delay is, if buffer space will be sufficient data packets could be send to other node very quickly because no packets have to wait for getting space in buffer. And if buffer size will be more less chances if data losing because if no link between two node found then buffer store data till link formation. Chances of losing data packets are high in small buffer size. Therefore, we can say that end-to-end delay can be reduce with large buffer space.

5 Conclusion

In this article, we proposed a multi hop delay tolerant network routing algorithm for maritime networks for creating mesh network in sea. By addressing the intermittent connectivity and long delay problems in maritime network, researchers have used delay tolerant network routing protocols for maritime networking. But the existing DTN routing protocols having the problems when they are used in maritime networks like low-delivery probability and high delay on data transfer. Therefore, we proposed a probabilistic based multi hop delay tolerant Network that finds path for deliver data to the destination with the minimum time and high-delivery rate. We simulate this environment using ONE simulator and compare the proposed routing algorithm with existing DTN routing algorithms that are used in maritime networks. We got that proposed routing algorithm has the better performance as compared to existing techniques.

6 Future Work

In this research work, we have evaluated the multi hop DTN routing algorithm for maritime network by using the standard mobility models. In future, for getting accurate result, we can evaluate this work by real time networks or real life mobility traces with physical nodes.

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Performance Evaluation of a Novel $Si_{0.6}Ge_{0.4}$/Ge Doping-Less TFET for Enhanced Low Power Analog/RF Applications

Suruchi Sharma, Rikmantra Basu, and Baljit Kaur

1 Introduction

TFET is well thought-out as one of the most forthcoming replacements to succeed MOSFET by virtue of its low subthreshold swing (SS), small off-state current (I_{OFF}), ultra-low voltage operation ($V_{DD} < 0.5$ V), and immunity toward short channel effects [1–3]. However, along with the impediment of low on-current (I_{ON}), the operation of TFET necessitates higher doping concentration and abrupt junctions, which leads to the necessity of complex thermal budget and exorbitant annealing approaches. These requirements further exaggerate the variability in device functioning on account of random dopant fluctuations (RDFs), resulting in an increment of I_{OFF} [4].

Consequently, several approaches have been described in the literature such as the work function (WF) engineering [5, 6], the gate dielectric engineering [7, 8], spacer engineering [9, 10], band-gap engineering [11], material engineering [12–15], pocket engineering [16], and so on to deal with the issues mentioned above. Among them, a charge plasma-based Doping-less TEFT (DLTFET) has engaged much attention as its p^+ source, and n^+ drain is designed by applying the suitable WF of the metal electrodes contacting with the semiconductor [17]. This DL TFET structure circumvents RDF and issues related to thermal budget resulting in the formation of the abrupt junction without any chemical doping. However, Si-DLTEFT exhibits a low I_{ON} owing to large effective mass of electron in Si and the small horizontal electric field in the tunneling junction, likewise conventional Si-TFET.

Furthermore, different semiconductor materials illustrate different electrical properties, i.e., indirect semiconductor material (Si, Ge) shows indirect band-to-band tunneling (BTBT) [18], while compound semiconductor material (SiGe) exhibits

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direct BTBT [19–22]. Regarding this, the utilization of small band-gap semiconductor material in the source section boosts I_{ON}, and large band-gap semiconductor material in the drain section suppresses I_{OFF}. Therefore, in this paper, we reported a $Si_{0.6}Ge_{0.4}$/Ge heterojunction (HJ) DLTFET with a high-κ dielectric (HD) to boost performance concerning DC and analog/RF performance parametric. In HJ HD DLTFET, for the first time, to the best of the authors' insight, Ge is used as source and the channel region, and $Si_{0.6}Ge_{0.4,}$ being a wide band-gap semiconductor material, is used in the drain region.

The remaining paper is arranged in a subsequent manner. Section II pronounces the physical parameters of HJ HD DLTFET and simulation models used in the simulation to define physics and charge carrier movement in the device. Section III articulates the relative analysis of the HJ HD DLTFET with the conventional DLTFET, concerning DC and analog/RF attributes. In the last, section IV delivers the conclusion.

2 Device Structure and Simulation Setup

2.1 Device Structure

The cross-sectional interpretation of the DLTFET and HJ HD DL TFET is displayed in Fig. 1a and b, respectively. In HJ HD DLTFET, the source and channel region employ germanium (Ge) [23, 24], and the drain region employs $Si_{0.6}Ge_{0.4}$ [25, 26]. The small band-gap, high mobility, small tunneling masses, and compatibility with silicon make Ge an ideal substitute for silicon. The p^+ and n^+ areas are induced in the source and the drain, respectively, using the CP concept. In HJ HD DLTFET, the work function of the drain, channel, and source metal electrode is 4.2, 4.6, and 5.93 eV, respectively. Two spacers, i.e., HfO_2 and SiO_2, having a dielectric constant of 22 and 3.9, are used at drain-channel electrode and source-channel electrode, respectively [27]. Additionally, TiO_2 is used as a gate dielectric to reduce the large offset current associated with the small band-gap semiconductor material (Ge) of the source and intrinsic channel area [28]. The device design requirements considered for the simulation are listed in Table 1.

2.2 Simulation Setup

The TCAD simulator that has been used for the simulation of the conventional DLTFET, as well as HJ HD DLTFET [29], is Silvaco ATLAS. The lateral BTBT is accounted by the Wentzel-Kramers-Brillouin (WKB) method and nonlocal BTBT (NONLOCAL . BBT) model. The intrinsic carrier concentration and mobility effects are addressed by Fermi–Dirac statistics (NI . FERMI), Shockley–Read–Hall generation-recombination model [30], and Lombardi mobility model (CVT).

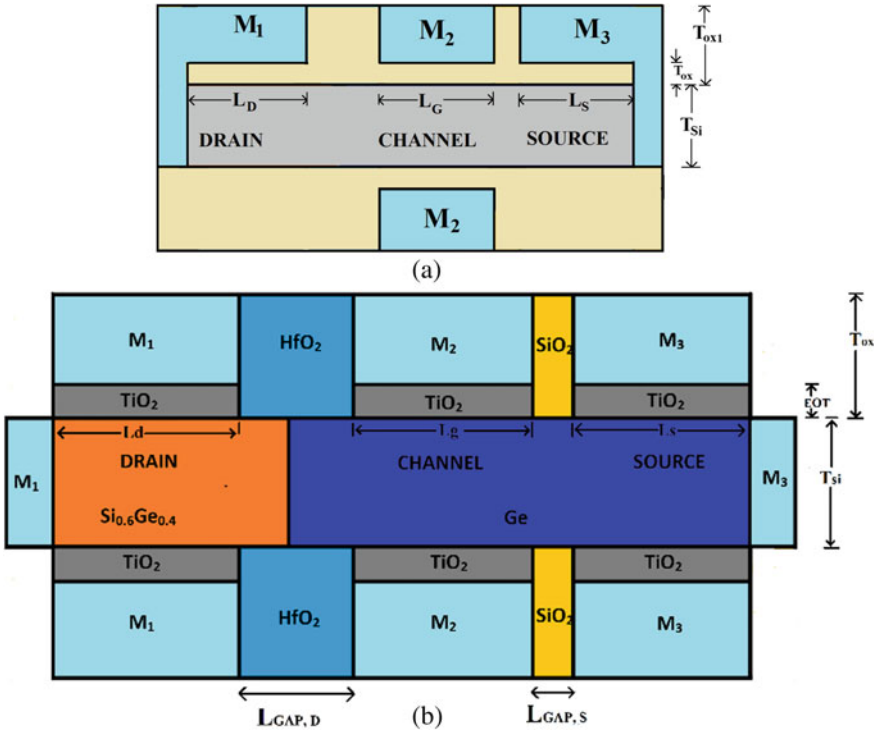

Fig. 1 A cross-sectional view of **a** DLTFET, **b** HJ HD DLTFET

Table 1 Device dimensions

Parameter	Symbol	Value	Unit
Channel length	L_g	20	nm
Source length	L_s	20	nm
Drain length	L_d	20	nm
Oxide thickness	T_{ox}	5	nm
Equivalent oxide thickness	EOT	1	nm
Gate-drain spacer length	$L_{GAP, D}$	10	nm
Gate-source spacer length	$L_{GAP, S}$	5	nm
Source electrode WF	M_3	5.93	eV
Gate electrode WF	M_2	4.6	eV
Drain electrode WF	M_1	4.2	eV
Silicon thickness	T_{Si}	5	nm

Furthermore, trap assisted tunneling (TAT) model and Hansch model are exploited to address ambipolar state and quantum confinement effects, respectively.

3 Results and Discussions

Figure 2a shows the energy band diagram (EBD) over the device length for HJ HD DLTFET under the off-state in which the V_G is kept at 0 V and V_D of 0.3 V is applied, resulting in the presence of energy barrier over the source-channel boundary, ensuing in inhibition of BTBT as the valence band of the source section is unaligned with the conduction band of the channel. Consequently, little values of current flow in the off-state. However, under the on-state in which V_G of 1.5 V and V_D of 0.3 V is applied, the energy barrier is reduced across the source-channel interface because small band-gap semiconductor material is used in the source section of the device. The EBD over the device length for HJ HD DLTFET under on-state is illustrated in Fig. 2b.

Furthermore, the comparative analysis of the transfer characteristics for conventional DLTFET and HJ HD DLTFET at V_D of 1.0 V and 0.3 V is demonstrated in Fig. 3a and b, respectively. The transfer characteristics are compared at V_D = 1.0 V, as the conventional DLTFET had shown its results at this drain voltage [17]. However, the HJ HD DLTFET shows excellent characteristics at even $V_D = 0.3$ V, proving its potential benefit to operating as a low voltage and energy-efficient device. It can be perceived from Fig. 5 that HJ HD DLTFET demonstrates I_{ON} of the order of 10^{-3} A/μm because Ge is applied at the source side, which enables more band bending and higher electron tunneling.

Additionally, it can be presented that the high band-gap material ($Si_{0.6}Ge_{0.4}$) applied at the drain side enables to maintain small values of the off-state current as well as ambipolar current. For $V_D = 0.3$ V and $V_G = 1.5$ V, HJ HD DLTFET obtains $I_{ON} \sim 1.2 \times 10^{-3}$ A/μm, $I_{OFF} \sim 3 \times 10^{-17}$ A/μm, I_{ON}/I_{OFF} ratio ~ 10^{14} and SS_{avg} ~ 36.14 mV/decade.

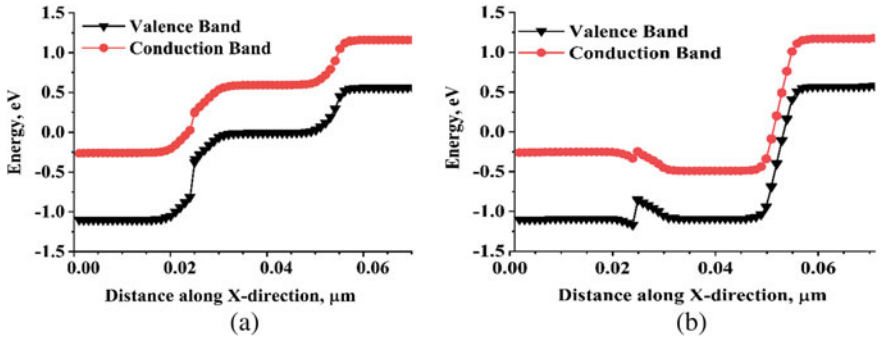

Fig. 2 EBD for HJ HD DLTFET under **a** off-state, **b** on-state

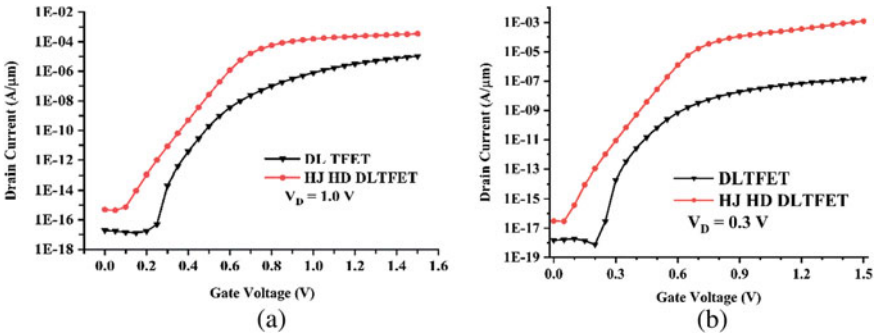

Fig. 3 Variation in transfer characteristics for conventional DLTFET and HJ HD DLTFET with gate voltage **a** $V_D = 1.0$ V, **b** $V_D = 0.3$ V

Now, analog/RF figures of merit (FoMs) of the device, which include transconductance (g_m), gate-to-drain capacitance (C_{gd}), cut-off frequency (f_T), and gain-bandwidth product (GBP) are discussed.

Among these, g_m performs a significant character to advance the performance of the device as it is a vital device design constraint, which translates the applied gate voltage into drain current [31] and is stated as:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{1}$$

Figure 4 compares the transconductance of DLTFET and HJ HD DLTFET concerning gate voltage on the horizontal axis and illustrates that g_m of HJ HD DLTFET is greater than that of DLTFET as it is a reflection of the enhanced current drivability.

At high frequencies, parasitic capacitances, for instance, gate-to-drain capacitance (C_{gd}) and gate-to-source capacitance (C_{gs}), affects device performance significantly as these capacitances provide a feedback pathway amid input and output signal, ensuing in parasitic fluctuations and later distortion of the signal. For TFETs, C_{gd} dominates due to the formation of the inversion sheet of the electron over the gate dielectric boundary in the channel area [32] and is formulated as:

$$C_{gd} = \frac{\partial Q_G}{\partial V_D} \tag{2}$$

The HJ HD DLTFET offers marginally more C_{gd} than conventional DLTFET at higher V_G, as demonstrated in Fig. 5 due to enhanced density of conduction states and capacitive coupling [33], resulting in the formation of significant energy barrier at drain-channel junction. Furthermore, f_T is a significant factor for the usage of the device in wireless and RF applications [34]. The frequency whereat the short circuit device gain advances toward unity serves as cut-off frequency and is stated as:

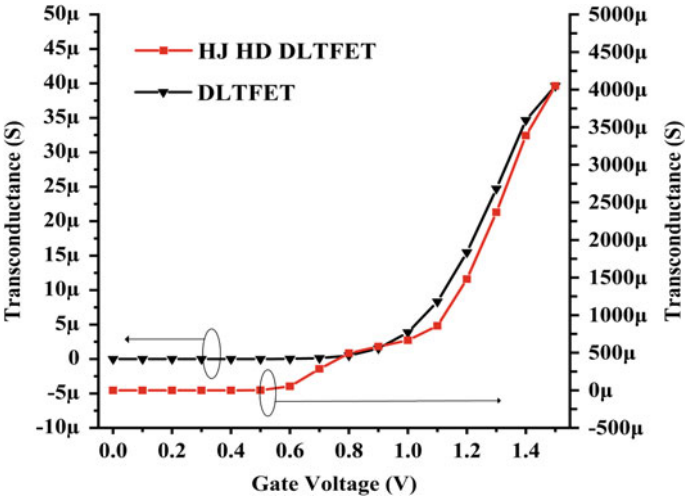

Fig. 4 Variation in transconductance for conventional DLTFET and HJ HD DLTFET with gate voltage

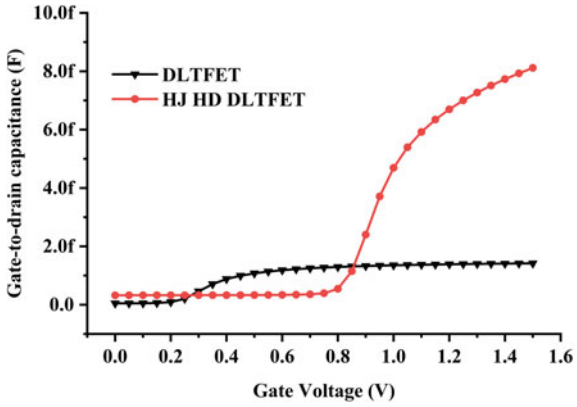

Fig. 5 Variation in gate-to-drain capacitance for conventional DLTFET and HJ HD DLTFET with gate voltage

$$f_{\mathrm{T}} = \frac{g_{\mathrm{m}}}{2\prod\left(C_{\mathrm{gd}} + C_{\mathrm{gs}}\right)} \tag{4}$$

It can be shown from Fig. 6 that initially, as gate voltage increases, f_{T} increases due to increment in g_{m}. Then, as the gate voltage increases, f_{T} falls after a particular gate voltage because the parasitic capacitances increase at higher V_{G}.

Besides f_{T}, the GBP is also a vital device design parameter for RF applications and provided for a DC gain often [35]. It can be stated as:

$$\mathrm{GBP} = \frac{g_{\mathrm{m}}}{20\prod C_{\mathrm{gd}}} \tag{5}$$

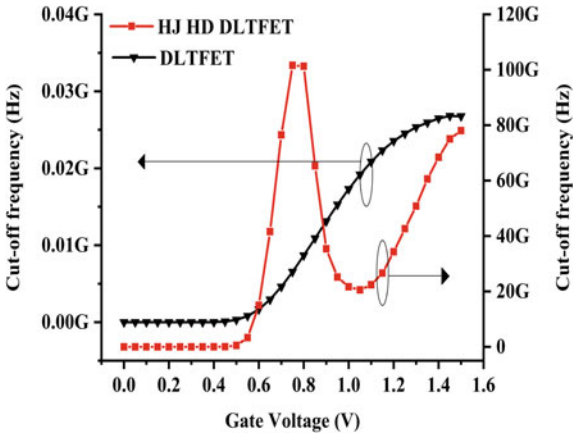

Fig. 6 Variation in cut-off frequency for conventional DLTFET and HJ HD DLTFET with gate voltage

Furthermore, it can be illustrated from Fig. 7 that HJ HD DLTFET obtains higher GBP in comparison with conventional DLTFET. As gate voltage increases, GBP initially increases owing to substantial growth in g_m, albeit it declines for higher values of V_G as a result of an increase in parasitic capacitances. It can be concluded that higher GBP explains more significant device gain, coupled with high bandwidth for HJ HD DLTFET in comparison with conventional DLTFET. Additionally, the graph of GBP also follows the trend of cut-off frequency, and the reason is pronounced from the formula.

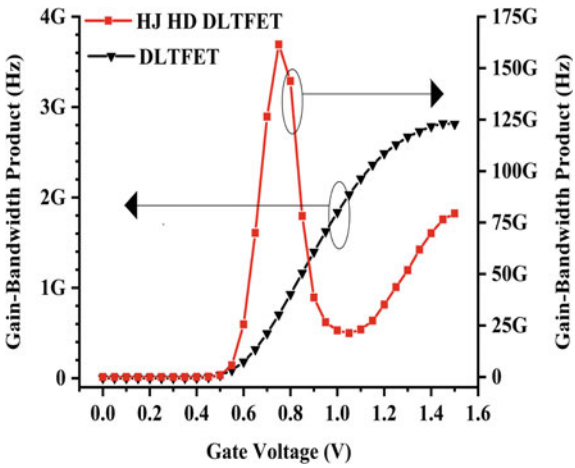

Fig. 7 Variation in gain-bandwidth product for conventional DLTFET and HJ HD DLTFET with gate voltage

Table 2 Comparison of electrical device characteristics of DLTFET and HJ HD DLTFET at different V_D and V_G

Computed at		Parameters	DLTFET	HJ HD DLTFET
V_D (V)	V_G (V)			
0.3	0.0	I_{OFF} (A/μm)	1.4×10^{-18}	3.01×10^{-17}
	1.0	I_{ON} (A/μm)	3.2×10^{-8}	1.74×10^{-4}
	1.5	I_{ON} (A/μm)	1.41×10^{-7}	1.2×10^{-3}
		SS_{avg} (mV/dec)	17.83	36.14
0.5	0.0	I_{OFF} (A/μm)	1.5×10^{-17}	6.7×10^{-17}
	1.0	I_{ON} (A/μm)	1.98×10^{-7}	1.6×10^{-4}
	1.5	I_{ON} (A/μm)	1.1×10^{-6}	6.7×10^{-4}
		SS_{avg} (mV/dec)	17.9	37.13
1.0	0.0	I_{OFF} (A/μm)	1.95×10^{-17}	4.8×10^{-16}
	1.0	I_{ON} (A/μm)	8.04×10^{-7}	1.6×10^{-4}
	1.5	I_{ON} (A/μm)	1.06×10^{-5}	3.8×10^{-4}
		SS_{avg} (mV/dec)	35.64	45.52

4 Conclusion

In this manuscript, we have designed and studied an HJ HD DLTFET based on the CP concept with the high-κ dielectric and spacer engineering to improve device operation for analog/RF applications. From this perspective, the comparative analysis for both the devices (i.e., conventional DLTFET and HJ HD DLTFET) for the different gate and drain voltages is listed in Table 2. The presence of high-κ gate dielectric (i.e., TiO_2) effectively reduces off-state current associated with the utilization of low band-gap semiconductor material in the source area. Additionally, the simulation results of the HJ HD DLTFET demonstrate noteworthy enhancement in I_{ON} (~1.2×10^{-3} A/μm) and low I_{OFF} (~3×10^{-17} A/μm) ensuring enhanced I_{ON}/I_{OFF} ratio (~10^{14}) at a low $V_D = 0.3$ V. This makes HJ HD DLTFET a potential candidate for progression of CMOS in low power analog/RF and IoT applications. Furthermore, reliability and circuit analysis can be explored in the future for several sensor devices.

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Synthesis of Thinned Antenna Arrays Using Salp Swarm Optimization Techniques

Amiya Kumar Mondal and Prerna Saxena

1 Introduction

An antenna is a device used to transmit and/or receive radio waves [1]. In single element antenna, the main drawback is limited gain. There are some ways to improve the gain of antennas such as changing their structure and expanding the length and aperture area. Expanding aperture area and the length of antennas is infeasible [1]. On the other hand, antenna arrays provide high gain, high directivity and beam steering capabilities.

The thinning process in an antenna array involves removing some antenna elements from the antenna array to achieve the same radiation characteristics as a fully populated array. The different radiation characteristics of the antenna array, such as gain, half power beam width, directivity and MSLL, can be optimized by steering parameters, such as amplitude excitation coefficients, inter-element spacing and relative phases, along with the geometrical arrangement of an array. The main motivation for antenna array thinning is the reduction of power utilization, cost and weight. Many optimization techniques have been used for array thinning such as, analytical methods involving binomial distribution, iterative FFT techniques [2] and differential evolution (DE) [3]. Recently, several nature inspired metaheuristic techniques have been proposed for antenna array thinning. These include Particle Swarm Optimization (PSO) [4], Genetic Algorithm (GA) [5], Binary Butterfly Mating Optimization (BBMO) [6] and Ant Colony Optimization (ACO) [7]. Metaheuristics offer advantages of implementation ease, improved radiation pattern characteristics and reformed optimization speed.

In this paper, novel swarm intelligence techniques, Salp Swarm Algorithm (SSA) and Binary Salp Swarm Algorithm (BSSA) have been proposed for optimization

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of large LAA. SSA is a metaheuristic algorithm whose motivation is swarming behaviour of salps in the deep sea. The SSA algorithm has been applied in three-bar truss design, cantilever beam design, welded beam design, 2D airfoil design and marine propeller design for optimization problems [8]. Compared with deterministic methods, the main motivation for using metaheuristics is their ability to deal with non-differentiability and optimize discontinuous objective functions. In this paper, SSA and BSSA are proposed for antenna array optimization for the first time, to the best of the authors' knowledge. The SSA and BSSA are proposed for LAA thinning, suppression of MSLL as well as minimization of SLL.

The rest of the paper is organized as follows. In Sect. 2, the problem formulation has been discussed. Section 3 conducts a comprehensive analysis of SSA optimization and describes the detailed steps with a flow chart. The binary salp swarm optimization algorithm, along with its flow chart, is discussed in Sect. 4. The design examples and obtained results for array thinning are verified by comparing with other state-of-the-art approaches and are represented in Sect. 5. The concluding remarks are made in Sect. 6.

2 Problem Formulation

The geometrical arrangement of LAA is given in Fig. 1. The array comprises of symmetrically placed $2N$ isotropic elements with respect to the x-axis. The array factor (AF) taken at an angle (θ) in $x-z$ plane is computed as [6].

$$\mathrm{AF}(\theta) = 2\sum_{n=1}^{N} I_n \cos\left(\frac{2n-1}{2} \times \beta x_n \cos\theta + \varphi_n\right) \tag{1}$$

where the nth element excitation amplitude is represented by I_n, φ_n is phase of nth element, $\beta = (2\pi)/\lambda$ and x_n is the position of nth element. In the antenna array thinning, if the state of the nth element is 'off', the excitation amplitude I_n is 0; if the state of the nth element is 'on', the excitation amplitude I_n is 1. The spacing between elements is assumed as 0.5λ, and the phase excitation of all elements is uniform, i.e. ($\varphi_n = 0$). Thus, (1) can be rewritten as

$$\mathrm{AF}(\theta) = 2\sum_{n=1}^{N} I_n \cos(\pi \times (n-0.5)\cos\theta) \tag{2}$$

For antenna array thinning,

$$I_n = \begin{cases} 0, & \text{if } n\text{th element is 'off'} \\ 1, & \text{if } n\text{th element is 'on'} \end{cases} \tag{3}$$

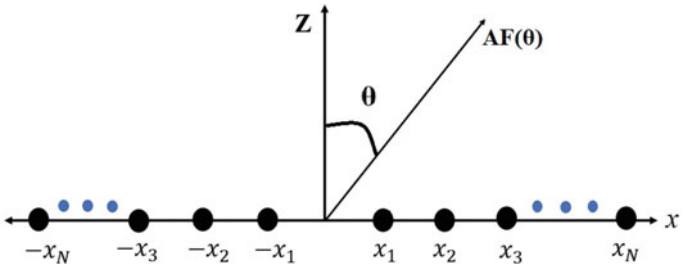

Fig. 1 The geometry of a symmetrical LAA

The MSLL is recognized as fitness function so as to minimize the MSLL, and it is formulated as,

$$F_{\mathrm{MSLL}}(I) = \max_{\forall\theta\in R}\left\{20\log\left|\frac{\mathrm{AF}(I,\theta)}{\mathrm{AF}_{\max}}\right|\right\} \tag{4}$$

where R represents the sidelobe region without considering the main beam, $\mathrm{AF}_{\max}$ is the maximum array factor.

3 Salp Swarm Algorithm

SSA is one of the recently developed optimization algorithms which is nature inspired [8]. SSA utilizes the principle of bionics which states that salps frequently form a swarm in deep ocean known as salp chain. In the salp population, the leader is placed in the beginning, and the remaining salps are assumed as followers in the chain. The conduct of swarm is like follower salps travel at the back of the main salp. The leading salp travels towards food sources. If the food source is replaced with the aid of the most reliable source globally, automatically the salp chain moves in the direction of it. The SSA is mathematically modelled as follows.

In SSA, the salps area is described in an n-dimensional search space. It is presumed that a food source F placed inside the search space as the prey for the swarm. The main steps of the algorithm are summed up as follows.

3.1 Position Update

It is recommended to use the equation given below to upgrade the position of the leader:

$$x_j^1 = \begin{cases} F_j + C_1((ub_j - lb_j)C_2 + lb_j) & C_3 \geq 0 \\ F_j - C_1((ub_j - lb_j)C_2 + lb_j) & C_3 < 0 \end{cases} \tag{5}$$

where the position of the leader in jth dimension is represented by x_j^1, ub_j and lb_j indicates the upper and lower bound in jth dimension, the food source position in jth dimension is represented as F_j, and the distributed random numbers in the interval [0, 1] are represented by C_1, C_2 and C_3.

Equation (5) describes that relative to the food source, the leader only promotes its location. The coefficient C_1 balances exploration and development, so it is the significant parameter in SSA. It is expressed as (6).

$$C_1 = 2\mathrm{e}^{-\left(\frac{4l}{L}\right)^2} \tag{6}$$

where the present iteration is represented by l and the utmost number of iterations is represented by L.

3.2 Distance Computation

In order to update the location of the follower, the equation given below is used to calculate the distance between the followers (Newton's law of motion):

$$x_j^i = \frac{1}{2}at^2 + v_0 t \tag{7}$$

where $i \geq 2$, the time is represented by t, the location of ith follower salp in jth dimension is represented by x_j^i, initial speed is represented by v_0 and $a = \frac{v_{final}}{v_0}$ where $v = \frac{x - x_0}{t}$. Considering $v_0 = 0$ and the distinction between iterations is unity, this equation can be rewritten as:

$$x_j^i = \frac{1}{2}\left(x_j^i + x_j^{i-1}\right) \tag{8}$$

The salp chains can be simulated using (5) and (8). In Fig. 2, the flow chart describes the steps involved in SSA optimization.

4 Binary Salp Swarm Algorithm

The BSSA is applied to solve general binary optimization problems. The variable representing the on/off state in the thinned antenna array is binary. By using the basic crux of SSA, the BSSA algorithm for binary optimization is proposed [9]. The mathematical model of the BSSA is summarized below.

The puddle of solutions in BSSA is represented by a value of 0 and 1. The buffer position is updated accordingly through a 0–1 bit flip operation. This flipping operation is done by means of a threshold value associated with the transfer function.

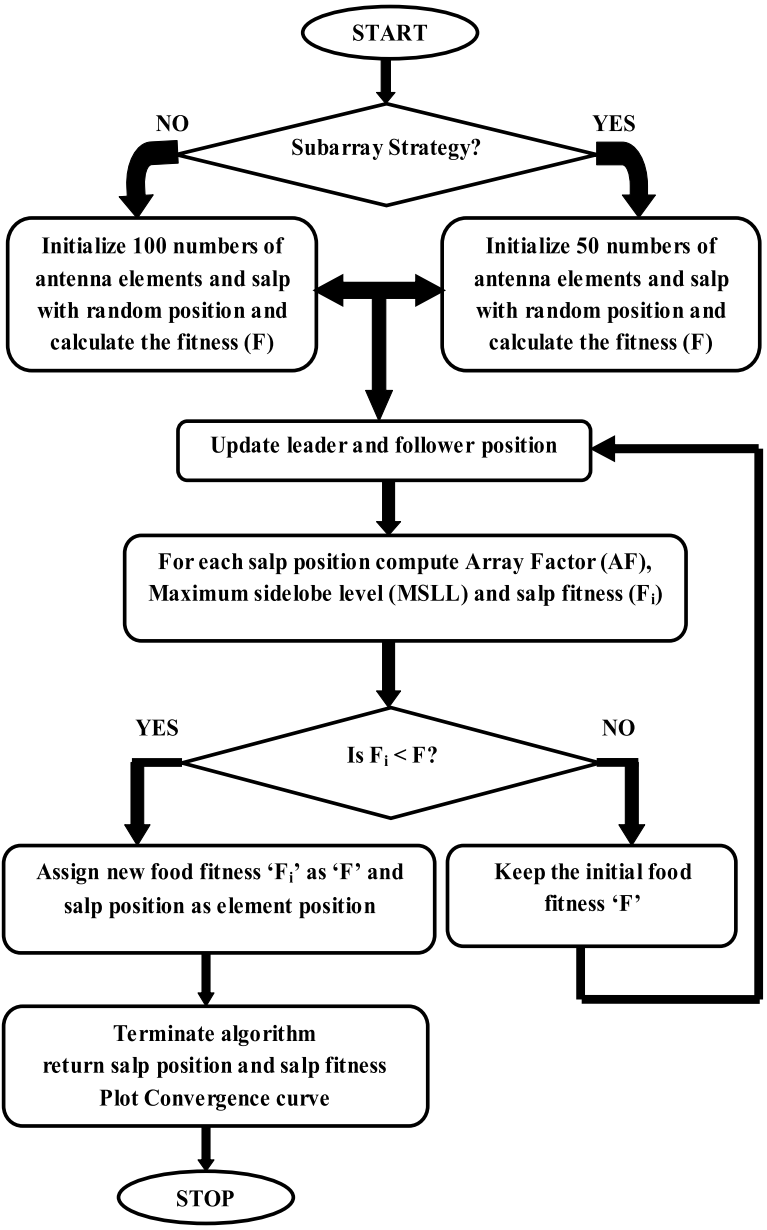

Fig. 2 Flow chart showing the optimization steps through the proposed method SSA

For position update in the binary scheme, a tangent hyperbolic transfer function is introduced. The tangent hyperbolic transfer function is expressed as $T(x_i^j(t+1))$ and formulated as,

$$T(x_i^j(t+1)) = \tanh(x_i^j(t+1)) = \frac{e^{(2x_i^j(t+1))} - 1}{e^{(2x_i^j(t+1))} + 1} \tag{9}$$

Accordingly, the position upgrade is as follows:

$$\Delta_i^j(t+1) = \begin{cases} 1 & \text{if } T(x_i^j(t+1)) > \lambda_1 \\ 0 & \text{otherwise} \end{cases} \tag{10}$$

where distributed random number over 0 and 1 is represented by λ_1. The flow chart describing the steps involved in BSSA optimization is depicted in Fig. 3.

5 Results and Discussion

In this section, the proposed approaches (with and without subarray strategy) are used to achieve the thinning of antenna array. MATLAB is used to implement the algorithms on Intel Pentium (R), 3.5 GHz processor with 4 GB RAM.

5.1 Thinning and Suppression of MSLL Using SSA and BSSA Without Subarray Strategy

A linear antenna array, having 100 elements that are placed symmetrically along the x-axis with an inter-element spacing of 0.5λ, is considered, and the proposed approaches (SSA and BSSA) are used for optimization and thinning. It is assumed that the phase excitation is uniform($\varphi_n = 0$). 100 independent runs are carried out with 300 iterations each, and the average of 100 runs is reported. Firstly, the proposed method (SSA) is used to optimize the antenna currents. The LAA thinned pattern acquired by using SSA is represented in Fig. 4. The MSLL acquired by SSA is −17.12 dB. The number of antenna elements 'on' after optimization is 72, and the number of antenna elements 'off' is 28. Figure 5 represents the status of optimized antenna elements.

Next, to optimize the antenna currents, the BSSA has been proposed. It is assumed that the phase excitation is uniform ($\varphi_n = 0$) with symmetrically placed antenna elements at a uniform inter-element spacing of 0.5λ. Figure 6 depicts the thinned LAA pattern achieved by the BSSA algorithm. The MSLL acquired by BSSA is −19.82 dB. The number of antenna elements 'on' after optimization is 76, and the

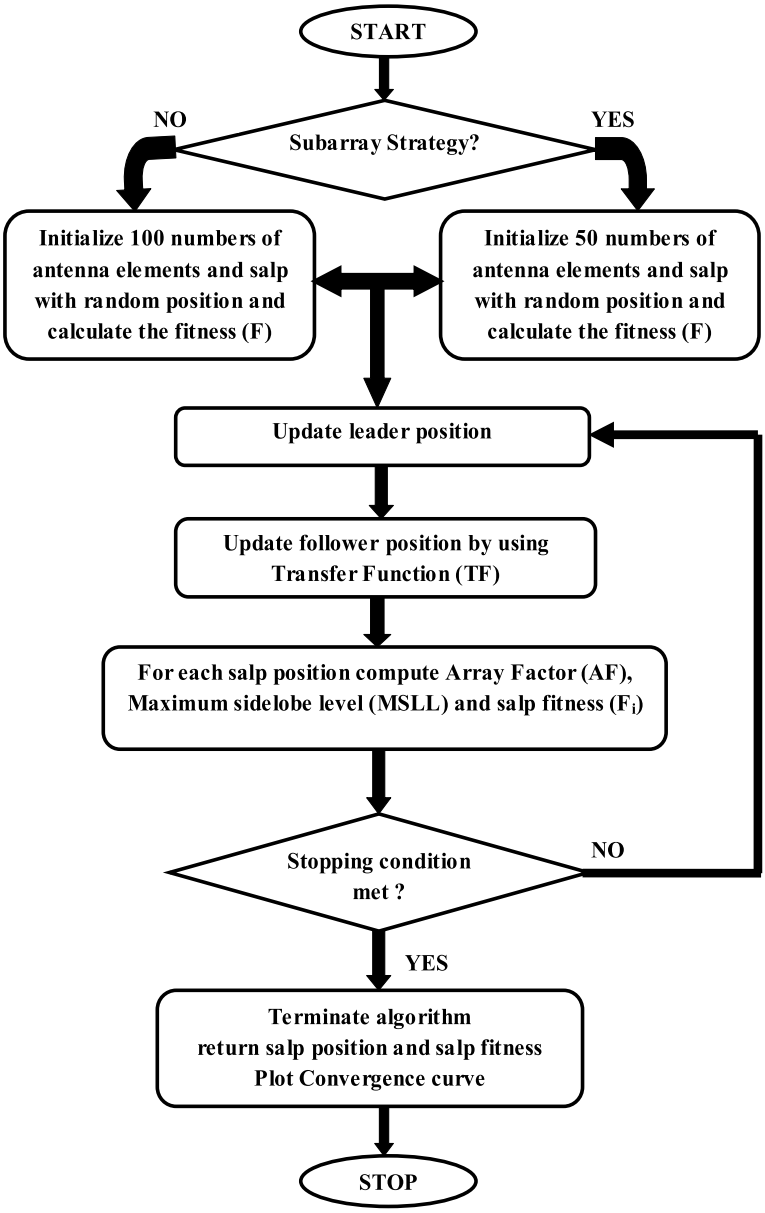

Fig. 3 Flow chart showing the steps involved in the proposed method BSSA optimization

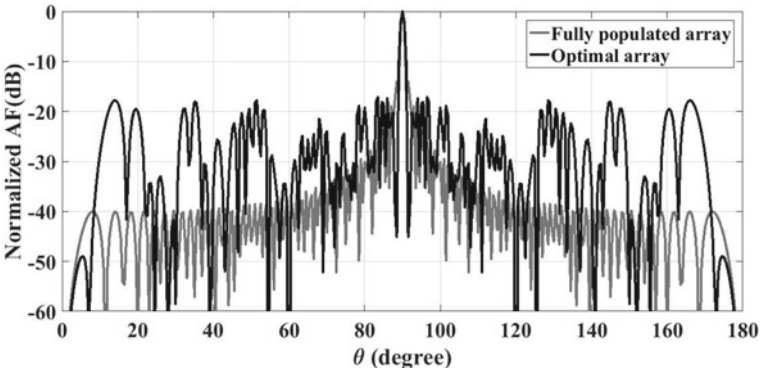

Fig. 4 Array pattern of the thinned LAA using proposed approach SSA

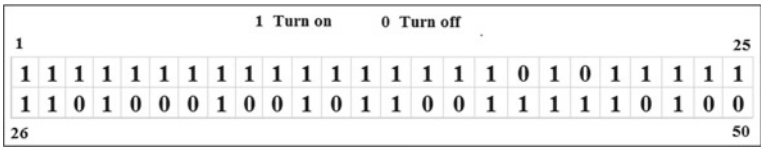

Fig. 5 The element status obtained by SSA

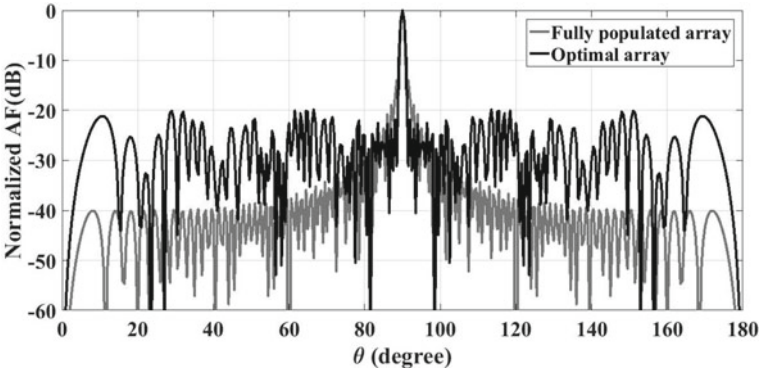

Fig. 6 Array pattern of the thinned LAA using proposed approach BSSA

number of antenna elements 'off' is 24. Figure 7 represents the status of optimized antenna elements.

Figure 8 represents the convergence curves of SSA and BSSA to obtain the best fitness value. It can be clearly seen that BSSA is faster than SSA and only requires 86 iterations to converge to the optimal value.

To validate the performance of the proposed algorithms, their performance is compared with other existing optimization techniques, and the results are summarized in Table 1. The results depict that the MSLL of −19.82 dB acquired by the proposed

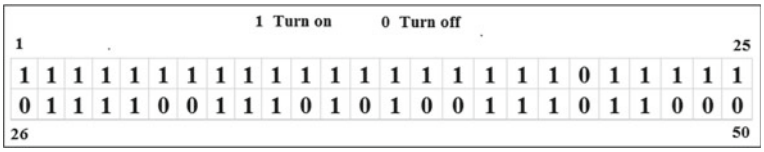

Fig. 7 The element status obtained by BSSA

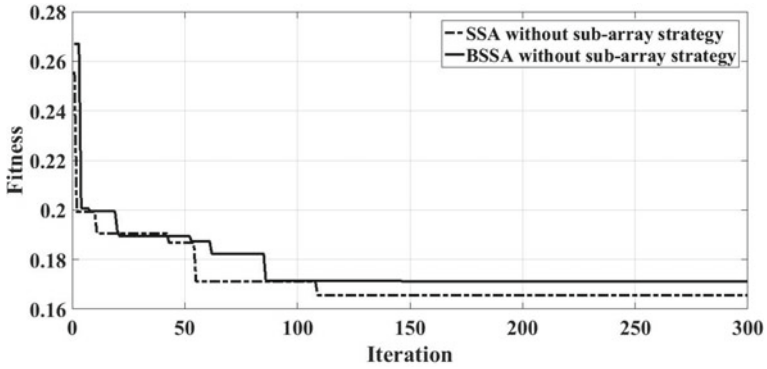

Fig. 8 Convergence curve

method BSSA is lower than BPSO [4], BGA [5], BBMO [6], ACO [7], BDE [10] and SSA but higher than CBPSO [4] and IBIWO [11]. The percentage of thinning acquired by BSSA is 24% which is more than BPSO [4], ACO [7], BDE [10] and IBIWO [11], but SSA obtained the best thinning percentage of 28%. In addition, other state-of-the-art approaches such as Biogeography-Based Optimization (BBO) [12], Real-Coded Genetic Algorithm (RGA) [13] and Immunity Genetic Algorithm (IGA) [14] give a maximum side lobe level of around −20 dB; however, the number of iterations required for convergence for RGA and IGA is very large, and the thinning percentage (22%) is lower for BBO. The thinning percentage obtained by Binary Genetic Algorithm (BGA) [5] is 24%; however, the MSLL is very high (−16.5 dB), and it requires 150 iterations to converge.

A very recently proposed technique, brainstorm optimization (BSO) [15] offers a very high thinning percentage of 44%; however, it takes 160 iterations to converge and results in a high MSLL of −17 dB. Table 1 also summarizes the performance of the Iterative Fast Fourier Transform (IFFT) [2] and the hybrid technique based on differential evolution (DE) and Iterative Fourier Transform (IFT) [3]. It is seen that though these methods result in a reduced maximum side lobe level of around −22 dB, they have drawbacks in terms of a lower thinning percentage and a large convergence time. A higher thinning percentage is required for reducing the power requirements, weight, as well as array cost.

Mostly thinned arrays find applications in satellite communications, radio astronomy, ground-based radars, etc. From Table 1, it is seen that there exists a trade-off

Table 1 Performance summary and comparison with the results with the state-of-the-art approaches without using subarray strategy

Approach	MSLL (dB)	Number of antenna elements 'ON'	Thinning percentage (%)	Convergence iterations
Fully populated	−13.73	100	0	0
IFFT [2]	−22.90	154	23	10,000
IFT-DE [3]	−22.20	80	20	100
BPSO [4]	−14.60	80	20	236
CBPSO [4]	−21.29	76	24	181
BGA [5]	−16.50	76	24	150
BBMO [6]	−19.80	76	24	62
ACO [7]	−19.10	80	20	203
BDE [10]	−18.50	78	22	193
IBIWO [11]	−22.04	78	22	200
BBO [12]	−20.84	78	22	40
RGA [13]	−20.56	78	22	300
IGA [14]	−20.24	80	20	1000
BSO [15]	−17.00	56	44	160
Proposed approach (SSA)	**−17.12**	**72**	**28**	**109**
Proposed approach (BSSA)	**−19.82**	**76**	**24**	**86**

between the obtained MSLL, thinning percentage and the convergence time. It is observed that the proposed technique(BSSA) strikes a good balance between all these conflicting parameters and provides a low MSLL of −19.82 dB with 24% thinning and takes only 86 iterations to converge, which makes it suitable for real-time applications.

5.2 *Thinning and Suppression of MSLL Using SSA and BSSA with Subarray Strategy*

This part highlights SSA and BSSA utilizing subarray strategy for thinning of LAA. In subarray approach, the linear array is partitioned into portions, one section with a certain range of antennas turned 'on' forming the first subarray and the rest of the antennas on the edge of array creating another subarray. One part is named as front linear array which is 'on' always, and another part is named as back linear array which is optimized. The proposed approaches (SSA and BSSA) are used for optimization of these 50 elements.The proposed approach SSA algorithm with subarray strategy

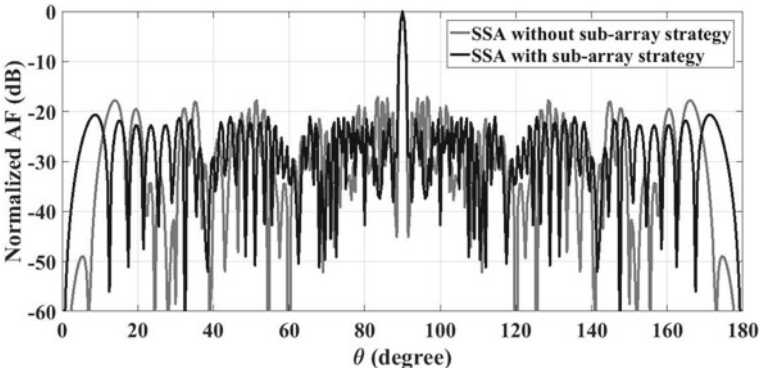

Fig. 9 Array pattern of the thinned LAA using proposed approach SSA with subarray strategy

1 Turn on 0 Turn off

1																								25
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	0	1	0	0	1	1	0	0	1	0	1	0	1	0	0	0	0	0	1	1	1
26																								50

Fig. 10 The element status obtained by SSA

is used to optimize the antenna currents. It is assumed that the phase excitation is uniform ($\varphi_n = 0$) with symmetrically placed antenna elements.

Figure 9 shows that the thinned LAA pattern is obtained using SSA. The MSLL acquired by SSA incorporating subarray strategy is −20.7 dB. After optimization, the total number of 'on' antenna elements is 74, whereas that in 'off' state is 26. Figure 10 represents the status of optimized antenna elements.

Next, the proposed approach BSSA algorithm with subarray strategy is applied to optimize the antenna currents. The thinned LAA pattern acquired by using BSSA algorithm with subarray strategy is depicted in Fig. 11. Using BSSA with subarray strategy, the MSLL acquired is −21.08 dB. The number of antenna elements 'on' after optimization is 76, and the number of antenna elements 'off' is 24. Figure 12 represents the status of optimized antenna elements.

The convergence curves of SSA and BSSA to obtain the best fitness value through the subarray strategy are represented in Fig. 13. It is observed that the execution of BSSA is faster than SSA, and it only takes 59 iterations to converge to the optimal value. To validate the performance of proposed algorithms with subarray strategy, comparison with other existing approaches is carried out, and results are shown in Table 2.The proposed approach BSSA obtains the best MSLL, i.e. −21.08 dB which is lower than SSA but more than BBMO [6]. The percentage of thinning acquired by BSSA is 24% which is more than BBMO by 4%. However, comparing the results with the existing state-of-the-art methods, SSA obtains the best thinning percentage 26% through the subarray strategy.

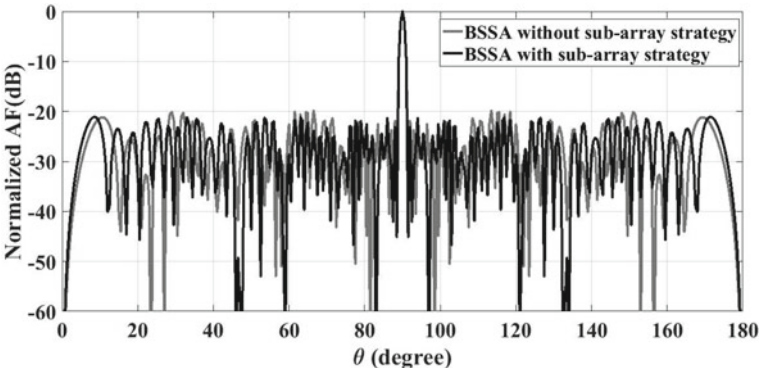

Fig. 11 Array pattern of the thinned LAA using proposed approach BSSA with subarray strategy

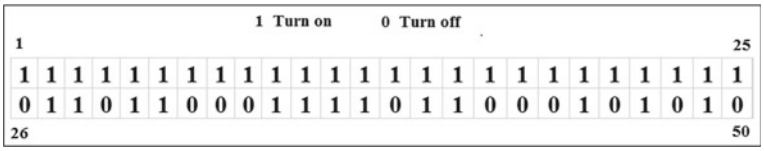

Fig. 12 The element status obtained by BSSA

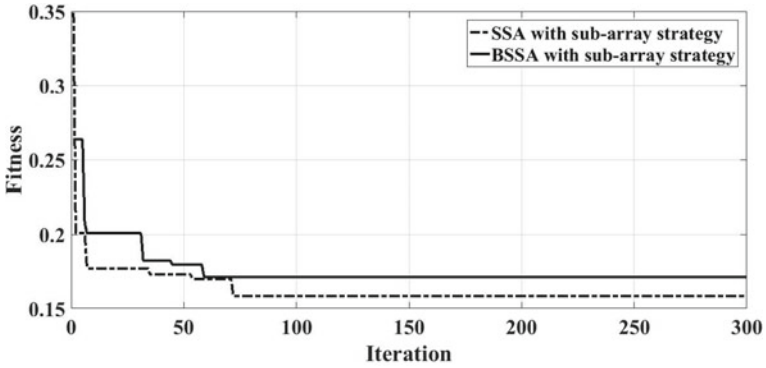

Fig. 13 Convergence curve

6 Conclusion

The thinning of antenna arrays decreases power requirements, weight, as well as array cost. In this paper, antenna array thinning has been done by using proposed novel metaheuristic techniques SSA and BSSA. Using these proposed approaches, the synthesis and thinning of 100-element antenna array were proposed. It has been shown that the maximum SLL obtained with the proposed method SSA is −17.12 dB and by using BSSA is −19.82 dB. The achieved thinning percentage is 28% and

Table 2 Performance summary and comparison with the results with the state-of-the-art approaches using subarray strategy

Approach	MSLL (dB)	Number of antenna elements 'ON'	Thinning percentage (%)	Convergence iterations
BBMO [6]	−22.60	80	20	38
Proposed approach (SSA)	**−20.70**	**74**	**26**	**72**
Proposed approach (BSSA)	**−21.08**	**76**	**24**	**59**

24%, respectively. By applying subarray strategy with the proposed approaches, the maximum SLL acquired by using SSA is −20.7 dB and by using BSSA is −21.08 dB. The obtained thinning percentage is 26% and 24%, respectively. In addition, the BSSA with subarray strategy converges more quickly than the other state-of-the-art optimization methods. The effectiveness of the proposed approaches is illustrated by comparing with other state-of-the-art approaches. The proposed thinned arrays find applications in satellite communications, radio astronomy, ground-based radars, etc.

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Comparative Analysis of a Dopingless Tunnel FET and MOSFET-Based Current Mirror

Harihar Nath, Suruchi Sharma, Abhishek Verma, and Baljit Kaur

1 Introduction

MOSFET is a metal oxide semiconductor field effect transistor, which is a voltage control device. With the advancement of technology day by day, the rapid down-scaling of the MOSFET technology is helping to scale down the source voltage and thereby increases the current driving capacity with the reduced power supply. However, the higher leakage by the off-state (current leakage during the off-state of the MOSFET) has always been detrimental to MOSFET technology. This paper is about in helping to overcome such limitations which include:

- Restrictions to subthreshold swing (SS) to 60 mV/dec.
- Random dopant fluctuation (RDF)
- Drain induced barrier lowering (DIBL)
- Short channel effects (SCEs) [1–4].

by adopting the conventional doped TFET [5–7] with low off-state leakage current. DLTFET [8–10] was introduced to produce large on-state current and neutralize doping variability. DLTFET also has a low thermal budget.

1.1 Dopingless TFET

In the last few years, several papers have been published on the Tunnel FET. Tunnel FET has been introduced to lift the limitations of MOSFETs such as SCEs ad SS. Owing to the actual doping of atoms, the on-current of the Tunnel FET was very low due to the RDF. Kumar et al. used the plasma charging theory to evaluate the

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source and drain of the tunnel FET [8] (known as Dopingless Tunnel FET), and the ion implantation technique for the tunnel FET is not necessary now. In order to increase the on-current, he also strengthened the BTBT. Sharma et al. proposed another DLTFET [11] in which work function engineering was also introduced which means the source and drain were generated using two separate working function metals. The novel DLTEFT was proposed by Nigam et al. [12] with the control gate of dual material; holes were induced in the source using platinum metal working function 5.93 eV, and electrons were induced in the drain with the aid of Hafnium metal working function 3.9 eV. Yadav et al. [13] suggested another DLTFET to replace the traditional TFET, in which he used InAs material (hetero material) to reduce the source-channel lateral tunneling distance, which helped to increase the on-current by improving the BTBT intensity, which is a narrow band gap material in Si position in the source area. Harris et al. [14] suggested a DLTFET hetero structure in which GaAs material was used to minimize the off-current without affecting the on-current in the drain area. He also made the traditional DLTFET better by adding the metallic layer between the gate oxide and the source interface that lowered the SS and increased the on-current. Another DLTFET that is used for the circuit in this paper was proposed by Verma et al. [15]. DLTFET's sectional cross-view is shown at Fig. 1, and there are physical parameters in Table 1. For the source region with *p*+ and drain region with *n*+ platinum, the charge plasma principle was used to create the holes in the source region, and Hafnium was used to generate electrons in the drain region. In order to increase the on-current, a strip of GaAs is inserted between the channel and the source since its electron mobility is 8500 cm^2/Vs, which increases electron tunneling at the channel and source interface. During the off-state, the electron of the valence band (VB) of the drain cannot pass to the conduction band (CB) of the source because the bands are not aligned; when they are aligned during

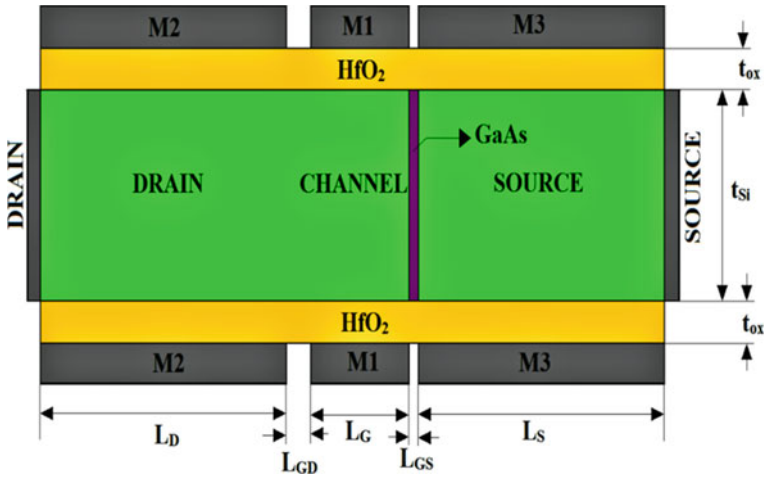

Fig. 1 Sectional cross-view of DLTFET

Table 1 Device structure parameters for simulation

Parameters	Values
Length of drain, (L_D)	50 nm
Work function of gate ($M1$)	4.3 eV
Source and gate space (L_{GS})	2 nm
Length of source (L_S)	50 nm
Work function of source ($M3$)	5.93 eV
Length of channel (L_{CH})	20 nm
Silicon thickness (t_{Si})	10 nm
Oxide material of gate	HfO_2 ($\varepsilon = 21$)
Work function of drain ($M2$)	3.9 eV
Drain and gate space (L_{GD})	5 nm
Thickness of GaAs	2 nm
Physical oxide thickness (t_{ox})	2 nm

the on-state state, the electron can easily pass from the VB of the source to the CB of the drain by the BTBT [8].

DLTFET must be promoted for the BCM over the MOSFET due to the following reasons:

- Shorter channel length (20 nm)
- Lesser leakages
- No channel length modulation effect
- Lower subthreshold swing.

The process which is adopted for evaluation and the comparison of the DLTFET and NMOS-based BCM:

- GaAs DLTFET is simulated with on TCAD Silvaco with the dimensions and material mentioned in [11]. Table 2 shows the results for the DLTFET.
- Look-up tables for I_d, C_{gs}, and $C_{gd,}$ are made for DLTFET with the help of the same software.
- DLTFET device is used in HSPICE with the help of Verilog-A and look-up tables.
- DLTFET-based BCM circuit is simulated on HSPICE.

Table 2 Some output results for the DLTFET

Parameters	Values
I_{ON} (A/um)	10^{-4}
I_{OFF} (A/um)	10^{-19}
I_{ON}/I_{OFF}	10^{15}
Subthreshold swing (SS) (mV/dec)	~10.25

- All three NMOS technologies Berkley Predictive Technology Models (BPTM) are used for the gate dielectric of SiO_2 to simulate the BCM circuit on HSPICE.
- All the results of all the four transistors BCM circuits are compared.

1.2 Basic Current Mirror

The CM sometimes called a current amplifier having current gain equal to 1, which signifies that the output current must be equal to the input current. Figure 2 shows the BCM circuit with 2 MOSFETs M_1 and M_2. CM is one of the critical building blocks and used to improve the performance of many analog integrated circuits (ICs). CM is used as an active load and as a biasing for many circuits like op-amp, analog to digital circuits, digital to analog circuits [16, 17], etc. CM is used as an active load to improve the gain without increasing the supply voltage and chip area [16, 17]. It copies direct current (DC) from one branch to another branch of the circuit, which can help to detect the alteration in the given voltage. Thus, it can be used as a replacement for external resistance in the chips or active load [16]. CM can also be used as a current amplifier by calibrating the width of the transistor/MOSFETs [16, 18]. Hence, it implies that the performance of the ICs depends on the performance of the CM. Ideal CM is required in various circuits such as bio-medical circuits, bio-amplifiers [19, 20], and the current source for the differential amplifier to advance the CMRR [16, 17]. There are billions of transistors to perform many logic functions. Signal processing, such as in audio amplifiers, is also based on the current source. But constant current source does not exist in this world because of energy loss. So, transistors are used to make the constant current source by using the BCM. BCM circuit was made by using the MOSFET and Carbon Nanotube Field Effect Transistor (CNTFET) in the paper [21]. All the parameters for different technologies were compared. It was observed that current error was increasing as the MOSFET channel length scale down from 45 to 22 nm, and the current error was negligible in the case of CNTFET-based BCM, but the input resistance was found high which should be low as possible. Researchers designed many CMs such as Wilson CM, Cascode CM, Advance CM, etc., to improve the accuracy but, however, were complicated and little inaccurate.

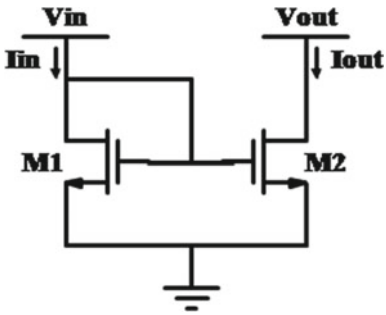

Fig. 2 Basic current mirror circuit using NMOS

The main reason behind this paper is to make a simple, accurate, CM which should have low input and high output impedance.

It is not possible to make BCM through MOSFET in which output current is equal to the input current even when both the transistors are in the saturation region because of the following drain current equation.

$$I_{\mathrm{d}} = \frac{1}{2}\mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L}\left(V_{\mathrm{gs}} - V_{\mathrm{t}}\right)^2 (1 + \lambda V_{\mathrm{ds}}) \tag{1}$$

For an ideal MOSFET, λ is zero. Since λ always greater than zero, due to which drain current varies linearly with V_{ds} even in the saturation mode. If we apply DC input voltage more than the threshold voltage of the transistor $M1$ in the BCM, then the gate voltage for both the transistors will be same which means same drain current should flow through both the transistors (output current should be equal to the input current), but they are not same due channel length modulation part, i.e., $(1 + \lambda V_{\mathrm{ds}})$.

Pseudo Code for the simulation of BCM

```
Call the device                                  // because none of the device is inbuilt in HSPICE.

Voltage source 1 (Vin)

        Positive terminal = input terminal       // DC voltage, pulse or AC supply
        Negative terminal = ground

Voltage source 2 (Vout)

        Positive terminal = output terminal      // DC voltage, pulse or AC supply
        Negative terminal = ground

Transistor 1 (M1)

        Drain = input terminal
        Gate = input terminal
        Source = ground
        Body = ground

Transistor 2 (M2)

        Drain = output terminal
        Gate = input terminal
        Source = ground
        Body = ground
```

Apply transient analysis, DC analysis or AC analysis as per the requirement.

Print “input voltage,” “output voltage,” “input current,” and “output current” w.r.t. “time” for transient analysis or w.r.t. “frequency” for AC analysis.

2 Simulation Results and Discussion

CMs are mainly compared by two parameters. One of the parameters is the current error which states that the difference of the output and the input current should be zero. And AC output impedance is the second parameter which should be high for the extended frequency band. This helps us to see how I_{out} is varying with respect to the applied voltage to the BCM. Some more parameters are also there which describe the BCM like input impedance, transient response, leakage current, etc. Therefore, based on these parameters, the MOSFET-based BCMs are compared with the DLTFET-based BCM.

2.1 Output Characteristics Comparison of the Devices

To compare the output characteristics of the devices, we kept the V_{gs} at 0.9 V while varying the V_{ds} from 0 to 1.2 V to draw the output characteristics. Figure 3 shows the output characteristic of the three NMOS and of the DLTFET. We can observe that for DLTFET, current became constant in the saturation region; whereas for the other devices, the current keeps on increasing in the saturation region. Since current is constant in the saturation region, so DLTFET is a more stable device than the other.

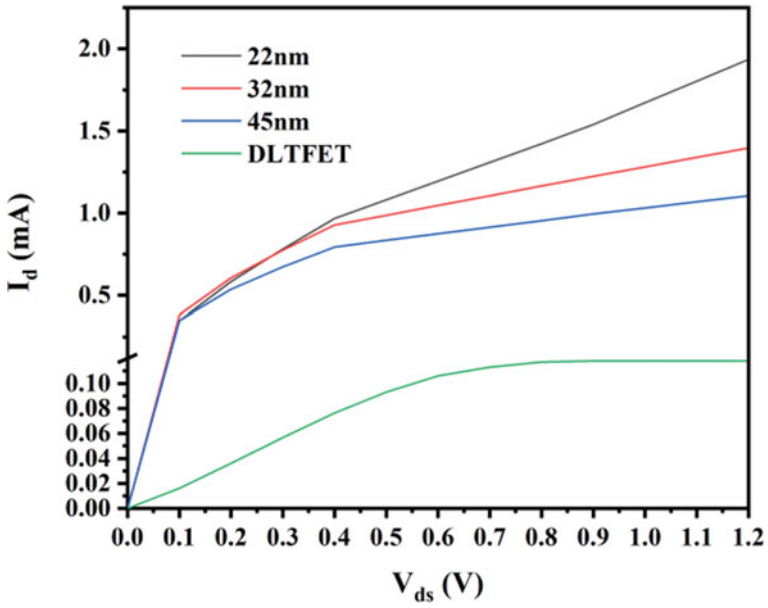

Fig. 3 Output characteristics at $V_{gs} = 0.9$ V of different N-type MOSFETs and DLTFET

2.2 *Variation in the Output Current (I_{out}) w.r.t. The Input Voltage (V_{in})*

The stability of the output current should be maintained in the BCM. Input current changes with the input voltage, which must give rise to a similar change in the output current. The input voltage is altered from 0 to 1.2 V, and the output voltage is remained steady at 1.2 V to see the variation in the input current and the output current. From Fig. 4, we can observe that the output current curve is completely different from the input current curve in the NMOS-based BCM, but they are same in the DLTFET-based BCM. BCM must show the minimum current error ($\Delta I = I_{\text{out}} - I_{\text{in}}$). From Fig. 5, it can be observed that the current error is maximum in 22 nm NMOS BCM and minimum in DLTFET BCM. DLTFET BCM exhibits a typical

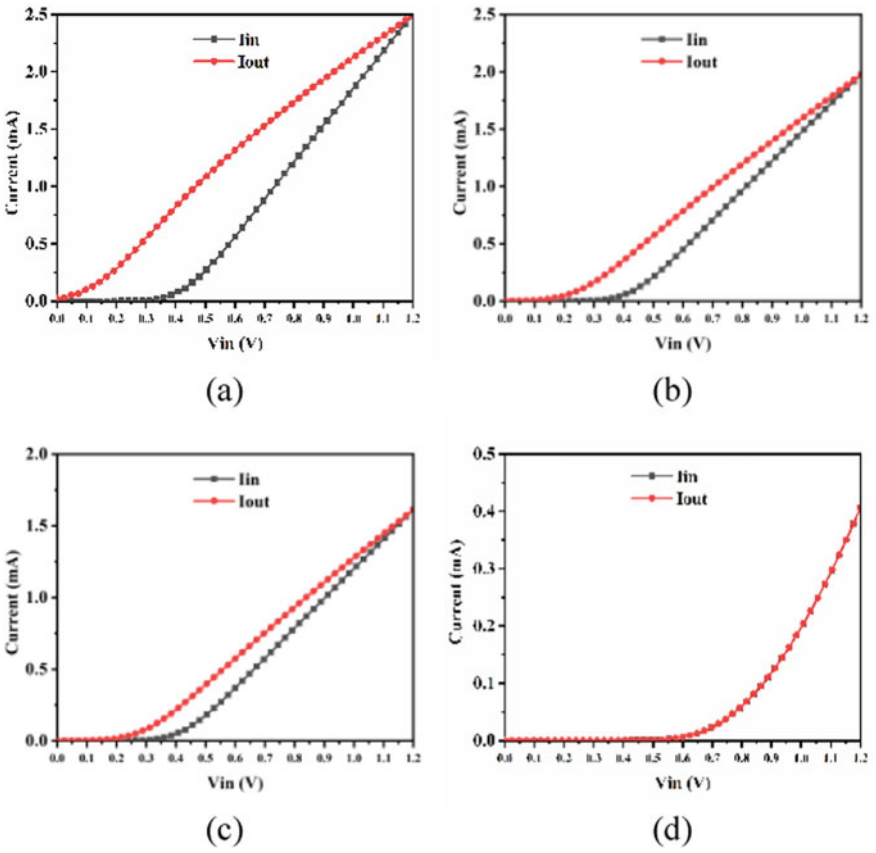

Fig. 4 Input current and output current variation w.r.t. the input voltage with keeping the output voltage constant at 1.2 V for **a** 22 nm NMOS-based BCM, **b** 32 nm NMOS-based BCM, **c** 45 nm NMOS-based BCM, and **d** 20 nm N-type DLTFET-based BCM

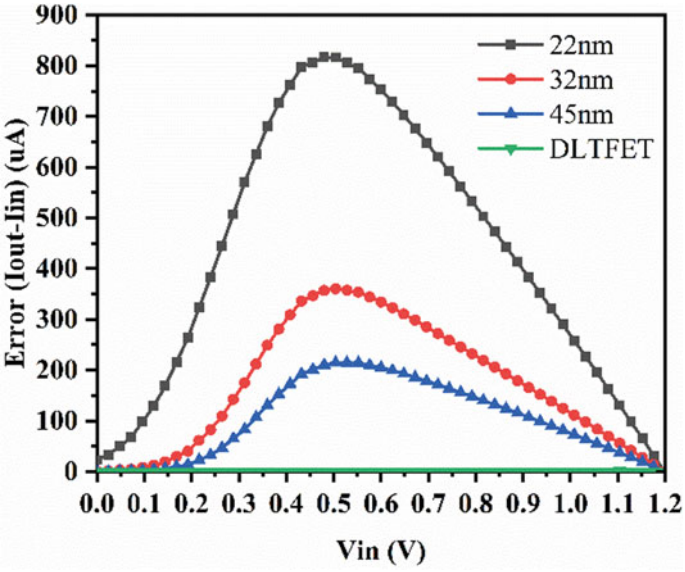

Fig. 5 Error ($\Delta I = I_{\text{out}} - I_{\text{in}}$) is shown in the plot when V_{in} is altered from 0 to 1.2 V. DLTFET is showing the ideal behavior with negligible error

behavior with a negligible current error. It is all because of the less effect of channel length modulation on DLTFET.

2.3 Variation in the Output Current (I_{out}) w.r.t. The Output Voltage (V_{out})

Input current produced in the BCM depends on the applied input voltage only, in the triode region and the saturation region, but the output current depends on the input voltage and the output voltage in the triode region, and it should depend on the input voltage only in the saturation region. For analyzing input voltage fixed at 1.2 V while the output voltage varied from 0 to 1.2 V. From Fig. 6a, it can be observed that the on-current is minimum for the DLTFET. This is the disadvantage of DLTFET. Figure 6b shows that the leakage current DLTFET-based BCM is minimum as compared to the other three transistors-based BCM.

The ratio of the output current to the input current is known as the normalized output current. The necessary condition that should be fulfilled in the BCM is that the normalized output current should be equal to 1 and from Fig. 7 shows that the DLTFET-based BCM reaches that condition first.

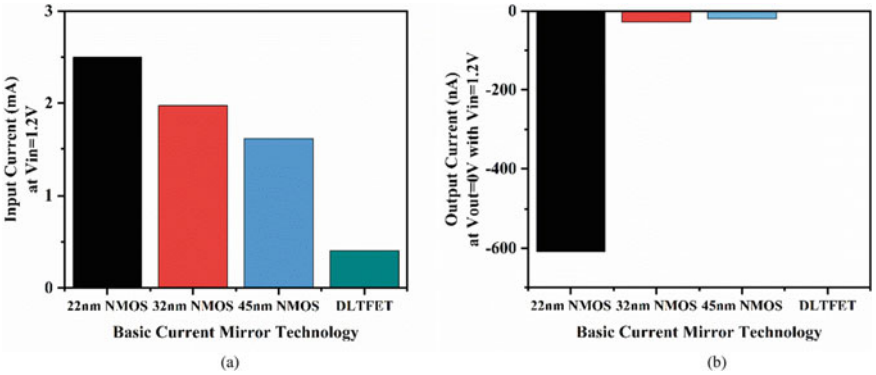

Fig. 6 **a** I_{in} produced at $V_{in} = 1.2$ V. **b** Leakage current obtained at $V_{in} = 1.2$ V and $V_{out} = 0$ V

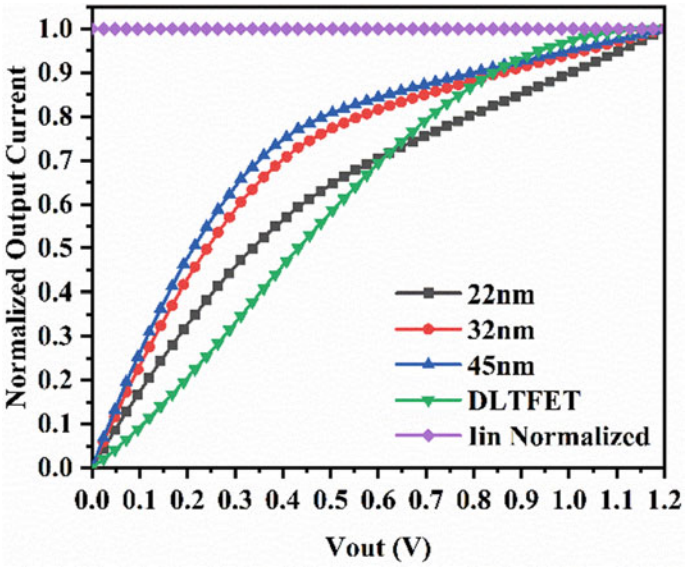

Fig. 7 Normalized I_{out} is plotted with V_{out} varying from 0 to 1.2 V

2.4 Transient Response to the Square Wave Input

The square wave is practiced at the output voltage (initial voltage = 0 V, final voltage = 1.2 V, delay time = 100 ps, rise time = 100 ps and fall time = 100 ps, pulse width = 2 ns, and time period = 4 ns). Input voltage is remained steady at 1.2 V. Current transient response for the BCM based on the four transistors is shown in Fig. 8. We can observe that delay time is highest in DLTFET-based BCM among the four, and

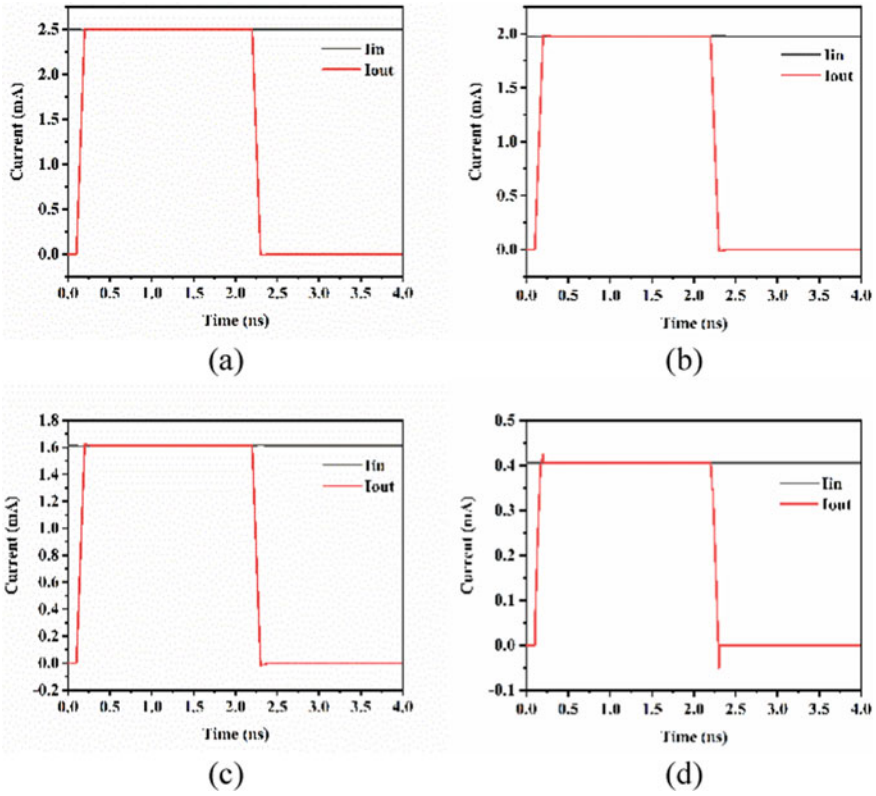

Fig. 8 Transient response of I_{in} and I_{out} of the BCM using different technologies **a** 22 nm NMOS, **b** 32 nm NMOS, **c** 45 nm NMOS, **d** DLTFET

the consumption of power is lowest, due to which its PDP is less than the PDP of 22 nm NMOS-based BCM (Table 3).

2.5 Input Impedance (Z_{in}) Alter with Frequency

The input impedance of a BCM should be low and be stable for a broad frequency band. We can observe from Fig. 8a that the input impedance of the DLTFET-based BCM is minimum among the four BCMs. It is unable to figure out from the Fig. 9a that input impedance of the DLTFET-based BCM is stable up to which frequency, therefore, input impedance versus frequency graph is plotted in the Fig. 9b for the same.

Table 3 Compared parameters for current transient response of I_{in} and I_{out} of BCM technologies at $V_{in} = 1.2$ V and pulse V_{out}

Parameters	Unit	22 nm NMOS	32 nm NMOS	45 nm NMOS	DLTFET n-type
Output current	mA	2.498	1.976	1.613	0.406
Rise time	ps	77.43	66.91	63.84	62.95
Fall time	ps	77.66	68.22	64.91	71.77
Negative overshoot	μA	12.5	13.69	14.9	51.48
Positive overshoot	uA	11	11.7	12	24.84
Delay 50% (low to high)	ps	11	12	11	80
Delay 50% (high to low)	ps	20	2	7	80
Total delay	ps	31	14	18	160
Power	mW	3.835	3.04	2.48	0.62
Power delay product	fJ	118.88	42.56	44.64	99.2

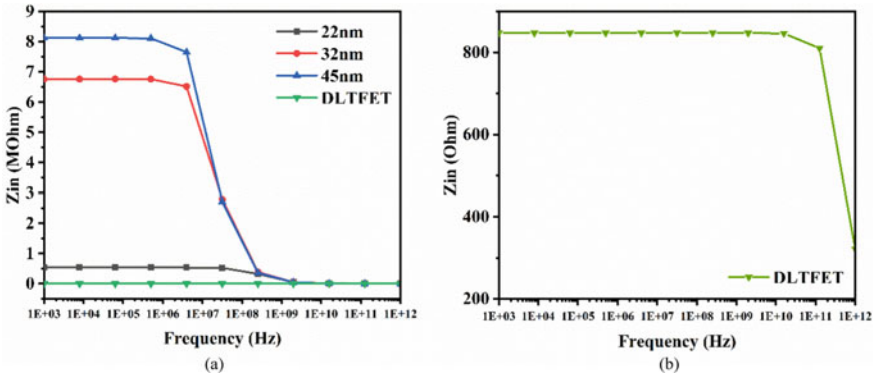

Fig. 9 **a** Z_{in} versus frequency plot of the BCM for different technologies. **b** Z_{in} versus frequency plot of the BCM for DLTFET

2.6 Output Impedance (Z_{out}) Alter with Frequency

The output impedance of the BCM should be high for the extended frequency range. We can observe from Fig. 10 that DLTFET-based BCM is at the top among the four transistors-based BCM for the frequency range up to 10 GHz.

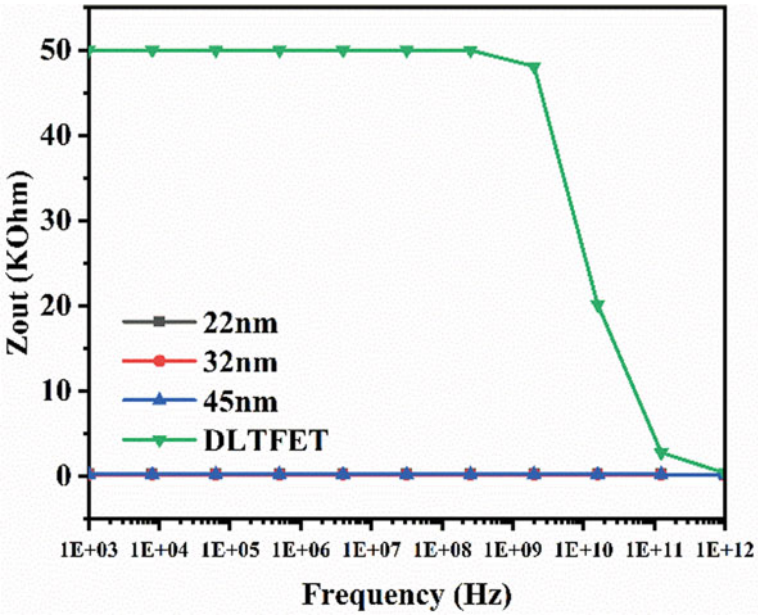

Fig. 10 Z_{out} versus frequency plot of the BCM for different technologies

2.7 AC Analysis

V_{in} and V_{out} are kept at 1.2 V DC for biasing, and to keep them in the saturation region 1 mV, 1 kHz AC sine wave signal is superimposed over the DC supply. To study the response of I_{in} and I_{out} and gain w.r.t. the frequency for all the BCMs. Frequency is swept from 1 MHz to 1 PHz. We can observe from Fig. 11a that response of I_{in} is nearly the same for all the four transistors-based BCMs, and from Fig. 11b, the response of I_{out} for DLTFET-based BCM becomes constant. Figure 11c shows that the $-$ 3 dB gain is zero for all the transistors-based BCMs for the same frequency range that is up to 100 GHz. Due to the presence of parasitic capacitances and other parameters in NMOS and DLTFET, they show different current gain curve w.r.t. the frequency.

3 Conclusion

From the above results and discussion, 20 nm DLTFET can be used as a better substitute of NMOS technologies since for analog applications beyond 45 nm; it has low V_{th}, high Z_{out}, lower Z_{in}, symmetrical response ($\Delta I = 0$), stable gain with frequency, and negligible leakage. 20 nm DLTFET is supported by this paper for BCM because its performance is better than the other three MOSFET transistors by

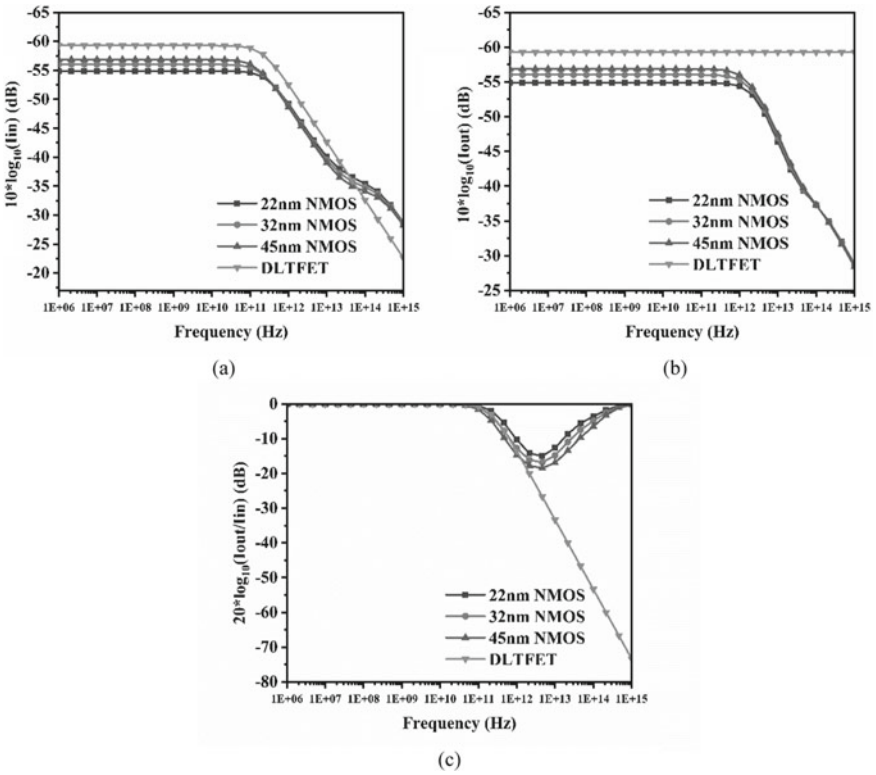

Fig. 11 BCM **a** I_{in} **b** I_{out} **c** − 3 dB gain versus frequency response for different technologies

considering the comparative parameters. The same kind of evaluation can be done for the other analog circuits like Cascaded CM, operational amplifier, differential amplifier, etc., by using the 20 nm DLTFET.

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Meta-heuristic Algorithm for Energy-Efficient Task Scheduling in Fog Computing

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1 Introduction

Fog computing is an evolving paradigm which supports QoS as provided to the consumers along with cloud computing. Fog nodes are not of their whole computing capabilities, and so these are used along with cloud computing. It follows pay-as-per-usage model. The usage of cloud computing is leading to high latency and high-bandwidth [1–3].

Due the growth of the data centers, there is a rise in energy consumption, and the emission of CO_2 in the data centers is growing exponentially. Figure 1 shows the electricity usage of data centers from 2010 to 2030. The growth in the data centers grows the emission of CO_2. Green DCs use the energy-efficient technologies including low power servers, free air cooling, and smart grid. Lately, fog computing comes to extend the capabilities of cloud computing. IoT is another emerging concept which has integrated with fog computing [2, 4]. It serves in the field of smart health care, smart city, smart manufacturing, and smart traffic control. IoT collects data using sensors and sends them to the fog layer. Later if the data is needed to store, it will send to the cloud data center for long-term storage and analytics [5, 6]. Task scheduling in fog server is complex and challenging problem, as inefficient task scheduling can result in higher energy consumption. This paper has suggested Harris Hawks

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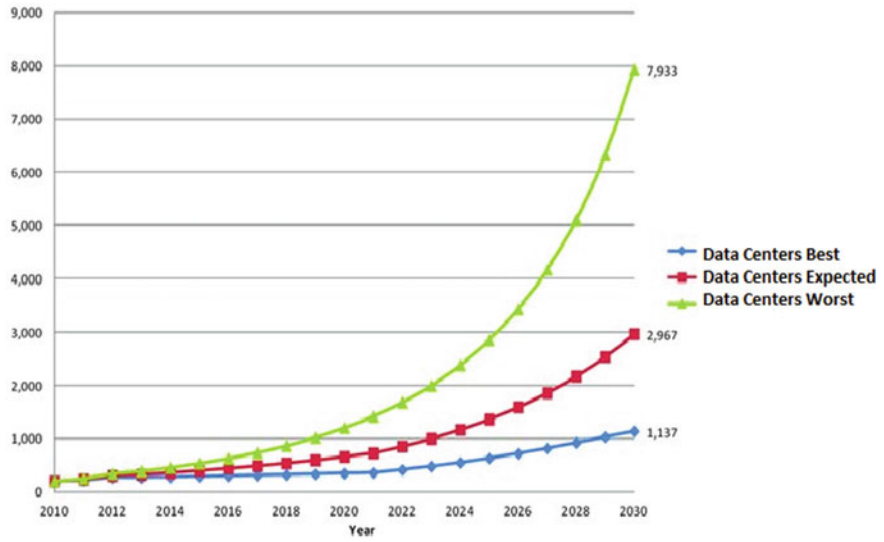


Fig. 1 Electricity usage in TWh of data centers 2010–2030 [1]

optimization algorithm for scheduling the tasks in fog servers. The paper is organized as follows. Section 2 presents the related works related to task scheduling in VMs, Sect. 3 depicts the task scheduling problem in the fog servers, Sect. 4 describes the standard Harris Hawks meta-heuristic optimization algorithm. Section 5 presents the proposed algorithm for task scheduling in fog servers, Sect. 6 explains the algorithm by an illustration, Sect. 7 does the result analysis, and finally, Sect. 8 concludes the paper.

2 Related Works

In recent days, the task scheduling has attracted the attention of many researchers because efficient task scheduling algorithms have direct impact on energy saving and resource utilization. Wu et al. [7] proposed an energy-efficient technique for saving the energy consumption in IoT and fog computing. Meta-heuristic algorithms play an important role in solving the task scheduling problems in fog servers [8–10]. Goswami et al. [11] studied the performance of the system which depends on the queue length to scale the VMs along with improves the QoS parameters of the system. Patra [12] derived meta-heuristics for energy-efficient task consolidation algorithms in cloud environment. Patra et al. in [13] designed algorithms for profit maximization by saving energy and spot allocation quality guaranteed services in cloud environment.

3 Task Scheduling Problem in Fog Server

Fog servers are present in between the cloud layer and the end-user device layer, as shown in Fig. 2. It is mentioned as computing platform with large number of distributed nodes, which are highly virtualized and scalable in nature. As shown in the Fig. 2, the fog layer contains multiple fog nodes. The hypervisor or virtual machine monitor (VMM) programs allow creating and managing new virtual machines (VMs). There are n number of VMs (VM_1, VM_2, … VM_n) that can run on a fog node. All VMs share the resources of the fog server, such as memory, disk, and CPU cores. These resources can effectively scale up and scale down as per the SLA and saves the infrastructure resources. Task scheduling is a problem in which it has to schedule m number of heterogeneous tasks to be scheduled on n heterogeneous VMs.

The tasks are independent in nature and may be submitted by different service users. Each VM has its own guest OS which can run various application programs on the same physical fog node. It is depicted in Fig. 3.

The task scheduling problem can be defined as follows. There is a set of m tasks $\{t_1, t_2, t_3, \ldots t_m\}$. A task t_i is assigned a workload w_i. Each w_i can be represented in terms of Million Instructions (MI). Since each w_i are different in size, we can say the tasks are heterogeneous. There is a set of n VMs in the fog system $\{v_1, v_2, v_3, \ldots v_n\}$.

Each VM_j has a processing speed s_j in terms of MIPS. $F(t_i) = VM_j$, means a task t_i is assigned to VM_j at an instance. The ETC matrix ETC(i,j) shows the execution time of a task i, t_i in VM j VM_j.

$$\mathrm{ETC}(i, j) = \frac{w_i}{s_j} \tag{1}$$

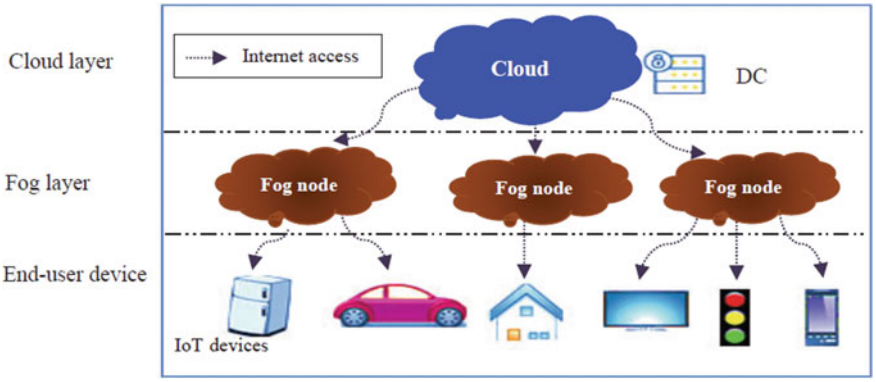


Fig. 2 Architecture of fog layer [14]

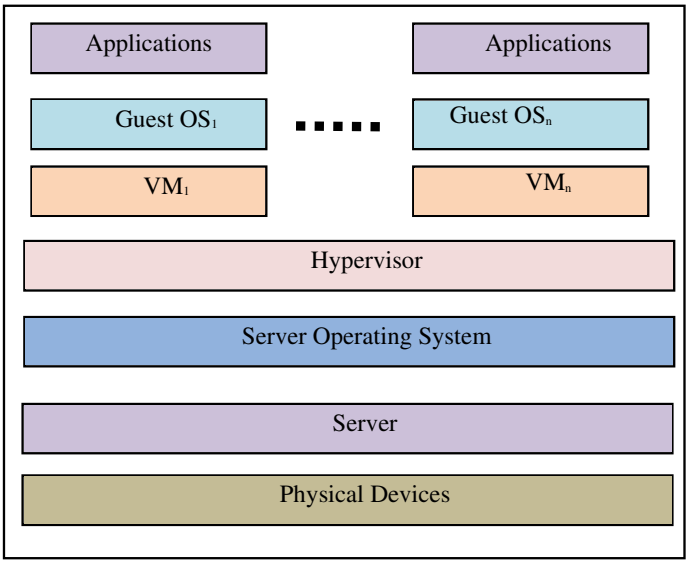


Fig. 3 Fog server virtualization [15]

4 Harris Hawks Optimization Algorithm

Haidari et al. [16] have proposed a nature-inspired algorithm that simulates the nature of Harris Hawks called Harris Hawks meta-heuristic optimization algorithm. The important parameter of Harris Hawks is to catch a prey related to surprise pounce. It is also called Seven-Kills scheme. In this scheme, many hawks are demanding to agreeably attack from many directions and concurrently converge on a detected escaping rabbit exterior the cover. This algorithm is operated on two stages—exploration phase and exploitation phase. In HHO, the Harri's hawks perch haphazardly on few locations and stay to notice a prey based on two important strategies. If it considers an equivalent probability q for every awaiting strategy, they perch depending on the placements of former members of family and the rabbit. It has derived in Eq. (2) on the circumstance of q which is less than 0.5 else the perch on arbitrary tall trees or condition for $q >= 0.5$.

$$f(t+1) = \begin{cases} f_{\text{random}}(t) - \text{rand}_1 | f_{\text{random}}(t) - 2\text{rand}_2 f(t) | & q \geq 0.5 \\ f_{\text{rabbit}}(t) - f_{\text{mean}}(t) - \text{rand}_3(\text{LB} + \text{rand}_4(\text{UB} - \text{LB})) & q < 0.5 \end{cases} \tag{2}$$

In this case, both $F(t)$ and $F(t+1)$ are two point vectors of hawks for the existing and the subsequently iterations. $F_{\text{random}}(t)$ is the random hawk elected from the populations. $F_{\text{rabbit}}(t)$ is where the rabbit is placed. q, rand_1, rand_2, rand_3, and rand_4 are random numbers. LB as well as UB are the lower, upper bounds for generating

random locations within the Hawks' home. $F_{\text{mean}}(t)$ is the mean location of hawks for the current population. The energy of a prey minimizes noticeably on the avoidance behavior. The energy of a prey is derived as the following Eq. (3).

$$E = 2E_0\left(1 - \frac{t}{\text{Max} - \text{iter}}\right) \tag{3}$$

Here E denotes the prey's escaping energy, T is the max no. of iterations, and E_0 is the initialized energy. E_0 changes in between $(-1, 1)$ in each iteration. The hawks encircle the rabbit softly and suddenly pounce the rabbit. It can be modeled as

$$f(t+1) = \Delta f(t) - E|\text{RJ} * f_{\text{rabbit}}(t) - f(t)| \tag{4}$$

where $\Delta f(t)$ is the rabbit positions minus the hawk's position. RJ refers to the strength of the random jump of rabbit and through the escaping process and is absorbed by a random number rand $\in [0.1]$. $\Delta f(t)$ and RJ are computed as:

$$\Delta f(t) = f_{\text{rabbit}}(t) - f(t) \tag{5}$$

$$\text{RJ} = 2(1 - \text{rand}) \tag{6}$$

The hard besiege is derived as,

$$f(t+1) = f_{\text{rabbit}}(t) - E|\Delta f(t)| \tag{7}$$

The next move of the Hawks is formulated with the depending on what the previous move it has taken:

$$n = f_{\text{rabbit}}(t) - E|\text{RJ}\, f_{\text{rabbit}}(t) - f(t)| \tag{8}$$

If the previous dive is not good, they will dive based on the Levy flight pattern s using the rule:

$$Z = n + s * \text{Levy\_Flight(dim)} \tag{9}$$

$$f(t+1) = \begin{cases} n & \text{if } f(n) < f(f(t)) \\ z & \text{if } f(z) < f(f(t)) \end{cases} \tag{10}$$

The benefit of using evolutionary meta-heuristics algorithm is it provides the global optimization. Its flexibility, adoption to the different and complex optimization problems without requiring any special feature to its objective functions as well the constraints like continuity, differentiability, or convexity.

5 Proposed Algorithm for Task Scheduling in Fog Server

In this section, it has described the proposed algorithm which has included with five important steps. These five steps are population, evaluation, fitness function, normalization with scaling, mutation, and best search.

A. **Population**
In population phase, random population of h hawks is initialized. Let we have a task scheduling problem having $m = 7$ and $n = 3$, a candidate solution can be considered as shown in Fig. 4. The Fig. 4 shows that VM_1 is assigned to task t_2 and also t_4.

B. **Evaluation**
Energy consumption is evaluated in this phase for the initial population. The fitness function is defined here. Every VM in the fog node is either in active state or in idle state. Energy consumption of a VM is the consumed energy in active as well as idle state. Energy consumption of VMs dissipate about 60% as much as energy when idle as when fully loaded [4].

C. **Fitness Function**
Makespan along with energy consumption is the two most important functions which influences the other factors such as cost, CO_2 rate as well as time of flow. Thus, we can write a bi-objective function to employ the candidate solution.

$$\text{Fitness} = \xi * \text{total\_energy} + (1 - \xi) * \text{MK} \tag{11}$$

D. **Normalization and Scaling phase**
The newly generated hawk $f(t + 1)$ of HHO contains continuous values. The continuous values of hawk must be translated to discrete values (VM numbers). The first step is the hawk vector that is to be normalized in the interval [0,1]

$$\text{Normalized}_i(t + 1) = \frac{f_i(t + 1) - \min}{\max - \min} \tag{12}$$

where min and max are the two extremes of the hawk vector. $F_i(t + 1)$ represents each hawk value where $i = 1,2, \ldots m$. $\text{normalized}_i(t + 1)$ refers to the ith value in the normalized hawk vector. After that using the following equation, the normalized hawk will be scaled in [1 … n] as represented in Fig. 5.

$$\text{scaled}_i(t + 1) = \text{normalized}_i(t + 1) * (n - 1) + 1 \tag{13}$$

where $\text{scaled}_i(t + 1)$ is the ith value in the scaled hawk vector. N is the number of VMs.

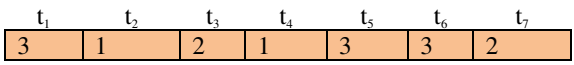


Fig. 4 Vector representation Harris Hawks

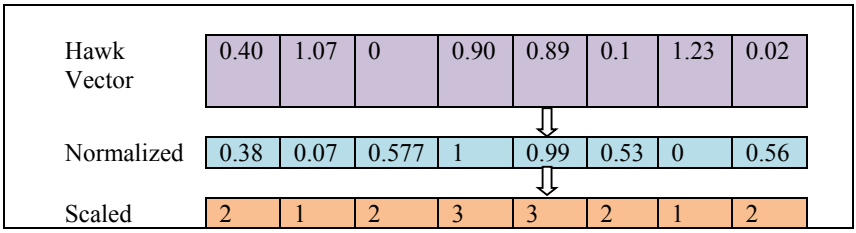


Fig. 5 Normalization and scaling from continuous to discrete

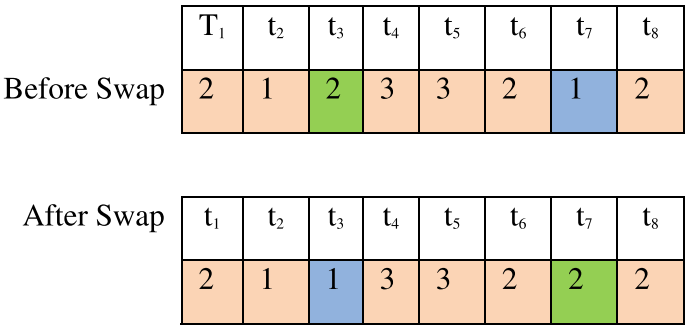


Fig. 6 Mutation operation

E. **Mutation**
The process of mutation is shown in Fig. 6. Here, the locations 3 and 7 are randomly chosen and swapped to get the new candidate solution. After mutation, the task t_7 has to be run in VM2, and t_3 is run on VM_1.

F. **Best Search Strategy**
The best search strategy is utilized to prop the best solution in every iteration. The algorithm for the proposed **Harris Hawks meta-heuristic optimization algorithm** is shown in Algorithm 1.

Algorithm 1: Proposed algorithm HHMHOA

Input : The input will be the population_size=h, maximum no. of iterations Max_Iter, no. of VMs n, no. of tasks m, VM's s_i and w_i of tasks.

```
1.  Initialize the population of h random hawks fi (i=1,2,3,…h)
2.  Calculate the fitness of each hawk using Eq. (19)
3.  Find the best position with minimum fitness f_rabbit
4.  iter=1
5.  While (iter <= Max_Iter)
6.    Update E using Eq (4)
7.    If (|E| >1)
8.        Update f(iter+1) using Eq (2)
9.    Else if (|E| < 1)
10.           If (chance, p>= 0.5 && |E| >=0.5)
11.               Update f(iter+1) using soft besiege
12.           Else if (chance, p>= 0.5 && |E| <0.5)
13.               Update f(iter+1) using difficult surround
14.           Else if (chance, p<0.5 && |E| >=0.5)
15.               Update f(iter+1) using easy surround with Progressive Rapid
                  diving (PRD)
16.       Else if (chance, p<0.5 && |E| >=0.5)
17.               Update f(iter+1) using easy surround with Progressive Rapid
                  diving (PRD)
18.       Else if (chance, p<0.5 && |E| <0.5)
19.                Update f(iter+1) using easy surround with Progressive Rapid
                  diving (PRD)
20.       Normalization_Scaling(f(iter+1))
21.       Swap(f(iter+1))
22.       If fitness f(iter+1) < fitness (f_rabbit )
23.           f_rabbit=f(iter+1)
24.       Apply Best search strategy to f_rabbit
25.     iter++
26. End while
27. End Algo
```

Output : rabbit position f_{rabbit}

6 An Illustration

Let the number of tasks $m = 8$ and number of VMs $n = 3$. The workload for eight tasks are taken as <3000, 5600, 4800, 7600, 9800, 10,000, 2000, 8100> . Table 1 is the ETC matrix, and the allocation matrix can be represented as <(0,0,1), (1,0,0), (0,1,0), (1,0,0),(0,0,1)(0,0,1)(0,1,0), (0,1,0)> . The execution time of the VMs is <13.22, 7.45, 9.15>, and for the three VMs, the energy consumption <β_j, α_j, Energy (VM_j)> is <(0.01, 0.06,131), (0.04,0.024,873), (0.06,0.036,1806)> . Figure 7 illustrates a Gantt chart where the candidate solution of the problem is 3-1-2-1-3-3-2-2.

Table 1 ETC matrix

8×3	VM_1	VM_2	VM_3
t_1	3.2	1.5	1.3
t_2	5.5	2.9	2.25
t_3	4.8	2.42	1.93
t_4	7.7	3.9	3.03
t_5	9.86	4.7	3.93
t_6	10	5.1	4.2
t_7	2	1.3	0.87
t_8	8.2	4.02	3.25

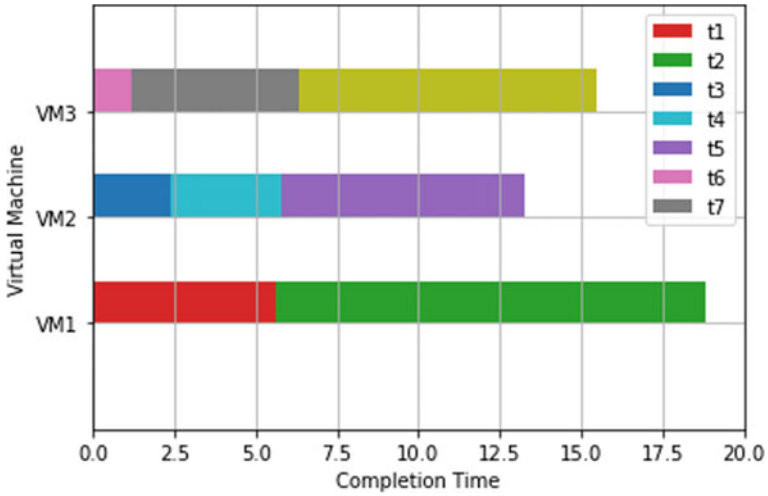


Fig. 7 Candidate solution

7 Results Analysis

The dataset is randomly generated. The data center is considered with 500 to 1500 tasks having 15 VMs in each case. Figures 8 and 9 explain the energy consumption versus the no. of tasks for the existing and the proposed algorithm. The graph shows that HHMH algorithm is outperforming as compared to the PCO and TLBO algorithms in terms of energy consumption.

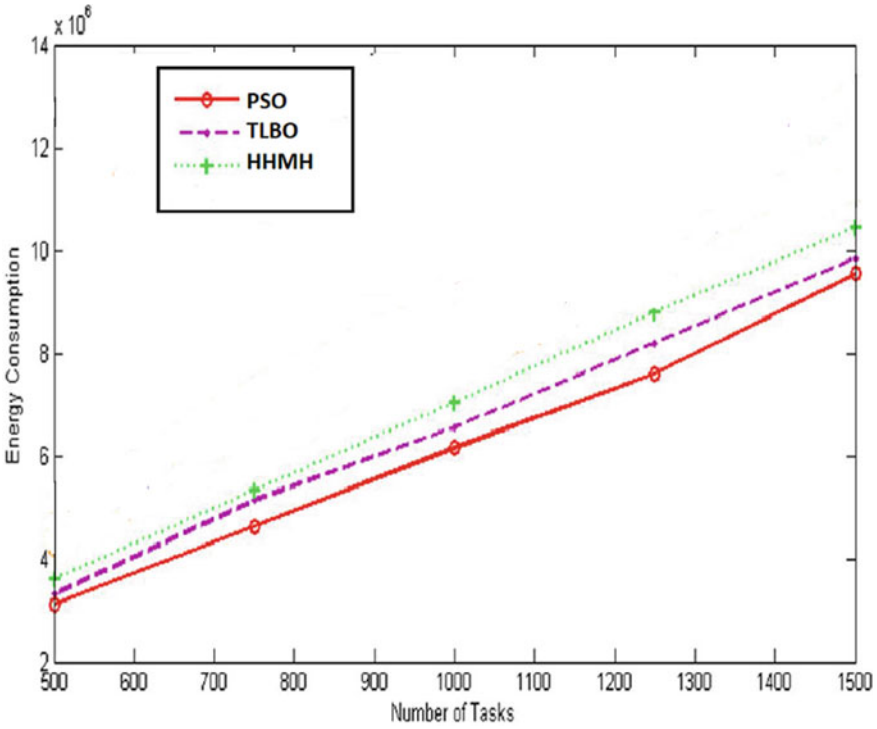
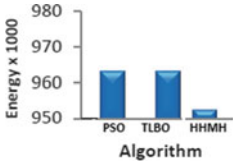


Fig. 8 Number of tasks versus energy consumption

Fig. 9 Algorithm versus energy on 15 VM



8 Conclusion

In this paper, a meta-heuristic algorithm Harris Hawks on the task consolidation problem on fog environment is implemented. The HHO algorithm is for continues data. Using standardization and normalization, the continuous problem is converted to discrete problem. Simulation study has done to compare the performance of the proposed algorithm HHMHOA with particle swam optimization (PSO) and teaching learning-based optimization (TLBO) techniques. The results show that the proposed algorithm outperforms.

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Implementation and Performance Evaluation of Various Reversible Vedic Multiplier Architectures for Reversible Digital Filters

U. Swathi and U. Smitha

1 Introduction

The field of microelectronics has been able to cater to the needs of this generation for more compact and non-expensive devices. There are continuous challenges that are to be addressed due to a number of key limitations associated with this field [1]. The limitations could be physical, technological, material-related, device-related or other system related limitations. Scaling of MOS (metal-oxide semiconductor) devices to nanometer range leads to a number of issues like increased leakage current that impairs the behavior and degrades the performance of the device which in turn paves the way for the exploitation of alternative technologies [1].

The semiconductor industry has been able to scale down the dimensions of the fundamental computing component, i.e. a transistor, to a great extent despite the continued challenges [1]. But it is a fact that the process of scaling cannot continue to a further level as there are a number of issues associated with scaling in the case of nanometer process technology. The main is the leakage current across the oxide layer due to the process of quantum mechanical tunneling of electrons from gate oxide to the transistor channel. As transistor shrinks, more of such quantum effects or short channels effects would come into picture affecting its performance and limiting the scaling process which brings out the need for an efficient alternative technology that can overcome these drawbacks [1].

Landauer [2] in his work in 1961, showed that for every irreversible bit operation there is an energy loss of $kT * \ln 2$ Joules (where $k = 1.3806505 \times 10^{-23}$ J/K represents Boltzmann's constant, T represents temperature in Kelvin). Although this appears to be a small amount of energy, if we think about the entire processor where millions of transistors are operating then the dissipated energy can be significant [2]. Moore made the observation that, in the case of a dense IC, the transistor count

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will double approximately every two years. This will increase the heat dissipation exponentially with time. But if a system is capable of returning to its initial state from its final state, there would be no energy dissipated and theoretically the system would act as a lossless system [3]. Bennett [4] in his work in 1973, proved that if a circuit is made reversible then the energy dissipation of kT * ln2 can be avoided since there is no information loss.

Dissipation of heat for every bit of information loss is a drawback of conventional combinational circuits. The second law of thermodynamics also states that every irreversible process leads to energy loss [5, 6]. Reversible logic is considered to be a great alternative to traditional digital logic circuits in this regard with wide range of applications in future emerging technologies like quantum computing, optical computing, ultra-low power VLSI circuits, QCA, nanotechnology etc. Reversible design eliminates the loss of information by allowing the system to run backwardly, thereby helping to recover the inputs from outputs. It also has a unique one-to-one mapping between the input lines and the output lines and is indispensable for quantum computing. [7].

Multipliers are key elements of any processing or computing system. The performance of digital signal processor or the microcontroller is more or less evaluated taking into account the multiplication time [8]. They are used for a number of digital signal processing applications including digital filtering, FFT, convolution, wavelet compression, ALU and also several image processing applications. Since the performance of the system predominantly depends on the performance of the multiplier unit, it is very important to utilize faster multiplier architectures in order to increase the system performance. Vedic multiplier is one such multiplier architecture which performs exceptionally well as compared to conventional multipliers, with decreased delay. Thus, it's important to combine the low-power advantage of reversible design and the incredible high speed of Vedic multipliers units to increase the overall system performance.

There are several efficient techniques for performing the multiplication operation that are proposed in the past which are available in the literature. Many of them have made use of reversible logic [9–21]. In this paper we have implemented six of those architectures of the Vedic multiplier using reversible logic that are quite efficient at performing the multiplication operation compared to the traditional designs. A number of computational units have been used like adders, fan-out generators which are proved to be efficient [22–25]. We have implemented 2 * 2, 4 * 4, 8 * 8 and 16 * 16 multiplier units using each of the six architectures and the performance of the same has been compared. The performance of the implemented design is tabulated in terms of the performance parameters like quantum cost, gate count, garbage output, implementation cost, as well as the area and delay factors.

This paper has been organized as follows: Sect. 2 details the fundamentals of reversible logic design. Section 3 sheds light on the Urdhva Tiryagbhyam Sutra. Section 4 shows with the implementation of the various architectures of the Vedic multiplier. Section 5 deals with the results and the analysis followed by the conclusion in Sect. 6.

2 Fundamentals of Reversible Logic Design

A reversible logic gate is the one in which there are n inputs and n output lines with one-to-one mapping between each other. This helps to retrieve the inputs from the outputs as each input produces unique output. Since there is no information loss in reversible circuits, it is said to have theoretically zero power dissipation [26].

It is important to keep several facts in mind while we design our circuit using reversible logic gates. They are:

- Number of inputs has to be equal to the number of outputs
- For every input there has to be a unique output
- Fan-out should be avoided
- Loops or feedbacks should be avoided
- Cost metrics are to be kept minimum.

2.1 Performance Parameters/Cost Metrics

Important parameters which are to be considered during reversible logic design are the following [27, 28]:

Constant/Auxiliary input (CI): In order to implement the required logic, we will have to set the inputs of reversible gates used in our design to either 0 or 1. These are termed as constant inputs.

Garbage output (GO): In addition to the required outputs, reversible gate also generates outputs which are not utilized or are not necessary in the design. These are termed as garbage outputs.

Number of gates/gate count (NG): It refers to the total number of gates that are used to implement the design.

Quantum cost (QC): The number of 1×1 or 2×2 gates called primitive gates used to implement the logic is called QC.

Total reversible logic implementation cost (TRLIC): It refers to the total cost of the circuit which is the sum of total number of gates, CI, QC and GO required to implement the design. Mathematically, it can be written as:

$$\text{TRLIC} = \sum \text{NG} + \sum \text{CI} + \sum \text{QC} + \sum \text{GO} \tag{1}$$

A number of reversible logic gates have been proposed earlier, and a few of those that are used in our implementation are given below.

2.2 Basic Reversible Gates

Feynman gate [FG]/CNOT gate: It is a 2 × 2 reversible gate with a quantum cost of 1. The logic diagram and the quantum representation of Feynman gate are shown in Fig. 1

Peres gate [PG]: It is a 3 × 3 gate and it has a quantum cost of 4. The logic diagram and the quantum representation of Peres gate are shown are Fig. 2.

Toffoli gate (TG): It is a 3 × 3 gate with QC = 5. The logic diagram and the quantum representation of the same are shown in Fig. 3.

HNG gate: It is a 4 × 4 gate with QC = 6. The logic diagram and the quantum representation of the same are shown in Fig. 4.

BVF gate: It is a 4 × 4 gate with QC = 2. The logic diagram and the quantum representation for the same are shown in Fig. 5.

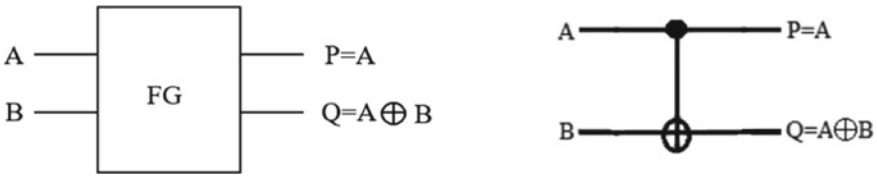


Fig. 1 Logic diagram and quantum representation of Feynman gate

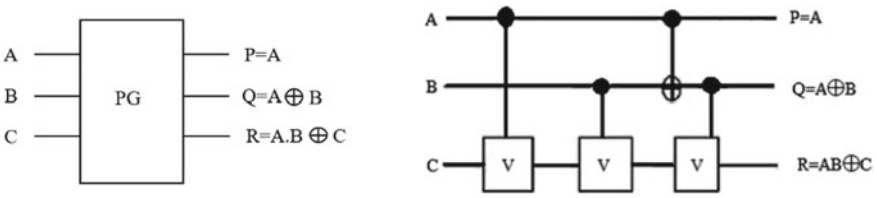


Fig. 2 Logic diagram and quantum representation of Peres gate

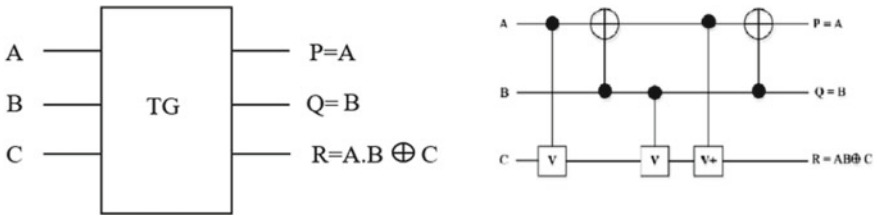


Fig. 3 Logic diagram and quantum representation of Toffoli gate

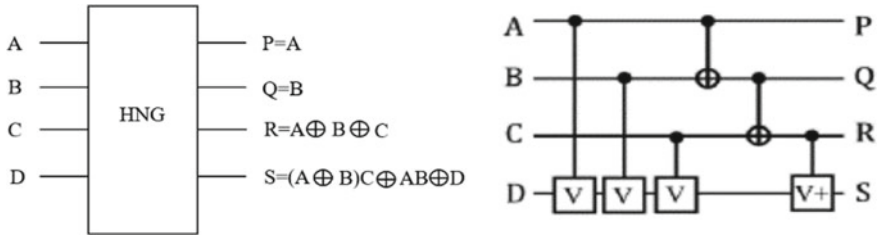


Fig. 4 Logic diagram and quantum representation of HNG gate

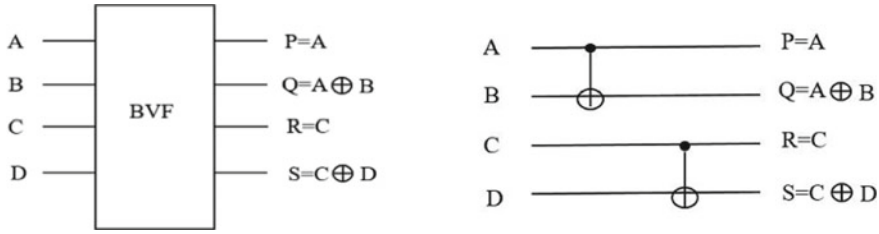


Fig. 5 Logic diagram and quantum representation of BVF gate

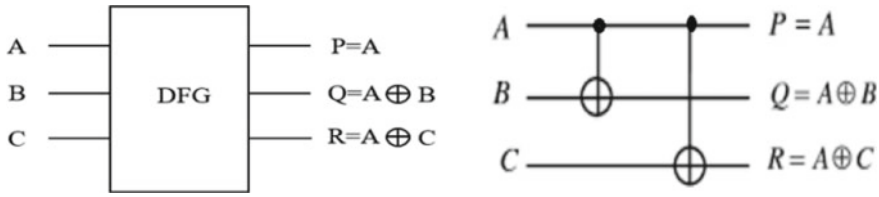


Fig. 6 Logic diagram and quantum representation of DFG gate

DFG gate: It is a 3 × 3 gate with QC = 2. The logic diagram and the quantum representation for the same are shown in Fig. 6.

BVPPG gate: BVPPG gate is a 5 * 5 reversible gate with QC = 10. The logic diagram and the quantum representation of the same are shown in Fig. 7.

BME gate: BME is a 4 * 4 reversible gate with a quantum cost of 5. The logic diagram for the same is shown in Fig. 8.

3 Urdhva Tiryagbhyam Sutra

High-performance real-time DSP applications demand highly efficient multiplier architectures as it is one of the most important arithmetic operations [22]. There are

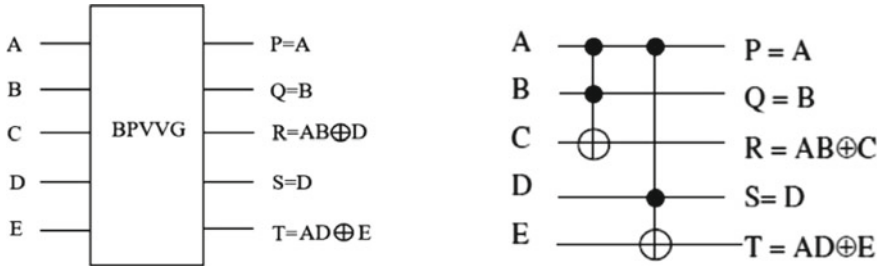
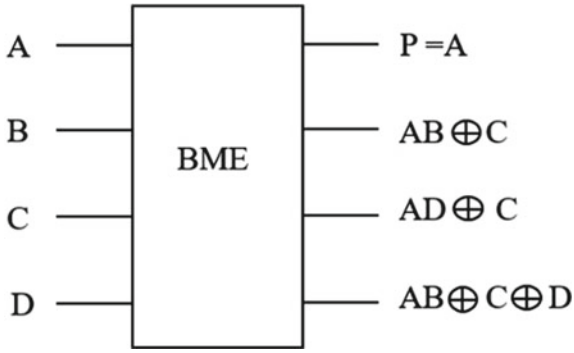


Fig. 7 Logic diagram and quantum representation of BVPPG gate

Fig. 8 Logic diagram of BME gate



a number of multiplier architectures which have been evolved to optimize area, power or delay. Vedic multipliers too emerged to meet these demands. Vedic multiplier can be designed based on a number of ancient Vedic sutras. There are 16 sutras which has got applications in science and engineering stream and can be used for performing multiplication operation [22]. These are known for its high speed and reduced delay. Here, we have used one of the 16 sutras which is considered to be highly efficient in terms of the operating speed, i.e., Urdhva Tiryagbhyam Sutra [22].

Urdhva Tiryagbhyam Sutra (UT sutra) can be applied for performing multiplication of two numbers in either binary or hexadecimal or decimal number system. It is also termed as vertically and crosswise method [9]. Unlike conventional multiplication schemes where we generate partial products and then perform addition to get the final product, here we can calculate the product concurrently. This parallelism feature makes UT multiplier to be one of the fastest multipliers. In other multiplier architectures as the number of bits of the multiplicand/multiplier increases the computation time too increases but here it is not so. Also the computation time is not dependent on the clock frequency [9].

It has got the following advantages:

1. Since the computation time is non-correlated to the clock frequency, we can set the frequency to a low value, thus lowering the energy dissipation.

2. As the bit width of the input increases, the delay and area increase very slowly compared to other conventional architectures of multiplier [9].

3.1 *Urdhva Tiryagbhyam Sutra: Computation for 2/4-bit Numbers*

Consider x and y to be the two bit numbers where $x = x_1x_0$, $y = y_1y_0$ which are multiplicand and multiplier, respectively. Let $p = p_3p_2p_1p_0$ be the product. The product is computed as follows.

$p_0 = x_0y_0$
$p_1 = x_1y_1 + x_0y_1$
$p_2 = x_1y_1 + c_1$ (carry of p_1)
$p_3 = c_2$ (carry of p_2)

Thus, UT Sutra for 2-bit numbers can be shown as in Fig. 9.

Suppose the multiplicand and multiplier are 4 bits wide, i.e., $x = x_3x_2x_1x_0$, $y = y_3y_2y_1y_0$ which are multiplicand and multiplier, respectively. Let $p = p_7p_6p_5p_4p_3p_2p_1p_0$ be the product.

The product is computed as follows which is also shown in Fig. 10

$p_0 = x_0.y_0$
$p_1 = x_1.y_0 + x_0.y_1$
$p_2 = x_2.y_0 + x_1.y_1 + x_0.y_2 + c1$ (carry of $p1$)
$p_3 = x_3.y_0 + x_2.y_1 + x_1.y_2 + x_0.y_3 + c_2$ (carry of p_2)
$p_4 = x_3.y_1 + x_2.y_2 + x_1.y_3 + c_3$ (carry of p_3)
$p_5 = x_3.y_2 + x_2.y_3 + c_4$ (carry of p_4)
$p_6 = x_3.y_3 + c_5$ (carry of p_5)
$p_7 = c_6$ (carry of p_6)

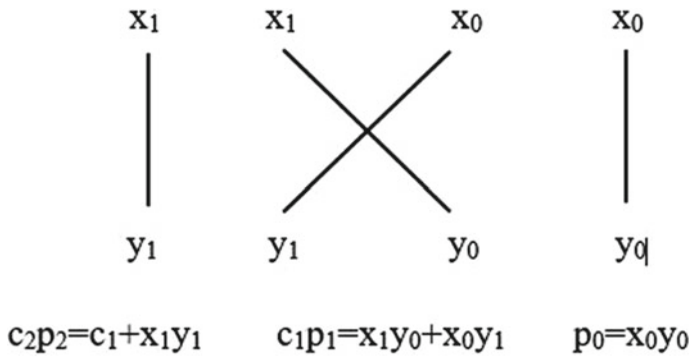


Fig. 9 Urdhva-Tiryagbhyam Sutra for 2 bit numbers

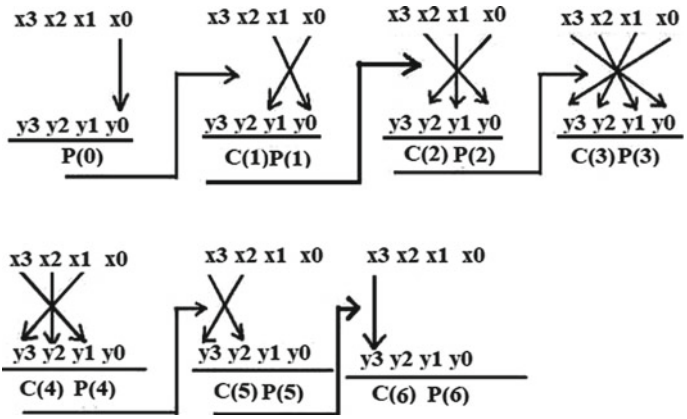


Fig. 10 Urdhva-Tiryagbhyam Sutra for 4 bit numbers

4 Implementation of Vedic Multiplier Units

The basic 2 * 2 UT multiplier block is implemented using the following equations:

$$q_0 = a_0 b_0 \tag{2}$$

$$q_1 = (a_1 b_0) \oplus (a_0 b_1) \tag{3}$$

$$q_2 = (a_0 a_1 b_0 b_1) \oplus (a_1 b_1) \tag{4}$$

$$q_3 = a_0 a_1 b_0 b_1 \tag{5}$$

This can be implemented in a number of ways and hence we have a number of proposed schemes for the 2 * 2 UT multiplier unit which is then used for implementing 4 * 4 multiplier unit which in turn is used to implement 8 * 8 UT multiplier and so on for the higher-order multipliers.

We have implemented six different architectures of the Vedic multiplier in this paper. Let's us have a look at all the six architectures of the reversible 2 * 2 UT multiplier which can then be used to implement higher-order multipliers.

*4.1 Design of 2 * 2 UT Multiplier Unit*

Multiplier_Design 1: This design uses the following gates: 5 Peres gates, a CNOT gate as shown in Fig. 11. Thus, the design has NG = 6, CI = 4, GO = 7 and QC =

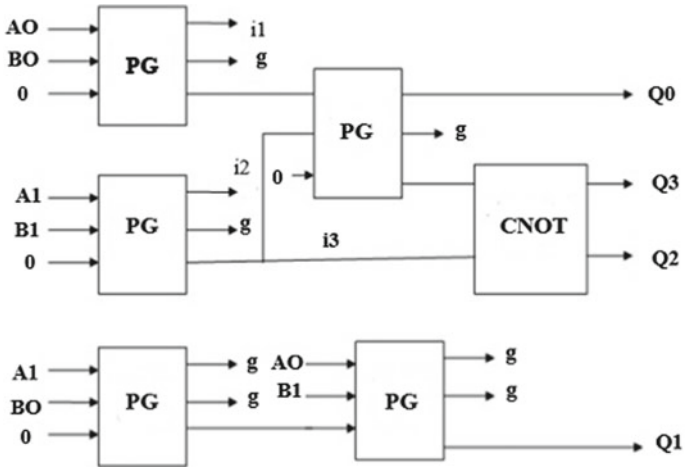


Fig. 11 2 × 2 UT multiplier design 1

21.

Multiplier_Design 2: This design uses 1 BVPPG gate, 3 Peres gates and a Feynman gate as shown in Fig. 12. Thus, the design has NG = 5, CI = 5, GO = 5 and QC = 23.

Multiplier_Design 3: This design uses a BVPPG gate, 2 Peres gates, an NFT gate and a Feynman gate as shown in Fig. 13. Thus, the design has NG = 5, CI = 5, GO

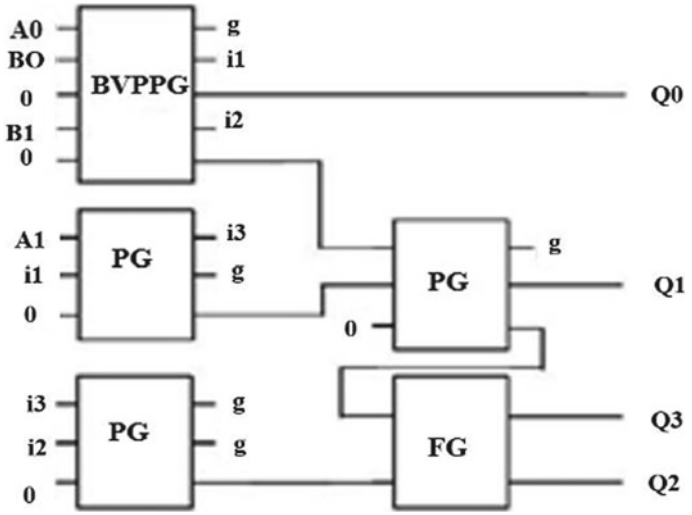


Fig. 12 2 × 2 UT multiplier design 2

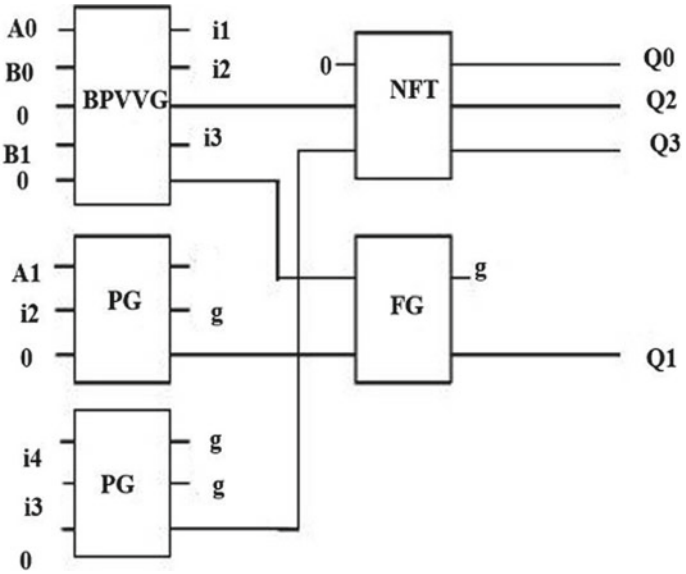


Fig. 13 2 × 2 UT multiplier design 3

= 4 and QC = 24.

Multiplier_Design 4: This design uses a BME gate, 3 Peres gates and a Feynman gate as shown in Fig. 14. Thus, the design has NG = 5, CI = 4, GO = 6 and QC = 18.

Multiplier_Design 5: This design uses two BME and 2 Peres gates as shown in Fig. 15. Thus, the design has NG = 4, CI = 4, GO = 6 and QC = 18.

Multiplier_Design 6: This design uses two BME gates, a Peres gate and a Feynman gate as shown in Fig. 16. Thus, the design has NG = 5, CI = 3, GO = 5 and QC = 15.

4.2 Proposed Fan-Out Generator

In all the above architectures, we have not considered the fan-out of the gates. In the design involving reversible gates, it's very important that we should have fan-out = 1 and hence to eliminate the issue of fan-out being greater than one we have to use any of the following fan-out generators as per the requirement. We can even combine these generators to get required copies of the output.

Feynman gate-based fan-out generator: It makes use of 8 Feynman gates as shown in Fig. 17 to generate two copies of the input and thus has a quantum cost of 8.

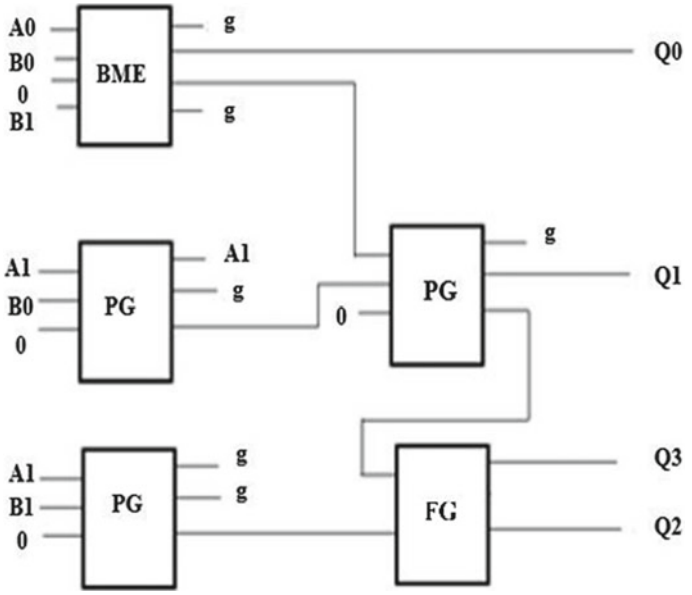


Fig. 14 2 × 2 UT multiplier design 4

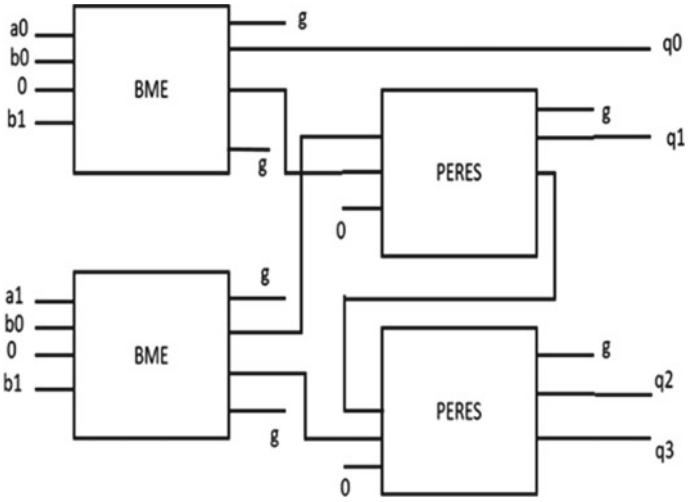


Fig. 15 2 × 2 UT multiplier design 5

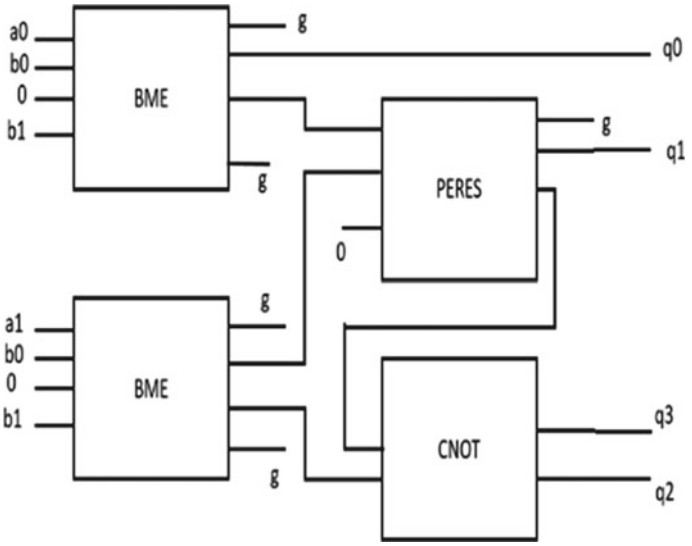


Fig. 16 2 × 2 UT multiplier design 6

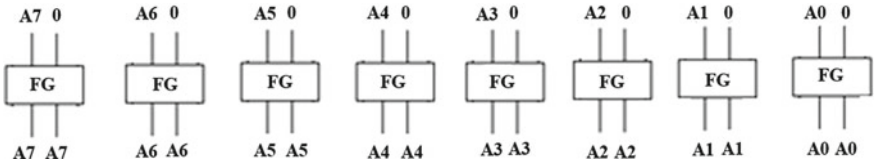


Fig. 17 Feynman gate based fan out generator

BVF gate-based fan-out generator: It makes use of 8 BVF gates as shown in Fig. 18 to generate four copies of the input. We must provide two copies of input using Feynman-based fan-out generator and thus quantum cost becomes 24.

DFG gate-based fan-out generator: It makes use of 8 DFG gates as shown in Fig. 19 to generate three copies of the input and thus has a quantum cost of 16.

In addition to the basic block of 2 * 2 UT multiplier, we will have to use the above fan-out generators in the design of the multiplier block which adds up to the cost of the design.

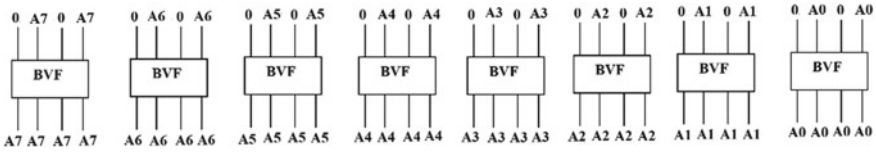


Fig. 18 BVF gate based fan out generator

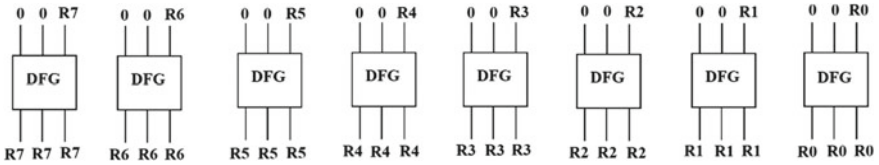


Fig. 19 DFG gate based fan out generator

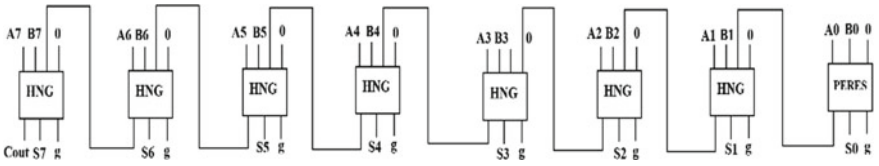


Fig. 20 8-bit RCA block

Adders: The other computational unit that we use in our design is the adder block which is a simple RCA (ripple carry adder) which uses HNG gates as shown below in Fig. 20.

We can combine the above 8 bit blocks to form next higher-order adders like 16-bit adder and so on.

*4.3 Design of 4 * 4 reversible UT multiplier*

The 4 * 4 multiplier can be implemented using any of the above six architectures as shown in Fig. 21. We use four 2 * 2 UT multiplier units along with two 4-bit RCA, a half adder and a 2-bit RCA unit.

*4.4 Design of 8 * 8 Reversible UT Multiplier*

The 8*8 multiplier can be implemented using any of the above six architectures as shown in Fig. 22. We use four 4 × 4 UT multiplier units along with two 8-bit RCA units, a half adder and a 4-bit adder.

*4.5 Design of 16 * 16 Reversible UT Multiplier*

The 16 * 16 multiplier can be implemented using any of the above six architectures as shown in Fig. 23. We use four 8 * 8 UT multiplier units along with two 16-bit

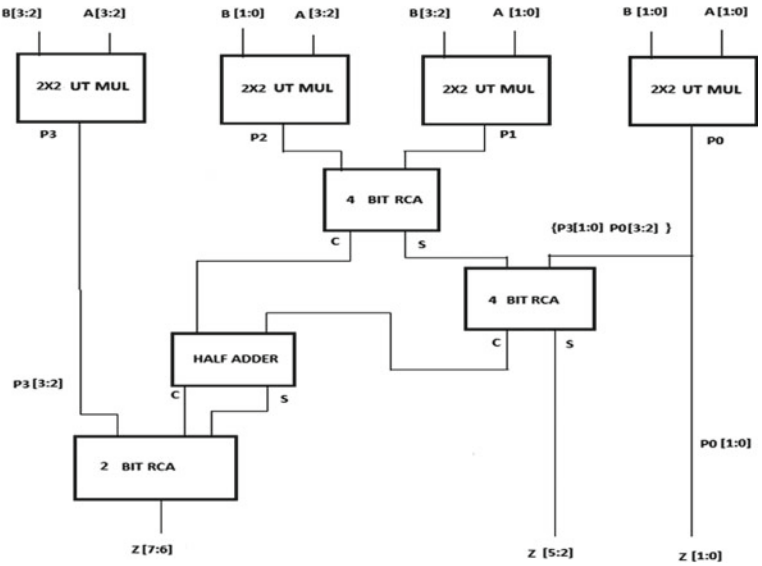


Fig. 21 4 × 4 Reversible UT multiplier

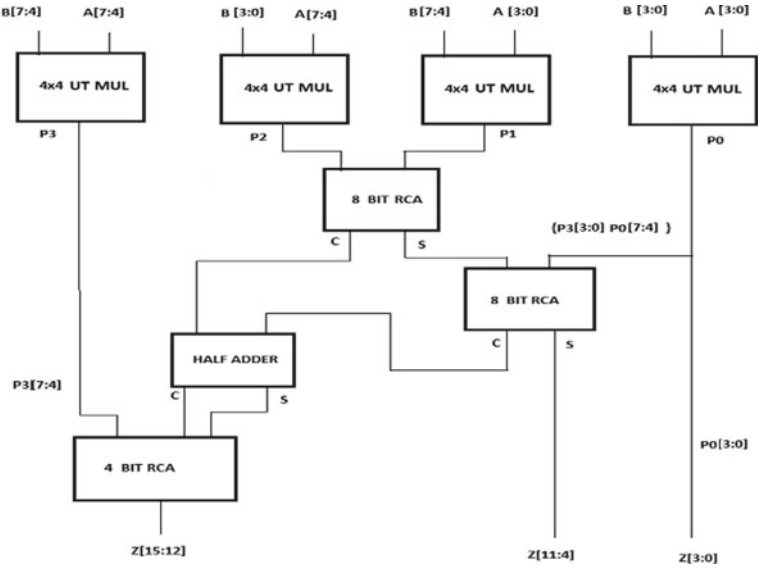


Fig. 22 8 * 8 reversible UT multiplier

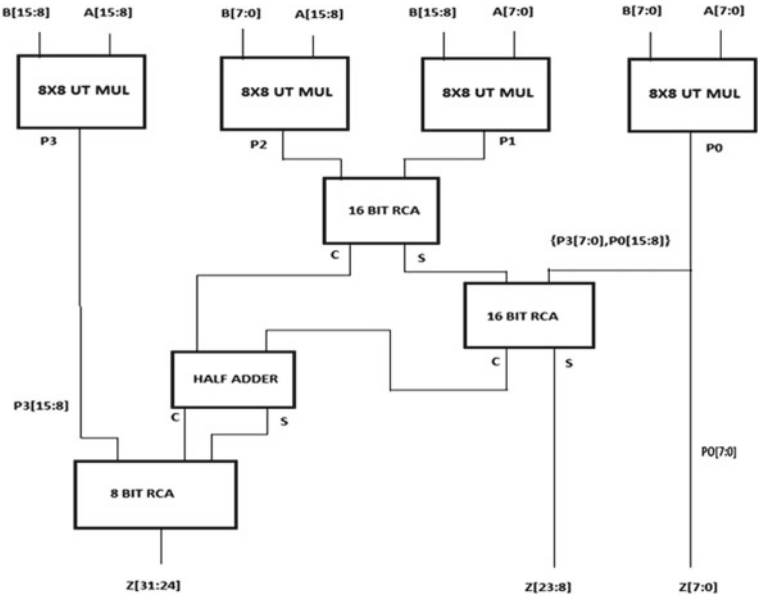


Fig. 23 16 * 16 reversible UT multiplier

RCA units, a half adder and an 8-bit adder.

5 Results and Analysis

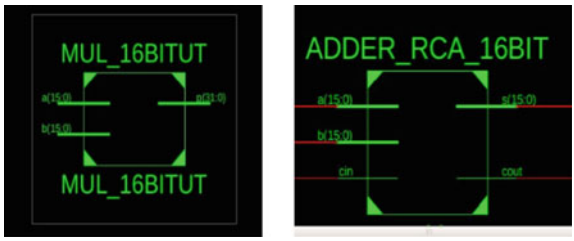
In this paper, we have shown the implementation of six different design architectures of Vedic multiplier using reversible logic. The design has been implemented using Xilinx ISE 14.7 Design Suite, using Verilog HDL on Spartan 6 FPGA. The results of the analysis of all the six architectures with its computational complexity have been presented in this section.

The block level diagrams, RTL of few of the units and results of simulation are shown in Figs. 24, 25, 26, 27, 28 and 29.

5.1 Analysis and Comparison Results of the Implemented Reversible Vedic Multiplier Designs

Tables 1, 2, 3 and 4 show the comparison of all the six design architectures for 2 * 2, 4 * 4, 8 * 8 and 16 * 16 multipliers, respectively, in terms of its cost metrics.

Figure 30 shows graphical representation of the comparison results for 8 * 8 and



(a) (b)

Fig. 24 Block level diagram of **a** 16 bit multiplier **b** 16 bit adder

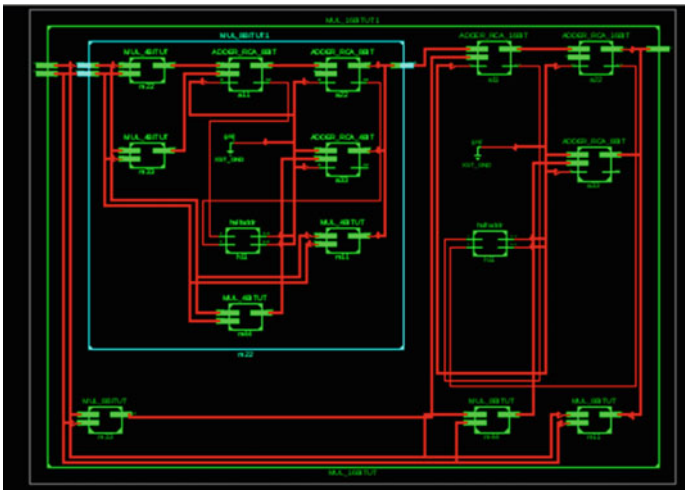


Fig. 25 RTL of 8 bit multiplier

16 * 16 multiplier. Figure 31 shows the TRLIC, power delay product (PDP), number of LUT slices and delay for the 16 * 16 multiplier implementation.

6 Conclusion

In this paper we have presented six different reversible Vedic multiplier architectures which can be used for the implementation of low-power digital filter. The results prove that of the six architectures the performance parameters of the sixth architecture are optimized in terms of all the factors including the cost metrics, area and delay as well as power consumption. Significant reduction in gate count, constant inputs, garbage output, quantum cost as well as overall cost of implementation is observed in the case of design 6 from the implementation. For a 16 * 16 multiplier, design 6 shows 7.2% reduction in total implementation cost compared to design 5, 8.5% compared to design 4 and 15.6% compared to the rest of the three designs. Quantum cost has

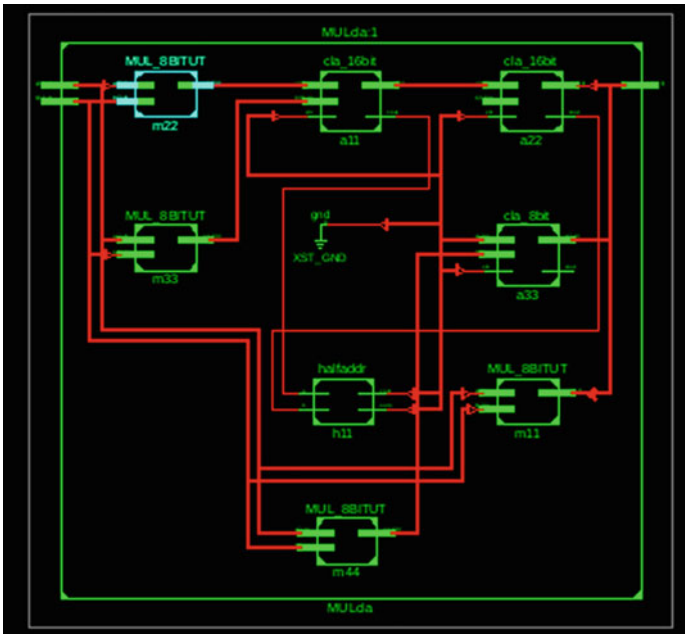


Fig. 26 RTL of 16 bit multiplier unit

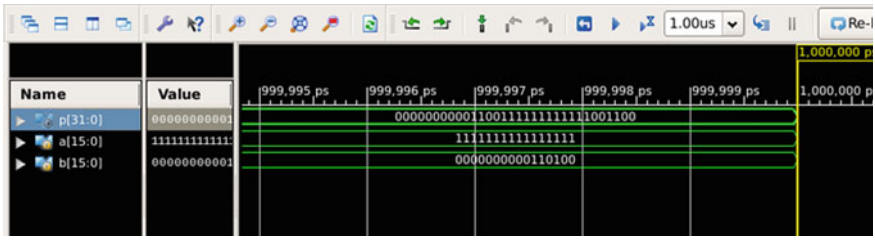


Fig. 27 Simulation waveform of 16 bit multiplier unit using design 4

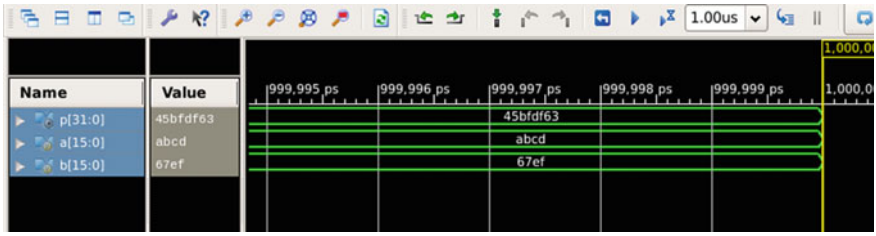


Fig. 28 Simulation waveform of 16 bit multiplier unit using design 5

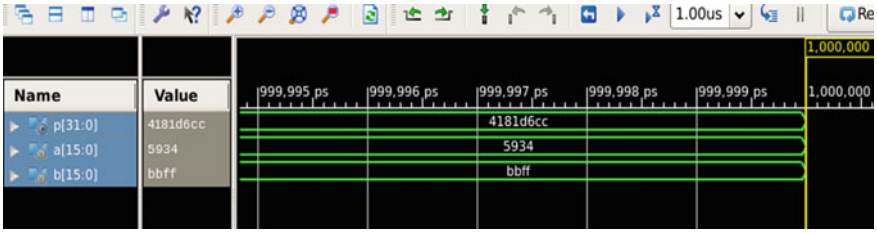


Fig. 29 Simulation waveform of 16 bit multiplier unit using design 6

Table 1 Cost metrics comparison for 2 * 2 UT multiplier

2 * 2 multiplier	NG	CI	GO	QC	TRLIC
Mul_Design 1	6	4	7	21	38
Mul_Design 2	5	5	5	23	48
Mul_Design 3	5	5	4	24	38
Mul_Design 4	5	4	6	18	33
Mul_Design 5	4	4	6	18	32
Mul_Design 6	4	3	5	15	27

Table 2 Cost metrics comparison for 4 * 4 UT multiplier

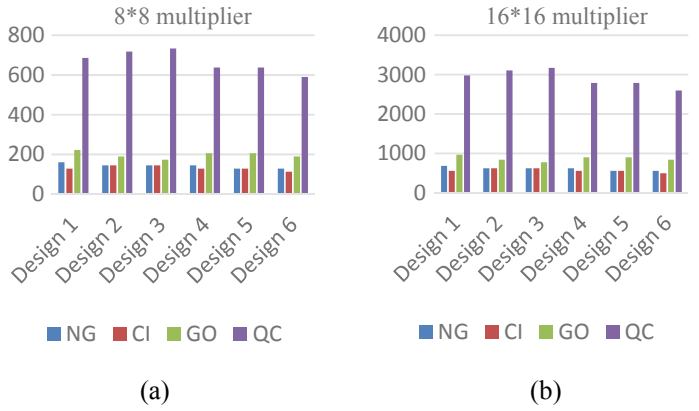
4 * 4 multiplier	NG	CI	GO	QC	TRLIC
Mul_Design 1	35	27	46	142	250
Mul_Design 2	31	31	38	150	250
Mul_Design 3	31	31	34	154	250
Mul_Design 4	31	27	42	130	234
Mul_Design 5	27	27	42	130	226
Mul_Design 6	27	23	38	118	206

Table 3 Cost metrics comparison for 8 * 8 UT multiplier

8*8 multiplier	NG	CI	GO	QC	TRLIC
Mul_Design 1	161	129	222	686	1198
Mul_Design 2	145	145	190	718	1198
Mul_Design 3	145	145	174	734	1198
Mul_Design 4	145	129	206	638	1118
Mul_Design 5	129	129	206	638	1102
Mul_Design 6	129	113	190	590	1022

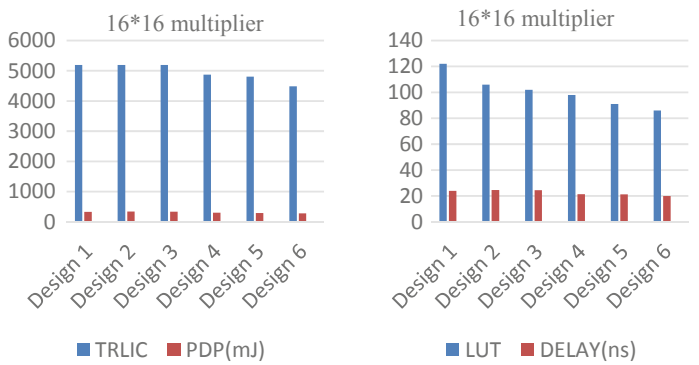
Table 4 Cost metrics comparison for 16 * 16 UT multiplier

16 * 16 multiplier	NG	CI	GO	QC	TRLIC
Mul_Design 1	685	557	966	2982	5190
Mul_Design 2	621	621	838	3110	5190
Mul_Design 3	621	621	774	3174	5190
Mul_Design 4	621	557	902	2790	4870
Mul_Design 5	557	557	902	2790	4806
Mul_Design 6	557	493	838	2598	4486



(a) (b)

Fig. 30 Comparison of the cost metrics for **a** 8 * 8 multiplier **b** 16 * 16 multiplier



(a) (b)

Fig. 31 Comparison of the **a** TRLIC and PDP **b** Area and delay for 16 * 16 multiplier

reduced by 7.4% compared to design 5 and 4, 22.1% compared to design 3, 19.7% compared to design 2 and 14.7% compared to design 1.The reduction in the number of gates is found to be 11.5% compared to design 2, 3 and 4, 23% compared to design 1. Reduction in LUT slices is found to be 5.8% compared to design 5, 13.9% compared to design 4, 18.6% compared to design 3, 23.3% compared to design 2 and 41.8% compared to design 1. This implementation finds applications in many of the reversible logic-based designs including reversible digital filters, quantum processing units (QPU) and other digital signal processing and image processing applications. In the future we plan to design new architectures for the reversible Vedic multiplier units with further optimized performance parameters and increased efficiency for implementing in reversible digital filters and other low-power processing units.

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Spectrum Defragmentation in SDM-EONs with Multi-core Fiber for Crosstalk Reduction

Arinjay Bisht and T. Velmurugan

1 Introduction

The Network Traffic demand as of recent has seen a rapid increase, and this growth is projected to continue well into the future. This increase in demand has been of concern to researchers who have as a result investigated a variety of technologies to deal with the lack of optical network capacity. For this purpose, the WDM technique provides an opportunity for effective utilization of bandwidth of a fiber with the additional capability of routing and switching the wavelengths, which certainly puts the WDM network in position to be considered as a viable candidate as far as optical networks are considered. In a WDM network, the inflexible and coarse granularity however, restricts optical networks having a rigid system for the assignment of bandwidth, and an inefficient utilization of network capacity, and high capital expenditure [1]. To counteract the inconsistencies and deficiencies of a WDM Network, another technology has been proposed, namely the elastic optical network, an introduction to which was first made in [2], and which is capable of expanding the capacity of optical fibers through the efficient utilization of spectrum resources with flexible allocation. This flexibility which is derived from fine-grained provisioning of resources can potentially reduce the wastage of spectrum resources [3], compared with traditional rigid spectrum assignments associated with WDM Networks. However, there are constraints limiting the capabilities of Routing and Spectrum Allocation techniques, which need to be satisfied according to traffic demands having a tendency of changing dynamically. Therefore, despite improvements in the performance of optical networks through dynamic resource allocation, it is anticipated that optical

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fibers will soon reach their physical limit in terms of capacity. Space-division multiplexing (SDM) is a relatively new multiplexing technology which has been proposed as a successor to WDM in a bid to assure the continued fiber capacity expansion, on which intensive research has been carried out over the years [4]. Multicore fiber (MCF) has been proposed as an innovative replacement for existing fiber technology to be used in combination with SDM technology. Doing so, it would be possible to theoretically scale the capacity of the fiber by a factor equivalent to the number of existing cores in the MCF, while simultaneously incrementing the density of the core through the usage of separate fiber bundles [5]. MCF faces a significant problem, i.e., the physical loss of transmission signals as a consequence of inter-core crosstalk. This is subject to the number of cores in the concerned MCF, information related to its refraction index, and the interior cladding disposition [6]. The crosstalk in MCF can be reduced by means of a suitable network resource management scheme. Also, with the help of SDM technology, MCF can help enhance the capacity of fibers by a factor which is proportionate with the number of cores. SDM-EONs are therefore being recognized as potentially suitable contenders for application in optical transport networks for future purposes. In order to realise the same, new routing and spectrum allocation (RSA) strategies are required as opposed to traditional ones which are highly customized, and therefore cannot be applied to SDM-EONs.

2 SDM-EON and Multi Core Fibers

A. Elastic Optical Networks

In an elastic optical network, the architecture involves the division of the allotted frequency spectrum into several frequency slots. Light-paths are established by means of flexible allocation of the frequency slots (FSs). The primary advantage of using this type of network architecture is that it facilitates efficient provisioning of spectrum resources, or in other words, allocating resources with just sufficient bandwidth as per the requirements of the network connections [3]. In case of a requirement of an optical path that is conveniently short, the network versatility can be exercised for the selection of a spectrally efficient scheme of modulation such as Quadrature Amplitude Modulation (QAM) in order to manage a spike in the optical signal-to-noise ratio (OSNR). Conversely, when the requirement is that of an optical path which is long, a modulation format like Quadrature Phase-Shift Keying (QPSK) is recommended, which is spectrally inefficient, in a bid to manage the case of lower OSNR. In an elastic optical network spectrum assignment has the attribute of being distance adaptive and also maintains the ability to save spectrum resources such as FSs. Therefore, it can be ascertained for a fact that the performance of EONs depends

strongly on the proper implementation of an effective Routing and Spectrum Allocation (RSA) Strategy which can efficiently manage and allocate available spectrum resources.

B. **Multi-Core Fiber**

Over the years, substantial research work has been conducted in search for a more efficient utilization of elastic optical networks. Input power is one of the physical limitations plaguing the fiber capacity, and is constrained mainly by two factors. One of the factors is the phenomenon involving the fusing of fibers [7]. Due to this in a situation where there is a large number of transmitted signals, yield of optical fiber power increases dramatically, excess of which can lead to the melting of the core of the fiber. This phenomenon continues to cause excessive overheating until the input power for the fiber is reduced to optimum levels. Signal degradation is the second factor with regards to nonlinear optical effects [8], which are responsible for generation of nonlinear interference in WDM signals. Therefore, to deal with the limitations surrounding existing technologies which continue to disrupt the expansion of the capacity of fibers, innovative fibers such as Multi-Core Fibers (MCF) have been proposed. MCF not only helps in promoting efficient spectrum resource allocation which in turn leads to expansion of its transmission capacity. At the same time this helps overcome the constraints involving RSA [2]. Multiple light-paths in an EONs with MCFs can be established, which can be characterized as having the same frequency slots, when they are being transmitted through different cores. It has also been indicated that using MCF with SDM scheme has been anticipated to effectively deal with physical limitations [9].

3 Related Work

Fragmentation is a well-known phenomenon in any Fiber Optics Communication System. To mitigate the constraints posed by Spectrum Fragmentation (SF) particularly considering dynamic traffic. The fragmentation problem has been addressed in [10], and in an effort to quantify the SF, a specific metric has been developed. Also, a provisioning strategy has been proposed which aims at efficiency with the help of optimum bandwidth portioning. In [11], it has been proposed by the authors that for flexible networks such as EONs, network defragmentation leads to significant consolidation of spectrum resources available. The RSA Strategy has been split into two challenges to be dealt with, i.e., routing scheme and spectrum allocation. In past research works, this strategy has been analysed comprehensively, and several solutions including those based on the Integral Linear Programming (ILP) have been suggested, but this was abandoned due to very high computational complexity. The SF problem has been addressed even further in [12], where authors proposed two strategies, in which more emphasis was put on addressing route fragmentation instead of link fragmentation which had served as the basis of past strategies. These

two strategies are namely RFARSA (Route Fragmentation Aware RSA) and LLRSA (Least Loaded RSA). Another work [13] elucidates the features of two proposed strategies for Spectrum assignment based on Defragmentation, the first one being the Shortest Path RSA (SPRSA) in which as the name suggests is based on calculating and subsequently selecting the shortest available route for the Network allocation of the spectrum that has been requested. The performance of this strategy declines and therefore is not suitable for application as a result of the two factors: (1) The spectrum is being unevenly assigned on the links, i.e., while undertaking spectrum assignment the loading of the link is not considered, and (2) Occurrence of Spectrum Fragmentation as a result of fragments being created in the links. This SF in the requested spectrum is a result of deallocation, and subsequent decrease in the available routes for handling upcoming requests. The second strategy holds more promise which corresponds to Defragmentation based Load Balancing RSA (DLBRSA). As part of this particular strategy the network resources initially get deallocated as a result of termination of connection, which is followed by defragmentation which assists in reallocation of network traffic and lastly a customized network reconfiguration. Our work has drawn inspiration from all these previous efforts which despite their shortcomings have proven their effectiveness to some extent, which has essentially motivated us to carry this work forward.: (1) Selection of a shorter route, (2) Reduction of fragmentation, and (3) Depreciation in the consumption of network capacity given that new route is shorter compared to the route prior the process of defragmentation. Fragmentation aware RWSA proposed in [14], aims at increasing spectrum utilization of the network and correspondingly reducing computational complexity. EONs act as the backbone which is primarily tasked to fulfil the forthcoming surge in the bandwidth demand. Therefore, it is essential to mitigate the effects of the limitations posed by existing strategies by modifying them to achieve their desired purpose in this new generation. This paper integrates an efficient technique of involving routing and the proper assignment of spectrum resources for implementing Crosstalk Elimination and Spectrum Defragmentation.

Fragmentation-aware RSA is a successful approach towards minimizing spectrum fragmentation in EON which has been demonstrated in [15], by formulating a linear integer programming model for multiple non-dynamic connection requests, and which has also considered the continuity and non-discrete nature of the optical spectra of the substrate fiber links (SFLs). This method has shown promise by facilitating a reduction in the fragments in a spectrum slot, while also improving the blocking rate of connection requests. In [16] a new "cut-based" metric has been proposed to evaluate link fragmentation, while another metric named "alignment" considers the misalignment of the slots available during the provisioning of connection paths. In [17] the authors made a case for a spectrum compactness index for determining the need to trigger a defragmentation process in a consolidated scattered spectrum. For this purpose, there has been an adoption of two major methods in the domain of optical spectra: (i) a routing and spectrum allocation (RSA) scheme which simultaneously keeps fragmentation in check, similar to the one proposed in [13], and is used to minimize the fragmentation in the first place, and reduce crosstalk, and (ii) Facilitating a uniform allocation of frequency slots (FSs) on the provided links

in a network, which further consolidates the scattered spectrum and correspondingly helps in increasing spectrum usage and an efficient usage of network bandwidth capacity.

4 Existing and Proposed Strategies

This section entails the key features related to the strategies that have been considered in this paper, which are as follows: (1) SPRSA, (2) LLRSA, (3) RFARSA, (4) CESDRSA.

A. **Shortest Path RSA (SPRSA)**

As part of this strategy, based on the availability of the requested shortest route the network assignment of the spectrum that has been requested is undertaken in accordance with the first fit policy. The constraints of continuity and contiguity must be satisfied by the route that has been requested. The decline in the performance of this particular strategy can be blamed on the two major factors: (1) The assignment of spectrum to the links is performed in an uneven manner, i.e., while undertaking spectrum assignment, the loading of the link is not taken into consideration and (2) Owing to the de-allocation of some of the requests, fragments are created in the links, which results in Spectrum Fragmentation and increases occurrences of Crosstalk. Therefore, the subsequent route availability decreases for future requests as a consequence of Crosstalk resulting from Spectrum Fragmentation.

B. **Least loaded RSA (LLRSA)**

In the following strategy, we take into consideration all the alternate routes for each connection request that is made. The least loaded route that is assigned to a particular connection request, is selected from K-alternate routes. For such a route, the number of Frequency Slots that can be availed is maximum. This policy allocates the spectrum load homogeneously among the various links in the network.

C. **Route fragmentation aware RSA (RFARSA)**

In RFARSA, the assignment to a given connection request is made by selecting the route which has the lowest value of RFI, where RFI can be expressed in the form of the equation: $-\ \mathrm{RFI} = 1 -$ (Maximum Adjoining Frequency Slots that are also free on a given Route/Total Number of Frequency Slots that are free on a given Route). As part of this strategy, the route having the maximum number of adjoining Frequency Slots (FSs) is given preference over other routes that are potential candidates for assignment, and the routes which are less fragmented are accorded a higher priority. In this strategy the route which best conforms to the continuity of the spectrum and its respective contiguity when compared to all the other routes, gets the priority is which is favourable for the efficient assignment of spectrum.

D. Crosstalk Elimination Spectrum Defragmentation RSA (CESD-RSA)

In this proposed strategy, following the termination of connection the network resources get deallocated. In our observations we noticed that even after deallocation some spectrum fragments continue to remain in the network links, which leads to a case of unutilized spectrum. In an effort to deal with the bandwidth drop that would normally accompany this, we would deploy defragmentation which aims at re-assigning the network traffic. This also helps in minimizing the crosstalk effect in MCF which significantly depends on the arrangement of connection links in context of the spectrum and core. On completing the search for the least loaded shortest route—which is the one having the maximum available Frequency Slots—the utilized resources are minimized. Once the deallocation process is complete, the reconfiguration of network takes place in accordance with the proposed strategy which proves to be advantageous in the following ways: (1) Choosing of a shorter route having maximum frequency slots, (2) Reduction in fragmentation and corresponding crosstalk, and (3) As the new route is proposed to be shorter than the original route before defragmentation process takes place, a decrease in network capacity consumption is also observed (Fig. 1).

In the proposed algorithm described in the above flowchart, Step 2 has a computational complexity of (N_oR) (where N_oR stands for the number of requests), while Step 3 has a computational complexity of (J) (where J represents the number of alternative available routes). We let *ECR* stand for the total number of existing requests for connection in the given network. Similarly, the computational complexity of the operations involving Steps 11 and 12 are $O(ECR)$ and $O(ECR \times J)$ respectively, while the rest of the steps have a constant computational complexity $(O(1))$. Hence, we can calculate the net computational complexity of the proposed system to be equal to $O((N_oR \times J) + (ECR(J + 1))$.

5 Result and Analysis

In an effort to evaluate the performance aspects of the CESD-RSA strategy, and subsequently compare the same with existing strategies, such as SPRSA, LLRSA, RFARSA, we performed simulations using suitable programming toolkits available with the MATLAB software. The strategies have been evaluated on two realistic network topologies namely National Science Foundation Network (NSFNET), and Elastic Optical Network (EON). We simulated the CESD-RSA, SPRSA, LLRSA and RFARSA strategies on the bases of two metrics of critical to the success of our proposed strategy. These are the Bandwidth Blocking Probability (BBP), and the percentage of network capacity utilization (NCU).

We have evaluated the performance of the aforementioned strategies under two predefined scenarios: (1) for an increase in load (in Erlang), and (2) for an increase in demand for FSs. While, the management of spectrum resources for different scenarios concerning demand in each of these strategies is evaluated by the increase in load,

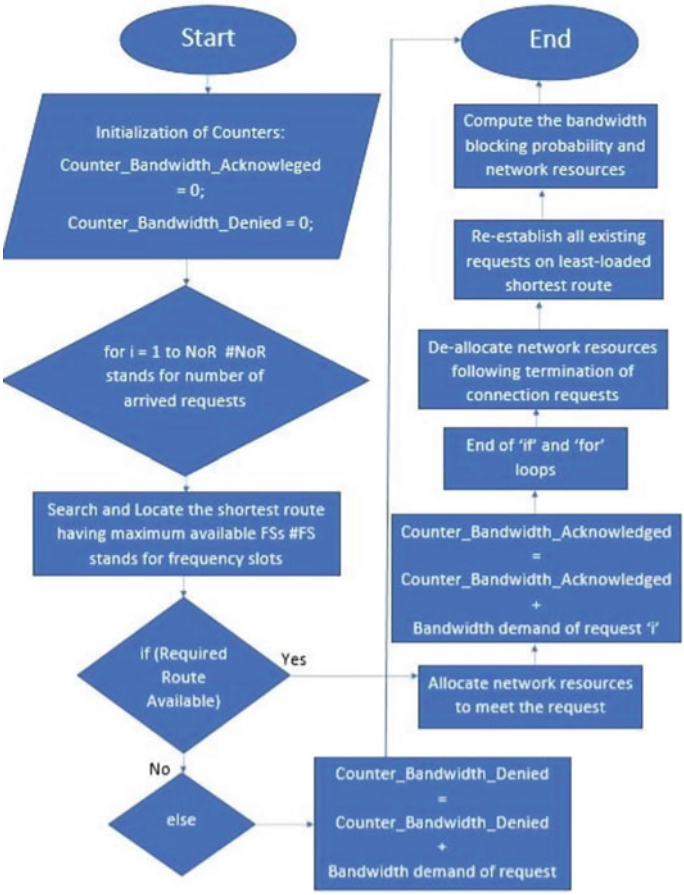

Fig. 1 CESD-RSA algorithm flowchart

the evaluation made upon an increase in demand for FSs helps in the analysis the impact of constraints involving spectrum allocation on both the proposed strategy and the ones that are already in action.

A. **Bandwidth Blocking Probability**

In Fig. 2a and b, we can observe the variation in Bandwidth Blocking Probabilities (BBP) for the strategies taken into consideration with load (Erlang) for the network topologies NSFNET and EON respectively. BBP is the ratio of the blocked bandwidth demands to the total demand of bandwidth. the proposed CESDRSA strategy, the BBP is substantially lower than that of SPRSA, LLRSA and RFARSA. Considering Fig. 3a and b which illustrates the BBP variation of the strategies for an increase on the number of frequency slots, given a load of 200 Erlang in the NSFNET and EON network topologies respectively, we can clearly observe that CESD-RSA provides

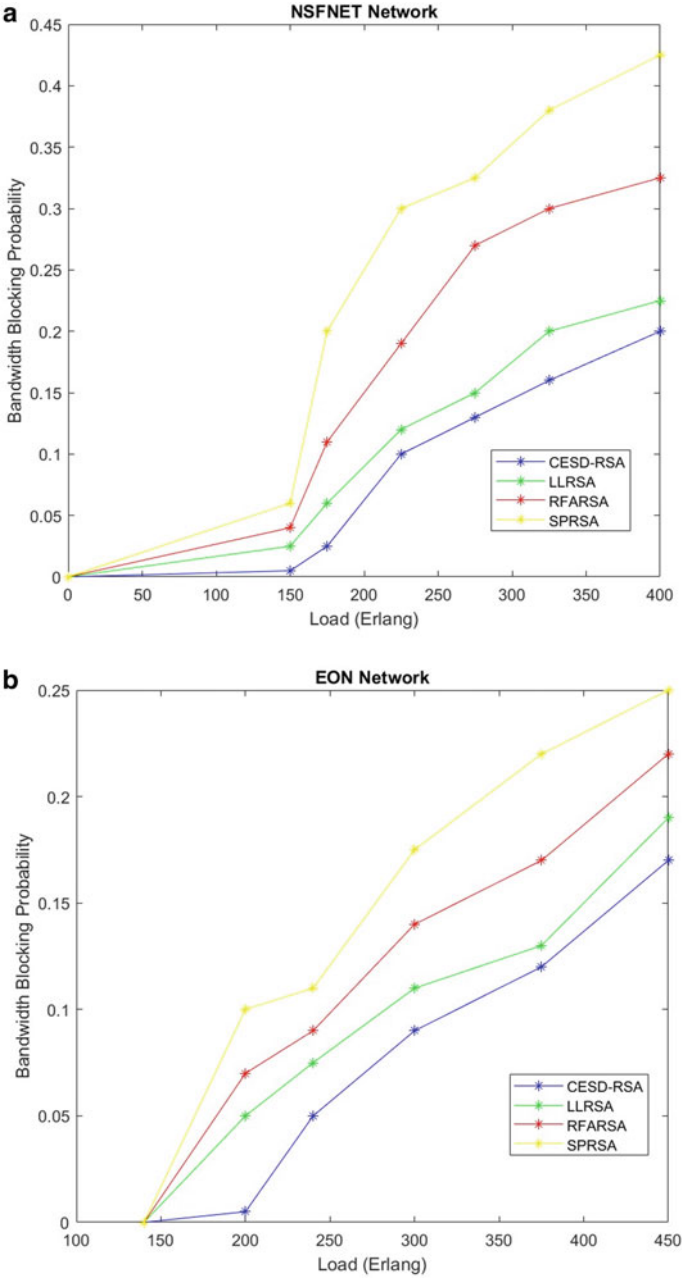

Fig. 2 **a** Bandwidth blocking probability versus Load (in Erlang). **b** Bandwidth blocking probability versus load (in Erlang)

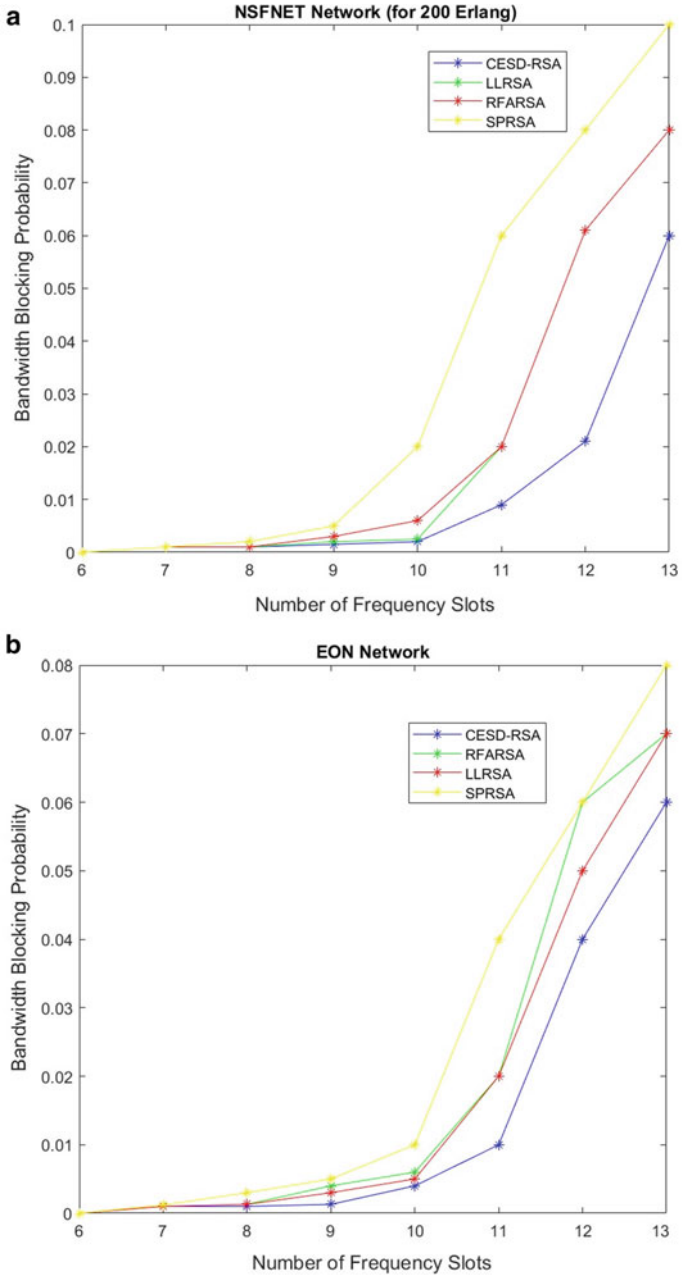

Fig. 3 **a** Bandwidth blocking probability versus number of frequency slots (for 200 Erlang). **b** Bandwidth blocking probability versus number of frequency slots (for 200 Erlang)

much better results than the other existing strategies. All this correspondingly proves that the proposed strategy does make a substantial difference. Lower BBP of CESD-RSA can be attributed to the following: (1) Efficient utilization of network resources, due to the selection of a path having the largest frequency segment that is available, and (2) Reduction of network fragmentation with the help of defragmentation in order to enable proper resource utilization. This leads to an increase in the availability of routes, thereby causing a reduction in the BBP. A lower Bandwidth Blocking Probability is usually preferred for Network Topologies as it ensures seamless data transfer capabilities for the comfort of the user, without facing any unwanted obstructions which can hamper its performance and cause inconvenience.

B. **Network Capacity Utilization**

The utilization of the given network in terms of its load capacity for the aforementioned topologies is illustrated in Figs. 4 and 5. In the case of a high network load, there is more demand of network resources, which leads to a proportionate increase in resource consumption. In Fig. 4a and b we can observe the variation in Network Capacity Utilization for an increase in load (in erlang) in the network topologies namely NSFNET and EON respectively, while in the case of Figure of 5(a) and 5(b) we can observe the variation in Network Capacity Utilization for an increase in the number of frequency slots, given a load of 200 Erlang in the NSFNET and EON network topologies respectively. A lower Network Capacity Utilization value is preferred for network topologies since it leaves more room for any other miscellaneous data transfer and operations involving storage and handling of data.

From the results demonstrated for both network topologies, we can infer that the NCU is lower for the CESD-RSA strategy when compared with the SPRSA strategy or for that matter other existing strategies because the longer routes tend to get clubbed up with the shorter paths following reconfiguration, of which the shortest path is given priority since it has the maximum number of available FSs. Conversely, in other existing strategies, issues with proper spectrum alignment, higher fragmentation, along with an increase in load, lead to unavailability of the shorter routes. Hence, all this contributes to the deterioration of the performance of these strategies. The same can be inferred from the results tabulated in the Tables 1 and 2.

6 Conclusion

Here we successfully addressed two fundamental problems that are commonly encountered when developing schemes which can act as a barrier in the efficient implementation of traditional RSA strategies: (1) spectrum fragmentation leading to crosstalk, and (2) inefficient usage of network bandwidth capacity as a result of frequency slots being non-uniform allocated on the network connection links. We have attempted to minimize these problems using the CESD-RSA Strategy. In our undertaking of allocating resources to a connection request, we have assigned the

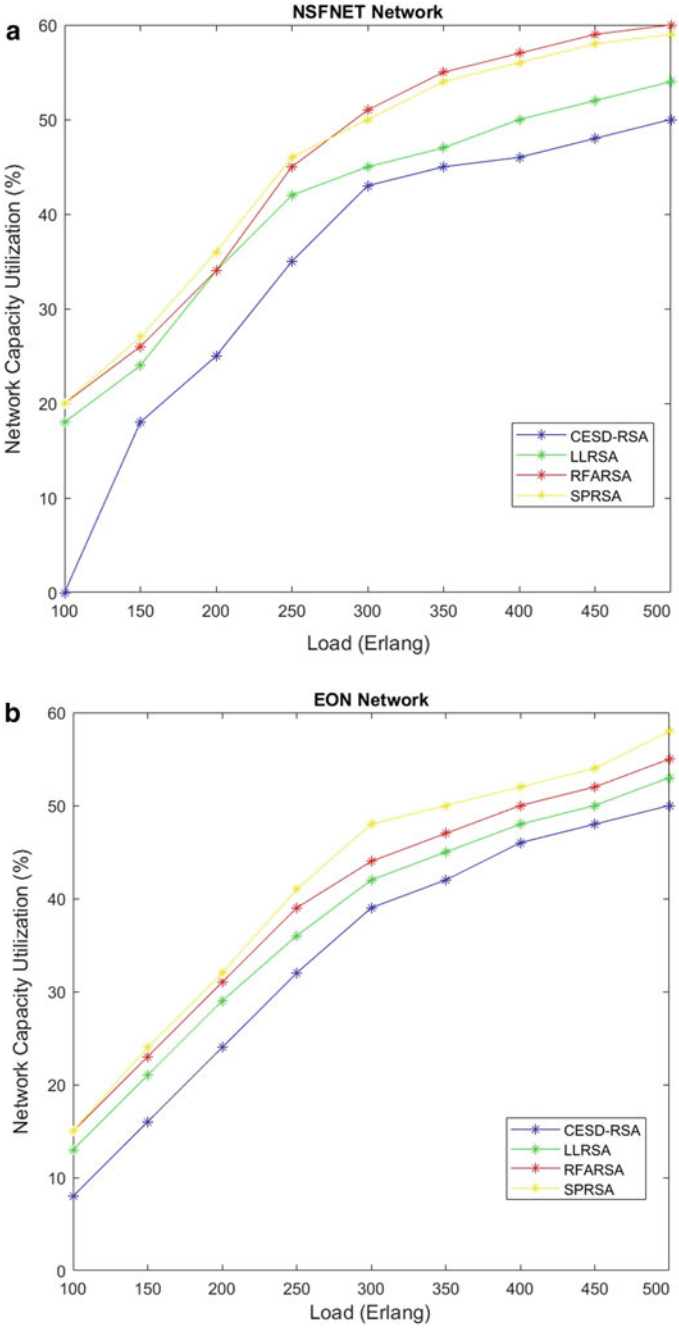

Fig. 4 **a** Network capacity utilization (%) versus load (in Erlang). **b** Network capacity utilization (%) versus Load (in Erlang)

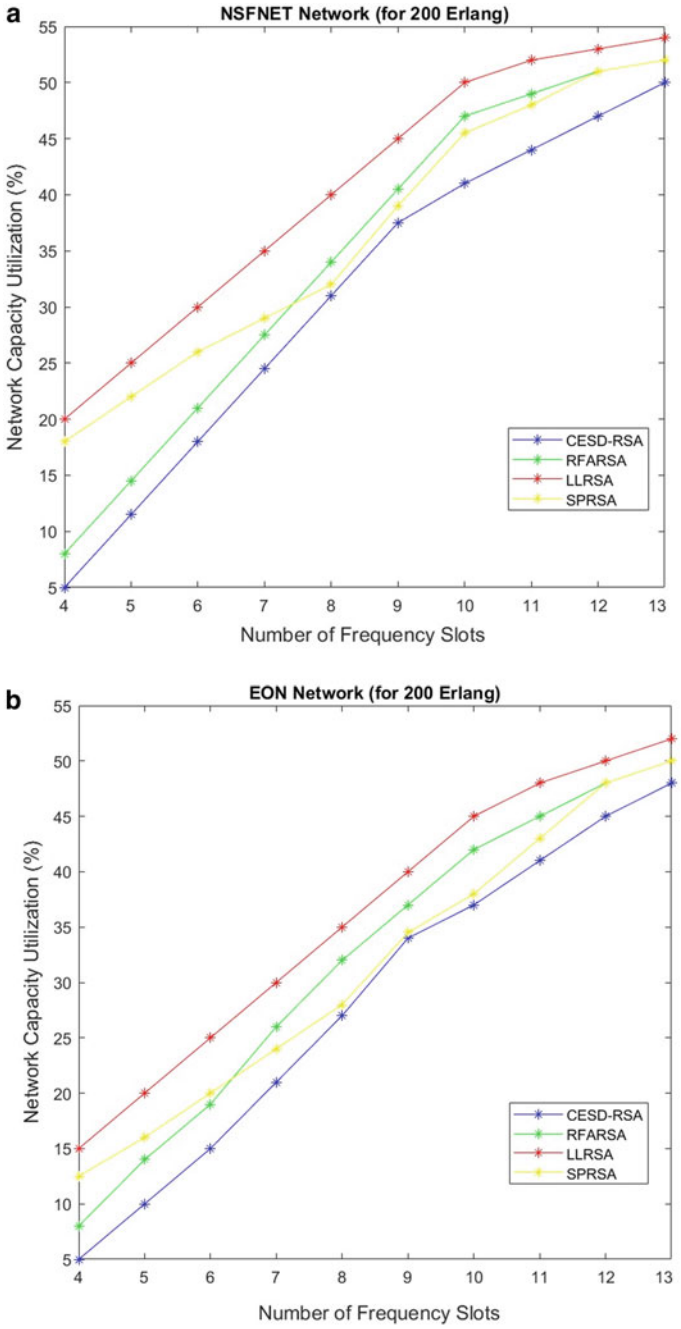

Fig. 5 **a** Network capacity utilization (%) versus number of frequency slots (for 200 Erlang). **b** Network capacity utilization (%) versus number of frequency slots (for 200 Erlang)

Table 1 Average of different values of network parameters of Figs. 2a, b, 4a and b

Network parameter	Network topology	RFARSA	SPRSA	CESD-RSA	LLRSA
BBP	NSNFET	0.205	0.28625	0.1075	0.12875
	EON	0.15125	0.1875	0.1	0.1175
Network capacity utilized (%)	NSNFET	52.25	52.25	41.25	46
	EON	39	40.25	30.5	36

Table 2 Average of different values of network parameters of Figs. 3a, b, 5a and b (for Load: 200 Erlang)

Network parameter	Network topology	RFARSA	SPRSA	CESD-RSA	LLRSA
BBP	NSNFET	0.041	0.04375	0.0225	0.04025
	EON	0.03975	0.0495	0.02775	0.037
Network capacity utilized (%)	NSNFET	38	38.25	35.05	46
	EON	36	36.15	32	38.35

shortest route having the largest number of FSs available. This leads to an increase in the optimum utilization of the available network capacity. The simulations performed have displayed the comparatively lower BBP values as well as relatively efficient utilization of network capacity upon testing the proposed strategy. These encouraging results further support our claim that the proposed CESD-RSA algorithm is better than its contemporaries for both NSFNET and EON network topologies. As for future applications, the proposed algorithm shows great promise to be effectively used on a variety of network applications ranging from 3D designs for elastic optical network to virtual embedding of optical networks in EONs.

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Miniaturized Circularly Polarized Broadband Antenna Based on CRLH-TL Metamaterials for 5G Millimeter-Wave Applications

Swati Sharma, Rekha Mehra, and Sanjeev Yadav

1 Introduction

To overcome the issue of limited bandwidth, channel capacity, increase in wireless traffic, and need of high data rate for upcoming technologies like virtual reality and smart cities, the prime focus of researchers is to utilize the unused millimeter-wave spectrum for 5G. To meet the requirements of 5G mobile communication, the expectation from the antenna is to be compact, broadband, circularly polarized having high gain, and high efficiency. Over the years, the number of techniques has been applied to achieve broadband circularly polarized antenna [1–4]; however, they are having a large dimension.

Several techniques are applied to miniaturize the antenna [5–7]; however, they suffer from narrow bandwidth. Literature is available of high gain and high-efficiency antenna, but their dimension is large, and even bandwidth is low [8, 9].

There are two types of frequency band that are anticipated to be used for 5G, sub-6 z, and millimeter-wave spectrum [10]. CRLH-TL based metamaterial is widely used in miniaturized antenna due to its electromagnetic property of zero propagation constant and anti-parallel phase and group velocity though they are pursuing narrow bandwidth [11, 12]. When the CRLH unit cell is used along with the co-planar waveguide feeding technique, it increases the aperture of the antenna.

Based on the above requirements and findings, a novel CRLH metamaterial-based, CPW-fed, highly compact, and circularly polarized broadband antenna is presented in this paper, which covers the millimeter-wave spectrum allocated for 5G mobile communication with the desired radiation pattern.

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2 Antenna Design

In this section, the stepwise design of the proposed antenna is explained in detail. The antenna is fabricated on Rogger RT 5880 substrate ($\varepsilon_r = 2.2$, $h = 0.51$ mm), with the dimension of 10 mm × 10 mm, and the values of parameters are shown in Table 1. The simulation is performed using CST microwave studio suite 2020. Figure 1 displays the stepwise design of the antenna and the schematic structure is presented in Fig. 2. Here, CPW feeding technique is used which reduces the dispersion losses, so it is suitable for the development of wide-band antennas. The characteristic impedance $\mathbf{Z_0}$ of the CPW using the conformal mapping method has been obtained [13]:

$$Z_{\mathrm{o}} = \frac{30\pi}{\sqrt{\varepsilon_{\mathrm{eff}}}} \frac{K^{'}(k_1)}{K(K_1)} \tag{1}$$

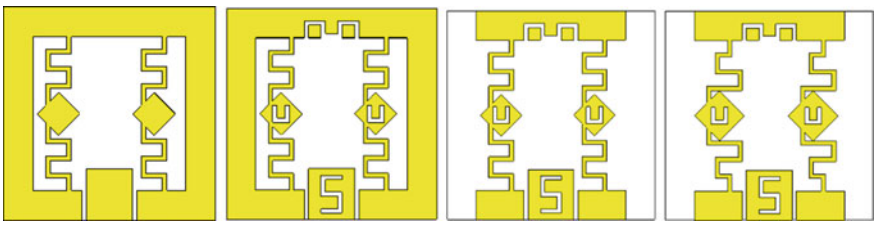
$$\varepsilon_{\mathrm{eff}} = 1 + \frac{\varepsilon_{\mathrm{r}} - 1}{2} \frac{K'(k_1)}{K(k_1)} \frac{K(k_2)}{K'(k_2)} \tag{2}$$

where $K(k)$ and $K^{'}(k)$ represent the complete elliptic integral of the first kind and its complement.

$$k_1 = \frac{W_{\mathrm{f}}}{W_{\mathrm{f}} + 2s} \text{ and } k_2 = \frac{\sinh\left(\frac{\pi W_{\mathrm{f}}}{4h}\right)}{\sinh\left(\frac{\pi (W_{\mathrm{f}}+2s)}{4h}\right)}$$

Table.1 Parameters of the proposed antenna with its dimensions

Parameters	Value	Parameters	Value	Parameters	Value
$L = W$	10	L_{f}	2.4	W_{f}	2.2
L_{m}	1	M_{s}	1.8	W_{m}	0.24
U	1.4	R	1.7	s	0.2



(a) Ant_1 (b) Ant_2 (c) Ant_3 (d) Ant_4

Fig. 1 Design steps of the proposed antenna **a** CPW-fed CRLH antenna **b** Engraved shapes on matching stub, diamond-shaped patch and IDC at the top arm of CPW **c** Slotted right and left arm of CPW-fed antenna **d** Asymmetric meander line-based CRLH antenna

In Ant_1, CPW-fed square-shaped antenna where two symmetric vertical meander lines along with a diamond-shaped patch are grounded. For the meander lines, width (W_m) and the length (L_m) of fingers can be calculated using the following equations [14]:

$$L_m \approx \frac{\lambda_g}{8} \approx \frac{c_0}{8 f_0 \sqrt{\varepsilon_r}} \quad W_m \approx \frac{W_f}{\left(\frac{5N}{3} - \frac{2}{3}\right)}$$

Here $N = 6$, number of fingers.

Here, CPW feeding with matching stub forms a 50 Ω impedance. The simulated $|S_{11}|$ graph of different stages of the proposed antenna is illustrated in Fig. 3. It is visible that, Ant_1 resonates within a band of 24–42.5 GHz with two wide notches of 2.4 GHz (28.9–31.3 GHz) and 5 GHz (35.6–42.6 GHz), without CP. In the next steps of antenna design [Ant_2], different shapes of meander line, like 'S' in matching stub, 'U' in the diamond-shaped patch along with inter digital capacitance (IDC) at upper portion of CPW ground, are introduced. In Ant_3, the left and right arms of CPW ground have been slotted, which gives only a single notch of 1.1 GHz (30.3–31.4 GHz) without CP. In Ant_4, the CP is introduce by transforming symmetric ML to asymmetric MLs. Further to increase the aperture of the antenna, without increasing its dimension, the diamond-shaped patches have been attached with the meander lines, which eliminates the notch and gives complete broadband of 11.7 GHz from (28–39.7 GHz), along with this the ARBW will also be increased widely by joining diamond patches to MLs.

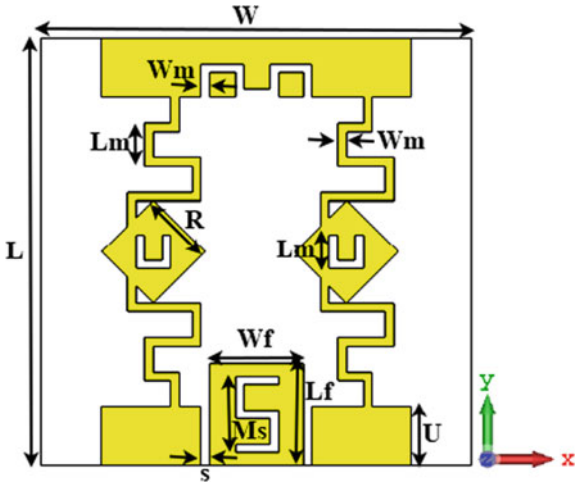


Fig. 2 Structure of the proposed antenna

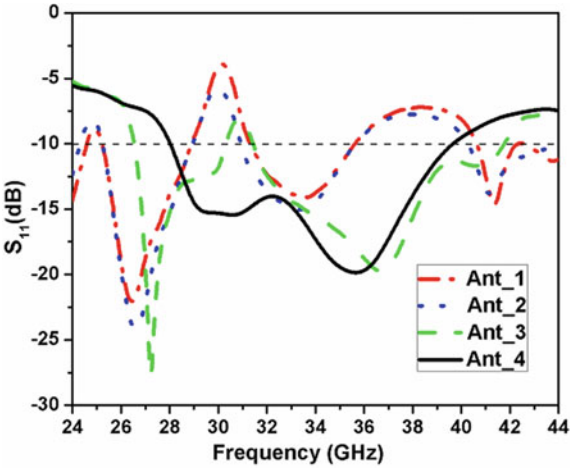


Fig. 3 Simulated S-parameter graph at different stages of antenna design

3 Results and Analysis

The simulated $|S_{11}|$ parameter is shown in Fig. 4, which shows that the proposed structure provides a complete broadband of 11.7 GHz (28 GHz–39.7 GHz). The 3-dB axial ratio plot which signifies the circular polarization is shown in Fig. 5. It is depicted from the figure the ranging from 34.3 GHz to 37.4 GHz, which is of 3.1 GHz wide ARBW has been achieved.

The surface current distribution analysis has been done to discuss the circular polarization mechanism of the antenna at a peak of CP frequency, i.e. 35.7 GHz as shown in Fig. 6. At the different time instants like $\omega t = 0°$, 90°, 180°, 270°, the resultant current vector rotate in anticlockwise direction, gives the right-handed

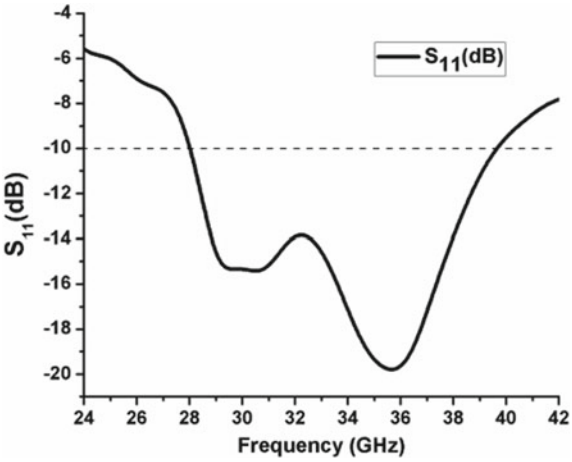


Fig. 4 Simulated $|S_{11}|$ graph of the antenna

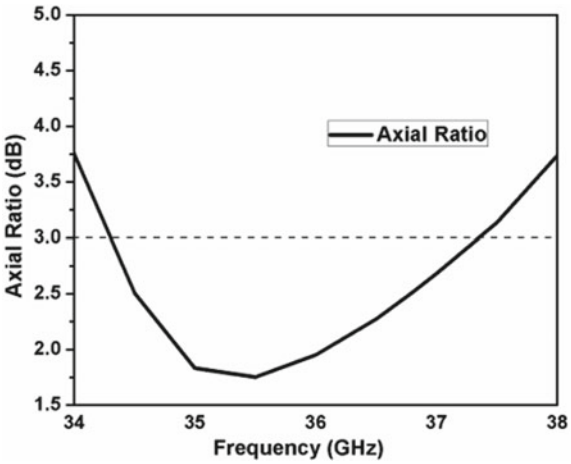


Fig. 5 Axial ratio graph of the antenna

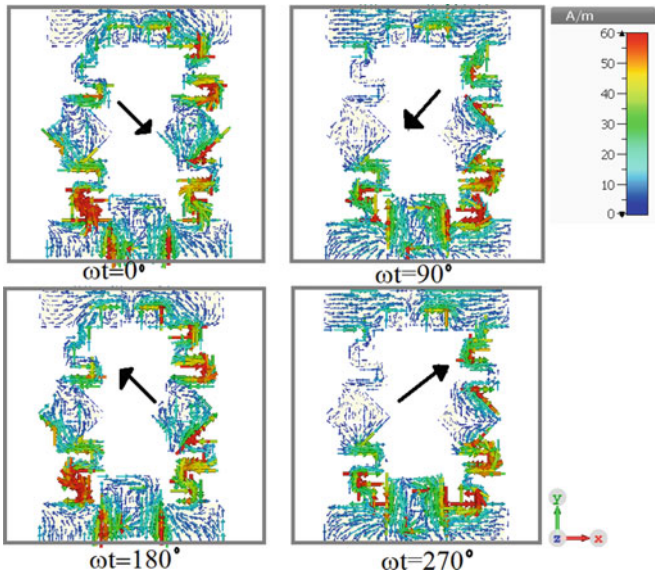


Fig. 6 Simulated distribution of current vectors of proposed antenna at 35.7 GHz

circular polarization (RHCP) in + Z direction. And gives the left-handed circular polarization (LHCP) in − Z direction shown in Figure.

The proposed antenna presents linearly polarized characteristic at 30.7 GHz and circularly polarized characteristics at 35.7 GHz. The 2D normalized radiation pattern of the proposed antenna at 30.7 GHz and 35.7 GHz in *XZ* plane and *YZ* plane is shown in Fig. 7. It is found from Fig. 7(a, b) that at 30.7 GHz, the level of cross polarization is much lower than level of co-polarization. It is found from Fig. 7(c, d) that, at

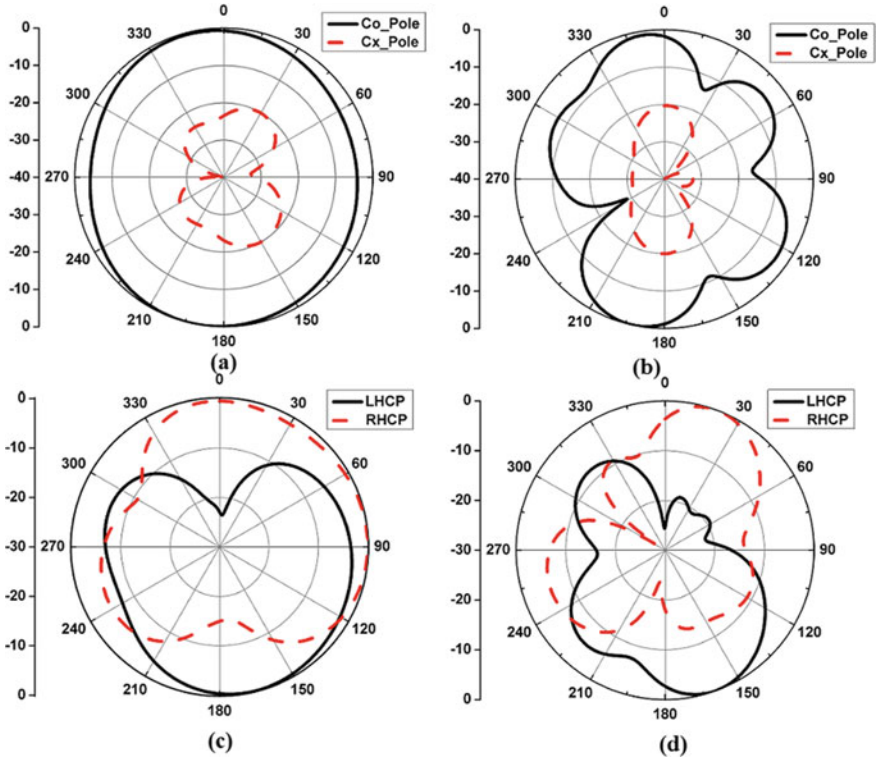


Fig. 7 Simulated radiation patterns of proposed antenna at **a** 30.7 GHz in *XZ* plane **b** 30.7 GHz in *YZ* plane **c** 35.7 GHz in *XZ* plane **d** 35.7 GHz in *YZ* plane

35.7 GHz, the antenna shows the RHCP radiation in +Z direction and LHCP in − Z direction in both (XZ and YZ) plane. The simulated gain over the frequency plot is shown in Fig. 8, which depicts the maximum gain of 5.7 dBi, and it varies in the complete range from 26 to 42 GHz.

The radiation efficiency over the frequency plot of this antenna is illustrated in Fig. 9, which shows that the efficiency of the antenna is always greater than 80% in the entire range. It depicts that the proposed CP antenna works efficiently in compete band. Table 2 shows the comparison of the proposed antenna with previously published work on the 5G millimeter-wave antenna.

4 Conclusion

A low profile, broadband, and the circularly polarized antenna is designed and analyzed in this paper. The compact size antenna is achieved using CRLH-TL based

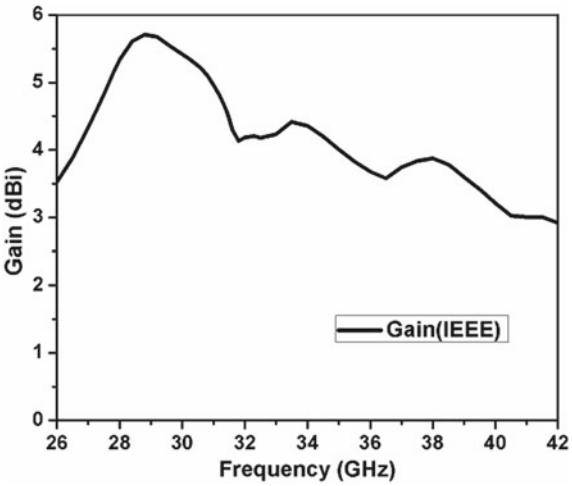


Fig. 8 Simulated gain plot

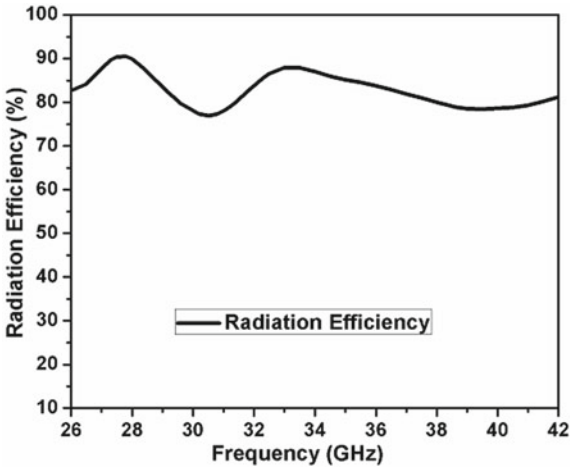


Fig. 9 Radiation efficiency plot

metamaterial unit cells, IDC and by placing meander lines of different shapes. Broadband characteristics of antenna have been achieved by applying the CPW feeding method and by attaching diamond-shaped CRLH unit cells to vertical meander lines. Circular polarization has been achieved through asymmetric vertical meander lines. This antenna exhibit 11.7 GHz wide impedance bandwidth ranging from 28 to 39.7 GHz with fractional bandwidth (FBW) of 34.6%. Axial ratio bandwidth of 3.1 GHz wide, ranging from 34.3 to 37.4 GHz with 8.7%. The radiation pattern was studied at two different frequencies 30.7 and 35.7 GHz in *XZ* and *YZ* plane. The antenna exhibits a maximum gain of 5.7 dBi and more than 80% efficiency in the entire band. The proposed structure can be the good candidate for 5G millimeter-wave communication.

Table.2 Comparison of the proposed antenna with previously published mm-wave antenna

Ref. No.	Resonating band (GHz)	Bandwidth (GHz)	Polarization	AR bandwidth (GHz)	Number of layers	Size (mm^3)
[10]	24.5 – 31	6.5	Circular	4.6	2	12.4 × 12.4 × 0.51
[15]	23.41–33.92	10.51	Linear	–	3	37.6 × 14.3 × 0.25
[16]	27–30	3	Linear	–	3	31 × 31 × 0.51
[17]	27.58–28.64, 37.21–38.64	1.06, 1.43	Linear	–	3	55 × 110 × 0.508
[18]	24–34.1	10.1	Circular	5.3	5	12 × 12 × 1.02
Proposed	**28–39.7**	**11.7**	**Circular**	**3.1**	**2**	**10 × 10 × 0.51**

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Early Detection of Breast Tumor Using Antenna

T. A. Karthikeyan and M. Nesasudha

1 Introduction

The outermost covering part of the body is a skin, and it protects us against heat, light, injury and contamination. It directs internal heat level and stores water, fat and nutrient D. The skin weighs around 6 pounds, and is the biggest organ of body. The skin has three layers, epidermis, dermis and hypodermis. The external layer of the skin is called as epidermis. The capacity of the epidermis is to go about as a natural and physical obstruction to the outside condition, and forestall entrance by aggravations and allergens. And furthermore, it forestalls the loss of water and keeps up interior homeostasis. There are various sorts of tumors, and they are carcinoma, sarcoma, melanoma, lymphoma and leukemia. Carcinoma is the most normally analyzed tumors that begin in the skin, lungs, bosoms, pancreas, different organs and glands. Breast cancer influences numerous ladies and is a dangerous cell development in the bosom. Whenever left untreated, it spreads to different parts of the body. Early analysis is the most significant boundary to identify and meddle with malignancy tissue. There are numerous strategies to recognize bosom malignancy (Fig. 1).

The dermis is considered as the "center" of the integumentary framework. It contains blood and lymph vessels, nerves and different structures. The hypodermis is a layer straightforwardly beneath the dermis and serves to interface the skin to the basic tissue of the bones and muscles. The radio wire structure as a square fix recieving wire is utilized to distinguish tumor tissue in the bosom structure. Thus, a straightforward 3D bosom structure is displayed to characterize harmful tissue.

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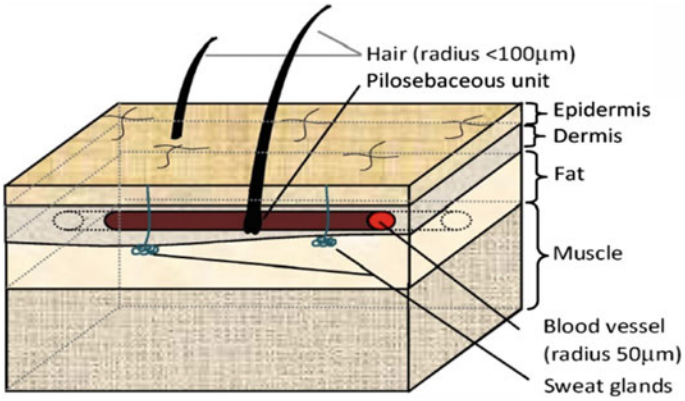

Fig. 1 The layers of skin

The reproduction work is actualized utilizing CST software. Better performance is achieved by changing the ground plane of the microstrip antenna. The designed antenna structure working at 2.4 GHz is kept under bosom skin. The analysis is based on current distribution which is carried out to detect the presence of tumor. Different current density analysis with and without breast tumer is presented [3]. The researchers have proposed that the maximum current density will be present at the place of tumor [8]. The FCC recommended SAR value should be less than 1.6 W/Kg for 1 G tissue [10].

2 Antenna Design

In this work, a square patch antenna is designed. The substrate used is FR4. Figure 2 shows the structure of antenna and Table 1 represents design parameters. The square shaped ground plane is created with copper material of 0.035-mm height, the length and width of the ground is 56.9 mm and 56.9 mm, respectively. Next, a substrate is designed using FR4 (Flame Retardant 4) material composed of woven fiber glass with epoxy resin, and it is a zero water absorption which is used as insulator [4].

Fig. 2 Structure of antenna

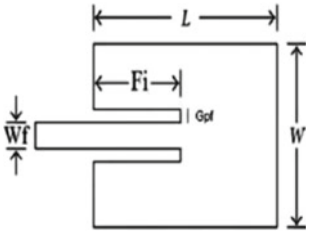

Table 1 Design parameters of the antenna

S. No	Parameters	Measurement (mm)
1	Width of antenna W	28.45
2	Length of antenna L	28.45
3	Length of feed line F_{i}	9
4	Width of micro strip feed line W_{f}	1.137
5	Gap between patch and insert feed G_{pf}	1
6	Length of ground L_{g}	56.9
7	Width of ground W_{g}	56.9
8	Height of conductor Ht	0.035
9	Height of dielectric substrate	1.6

The rectangular patch is created using copper material of thickness 0.035 mm with the length and width as 28.45 mm. The feedline is inserted. The feedline is used to connect antenna with radio transmitter or receiver, and then the port is inserted.

The equations from 1 to 8 represent the formulas used to calculate different antenna parameters like width and length. Where as the height of the conductor (ht) is fixed at 0.035 mm. The gap between patch and inset fed (G_{pf}) is usually 1 mm and the input impedance is 50 Ω, and the velocity of the light is $C = 3 * 10^8$ m/s.

$$W = \frac{C}{2f\sqrt{\frac{(\in r+1)}{2}}} \tag{1}$$

$$\in r_{\mathrm{eff}} = \frac{\in r+1}{2} + \frac{\in r-1}{2}\left(1 + 12\frac{h}{W}\right)^{-\frac{1}{2}} \tag{2}$$

$$L_{\mathrm{eff}} = \frac{c}{2f\sqrt{\in r_{\mathrm{eff}}}} \tag{3}$$

$$\Delta L = 0.412h\frac{(\in r_{\mathrm{eff}} + 0.3)\left(\frac{W}{h} + 0.264\right)}{(\in r_{\mathrm{eff}} - 0.258)\left(\frac{W}{h} - 0.8\right)} \tag{4}$$

$$L = L_{\mathrm{eff}} - 2\Delta L \tag{5}$$

$$L_{\mathrm{g}} = 2 * L \tag{6}$$

$$W_{\mathrm{s}} = 2 * W \tag{7}$$

$$Fi = \frac{6h}{2} \tag{8}$$

Usually, the designed antenna will be places over human phantom model [2]. Figure 3 shows the placement of antenna under breast phantom model. The breast phantom layer is designed as shown in Fig. 4.

The breast phantom model is designed in the same way as that of antenna design but the materials used is different [1]. Table 2 represents the different dielectric and conductive parameters of different tissue parameters.

The layers of breast tissue are selected as SKIN, FAT and TUMOR [5]. These layers are created taking different values of the permittivity, electrical conductance and density. The breast phantom is spherical in strucuture, and the tumor layer is placed in side these layers. These three layers of breast phantom are deigned in the way that outer most layer is skin, then the fat layer is placed inside that and finally tumor layer is inserted. These phantom look like spherical shape.

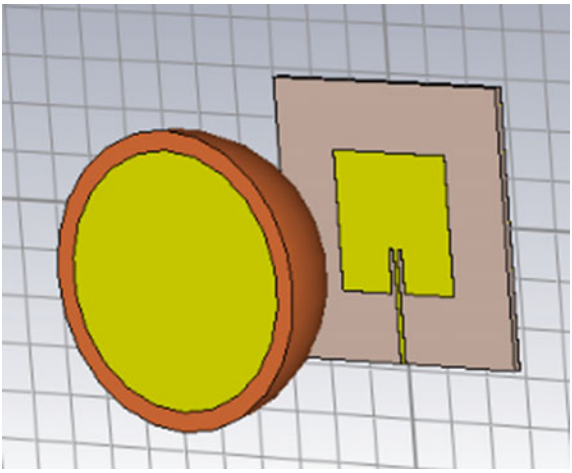

Fig. 3 Antenna and breast phantom

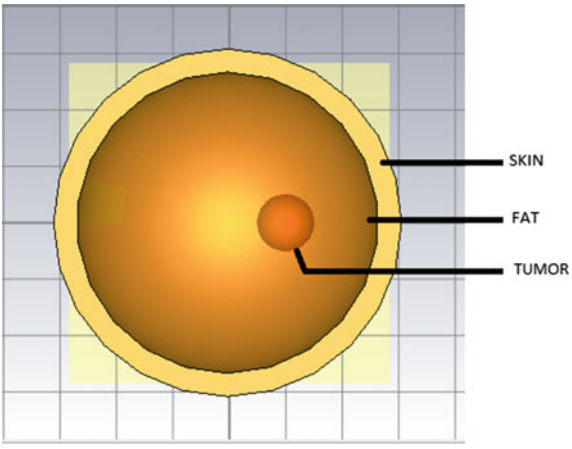

Fig. 4 Stucture of breast phantom

Table 2 Measurement for different parameters for breast phantom model

S. No	Tissue	Permittivity (F/m)	Electrical conductance (S/m)	Density (Kg/m^2)
1	Skin	36.7	2.34	1109
2	Fat	4.84	0.262	911
3	Tumor	54.9	4	1058

3 Simulation and Results

Figure 5 shows the return loss of the designed antenna. The antenna is designed for the frequency of 2.4 Ghz of ISM band. The return loss or reflection coefficient S11 parameter tells the amount of power reflected from the antenna. As shown in Fig. 5, the return loss is − 25 dB at 2.4 GHz, which is acceptable.

Voltage standing wave ratio (VSWR) is the ratio between maximum voltage and minimum voltage in a standing wave. VSWR is the measure of how much power is transmitted from the source to the load through the transmission line. The expected value of VSWR is less than 2 (Between 1 and 2). Figure 6 shows the obtained VSWR of 1.041 at 2.4 Ghz for the designed antenna.

The ratio between the total power transmitted and power accepted by the antenna is called as radiation efficiency. The antenna radiation efficiency can be measured using anechoic chamber and Fig. 10 shows the radiation pattern. Figure 7 shows the radiation efficiency of 22% the designed antenna. Inorder to improve the efficiency, some metameterial structures can be adopted.

The current density is the quantity of charge per unit time that move through a unit area of a selected cross section. The area need to be computed is flat or curved, real or imaginary, either a cross-sectional area or a surface. Like, for charge carriers going through an electrical conductor, the territory is the cross section of the conductor, at

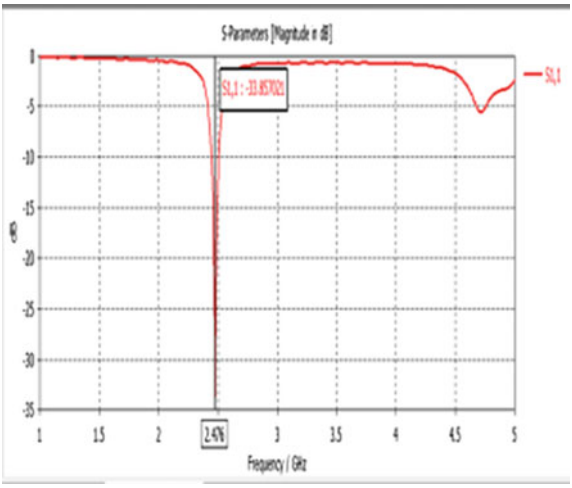

Fig. 5 Reflection coefficient simulated results

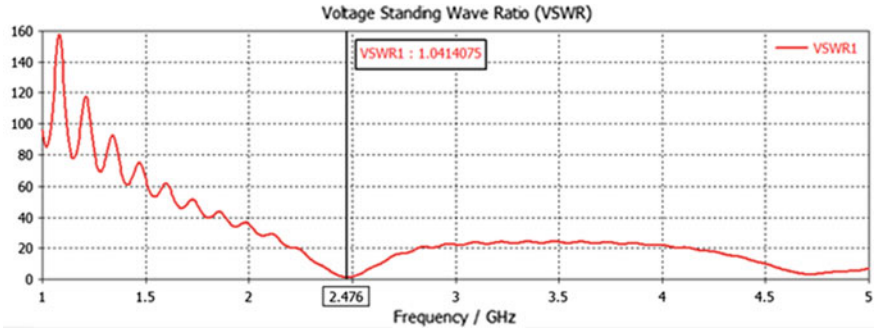

Fig. 6 VSWR

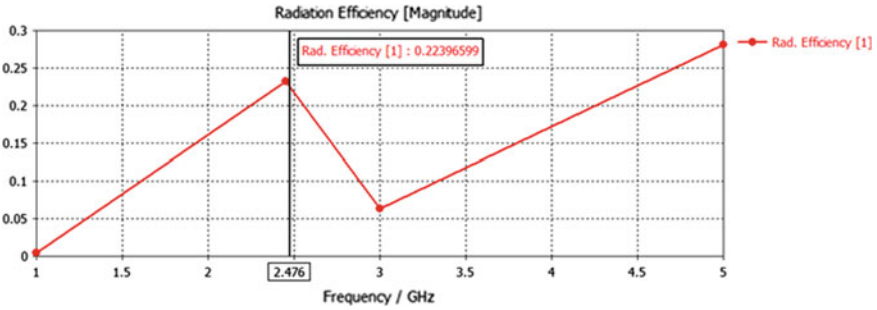

Fig. 7 Radiation efficiency

the area considered. Figure 8 shows the breast phantom with tumor and the current density output.

The current density is 169.815 A/m^2 for breast phantom with tumor and then the current density is calculated for breast phantom without tumor. Figures 9 and 10 show the current density output.

Specific absorption rate (SAR) is to compute the rate at which energy is absorbed by the human body. It is measured in W/kg. The SAR values are normally taken either from 1 g of skin tissue or 10 g of skin tissue. As per FCC, the recommended SAR value to be used in India is 1.6 W/kg for 1 g tissue (Table 3).

As far as possible, the FCC limit for open exposure from cell phones is a SAR level of 1.6 W/kg [9]. SAR values rise as the conductivities of human body tissues increase and drop as the increase in relative permittivities of human body tissues increase.

The simulated results of breast tissue with tumor and without tumor are shown in Table 4. It discusses about the relation between electric field, magnetic field and current density. From this table, it is infered that current density is more with tumor. The illustrations are evaluated to distinguish tumor.

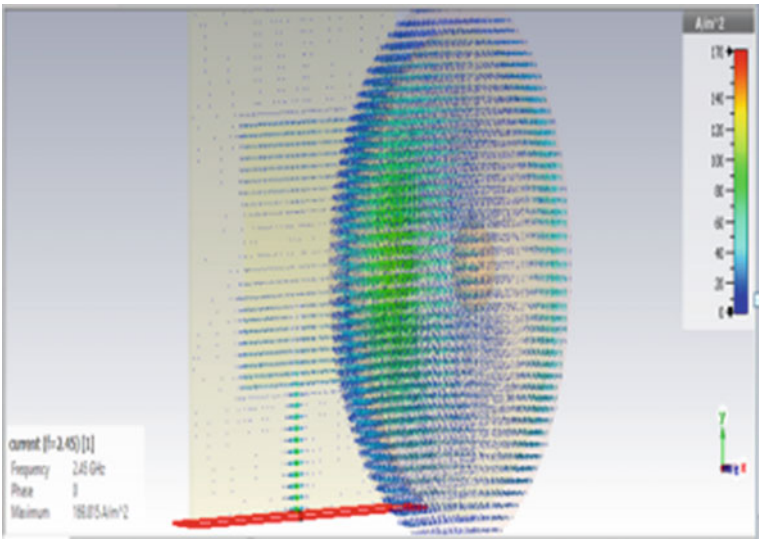

Fig. 8 Breast phantom with tumor and the current density output

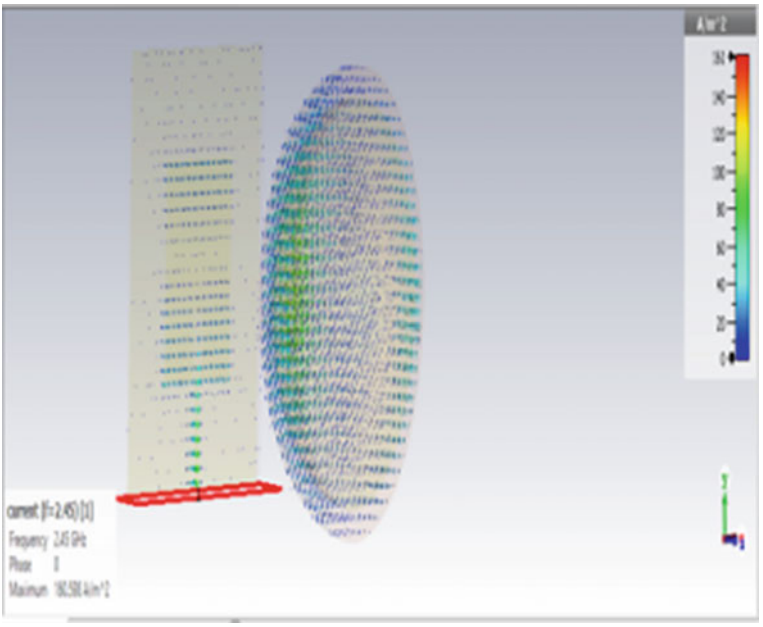

Fig. 9 Current density in breast phantom without tumor

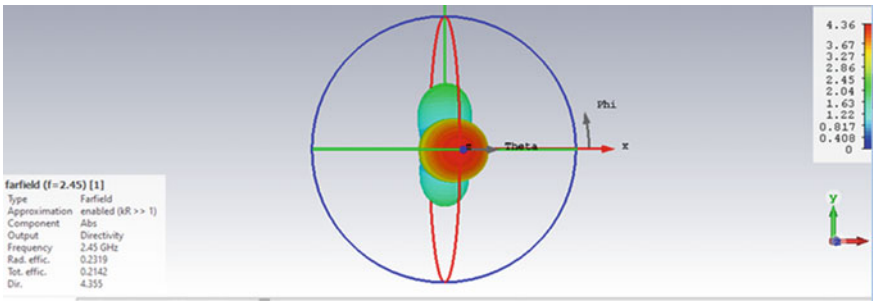

Fig. 10 Radiation pattern

Table 3 SAR calculation

Maximum SAR (1 g) (W/kg)	1.00307
Maximum at (x, y, z) (mm)	−0.20425, 0.25, 40.2057
Avg.vol.min (x, y, z) (mm)	−5.3377, −4.80345, 40
Avg.vol.max (x, y, z) (mm)	4.7692, 5.30345, 50.1049
Largest valid cube (mm)	10.4501
Smallest valid cube (mm)	10.0417
Avg. Vol. accuracy (%)	0.0001

Table. 4 Comparision of current density with tumor and without tumor

Breast phantom	Current density (A/m^2)	e-field (V/m)	H-field (A/m)
With tumor	169.815	17,890.2	55.4217
Without tumor	160.598	16,242.8	55.8628

The analysis of phantom model in terms of current desity in e-field, H-field and current density with tumor and without tumor is tabulated in Table 4. These changes of values infer the presence of tumor.

4 Conclusion

This research work dealt with the disign of a square patch antenna structure which is used for early detection of breast tumor. The antenna is working at 2.4 GHz. The designed antenna is placed over the breast phantom model. The specific absorption rate (SAR) of antenna at 1G tissue is analysed. The obtained SAR value is 1 W/kg, which is less than the FCC recommended value of 1.6 W/kg. The electric field of 17,890.2 V/m, magnetic field of 55.4217 A/m and current density of 169.815 A/m^2 are obtained with tumor. Where as the values obtained for curent density, electric field

and magnetic fields are 16,242.8 V/m, 55.8628A/m and 160.598A/$m^{2,}$ respectively. From these analysis, it is easy to detect the presence of breast tumor in the early stage itself.

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Localized Tamper Detection in Digital Images Using Three Phase Reversible Watermarking

Praneesh Gupta and Jeebananda Panda

1 Introduction

Tampering in digital image during transmission can occur due to different types of unintentional and intentional attacks that may affect complete or part of the image. The integrity and source authentication of digital images can be ensured by means of fragile digital watermarking which embeds a checksum data in an image [1, 2], but the host image is modified permanently. To overcome this, reversible digital watermarking which is in general fragile in nature and permits lossless recovery of image can be employed for providing authentication and integrity verification of the sensitive data in applications like military imaging, forensics industries, and healthcare industries where the cover image is extremely important [3, 4]. If integrity of the whole cover image is used as a watermark, then integrity failure leads to rejection and retransmission of complete image. Instead, if the tampered areas are localized in the received image, then.

- In case the corruption occurs in some region of non-interest (RONI) then the received image will be accepted without request of retransmission.
- In other scenario, where some regions of interest (ROI) are corrupted then only that regions will be retransmitted, resulting in saving of the channel bandwidth.

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In this paper, we present an application of three phase reversible watermarking scheme [3] for the purpose of localized tamper detection in grayscale digital images. We choose three phase reversible watermarking as it provides significant performance in terms of embedding capacity and PSNR. This application allows the authentic receiver to detect the tampered blocks in the received image and lossless recovery of intact blocks.

Most of the localized tamper detection schemes proposed in the literature do not take the type of image modifications with the intension of forgery. We incorporate measures to mitigate this type of threat and highlight ways to choose optimal block size and integrity check algorithm for faithful operation. A brief discussion on the schemes proposed in the literature appears in the next section, whereas Sect. 3 describes the proposed methodology of localized tamper detection process in detail. Section 4 deals with experimental results and analysis. Conclusions are made in Sect. 5.

2 Literature Review

Tamper detection and authentication in digital images can be achieved through digital signature and digital watermarking [5]. Digital signature-based methods provide tamper detection but in general does not localize the tampered regions in received image. Karsh et al. [6, 7] proposed schemes robust against some content preserving operations in transmitted image that generates image hash using global, local, and scaling feature vectors. The calculated image hash is transmitted along with the image for authentication and localization of tampered areas. Localization of tampered areas based on fragile watermarking was first introduced by Walton [8], where the image is divided into blocks and the checksum of respective block is embedded in the LSBs of pixels within block but it produces irreversible modifications in the host image. Lo et al. [9] and Gao et al. [10] presented tamper detection and authentication for digital images employing reversible watermarking algorithm. Based on the concept of ROI and RONI regions in medical images, tamper detection and recovery for medical images were presented in [11, 12]. The authentication and parity bits along with the intensity information are embedded in LSBs of ROI sub-blocks and for lossless recovery of ROI, LSBs will be saved in RONI regions. Naskar et al. [13] generalize the process for tamper detection and localization in digital images using reversible watermarking schemes. They discuss a lower bound on minimum block size based on hash length and size of overhead and propose merging of four adjacent blocks when the embedding capacity is not sufficient. The scheme does not provide protection against block copy and move type of attack and produces more falsely rejected blocks when more merged blocks were tampered. Malayil et al. [14] introduce authentication of medical images using reversible watermarking, which ensures that the tamper detection can be done efficiently even when the watermarked image is subjected to image processing operations. Gao et al. [15] present a localized

reversible authentication with approximate recovery of tampered regions based on prediction error expansion and compressed sensing.

3 Methodology of Localized Tamper Detection

This section presents details of embedding and localized tamper detection process in grayscale images, which is based on the scheme presented in [13].

3.1 Embedding Process

The watermark embedding process for the purpose of localized tamper detection is illustrated in Fig. 1; detail of each block is described in following steps.

Step 1 *Partition of Cover Image into Blocks:* The cover image is partitioned into equal sized non-overlapping blocks with $n_1 \times n_2$ pixels such that the entire image is covered.

Step 2 *Generation of Watermark*: The blocks are raster scanned, and for each block, the integrity value is calculated using suitable integrity check algorithm depending on embedding capacity, channel conditions, and attack scenario.

Step 3 *Reversible Watermark Embedding*: For embedding of the integrity value, each block is divided into four types of pixels, viz. base (indicated by 0's in Fig. 2) and three phase candidate pixels (indicated by 1, 2, and 3's in Fig. 2) as described in [3, 4].

Base pixels remains intact in watermarked image while other candidate pixels are predicted based on median of the original neighboring context pixels. The prediction errors (say e) between the candidate and corresponding predicted value is given as,

$$e(i, j) = P(i, j) - P_{pred}(i, j) \tag{1}$$

Embedding is done phase wise and only errors that lie within some threshold limit (say k_1 and k_2) are utilized to embed the watermark bit $w \in \{0, 1\}$. The modified prediction error e_{mod} and marked pixel P_{wat} are given by Eqs. (2) and (3) [16].

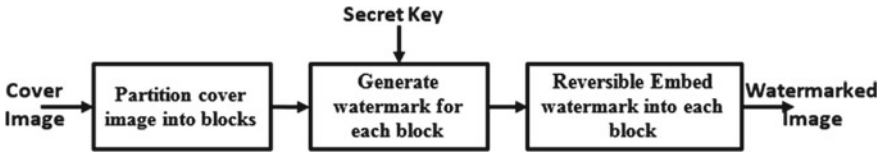
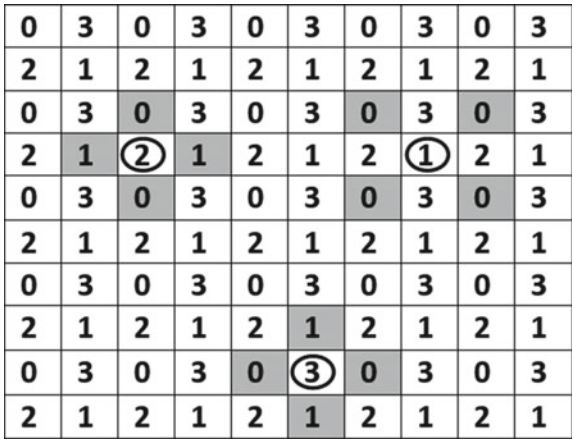


Fig. 1 Watermarking embedding process

Fig. 2 Base and three phase candidate pixel positions in grayscale image



$$e_{mod}(i,j) = \begin{cases} 2e(i,j) + w & \text{if } e(i,j) \in [-k_1, k_2] \\ e(i,j) + k_2 + 1 & \text{if } e(i,j) > k_2 \\ e(i,j) - k_1 & \text{if } e(i,j) < -k_1 \end{cases} \tag{2}$$

$$P_{wat}(i,j) = e_{mod}(i,j) + P_{pred}(i,j) \tag{3}$$

For blind extraction, the side information k_1, k_2 and location map (to handle over/underflow) are inserted into 1st phase LSB's. To handle, the blocks whose embedding capacity (EC) are not sufficient, the current block and the next block are combined together (say, B_{comb}) and the integrity value of the combined block is embedded in B_{comb}. Also, to facilitate the receiver, an indicator '0' or '1' for normal/combined block is appended in the side information [13]. The effective watermark and side information is given by (4) and (5).

$$\text{Watermark} = \text{H} \| \text{LSB}'\text{s of 1st Phase Pixels(used for side information)} \tag{4}$$

$$\text{Side Info} = \text{indicator bit} \,||k_1||k_2|||| \text{location map size} || \text{ location map} \tag{5}$$

where H represents the computed hash value considering block number B along with the pixels within the block, i.e., $H = hash(B||\text{Block } B \text{ pixels})$.

3.2 Extraction, Recovery and Tamper Detection

The localized tamper detection process at the receiver side is illustrated in Fig. 3, detail of each block is described in following steps.

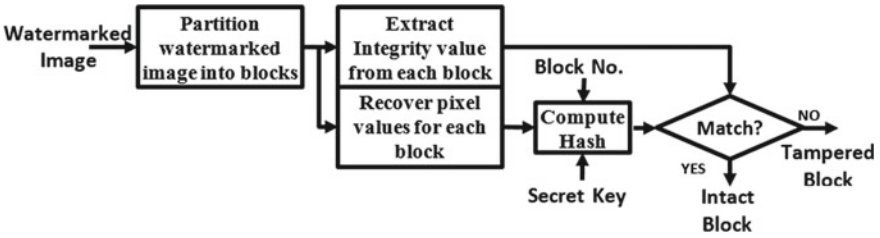


Fig. 3 Localized tamper detection process

Step 1 *Partition of Watermarked Image into Blocks*: The watermarked image is partitioned into non-overlapping blocks of size $n_1 \times n_2$.

Step 2 *Extraction and Pixel Recovery:* The block pixels are categorized into four types as described in Sect. 3.1. The extraction process is carried out phase wise so that the prediction context consists of original pixels, and hence, we get same predicted values. After computing the expanded error (Eq. (6)), with the help of thresholds and location map; the watermark bit, actual error and finally the original pixel is obtained using Eqs. (7), (8), and (9) [16].

$$e_{mod}(i, j) = P_{wat}(i, j) - P_{pred}(i, j) \tag{6}$$

$$w = e_{mod}(i, j) \text{mod} 2, \text{ if } e_{mod}(i, j) \in [-2k_1, 2k_2 + 1] \tag{7}$$

$$e(i, j) = \begin{cases} (e_{mod}(i, j) - w)/2 & if \ e_{mod}(i, j) \in [-2k_1, 2k_2 + 1] \\ e_{mod}(i, j) - k_2 - 1 & if \quad e_{mod}(i, j) > 2k_2 + 1 \\ e_{mod}(i, j) + k_1 & if \quad e_{mod}(i, j) < -2k_1 \end{cases} \tag{8}$$

$$P(i, j) = P_{pred}(i, j) + e(i, j) \tag{9}$$

Step 3 *Tamper Detection*: For each block, after extraction of watermark and restoration of pixels, the integrity value of the restored pixels along with corresponding block number is computed. If the computed value is not identical with the extracted integrity value, then that block is declared as tampered. Pseudocode for localized tamper detection process is mentioned in Algorithm 1.

ALGORITHM-1: EXTRACTION, RECOVERY & TAMPER DETECTION

Input: Marked Image P_{wat}, Block Size (n_1, n_2), Integrity Algo $(Hash)$, Secret Key (K)
Output: Tampered Blocks (B_T), Restored Image (P_{recov})

Partition watermarked image into Blocks of size $n_1 \times n_2$
$i \leftarrow 1$ *and* $B \leftarrow 1$ // Block Number
While $(B \leq \#\, Blocks)$ **do**
  Extract *Indicator* bit from LSB of 1st phase pixel
  if (*indicator = 0*) **then**
    Extract side information $//k_1, k_2$ and location map
    Extract Hash (H) and restore pixels of block B
    Compute $H_{comp} \leftarrow Hash\,(B \,||\, Restored\ block\ B, K)$
    if $(H = H_{comp})$ **then** Authenticate and accept block B
    else $B_T\,(i++) \leftarrow B$ //Block B is Tampered
    endif
    $B \leftarrow B + 1$
  endif
  if $(indicator = 1)$ **then**
    $Bcomb \leftarrow Block\ B \,||\, Block\ (B+1)$ //Combine current and next block
    Extract side information $//k_1, k_2$ and location map
    Extract Hash (H) and restore pixels of block B_{comb}
    Compute $H_{comp} \leftarrow Hash\,(B \,||\, Restored\ Block\ B_{comb}, K)$
    if $(H = H_{comp})$ **then** Authenticate and accept block B_{comb}
    else $B_T\,(i++) \leftarrow B$
      $B_T\,(i++) \leftarrow B + 1$ //Blocks B & $(B+1)$ are Tampered
    endif
    $B \leftarrow B + 2$
  endif
end while
$P_{recov} \leftarrow Combine\ all\ restored\ blocks\ in\ their\ respective\ location$
RETURN P_{recov} and B_T

3.3 Selection of Integrity Check Algorithm

Framework for selection of integrity check algorithm based on various types of corruption and attack scenario is given below.

- For detecting random and unintentional corruption during transmission, simple checksums such as additive, CRC, etc., can be used as the integrity check algorithm. Since length of integrity value for these algorithms are relatively small, we can use smaller sized blocks.

- To detect intentional corruption in image, cryptographic hash function (MD5, RIPEMD, SHA, etc.) [17] can be used to generate integrity value. It has a property of collision resistance and single bit corruption will drastically change the hash. Here, we assume that the attacker does not modify the integrity value.
- To protect against forgery where the attacker can modify both the block pixels and the embedded checksum, message authentication code (e.g., HMAC) can be used. It requires a pre-shared secret key along with cryptographic hash function for computation of integrity value. HMAC is computed for the given data using Eq. (10) [17].

$$\text{HMAC(data}, K) = \text{Hash}\left((K_0 \oplus \text{opad}) || \text{Hash}\left((K_0 \oplus \text{ipad}) || \text{data}\right)\right) \quad (10)$$

where K_0 represents processed secret key K, ipad is 0x36 replicated B_H (block size in Hash) times and opad is 0x5C replicated B_H times.

- To provide detection of block copy and move attack in image we prefix block number to the block pixels before computing integrity value. Note that the use of cryptographic hash function or MAC for integrity computation provides detection of any watermark attacks such as image processing attacks, geometric attacks, etc., in the marked image, as even one-bit modification in a block will bring about a drastic change (around 50%) in the integrity value.

4 Experimental Results and Analysis

The algorithm for localized tamper detection in digital images using three phase reversible watermarking scheme was simulated in MATLAB for validation and performance analysis. The effectiveness of the algorithm was tested on some standard test images. For experimentation purpose, HMAC-SHA1 with key size 256 bits and digest size 160 bits is chosen for integrity. To enable faithful embedding, we target to minimize the number of combined blocks (say less than 10) where embedding capacity goes below the size of watermark. Experimentally, we determined that the block size 32×32 is optimal for this purpose. Therefore we fix block size 32×32 for further experimentation and thresholds $k_1 \& k_2$ are taken in the range [0,10]. The embedding results for different test images in terms of number of unit blocks, combined blocks, PSNR, and SSIM index values are given in Table below. The results demonstrate that only few number of blocks are combined for HMAC-SHA1, also the watermarked image has PSNR value greater than 35 dB and the SSIM index is greater than 98% thus the structural information is preserved in watermarked image, and the existence of watermark is not perceived visually.

The performance of the algorithm is also analyzed for various types of attacks and corruption in marked image. The results in Fig. 4 demonstrate its effectiveness. Further, the scheme is compared with the generalized tamper localization scheme [13] employing state-of-the-art schemes [18–21] in terms of combined blocks and maximum possible false rejection rate (FRR) (Tables 1 and 2).

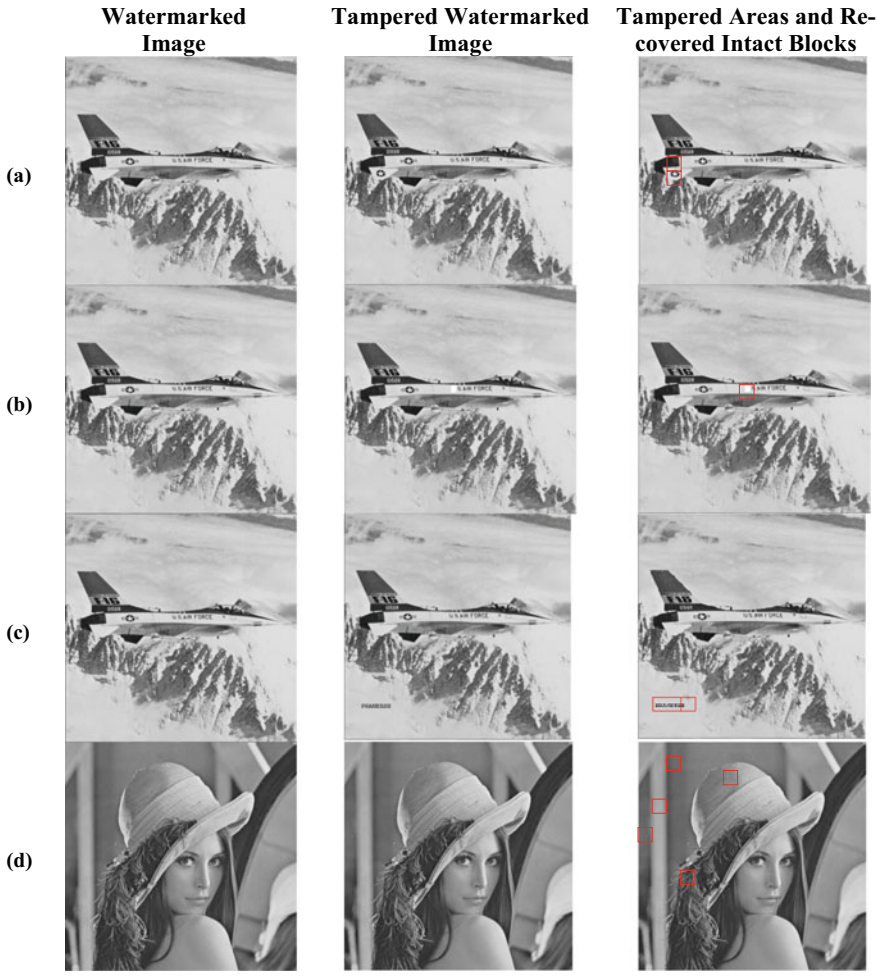


Fig. 4 Performance analysis of localized tamper detection. **a** Copy-move attack, **b** Crop attack **c** Copy-paste attack, **c** Random corruption

$$\text{FRR} = \frac{\text{Number of false rejected blocks}}{\text{Total of Number of Blocks}} \tag{11}$$

5 Conclusion

In this paper, an application of three phase reversible scheme for detecting tamper regions in the received grayscale digital image is presented. Localization of tampered regions at the receiver side is achieved by dividing the image into small blocks

Table 1 Embedding results for localized tamper detection

Test image	Size	No. of 32 × 32 size blocks	No. of combined blocks	PSNR (dB)	SSIM index
Lena	512 × 512	256	0	48.154393	0.994429
Boat	512 × 512	256	0	43.972021	0.989381
Baboon	512 × 512	238	9	35.859162	0.985730
Tank	512 × 512	254	1	44.693777	0.989163
Airplane	512 × 512	256	0	48.458800	0.995571
Goldhill	512 × 512	256	0	43.980430	0.990840
Peppers	512 × 512	254	1	46.050851	0.990521

Table 2 Performance comparison in terms of FRR (%)

Test image	Maximum possible FRR (%)				
	Proposed	Scheme [13] with Hu et. al.'s algorithm	Scheme [13] with Yang et. al.'s algorithm	Scheme [13] with Luo et. al.'s algorithm	Scheme [13] with Celik's et. al.'s algorithm
Lena	0	1.1719	5.8594	2.3438	7.0313
Baboon	3.5156	10.5469	10.5469	4.6875	11.7188
Airplane	0	0	3.5156	0	2.3438
Goldhill	0	0	5.8594	1.1719	4.6875

and embedding the integrity value, which is computed by considering entire within block pixels along with block number. The scheme allows combining of current and next block dynamically, when the capacity of the block is not sufficient and an indicator bit is inserted in the image to facilitate the receiver. In addition, considering block number during integrity calculation provides detection against block copy and move type of attack. The experimental results show that for most of the test images number of blocks combined are relatively small with high PSNR and SSIM value of watermarked image. Also, results for different types of attacks on watermarked image demonstrates the effectiveness of the localized tamper detection scheme. Comparison results with generalized method for tamper localization employing various reversible schemes demonstrate the advantages of the scheme in terms of false rejection rate.

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Analysis of Nano Opto-Mechanical Tuning of Photonic Crystal Waveguide-Based Device for Pressure Sensing

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1 Introduction

Micro-opto-electro-mechanical-system (MOEMS) devices are based on the integration of photonics and micromachining process on VLSI technology, and it has immense potential to provide wide range of tunable photonics devices [1, 2]. The suspended silicon structures have already demonstrated miniaturized photonic devices like switches, resonators to fulfill the demand of high-speed data rate for different Internet of things (IoT) applications [3]; however, the photonic crystal waveguide (PCW) structures integrated with the MOEMS technology are less investigated for the applications ranging from the presence of different aptamers in liquid phase atmospheres [4, 5] and nano-sensing. Conventionally, the devices like Mach-Zhender interferometers and directional couplers are used for sensing structures [6, 7]; however, the PCW structures have the capacity to fulfill the demand of highly selective and sensitive devices. The deflection in the suspended photonic crystal waveguide is either sensed by capacitive or optical methods. However, the measurement of deflection is less sensitive in the capacitive detection while the photonics approaches are more accurate and provides high selectivity [8, 9]. The nano-scale periodic structure is integrated as a suspended flexible platform to form a tunable sensing device for photonic applications.

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Photonic crystal are engineered artificial nanostructures and capable of controlling and manipulating the propagation of electro-magnetic waves within a certain range of frequency [10]. Photonic band-gap structures are assembled by arranging alternating materials with different dielectric constants to produce a desired effective band-gap [9, 10]. Photons within a certain energy range cannot be allowed to propagate within the band-gap of the structure. This property has made these structures useful for many applications such as strain sensing applications [11–13]. Photonic crystal has also shown its potential in providing different advantages like high power confinement, unique band-gap effect and guided modes in waveguide region. In recent decade, a lot of efforts are made with the integration of various nano-photonics devices based on different defect in waveguide structures like line defect for channel drop-structures and point defects for micro-ring resonators to perform different operations in highly re-configurable optical devices [14–16]. The operating principle is governed by the measurement of change in effective refractive index to the applied excitation provided in the device [17, 18].

In this work, the photonic crystal waveguide-based nano-cavity is integrated on flexible platform for sensing applications. A suspended structure comprises of PCW nano-cavity is proposed to perform the opto-mechanical tuning of device. The waveguide is considered on silicon slab and the analysis of electro-magnetic field is performed for applying different pressure in the device. The output parameters are obtained in the suspended nano-cavity based on photonic crystal waveguide.

2 Principle of Operation

The band gap in the photonic crystal (PC) can be tuned by introducing the defect in the nano-structure. In the device, the PC structure is composed as an array of air holes in the silicon slab, arranged in triangular lattice with the radius of holes (r) as 168 nm and lattice constant (a) as 482 nm. The suspended photonic crystal waveguide is designed by patterning a plate on the buffer layer for providing pressure between suspended PCW and pad present in the configuration of the device. The deep UV photolithography is to be performed for designing suspended PCW on silicon-on-insulator substrate. The suspended PCW structure is free at one end, while the other part is fixed in the device. The suspended silicon slab made of photonic crystal waveguide has a young modulus of 153 GPa and Poisson ratio of 0.23. When a pressure is not applied between the pad and the PCW, the device structure inhibits in its initial state, and the signal directly transmits at the output port with the circular ring defect so as to have transverse electric (TE) like propagation inside the core. Based on the configuration of device, when the suspended PCW is under the applied pressure, the strain is appeared in the waveguide region. With the applied pressure in the device, the suspended PCW experiences strain that tries to pull it over the contact pad. At that point, rigidness of the suspended PCW is compensated by the applied stress in PCW. When the pressure is further increased, the stress across the PCW overcomes the rigid force inside the suspended PCW that snaps suspended

PCW downwards toward the contact pad. With the bending of suspended PCW over the pad, the transmission spectrum that is being transmitted through the waveguide initially has a wavelength shift inside the transmission spectrum of the circular nano-cavity. The number of rows along the y-axis in nano-cavity is also optimized to obtain high-power confinement in excited region. The applied pressure inside the device that suspends the nano-cavity on pad will depend on required deflection distance for transmission of power efficiently in PCW from input to output port. The separation distance between the suspended photonic crystal and the pad should be comparable with the strain limit inside the waveguide. The thickness of suspended photonic crystal waveguide is also optimized for sensing low-pressure values in the waveguide to actuate on the pad. The suspended waveguide snaps on pad due to modulus of elasticity of silicon present in PCW.

Figure 1a and b shows the schematic of nano-cavity based on suspended photonic crystal waveguide. The PCW consists of a circular ring of five air holes at the center

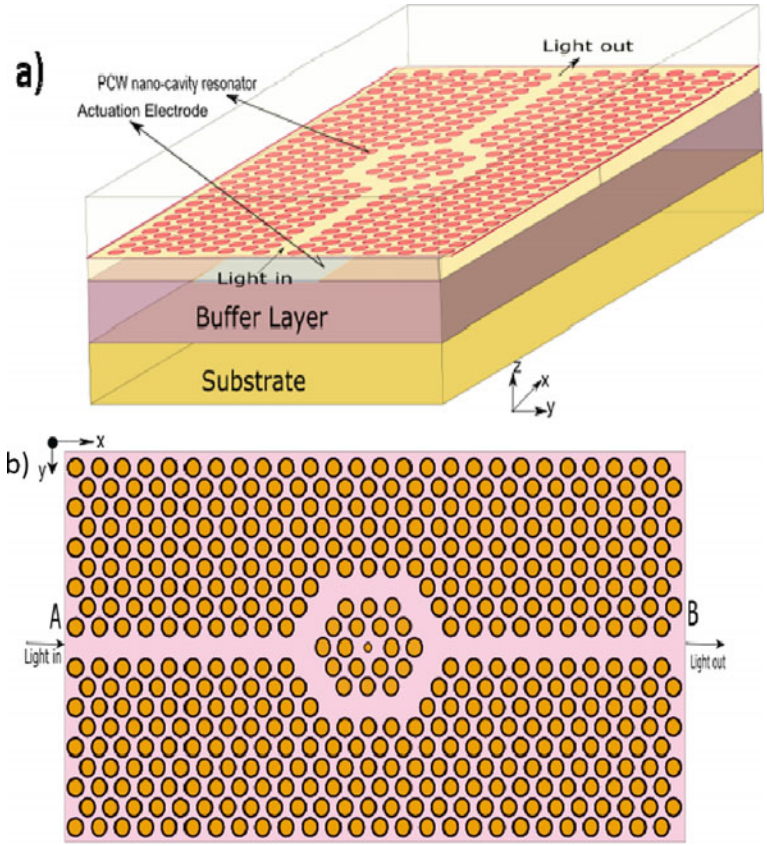

Fig. 1 Schematic of the **a**) proposed device **b**) nano-cavity based on suspended photonic crystal waveguide

with four and three air holes at the bottom and above of it. In the center of cavity, a nano-hole is created for the confinement of electro-magnetic fields. The line defect is patterned in the input and output of circular ring to provide excitation in the nano-cavity based on PCW. The finite element method is employed for propagation of electro-magnetic waves inside the nano-cavity. The light signal is feed in core region of the waveguide to propagate electro-magnetic waves inside the nano-cavity created in the waveguide region.

Figure 2a and b shows the mode profile with normalized electric field distribution inside the optimized circular ring of nano-cavity in photonic crystal waveguide. The effective mode index for the suspended photonic crystal waveguide structure is obtained as 3.2792. The electromagnetic field is highly confined in the ring cavity region. Figure 3 shows the pattern of normalized transmittance of electric field inside the waveguide region by drawing a cut-line along y-axis at an x-distance of 6.4 μm.

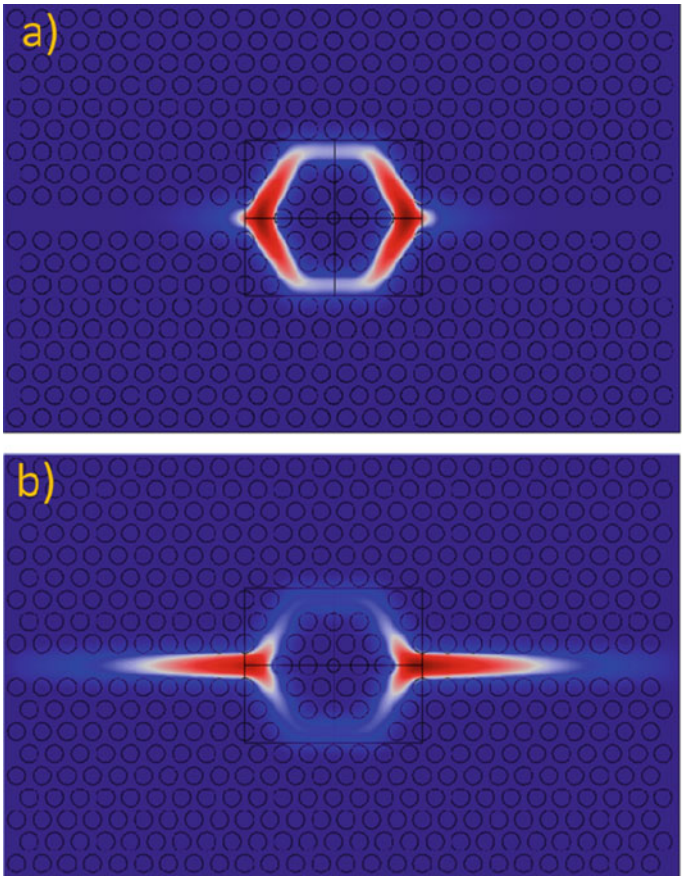

Fig. 2 Normalized mode profile in the optimized dimensions of nano-cavity present in photonic crystal waveguide

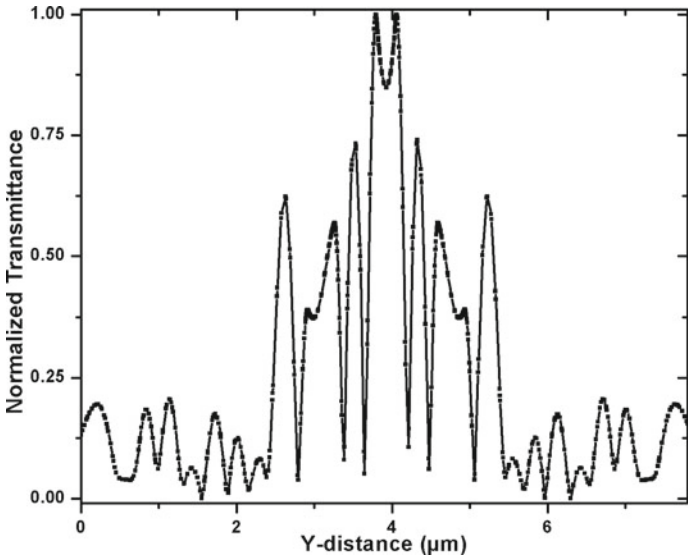

Fig. 3 Normalized transmittance of electric field along the *y*-axis in photonic crystal waveguide structure

It can be seen that the nano-cavity shows high confinement of electro-magnetic fields inside the ring of nano-cavity resonator.

The suspended PCW is optimized for varying different pressure in the device. The two suspended PCWs of varying thickness of 320 and 370 nm is considered for optimization in the device configuration. The *z*-displacement versus pressure plot is shown in Fig. 4 for varying the pressure from 1 to 4 MPa while the structure in [10] is used for the pressure range in between 0 and 0.10 MPa. The amplitude of displacement is derived with respect to the applied pressure for obtaining large displacement with low transmission loss in the cavity region. It can be seen that the displacement in the waveguide with thickness of 320 nm is more with the applied pressure as shown in Fig. 4. With increase in pressure, the shift in displacement also increases in the waveguide. It can also be seen that for a fixed displacement, less pressure is required to deflect the waveguide in downwards direction. As with increase in the thickness of waveguide structure, spring constant of structure also increases, and it requires more pressure to deflect on the contact pad in the device. Therefore, the thickness of waveguide is optimized for 320 nm to increase the power transmission efficiency in the device.

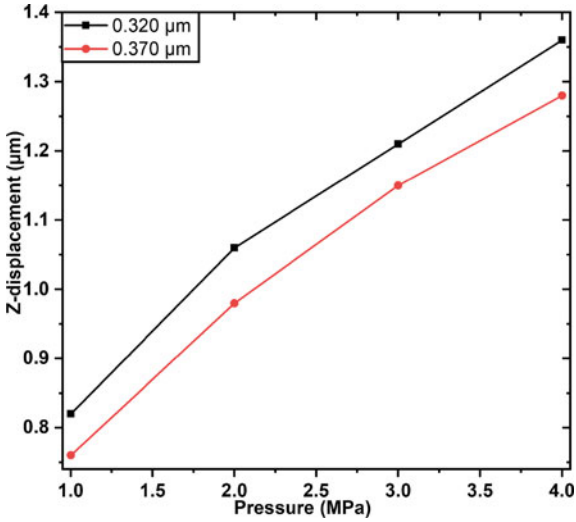

Fig. 4 Z-displacement versus applied pressure in the suspended nano-cavity photonic crystal waveguide

3 Results and Discussions

The optimized nano-cavity based on photonic crystal waveguide is excited with the pressure applied between the pad and silicon PCW. The normalized transmittance of the ring cavity PCW is shown in Fig. 5 which shows the transmission spectrum in the PCW with the wavelength varying from 1535 to 1554 nm. The normalized transmission spectrum is shown for varying pressure from 0 to 4 MPa in the device. The resonant wavelength increases with increase in the pressure. It shows the change in normalized transmittance with the displacement in the suspended PCW developed due to applied pressure in the structure. The suspended PCW silicon slab is utilized

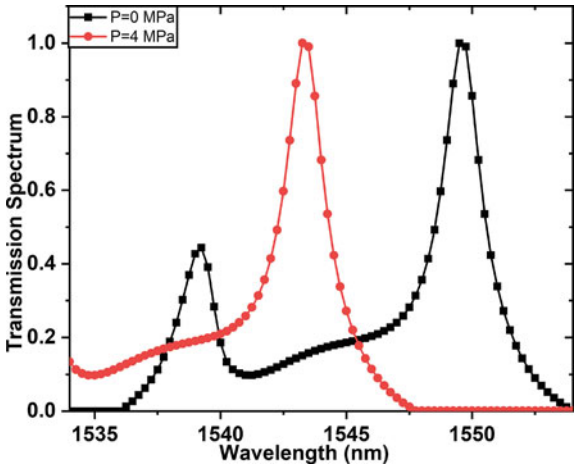

Fig. 5 Normalized transmittance of the suspended nano-cavity photonic crystal waveguide from 1535 to 1554 nm

for sensing in large photonic networks. The bending of suspended photonic crystal waveguide is more sensitive to introduce the interference in the propagation modes of nano-cavity.

4 Conclusion

The nano-cavity photonic crystal waveguide is optimized to acquire a high-confined mode profile in the waveguide region. The propagation of dominant normalized electric field is also investigated to confine the power in the cavity region. The opto-mechanical devices in combination with the nano-photonics structures has a great capability to get compatible with the existing Complementary metal oxide semiconductor (CMOS) process technology. The deformation process in the suspended PCW configuration has a capacity to sense the pressure in different applications. The suspended waveguide structures can also be expanded to the applications of switches and filters for tuning the wavelength.

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Design and Analysis of Thermo-optic Photonic Crystal Waveguide-Based Optical Modulator

Saurabh Agarwal, Jitendra K. Mishra, and Vishnu Priye

1 Introduction

There are in numerable methods for external tuning of photonics waveguides-based devices [1]. The thermo-optic tuning is emerged as an important techniques in photonics networks for the applications like modulating and sensing [2, 3]. They show an advantage of low power, high compactness and very high-quality factor in comparison to other tunable techniques [4]. Optical modulators are replacing the conventional modulators due to their high speed with very low optical loss [3, 4].

With the periodic arrangement of material inside photonic crystal (PC), the on-chip networks have gained a lot of attention in internet of things applications using the devices like interferometers and modulators [4, 5]. The photonic crystal waveguide in silicon photonics emerges as a potential platform due to its advantages of tightly confined modes with a very high confinement factor [5]. A highly compact thermo-optic photonic crystal waveguide-based optical lens is demonstrated for the polarization of light near the wavelength of 1550 nm [6]. Further, an optical modulator is also demonstrated using thermo-optic tuning for wavelength division multiplexing techniques [7]. The multi-layers stress in configurable devices is required to be minimized for providing high efficiency in the device. An air suspended technique for the micro-hotplate is employed for minimizing the stress and providing high thermal

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conductivity [8]. The thermal effect in the device is either provided by plasma injection effects in diode or by placing a micro-hotplate inside the photonics devices. The design of micro-hotplate is also crucial for minimizing the power consumption and increasing reliability in the optimized device. The optimized device further results in providing low optical losses and very high isolation between the waveguide and the micro-hotplate. Optical modulation is one of the crucial operation that has a capacity of shifting data in the wavelength division multiplexed (WDM) channels for forthcoming optical communication system [8].

Recently, various optical modulation devices based on PC have been investigated to analyze the performance parameters like extinction ratio and propagation of modes inside the device [7, 8]. The devices based on the principle of multimode interference structures [9], total internal reflection [10], and photonic crystal fiber [11] are published. However, the extinction ratio of these works is relatively low and is being responsible for under-performance of these devices. In development, the photonic crystal waveguide (PCW)-based directional coupler is also proposed to perform modulating function for wide-bandwidth region [12], but a complicated design with large number of fabrication steps are involved in these type of devices. The impact of isolation layer for increasing the mechanical stability is also reported [13]. However, the investigation for the variation in transmission spectrum with thermal conduction is still needs a look. Furthermore, an analysis of variation of temperature for the variation in modes is presented in waveguide [14, 15]. But, the temperature gets non-uniformly distributed over the waveguide that impacts the reliability and mechanical stability of the device [16]. Although, the technological fabrication aspects of thermo-optical devices have well investigated, but their performance is still restricted due to the presence of stress in multilayers [17, 18].

In this work, a MHP-based PCW-based device is proposed on silicon on insulator (SOI) platform for optical modulation. The optimization is carried out in the MHP for its high thermal efficiency and mechanical stability. The total electromagnetic fields in the form of transmission spectra, spectral shift and other parameters are investigated in detail to perform the modulator operation in the PCW-based modulator.

2 Device Description

Figure 1 shows the proposed cavity-based photonic crystal optical modulator integrated with micro-hotplate on SOI platform. The proposed device consists of a cavity inside the photonic crystal and an insulation layer of silicon dioxide is provided of thickness 0.15 μm. Over the oxide layer, a micro-hotplate is optimized and integrated with the proposed device for providing the thermo-optic tuning. The silicon photonic crystal waveguide consists an array of air holes with the diameter as 288 nm and the center to center gap between the holes is 415 nm. In this work, an air hole pattern in triangular lattice of silicon is patterned on the oxide buffer layer. The line defect

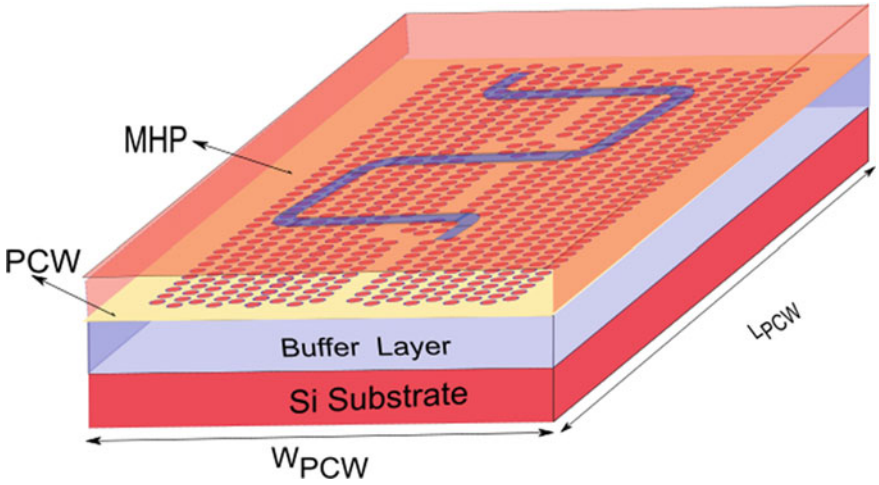

Fig. 1 Cavity-based photonic crystal optical modulator integrated with micro-hotplate on SOI platform

photonic crystal waveguide consists a pattern of air holes with 36 period array of air holes along y-direction with a footprint of 17.8 × 8.2 μm^2 in silicon slab.

In the PCW, the two cavities are incorporated inside the line defect with three air holes are present in the path of silicon. The cavities are created for confining the electro-magnetic radiations with a mechanism of Bragg's law and Fresnel deflection. The cavities are created inside the line defect to resonate a particular frequency. The waveguide is excited by allowing a laser source of light near 1550 nm inside the line defect region. The coupling is provided by a rectangular waveguide placed near optimized photonic crystal waveguide device. Over the optimized photonic crystal waveguide, an insulation layer is provided for the isolation between the waveguide and the optimized micro-hotplate. The isolation is provided inside the device for providing high thermal conductivity in optical modulator by acting as a heat barrier that further results in increasing the efficiency with very low optical losses inside the device. The micro-hotplate is also optimized for low multilayers stress inside the device. The effective index inside the cavity increases with increase in the temperature with a thermo-optic coefficient of $1.86 \times 10^{-4}\ K^{-1}$. With the increase in temperature from room temperature to 370° K, the effective index of the silicon slab increases due to which the resonant wavelength inside the cavity increases from 1561.8 to 1568 nm. The resonant wavelength inside the cavity is obtained with the optimized parameters of very high quality factor with tightly confined mode. The modified Sellmeier model for the variation in effective index with the temperature is given as [15]:

$$n^2(\lambda.T_m) - 1 = \sum_{i=1}^{m} \frac{S_i(T_m).\lambda^2}{\lambda^2 - \lambda_i^2(T_m)}. \tag{1}$$

3 Results and Discussions

The modes are calculated inside the optimized photonic crystal waveguide using the finite element method. A tightly confined modes with high confinement is obtained as shown in Fig. 2a and b. The confinement power is given as:

$$\Gamma = \frac{\int\int P_{n,\text{core}}(x, y)\mathrm{d}x\mathrm{d}y}{\int\int P_{n,\text{total}}(x, y)\mathrm{d}x\mathrm{d}y}. \tag{2}$$

The distribution of normalized transmittance is calculated for the optimized cavity at wavelength of 1561.8 nm is shown in Fig. 3 that shows high confinement inside the two cavities present in photonic crystal waveguide. The transmittance is calculated by providing the excitation in optimized device at different applied temperatures as shown in Fig. 4. With the change in temperature, there is a change in effective index of tightly confined modes present inside the cavity and due to which the resonant

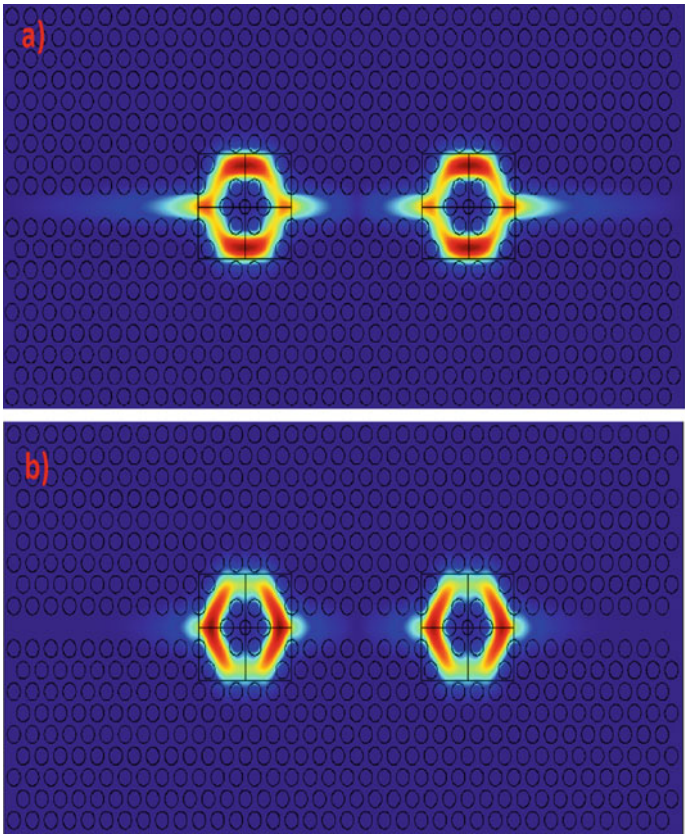

Fig. 2 Mode exist inside the photonic crystal waveguide for optical modulator

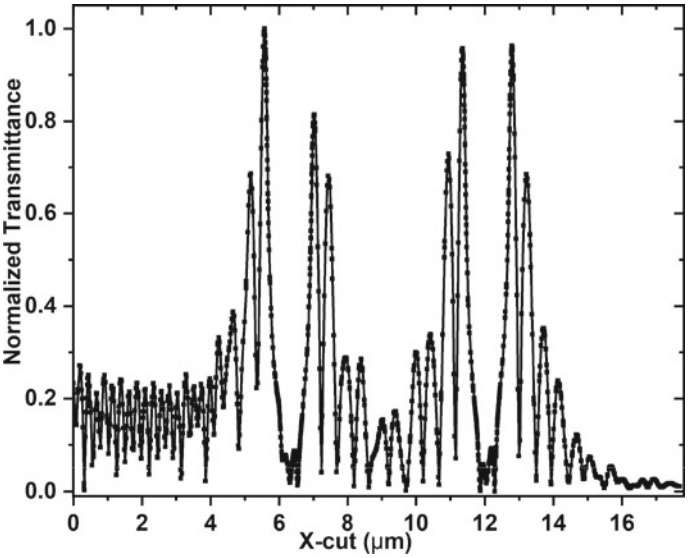

Fig. 3 Propagation of normalized electric field along x-direction inside the optimized device

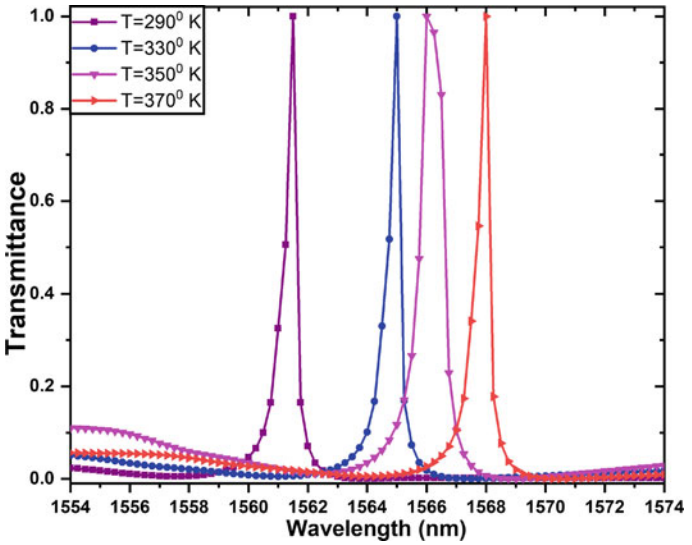

Fig. 4 Variation of transmittance versus wavelength with the application of temperature in thermo-optic photonic crystal based device

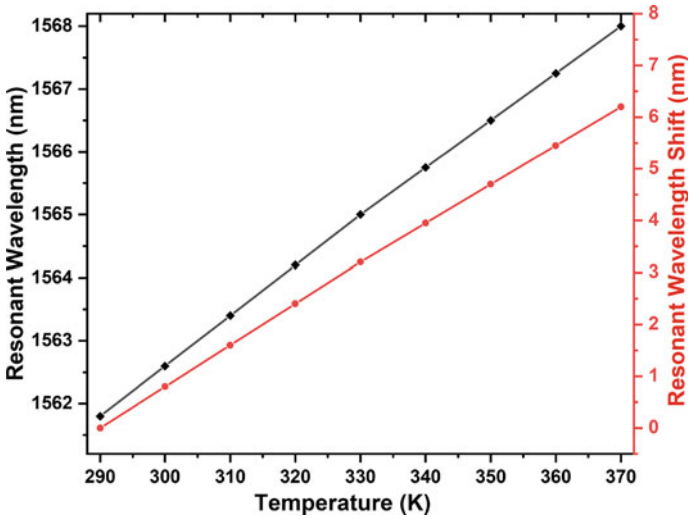

Fig. 5 The variation in resonant wavelength and resonant wavelength shift with the applied temperature in proposed device

wavelength inside the cavity gets increases with increase in the room temperature in cavity. The resonant wavelength and their shift is calculated at different thermal excitation by varying the temperature from 290° to 370° K that shows the shift in resonant wavelength from 1561.8 nm to 1568 nm with a spectral shift of 6.2 nm as shown in Fig. 5.

4 Conclusion

A model of temperature and stress in photonic crystal waveguide-based optical modulator is proposed for its high mechanical stability. The performance parameters of thermo-optic photonic crystal cavity are investigated utilizing the thermal model in micro-hotplate. Moreover, the spectral shift varies linearly with increase in the thermal excitation in the device and can be varied based on different applications. The optimized optical modulator can be integrated with other re-configurable optical circuits for sensing applications. The other different parameters in micro-hotplate can also be optimized according to the applications based on confined modes inside waveguide.

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A 0.18 μm β-Ga_2O_3 MOSFET Using $Al_2O_3/HfO_2/SiO_2$ Gate Dielectric for Low-V_{TH} High-Power Electronics Applications

Pratosh Kumar Pal, Avaneesh Kumar Dubey, Rajeev Kumar Chauhan, and Rajendra Kumar Nagaria

1 Introduction

There is the need of wide bandgap semiconductors other than GaN or SiC for high-power switching and power amplifier applications. Such need is being researched by number of wide and ultra-wide bandgap semiconductors. One of these less developed wide bandgap semiconductors is Gallium Oxide (Ga_2O_3). The β-Ga_2O_3 is the most stable polymorph of Ga_2O_3. The power control and switching applications are emerging very rapidly from electric and sensor-based autonomous vehicles to lightweight systems like drones and robotic controls [1]. These application requirements can be fulfilled by extending the performance of GaN and SiC or having another ultra-wide bandgap semiconductor like Ga_2O_3. The Ga_2O_3-based devices can handle very high switching voltages as it has breakdown electric field around 3X of GaN or SiC. It has ultra-wide bandgap ranging from 4.6 to 4.9 eV [2].

In [3], a 10 nm thick Ga_2O_3 is used as dielectric oxide grown over the GaAs/AlGaAs wafer for having low defect and high-k device. It has too low leakage current activation energy even though high-quality oxide is being used. The Edge-defined Film-fed Growth (EFG) method-based 2-in. β-Ga_2O_3 crystals are grown in [4], and its dislocation densities were estimated for growth of larger single-crystalline β-Ga_2O_3 crystal using EFG method. In [5], recess depth effect is investigated for

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electronic characteristics of β-Ga_2O_3 by considering 25 nm of HfO_2 as the dielectric. The performance analysis of β-Ga_2O_3 for Al_2O_3 and HfO_2 as dielectrics for around 10 nm to 30 nm of oxide thickness is investigated in [6–15], respectively, for different types of parametrical analysis. Similarly, the demonstration of Ga_2O_3 MOSFET for SiO_2 as dielectric is performed in [16] by considering the parameters for RF applications. Finally, the basic simulation of Ga_2O_3-based MOSFET devices is demonstrated in [17] by considering the all necessary steps to be followed for Gallium Oxide substrate MOS devices and a basic device simulation is explained in [18] by varying the doping and work function for an understanding.

This paper investigates different performance parameters of Ga_2O_3 substrate-based MOSFET for three different dielectric materials Al_2O_3, HfO_2, and SiO_2 by changing the oxide thickness of these dielectric materials. The comparison has been done in terms of parameters threshold voltage, ON resistance, ON current, OFF current, ratio of ON current and OFF current, transconductance, current density, and breakdown voltages. The simulations are performed using Silvaco TCAD software.

2 Device Design and Simulation

The Silvaco TCAD software is used for device simulation along with a non-isothermal model [5]. The device structure of β-Ga_2O_3 MOSFET is shown in Fig. 1a. This is the simplified model that has been used for the analysis of effect of different oxides on the β-Ga_2O_3 MOSFET devices. The low-field mobility model and constant thermal conductivity model have been assumed for simulations. The device dimensions were evaluated according to the required channel length. The β-Ga_2O_3 has the thermal conductivity of 0.13 cm^{-1} K^{-1}, and the other material parameters are considered mostly according to the data of [17].

The β-Ga_2O_3 MOS device structure in terms of potential across the layers, electron concentration, and hole concentration are shown in Fig. 1b, c, and d, respectively, for HfO_2 as dielectric. The I_D versus V_{GS} transfer characteristic of β-Ga_2O_3 MOSFET for HfO_2 as gate dielectric is shown in Fig. 2. The positive V_{TH} of β-Ga_2O_3 MOSFET is obtained from characteristic curve shown in Fig. 2. The V_{TH} of β-Ga_2O_3 MOSFET is 0.5 V, 0.8 V, and 1.4 V for HfO_2, Al_2O_3, and SiO_2 gate dielectric materials, respectively, when $t_{ox} = 5$ nm at $V_{DS} = 5$ V. As discussed in [14], the positive V_{TH} for homo-epitaxial Ga_2O_3 with the high-K dielectric material would be characterizing toward the enhancement mode behavior. But it will affect the ON current and the breakdown characteristic of the device by lowering them; however, this can be further improved in homo-epitaxial Sn-doped Ga_2O_3.

The I_D versus V_{DS} output characteristic of β-Ga_2O_3 MOSFET for HfO_2 gate dielectric is shown in Fig. 3. To verify the breakdown criteria of the device, it was simulated with $V_{GS} \ll V_{TH}$ and for large V_{DS}. The breakdown of device has been observed near to 78 V. The device exhibits good pinch-off characteristic with the maximum drain current of 194 mA/mm at $V_{GS} = 10$ V and $V_{DS} = 20$ V. The on

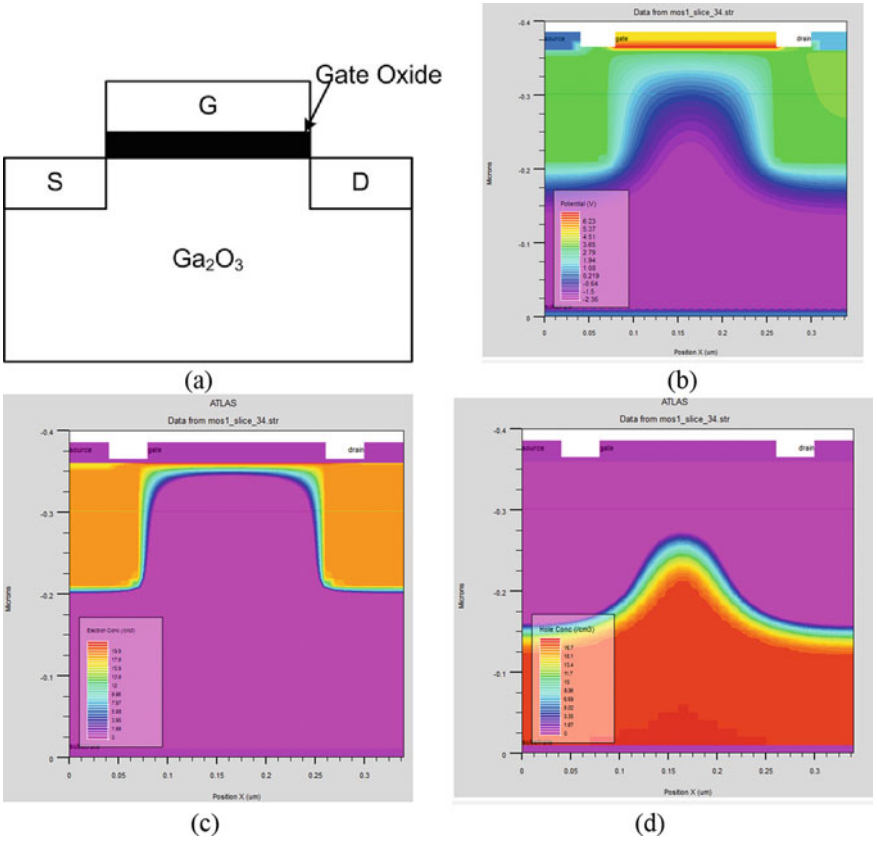

Fig. 1 The plots are for HfO_2 as dielectric in Ga_2O_3-based MOS **a** The device structure of β-Ga_2O_3 MOSFET, **b** plot of potential, **c** plot of electron concentration of MOS device, and **d** plot of hole concentration of MOS

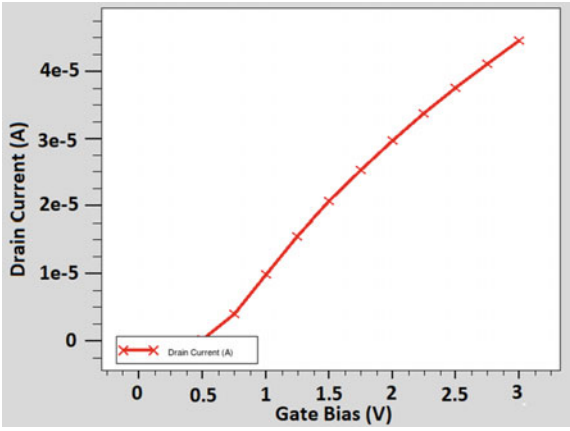

Fig. 2 The I_D versus V_{GS} transfer characteristic of β-Ga_2O_3 MOSFET for HfO_2 as gate dielectric at tox = 5 nm and $V_{DS} = 5$ V

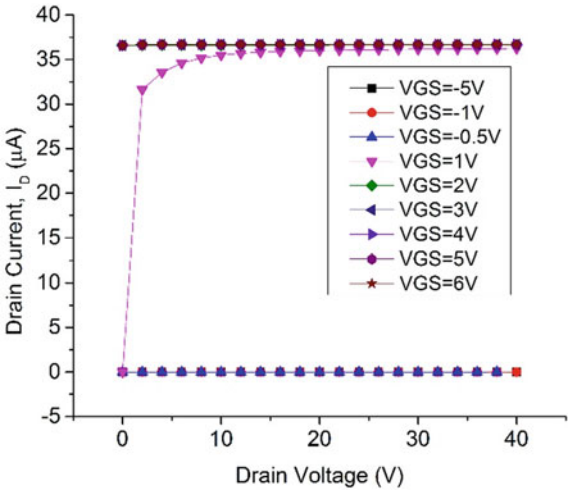

Fig. 3 The I_D versus V_{DS} output characteristic of β-Ga_2O_3 MOSFET for HfO2 gate dielectric at $t_{ox} = 5$ nm

resistance of device has been found as 28 5Ω mm from the I_D versus V_{DS} curve at $V_{GS} = 1$ V.

3 Results and Discussion

The effect of variation of T_{ox} (nm) for different oxide material on various device parameters such as (a) V_{TH} (b) Transconductance (c) I_{ON}/I_{OFF} (d) I_{ON} and I_{OFF} (log scale) is shown in Fig. 4. The T_{OX} is varied from 5 to 20 nm for this simulation study as most of the research papers consider this as the range of oxide thickness. Here, it is obvious that the wider T_{OX} gives lesser control of gate over channel, hence larger V_{TH}. The lowest V_{TH} has been found for HfO_2 dielectric when $T_{OX} = 5$ nm and $V_{DS} = 1$ V. The negligible off current is reported, which is in the range of 5×10^{-18} A for Al_2O_3 and HfO_2 at $T_{OX} = 5$ nm and goes toward 10^{-20} A when $T_{OX} = 20$ nm. It is because of the higher band gap of Ga_2O_3 and wider T_{OX}, which secures the penetration of tunneling through the oxide layer. The lowest off-state current is in the range of 10^{-21} A for HfO_2 at $T_{OX} = 15$ nm. The very large I_{ON}/I_{OFF} ratio (10^{+13} to 10^{+15}) has been achieved due to negligible off-state current flowing through the device. The maximum on current is about 40 μA, and it saturates near the $T_{OX} = 10$ nm. The electron accumulation barrier gets lower as the V_{DS} increases and device depleted again; it means higher gate voltage will be required for inversion layer and to flow of electrons through the device. The maximum transconductance of about 140 μA/V at $V_{DS} = 1$ V and $T_{OX} = 5$ nm is obtained for HfO_2.

The variation in current density (mA/mm) and transconductance (mA/V mm) with respect to T_{OX} for different oxide material is shown in Fig. 5a current density (mA/mm) and (b) transconductance (mA/Vmm), respectively. The current density

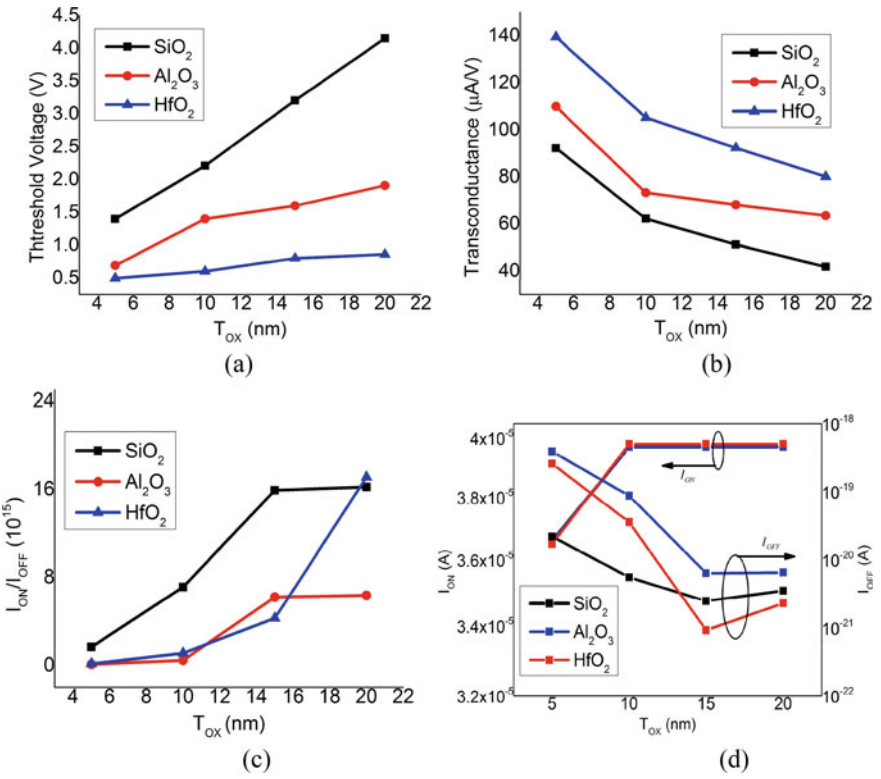

Fig. 4 Effect on various device parameters with respect to T_{OX} (nm) for different oxide material **a** $V_{TH,}$ **b** Transconductance, **c** $I_{ON}/I_{OFF,}$ **d** I_{ON} and I_{OFF} (log scale)

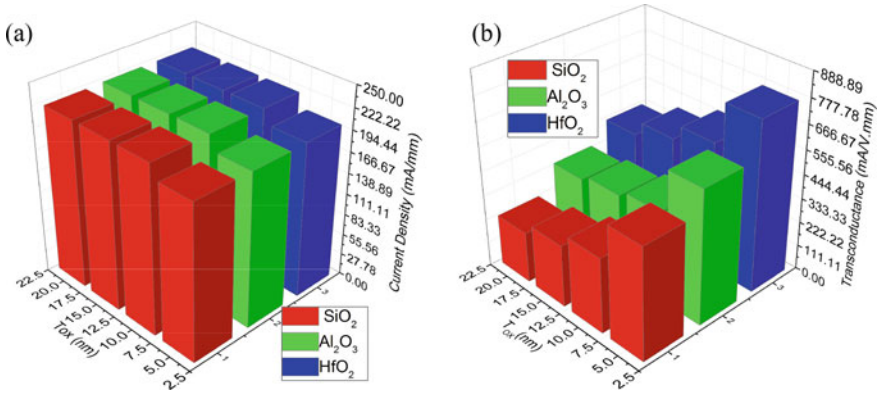

Fig. 5 Variation in current density (mA/mm) and transconductance (mA/V mm) with respect to T_{OX} for different oxide material **a** current density (mA/mm) **b** transconductance (mA/V mm)

Table 1 Comparison of Ga_2O_3 MOSFET reported in recent literatures with this work

Parameters	[11]	[13]	[14]	[15]	This work		
Year	2019	2019	2016	2019	2020		
Channel Length (μm), L_{SD}	3	2	3	2	0.18		
T_{OX} (nm)	20	20	42	25	5		
V_{DS} (V)	30	10	–	–	1		
Gate dielectric material	Al_2O_3	Al_2O_3	HfO_2	HfO_2	HfO_2	Al_2O_3	SiO_2
V_{TH} (V)	− 4.6	+ 4.2	+ 2.9	− 13.7	0.5	0.7	1.4
R_{ON} (Ω mm)	959	364	818	146	285	251	206
I_{OFF} (A)	1×10^{-7}	-	4×10^{-10}	7.1×10^{-11}	2.1×10^{-17}	5.4×10^{-16}	9.7×10^{-16}
$I_{ON}/\Delta I_{OFF}$	10^7	10^7	–	10^9	1×10^{16}	3.6×10^{15}	2×10^{15}
Max. on current Density (mA/mm)	10	11	11.1	101	194.4	194.4	194.4
Max. transconductance (mA/V mm)	2.55	2.7	0.18	–	140	111	92
V_{BR} (V)	2.32 k	–	80	240	78	106	124

is highest in the device with SiO_2 dielectric as it remains with highest possible on current. For the same value of V_{GS} and V_{DS}, the use of high-K dielectric material reduces the on current as it lowers the V_{TH}. But is also known that the high-K dielectric materials are more sensitive toward the change in gate voltage, therefore the change in current with respect to gate voltage will be more. Due to this, the transconductance of device is highest for HfO_2, which is about 700 mS/mm at T_{OX} = 5 nm. The transconductance of device reduces for the wider T_{OX}, as the gate control over the channel gets lesser for wider T_{OX}.

Comparison of Ga_2O_3 MOSFET reported in the literatures with this work is shown in Table 1. The simulation work shows that the Ga_2O_3 MOSFET has achieved positive V_{TH} as low as 0.5 V for high-k dielectric material HfO_2 when channel length, L = 0.18 μm and T_{OX} = 5 nm.

4 Conclusion

In this paper, the comparative analysis of β-Ga_2O_3 is performed for different gate dielectric materials by varying the gate oxide thickness. It is evident from the simulations results that the HfO_2 as gate dielectric shows the minimum value of threshold voltage of 0.5 V, and it has minimum variation in threshold voltage. In terms of

transconductance value, the HfO_2 as gate dielectric has the maximum value for the complete range of 5–20 nm of oxide thickness. The device shows very low OFF current and high I_{ON}/I_{OFF} ratio. Hence, it is suitable for high switching activity in electronic circuits. Along with the very low-V_{TH}, it also shows the nominal breakdown voltage. The transconductance of the device is large enough as compared to the [11, 13, 14]. Therefore, it is suitable for power amplifiers applications.

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ACF/PACF-Based Distance Measurement Techniques for Detection of Blockages in Impulse Lines of a Pressure Measurement Circuit for Nuclear Reactors

Ajit R. Pappu, Soumitra Kar, and Sachin Kadu

1 Introduction

Control and monitoring of Nuclear Reactors (NR) use hundreds of measurements like pressure, flow, and level. The signals from these measured parameters are transferred to control room via measurement transmitters. The signals from the measurement points are transmitted upto the transmitters by means of impulse lines. Usually, the impulse lines contain process fluids, but for certain process systems using hazardous fluids, another fluid as intermittent sealant is used. Here, we are focusing on impulse lines with process fluids.

The impulse lines-related faults affect performance of the measurements in NR. These faults include blockages in the lines, presence of bubbles or voids in the lines, and leakages. The blockages could be due to partial closure of the valves in the measurement circuit or sedimentation from the process fluid. These measurement faults result in consuming more maintenance time resulting in reduction of availability factor of NR. Globally, lot of research is going on for Fault Detection and Diagnosis (FDD) for NR for reducing their down times and to enhance the NR safety. Similar challenges are also faced by many chemical process plants, where the measurements are done with the impulse lines.

In this manuscript, we have presented an evolved blockage detection technique, by analyzing the pressure signals. A promising technique is researched based on statistical Autocorrelation functional (ACF) and Partial Auto correlation functional (PACF) distances by comparing healthy and blockage conditions.

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2 The Related Work

Fault Detection and Diagnosis (FDD) techniques are continuously being evolved for NR and also for many chemical process plants. Impulse line-related faults also falls in the FDD category. A book by Gertler [1] covers FDD in details. Venkatasubramanian et al. [2–4] have elaborated the FDD techniques in a series of three papers covering quantitative, qualitative, and process history-based techniques, respectively.

Particularly for NR, Hashemian [5] has written a book covering FDD techniques, dedicating a chapter for sensing line issues. In another references, Hashemian et al. [6, 7] have covered impulse line-related issues like blockages, voids, and leakages. Lin et al. [8–10] have done the diagnostics of impulse lines with focus on nuclear power plants (NPP). NPP are electricity generating type NR. The authors have modeled and theorized the impulse line diagnostics, using analogy of hydraulic-electrical circuits and formulated transfer function of the circuits using electrical parameters like resistance, inductance, and capacitance. They have modeled presence of voids, blockages, and leakages. Another authors Garcia-Berrocal et al. [11] have also modeled pressure transmitters for NPP using the electrical analogy. This electrical analogy concept is applied for general pipelines by Matko et al. [12], modeling the equivalent circuits and applied transfer functions using wave equations and Laplace transforms. Barbero et al. [13] have used noise analysis techniques, spectral shift of Power Spectral Density (PSD), again modeled with the electrical analogy.

All these models are derived making certain assumptions like lumping of parameters in the modeled component (s) and are approximate. These models are good to prove the theory that certain faults can be detected by analyzing the circuits.

This manuscript focuses primarily on a data driven technique. The data driven techniques account for the unknown phenomenon as well as complex nature of a system, thus appears appropriate for the application.

The data driven technique covered in this manuscript is time series clustering and application of Autocorrelation/Partial Autocorrelation Functional (ACF/PACF) distance computation for detection of blockage in the impulse lines.

In the actual application, the time series data under healthy conditions can be captured and saved which will be compared with the online data so as to detect a fault.

3 Pressure Measurement Using Impulse Lines

As discussed in the Sect. 1, pressure measurement is one of the widely used parameters in the NR. The impulse lines connect the process measurement points to the Pressure Transmitters (PT) or Differential Pressure Transmitters (DPT). Figure 1 shows a typical Venturi flow meter measurement circuit using a DPT.

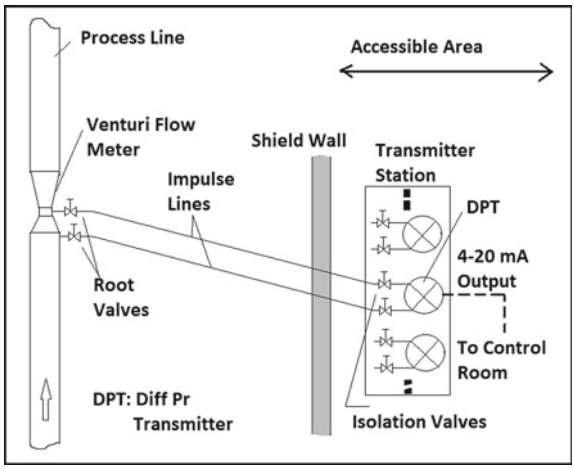

Fig. 1 Typical pressure measurement circuit in a nuclear reactor

The pressure signal lines need to be taken out from a shield as shown in the figure which consists one or more valves. The DPT gives analog electrical 4–20 mA signal output, fed to receiving instruments like plant computers, recorders, dataloggers, etc. Many flow and level measurements are based on measurements of differential pressure, for which impulse lines are provided to transmit the process signal up to the DPT, installed many meters away from the measurement points. The impulse lines are closed at the transmitter end; thus, no flow exists in the lines. The fluid in the lines may be the process fluid itself. In Indian Pressurized Heavy Water Reactors (PHWR), a type of NPP, water or heavy-water is the main process fluid.

4 The Techniques Applied

The pressure transmitters record the system pressure at the measurement point as well as picks up the "noise" generated by the measurement system itself. The signal other than the actual process dynamics is treated as the "noise." Process dynamics are of low frequency as compared to the "noise." When a high pass filter (HPF) is applied to the pressure signal, the low frequency process dynamics are filtered out. The leftover signal is nothing but "noise." Interestingly, this "noise" itself contains a lot of information about the process as well as the measurement system itself.

The research covered here focuses on blockages in the impulse lines. Other measurement system faults like voidage in the impulse lines are researched and covered in another publication [14].

We have explored various time series clustering techniques, which are not applied earlier for impulse line fault detection. The approach followed is comparison of the two time series captured under normal working conditions and with blockage conditions in the impulse lines. We have explored techniques like statistical distance measures, deviation from a particular statistical distribution. Markatou et al. [15] have elaborated distance measurement techniques.

As the pressure signals consist process dynamics as well as the captured "noise" with hidden certain system characteristics, Fast Fourier Transform (FFT)-based filters are applied to filter out process dynamics, and the techniques are applied to the "noise" component of the signals.

Various time series clustering approaches are explored and distance between healthy and faulty conditions is compared. The analysis shows promising results for applying Autocorrelation and Partial Autocorrelation Function (ACF/PACF) for detecting presence of blockages in the impulse lines. The FFT and ACF/PACF are discussed in the subsequent subsections.

4.1 Filtering Process Component of the Pressure Signal

Discrete Fourier Transform (DFT) of a signal $x[n]$ for N observations is computed using analysis equation, as given by Oppenheimer [16],

$$X[k] = \sum_{n=0}^{N-1} x[n] W_N^{kn}, 0 \leq k \leq N-1, \text{ where, } W_N = e^{-j\left(\frac{2\pi}{N}\right)} \tag{1}$$

$X[k]$ is the DFT with k terms.

For filtering low frequency process dynamics, a frequency threshold F_k is chosen and the amplitude of frequency components below the threshold frequency is set to zero as,

For $k < F_k$, $X[k] = 0$.

Using synthesis equation, Inverse Fourier Transform is applied as,

$$z[n] = \sum_{k=0}^{N-1} X[k] W_N^{-kn} 0 \leq n \leq N-1 \tag{2}$$

where $z[n]$ is the filtered series after filtering low frequency component.

4.2 Statistical Moments

Standard deviation, Skewness, and Kurtosis are second, third, and fourth order statistical moments, respectively.

These statistical moments are computed to see any reflection of the blockages in these parameters. The first moment is mean which is zero for standardized data series. In fact, standarization is the first step of our analysis.

The equations for the moments are as follows,

$$\sigma^2 = E(X-\mu)^2 = \sum_{x=-\infty}^{\infty} (x-\mu)^2 f(x) \tag{3}$$

where $f(x)$ is probability mass function.

$$S = E\left[\frac{(x-\mu)^3}{\sigma}\right] \tag{4}$$

$$K = \frac{E(x-\mu)^4}{\left[E\left((x-\mu)^2\right)\right]^2} \tag{5}$$

where, σ^2, S and K are Standard deviation, Skewness, and Kurtosis.

E is the expectation and μ is the mean.

4.3 Time Series Clustering

Time Series Clustering is briefly well compiled and elaborated by Montero and Vilar [17], covering various parametric and nonparametric techniques for dissimilarity measures with applications of statistical software R package. Recent version of R package is 6.2.2 [18]. Corduas and Piccolo [19] have investigated statistical properties of Autoregressive (AR) distance for Autoregressive Integrated Moving Average (ARIMA) process. Earlier, Piccolo (1986) [20] has done foundation for distance measuring for ARIMA process. Galeano et al. [21] have formulated Clustering of a time series based on parametric modeling. Comparison of two time series has been done by various statistical distance measurement techniques. Auto Correlation Function (ACF) and Partial Auto Correlation (PACF) distances are used for this application, elaborated in subsequent subsection. For evolving data analysis software code, a book by Cryer et al. [22] is handy which elaborates Time series analysis using R software package.

4.4 Auto Correlation Function and Auto Correlation Distance

Auto Correlation and Partial Auto Correlation Function (ACF and PACF, respectively) computes correlation of a series with itself with a time lag. Auto correlation is a measure of variables current value with lagged value. It ranges between + 1 positive autocorrelation and − 1 negative autocorrelation. Zero value indicates no correlation.

The partial autocorrelation at lag k is the correlation that results after removing the effect of any correlations due to the terms at shorter lags.

For this research, the 4–20 mA analog signals from process transmitters are acquired in digitized form in a data acquisition system. As a first step of analysis, acquired digital signals "$\boldsymbol{x}$" are standardized using mean "μ" and standard deviation "σ" as follows,

$$z = \frac{x - \mu}{\sigma} \tag{6}$$

Box and Jenkins et al. [23] give covariance and correlation for zero mean series z for lag "l," derived from expectation E as,

$$\gamma_l = \text{cov}(z_t, z_{t+l}) = E\big[(z_t - \mu)(z_{t+l} - \mu)\big] \tag{7}$$

$$\rho_l = \text{corr}(z_t, z_{t+l}) = \frac{E\big[(z_t - \mu)(z_{t+l} - \mu)\big]}{\sqrt{E[z_t - \mu]^2 E\big[z_{t+l} - \mu\big]^2}} \tag{8}$$

where variance is, $\sigma_z^2 = \sqrt{E[z_t - \mu]^2 E\big[z_{t+l} - \mu\big]^2}$.

For a stationary process, variance doesn't change with a time lag l, which gives,

$$\rho_l = \frac{\gamma_l}{\gamma_0} \tag{9}$$

Now, let us consider two time series X_T and Y_T with T observations. **Distance between ACF and PACF coefficients are to be computed.**

Correlation vectors for X_T and Y_T components are given as (2008) [17],

$$\rho_{X_T} = \big(\rho_{1,X_T}, \rho_{2,X_T}, \ldots, \rho_{k,X_T}\big)^T \text{ and } \rho_{Y_T} = \big(\rho_{1,Y_T}, \rho_{2,Y_T}, \ldots, \rho_{l,Y_T}\big)^T \tag{10}$$

where l is chosen such that for $\rho_{l,X_T} \approx 0$ and $\rho_{l,Y_T} \approx 0$.

Auto Correlation Functional distance (ACF) is,

$$D_{\mathrm{ACF}}(X_T, Y_T) = \sqrt{\left(\rho_{X_T} - \rho_{Y_T}\right)^T \Omega \left(\rho_{X_T} - \rho_{Y_T}\right)} \tag{11}$$

where Ω is a matrix of weights.

For uniform weights, it's identity matrix and the distance becomes Euclidean distance.

If the weights are geometrically decaying with autocorrelation lag, the ACF, as given by [17] is,

$$D_{\mathrm{ACF}}(X_T, Y_T) = \sqrt{\sum_{i=1}^{k} p(1-p)^i \left(\rho_{i,X_T} - \rho_{i,Y_T}\right)^2} \tag{12}$$

where $0 < p < 1$,T is number of samples and "l" is the lag.

We are experimented that for our analysis, Eq. (11) is adequate.

The same equations are also applicable for Passive Auto Correlation Functional distances (PACF) as the distances between the ACF/PACF coefficients are computed.

5 Experimental Setup and Test Matrix

An experimental setup is evolved as shown in Fig. 2 with intention of this initial stage is to establish a technique for blockage detection by processing of an acquired signal.

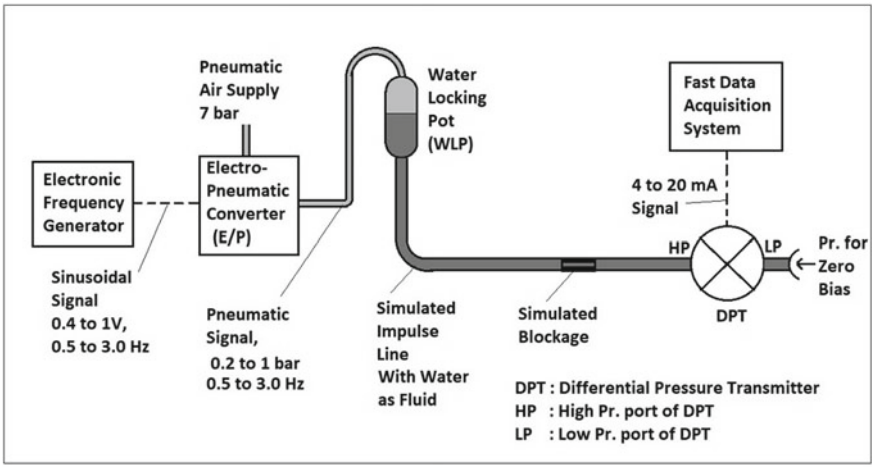

Fig. 2 Simulated setup for detection of blockage in an impulse line

The research is focused on "noise" analysis of an acquired pressure signals. Thus, the technique shall be able to distinguish process dynamics from the noise. In order to simulate process dynamics, a sinusoidal pressure generator of various frequencies has been evolved and the tests are carried out from 0.5 Hz to 3.0 Hz signal, a typical range of the process dynamics for NR. The analysis primarily involves filtering the process dynamics and applying various digital signal processing techniques to the "noise" component of the signal to identify signatures for various phenomenon hidden in the "noise." This manuscript is focused on identification of signature of impulse line blockages hidden in the "noise."

The setup generates sinusoidal pneumatic pressure test signal of different frequencies. This is achieved by applying sinusoidal signal from an electronic frequency generator to an Electro-Pneumatic converter (E/P). The pneumatic signal is converted to hydraulic signal by applying it to a Water Locking Pot (WLP). The Differential Pressure Transmitter (DPT) used is having High Pressure (HP) and Low Pressure (LP) ports. From the WLP, the hydraulic pressure signal is fed to HP port of the DPT. The LP port of the DPT is connected to a fixed pressure for adjusting zero bias of the DPT so as to configure it at required signal range. The DPT is calibrated for range 0 to 1 bar differential pressure for linear output signal of 4–20 mA. The response time of the DPT, that is time to reach 63.2% output when a step input signal is given as per IEC 17025 is 20 ms. The DPT output signal is fed to a Fast Data Acquisition System (FDAS) having configurable features of scanning speed, input signal type, range, etc.

The impulse tube selected is 2 m long, with internal diameter of 10 mm. The inserts made to simulate blockages are having 2 mm internal diameter, 25 mm long (BK), tightly fitting into the impulse line. The experimentations are carried out using one and two inserts inserted in the line. The test matrix is given in Table 1.

Table 1 Test matrix for impulse line blockage simulation

Test condition	Set No	Data sample nomenclature for various input sinusoidal signal in Hz			
		0.5	1.0	2.0	3.0
No blockage (WO)	Set-1	WO-S1-P5	WO-S1-1	WO-S1-2	WO-S1-3
	Set-2	WO-S2-P5	WO-S2-1	WO-S2-2	WO-S2-3
BK, one unit	Set-1	BK-1-S1-P5	BK-1-S1-1	BK-1-S1-2	BK-1-S1-3
	Set-2	BK-1-S2-P5	BK-1-S2-1	BK-1-S2-2	BK-1-S2-3
BK, two units	Set-1	BK-2-S1-P5	BK-2-S1-1	BK-2-S1-2	BK-2-S1-3
	Set-2	BK-2-S2-P5	BK-2-S2-1	BK-2-S2-2	BK-2-S2-3

Abbreviation: *BK* Block, *WO* Without Block

For each test, the data acquisition has been done at 1 ms interval for 4096 samples.

Software Platform R version 6.2.2 (2019) [18] has been used for evolving a code for data analysis.

6 Analysis and Results

The intention of this work is to identify signature(s) of blockages in the impulse lines hidden in the "noise" captured by the measurement circuit. Thus, the process dynamics need to be filtered out from the acquired signal. The test matrix is given in Table 1 is chosen to cover input sinusoidal test signals with frequencies from 0.5 to 3.0 Hz. Low frequency process dynamics components are filtered out while processing the signals. Thus, only the "noise" components remain. Intention is to identify signatures independent of the process dynamics. We also point out that the acquired signals are in the engineering units, that is 4–20 mA current signal with linear relation to the calibrated range of the DPT, thus scaling and standardization of the signal is done. In order to ascertain the signal pattern for a particular condition, two sets of tests are conducted for each of the condition.

The analysis covered in this manuscript, also looks for the blockage signatures in the most common basic statistical moments under the different conditions, viz. Standard deviation, Skewness, and Kurtosis. These moments are computed for the "noise" components. Figure 3 shows bargraphs under differ conditions and it is clear that with these common statistical moments it is not possible to identify signature of presence of blockage in the impulse lines.

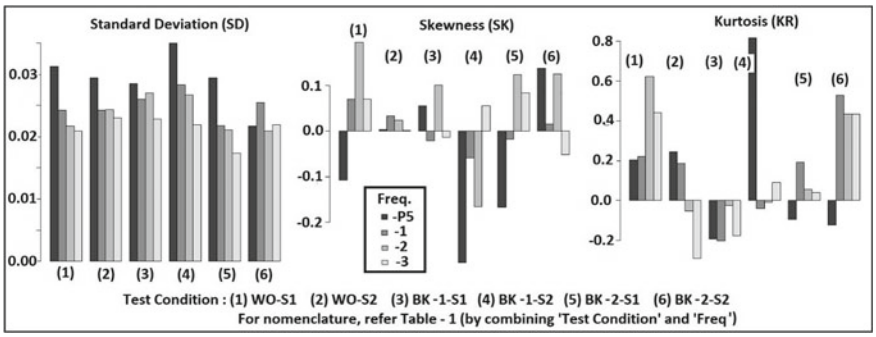

Fig. 3 Standard deviation, skewness, and kurtosis under different impulse line blockage conditions computed at different input signal frequencies

As no signature is detected in the moments, we have explored various advanced techniques for identifying the signature (s) for detecting the blockages. We have realized that time series clustering techniques by comparing the signals of healthy and faulty conditions could be a promising approach. Montero and Vilar (2017) [16] have elaborated various time series clustering techniques for comparing various statistical distance measures between the time series. We explored Dynamic Time Warp (DTW), Frechet Distance (FD), Hellinger and Squared Hellinger distance (HD/SHD), Probability Distribution Clustering (PDC), Autocorrelation and Partial Auto Correlation Function (ACF/PACF) distance. We found ACF and PACF as one of the most promising.

The ACF and PACF distances are computed by evolving a code using R package "TSclust" [24]. Governing equations for the computations are as mentioned in the Sect. 4.0. Figures 4 and 5 represent certain results of comparing ACF and PACF under two conditions of blockage, as described in Table 1. The signals with no blockages are used as a reference signal for comparing with the signal with impulse line blockage conditions.

Figure 4 compares the distances with one unit of the block BK, and Fig. 5 compares the distances with two units of the block BK. For process dynamics of the order of 0.5 Hz, as seen from the barplots (a) and (e) of Figs. 4 and 5 clearly distinguishable partial blockage in the impulse line are observed. The ACF/PACF distances increases as the blockage in the line increases. Another observation is that the distances are also a function of input signal process dynamic frequency. Even though this frequency is filtered out using a high pass filter, the process dynamics still continues to affect

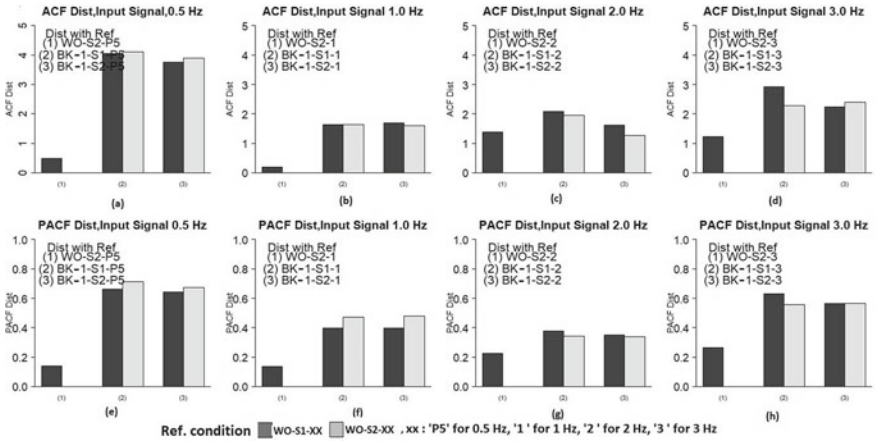

Fig. 4 Bar graphs showing the ACF/PACF distances under various conditions with **single** unit of block BK

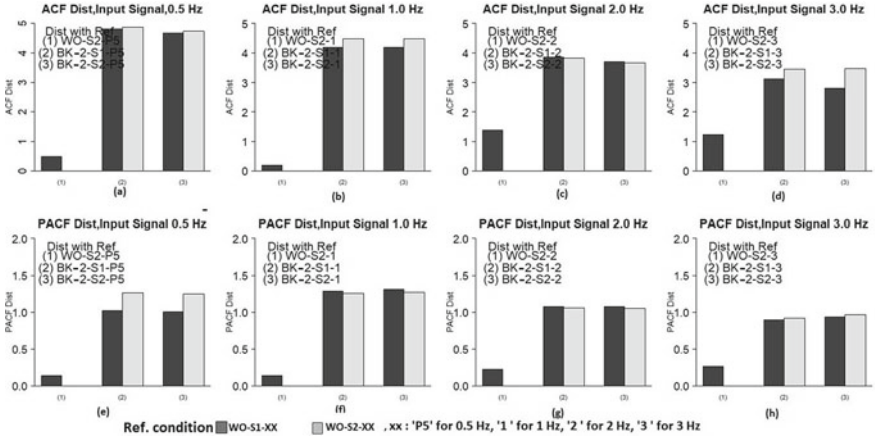

Fig. 5 Bar graphs showing ACF and PACF distances under various conditions with **two** units of block BK

the ACF/PACF distances. At low frequency process dynamics, the detection is more prominent.

7 Conclusions

This research shows that Auto Correlation and Partial Auto Correlation Functions (ACF/PACF) are proving to be effective techniques for detecting blockages in the impulse lines. There is further scope for refining the technique by more simulations and experimentations.

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Multi-objective Particle Swarm Optimization Based Enhanced Fuzzy C-Means Algorithm for the Segmentation of MRI Data

Munendra Singh, C. S. Asha, and Neeraj Sharma

1 Introduction

Magnetic resonance imaging (MRI) data provide three-dimensional images and are widely used to diagnose by means of studying the internal structure of different organs. MRI renders superior soft-tissue contrast, which provides more information required for the detailed analysis of the body organs such as spine, brain and other soft tissues. Furthermore, the specific pathological conditions are characterized through the different pulse sequences. MRI is safe medical imaging modality due to its non-ionizing behavior as compared to the CT scan. The clinicians highly appreciate the segmentation of MRI data for quantitative analysis of the pathology. Hence, the current work includes T1 and T2 sequences of MRI data for the segmentation that aids clinical applications.

Brain segmentation is the process the segregation of non-overlapped regions of brain tissues such as cerebrospinal fluid, white matter, and gray matter. The gray values of pixels play important role to characterize the segmentation of MRI images. The segmentation of an image can be achieved, using several approaches that normally includes edge detection, thresholding, region extraction, and clustering. Out of these segmentation techniques, clustering method is widely employed for segmentation of an image, which is based on unsupervised learning approach. Previously, several clustering methods such as fuzzy c-means (FCM) [1], and k-mean [2] algorithms have been utilized to achieve the segmentation of images. In FCM approach, the pixel membership degree associated with a particular cluster is

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considered to separate the image into the multiple regions, whereas k-mean clustering method looks at whether the pixels are close to the particular cluster or not. Recently, the conditional spatial FCM algorithm achieved superior performance over k-means for MRI data [3]. The FCM algorithm has been found valuable in various medical and biological applications [4–6]. However, the performance of the standard FCM algorithm is a matter of concern in the presence of noise to segment the different regions in MRI data.

The probabilistic FCM algorithm simultaneously reduces the bias field and segments the MRI data with greater accuracy [7]. Chuang et al. included the spatial information of local neighbors in the SFCM approach by modifying the objective function of FCM [8]. The algorithm produces the impressive result after segmenting the image data even in the presence of high noise. Further, the mean and median filtered data of the images have been inculcated in the fitness function of standard FCM, and Chen and Zhang names these methods FCM_S1 and FCM_S2, respectively [9].

Further, Szilagyi et al. mentioned a practical approach to handle the drawback of FCM_S1 and FCM_S2 algorithms [10]. The work altered the original concept by adding the local spatial information of an image in advance. The enhanced FCM (EnFCM) improved the processing time and enhanced efficiency with promising segmentation results. However, the quality of segmentation depends on the weighted factor of de-noised data [11]. The algorithm is robust to the noise when the weight factor is high, however, yielded over segmentation. Further, the segmented data preserves the details if the weighted factor is low. But, the selection of the weight factor is tedious when the unknown noise content is present in the information. Hence, trial and hit methods were often occupied to alleviate such circumstances.

In spite of high segmentation accuracy, the shortcoming of the current method suggests the necessity of an adaptive weighting factor leading to precise segmentation for different sequences of MRI data in the presence noise. Hence, the proposed work recommends EnFCM algorithm optimized by multi-objective particle swarm optimization (MOPSO). The proposed algorithm addresses tuning of the weighted factor based on the noise level present in the MRI data.

The present study is arranged as follows. Section 2 highlights the fundamental algorithm of EnFCM. Section 2.2 provides the concept of MOPSO. Sections 2.3 and 2.4 discuss the proposed methods employed for noisy data segmentation. In Sect. 3, it analyzes the experimental results and compares proposed approach with existing popular methods followed by conclusion in Sect. 4.

2 Background

2.1 Enhanced FCM

Let the image data $I = [p_{11} \ldots p_{kl} \ldots p_{mn}]$ has c number of clusters. We consider 3×3 kernal around the kth pixel to find the local average value. This average value with original data is utilized to compute the normalized local weighted sum S_k for kth pixel [10] given as follows:

$$S_k = \frac{1}{1+w}\left(p_k + \frac{w}{N_w}\sum_{w \in N_w} p_n\right) \tag{1}$$

where p_n represents the nearby pixels around the central pixel p_k, and N_w denotes the number pixels in the kernal. The weight factor w controls the influence of surrounding pixels. The data S, which has local pixel information is calculated in prior using Eq. (1) while assuming all pixels in the image as the central pixel. Let X are the different sets of intensity values of an image data S, where X is less in comparison to the total pixels N in an image. The pixels with the intensity value of l is represented as Ψ_l. Therefore, $\sum_m^p \Psi_m = N$ is satisfied. Finally, the objective function is calculated as follows:

$$F_{\text{EnFCM}} = \sum_{j=1}^{c}\sum_{l=1}^{X} \Psi_l u_{jl}^m \left(S_l - v_j\right)^2 \tag{2}$$

where c denotes total possible clusters in input image, u_{jl} represents the fuzzy membership value of lth pixel to jth cluster, m represents the fuzzy exponent and v_j denotes the center of the cluster. The membership function and center of the cluster used in Eq. (2) is derived as follows:

$$u_{jl} = \left[\sum_{m=1}^{c}\left(\frac{S_l - v_m}{S_l - v_j}\right)^{2/m-1}\right]^{-1} \tag{3}$$

$$v_j = \frac{\sum_{l=1}^{p} \Psi_l u_{jl}^m S_k}{\sum_{l=1}^{p} \Psi_l u_{jl}^m} \tag{4}$$

The goal of the present work is automated selection of weight factor w, which plays the crucial role in regulating the amount of noise in the output segmented image. The work introduces the adaptive selection of weight factor w using MOPSO algorithm.

2.2 Multi-objective Particle Swarm Optimization

Particle swarm optimization (PSO) is an evolutionary computation algorithm that mimics the social behavior of a flock of birds [12]. This algorithm is popular and useful in producing the optimum result while using single objective function or more than one objective functions. The problem where more than one objective functions are possible, known as multiple objective functions, and the algorithm is popularly known as Multi-Objective Particle Swarm Optimization (MOPSO). This algorithm yields a set of optimal solutions called Pareto Fronts rather a single optimal solution [13]. In literature, MOPSO has been employed in various image processing applications [14–16]. The optimization of N objectives is formulated as follows:

$$\text{maximize } f(x) = [f_1(x), f_2(x), \ldots f_N(x)] \tag{5}$$

where $f_i(x)$ denotes the objective function for the multi-objective problem. Assume we have two sets of solutions s_1 and s_2, the two possibilities are: (i) one solution dominates the other solution, and (ii) none of the solution dominates the other. These two conditions are represented as follows:

$$\begin{aligned} &\forall i \in \{1, 2, \ldots, N_{\text{obj}}\} : f_i(s_1) \leq f_i(s_2) \\ &\exists j \in \{1, 2, \ldots, N_{\text{obj}}\} : f_j(s_1) < f_j(s_2) \end{aligned} \tag{6}$$

If the conditions stated in the above equation is violated, then the solution s_1 will not dominant the solution s_2. The solutions obtained from the MOPSO are non-dominated in nature and known as Pareto-optimal solutions [17]. The particles in PSO are moving in search of the best solution. In $(k+1)$th iteration, the velocity of the particle i is v_i^{k+1}, which is defined as follows:

$$v_i^{k+1} = w v_i^k + c_1 r_1 \left(p_i - x_i^k\right) + c_2 r_2 \left(p_g - x_i^k\right) \tag{7}$$

where w is the weight, c_1, c_2 are the particle's rate of learning, r_1, r_2 are the normalized random numbers valued from 0 to 1. The personal best positions of the particles are p_i and p_g is the global best position of all the particles achieved till $(k+1)$th iteration. The present position of the particle at kth iteration is x_i^k, which is defined as follows:

$$x_i^{k+1} = x_i^k + v_i^{k+1} \tag{8}$$

Position and velocity of the particle keep updating according to the objective function till the convergence criterion is met. The present work selects the controlling hyper parameters as provided in Table 1.

Table 1 Hyper parameter settings of MOPSO algorithm for optimized EnFCM method

Parameter settings	Range of values
Iterations	30
Population size n	15
Rate of learning, i.e., c_1 and c_2	1.2 and 1.2
Adaptive weight w	0.9–0.4
Two objective functions	DC and JS

2.3 Fitness Functions

The proposed method utilizes the combination of segmentation quality index called Jaccard similarity (JS) [18] and Dice coefficient (DC) [19] as objective functions. The Jaccard similarity index measures the segmentation quality, which is the ratio of the intersection of the segmented image I_S and reference image I_R and union of the segmented image I_S and reference image I_R.

$$\text{JS} = \frac{|I_S \cap I_R|}{|I \cup I_R|} \tag{9}$$

Dice coefficient (DC) is also employed to measure the segmentation quality in a slightly different way, which is given as follows:

$$\text{DC} = \frac{2|I_S \cap \text{I}_R|}{|I_S| + |I_R|} \tag{10}$$

The proposed work is validated using the above defined segmentation quality indexes.

2.4 Materials and Methods

The proposed method has used the simulated MRI data obtained from the BrainWeb database (www.bic.mni.mcgill.ca/brainweb/) [20]. The size of each image is 181 × 217. Each of these images comprise four different segments such as cerebrospinal fluid (CSF), gray matter (GM), white matter (WM), and background. As the computation of magnitude MRI is a nonlinear mapping. In the experimental section, we considered noise with different mean and the standard deviation of 5, 7.5, 10, and 12.5. This helps to evaluate the noise robustness of the presented methodology.

The proposed approach has selected 3 × 3 size moving kernal and computed mean to derive the weighted sum data. The nature of noise in the MRI data have Rician distribution. In this view, the present study includes the Rician distributed noise in the MRI data.

3 Results and Discussion

The value of weight factor w in enhanced FCM method (EnFCM) assumed to be static or constant. The MRI image suffered from low noise, the higher value of weight factor produces over segmentation. In present method, optimized EnFCM algorithm is employed to adaptively chose this weight factor. Figure 1 depicts the output image corresponding to 90th slice and 100th slice of T1 weighted BrainWeb simulated MRI data. The value of weight factor λ shown in Fig. 1 suggested that the value of weight factor λ is varying for the same MRI image suffered with different amount of noise. It is also observed from the figure that the value of weight factor keeps increasing as noise content increases in the image. For high noise content, the relatively larger value of weight factor is needed.

Figure 2 presents the comparison of the EnFCM and the our modified method optimized EnFCM using JS and DC. The value of the weight factor is kept same for various images of the dataset while running EnFCM. However, this value is adaptive and will vary based on the objective function chosen to get the output image of maximum segmentation accuracy. The presented graphs show the advantage of adaptive choice as compared to the constant value of the weigh factor. Figure 2 ensures that the optimized EnFCM has attained better quantitative metrics like JS and DC as compared with the standard EnFCM for both white matter and gray matter tissues of brain MRI is concerned. Besides, figures clearly show that the difference between the performances of both the algorithms that the accuracy increases with the rise in the noise level. The proposed algorithm is compared with recent state-of-the-art methods such as: FCM_S1 [9], FCM_S2 [9] and EnFCM [10] quantitatively and qualitatively. Table 2 confirms the better quantitative performance of the proposed optimized EnFCM with respect to state-of-the-art methods. In addition, the table compares the segmentation accuracy of three regions of brain MRI that includes WM, GM, and CSF with respect to metrics JS and DC. It is evident in the table that

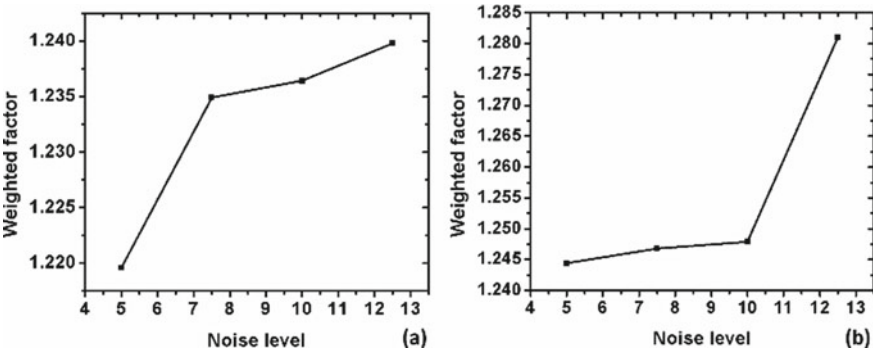

Fig. 1 Effect of change in the weighted factor in presence of different level of noise for **a** 90th slice of T1 weighted MRI image, and **b** 100th slice of T1 weighted MRI image

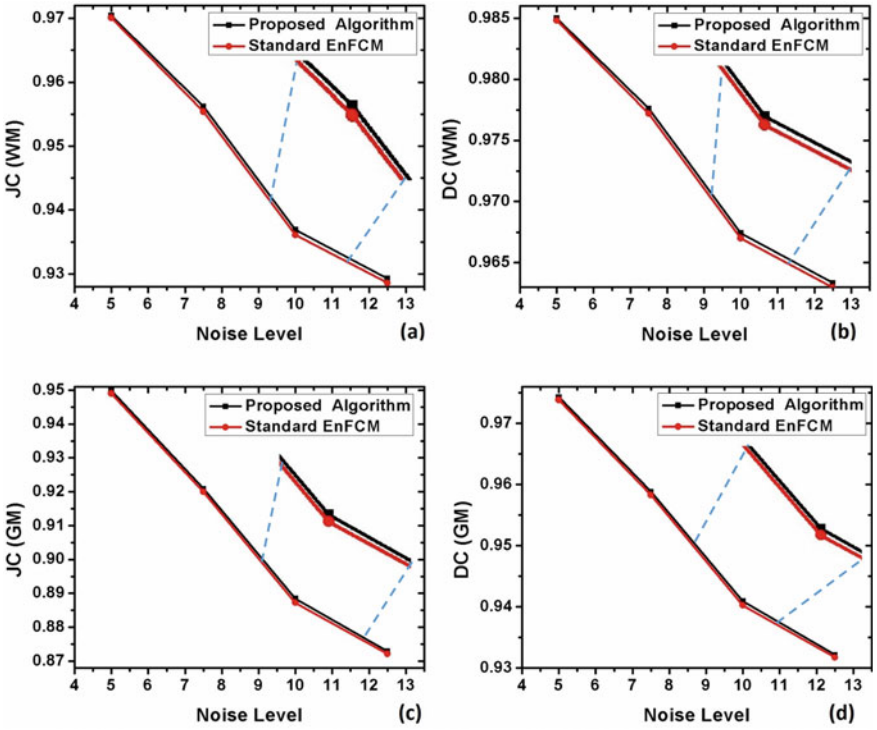

Fig. 2 Comparison of proposed MOPSO optimized EnFCM with its base algorithm, i.e., popular EnFCM on 90th slice of T1 weighted MRI. Here, the value of weighted factor w has been chosen 1.2 0 for popular EnFCM algorithm. The segmentation results in presence of different amount of noise in terms for **a**, **b** white matter (WM) in terms of Jaccard Similarity (JS) and Dice coefficient (DC), and **c**, **d** gray matter (GM) in terms of JS and DC

the proposed MOPSO optimized EnFCM algorithm outperforms considered classical FCM_S1, FCM_S2 and EnFCM segmentation techniques. The performance of FCM_S2 remains poor for the images chosen than the other segmentation algorithm. Further, the qualitative comparison of these segmentation algorithms for 100th and 90th slices of T1 weighted BrainWeb MRI dataset is provided in Fig. 3. We have added noise variance of 10 and 12.5 to both of the slice images in order to evaluate the robustness of the proposed method. Qualitative inspection of the results shown in Fig. 3, it can be identified that the proposed MOPSO based EnFCM method is producing segmentation results most closest to the reference segmentation results in comparison to FCM_S1, FCM_S2 and EnFCM algorithms.

Table 2 Quantitative comparison of proposed MOPSO optimized EnFCM with FCM_S1, FCM_S2 and EnFCM algorithms in terms of JS and DC for 90th slice and 100th of T1 weighted MRI images

Data	Noise level	Region	Segmentation algorithm							
			FCM_S1		FCM_S2		EnFCM		Proposed EnFCM	
			JS	DC	JS	DC	JS	DC	JS	DC
90 T1	5	WM	0.968	0.984	0.964	0.981	0.970	0.984	**0.970**	**0.985**
		GM	0.947	0.972	0.934	0.966	0.949	0.973	**0.949**	**0.974**
		CSF	0.922	0.959	0.908	0.951	0.918	0.957	**0.919**	**0.958**
	7.5	WM	0.951	0.975	0.949	0.974	0.955	0.977	**0.956**	**0.977**
		GM	0.915	0.955	0.907	0.951	0.919	0.958	**0.920**	**0.958**
		CSF	0.874	0.933	0.860	0.924	0.873	0.932	**0.873**	**0.932**
	10	WM	0.931	0.964	0.929	0.963	0.936	0.967	**0.936**	**0.967**
		GM	0.880	0.936	0.876	0.934	0.887	0.940	**0.888**	**0.940**
		CSF	0.818	0.900	0.813	0.896	0.822	0.902	**0.823**	**0.902**
	12.5	WM	0.919	0.958	0.917	0.956	0.928	0.963	**0.929**	**0.963**
		GM	0.859	0.924	0.854	0.921	0.872	0.931	**0.872**	**0.932**
		CSF	0.783	0.878	0.771	0.871	0.792	0.884	**0.792**	**0.884**
100 T1	5	WM	0.973	0.986	0.971	0.985	0.973	0.986	**0.974**	**0.987**
		GM	0.945	0.971	0.935	0.966	0.947	0.973	**0.949**	**0.974**
		CSF	0.909	0.952	0.896	0.945	0.908	0.952	**0.909**	**0.952**
	7.5	WM	0.957	0.978	0.954	0.976	0.962	0.980	**0.962**	**0.980**
		GM	0.914	0.955	0.908	0.951	0.922	0.959	**0.922**	**0.959**
		CSF	0.868	0.929	0.858	0.923	0.865	0.928	**0.866**	**0.928**
	10	WM	0.942	0.970	0.941	0.969	0.949	0.974	**0.951**	**0.975**

(continued)

Table 2 (continued)

Data	Noise level	Region	Segmentation algorithm							
			FCM_S1		FCM_S2		EnFCM		Proposed EnFCM	
			JS	DC	JS	DC	JS	DC	JS	DC
		GM	0.884	0.938	0.879	0.936	0.895	0.945	**0.898**	**0.946**
		CSF	0.825	0.904	0.815	0.898	0.826	0.904	**0.826**	**0.905**
	12.5	WM	0.919	0.958	0.916	0.956	0.929	0.963	**0.931**	**0.964**
		GM	0.847	0.917	0.838	0.911	0.861	0.925	**0.864**	**0.927**
		CSF	0.771	0.871	0.755	0.860	0.779	0.875	**0.781**	**0.877**

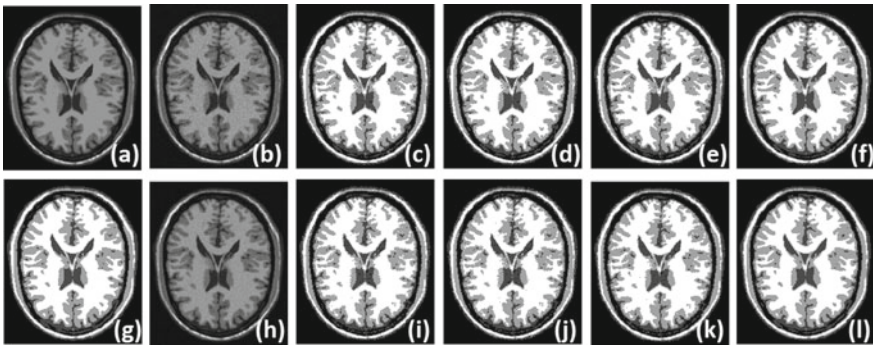

Fig. 3 Qualitative comparison of proposed method with FCM_S1, FCM_S2 and EnFCM algorithms on **a** 90th slice of T1 weighted MRI free from noise assumed as the reference image, **g** respective segmentation results. The reference image is corrupted with noise **b** having standard deviation 10, and **h** noise having standard deviation 12.5. The results obtained from **c**, **i** FCM_S1, **d**, **j** FCM_S2, **e**, **k** EnFCM, and **f**, **l** proposed MOPSO optimized EnFCM

4 Conclusion

The proposed work focused to obtain the automated weight factor of the enhanced FCM algorithm using on MOPSO algorithm. The proposed algorithm has employed an adaptive tuning of the linear weighed factor for maximizing the segmentation accuracy. The current approach has been found highly helpful when the of noise content in the image is unknown. The qualitative results clearly show the precise edges of the MRI images when compared with the other considered algorithms. The quantitative comparison showed outperformed accuracy among the state-of-the-art segmentation approaches. The timing complexity of the proposed method could be reduced using a parallel computing approach. This approach is expected to reduce the processing time of the algorithm to overcome the shortcoming of the nature-inspired algorithms. Furthermore, a large, diverse dataset of MRI sequences will be considered to validate the testing results.

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Recognition of Facial Images via Self-Organizing Landmark Location with Approximate Graph Matching

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1 Background

Face recognition (FR) has got significant attention of researchers over the past few years [1–7]. This growth is mainly due to its applications for person identification in the field of private and secure systems. FR is one of the most used traits of biometric systems. Elastic bunch graph matching (EBGM) [8], support vector machines (SVM) [9], self-organizing map (SOM) [10, 11, 12, 13], and landmark geometry [14, 15], etc., are some of the methods used for face recognition.

The support vector machines are among the most successful face recognition algorithm where varieties of kernel are used either globally or locally [9]. SVM classification technique can be used for both multi-view face detection and pose estimation by enriching support vectors with extra pose information. Landmark geometry refers to extraction of important features in face image and then comparing these features with those of other images for recognition [14, 16].

EBGM is another popularly used method for FR which uses graph matching techniques. In EBGM, a face is represented by an image graph where each node labeled by complex Gabor wavelet coefficients set. Graph of a new image is matched with the bunch graph formed from all the faces available in the model dataset. The best matching indicates the recognized face. It uses phase information of complex Gabor wavelet coefficients for accurate node positioning. Object adapted graphs are formed so that nodes indicate to particular facial landmarks and large rotations can be handled. It uses a new data structure named face bunch graph (FBG) [8]

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for generalized representation of the face graphs but has the limitation of manual generation of the first set of model image graphs. Each model graph utilizes grid structure, and nodes belonging to same landmark points. The present work aims at automatic generation of the face graph using self-organization of the salient points as decided by the GC.

In the proposed technique, the problem of face recognition is interpreted as a graph matching problem. Unlike EBGM, the proposed technique does not require manual generation of image graph. Gabor filter is utilized to extract the landmark points in the face. A set of GC is incorporated with every landmark point of the face image. Further, SOM is trained by GC of landmark points to obtain the topology of the facial image (i.e., face geometry). The SOM is created for each face image, and then these graphs are matched using an *Approximate Graph Matching* (*AGM*) technique.

The SOM has been adopted earlier in numerous models for FR [13, 17, 18], but its application had been confined for feature matching. Here, in SOM graph, we attempt to capture the geometry of facial image. For the purpose, the existing SOM is modified and named as Bi-Self-Organizing Map (Bi-SOM). Further, a matching technique is formed to match facial geometries generated by Bi-SOM graphs for all facial images, and the proposed technique is denoted as *Bi-SOM* + *AGM*.

The direction to rest sections of this paper is as follows. An overview of the proposed technique is exhibited in Sect. 2. Gabor feature extraction has been presented in Sect. 3. Self-organizing Map has been introduced in Sect. 4. Section 5 describes the graph matching technique. Experimental outcomes are presented in Sect. 6. The summary of the work is presented in Sect. 7.

2 System Overview

At first, Gabor-filtered facial images are obtained from test/training faces by passing them through a band of Gabor Filters with varying orientations and scales. Then, landmark detection technique [19] is utilized to locate facial landmarks in each facial image based on its Gabor-filtered version (for each face, coefficients of all orientations and scales are coupled). By utilizing generated facial landmarks as inputs, the *Bi-SOM* is trained for capturing the facial geometry of the corresponding facial image. The same procedure is followed to form face graphs for all training (or gallery) faces. On the arrival of a new test face (probe image), the same set of steps is followed to generate its face graph. In the last step, the *AGM* technique is utilized to perform FR by matching the test image face graph with face graphs of all training (or gallery) faces. The best match is recorded as the concluding recognition decision for that probe image.

3 Gabor Feature Extractions

3.1 Gabor Filters

Bandpass filters or Gabor filters are utilized in the field of image processing for different purposes including stereo disparity estimation, texture analysis, and feature extraction [20–24].

Gabor filters can be described as the convolution of an image $I(\mathbf{x})$ for $\boldsymbol{x} = (x, y)$ using family of *Gabor Kernels* $\boldsymbol{\psi_k}(\boldsymbol{x})$ [20] that is parameterized over the wave vector **k** which defines the orientation and wavelength of the kernel. The kernel is a plane wave bound by Gaussian envelope function, formulated as:

$$\psi_k(x) = \left(\frac{k^2}{\sigma^2}\right) e^{-\left(\frac{k^2 x^2}{2\sigma^2}\right)} \left[e^{ikx} - e^{-\left(\frac{\sigma^2}{2}\right)}\right] \tag{1}$$

where,

$$k = \begin{pmatrix} k_\upsilon \cos \varnothing_\mu \\ k_\upsilon \sin \varnothing_\mu \end{pmatrix};$$

$$\text{for } k_\upsilon = 2^{-(\upsilon+2)/2}\pi; \text{ and } \emptyset_\mu = \frac{\pi}{8}\mu \tag{2}$$

Here, μ and ν denote Gabor filters orientation and scale, respectively. The Gabor filters formulated in Eq. (1) are self-similar where all filters can be produced from single-mother wavelet through rotation and dilation. Gaussian envelope function is controlled by relative width $\sigma = 2\pi$. In Eq. (1), term e^{ikx} defines the oscillatory part of filters, whereas term $e^{-(\sigma 2/2)}$ allows filters to be DC-free and hence, invariant to any shift in gray-level of the image.

3.2 Gabor Coefficients (GC) Formation

There are some points in the face with high-information content, called *landmark points*. In the proposed approach, these features are being extracted using Gabor filters [8, 9, 14, 22]. A set of GC are found for every pixel of facial image and then pixels having high valued GC are selected as the landmark points for that image [19]. For finding a set of GC, *five* different scales $v \in \{1,2,3,4,5\}$ and *eight* orientations $\mu \in \{0,1,2,3,4,5,6,7\}$ are used, i.e., 40 GC for each image. An original facial image and its expected Gabor-filtered images are depicted in Fig. 1.

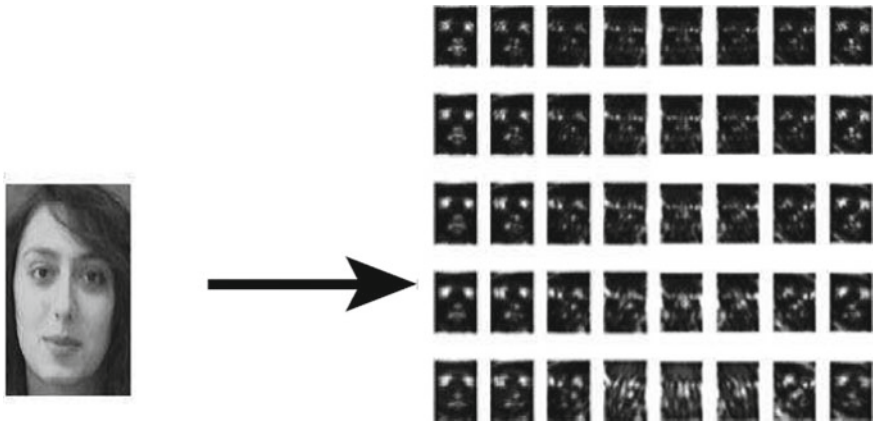

Fig. 1 Original test face (left), and Gabor-filtered images for different frequencies and orientations (right)

3.3 Landmark Points Detection

In order to obtain landmark points in a facial image, a single-saliency value for each pixel is generated by adding all 40 GC. Each image is completely scanned through 7×7 window to choose the pixels in such a way that center pixel saliency value is higher than other pixels in that window, and all pixel saliency values are above the global average saliency computed over all the pixels [19]. All the identified pixels denote the landmark points in the facial image. In this paper, 80 such pixels are selected to represents landmark points. The sampled facial image with few of the landmark points is shown in Fig. 2.

3.4 Landmark Feature Vectors

A feature vector at each chosen landmark point is formed after landmark points section process. Then, Bi-Self-Organizing Map (Bi-SOM) utilizes these feature vectors as input for training purpose. The feature vectors are computed as a combination of transform coefficients of Gabor Wavelet. The kth feature vector for i^{th} facial image can be formulated as:

$$V_{i,k} = \left\{ G_{i,j}(x_k, y_k), x_k, y_k; \text{ for } j = 1, 2, \ldots, 40 \right\} \tag{3}$$

where $V_{i,k}$ denotes kth feature vector of ith face (i.e., $k = 1, 2, \ldots, 80$ landmark points in the face), $G_{i,j}(x_k, y_k)$ represents 40 GC of each landmark point k, and (x_k, y_k) denotes location of kth landmark in an image i.

Fig. 2 Few representative landmark points in test face image

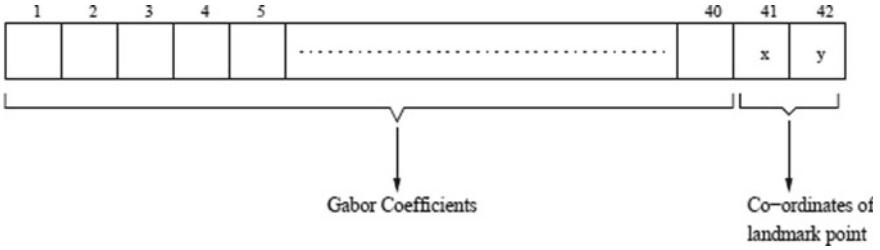

Fig. 3 Structure of 42-dimensional feature vector

Feature vector consists of 42 components, first two from right denote the landmark point location and remaining 40 represents the magnitude of GC at various orientations and scales. Information about the feature locations assists in obtaining the feature vectors and facial geometry. The structure of feature vector is shown in Fig. 3.

4 Bi-Self-Organizing Map

The original self-organized map (SOM) has an ability to transform an arbitrary dimensional incoming signal pattern into discrete maps of dimension one or two. It is accomplished adaptively in a topologically ordered fashion [13, 18, 19, 22, 25]. Each input pattern typically constructed from a localized region whose nature and location differs from one realization of the input pattern to another. SOM is built

on the architecture of neuron where each map attempts to reorient itself after each iteration on the basis of an input pattern. Each neuron is represented in the form of some weights, usually initialized by some values in the beginning of the process. After each iteration, neuron weights are adjusted if the neuron comes within the neighborhood of best matching unit (BMU).

Here, the original SOM is modified to capture the geometry of facial images named as Bi-Self-Organizing Map (Bi-SOM) which is used as a 2-D map of size 6 × 6. In this map, the 42-dimensional weight vector is associated with each neuron. For initializing these weights vector, 36 vectors out of 80 input patterns are randomly selected and allocated in the ascending sequence of their pixel position in the face. Further, to find BMU, each input vector is chosen one by one and match with all the Bi-SOM neurons. The details of Bi-SOM and procedure of calculating match are provided in Algorithm 1 and 2. On the calculation of the BMU, the radius of the neighborhood is determined using the following formulation:

$$\sigma(t) = \sigma_0 e^{-\frac{t}{\lambda}}, \text{ for } t = 1, 2, 3, \ldots. \tag{4}$$

where $\lambda = n/\log(\sigma_0)$ is time constant; σ_0 denotes lattice width at time t_0 and its value is six, t denotes current time-step, and n denotes iteration numbers.

During each iteration, weight vectors of BMU and its neighborhood nodes are settled using the following formulation:

$$W(t+\mathbf{1}) = W(t) + L(t)(V(t) - W(t)) \tag{5}$$

$$L(t) = L_0 e^{-\frac{t}{\lambda}}, \text{ where } t = 1, 2, 3, \ldots. \tag{6}$$

where L denotes the learning rate that reduces with time, and L_0 denotes its initial value; $V(t)$ represents the input vector; t denotes current time step or iteration number; $W(t)$ denotes neuron weight vector at time t.

After a fixed number of iterations, the proposed Bi-SOM technique generates the graph for each image. An initial Bi-SOM grid and face graph for a sample face is shown in Fig. 4a, b, respectively. The proposed Bi-SOM, each input vector is formed from two kinds of sub-vectors; (i) two-dimensional position vector of a selected pixel and (ii) 40-dimensional vector of GC. Finally, the best match unit (BMU) is obtained by combining the results calculated separately for each sub-vector.

5 The Proposed Graph Matching Procedure

Graph of an input facial image is matched with all face graphs in the database to recognize a person accurately. Due to the variation in pose and expression of two or more faces, their corresponding face graphs cannot be matched precisely. Hence, AGM operation is performed where the graph in the training set having the smallest

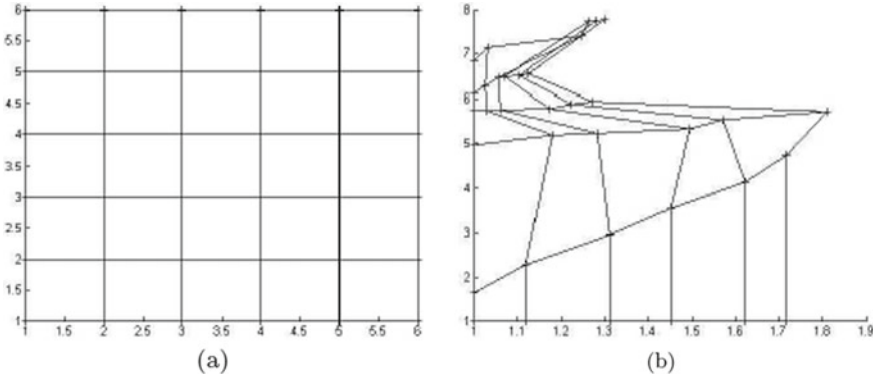

Fig. 4 For a sample face **a** Initial Bi-SOM grid, and **b** Face graph after training process

deviation from the test (or probe) facial image is granted to be the best match. The step-by-step procedure of the proposed approximate graph match technique is presented in Algorithm 3. Usually, for matching two face graphs simply GC are examined [8, 19], but the proposed technique also considers face geometry that exhibits the superior performance over conventional technique.

Algorithm 1: Bi-SOM Formulation

Step 1: Initialize Bi-SOM network neurons weights. These weights are having dimension same as input vectors.
Step 2: Randomly chose the input vector n from training images and supplied to the network.
Step 3: Among all neurons, select a neuron with weight closest to the input vector. The winning neuron is usually recognized as BMU as per Algorithm 2.
Step 4: Measure the neuron neighborhood ratios of BMU using Eq. (4). All neurons within this radius are assumed to be inside the neighborhood of BMU.
Step 5: Regulated the weight of each adjacent neuron to make it closer to the input vector. The weights of neurons that are closer to the BMU are mostly adjusted (using Eq. (5)) to reduce the distance from BMU.
Step 6: Repeat Steps 1 through 5 till all the prominent variations are recognized in the feature map.

Algorithm 2: Finding Best Match Unit

Step 1: Calculated the cosine distance using Eq. (7), i.e., C_j between an input vector and each neuron weight vectors of dimensions 40.

$$C_j = \sum \frac{x_i a_{i,j}}{|x_i||a_{i,j}|}; \text{ for } i = 1, 2, \ldots, 40 \tag{7}$$

where $X = \{x_i\}$ denotes input vector; $a_{i,j}$ represents ith dimension (Gabor coefficient) of jth neuron ($j = 1, \ldots, 36$).
Step 2: Calculated the Euclidean distance E_j (using Eq. (8)) between the input vector and 2-dimensional position vector of weights associated with each neuron.

$$E_j = \sqrt{\sum (x_i - a_{i,j})^2}; \text{ for } i = 41, 42, \text{ and } j = 1, 2, \ldots, 36 \tag{8}$$

Step 3: A neuron with maximum $(C_j - E_j)$ value is decided as BMU for that particular input vector.

Algorithm 3: Approximate Graph Match

Step 1: C_j and E_j (refer Eqs. (7) and (8)) calculated between each neuron of the probe and all neurons of gallery images. The C_j and E_j distances are used for a sub-vector having dimensions 40 and 2, respectively.
Step 2: Compute $(C_j - E_j)$ for each pair.
Step 3: The maximum $(C_j - E_j)$ value pair is recorded, and its value is added to the former sum set to zero initially.
Step 4: For each neuron of probe image above steps are executed, and final sum value is obtained by adding all maximum values. If final sum value is greater than a specified threshold, then face is recognized.

6 The Experimental Results

6.1 Databases Used

The details of benchmark face databases used in the present paper are given below:

6.1.1 ORL Face Database

In this database [26], total 400 images of 40 subjects are available, i.e., 10 images per subject. Facial images are varying in terms of facial expressions (smiling/non-smiling, open/closed eyes), lighting, and facial details (glasses/no-glasses). A dark homogeneous background is set for all captured images. All faces are gray-scale and size of 92×112 pixels. Frontal faces of each subject are used for training and remaining images are utilized for testing.

Fig. 5 Sample face images of FERET Dataset

6.1.2 FERET Face Database

The FERET database [16] is another benchmark facial image dataset which is utilized in present paper for analyzing the effectiveness of the proposed face recognition technique. There are 14,051 facial images of 1196 subjects. All faces are 256 × 384 Gy scale images. Facial pictures of a particular subject were taken in sets of 5–11 photographs. Two frontal view faces one with a natural expression (fa), and other with alternative facial expression (fb) were captured.

For 200 sets of photographs, a third frontal face was captured under different lighting condition by a different camera (fc). The remaining pictures were recorded at various aspects of right and left profile such as (i) half right and half left profile (hr, hl), (ii) left and right profile (labeled pl and pr), and (iii) quarter right and the quarter left profile (qr, ql). In this paper, frontal views (fa- fb), profiles (pl-pf), and half- profiles (hl-hr) images are utilized in such a way that hr, pr, and fa images are utilized as gallery, while hl, pl, and fb are employed as probe (or testing). Figure 5 presents sample views of an individual from the FERET database.

6.2 Experimental Results

6.2.1 Experiments on ORL Face Dataset

All experiments are done on 400 images from ORL database. A single-frontal face per person is utilized for training. To examine the efficiency of the proposed technique, two criteria viz. False Rejection Ratio and False Acceptance Ratio, are used. To calculate False Rejection Ratio, training image of a person is matched with all the 10 images of that person (total 400 (40 × 10) comparisons are done). To calculate False Acceptance Ratio, all the training images are compared with other 39 images in the model database (total 1560 (39 × 40) comparisons are done). Threshold is set accordingly to reject and accept the images. The results thus obtained are: False acceptance rate (FAR) = 29.23%; False rejection rate (FRR) = 30.25%.

One more test is done to find the recognition results for frontal views of face images. Only frontal faces are chosen from ORL dataset. Here, one/two faces per subject are utilized for training, while testing is done with three faces per subject. The recognition results for first, and fifth ranks are shown in Table 1. The outcome

Table 1 Recognition Results on ORL Facial Dataset

# Training images	Model gallery	Probe faces	EBGM Rank 1		Bi-SOM + AGM Rank 1		EBGM Rank 5		Bi-SOM + AGM Rank 5	
			#	%	#	%	#	%	# %	%
1	40	120	96	80.0	108	90.0	112	93.3	117	97.5
2	80	120	104	86.7	115	96.3	116	96.7	120	100

Table 2 Performance on FERET Dataset

Model gallery	Probe images	EBGM Rank 1		Bi-SOM + AGM Rank 1	
		#	%	#	%
250 fa	250 fb	245	98.0	249	99.6
250 hr	250 hl	143	57.2	163	65.3
250 pr	250 pl	210	84.0	220	88.0

of EBGM is calculated from the original code of Wiskott et al. [8].

6.2.2 Experiments on FERET Dataset

Further, experiments are conducted on the FERET facial dataset. From this, facial images with distinct poses are utilized for the experiments. The description of poses used in our experiments are as: face with frontal and natural expression (fa); frontal with distinct facial expression (fb); half-profile left (hl) and right (hr) (rotated by about 40°–70°); and profile left (pl) and right (pr). The total 250 faces are chosen where faces are with and without glasses. Experiments are performed in following three sets: (i) Trained the system on frontal with natural expression, while testing is performed by frontal face with varying expression (fa–fb), (ii) Another run executed with pose distinction, i.e., half-profile right and half-profile left facial images (hl–hr), and (iii) with right profile and left profile faces (pl–pr). The outcome of EBGM and Bi-SOM + AGM regarding recognition rate (rank first) is presented in Table 2.

6.3 Performance Analysis

For ORL facial dataset, the FAR and FRR are obtained approximately 10%. The reason for high value of FAR and FRR are due to images with varying poses and expressions. Training is done only using one image per person and so the probability of getting rejected of images with side poses is very high. It can be seen from the results that if images with frontal view are used for testing then it shows accuracy of 90%. If two faces per subject are applied for training, then maximum faces are recognized accurately and producing the recognition accuracy greater than 96% for rank one matching, and it is 100% for rank 5.

For frontal against frontal images from FERET, the recognition result is quite high (99.6%). However, due to the facial asymmetry in or half left and half right profiles, performance decreased sharply. Although, results for all the three poses, i.e., frontal view, half profile and profile as presented in Table 2 indicates that the proposed *Bi-SOM + AGM* performed better than the EBGM technique. Additionally,

the proposed *Bi-SOM + AGM* eliminates the manual labeling problem of EBGM required for identifying features.

7 Conclusions

In the present paper, a novel technique is proposed to solve the face recognition problem. The proposed technique utilizes the architectural characteristics of the self-organized neural network to proposed new Bi-Self-Organizing Map (Bi-SOM). Moreover, the existing graph matching technique is also modified to make them appropriate for our scenario, named as approximate graph matching (AGM). The inherited characteristics of SOM and AGM make the proposed technique robust to different variations in captured facial images such as poses, and expressions. As related to elastic bunch graph matching (EBGM) approach, the proposed Bi-Self-Organizing Map (Bi-SOM + AGM) approach also reduces the manual efforts. The proposed technique is fully automated and give better performance as compared to other methods.

The future work will concentrate toward making the system more robust for illumination changes, occlusion, pose variation, and low-resolution FR problem.

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Design of MEMS Phase Shifters for Phased Array Antenna Applications

E. K. Arunima Raj and E. S. Shajahan

1 Introduction

Advancements in phased array antenna systems have brought about major developments in military radars [1], mobile communications, and satellite broadcasting for space communications [2]. It would be interesting if we look down for a narrow electromagnetic frequency beam for communication with conventional satellites. Due to the antennas size and weight, it can be quite difficult and costly to track a moving obstacle. Phased arrays are composed of several smaller, fixed antennas. Each unit transmits signal by changing the relative phase and the combination of all these small signals produces a large focused beam. A phased array antenna system tracks an obstacle regardless of its movements, without any mechanical moving parts.

PAA are also extensively used for obtaining fixed as well as steerable beam patterns. Beam produced by the PAA is steered in required direction by fine-tuning of phase of individual antenna element [1]. Phased array antenna is flexible for receiving signals from different directions which does not contain any obstacles, and transmit to the preferred direction. The antenna elements are fed through a phase shifter in order to obtain steerable beam pattern. The comprehension of mechanical phase shifter is costly and bulky so they are not preferable for smaller electronic devices due to area constraint [2, 3].

The approach to enhance the performance of the antenna is by synthesis of the array antenna. The antenna array is obtained by integrating different antenna elements in an array format [4]. Patch antenna with coaxial feed and the microstrip line-based phase shifters are used in a wide range of applications including healthcare applications [5]. In the current scenario, antenna array are used in Wi-Fi and LTE technology [6]. Mobile phone uses several compact multi-band antenna designs which are the

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required characteristics of wireless devices. A bunched four-element linear phased array antenna with Wilkinson power divider as the feed technique is proposed [7, 8]. This work included the design of a phase shifter for a four elemental patch antenna array. This antenna could operate on 4.85 GHz. Entire plots are analyzed within the range of frequency 4–6.5 GHz which belongs to c-band, so this PAA is used for c-band applications. Our main intention is to construct a phase shifter small enough to fit within the antenna element, so that the proper realization is possible under each antenna unit.

As in switched-line phase shifter, input signal is fed to the antenna through the transmission line of different length which causes the signal captured by antenna on various times. Thus, a time delay is obtained in the switched-line phase shifter shown in [9] and [10]. A four-bit switched-line phase shifter recognition adopting microelectromechanical system is shown in [9] and in [10], and they described about constant phase shift produced between reference and phase shifter line. The phase shift produced by the extension of transmission lines with the help of switches is explained in this work.

The transmission lines are arranged in a circular trace around via which coaxial feed signal provided to the antenna. The measured results show that the four phases of 0°, 90°, 180°, and 270° should be achieved.

2 Design

A four-elemental rectangular patch antenna with coaxial feed is designed and simulated in high-frequency structural simulator (HFSS). All the antennas are identical in dimension as well as in structure. The antenna and the phase shifter are kept on a separate dielectric substrate with an air gap, contribute to a negligible error resulting from local reflections, and a great saving in solution time also [11]. The antenna designed for frequency 4.8 GHz, RogersRT/Duroid6006, is used as a dielectric substrate for an antenna with a relative permittivity of 6.15. The size of an antenna is inversely proportional to the dielectric constant, higher the dielectric constant causes to minimize the size of the antenna. The dielectric substrate for phase shifter is Duroid™ with a relative permittivity of 2.2, and 1.524 mm is the height of the dielectric substrate in both cases. 11.37 mm and 20.73 mm are the length and width of antenna, respectively [3]. The antenna elements as well as the phase shifter structures are implanted on a substrate with the length of 81 mm and width of 142 mm. The antenna elements are placed at a distance of half-wavelength apart. For obtaining high gain and reduced spurious effect, the phase shifter is kept on isolated from the antenna. With this design, the radiation pattern of the antenna is obtained in the desired direction with suppressed side lobes, and it also helps to reduce the false signals. In [10], they find out that the ration of the main lobe to the side lobes for an antenna with a separate feeding network which was double for an antenna on the same substrate, and values are: antenna with separate feeding network is −11.9 dB. The antenna and feed networks are placed on the same substrate resulted in −5.35 dB (Fig. 1).

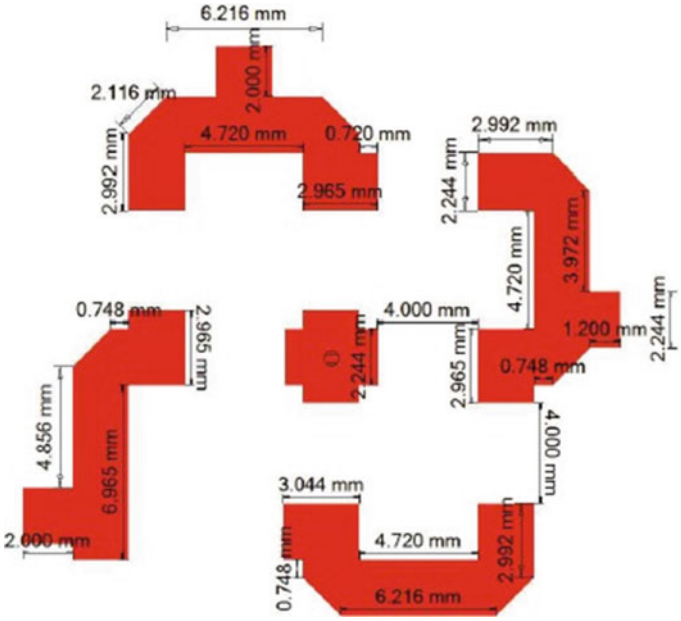

Fig. 1 Transmission line dimensions on a phase shifter [3]

2.1 Phase Shifter Structure with Wilkinson Power Divider Feed Network

The antenna and phase shifter is designed on different substrate, and phase shifters are placed under each antenna element through which the input signals are feeding. The Wilkinson power divider is used as feed network to the antenna through a phase shifter. The Wilkinson feed connected antenna array is shown in Fig. 2. The Wilkinson power divider/Wilkinson combiner separates input to provide two output signals which are in phase by splitting the applied input signal by using quarter wave transformers. The two output ports have resistance between them which provide isolation as well as facilitate the impedance match between two outcomes. The Wilkinson power divider resistance does not dissipate any power; hence, it is considered as theoretically loss less. The values within the Wilkinson power divider/combiner can be calculated using Eqs. (1) and (2).

It is necessary to ensure that the impedance within the Wilkinson power divider is maintained because of the power is being split. In order to achieve the above structure, represent phase shifter with Wilkinson's power divider along feed network. As the power is being split, it is necessary to ensure that the impedance with in Wilkinson's dividers are maintained. For achieving this, four output ports must appear as impedance of $4Z_o$ because they are in parallel will represent an overall impedance of Z_o. At the time of signal transformation, the feed impedance gets maintained.

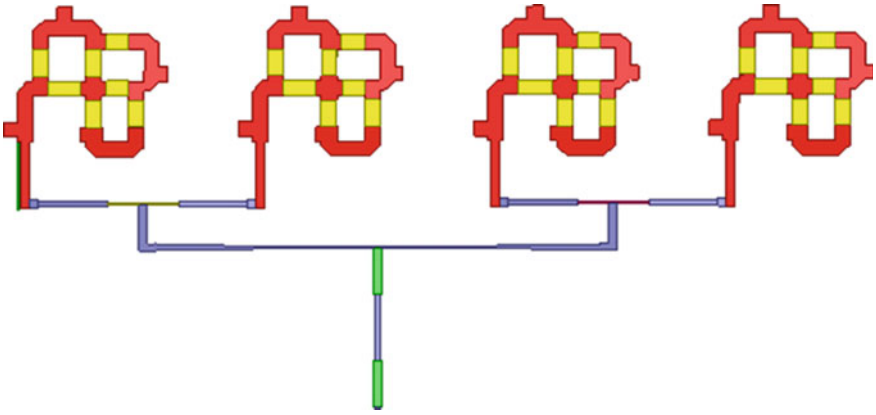

Fig. 2 Phase shifter structure with Wilkinson power divider feed network

$$R = 2Z_0 \tag{1}$$

$$Z_{\text{MATCH}} = \sqrt{2}Z_0 = 1.414Z_0 \tag{2}$$

R	The resistance value connected between two ports.
Z_o	Impedance characteristics of overall system.
Z_{MATCH}	Power divider impedance.

2.2 *Antenna Design*

Antenna receives the input signals which are phase shifted through contact at the center of the phase shifter. The antenna uses coaxial feed technique so as to easily combine with the input signal feed through the via where all traces of the transmission lines of the phase shifter are connected. The antenna is designed on the Rogers RT/Duroid 6006 substrate of thickness 1.524 mm. Patch antenna is on the top of the substrate, and by solving the equation given below, the antenna parameters are obtained.

$$\text{Width } (w) = \frac{C}{2f_{\text{r}}\frac{\sqrt{\varepsilon_r+2}}{2}} \tag{3}$$

$$\text{length } (l) = L_{\text{eff}} - 2\Delta L \tag{4}$$

$$L_{\text{eff}} = \frac{C}{2f_{\text{r}}\sqrt{\varepsilon_{\text{eff}}}} \tag{5}$$

The ground plane is situated in the bottom portion of the substrate. An inner conducting coaxial cable with a diameter '*a*' is starting from the patch antenna and ended at the contact, caused by penetrating through the substrate and ground. While there is an outer coaxial feed of diameter '*b*' surrounded by the inner conducting structure.

Here '*w*' and '*l*' are the width and length of the antenna, respectively, 'f_r' is the resonant frequency, and '*h*' is the thickness of the dielectric substrate (1.524 mm).The resonant frequency for the structure is 4.85 GHz. Solving Eqs. (3) and (4), the width dimension is found to be 11.2 mm, and the length of dimension 20.88 mm is obtained, respectively. Antenna dimensional parameters are shown in Fig. 3. Thus, the theoretical and simulated values are found in good agreement (Table 1).

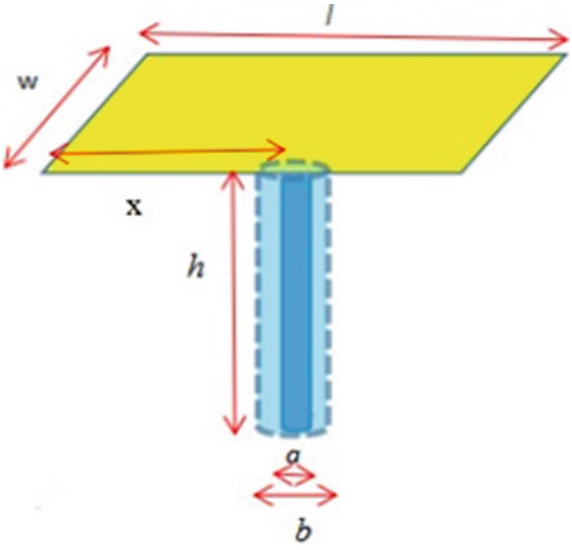

Fig. 3 Patch antenna with coaxial feed

Table 1 Patch antenna dimensional parameters

Parameters	Values (mm)
Width of the antenna (*w*)	10.81
Length of the antenna (*l*)	21.21
Distance between the patch and coaxial cable (*x*)	11.048
Height of the coaxial cable (*h*)	9.524
Diameter of the inner coaxial cable (*a*)	0.4
Diameter of the outer coaxial cable (*b*)	0.7

3 Simulation Results

The simulation and analysis of the phase shifter are done in Ansoft HFSS. The MEMS phase shifter is designed on dielectric substrate having the thickness of 1.524 mm.

Each phase shifter structure contains four arms of transmission lines, and the switches turn ON an OFF to produce 90° phase shift. The different combination of these transmission lines result in four-phase shifts such as, 0°, 90°, 180°, and 270°. Conducting rectangular sheets are provided as a lumped port for the input and output port of feed the network. Top view of the proposed phased array antenna is shown in Fig. 4, and the slant view is also shown in Fig. 5.

When MEMS bridges touch the dielectric layer on the application of an external excitation. So that it makes a connection between the ground and the transmission

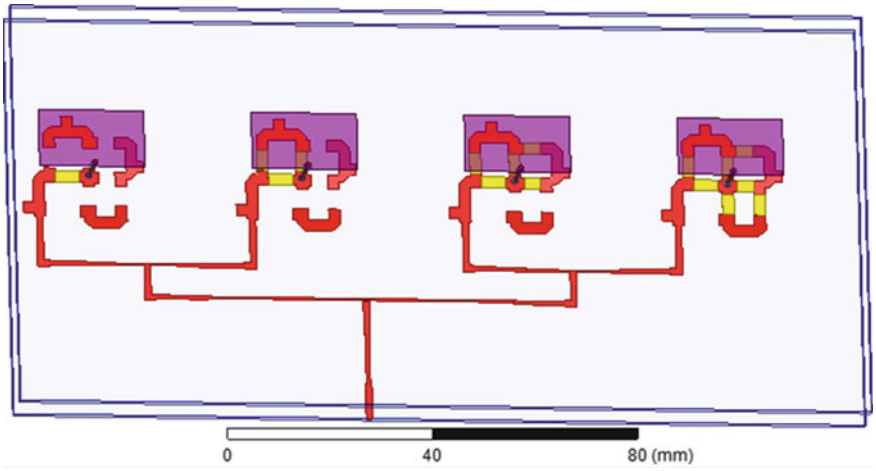

Fig. 4 Top view of the phased array antenna

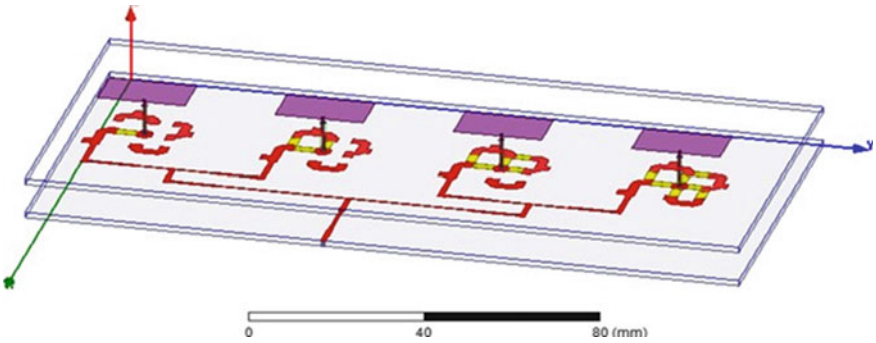

Fig. 5 Slant view of the phased array antenna

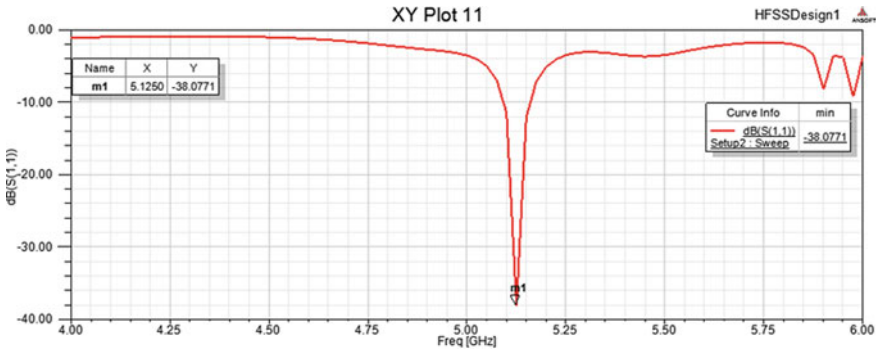

Fig. 6 S-parameter plot

line and acts as a short circuit which in turns varies the MEMS capacitance. This results in a change in impedance of the loaded transmission-line and phase velocity, which in turn causes the phase shift [12].

When simulating the entire designed structure, we obtain the reflection coefficient or S11 parameter as shown in Fig. 6 and the value nearly equal to -38.07 dB at frequency 5.25 GHz. The array antenna performance is very good within this array pattern; we obtain proper radiation also. The simulation in HFSS gives the plot between reflection coefficient (S11) in dB versus frequency in GHz, wrapped phase shifter in degree versus frequency in GHz, and unwrapped phase shifter in degree versus frequency in GHz. For each case of the phase shifter designed separately, analyze the results. While looking for the phase shift concept, simply explained as the structure, Fig. 7 shows each transmission line are of identical structure and get connected to the central via contacting strip denoted by yellow color. In the ON state, as the number of periodic elements increases, the insertion loss increases, and thus the delay of input signal increases. When the left most transmission line connected the via shows 0° phase shift which is the reference, then the next transmission line gets added to the existing structure with an ON state switch resulted in 90° phase shift. Then, adding second transmission line provides a phase shift of 90° which all together resulted in 180°, and similarly when the third transmission line gets added, it will also provide a phase shift of another 90 which all together contributed to a phase change of 270°. For each case of the phase shifter designed separately, analyze the results.

3.1 Scattering Parameters

The S11 graph represents the reflection coefficient or the scattering parameter. How much power is reflecting from an antenna is measured here, so it is called the reflection coefficient (γ) or return loss. When S11 = 0 dB, then nothing is radiated from the

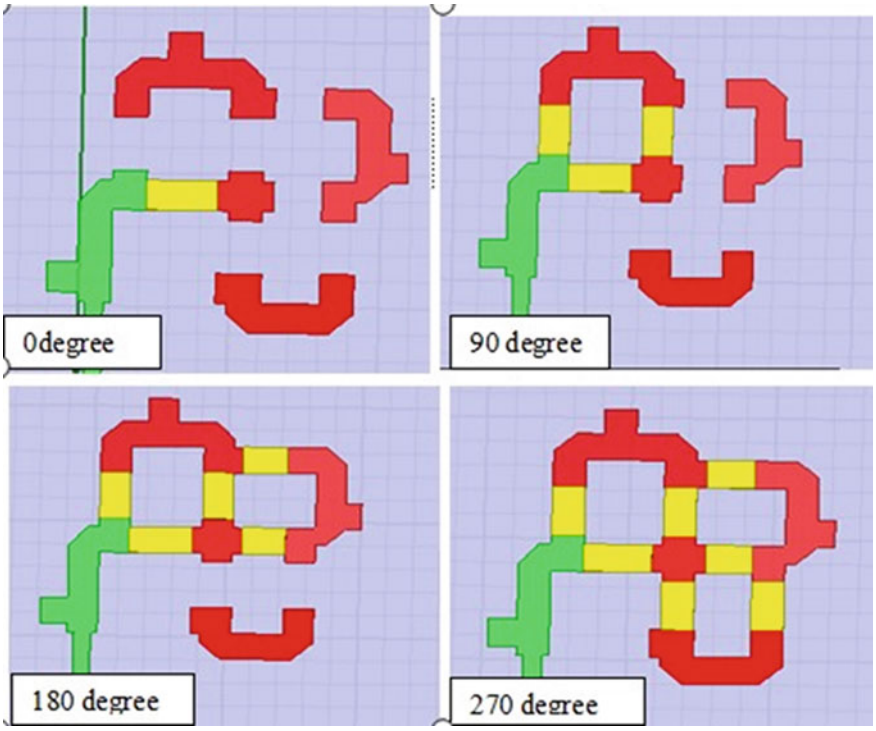

Fig. 7 Phase shifter with on and off state of the switch for each phase

antenna since all power is reflected. When the antenna is designed with low loss the total power remaining after reflection gets radiated. The peaks in the graph represent the frequency at which the input is radiated, and whenever the reflection coefficient increases in negative value, the radiation will be improved that much.

In the reflection coefficient as well as the frequency graph is given below in Fig. 8, the black line in the plot represents the graph for 0° and the reflection coefficient obtained for this phase shift is −1.3 dB, the green line in the plot represents the graph for 90° and the reflection coefficient obtained for this phase shift is −9.64 dB, the blue line in the plot represents graph for 180° and the reflection coefficient obtained for this phase shift is -12.98 dB, and the red line in the plot represents graph for 270°, and the reflection coefficient obtained for this phase shift is −18.96 dB where the radiation obtained is maximum.

3.2 Phase Shift Characteristics

All geometric structures constructed in HFSS have some inductance capacitance resistance values. For example, inductance opposes current due to back emf the

current reaches a peak value after voltage. Since the current and voltage no longer rises or fall together, there causes a phase shift in circuits which is the basis of phase shifter circuits constructed. The phase angle is the angle between the equivalent reactants and equivalent resistance of the circuit. It is an important parameter as it decides the power factor and power consumed. It can be plotted in two ways wrapped and unwrapped phase shifts.

In wrap phase shift characteristics, all phase values are concentrated to a range of −180° to +180°. Figure 9 shows that the addition of each transmission line gets contributed to a 90° phase shift. That is, in the first case, the red graph represents the reference value of 5.3489°, and by adding the first transmission line, we obtained a phase value of 93.5683° represented by the blue graph. The phase difference between this phase values resulted in −88.2194°. Again by adding the next transmission line, we obtain the value equal to 177.4695° given by the pink graph in the figure, and the phase shift obtained as −83.9012°. The last transmission line added will provide a value equal to 80.5034° given by the green graph. Then, the phase shift is about

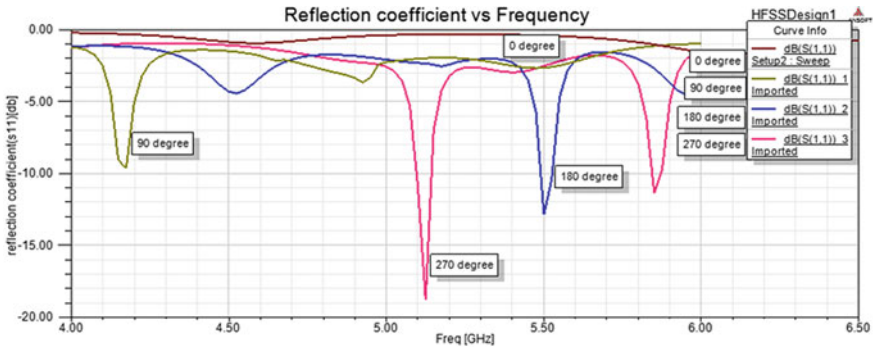

Fig. 8 Plot of scattering parameter versus frequency

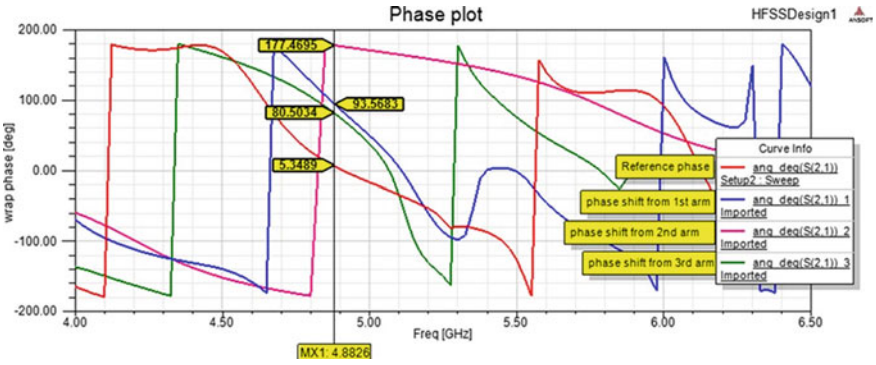

Fig. 9 Plot of wrap phase shift versus frequency

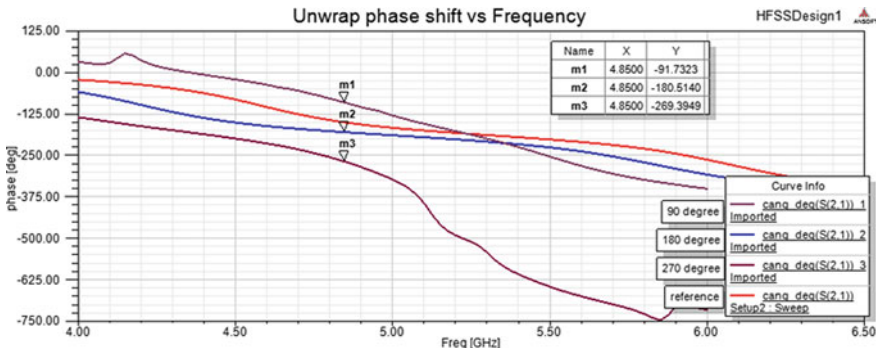

Fig. 10 Plot of unwrap phase shift versus frequency

96.9661°. All the responses are obtaining within the frequency 4.8826 GHz. Thus, in each case, a phase shift value nearly equal to 90° in magnitude is obtained.

3.3 Unwrap Phase Shift Plot

The phase values are unwrap with reference to the frequency axis. It represent actual phase shift of the circuit. In the phase shift versus frequency graph shown in Fig. 10, there is a reference phase given by the red plot. The brown graph shows a phase shift value of −91.732°, instead of −90°, and the blue graph represents −180.514°, instead of −180°, and the phase shifter shows −269.394°, instead of −270° denoted by the violet graph. All these values obtained at 4.85 GHz. The errors obtained are 1.732°, 0.514°, and 0.605°, respectively, for 90°, 180°, and 270°. In each of the cases, we obtained a negligible error, so the structure designed almost in a precise manner.

3.4 Radiation Pattern

Radiation pattern shows how strongly antenna radiate in particular direction. The corresponding 3D and 2D radiation pattern for designed structure is represented in Figs. 11 and 12, respectively.

When a single-phase shifter structure attached to an antenna element is considered, the gain value obtained is 1.5373 dB. When it becomes two antenna structure feed through two phase shifters separately then gain increased to 3.6065 dB and so on. Fig. 13 gives the gain for designed phased array antenna with a maximum value of 9.3966 dB. The periodic cascading of the unit elements will represent an improved gain is given in Table 2.

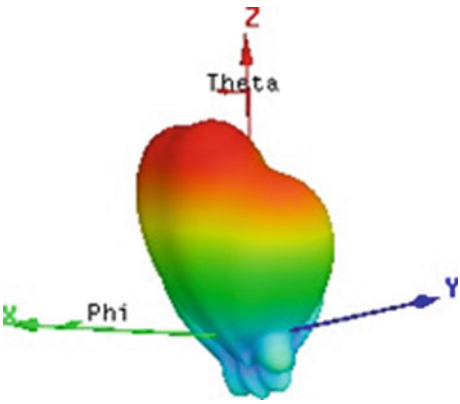

Fig. 11 3D radiation pattern of designed phase shifter

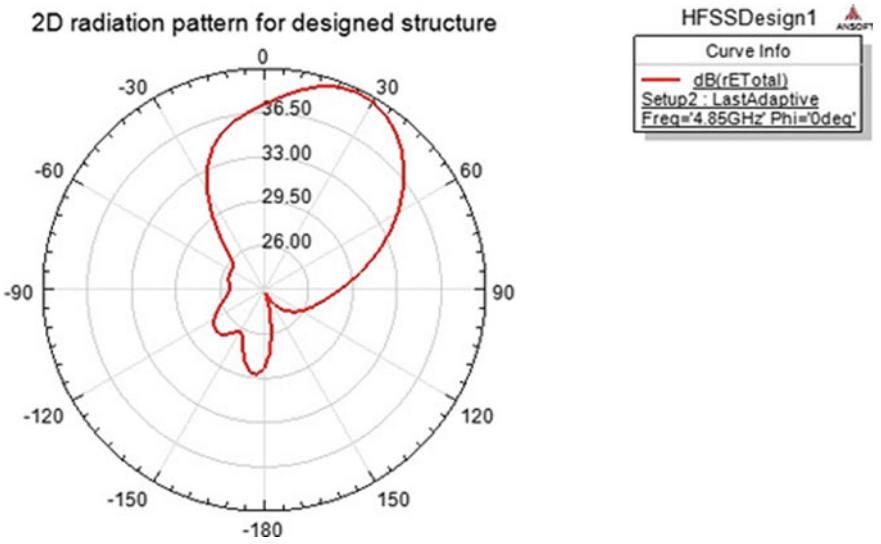

Fig. 12 2D radiation pattern of designed phase shifter

The 2D radiation pattern observed with each phase shifting values is represented in Fig. 14.The steering of beam pattern is obtained for each phase shift is combined together in Fig. 15, which separately represent the radiation pattern for 0°, 90°, 180°, and 270° phase shift values. The beam steering angle is calculated using Eq. (6),

$$\Delta\varphi = \frac{2 \times \pi \times d \times \sin\theta}{\lambda} \tag{6}$$

where

λ Wavelength.

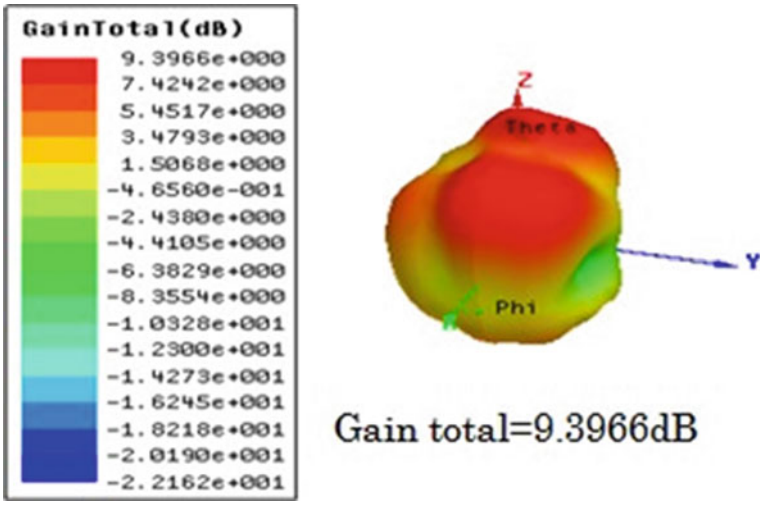

Fig. 13 Gain of designed phase shifter

Table 2 Comparison of gain

Number of antenna element in a phased array	Gain total in dB
1 antenna	1.5373
2 antenna	3.6065
4 antenna	9.3966

θ The phase shift provided.
$\Delta\varphi$ Beam steering angle.
D Distance between antenna element.

Here, we come up with MEMS switches for tuning because they have some advantages over PIN diodes, such as higher quality factor, lower insertion loss, lower noise figure, higher linearity, lower power losses, and very little DC power consumption. Recent advances in MEMS technology enable the realization of MEMS with improved switching speed and compact size. The MEMS switches and PIN diodes were found to provide comparable performance in on-state configuration, while MEMS switches were more robust in off-state, high-powered operation, and they also provide higher isolation. So MEMS switching has more advantages over other tuning methods.

4 Conclusion

The designed phase shifter for antenna array performance not only met the design expectation but also produce good results. When each transmission line traces of

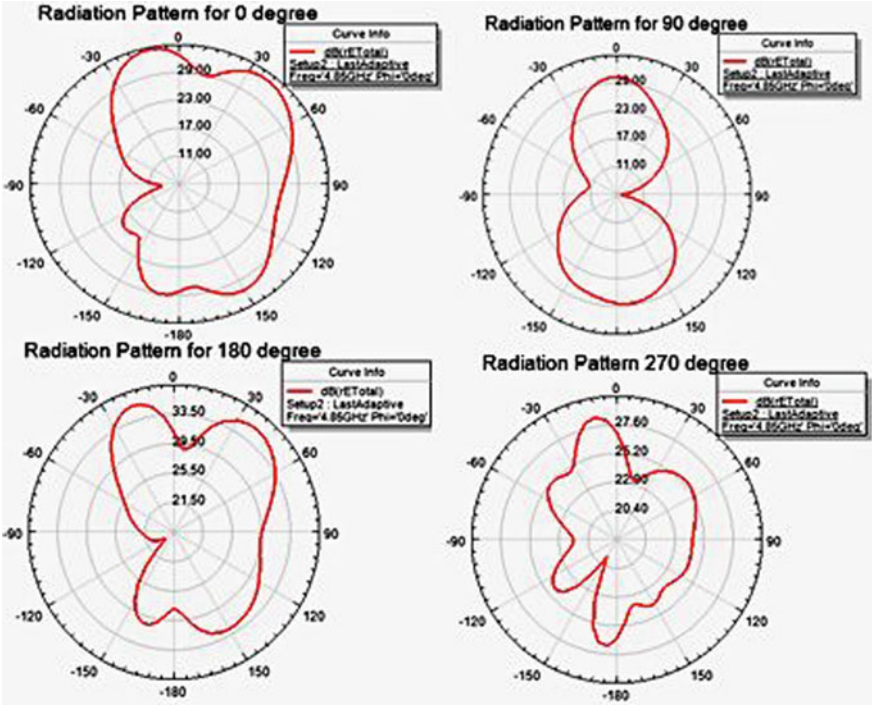

Fig. 14 D radiation pattern for different phase shifts

phase shifter added to the provided reference line and phase shift values near to 90° with a minimum reflection is obtained. So we obtain 0°, 90°, 180°, and 270°, respectively while adding each transmission line traces with connecting to an ON switch. A beam steering was obtained at the desired frequency band. All plots such as scattering parameter versus frequency, phase shift versus frequency are obtained within the range of frequency 4–6.5 GHz at c-band. So this design is very useful to characterize the phased array antenna in c-band applications. The design of the phase shifter done in order to fit within the space of antenna elements, and this is also very useful for small electronic devices that contain antenna elements which have area constraint. The simulation also resulted in proper beam steering as well as the narrow beam production of the field towards the desired direction. This phase shifting method can be used for directional beam pattern required Wi-Fi applications, TV stations, smart antenna, MIMO communications, radar scanning, beam steering technologies, etc.

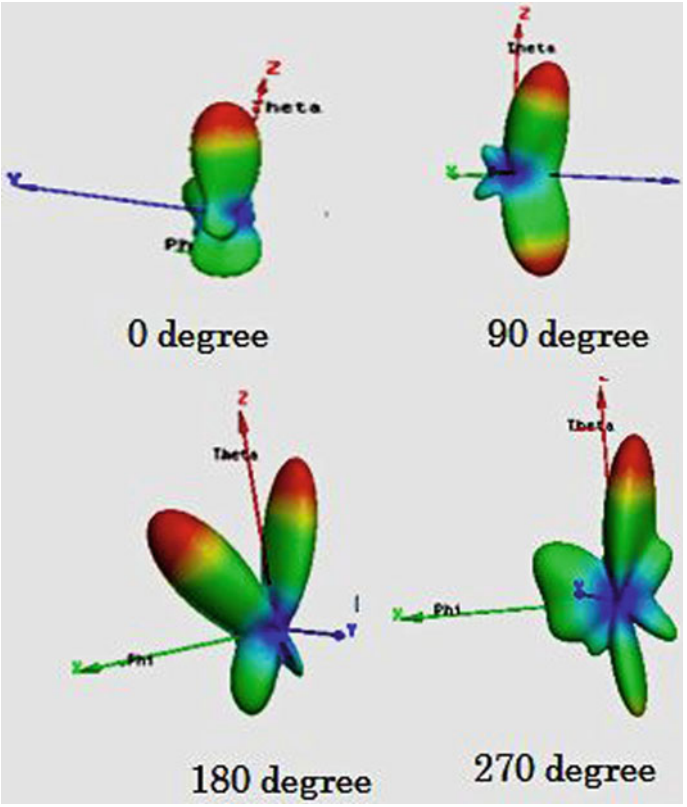

Fig. 15 Radiation pattern for different phase shifts

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Sierpinski Fractal-Based Ceramic Antenna for Wideband Applications

Kapil Gangwar, Anand Sharma, and Ravi Kumar Gangwar

1 Introduction

Current advancements of technology in cellular communication mainly focus on high-speed data rates. Dielectric radiator antennas play a vital role to yield wideband applications for microwave and mm-wave frequency range. The height and radius of the cylindrical dielectric resonator decide the resonating frequency [1]. Advantages of using dielectric resonator comprised of no conductor and surface wave losses, stable radiation pattern, lighter weight, lower fabrication complexity, and circular polarization [2, 3]. Higher-order radiating modes and reduction in volume-to-surface ratio are some of the predominant techniques to accomplish wideband characteristics [4].

Fractal geometry is a self-similar pattern which has manifested to be convenient for enhancing the wide impedance bandwidth. This concept is suitable to combine the two technique, i.e., reduction in Q-factor and descending higher-order modes frequency spaces [5]. Gangwar et al. proposed DRA conferred the wideband application used a rectangular shaped fractal design with an operating bandwidth of 18.44% [6]. Hajihashemi and Abiri were the researchers who presented wideband fractal Koch Island geometry-based DRA yielding ∼26.4% bandwidth [7]. Introductory investigation on Sierpinski fractal geometry-based dielectric resonator antenna was proposed by Prof. Ghatak providing 31.1% impedance bandwidth [8]. Pixelated [9]

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and Minkowski [10] fractal geometry is also formerly used to build DRA producing 32.32% and 32.64% bandwidth, respectively.

In this paper, Sierpinski fractal geometry-based cylindrical and ring dielectric resonator antenna is proposed. Radiating modes and reduction in volume-to-surface ratio coalesce to expound the wide impedance bandwidth behavior using fractal design methodology. The proposed radiator design works in the frequency range of 2.45–3.55 GHz.

2 Aerial Structure and Design

The geometrical arrangement of the proposed fractal radiator is shown in Fig. 1. The cylindrical and ring resonators are made up of alumina material having dielectric constant of 9.8 and loss tangent of 0.002. The parental cylindrical DRA radius ($R1$) and height (H) are 25 mm and 13.0 mm correspondingly. It is fed with a coaxial probe of height 11.4 mm. Initially, this DRA is placed on the copper ground plane having a depth ($H1$) of 1.6 mm and diameter (R) of 150.0 mm. The parental DRA center is placed at the distance (D) of 13.0 mm from the center of the ground plane. The radius ($R2$) of the first iteration ring resonators is 19.0 mm.

The radius ($R3$) of the second iteration ring resonators is 15.0 mm. The radius ($R4$) of the third iteration is 11.0 mm. The thickness (D) and height (H) of all the ring resonators are 3.0 mm and 13.0 mm, respectively.

3 Outcomes and Its Analysis

This section shows the simulated results of the proposed fractal-based DRA. Figure 2 shows simulated S11 with respect to frequency for all the iteration used in the proposed antenna design. From Fig. 2, it can be noticed that the operational bandwidth increases for each iteration till third iteration which works over the frequency range of 2.45–3.55 GHz. Figure 3a, b shows the far-field of the proposed Ariel at 2.75 GHz in both principal plane, respectively. At 2.25 GHz, diversified radiation pattern characteristics are being observed for the third iteration fractal antenna.

Peak gain (simulated) and radiation efficiency (simulated) as a function of frequency are shown by Fig. 4. It can be stated that the maximum value of gain is ~6.18 dBi. The radiation efficiency is about 90% in the working frequency range.

Table 1 presents comparison with reference to shape, bandwidth, and fabrication complexity for the proposed antenna geometry with some previously designed fractal-based antenna geometries. From Table 1, it can be observed that the projected

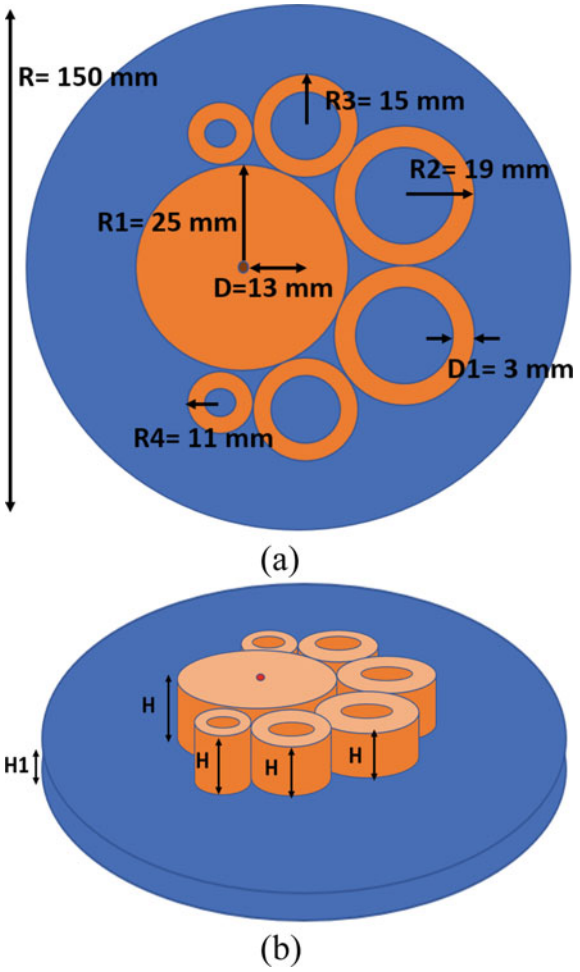


Fig. 1 Ariel design: **a** Upper view, **b** Isometric vision

fractal radiator geometry exceeds in bandwidth and fabrication complexity properties contrast to previously designed antenna structures based on fractal design methodology.

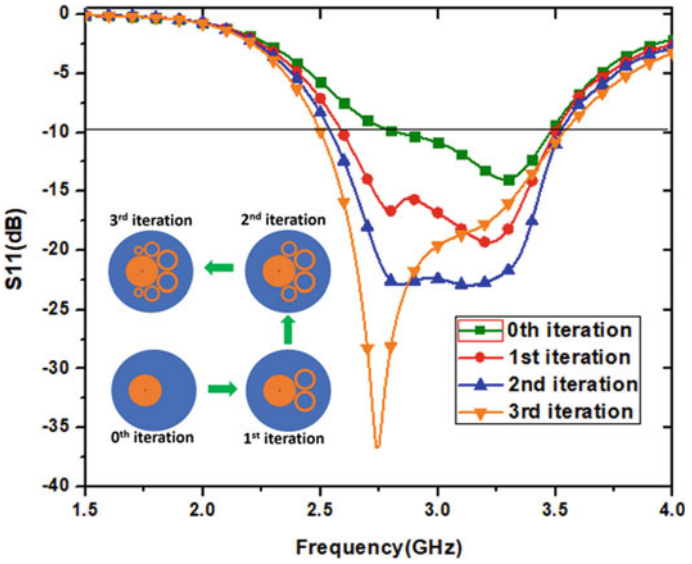
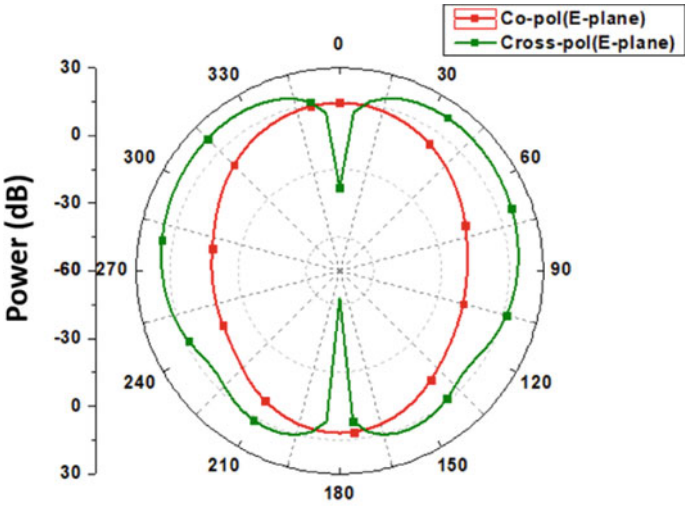


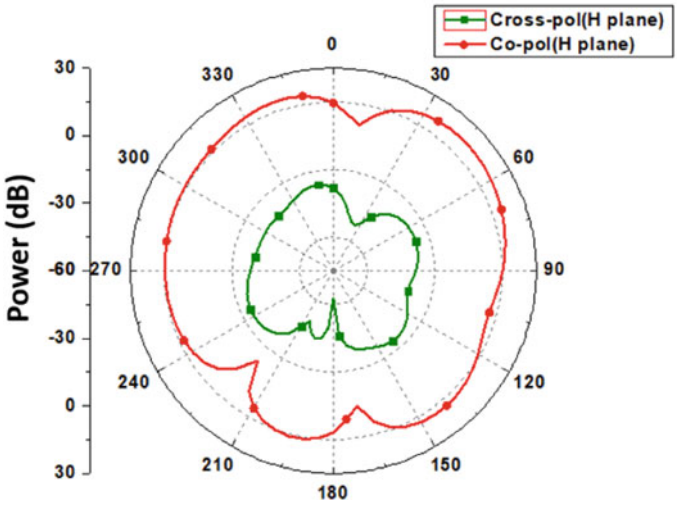
Fig. 2 S11 (simulated) variation with respect to frequency for all iterations used in proposed antenna geometry

4 Conclusion

In this article, a Sierpinski fractal-based cylindrical and ring dielectric resonator antenna have been presented. The antenna provides the wideband characteristics by compounding two techniques: generation of higher-order radiating modes and reduction in volume-to-surface ratio. The proposed fractal antenna works in the frequency range of 2.45–3.55 GHz having a maximum gain of 6.18 dBi. The proposed antenna can be efficiently used for WLAN (2.5 GHz) and WiMAX (3.3 GHz) applications.



(a) E-plane radiation pattern



(b) H-plane radiation pattern

Fig. 3 Radiation pattern (simulated) at 2.75 GHz: **a** E-plane, **b** H-plane

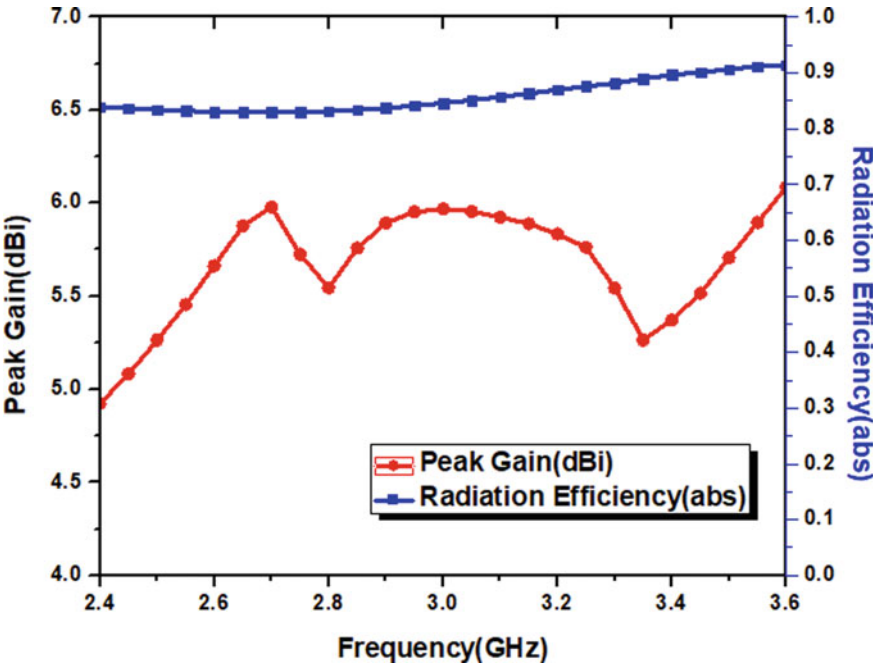


Fig. 4 Peak Gain (simulated) and radiation efficiency (simulated) as a function of frequency

Table 1 Comparison with reference to shape, bandwidth, and fabrication complexity for the proposed antenna geometry with some previously designed fractal-based antenna geometries

Fractal geometry	DRA shape	Bandwidth (%)	Fabrication complexity
Square [6]	Rectangular	18.44	High
Koch island [7]	Rectangular	26.4	Very high
Modified square [8]	Rectangular	31.10	Very high
Pixelated [9]	Rectangular	32.32	Very high
Minkowski [4]	Triangular	32.64	Low
Proposed	**Cylindrical**	**36.66**	**Low**

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Further Results on Delay-Dependent Stability Analysis of Uncertain Discrete-Time Systems Exerting Generalized Overflow Nonlinearities and Time-Varying Delays

Pushpendra Kumar Gupta, Kalpana Singh, and V. Krishna Rao Kandanvli

1 Introduction

When a category of discrete-time systems (DTS) are realized using fixed-point arithmetic via computer or digital hardware, nonlinearities (quantization/overflow) are encountered due to finite wordlength effects [1–13]. There is a chance of instability in the designed DTS due to such nonlinearities [1–13]. One can neglect the quantization effects if the size of quantization step is small and considered only overflow effects [1, 3–5, 7–13].

Besides nonlinearities, time delays are another factor that makes the system unstable. Time delays occurred in many practical engineering systems such as neural network [14], robust control system [15], sensor network [16], multi-path communication system, Markovian jump system [17], etc. Several results are reported in the literature on the stability issues concerning to the systems with constant delay [3, 4, 7, 8, 10, 18–20] and systems in presence of time-varying delay (TVD) [6, 7, 9, 14, 17, 21–23]. While dealing with the TVD in the DTS, it is often that one must find the upper delay bound (UDB) for the given lower delay bound (LDB) so that the system is stable. One can achieve less conservative stability results by selecting proper Lyapunov–Krasovskii function (LKF) and/or tighter estimation on the sum and cross term of the forward difference (FD) of the LKF. Several techniques are available to handle the sum and cross terms of the FD of the LKF such as Free weighting matrix [7], Jensen inequality [9], Wirtinger-based inequality [6, 8, 24] and Reciprocal convex lemma [6, 21], etc.

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Another factor that may lead the system toward instability is parameter uncertainty (PU) and the effects of PU is extensively studied in [3, 4, 6–10, 15, 18–20, 25].

To the best of author's knowledge, very few results are available in the literature concerning to the stability analysis of DTS involving TVD, PU and generalized overflow nonlinearities (GON) [3, 7, 9]. The criterion in [3] is delay-independent and the criteria in [7, 9] are delay-dependent. In general, delay-independent criterion provides more conservativeness than delay-dependent criterion. For handling the sum and cross term of the FD of the LKF, free weighting matrix method is used in [7], whereas Jensen's inequality is employed in [9]. The Wirtinger inequality [6, 24] and Reciprocal convex lemma [6, 21] are used in this paper to this end. The development of the stability criterion with less conservativeness and computational complexity for the DTS in presence of TVD, parameter uncertainties and GON is an important and challenging task. Motivated by the above discussion, in this paper, we focus on the global asymptotic stability (G.A.S.) problem for the DTS with TVD, parameter uncertainties and GON.

The organization of the remaining paper is as follows. In Sect. 2, the system under investigation is described while, in Sect. 3, two new computationally tractable delay-dependent criteria are proposed. In Sect. 4, three examples are provided to show the efficacy and improvement over previously reported criteria. Finally, concluding statements of the paper is given in Sect. 5.

Notations: Throughout the paper, $\mathbb{R}^{\alpha\times\beta}$ stands for the set of real $\alpha \times \beta$ matrices. $\mathbb{R}^{\alpha}$ represents the set of real $\alpha \times 1$ vectors. $\boldsymbol{Z}^T$ stands for the transpose of the $\boldsymbol{Z}$ matrix. $\boldsymbol{Z} > \mathbf{0}$ and $\boldsymbol{Z} < \mathbf{0}$ means that $\boldsymbol{Z}$ is positive and negative definite symmetric matrix, respectively. $*$ symbol infers the symmetric terms of a symmetric matrix. The diagonal matrix with diagonal elements $g_1, g_2,\ldots, g_n$ is represented by *diag* $(g_1, g_2,\ldots, g_n)$. $\mathbf{0}$ is null matrix or null vector of suitable dimension. $\mathbf{I}$ is the identity matrix of compatible dimension.

2 System Description

The system under consideration is given by

$$\begin{aligned} \boldsymbol{w}(u+1) &= \boldsymbol{\lambda}(\boldsymbol{z}(u)) \\ &= [\lambda_1(z_1(u))\,\lambda_2(z_2(u))\ldots\lambda_n(z_n(u))]^T \end{aligned} \tag{1a}$$

$$\begin{aligned} \boldsymbol{z}(u) &= \overline{\mathbf{A}}\boldsymbol{w}(u) + \overline{\mathbf{A}}_{\mathbf{d}}\boldsymbol{w}(u-h(u)) \\ &= [z_1(u)\,z_2(u)\ldots z_n(u)]^T \end{aligned} \tag{1b}$$

$$\boldsymbol{w}(u) = \boldsymbol{\varphi}(u), \forall u \in [-d_2, 0] \tag{1c}$$

$$\overline{\mathbf{A}} = \mathbf{A} + \Delta\mathbf{A},\ \overline{\mathbf{A}}_d = \mathbf{A}_d + \Delta\mathbf{A}_d \tag{1d}$$

where $\boldsymbol{w}(u) \in \mathbb{R}^n$ is the state variable; $\mathbf{A}$, $\mathbf{A_d} \in \mathbb{R}^{n\times n}$ are the known constant matrices; the unknown matrices $\Delta\mathbf{A}$, $\Delta\mathbf{A_d} \in \mathbb{R}^{n\times n}$ representing parametric uncertainties in $\mathbf{A}$, $\mathbf{A_d}$, respectively; the initial state value at time u is $\boldsymbol{\varphi}(u) \in \mathbb{R}^n$.

The characteristic of GON is specified by [1, 3, 5, 7–9]

$$\left.\begin{array}{ll} L \le \lambda_i(z_i(u)) \le 1, & z_i(u) > 1 \\ \lambda_i(z_i(u)) = z_i(u), & -1 \le z_i(u) \le 1 \\ -1 \le \lambda_i(z_i(u)) \le -L, & z_i(u) < -1 \end{array}\right\} i = 1, 2, 3 \ldots n \tag{2a}$$

where

$$L \in [-1, 1] \tag{2b}$$

With applicable choice of L, (2) represents the usual types of overflow arithmetic employed in practice, such as zeroing ($L = 0$), saturation ($L = 1$), triangular ($L = -1$) and two's complement ($L = -1$), etc., and the TVD $h(u)$ satisfying

$$1 \le d_1 \le h(u) \le d_2 \tag{3}$$

where d_1 is the LDB and d_2 is the UDB. The parameter uncertainties in the state matrices are of the following form

$$\Delta\mathbf{A} = \boldsymbol{H}_0\mathbf{F}_0\boldsymbol{E}_0 \tag{4a}$$

$$\Delta\mathbf{A_d} = \boldsymbol{H}_1\mathbf{F}_1E_1 \tag{4b}$$

where $\boldsymbol{H_i} \in \mathbb{R}^{n\times p_i}$, $\boldsymbol{E_i} \in \mathbb{R}^{q_i\times n}$ $(i = 0, 1)$ are known constant matrices and $\mathbf{F_i} \in \mathbb{R}^{p_i\times q_i}(i = 0, 1)$ is an unknown matrix which satisfies

$$\mathbf{F_i}^T\mathbf{F_i} \le \mathbf{I},\ i = 0, 1. \tag{4c}$$

Equations (1)–(4) is helpful to represent many practical engineering problems like fixed-point processor used in digital control systems, Hopfield neural networks, Sensor networks with finite word length register, cold rolling mills. Network control system is also an example of discrete-time system represented by (1)–(4), where generated delay is time-varying which may be induced due to network transmission.

The following lemmas are useful in obtaining our main results.

Lemma 1 [6, 24] For a given matrix $\mathbf{0} < \boldsymbol{N} = \boldsymbol{N}^T$ and three non-negative integers

b_1, b_2, u, as $b_1 \le b_2 \le u$, if

$$\boldsymbol{\zeta}(u, b_1, b_2) = \frac{1}{b_2 - b_1}\left[\left(2\sum_{k=u-b_2}^{u-b_1-1} \boldsymbol{w}(k)\right) + \boldsymbol{w}(u-b_1) - \boldsymbol{w}(u-b_2)\right],\ b_1 < b_2$$
$$= 2\boldsymbol{w}(u-b_1),\ b_1 = b_2 \tag{5}$$

then

$$-(b_2 - b_1)\sum_{k=u-b_2}^{u-b_1-1} \boldsymbol{\xi}^{\mathrm{T}}(k)\boldsymbol{N}\boldsymbol{\xi}(k) \le -\begin{bmatrix}\boldsymbol{\theta}_0 \\ \boldsymbol{\theta}_1\end{bmatrix}^{\mathrm{T}}\begin{bmatrix}\boldsymbol{N} & \mathbf{0} \\ \mathbf{0} & 3\boldsymbol{N}\end{bmatrix}\begin{bmatrix}\boldsymbol{\theta}_0 \\ \boldsymbol{\theta}_1\end{bmatrix} \tag{6}$$

where

$$\boldsymbol{\theta}_0 = \boldsymbol{w}(u-b_1) - \boldsymbol{w}(u-b_2) \tag{7}$$

$$\boldsymbol{\theta}_1 = \boldsymbol{w}(u-b_1) + \boldsymbol{w}(u-b_2) - \boldsymbol{\zeta}(u, b_1, b_2) \tag{8}$$

$$\boldsymbol{\xi}(k) = \boldsymbol{w}(k+1) - \boldsymbol{w}(k) \tag{9}$$

Lemma 2 [3, 4, 6–10, 15, 18–20, 25] Let $\boldsymbol{U}$, Λ, Θ and $\boldsymbol{\Xi}$ be matrices (real) of suitable dimensions with $\boldsymbol{\Xi} = \boldsymbol{\Xi}^{\mathrm{T}}$, then

$$\boldsymbol{\Xi} + \mathbf{U}\,\Theta\,\boldsymbol{\Lambda} + \boldsymbol{\Lambda}^{\mathrm{T}}\,\Theta^{\mathrm{T}}\,\mathbf{U}^{T} < \mathbf{0} \tag{10}$$

for all $\Theta^{\mathrm{T}}\Theta \le \mathbf{I}$, if there exists a positive scalar ε such that

$$\boldsymbol{\Xi} + \varepsilon^{-1}\,\mathbf{U}\,\mathbf{U}^{\mathrm{T}} + \varepsilon\ \boldsymbol{\Lambda}^{\mathrm{T}}\,\boldsymbol{\Lambda} < \mathbf{0} \tag{11}$$

Lemma 3 [4, 5, 8, 13] Consider the matrix $\boldsymbol{C} = [c_{\alpha\beta}] \in \mathbf{R}^{n\times n}$ is given by

$$c_{\alpha\alpha} = \sum_{\beta=1,\,\beta\neq\alpha}^{n} (\xi_{\alpha\beta} + \psi_{\alpha\beta}),\quad \alpha = 1, 2 \ldots n \tag{12a}$$

$$c_{\alpha\beta} = L(\xi_{\alpha\beta} - \psi_{\alpha\beta}),\ \alpha, \beta = 1, 2, \ldots n\ (\alpha \neq \beta) \tag{12b}$$

$$\xi_{\alpha\beta} > 0,\ \psi_{\alpha\beta} > 0,\ \alpha, \beta = 1, 2, \ldots n\ (\alpha \neq \beta) \tag{12c}$$

$$L \in [0, 1] \tag{12d}$$

(for $n = 1$, $\boldsymbol{C}$ turn into a positive scalar)**,** then

$$\sum_{\alpha=1}^{n} 2[z_\alpha(u) - \lambda_\alpha(z_\alpha(u))]\left[\sum_{\beta=1,\,\beta\neq\alpha}^{n} (\xi_{\alpha\beta} + \psi_{\alpha\beta})\lambda_\alpha(z_\alpha(u)) + L(\xi_{\alpha\beta} - \psi_{\alpha\beta})\lambda_\beta(z_\beta(u))\right]$$
$$= z^{\mathrm{T}}(u)\boldsymbol{C}\boldsymbol{\lambda}(z(u)) + \boldsymbol{\lambda}^{\mathrm{T}}(z(u))\boldsymbol{C}^{\mathrm{T}}z(u) - \boldsymbol{\lambda}^{\mathrm{T}}(z(u))(\boldsymbol{C} + \boldsymbol{C}^{\mathrm{T}})\boldsymbol{\lambda}(z(u)) \geq 0 \tag{13}$$

where $\boldsymbol{\lambda}(z(u))$ is given by (2a) and (12d).

Lemma 4 [4, 5, 8, 12] Consider $\boldsymbol{D}$= *diag* $(g_1, g_2,\ldots, g_n) > \boldsymbol{0}$. Then, concerning to (2a) and $L \in [-1, 0)$, the relation given below is fulfilled.

$$\sum_{k=1}^{n} 2d_k[z_k(u) - \lambda_k(z_k(u))]\,[-Lz_k(u) + \lambda_k(z_k(u))]$$
$$= (1 + L)z^{\mathrm{T}}(u)\boldsymbol{D}\boldsymbol{\lambda}(z(u)) + (1 + L)\boldsymbol{\lambda}^{\mathrm{T}}(z(u))\boldsymbol{D}z(u)$$
$$- 2\boldsymbol{\lambda}^{\mathrm{T}}(z(u))\boldsymbol{D}\boldsymbol{\lambda}(z(u)) - 2Lz^{\mathrm{T}}(u)\boldsymbol{D}z(u) \geq 0 \tag{14}$$

Lemma 5 [6, 21] For any vectors $\boldsymbol{\chi}_1$ and $\boldsymbol{\chi}_2$, matrices $\boldsymbol{P}$, $\boldsymbol{Q}$ and real numbers $a_1 \geq 0$,$a_2 \geq 0$ fulfills

$$\begin{bmatrix} \boldsymbol{P} & \boldsymbol{Q} \\ * & \boldsymbol{P} \end{bmatrix} \geq 0,\ a_1 + a_2 = 1 \tag{15}$$

$$\chi_i = 0,\ \text{if } a_i = 0 (i = 1, 2) \tag{16}$$

then

$$-\frac{1}{a_1}\boldsymbol{\chi}_1^T\boldsymbol{P}\boldsymbol{\chi}_1 - \frac{1}{a_2}\boldsymbol{\chi}_2^T\boldsymbol{P}\boldsymbol{\chi}_2 \leq -\begin{bmatrix} \boldsymbol{\chi}_1 \\ \boldsymbol{\chi}_2 \end{bmatrix}^T\begin{bmatrix} \boldsymbol{P} & \boldsymbol{Q} \\ * & \boldsymbol{P} \end{bmatrix}\begin{bmatrix} \boldsymbol{\chi}_1 \\ \boldsymbol{\chi}_2 \end{bmatrix} \tag{17}$$

Remark 1 In this paper, for covering the entire range of L, i.e., $-1 \leq L \leq 1$ (see in (2b)), two ranges of L are considered and these two ranges are $0 \leq L \leq 1$ and $-1 \leq L < 0$.

3 Main Results

This section contains two delay-dependent sufficient stability conditions (i.e., Theorems 1 and 2). Theorem 1 is valid for to the case where $L \in [0, 1][0, 1]$ and Theorem 2 is applicable for $L \in [-1, 0)$.

Theorem 1 For known integers d_1 and d_2 with $d_2 \geq d_1 \geq 1$, the DTS (1), (2a), (3), (4) is globally asymptotically stable (GAS) if there are suitable mensioned matrices $\boldsymbol{0} \prec \boldsymbol{G} = \begin{bmatrix} \boldsymbol{G}_1 & \boldsymbol{G}_2 & \boldsymbol{G}_3 \\ * & \boldsymbol{G}_4 & \boldsymbol{G}_5 \\ * & * & \boldsymbol{G}_6 \end{bmatrix} = \boldsymbol{G}^T$, $\boldsymbol{0} < \boldsymbol{M}_i = \boldsymbol{M}_i^T$ $(i = 1, 2, 3)$, any matrix $\boldsymbol{W} =$

$\begin{bmatrix} \boldsymbol{W}_{11} & \boldsymbol{W}_{12} \\ \boldsymbol{W}_{21} & \boldsymbol{W}_{22} \end{bmatrix}$, positive scalars ε_0,ε_1 and $L \in [0, 1]$ such that

$$\begin{bmatrix} \boldsymbol{N}_2 & \mathbf{0} & \boldsymbol{W}_{11} & \boldsymbol{W}_{12} \\ * & 3\boldsymbol{N}_2 & \boldsymbol{W}_{21} & \boldsymbol{W}_{22} \\ * & * & \boldsymbol{N}_2 & \mathbf{0} \\ * & * & * & 3\boldsymbol{N}_2 \end{bmatrix} > \mathbf{0} \tag{18}$$

and satisfying the following:

$$\boldsymbol{\Psi}(h(u) = d_1) < \mathbf{0} \tag{19a}$$

$$\boldsymbol{\Psi}(h(u) = d_2) < \mathbf{0} \tag{19b}$$

where

$$\boldsymbol{\Psi}(h(u)) = \begin{bmatrix} \boldsymbol{\Gamma}_{11} + \varepsilon_0 \mathbf{E}_0^T \mathbf{E}_0 & \mathbf{0} & (\boldsymbol{G}_3 - \boldsymbol{G}_2)/2 - 2\boldsymbol{N}_1 & -\boldsymbol{G}_3/2 & \boldsymbol{\Gamma}_{15} + 3\boldsymbol{N}_1 \\ * & \boldsymbol{\Gamma}_{12} + \varepsilon_1 \mathbf{E}_1^T \mathbf{E}_1 & \boldsymbol{\Gamma}_{23} & \boldsymbol{\Gamma}_{24} & \mathbf{0} \\ * & * & -\boldsymbol{M}_1 - 4(\boldsymbol{N}_1 + \boldsymbol{N}_2) & \boldsymbol{\Gamma}_{34} & \boldsymbol{\Gamma}_{35} + 3\boldsymbol{N}_1 \\ * & * & * & -\boldsymbol{M}_2 - 4\boldsymbol{N}_2 & -d_1 \boldsymbol{G}_5^T/2 \\ * & * & * & * & -3\boldsymbol{N}_1 \\ * & * & * & * & * \\ * & * & * & * & * \\ * & * & * & * & * \\ * & * & * & * & * \\ * & * & * & * & * \end{bmatrix}$$

$$\begin{bmatrix} \boldsymbol{\Gamma}_{16} & \boldsymbol{\Gamma}_{17} & \boldsymbol{\Gamma}_{18} + \boldsymbol{G}_2^T/2 + \mathbf{A}^T C & \mathbf{0} & \mathbf{0} \\ \boldsymbol{\Gamma}_{26} & \boldsymbol{\Gamma}_{27} & \mathbf{A}_{\mathbf{d}}^T \boldsymbol{C} & \mathbf{0} & \mathbf{0} \\ \boldsymbol{\Gamma}_{36} + 3\boldsymbol{N}_2 & \boldsymbol{\Gamma}_{37} & (\boldsymbol{G}_3^T - \boldsymbol{G}_2^T)/2 & \mathbf{0} & \mathbf{0} \\ \boldsymbol{\Gamma}_{46} & \boldsymbol{\Gamma}_{47} & -\boldsymbol{G}_3^T/2 & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & d_1 \boldsymbol{G}_2^T/2 & \mathbf{0} & \mathbf{0} \\ -3\boldsymbol{N}_2 & -\boldsymbol{W}_{22} & (h(u) - d_1)\boldsymbol{G}_3^T/2 & \mathbf{0} & \mathbf{0} \\ * & -3\boldsymbol{N}_2 & (d_2 - h(u))\boldsymbol{G}_3^T/2 & \mathbf{0} & \mathbf{0} \\ * & * & \boldsymbol{\Gamma}_{88} - (\boldsymbol{C} + \boldsymbol{C}^T) & \boldsymbol{C}\boldsymbol{H}_0 & \boldsymbol{C}\boldsymbol{H}_1 \\ * & * & * & -\varepsilon_0 \mathbf{I} & \mathbf{0} \\ * & * & * & * & -\varepsilon_1 \mathbf{I} \end{bmatrix} \tag{20}$$

$$\boldsymbol{\Gamma}_{11} = -\boldsymbol{G}_1 + (\boldsymbol{G}_2 + \boldsymbol{G}_2^T)/2 - 4\boldsymbol{N}_1 + \boldsymbol{M}_1 + \boldsymbol{M}_2 + (d_{12} + 1)\boldsymbol{M}_3 - \boldsymbol{\Gamma}_{18} \tag{21}$$

$$\boldsymbol{\Gamma}_{15} = d_1(\boldsymbol{G}_4 - \boldsymbol{G}_2)/2 \tag{22}$$

$$\boldsymbol{\Gamma}_{16} = (h(u) - d_1)(\boldsymbol{G}_5 - \boldsymbol{G}_3)/2 \tag{23}$$

$$\boldsymbol{\Gamma}_{17} = (d_2 - h(u))(\boldsymbol{G}_5 - \boldsymbol{G}_3)/2 \tag{24}$$

$$\boldsymbol{\Gamma}_{18} = -(d_1^2 \boldsymbol{N}_1 + d_{12}^2 \boldsymbol{N}_2) \tag{25}$$

$$\boldsymbol{\Gamma}_{22} = -\boldsymbol{M}_3 - 8\boldsymbol{N}_2 + \boldsymbol{W}_{11} + \boldsymbol{W}_{11}^T + \boldsymbol{W}_{12} + \boldsymbol{W}_{12}^T - \boldsymbol{W}_{21} - \boldsymbol{W}_{21}^T - \boldsymbol{W}_{22} - \boldsymbol{W}_{22}^T \tag{26}$$

$$\boldsymbol{\Gamma}_{23} = -2\boldsymbol{N}_2 - \boldsymbol{W}_{11}^T - \boldsymbol{W}_{12}^T - \boldsymbol{W}_{21}^T - \boldsymbol{W}_{22}^T \tag{27}$$

$$\boldsymbol{\Gamma}_{24} = -2\boldsymbol{N}_2 - \boldsymbol{W}_{11} + \boldsymbol{W}_{12} + \boldsymbol{W}_{21} - \boldsymbol{W}_{22} \tag{28}$$

$$\boldsymbol{\Gamma}_{26} = 3\boldsymbol{N}_2 + \boldsymbol{W}_{21}^T + \boldsymbol{W}_{22}^T \tag{29}$$

$$\boldsymbol{\Gamma}_{27} = 3\boldsymbol{N}_2 - \boldsymbol{W}_{12} + \boldsymbol{W}_{22} \tag{30}$$

$$\boldsymbol{\Gamma}_{34} = \boldsymbol{W}_{11} - \boldsymbol{W}_{12} + \boldsymbol{W}_{21} - \boldsymbol{W}_{22} \tag{31}$$

$$\boldsymbol{\Gamma}_{35} = d_1(-\boldsymbol{G}_4 + \boldsymbol{G}_5^T)/2 \tag{32}$$

$$\boldsymbol{\Gamma}_{36} = (h(u) - d_1)(-\boldsymbol{G}_5 + \boldsymbol{G}_6)/2 \tag{33}$$

$$\boldsymbol{\Gamma}_{37} = (d_2 - h(u))(-\boldsymbol{G}_5 + \boldsymbol{G}_6)/2 + \boldsymbol{W}_{12} + \boldsymbol{W}_{22} \tag{34}$$

$$\boldsymbol{\Gamma}_{46} = -(h(u) - d_1)\boldsymbol{G}_6/2 - \boldsymbol{W}_{21}^T + \boldsymbol{W}_{22}^T \tag{35}$$

$$\boldsymbol{\Gamma}_{47} = -(d_2 - h(u))\boldsymbol{G}_6/2 + 3\boldsymbol{N}_2 \tag{36}$$

$$\boldsymbol{\Gamma}_{88} = \boldsymbol{G}_1 - \boldsymbol{\Gamma}_{18} \tag{37}$$

$$d_{12} = d_2 - d_1 \tag{38}$$

and the matrix $\boldsymbol{C}$ is given by (12).

Proof Consider the LKF [6] as

$$V(\boldsymbol{w}(u)) = \boldsymbol{\Omega}^T(u)\boldsymbol{G}\boldsymbol{\Omega}(u) + \sum_{s=u-d_1}^{u-1} \boldsymbol{w}^T(s)\boldsymbol{M}_1\boldsymbol{w}(s)$$

$$+\sum_{s=u-d_2}^{u-1}\boldsymbol{w}^T(s)\boldsymbol{M}_2\boldsymbol{w}(s)+\sum_{\theta=-d_2}^{-d_1}\sum_{s=u+\theta}^{u-1}\boldsymbol{w}^T(s)\boldsymbol{M}_3\boldsymbol{w}(s)$$
$$+d_1\sum_{\theta=-d_1+1}^{0}\sum_{s=u-1+\theta}^{u-1}\boldsymbol{\xi}^T(s)\boldsymbol{N}_1\boldsymbol{\xi}(s)+d_{12}\sum_{\theta=-d_2+1}^{-d_1}\sum_{s=u-1+\theta}^{u-1}\boldsymbol{\xi}^T(s)\boldsymbol{N}_2\boldsymbol{\xi}(s) \tag{39}$$

where

$$\boldsymbol{\xi}(u)=\boldsymbol{w}(u+1)-\boldsymbol{w}(u)=\boldsymbol{\lambda}(z(u))-\boldsymbol{w}(u) \tag{40}$$

and

$$\boldsymbol{\Omega}^T(u)=[\boldsymbol{w}^T(u)\sum_{s=u-d_1}^{u-1}\boldsymbol{w}^T(s)\sum_{s=u-d_2}^{u-d_1-1}\boldsymbol{w}^T(s)] \tag{41}$$

Defining

$$\begin{aligned}\Delta V(\boldsymbol{w}(u))&=V(\boldsymbol{w}(u+1))-V(\boldsymbol{w}(u))\\&=\boldsymbol{\Phi}^T(u)\boldsymbol{\Upsilon}(h(u))\boldsymbol{\Phi}(u)+\boldsymbol{w}^T(u)\boldsymbol{M}_1\boldsymbol{w}(u)\\&\quad-\boldsymbol{w}^T(u-d_1)\boldsymbol{M}_1\boldsymbol{w}(u-d_1)+\boldsymbol{w}^T(u)\boldsymbol{M}_2\boldsymbol{w}(u)\\&\quad-\boldsymbol{w}^T(u-d_2)\boldsymbol{M}_2\boldsymbol{w}(u-d_2)+\boldsymbol{w}^T(u)\boldsymbol{M}_3\boldsymbol{w}(u)+d_{12}\boldsymbol{w}^T(u)\boldsymbol{M}_3\boldsymbol{w}(u)\\&\quad-\sum_{s=u-d_2}^{u-d_1}\boldsymbol{w}^T(s)\boldsymbol{M}_3\boldsymbol{w}(s)+\boldsymbol{\xi}^T(u)[d_1^2\boldsymbol{N}_1+d_{12}^2\boldsymbol{N}_2]\boldsymbol{\xi}(u)\\&\quad-d_1\sum_{s=u-d_1}^{u-1}\boldsymbol{\xi}^T(s)\boldsymbol{N}_1\boldsymbol{\xi}(s)-d_{12}\sum_{s=u-d_2}^{u-d_1-1}\boldsymbol{\xi}^T(s)\boldsymbol{N}_2\boldsymbol{\xi}(s)\end{aligned} \tag{42}$$

where

$$\begin{aligned}\boldsymbol{\Phi}^T(u)=\big[&\boldsymbol{w}^T(u)\,\boldsymbol{w}^T(u-h(u))\,\boldsymbol{w}^T(u-d_1)\,\boldsymbol{w}^T(u-d_2)\\&\boldsymbol{\zeta}^T(u,0,d_1)\,\boldsymbol{\zeta}^T(u,d_1,h(u))\,\boldsymbol{\zeta}^T(u,h(u),d_2)\,\boldsymbol{\lambda}^T(z(u))\big]\end{aligned} \tag{43}$$

$$\boldsymbol{\Upsilon}(h(u)) = \begin{bmatrix} -\boldsymbol{G}_1 + (\boldsymbol{G}_2^T + \boldsymbol{G}_2)/2 & \mathbf{0} & (-\boldsymbol{G}_2 + \boldsymbol{G}_3)/2 & -\boldsymbol{G}_3/2 & \boldsymbol{\Gamma}_{15} \\ * & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ * & * & \mathbf{0} & \mathbf{0} & \boldsymbol{\Gamma}_{35} \\ * & * & * & \mathbf{0} & -d_1\boldsymbol{G}_5^T/2 \\ * & * & * & * & \mathbf{0} \\ * & * & * & * & * \\ * & * & * & * & * \\ * & * & * & * & * \end{bmatrix}$$

$$\begin{bmatrix} \boldsymbol{\Gamma}_{16} & \boldsymbol{\Gamma}_{17} & \boldsymbol{G}_2^T/2 \\ \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \boldsymbol{\Gamma}_{36} & (d_2 - h(u))(\boldsymbol{G}_6 - \boldsymbol{G}_5)/2 & (-\boldsymbol{G}_2^T + \boldsymbol{G}_3^T)/2 \\ -(h(u) - d_1)\boldsymbol{G}_6/2 & -(d_2 - h(u))\boldsymbol{G}_6/2 & -\boldsymbol{G}_3^T/2 \\ \mathbf{0} & \mathbf{0} & d_1\boldsymbol{G}_2^T/2 \\ \mathbf{0} & \mathbf{0} & (h(u) - d_1)\boldsymbol{G}_3^T/2 \\ * & \mathbf{0} & (d_2 - h(u))\boldsymbol{G}_3^T/2 \\ * & * & \boldsymbol{G}_1 \end{bmatrix} \tag{44}$$

and $\boldsymbol{\zeta}(u, 0, d_1)$, $\boldsymbol{\zeta}(u, d_1, h(u))$, $\boldsymbol{\zeta}(u, h(u), d_2)$ are defined by (5).

Now

$$-\sum_{s=u-d_2}^{u-d_1} \boldsymbol{w}^T(s)\boldsymbol{M}_3\boldsymbol{w}(s) \le -\boldsymbol{w}^T(u - h(u))\boldsymbol{M}_3\boldsymbol{w}(u - h(u)). \tag{45}$$

Next, with the help of Lemma 1, the 10th and 11th terms of (42) are follows as

$$\begin{aligned} &-d_1 \sum_{s=u-d_1}^{u-1} \boldsymbol{\xi}^T(s)\boldsymbol{N}_1\boldsymbol{\xi}(s) \\ &\le -d_1 \begin{bmatrix} \boldsymbol{w}(u) - \boldsymbol{w}(u - d_1) \\ \boldsymbol{w}(u) + \boldsymbol{w}(u - d_1) - \boldsymbol{\zeta}(u, 0, d_1) \end{bmatrix}^T \\ &\begin{bmatrix} \boldsymbol{N}_1 & \mathbf{0} \\ \mathbf{0} & 3\boldsymbol{N}_1 \end{bmatrix} \begin{bmatrix} \boldsymbol{w}(u) - \boldsymbol{w}(u - d_1) \\ \boldsymbol{w}(u) + \boldsymbol{w}(u - d_1) - \boldsymbol{\zeta}(u, 0, d_1) \end{bmatrix} \end{aligned} \tag{46}$$

and

$$\begin{aligned} -\sum_{s=u-d_2}^{u-d_1-1} \boldsymbol{\xi}^T(s)\boldsymbol{N}_2\boldsymbol{\xi}(s) &= -d_{12} \sum_{s=u-h(u)}^{u-d_1-1} \boldsymbol{\xi}^T(s)\boldsymbol{N}_2\boldsymbol{\xi}(s) - \sum_{s=u-d_2}^{u-h(u)-1} \boldsymbol{\xi}^T(s)\boldsymbol{N}_2\boldsymbol{\xi}(s) \\ &\le -\frac{(d_2 - d_1)}{(h(u) - d_1)} \begin{bmatrix} \boldsymbol{w}(u - d_1) - \boldsymbol{w}(u - h(u)) \\ \boldsymbol{w}(u - d_1) + \boldsymbol{w}(u - h(u)) - \boldsymbol{\zeta}(u, d_1, h(u)) \end{bmatrix}^T \end{aligned}$$

$$\times \begin{bmatrix} N_2 & \mathbf{0} \\ \mathbf{0} & 3N_2 \end{bmatrix} \begin{bmatrix} \boldsymbol{w}(u-d_1) - \boldsymbol{w}(u-h(u)) \\ \boldsymbol{w}(u-d_1) + \boldsymbol{w}(u-h(u)) - \boldsymbol{\zeta}(u, d_1, h(u)) \end{bmatrix}$$
$$- \frac{(d_2-d_1)}{(d_2-h(u))} \begin{bmatrix} \boldsymbol{w}(u-h(u)) - \boldsymbol{w}(u-d_2) \\ \boldsymbol{w}(u-h(u)) + \boldsymbol{w}(u-d_2) - \boldsymbol{\zeta}(u, h(u), d_2) \end{bmatrix}^T$$
$$\times \begin{bmatrix} N_2 & \mathbf{0} \\ \mathbf{0} & 3N_2 \end{bmatrix} \begin{bmatrix} \boldsymbol{w}(u-h(u)) - \boldsymbol{w}(u-d_2) \\ \boldsymbol{w}(u-h(u)) + \boldsymbol{w}(u-d_2) - \boldsymbol{\zeta}(u, h(u), d_2) \end{bmatrix} \tag{47}$$

Lemma 5 (reciprocal convexity method) guarantees that if there exist matrix $\boldsymbol{W}$ such that (18) holds true, then (47) can be expressed as

$$- \sum_{s=u-d_2}^{u-d_1-1} \boldsymbol{\xi}^T(s) \boldsymbol{N}_2 \boldsymbol{\xi}(s)$$
$$\leq \begin{bmatrix} \boldsymbol{w}(u-d_1) - \boldsymbol{w}(u-h(u)) \\ \boldsymbol{w}(u-d_1) + \boldsymbol{w}(u-h(u)) - \boldsymbol{\zeta}(u, d_1, h(u)) \\ \boldsymbol{w}(u-h(u)) - \boldsymbol{w}(u-d_2) \\ \boldsymbol{w}(u-h(u)) + \boldsymbol{w}(u-d_2) - \boldsymbol{\zeta}(u, h(u), d_2) \end{bmatrix}^T \begin{bmatrix} \boldsymbol{N}_2 & \mathbf{0} & \boldsymbol{W}_{11} & \boldsymbol{W}_{12} \\ * & 3\boldsymbol{N}_2 & \boldsymbol{W}_{21} & \boldsymbol{W}_{22} \\ * & * & \boldsymbol{N}_2 & \mathbf{0} \\ * & * & * & 3\boldsymbol{N}_2 \end{bmatrix}$$
$$\times \begin{bmatrix} \boldsymbol{w}(u-d_1) - \boldsymbol{w}(u-h(u)) \\ \boldsymbol{w}(u-d_1) + \boldsymbol{w}(u-h(u)) - \boldsymbol{\zeta}(u, d_1, h(u)) \\ \boldsymbol{w}(u-h(u)) - \boldsymbol{w}(u-d_2) \\ \boldsymbol{w}(u-h(u)) + \boldsymbol{w}(u-d_2) - \boldsymbol{\zeta}(u, h(u), d_2) \end{bmatrix} \tag{48}$$

By considering (42)–(46) and (48), we get the following:

$$\Delta V(\boldsymbol{w}(u)) \leq \boldsymbol{\Phi}^T(u) \boldsymbol{\phi}(h(u)) \boldsymbol{\Phi}(u) - \delta_1 \tag{49}$$

where

$$\delta_1 = z^{\mathrm{T}}(u) \boldsymbol{C} \boldsymbol{\lambda}(z(u)) + \boldsymbol{\lambda}^{\mathrm{T}}(z(u)) \boldsymbol{C}^{\mathrm{T}} z(u) - \boldsymbol{\lambda}^{\mathrm{T}}(z(u))(\boldsymbol{C} + \boldsymbol{C}^{\mathrm{T}}) \boldsymbol{\lambda}(z(u)) \tag{50}$$

$$\boldsymbol{\phi}(h(u)) = \begin{bmatrix} \boldsymbol{\Gamma}_{11} & \mathbf{0} & (\boldsymbol{G}_3 - \boldsymbol{G}_2)/2 - 2\boldsymbol{N}_1 & -\boldsymbol{G}_3/2 & \boldsymbol{\Gamma}_{15} + 3\boldsymbol{N}_1 & \boldsymbol{\Gamma}_{16} & \boldsymbol{\Gamma}_{17} & \boldsymbol{\Gamma}_{18} + \boldsymbol{G}_2^T/2 + \overline{\mathbf{A}}^T \boldsymbol{C} \\ * & \boldsymbol{\Gamma}_{12} & \boldsymbol{\Gamma}_{23} & \boldsymbol{\Gamma}_{24} & \mathbf{0} & \boldsymbol{\Gamma}_{26} & \boldsymbol{\Gamma}_{27} & \overline{\mathbf{A}}_d^T \boldsymbol{C} \\ * & * & -\boldsymbol{M}_1 - 4(\boldsymbol{N}_1 + \boldsymbol{N}_2) & \boldsymbol{\Gamma}_{34} & \boldsymbol{\Gamma}_{35} + 3\boldsymbol{N}_1 & \boldsymbol{\Gamma}_{36} + 3\boldsymbol{N}_2 & \boldsymbol{\Gamma}_{37} & (\boldsymbol{G}_3^T - \boldsymbol{G}_2^T)/2 \\ * & * & * & -\boldsymbol{M}_2 - 4\boldsymbol{N}_2 & -d_1 \boldsymbol{G}_5^T/2 & \boldsymbol{\Gamma}_{46} & \boldsymbol{\Gamma}_{47} & -\boldsymbol{G}_3^T/2 \\ * & * & * & * & -3\boldsymbol{N}_1 & \mathbf{0} & \mathbf{0} & d_1 \boldsymbol{G}_2^T/2 \\ * & * & * & * & * & -3\boldsymbol{N}_2 & -\boldsymbol{W}_{22} & (h(u) - d_1) \boldsymbol{G}_3^T/2 \\ * & * & * & * & * & * & -3\boldsymbol{N}_2 & (d_2 - h(u)) \boldsymbol{G}_3^T/2 \\ * & * & * & * & * & * & * & \boldsymbol{\Gamma}_{88} \end{bmatrix} \tag{51}$$

In view of Lemma 3, the quantity δ_1 (see (50)) is greater than or equal to zero. From (49), it is obvious that $\Delta V(\boldsymbol{w}(u)) < 0$ if $\boldsymbol{\phi}(h(u)) < \mathbf{0}$ for all $h(u) \in [d_1,\ d_2]$.

Hence, $\boldsymbol{\phi}(h(u)) < \mathbf{0}$ with (18) is a condition for the G.A.S. of the DTS (1), (2a), (3), (4).

Using (4a), the condition (51) can be reexpressed as

$$\boldsymbol{\phi}_0(h(u)) + \boldsymbol{H}_0\mathbf{F}_0\boldsymbol{E}_0 + \boldsymbol{E}_0^T\mathbf{F}_0^T\boldsymbol{H}_0^T < \mathbf{0} \tag{52}$$

$$\overline{H}_0^T = \left[\underbrace{0\cdots 0}_{7\text{ times}}\ H_0^T C\right] \tag{53}$$

$$\overline{E}_0 = [E_0\ \underbrace{0\cdots 0}_{7\text{ times}}] \tag{54}$$

$$\boldsymbol{\phi}_0(h(u)) = \begin{bmatrix}
\boldsymbol{\Gamma}_{11} & \mathbf{0} & (\boldsymbol{G}_3-\boldsymbol{G}_2)/2-2\boldsymbol{N}_1 & -\boldsymbol{G}_3/2 & \boldsymbol{\Gamma}_{15}+3\boldsymbol{N}_1 & \boldsymbol{\Gamma}_{16} & \boldsymbol{\Gamma}_{17} & \boldsymbol{\Gamma}_{18}+\boldsymbol{G}_2^T/2+\mathbf{A}^T\boldsymbol{C} \\
* & \boldsymbol{\Gamma}_{12} & \boldsymbol{\Gamma}_{23} & \boldsymbol{\Gamma}_{24} & \mathbf{0} & \boldsymbol{\Gamma}_{26} & \boldsymbol{\Gamma}_{27} & \overline{\mathbf{A}}_d^T\boldsymbol{C} \\
* & * & -\boldsymbol{M}_1-4(\boldsymbol{N}_1+\boldsymbol{N}_2) & \boldsymbol{\Gamma}_{34} & \boldsymbol{\Gamma}_{35}+3\boldsymbol{N}_1 & \boldsymbol{\Gamma}_{36}+3\boldsymbol{N}_2 & \boldsymbol{\Gamma}_{37} & (\boldsymbol{G}_3^T-\boldsymbol{G}_2^T)/2 \\
* & * & * & -\boldsymbol{M}_2-4\boldsymbol{N}_2 & -d_1\boldsymbol{G}_5^T/2 & \boldsymbol{\Gamma}_{46} & \boldsymbol{\Gamma}_{47} & -\boldsymbol{G}_3^T/2 \\
* & * & * & * & -3\boldsymbol{N}_1 & \mathbf{0} & \mathbf{0} & d_1\boldsymbol{G}_2^T/2 \\
* & * & * & * & * & -3\boldsymbol{N}_2 & -\boldsymbol{W}_{22} & (h(u)-d_1)\boldsymbol{G}_3^T/2 \\
* & * & * & * & * & * & -3\boldsymbol{N}_2 & (d_2-h(u))\boldsymbol{G}_3^T/2 \\
* & * & * & * & * & * & * & \boldsymbol{\Gamma}_{88}
\end{bmatrix} \tag{55}$$

With the help of Lemma 2, (52) can be written as

$$\boldsymbol{\phi}_0(h(u)) + \varepsilon_0^{-1}\overline{\boldsymbol{H}}_0\overline{\boldsymbol{H}}_0^T + \varepsilon_0\overline{\boldsymbol{E}}_0^T\overline{\boldsymbol{E}}_0 < \mathbf{0} \tag{56}$$

where $\varepsilon_0 > 0$. Next, by the use of Schur's complement, one can rewrite (56) as

$$\begin{bmatrix}
\boldsymbol{\Gamma}_{11}+\varepsilon_0\mathbf{E}_0^T\mathbf{E}_0 & \mathbf{0} & (\boldsymbol{G}_3-\boldsymbol{G}_2)/2-2\boldsymbol{N}_1 & -\boldsymbol{G}_3/2 & \boldsymbol{\Gamma}_{15}+3\boldsymbol{N}_1 \\
* & \boldsymbol{\Gamma}_{12} & \boldsymbol{\Gamma}_{23} & \boldsymbol{\Gamma}_{24} & \mathbf{0} \\
* & * & -\boldsymbol{M}_1-4(\boldsymbol{N}_1+\boldsymbol{N}_2) & \boldsymbol{\Gamma}_{34} & \boldsymbol{\Gamma}_{35}+3\boldsymbol{N}_1 \\
* & * & * & -\boldsymbol{M}_2-4\boldsymbol{N}_2 & -d_1\boldsymbol{G}_5^T/2 \\
* & * & * & * & -3\boldsymbol{N}_1 \\
* & * & * & * & * \\
* & * & * & * & * \\
* & * & * & * & * \\
* & * & * & * & *
\end{bmatrix}$$

$$\begin{bmatrix} \boldsymbol{\Gamma}_{16} & \boldsymbol{\Gamma}_{17} & \boldsymbol{\Gamma}_{18}+\boldsymbol{G}_2^T/2+\mathbf{A}^T\boldsymbol{C} & \mathbf{0} \\ \boldsymbol{\Gamma}_{26} & \boldsymbol{\Gamma}_{27} & \bar{\mathbf{A}}_d^T\boldsymbol{C} & \mathbf{0} \\ \boldsymbol{\Gamma}_{36}+3\boldsymbol{N}_2 & \boldsymbol{\Gamma}_{37} & (\boldsymbol{G}_3^T-\boldsymbol{G}_2^T)/2 & \mathbf{0} \\ \boldsymbol{\Gamma}_{46} & \boldsymbol{\Gamma}_{47} & -\boldsymbol{G}_3^T/2 & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & d_1\boldsymbol{G}_2^T/2 & \mathbf{0} \\ -3\boldsymbol{N}_2 & -\boldsymbol{W}_{22} & (h(u)-d_1)\boldsymbol{G}_3^T/2 & \mathbf{0} \\ * & -3\boldsymbol{N}_2 & (d_2-h(u))\boldsymbol{G}_3^T/2 & \mathbf{0} \\ * & * & \boldsymbol{\Gamma}_{88} & \boldsymbol{C}\boldsymbol{H}_0 \\ * & * & * & -\varepsilon_0\mathbf{I} \end{bmatrix} < \mathbf{0} \tag{57}$$

Next, by following the steps similar to (52)–(57), one can easily show that (57) is equivalent to $\boldsymbol{\Psi}(h(u)) < \mathbf{0}$. Based on the feature of matrix affine function, the condition $\boldsymbol{\Psi}(h(u)) < \mathbf{0}$ holds if and only if (19) satisfies. This concludes the proof of Theorem 1.

Theorem 2 For given integers d_1,d_2 with $d_2 \geq d_1 \geq 1$, the DTS (1), (2a), (3), (4) is GAS if there are suitable dimensioned matrices $\mathbf{0} < \boldsymbol{G} = \begin{bmatrix} \boldsymbol{G}_1 & \boldsymbol{G}_2 & \boldsymbol{G}_3 \\ * & \boldsymbol{G}_4 & \boldsymbol{G}_5 \\ * & * & \boldsymbol{G}_6 \end{bmatrix} = \boldsymbol{G}^T$, $\mathbf{0} < \boldsymbol{M}_i = \boldsymbol{M}_i^T (i = 1, 2, 3)$, $\mathbf{0} < \boldsymbol{N}_i = \boldsymbol{N}_i^T (i = 1, 2)$, any matrix $\boldsymbol{W} = \begin{bmatrix} \boldsymbol{W}_{11} & \boldsymbol{W}_{12} \\ \boldsymbol{W}_{21} & \boldsymbol{W}_{22} \end{bmatrix}$, positive scalars ε_0,ε_1 and $L \in [-1, 0)$ such that (18) and (58) satisfy

$$\boldsymbol{\Psi}_1(h(u) = d_1) < \mathbf{0} \tag{58a}$$

$$\boldsymbol{\Psi}_1(h(u) = d_2) < \mathbf{0} \tag{58b}$$

where

$$\boldsymbol{\Psi}_1(h(u)) =$$

$$\begin{bmatrix}
\boldsymbol{\Gamma}_{11}+\varepsilon_0\mathbf{E}_0^T\mathbf{E}_0 & \mathbf{0} & (\boldsymbol{G}_3-\boldsymbol{G}_2)/2-2\boldsymbol{N}_1 & -\boldsymbol{G}_3/2 & \boldsymbol{\Gamma}_{15}+3\boldsymbol{N}_1 & \\
* & \boldsymbol{\Gamma}_{12}+\varepsilon_1\mathbf{E}_1^T\mathbf{E}_1 & \boldsymbol{\Gamma}_{23} & \boldsymbol{\Gamma}_{24} & \mathbf{0} & \\
* & * & -\boldsymbol{M}_1-4(\boldsymbol{N}_1+\boldsymbol{N}_2) & \boldsymbol{\Gamma}_{34} & \boldsymbol{\Gamma}_{35}+3\boldsymbol{N}_1 & \\
* & * & * & -\boldsymbol{M}_2-4\boldsymbol{N}_2 & -d_1\boldsymbol{G}_5^T/2 & \\
* & * & * & * & -3\boldsymbol{N}_1 & \\
* & * & * & * & * & \\
* & * & * & * & * & \\
* & * & * & * & * & \\
* & * & * & * & * & \\
* & * & * & * & * & \\
* & * & * & * & * &
\end{bmatrix}$$

$$\begin{bmatrix}
\boldsymbol{\Gamma}_{16} & \boldsymbol{\Gamma}_{17} & \boldsymbol{\Gamma}_{18}+\boldsymbol{G}_2^T/2+(1+L)\mathbf{A}^T\boldsymbol{D} & (-2L)^{1/2}\mathbf{A}^{\mathrm{T}}\boldsymbol{D} & \mathbf{0} & \mathbf{0} \\
\boldsymbol{\Gamma}_{26} & \boldsymbol{\Gamma}_{27} & (1+L)\mathbf{A}_d^{\mathrm{T}}\boldsymbol{D} & (-2L)^{1/2}\mathbf{A}_d^{\mathrm{T}}\boldsymbol{D} & \mathbf{0} & \mathbf{0} \\
\boldsymbol{\Gamma}_{36}+3\boldsymbol{N}_2 & \boldsymbol{\Gamma}_{37} & (\boldsymbol{G}_3^T-\boldsymbol{G}_2^T)/2 & \mathbf{0} & \mathbf{0} & \mathbf{0} \\
\boldsymbol{\Gamma}_{46} & \boldsymbol{\Gamma}_{47} & -\boldsymbol{G}_3^T/2 & \mathbf{0} & \mathbf{0} & \mathbf{0} \\
\mathbf{0} & \mathbf{0} & d_1\boldsymbol{G}_2^T/2 & \mathbf{0} & \mathbf{0} & \mathbf{0} \\
-3\boldsymbol{N}_2 & -\boldsymbol{W}_{22} & (h(u)-d_1)\boldsymbol{G}_3^T/2 & \mathbf{0} & \mathbf{0} & \mathbf{0} \\
* & -3\boldsymbol{N}_2 & (d_2-h(u))\boldsymbol{G}_3^T/2 & \mathbf{0} & \mathbf{0} & \mathbf{0} \\
* & * & \boldsymbol{\Gamma}_{88}-2\boldsymbol{D} & \mathbf{0} & (1+L)\boldsymbol{D}\boldsymbol{H}_0 & (1+L)\boldsymbol{D}\boldsymbol{H}_1 \\
* & * & * & -\boldsymbol{D} & (-2L)^{1/2}\boldsymbol{D}\boldsymbol{H}_0 & (-2L)^{1/2}\boldsymbol{D}\boldsymbol{H}_1 \\
* & * & * & * & -\varepsilon_0\mathbf{I} & \mathbf{0} \\
* & * & * & * & * & -\varepsilon_1\mathbf{I}
\end{bmatrix} \tag{59}$$

and $\boldsymbol{D}$ is a diagonal matrix considered in Lemma 4.

Proof By considering the LKF (39) and using (42)–(46) and (48), we have

$$\Delta V(\boldsymbol{w}(u)) = \boldsymbol{\Phi}^{\mathrm{T}}(u)\boldsymbol{\phi}_1(h(u))\boldsymbol{\Phi}(u) - \delta_2 \tag{60}$$

where

$$\begin{aligned}
\delta_2 &= (1+L)\boldsymbol{z}^{\mathrm{T}}(u)\boldsymbol{D}\boldsymbol{\lambda}(z(u)) + (1+L)\boldsymbol{\lambda}^{\mathrm{T}}(z(u))\boldsymbol{D}\boldsymbol{z}(u) \\
&\quad -2\boldsymbol{\lambda}^{\mathrm{T}}(z(u))\boldsymbol{D}\boldsymbol{\lambda}(z(u)) - 2L\boldsymbol{z}^{\mathrm{T}}(u)\boldsymbol{D}\boldsymbol{z}(u)
\end{aligned} \tag{61}$$

$$\boldsymbol{\phi}_1(h(u))$$

$$= \begin{bmatrix}
\boldsymbol{\Gamma}_{11}-2L\overline{\mathbf{A}}^{\mathrm{T}}\boldsymbol{D}\overline{\mathbf{A}} & -2L\overline{\mathbf{A}}^{\mathrm{T}}\boldsymbol{D}\overline{\mathbf{A}}_d & (\boldsymbol{G}_3-\boldsymbol{G}_2)/2-2\boldsymbol{N}_1 & -\boldsymbol{G}_3/2 \\
* & \boldsymbol{\Gamma}_{12}-2L\overline{\mathbf{A}}_d^{\mathrm{T}}\boldsymbol{D}\overline{\mathbf{A}}_d & \boldsymbol{\Gamma}_{23} & \boldsymbol{\Gamma}_{24} \\
* & * & -\boldsymbol{M}_1-4(\boldsymbol{N}_1+\boldsymbol{N}_2) & \boldsymbol{\Gamma}_{34} \\
* & * & * & -\boldsymbol{M}_2-4\boldsymbol{N}_2 \\
* & * & * & * \\
* & * & * & * \\
* & * & * & * \\
* & * & * & *
\end{bmatrix}$$

$$\begin{bmatrix} \boldsymbol{\Gamma}_{15}+3\boldsymbol{N}_1 & \boldsymbol{\Gamma}_{16} & \boldsymbol{\Gamma}_{17} & \boldsymbol{\Gamma}_{18}+\boldsymbol{G}_2^T/2+(1+L)\overline{\mathbf{A}}^{\mathrm{T}}\boldsymbol{D} \\ \mathbf{0} & \boldsymbol{\Gamma}_{26} & \boldsymbol{\Gamma}_{27} & (1+L)\overline{\mathbf{A}}_d^{\mathrm{T}}\boldsymbol{D} \\ \boldsymbol{\Gamma}_{35}+3\boldsymbol{N}_1 & \boldsymbol{\Gamma}_{36}+3\boldsymbol{N}_2 & \boldsymbol{\Gamma}_{37} & (\boldsymbol{G}_3^T-\boldsymbol{G}_2^T)/2 \\ -d_1\boldsymbol{G}_5^T/2 & \boldsymbol{\Gamma}_{46} & \boldsymbol{\Gamma}_{47} & -\boldsymbol{G}_3^T/2 \\ -3\boldsymbol{N}_1 & \mathbf{0} & \mathbf{0} & d_1\boldsymbol{G}_2^T/2 \\ * & -3\boldsymbol{N}_2 & -\boldsymbol{W}_{22} & (h(u)-d_1)\boldsymbol{G}_3^T/2 \\ * & * & -3\boldsymbol{N}_2 & (d_2-h(u))\boldsymbol{G}_3^T/2 \\ * & * & * & \boldsymbol{G}_1-\boldsymbol{\Gamma}_{18}-2\boldsymbol{D} \end{bmatrix} \tag{62}$$

In view of (14) (see Lemma 4), the quantity δ_2 (see (61)) is non-negative. With the help of (60), it is obvious that $\Delta V(\boldsymbol{w}(u)) < 0$ only when $\boldsymbol{\phi}_1(h(u)) < \mathbf{0}$. Therefore, $\boldsymbol{\phi}_1(h(u)) < \mathbf{0}$ along with (18) is a sufficient G.A.S. condition for the present system.

Next, follow the similar steps as mentioned in the proof of Theorem 1, the condition $\boldsymbol{\phi}_1(h(u)) < \mathbf{0}$ leads to $\boldsymbol{\Psi}_1(h(u)) < \mathbf{0}$. Under the property of matrix function affinity, the condition $\boldsymbol{\Psi}_1(h(u)) < \mathbf{0}$ satisfies if and only if (58) fulfills. It concludes the proof of Theorem 2.

Remark 2 The requirement of number of decision variables (NoDVs) for Theorem 3 of [7] and Theorem 3.1 of [9] is given by $14n^2+5n+2$ and $5n^2+3n+2$, respectively. For Theorem 1 and Theorem 2 of this paper, the required NoDVs are $12n^2+3n+2$ and $11n^2+5n+2$, respectively. It is clear that as compared to Theorem 3 of [7], the present criteria (Theorems 1 and 2) require less NoDVs. Consequently, the criteria presented in this paper have smaller numerical complexity than Theorem 3 of [7].

Remark 3 The presented criteria (Theorems 1 and 2) are LMI based and, hence, one can easily trace the feasibility of the presented criteria using MATLAB and YALMIP 3.0 parser [26, 27].

Remark 4 For saturation overflow nonlinearities (i.e., $L = 1$), Theorem 1 reduces to Theorem 2 of [6]. However, unlike Theorem 2 of [6], the present approach can handle other types of overflow nonlinearities (namely, zeroing, two's complement and triangular).

4 Numerical Examples

In order to show the effectiveness of the proposed criteria, we now consider the following examples.

Example 1 Consider the DTS (1), (2a), (3), (4) where

$$\mathbf{A} = \begin{bmatrix} 0.8 & 0 \\ .05 & 0.9 \end{bmatrix}, \mathbf{A}_d = \begin{bmatrix} 0.01 & 0 \\ 0 & 0.02 \end{bmatrix}, \boldsymbol{H}_0 = \boldsymbol{H}_1 = \begin{bmatrix} 0 \\ 0.1 \end{bmatrix},$$
$$\boldsymbol{E}_0 = [0.01 \quad 0], \boldsymbol{E}_1 = [0 \quad 0.01] \tag{63}$$

Concerning to $L = 1$ (Saturation overflow), it is checked that for the delay range $2 \leq h(u) \leq 41$, Theorem 1 provides feasible results. Therefore, according to Theorem 1, the system (1), (2a), (3), (4) and (63) is GAS. Concerning to this example, the conditions given in Theorem 1 are feasible for the values of unknown parameters as given below.

$$\boldsymbol{C} = \begin{bmatrix} 7871.7 & 315.5 \\ 331.2 & 1117.1 \end{bmatrix}, \varepsilon_0 = 6684.0', \varepsilon_1 = 1735.8, \boldsymbol{G}_1 = \begin{bmatrix} 8612.8 & 304.2 \\ 304.2 & 1104.5 \end{bmatrix},$$
$$\boldsymbol{G}_2 = \begin{bmatrix} 142.5167 & 2.1098 \\ 0.3637 & 3.3630 \end{bmatrix}, \boldsymbol{G}_3 = \begin{bmatrix} -0.3301 & -0.0310 \\ -0.0602 & -0.2332 \end{bmatrix}, \boldsymbol{G}_4 =$$
$$\begin{bmatrix} 126.4429 & 0.7689 \\ 0.7689 & 3.4261 \end{bmatrix}, \boldsymbol{G}_5 = \begin{bmatrix} 0.3042 & -0.0046 \\ -0.0132 & -0.0675 \end{bmatrix}, \boldsymbol{G}_6 = \begin{bmatrix} 1.1919 & 0.0065 \\ 0.0065 & 0.0184 \end{bmatrix},$$
$$\boldsymbol{M}_1 = \begin{bmatrix} 310.7017 & 1.5163 \\ 1.5163 & 8.9547 \end{bmatrix}, \boldsymbol{M}_2 = \begin{bmatrix} 475.8411 & 1.0202 \\ 1.0202 & 4.9393 \end{bmatrix}, \boldsymbol{M}_3 =$$
$$\begin{bmatrix} 25.4294 & -0.1983 \\ -0.1983 & 1.4460 \end{bmatrix}, \boldsymbol{N}_1 = \begin{bmatrix} 126.8201 & 0.0655 \\ 0.0655 & 1.4081 \end{bmatrix}, \boldsymbol{N}_2 = \begin{bmatrix} 3.8700 & 0.2023 \\ 0.2023 & 0.6655 \end{bmatrix},$$
$$\boldsymbol{W}_{11} = \begin{bmatrix} -1.1153 & -0.2034 \\ -0.2033 & -0.6637 \end{bmatrix}, \boldsymbol{W}_{12} = \begin{bmatrix} 0.1774 & 0.0521 \\ -0.0014 & -0.0052 \end{bmatrix}, \boldsymbol{W}_{21} =$$
$$\begin{bmatrix} -0.4430 & 0.0010 \\ -0.0602 & 0.0032 \end{bmatrix}, \boldsymbol{W}_{22} = \begin{bmatrix} -0.1153 & -0.0062 \\ -0.0055 & -0.0038 \end{bmatrix}.$$

By assuming random initial conditions, Fig. 1 validates the findings of Theorem 1 for the parameters reflected in Example 1 with $2 \leq h(u) \leq 41$ and $\boldsymbol{F}_0 = \boldsymbol{F}_1 = 1$.

Example 2 Consider the DTS described by (1), (2a), (3), (4) and (63) and $L = 0$ (Zeroing overflow). Theorem 1 assures the G.A.S. for the delay range $2 \leq h(u) \leq 41$. For this example, the conditions given in Theorem 1 lead to the following feasible solutions.

$$\boldsymbol{C} = \begin{bmatrix} 3262.0 & 0 \\ 0233.1 \end{bmatrix}, \varepsilon_0 = 1880.0, \varepsilon_1 = 367.54, \boldsymbol{G}_1 = \begin{bmatrix} 3569.4 & -007.2 \\ -007.2 & 230.7 \end{bmatrix},$$
$$\boldsymbol{G}_2 = \begin{bmatrix} 60.8650 & 0.6477 \\ -1.4302 & 0.6938 \end{bmatrix}, \boldsymbol{G}_3 = \begin{bmatrix} -0.1121 & 0.0432 \\ -0.0066 & -0.0489 \end{bmatrix}, \boldsymbol{G}_4 =$$
$$\begin{bmatrix} 49.8297 & -0.6120 \\ -0.6120 & 0.7152 \end{bmatrix}, \boldsymbol{G}_5 = \begin{bmatrix} 0.1612 & 0.0080 \\ -0.0037 & -0.0137 \end{bmatrix} \boldsymbol{G}_6 = \begin{bmatrix} 0.4922 & -0.0042 \\ -0.0042 & 0.0039 \end{bmatrix},$$
$$\boldsymbol{M}_1 = \begin{bmatrix} 116.6697 & -1.2219 \\ -1.2219 & 1.8458 \end{bmatrix}, \boldsymbol{M}_2 = \begin{bmatrix} 177.7413 & -1.7012 \\ -1.7012 & 1.0489 \end{bmatrix}, \boldsymbol{M}_3 =$$
$$\begin{bmatrix} 11.3719 & -0.1389 \\ -0.1389 & 0.3035 \end{bmatrix}, \boldsymbol{N}_1 = \begin{bmatrix} 44.5249 & -0.4872 \\ -0.4872 & 0.2916 \end{bmatrix}, \boldsymbol{N}_2 = \begin{bmatrix} 1.6294 & 0.0051 \\ 0.0051 & 0.1389 \end{bmatrix},$$

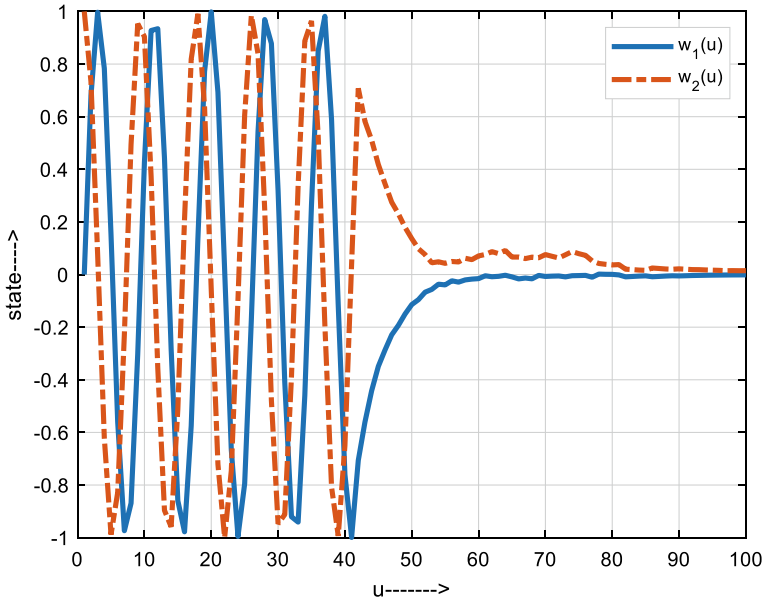

Fig. 1 State trajectories of the DTS in Example 1

$$\boldsymbol{W}_{11} = \begin{bmatrix} -0.4325 & -0.0179 \\ -0.0179 & -0.1384 \end{bmatrix}, \boldsymbol{W}_{12} = \begin{bmatrix} 0.0788 & -0.0012 \\ -0.0009 & -0.0007 \end{bmatrix}, \boldsymbol{W}_{21} = \begin{bmatrix} -0.1994 & 0.0023 \\ -0.0055 & 0.0011 \end{bmatrix}, \boldsymbol{W}_{22} = \begin{bmatrix} -0.0605 & -0.0000 \\ 0.0000 & -0.0007 \end{bmatrix}.$$

Under random initial conditions, Fig. 2 supports the fact that Theorem 1 affirms the G.A.S. for the present example with the allowed delay range $2 \leq h(u) \leq 41$ and $\boldsymbol{F}_0 = \boldsymbol{F}_1 = 1$.

Example 3 Consider the DTS described by (1), (2a), (3), (4) and (63) and $L = -1/3$. The DTS is GAS for the delay range $2 \leq h(u) \leq 34$. Concerning to this example, Theorem 2 provides feasible solutions for values of unknown parameters as given below.

$$\boldsymbol{D} = \begin{bmatrix} 54.7457 & 0 \\ 01.4866 \end{bmatrix}, \varepsilon_0 = 64.1859, \varepsilon_1 = 3.4574, \boldsymbol{G}_1 = \begin{bmatrix} 73.7274 & -0.0300 \\ -0.0300 & 1.9574 \end{bmatrix},$$

$$\boldsymbol{G}_2 = \begin{bmatrix} 1.2478 & -0.0027 \\ -0.0067 & 0.0020 \end{bmatrix}, \boldsymbol{G}_3 = \begin{bmatrix} 0.0019 & 0.0004 \\ -0.0000 & -0.0000 \end{bmatrix}, \boldsymbol{G}_4 = \begin{bmatrix} 1.1283 & -0.0052 \\ -0.0052 & 0.0022 \end{bmatrix}, \boldsymbol{G}_5 = \begin{bmatrix} 0.0048 & 0.0000 \\ -0.0000 & 0.0000 \end{bmatrix}, \boldsymbol{G}_6 = \begin{bmatrix} 0.0126 & -0.0000 \\ -0.0000 & 0.0000 \end{bmatrix},$$

$$\boldsymbol{M}_1 = \begin{bmatrix} 2.9127 & -0.0129 \\ -0.0129 & 0.0034 \end{bmatrix}, \boldsymbol{M}_2 = \begin{bmatrix} 4.5445 & -0.0190 \\ -0.0190 & 0.0057 \end{bmatrix}, \boldsymbol{M}_3 =$$

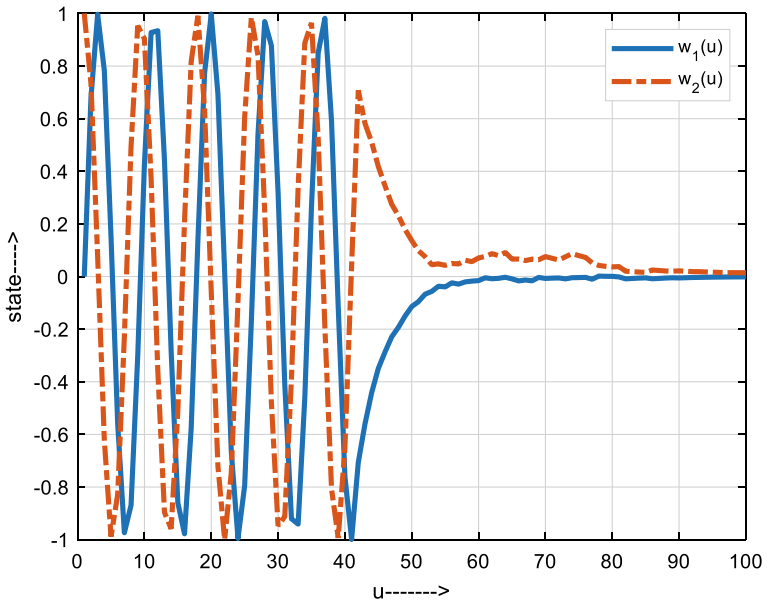

Fig. 2 State trajectories of DTS in Example 2

$$\begin{bmatrix} 0.2577 & -0.0011 \\ -0.0011 & 0.0042 \end{bmatrix}, \boldsymbol{N}_2 = \begin{bmatrix} 0.0258 & 0.0000 \\ 0.0000 & 0.0009 \end{bmatrix}, \boldsymbol{N}_1 = \begin{bmatrix} 1.0152 & -0.0046 \\ -0.0046 & 0.0006 \end{bmatrix},$$
$$\boldsymbol{W}_{11} = \begin{bmatrix} -0.0040 & -0.0001 \\ -0.0001 & -0.0009 \end{bmatrix}, \boldsymbol{W}_{12} = \begin{bmatrix} 0.0016 & -0.0000 \\ -0.0000 & 0.0000 \end{bmatrix}, \boldsymbol{W}_{21} = \begin{bmatrix} -0.0026 & 0.0000 \\ 0.0000 & -0.0000 \end{bmatrix}, \boldsymbol{W}_{22} = \begin{bmatrix} -541.9000 & -0.4000 \\ -0.5000 & -.90000 \end{bmatrix}.$$

The state trajectories are shown in Fig. 3 confirm the outcomes of Theorem 2 for the present example with $\boldsymbol{F}_0 = \boldsymbol{F}_1 = 1$.

From Tables 1, 2 and 3, it is observed that the presented criteria provide less conservativeness as compared to previously reported criteria of [7] and [9]. Table 4 presented comparison of NoDvs than the previously reported criteria of [7] and [9].

5 Conclusions

Two sufficient stability conditions for G.A.S. of DTS with PU, GON and TVD have been established. The approach presented in this paper supports in reducing the conservativeness which in turn provides a larger stability region than previously

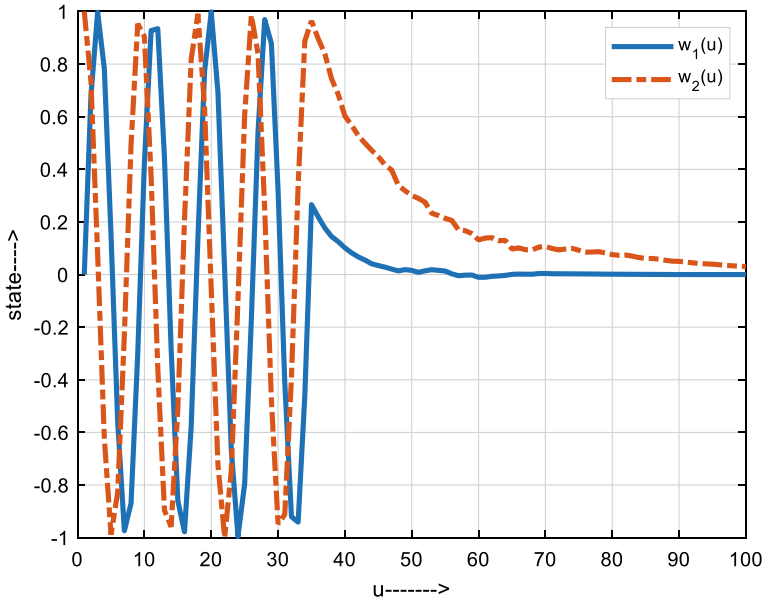

Fig. 3 State trajectories of DTS in Example 3

Table 1 UDB (d_2) for different LDB (d_1) for the system in Example 1

Methods/d_1	2	6	8
Theorem 3 [7]	23	27	29
Theorem 3.1 [9]	23	27	29
Theorem 1	41	45	47

Table 2 UDB (d_2) for different LDB (d_1) for the system in Example 2

Methods/d_1	2	6	8
Theorem 3 [7]	23	27	29
Theorem 3.1 [9]	23	27	29
Theorem 1	41	45	47

Table 3 UDB (d_2) for different LDB (d_1) for the system in Example 3

Methods/d_1	2	6	8
Theorem 3 [7]	23	27	29
Theorem 3.1 [9]	23	27	29
Theorem 2	34	38	40

Table 4 Comparison of NoDVs

Methods	NoDVs for $n = 2$	NoDVs for $n = 3$
Theorem 3 [7]	68	143
Theorem 3.1 [9]	28	56
Theorem 1	56	119
Theorem 2	56	116

reported criterion. The proposed criteria involve less NoDVs and, hence, computationally less complex. The efficacy of the presented criteria over previous result has been proved by numerical examples.

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Stability Criterion for Implementing Discrete-Time Delayed Systems Subjected to Finite Wordlength Nonlinearities with External Interference

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1 Introduction

Discrete-time delayed systems (DTDS) have gained remarkable attention in past many years due to their extensive applications in various fields which comprise wireless sensor networks [12], control systems [11], network echo cancellation [5], biomedical signal processing [10], speech processing [2], etc. Therefore, a number of authors have attained impetus in studying DTDS from the last several years.

In the implementation of DTDS on fixed wordlength processor like microcontroller or computer processor, the occurrence of nonlinearities (quantization and overflow) is generally unavoidable [3, 4]. The general types of quantization nonlinearities are value truncation (VT), magnitude truncation (MT) and round off (RO). Two's complement, saturation, triangular and zeroing are the commonly occurred overflow nonlinearities. The existence of these two nonlinearities, so called, finite wordlength nonlinearities (FWN) may generate oscillations and which in turn the system to be unstable. Many works have been published on the study of quantization effects in DTDS without overflow effects [13, 14] whereas many have considered the effects of overflow on DTDS without quantization effects [8, 15–19]. Thus, the study of stability of DTDS having FWN is practically more realistic [3, 4, 6, 7, 9, 21].

Time delay and external interference are also considered as the reasons for instability in many systems. Time delay is usually occurred in the system due to measurement lags, fixed velocity of data processing, transport lags, etc. Several researchers have gained attention in bringing stability conditions for systems with delay [1, 6, 9, 19]. While realizing higher-order DTDS on software or hardware, they are generally split and realized as serially lower-order DTDS. As a result, the external interferences among the lower-order DTDS are unavoidable and cause performance deprivation of DTDS [8, 15–18, 21, 22]. The approaches accounted in [8, 15–18, 22] are not

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adequate enough to remark about the exponential stability of externally interfered discrete systems. A few conditions [8, 15–18, 22] have been discussed for exponential stability of discrete systems with external interference and saturation nonlinearities. These conditions [8, 15–18, 22] are not relevant for the systems with FWN. Without considering the delay, stability analysis of discrete system with external interference and FWN has been done in [21].

Motivated by the works of [8, 15–18, 21, 22], a new criterion for the stability analysis of DTDS with FWN and external interference is addressed in this paper. By using Lyapunov Krasovskii functional (LKF), a sufficient criterion is obtained in linear matrix inequality (LMI) form which assures the exponential stability of DTDS. The remaining paper is organized as follows. Section 2 introduces the system description. Main result of the paper is discussed in Sect. 3. Section 4 provides some special cases of presented approach. By using example, the utility of the results is discussed in Sect. 5. Finally, Sect. 6 concludes the paper.

Notations: In this paper, $\mathbf{R}^{g\times h}$ is the set of $g \times h$ real matrices, $\mathbf{R}^{g}$ symbolize the g-dimensional space, 0 denotes the null matrix of suitable size, $\mathbf{C} < 0 (> 0)$ indicates that $\mathbf{C}$ is a negative definite (positive definite) symmetric matrix, $\mathbf{C}^{\mathrm{T}}$ is the transpose of $\mathbf{C}, ||\lambda||$ refers to the vector or matrix norm, $\lambda_{\max}(\mathbf{C})$ and $\lambda_{\min}(\mathbf{C})$ are maximum and minimum eigenvalues of $\mathbf{C}$, respectively.

2 System Description

This paper considers a class of DTDS operating under the presence of FWN and external interference. In particular, the DTDS is specified as

$$\begin{aligned}\boldsymbol{\sigma}(a+1) &= \mathbf{O}\{\mathbf{Q}(\mathbf{y}(a))\} = \boldsymbol{\Psi}(\mathbf{y}(a)) + \mathbf{u}(a)\\ &= \left[\Psi_1(\mathbf{y}_1(a)) \;\; \Psi_2(\mathbf{y}_2(a)) \;\; \ldots \;\; \Psi_r(\mathbf{y}_r(a))\right]^T\\ &\quad + [u_1(a) \;\; u_2(a) \;\; \ldots \;\; u_r(a)]^T, \end{aligned} \tag{1a}$$

$$\boldsymbol{y}(a) = \boldsymbol{A}\boldsymbol{\sigma}(a) + \sum_{i=1}^{s} \boldsymbol{A}_{di}\boldsymbol{\sigma}(a-d_i) \tag{1b}$$

$$\boldsymbol{\sigma}(a) = \Theta(a), \;\; a \in [-d_s, 0], \tag{2}$$

where $\mathbf{u}(a)$ is an external interference, $\boldsymbol{\sigma}(a)$ is a state vector, $\boldsymbol{O}(\cdot)$ and $\boldsymbol{Q}(\cdot)$ refers to overflow nonlinearities and quantization nonlinearities, respectively, $\boldsymbol{A}$ and $\boldsymbol{A}_{di}$ are the known matrices, $0 < d_i \;\; (i = 1, 2, \ldots, s)$ is state delay, s symbolized the number of delays in the state, $\Theta(a)$ represents the initial value at time a and $\boldsymbol{\Psi}(\cdot)$ is the combined nonlinear function.

When $\boldsymbol{Q}(\cdot)$ is MT or RO, $\boldsymbol{\Psi}(\cdot)$ is limited to the sector $[k_o, \; k_q]$, i.e.

$$\Psi_i(0) = 0, \quad k_o y_i^2(a) \le \Psi_i(y_i(a)) y_i(a) \le k_q y_i^2(a), \quad i = 1, 2, \ldots, r, \tag{3}$$

where

$$k_o = \begin{cases} 0, & \text{for saturation or zeroing} \\ -1/3, & \text{for triangular} \\ -1, & \text{for two's complement,} \end{cases} \qquad k_q = \begin{cases} 1, & \text{for MT} \\ 2, & \text{for RO} \end{cases}$$

For a given $\gamma > 0$, the target of the present paper is two-fold: (i) It gives a new stability condition for the DTDS (1)–(3) fulfilling

$$\sum_{a=0}^{\infty} \boldsymbol{\sigma}^T(a)\mathbf{F}\boldsymbol{\sigma}(a) < \gamma^2 \sum_{v=0}^{\infty} \boldsymbol{u}^T(a)\boldsymbol{u}(a), \quad \mathbf{0} < \mathbf{F} = \mathbf{F}^T, \tag{4}$$

for all $\boldsymbol{u}(a) \neq \mathbf{0}$ and zero initial conditions. (ii) It provides a less strict stability criterion which guarantees the exponential stability for the DTDS (1)–(3) with $\boldsymbol{u}(a) = \mathbf{0}$. The parameter γ is a scalar and represents the attenuation or $\mathbf{H}_\infty$ level.

3 Main Results

This section presents a criterion for the stability of the DTDS.

Theorem 1 For a known $\gamma > 0$, the DTDS (1)–(3) is exponentially stable, if there be matrices $\mathbf{K} > \mathbf{0}$, $\mathbf{Z}_i > \mathbf{0}$ $(i = 1, 2, \ldots, s)$, $\mathbf{F} > \mathbf{0}$, diagonal matrices $\mathbf{X} > \mathbf{0}$ and $\mathbf{W} > \mathbf{0}$ satisfying

$$\mathbf{R}_1 = \begin{bmatrix} \mathrm{T}_1 & \mathrm{T}_2 & \cdots & \mathrm{T}_4 & (k_q+k_o)\mathbf{A}^T\mathbf{X} & \mathbf{0} \\ * & \mathrm{T}_3 & \cdots & \mathrm{T}_5 & (k_q+k_o)\mathbf{A}_{d1}^T\mathbf{X} & \mathbf{0} \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots \\ * & * & * & \mathrm{T}_6 & (k_q+k_o)\mathbf{A}_{ds}^T\mathbf{X} & \mathbf{0} \\ * & * & * & * & -2\mathbf{X}+\mathbf{K}-\mathbf{W} & \mathbf{K} \\ * & * & * & * & * & \mathbf{K}-\gamma^2\mathbf{I} \end{bmatrix} < \mathbf{0} \tag{5}$$

where

$$\mathrm{T}_1 = \mathbf{F} - \mathbf{K} - 2k_q k_o \mathbf{A}^T\mathbf{X}\mathbf{A} + \sum_{i=1}^{s} \mathbf{Z}_i + k_q^2 \mathbf{A}^T\mathbf{W}\mathbf{A}$$

$$\mathrm{T}_2 = -2k_q k_o \mathbf{A}^T\mathbf{X}\mathbf{A}_{d1} + k_q^2 \mathbf{A}^T\mathbf{W}\mathbf{A}_{d1}$$

$$\mathrm{T}_3 = -2k_q k_o \mathbf{A}_{d1}^T\mathbf{X}\mathbf{A}_{d1} - \mathbf{Z}_1 + k_q^2 \mathbf{A}_{d1}^T\mathbf{W}\mathbf{A}_{d1}$$

$$\mathrm{T}_4 = -2k_q k_o \mathbf{A}^T \mathbf{X} \mathbf{A}_{ds} + k_q^2 \mathbf{A}^T \mathbf{W} \mathbf{A}_{ds}$$

$$\mathrm{T}_5 = -2k_q k_o \mathbf{A}_{d1}^T \mathbf{X} \mathbf{A}_{ds} + k_q^2 \mathbf{A}_{d1}^T \mathbf{W} \mathbf{A}_{ds}$$

$$\mathrm{T}_6 = -2k_q k_o \mathbf{A}_{ds}^T \mathbf{X} \mathbf{A}_{ds} - \mathbf{Z}_s + k_q^2 \mathbf{A}_{ds}^T \mathbf{W} \mathbf{A}_{ds}$$

Proof Consider the LKF of the form:

$$V(\boldsymbol{\sigma}(a)) = \boldsymbol{\sigma}^T(a) \boldsymbol{K} \boldsymbol{\sigma}(a) + \sum_{i=1}^{s} \sum_{j=-d_i}^{-1} \boldsymbol{\sigma}^T(a+j) \mathbf{Z}_i \boldsymbol{\sigma}(a+j), \tag{6}$$

Now, the forward difference of (6) is

$$\begin{aligned}
\Delta V(\boldsymbol{\sigma}(a)) &= V(\boldsymbol{\sigma}(a+1)) - V(\boldsymbol{\sigma}(a)), \\
&= (\Psi(\mathbf{y}(a)) + \mathbf{u}(a))^T \boldsymbol{K} (\Psi(\mathbf{y}(a)) + \mathbf{u}(a)) \\
&\quad - \boldsymbol{\sigma}^T(a) \left[\boldsymbol{K} - \sum_{i=1}^{s} \mathbf{Z}_i \right] \boldsymbol{\sigma}(a) \\
&\quad - \sum_{i=1}^{s} \boldsymbol{\sigma}^T(a-d_i) \mathbf{Z}_i \boldsymbol{\sigma}(a-d_i) \\
&= \Psi^T(\mathbf{y}(a)) \boldsymbol{K} \Psi(\mathbf{y}(a)) + \Psi^T(\mathbf{y}(a)) \boldsymbol{K} \mathbf{u}(a) + \mathbf{u}(a)^T \boldsymbol{K} \mathbf{u}(a) \\
&\quad + \mathbf{u}(a)^T \boldsymbol{K} \Psi(\mathbf{y}(a)) \\
&\quad - \boldsymbol{\sigma}^T(a) \left[\boldsymbol{K} - \sum_{i=1}^{s} \mathbf{Z}_i \right] \boldsymbol{\sigma}(a) - \sum_{i=1}^{s} \boldsymbol{\sigma}^T(a-d_i) \mathbf{Z}_i \boldsymbol{\sigma}(a-d_i),
\end{aligned} \tag{7}$$

Consider a non negative function ∂,

$$\begin{aligned}
\partial = 2 \, [& \boldsymbol{\Psi}^T(\mathbf{y}(a)) \mathbf{X} \, \boldsymbol{\Psi}(\mathbf{y}(a)) + k_o k_q \mathbf{y}^T(a) \mathbf{X} \, \mathbf{y}(a) \\
& - (k_q + k_o) \mathbf{y}^T(a) \mathbf{X} \boldsymbol{\Psi}(\mathbf{y}(a))].
\end{aligned} \tag{8}$$

For diagonal matrix $\mathbf{W} > \mathbf{0}$, one may obtain

$$k_q^2 \mathbf{y}^T(a) \mathbf{W} \mathbf{y}(a) - \boldsymbol{\Psi}^T(\mathbf{y}(a)) \mathbf{W} \, \boldsymbol{\Psi}(\mathbf{y}(a)) \geq 0. \tag{9}$$

From (1b), (7)–(9), we have

$$\begin{aligned}
\Delta V(\boldsymbol{\sigma}(a)) = & \Psi^T(\mathbf{y}(a)) \boldsymbol{K} \Psi(\mathbf{y}(a)) + \Psi^T(\mathbf{y}(a)) \boldsymbol{K} \mathbf{u}(a) \\
& + \mathbf{u}(a)^T \boldsymbol{K} \mathbf{u}(a) + \mathbf{u}(a)^T \boldsymbol{K} \Psi(\mathbf{y}(a))
\end{aligned}$$

$$
\begin{aligned}
&- \boldsymbol{\sigma}^T(a)\left[\boldsymbol{K} - \sum_{i=1}^{s} \mathbf{Z}_i\right]\boldsymbol{\sigma}(a) - \sum_{i=1}^{s} \boldsymbol{\sigma}^T(a-d_i)\mathbf{Z}_i\boldsymbol{\sigma}(a-d_i) \\
&- 2\,[\boldsymbol{\Psi}^T(\mathbf{y}(a))\mathbf{X}\,\boldsymbol{\Psi}(\mathbf{y}(a)) + k_o k_q \mathbf{y}^T(a)\mathbf{X}\,\mathbf{y}(a) \\
&- (k_q + k_o)\mathbf{y}^T(a)\mathbf{X}\boldsymbol{\Psi}(\mathbf{y}(a))] \\
&+ k_q^2 \mathbf{y}^T(a)\mathbf{W}\mathbf{y}(a) - \Psi^T(\mathbf{y}(a))\mathbf{W}\,\Psi(\mathbf{y}(a)) + \partial. \qquad (10)
\end{aligned}
$$

Next, addition and subtraction of $(\boldsymbol{\sigma}^T(a)\mathbf{F}\sigma(a) - \gamma^2 \boldsymbol{u}^T(a)\boldsymbol{u}(a))$ with (10) gives

$$
\Delta V(\boldsymbol{\sigma}(a)) \leq \tilde{\boldsymbol{\sigma}}^T(a)\mathbf{R}_1\tilde{\boldsymbol{\sigma}}(a) - \boldsymbol{\sigma}^T(a)\mathbf{F}\boldsymbol{\sigma}(a) + \gamma^2 \boldsymbol{u}^T(a)\boldsymbol{u}(a) + \partial, \qquad (11)
$$

where

$$
\tilde{\boldsymbol{\sigma}}^T(a) = [\,\boldsymbol{\sigma}^T(a)\ \boldsymbol{\sigma}^T(a-d_1)\ \cdots\ \boldsymbol{\sigma}^T(a-d_s)\ \boldsymbol{\Psi}^T(\mathbf{y}(a))\ \boldsymbol{u}^T(a)\,].
$$

From (11), one can examine that

$$
\Delta V(\boldsymbol{\sigma}(a)) < -\boldsymbol{\sigma}^T(a)\mathbf{F}\boldsymbol{\sigma}(a) + \gamma^2 \boldsymbol{u}^T(a)\boldsymbol{u}(a), \qquad (12)
$$

with $\tilde{\boldsymbol{\sigma}}^T(a) \neq \mathbf{0}$, if (5) holds. Summation of (12) on both sides from 0 to ∞ gives

$$
V(\boldsymbol{\sigma}(\infty)) - V(\boldsymbol{\sigma}(0)) < \sum_{a=0}^{\infty} \gamma^2 \boldsymbol{u}^T(a)\boldsymbol{u}(a) - \sum_{a=0}^{\infty} \boldsymbol{\sigma}^T(a)\mathbf{F}\boldsymbol{\sigma}(a). \qquad (13)
$$

As $V(\boldsymbol{\sigma}(0)) = 0$ and $V(\boldsymbol{\sigma}(\infty)) \geq 0$, the relation (4) is satisfied.

Next, it is necessary to show that the DTDS (1)–(3) with $\boldsymbol{u}(a) = \mathbf{0}$ is exponentially stable under the situation (5). $V(\boldsymbol{\sigma}(a))$ satisfies Rayleigh inequality [23]

$$
\begin{aligned}
\left[\lambda_{\min}(\mathbf{K}) + \sum_{i=1}^{s} \lambda_{\min}(\mathbf{Z}_1)\right]||\boldsymbol{\sigma}(a)||^2 &\leq V(\boldsymbol{\sigma}(a)) \\
&\leq \left[\lambda_{\max}(\mathbf{K}) + \sum_{i=1}^{s} \lambda_{\max}(\mathbf{Z}_1)\right]||\boldsymbol{\sigma}(a)||^2. \qquad (14)
\end{aligned}
$$

With $\boldsymbol{u}(a) = \mathbf{0}$, (12) becomes

$$
\Delta V(\boldsymbol{\sigma}(a)) < -\boldsymbol{\sigma}^T(a)\mathbf{F}\boldsymbol{\sigma}(a) \leq \lambda_{\min}(\mathbf{F})||\boldsymbol{\sigma}(a)||^2. \qquad (15)
$$

In the light of Theorem 1 in [22], (14) and (15) guarantee the exponential stability of the DTDS (1)–(3). This concludes the proof.

Remark 1 The condition (5) is in LMI form and can be solved by software MATLAB [24, 25].

Remark 2 Unlike the criterion [21], the presented criterion is applicable for external interference, FWN and state delay.

Remark 3 Many researchers derived the $\mathbf{H}_\infty$ performance criteria [8, 15–18, 22] for system with saturation and external interference. These approaches [8, 15–18, 22] cannot tackle the nonlinearities caused by FWN. On the other hand, Theorem 1 presents a novel condition for the exponential stability of DTDS (1)–(3) with FWN, external interference and state delay.

Remark 4 The $\mathbf{H}_\infty$ norm can be illustrated as [26]:

$$\boldsymbol{H}(a) = \frac{\sum_{z=0}^{a} \boldsymbol{\sigma}^T(z)\mathbf{F}\boldsymbol{\sigma}(z)}{\sum_{z=0}^{a} \mathbf{u}^T(z)\,\mathbf{u}(z)}. \tag{16}$$

For a given $\gamma > 0$, (4) can be symbolized by $\boldsymbol{H}(\infty) < \gamma^2$ which corresponds to (16).

4 Special Cases

This section presents some special cases of our main result.

Corollary 1 The system (1)–(3) without state delay, i.e.

$$\boldsymbol{\sigma}(a+1) = \boldsymbol{\Psi}(\boldsymbol{A}\boldsymbol{\sigma}(a)) + \mathbf{u}(a). \tag{17}$$

The system (2), (3) and (17) is exponentially stable with known $\gamma > 0$, if there be diagonal matrices $\mathbf{X} > \mathbf{0}$ and $\mathbf{W} > \mathbf{0}$, matrices $\mathbf{K} > \mathbf{0}$, $\mathbf{F} > \mathbf{0}$, satisfying

$$\mathbf{R}_2 = \begin{bmatrix} \mathrm{T}_1 & (k_q+k_o)\mathbf{A}^T\mathbf{X} & \mathbf{0} \\ * & -2\mathbf{X}+\mathbf{K}-\mathbf{W} & \mathbf{K} \\ * & * & \mathbf{K}-\gamma^2\mathbf{I} \end{bmatrix} < \mathbf{0}, \tag{18}$$

where

$$\mathrm{T}_1 = \mathbf{F} - \mathbf{K} - 2k_qk_o\mathbf{A}^T\mathbf{X}\mathbf{A} + k_q^2\mathbf{A}^T\mathbf{W}\mathbf{A}.$$

Proof Select the LKF (6) with $\mathbf{Z}_i = \mathbf{0}$. Now, with $\mathbf{A}_{di} = \mathbf{0}$, (11) becomes

$$\Delta V(\boldsymbol{\sigma}(a)) \le \hat{\boldsymbol{\sigma}}^T(a)\mathbf{R}_2\hat{\boldsymbol{\sigma}}(a) - \boldsymbol{\sigma}^T(a)\mathbf{F}\boldsymbol{\sigma}(a) + \gamma^2\boldsymbol{u}^T(a)\boldsymbol{u}(a) + \partial \tag{19}$$

where

$$\hat{\boldsymbol{\sigma}}^T(a) = \left[\, \boldsymbol{\sigma}^T(a)\ \boldsymbol{\Psi}^T(\mathbf{y}(a))\ \boldsymbol{u}^T(a) \,\right]$$

The remaining proof follows the similar steps as shown in the proof of Theorem 1.

Remark 5 Corollary 1 presents the stability criterion for discrete system with FWN and external interference. By considering $\mathbf{Z}_i = \mathbf{0}$ and $\mathbf{A}_{di} = \mathbf{0}$ in (5), one may get the result [21, Theorem 1] which is similar to (18). Thus, Theorem 1 [21] acts as a special case of Theorem 1.

Next, consider the DTDS (1)–(3) in absence of external interference. Pertaining this situation, we have the following corollary.

Corollary 2 The DTDS (1)–(3) with $\boldsymbol{u}(a) = \mathbf{0}$ becomes

$$\boldsymbol{\sigma}(a+1) = \boldsymbol{\Psi}(\mathbf{y}(a)) \tag{20a}$$

$$\boldsymbol{y}(a) = \boldsymbol{A}\boldsymbol{\sigma}(a) + \sum_{i=1}^{s} \boldsymbol{A}_{di}\boldsymbol{\sigma}(a-d_i) \tag{20b}$$

Then the DTDS (20) is globally asymptotic stable, if there be matrices $\mathbf{K} > \mathbf{0}$, $\mathbf{Z}_i > \mathbf{0}$ $(i = 1, 2, \ldots, s)$, diagonal matrices $\mathbf{X} > \mathbf{0}$ and $\mathbf{W} > \mathbf{0}$ satisfying

$$\mathbf{R}_3 = \begin{bmatrix} \mathrm{T}_1 & \mathrm{T}_2 & \cdots & \mathrm{T}_4 & (k_q+k_o)\mathbf{A}^T\mathbf{X} \\ * & \mathrm{T}_3 & \cdots & \mathrm{T}_5 & (k_q+k_o)\mathbf{A}_{d1}^T\mathbf{X} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ * & * & * & \mathrm{T}_6 & (k_q+k_o)\mathbf{A}_{dr}^T\mathbf{X} \\ * & * & * & * & -2\mathbf{X}+\mathbf{K}-\mathbf{W} \end{bmatrix} < \mathbf{0} \tag{21}$$

Proof With $\boldsymbol{u}(a) = \mathbf{0}$, (11) becomes

$$\Delta V(\boldsymbol{\sigma}(a)) \leq \overline{\boldsymbol{\sigma}}^T(a)\mathbf{R}_3\overline{\boldsymbol{\sigma}}(a) + \partial \tag{22}$$

where

$$\overline{\boldsymbol{\sigma}}^T(a) = \left[\boldsymbol{\sigma}^T(a)\ \boldsymbol{\sigma}^T(a-d_1) \cdots \boldsymbol{\sigma}^T(a-d_s)\ \boldsymbol{\Psi}^T(\mathbf{y}(a))\right].$$

Equation (22) satisfies $\Delta V(\boldsymbol{\sigma}(a)) \leq 0$ if (21) holds true. This completes the proof.

Remark 6 Corollary 2 presents the stability criterion which guarantees the absence of limit cycles in DTDS employing FWN.

5 Illustrative Example

To explain the utility of the presented criteria, let us consider an example of DTDS with

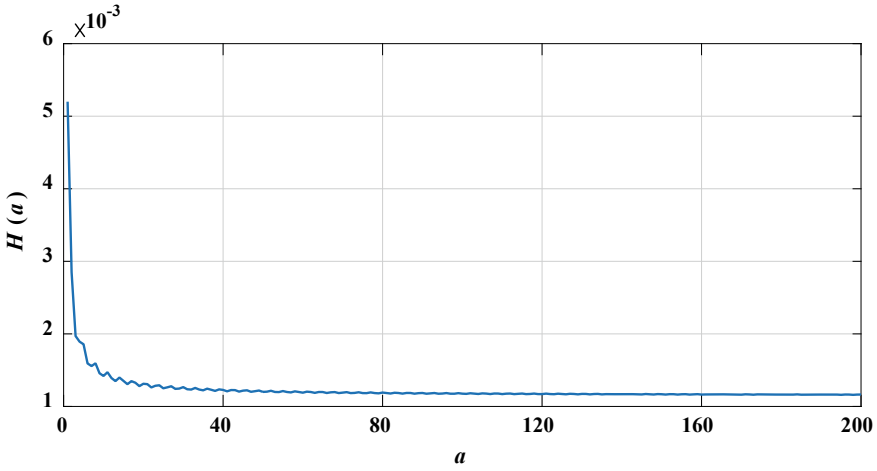

Fig. 1 The plot of $\mathbf{H}(a)$

$$\mathbf{A} = \begin{bmatrix} 0.25 & 0.5 \\ -0.5 & 0.7 \end{bmatrix}, \mathbf{A}_{d1} = \begin{bmatrix} 0 & 0.001 \\ 0.001 & 0 \end{bmatrix}, \mathbf{u}(a) = \begin{bmatrix} \cos(a) \\ \sin(a) \end{bmatrix}, k_o = -1, \quad k_q = 1. \tag{23}$$

For the design purpose (4), suppose $\gamma = 0.5$. Using the software MATLAB LMI toolbox [24, 25], Theorem 1 provides feasible solutions for the present example. The approaches in [1, 6, 7, 13, 14, 19] cannot be utilized to check the exponential stability of the system (1)–(3).

As discussed in [26], the condition (4) can be represented by $\mathbf{H}(\infty) < \gamma^2$ where

$$\mathbf{H}(a) = \frac{\sum_{a=0}^{\infty} \boldsymbol{\sigma}^T(a)\mathbf{F}\sigma(a)}{\sum_{a=0}^{\infty} \boldsymbol{u}^T(a)\boldsymbol{u}(a)}. \tag{24}$$

The plot of $\mathbf{H}(a)$ for the present example interprets in Fig. 1. It is apparent from Fig. 1 that $\mathbf{H}(\infty) < 0.25$. Thus, the $\mathbf{H}_\infty$ norm from $\boldsymbol{u}(a)$ to $\boldsymbol{\sigma}(a)$ is restricted with in attenuation level γ.

6 Conclusion

A criterion addressing the stability of DTDS with FWN and external interference has been established. Theorem 1 also assures the exponential stability and reduces the influence of interference to $\mathbf{H}_\infty$ level. The presented approach offers an improved stability domain in comparison with the existing approaches. The appropriateness of the result proposed in this paper has been exemplified by an example.

Many works have been presented for 2-*D* systems as they have broad applications in various regions like X-ray image management, power transmission lines [27], geophysics, projective radiography [28], Markov jump systems [20] and so on. Extension of the work presented in this paper to 2-*D* systems with FWN and external interference would also be an appealing area for future investigation.

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Study and Design of a Novel Half Adder Circuit Using QCA Gates with Optimized Parameters

Shubhra Dubey, Vandana Shukla, O. P. Singh, and G. R. Mishra

1 Introduction

It is well known that quantum dot cellular automaton (QCA) displays the signs of success in the current scenario of computing system by replacing the CMOS technology [1]. In the past, the CMOS technology had the recognition for its importance, but in today's scenario, this technology is being worsening to meet all the requirements, such as high-power consumption by CMOS technology, loss of information, and slow speed [2–4]. So, to overcome these problems, a large number of technologies are spread around us, but best suited technology is quantum-dot cellular automatons (QCA).

Now this QCA technology is very powerful approach in the field computation which gives a new approach to the computing systems at nano-levels [5, 6]. QCA technology was proposed by the Tougaw and Lent in 1993 [7, 8]. In the past few years, the QCA technology had made very dynamic changes in the field of electronic devices, such as reducing the complexity of the circuit, fast speed, less area consumption, reducing the size of the components, and decreasing the power consumption capacity. In QCA, a cell contains holes and electrons, and here, binary information in the QCA technology is encoded by the positions of electrons and information travels because of coulombic interaction among QCA cells [9, 10]. The polarization of electrons in one QCA cell makes the interconnection with the other neighbor's cells and binary information passes on. One of the best features of this technology is that there is zero current in between the cells, or there is no power supply for communication.

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Table 1 Existing designs of half adder circuit

Year	Author's name	Cells count	No. of gates	Clock delay
2014 [1]	Santra and Roy	64	4 (one OR and rest three is AND gate)	1
2014 [3]	Subhashee et al.	80	3 (one OR gate and rest two is AND gate)	1
2011 [6]	Karthigai Lakshmi and Athisha	77	3 (one OR gate and two AND gate)	1

The specialty of this technology is that logic information is represented by the cells. This QCA technology has solutions for the problems that we are facing in CMOS technology such as low power consumption and high-speed data. The circuits of the adder are the basic requirements in the field of the digital computing systems. Many QCA based circuit designs for half adder have been already pointed out by different researchers in the past. Some of them are mentioned in Table 1.

In this paper, we have shown QCA design for the half adder with the smaller number of cell counts, and the simulation of the proposed half adder circuit and the result have been checked on the QCA designer tool version 2.0.3.

The rest of this paper is organized in five sections. This section is Introduction of the proposed work, Sect. 2 contains basic information about QCA that describe wires, basic logics, and clocking system. Section 3 is about the proposed half adder circuit. Section 4 presents result and analysis of the proposed circuit design, and in Sect. 5, overall conclusion of paper is presented.

2 Fundamentals of QCA

Quantum dot cellular automata (QCA) technology contains four quantum dots in a square-shaped cell. These quantum dots are placed at the corners of the square-shaped cell consists of one electron. In each cell, there are two mobile electrons which are present and shown in Fig. 1.

The electrons in the cell are tunnel in between the dots within the cell but unable to move out from their cell [11, 12]. Electrons in the cells are located as diagonally and opposite to the quantum dots of the cells due to tight binding of electrostatic force of interaction. This quantum dot is made of a nano-semiconductor material having very small diameter such that its supplied energy is greater than k_bT. Here, k_b is constant known as the Boltzmann's constant, and T is room temperature [13].

Logic circuits and Clocking Scheme of the QCA technology

Some of the important terms in QCA technology are QCA wire, complement, and majority gate which are presented in Fig. 2 [13, 14]. Figure 2a shows the QCA wire which is made from the QCA cells. An array of these QCA cells is placed to

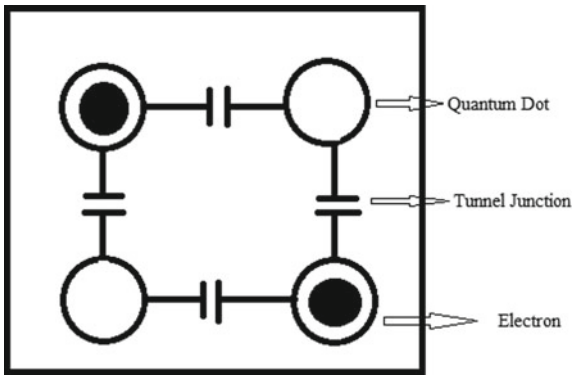

Fig. 1 QCA cell consist of dots, electrons, and tunnel junction

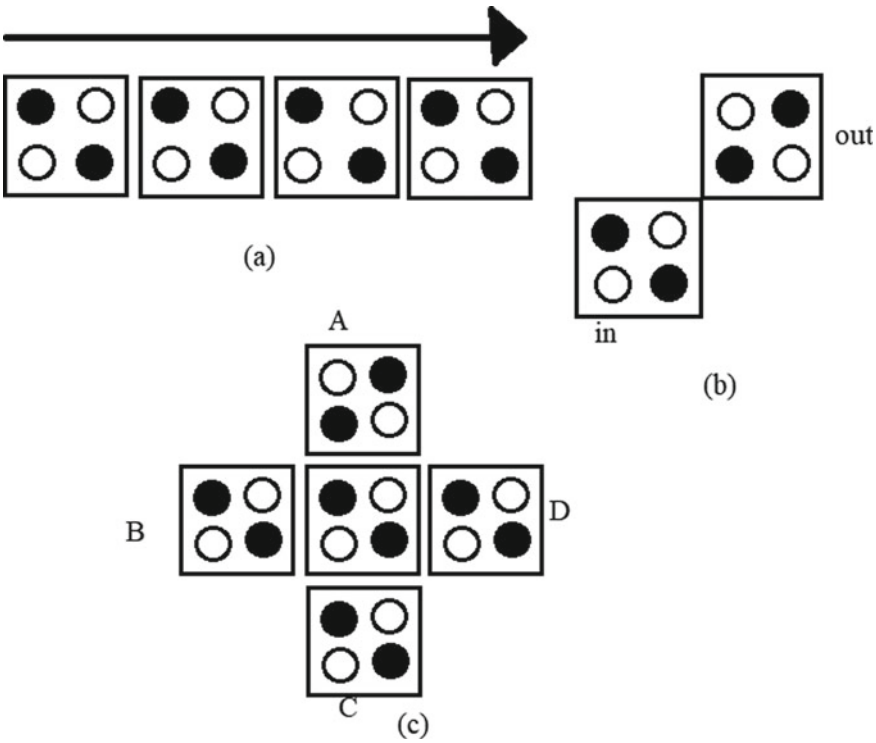

Fig. 2 **a** Wire of QCA cells, **b** simplest form of inverter gate, **c** majority gate and its symbol

form a QCA wire, based on the Coulomb theory of interactions. These wires are responsible for the travel of information from one end to another. Figure 2b shows the very common and simplest form of inverter by putting two cells diagonally apart.

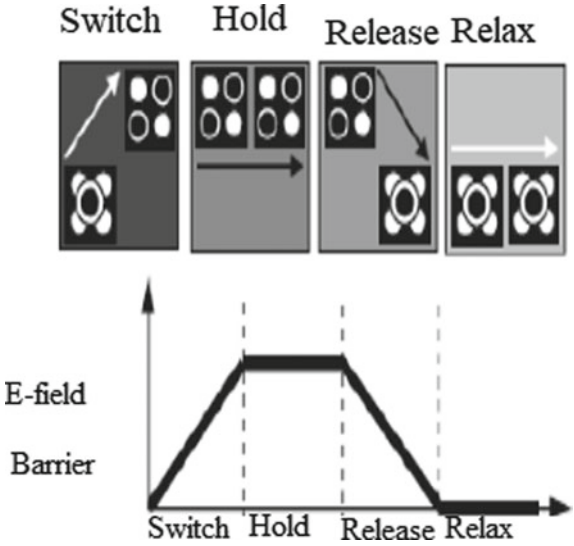

Fig. 3 Representation of a four clock phases

Figure 2c shows the symbol of the majority gate and its QCA implementation. From this majority gate, we can make the AND/OR gate also by setting one of the inputs for majority gate with the polarization 1 or −1. Here, if we provide the polarization 1 to the majority gate, it will work as a OR gate, whereas if we give polarization value −1, then it works as a AND gate [15].

Clocking scheme of the QCA technology has a four clock zones, and these four zones have four phases in it [16, 17]. The operations of these clock zones and its phases are shown in Fig. 3.

3 Proposed Design of Half Adder in QCA Technology

Among arithmetic operations, addition is one of the most vital parts in the field of the digital computers. Half adder is basically doing the addition of two bits. Basically, a half adder requires one 2-input exclusive OR gate along with one 2-input AND gate. Both A and B input signals are applied to XOR and AND gate to provide outputs as SUM and CARRY. Here, output SUM and CARRY are described as (Table 2):

SUM = A XOR B
CARRY = A AND B.

Previously many design approaches of half adder have been proposed using QCA technology [18]. The main purpose of this paper is to present a QCA design for half adder circuit which contains a smaller number of cells and less complex as compared to previously proposed designs by different researchers. For the implementation and

Table 2 Truth table of the half adder

INPUT		OUTPUT	
X	Y	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

simulation of proposed half adder circuit and to verify its results, we have used the freely available tool named as QCA designer tool version 2.0.3.

Proposed QCA Design of Half Adder

Figure 4 show our proposed half adder implemented in QCA technology. The circuit has been implemented in area 0.03 um^2 as shown by QCA designer tool. This proposed circuit has been designed from 26 cells only. In this case, there are two input cells and two output cells which are named as 'A' and 'B' (input cells) and 'SUM' and 'CARRY' (output cells). Colors of inputs and output cells are blue and yellow, respectively. Two clocks are used in proposed design named as Clock 0 in green color and clock 1 in purple color for proper functioning of circuit. There are no crossover cells and multi-layer cells in the proposed circuit design.

The proposed design of QCA based half adder circuit is better in terms of some key parameters from the previously proposed designs (Table 3).

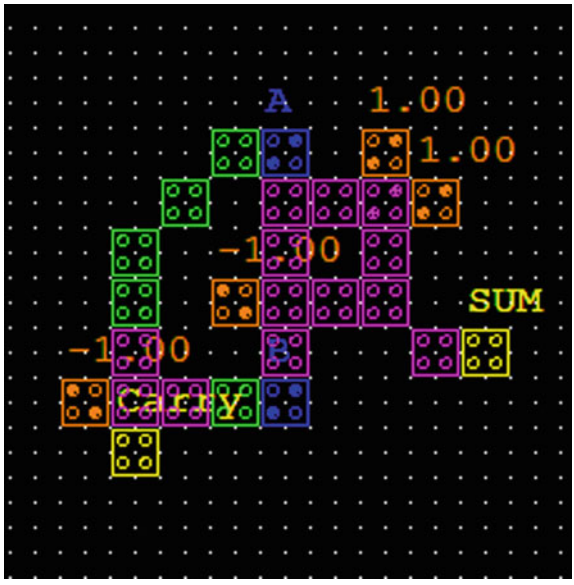

Fig. 4 Proposed half adder QCA circuit in QCA designer tool

Table 3 Parameters of proposed design

Area	No. of cells	Delay factor	File opened
0.03 μm^2	26	0.50	0.27 s

4 Result and Analysis of Proposed QCA Based Half Adder Design

Figures 5 and 6 show the simulation results of our proposed design of half adder circuit implemented in QCA technology. The simulation is performed on the QCA designer tool version 2.0.3. Here, simulation type is exhaustive by default, and the output of simulation result is same in both the engines setup, i.e., bi-stable engine and coherence vector engine. In the bi-stable engine, the simulation results have been obtained as two inputs and two outputs with total 26 cells, total initialization time 0 s, and total simulation time 4 s. The total simulation time taken by coherence vector engine is 13 s, and Euler method is used for coherence vectors.

Table 4 shows the comparison of proposed half adder design with the existing designs. Here, evaluation is performed on some selected parameters such as number of cells, clock cycle, number of gates used, and area. From this comparison table, we may deduce that our anticipated design is most optimized design as compared to existing ones.

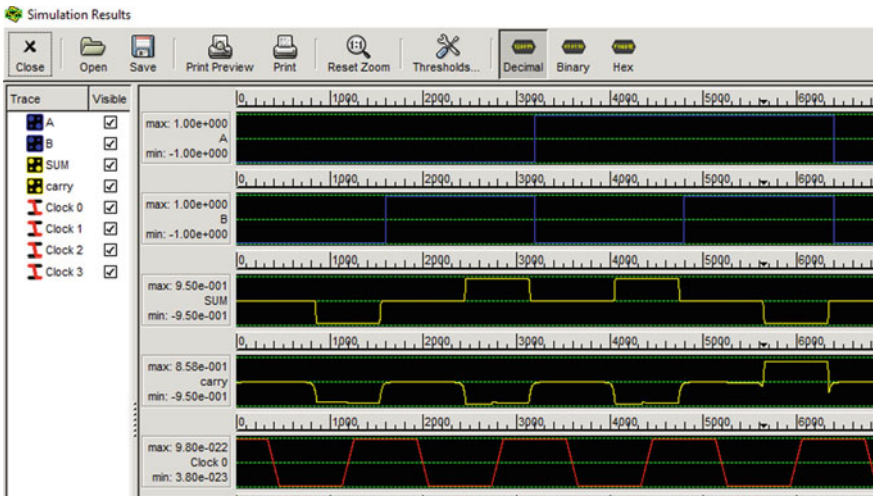

Fig. 5 Simulation results of proposed QCA half adder

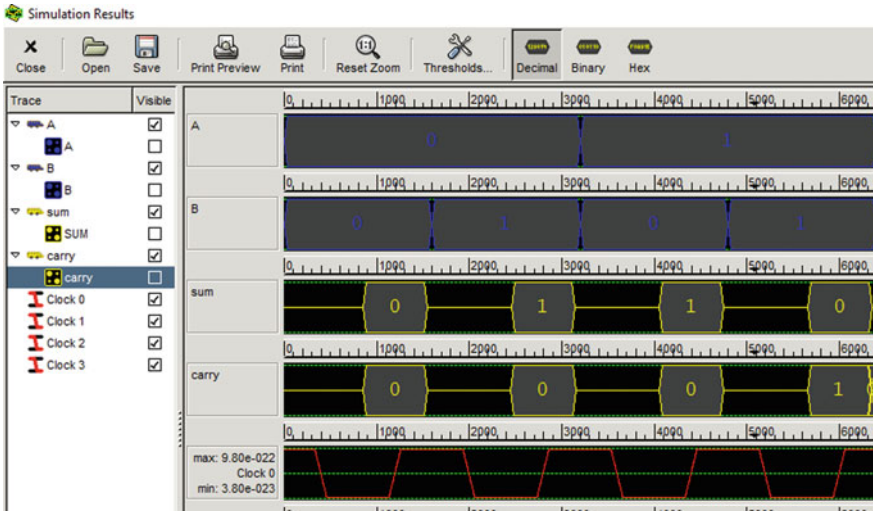

Fig. 6 Simulation results of proposed QCA half adder in digital form

Table 4 Comparison table

Design	No. of cells	Clock cycle	No. of gates used	Area in um^2
Existing design [1]	65	1	4	0.09
Existing design [2]	62	2	5	0.08
Existing design [3]	80	1	4	0.10
Existing design [4]	48	0.5	3	0.04
Existing design [6]	77	1	3	–
Existing design [9]	61	0.75	4	0.08
Existing design [10]	44	1	5	0.05
Proposed design structure of half adder	26	0.5	2	0.03
Improvement (%)	40.9	50	60	40

5 Conclusion

Here in this paper, we have proposed a novel approach to design an optimized QCA based half circuit. The simulation of proposed circuit has been performed on QCA designer tool version 2.0.3. From comparison table, it is inferred that the simulated results of proposed circuit are better as compared to other designed circuits reported by different researchers in terms of various key parameters. The circuit has been optimized in terms of number of cells, design area, and clock delay. Moreover, the

clocking scheme is done in proper manner for functioning of proposed circuit [18–20]. Further the proposed design may be used to reduce the complexity of various computing circuits with reduced area and number of cells.

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Low-Power Enhanced Speed Two-Tail Dynamically Controlled Comparator Suitable for Subthreshold CMOS Circuits

Avaneesh Kumar Dubey, Vikrant Varshney, Ankur Kumar, Pratosh Kumar Pal, and Rajendra Kumar Nagaria

1 Introduction

The most of devices in communication systems and consumer electronics use voltage reference circuits (VRC) [1], operational trans-conductance amplifiers (OTAs) [2–5], analog-to-digital converters (ADCs) [6–8] etc. as these are most likely to be portable and battery run. Therefore, these devices are required to be low-power, high-speed, and operational at very low power supply [9, 10]. In VLSI circuits, the digital and analog circuits can be integrated together due to the integration of the large number of transistors on a single chip. The digital circuits have the advantage over the analog circuits because of their smaller production cost and faster speed. But, on the other side, the analog circuits have their own importance as an inevitable interface between the digital and physical world. Eventually, the design of analog circuits sets the platform for the performance of the digital technology.

The conversion between analog and digital signal is one of the most important function in signal processing [6]. Analog-to-digital converter (ADC) [7, 8] typically contains one or more dynamic comparators, digital circuits, integrators, sample-and-hold and passive components. The dynamic comparator [11–27] is widely used in the

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process of converting analog signals to digital signals. In A/D conversion process, it is necessary to first sample the signals. This sampled signal then applied to the combination of dynamic comparators to determine the digital equivalent of analog signal. In the simplest form, the comparator can be considered as 1-bit ADC [13–15]. Dynamic comparators are the basic building blocks in Analog/Mixed-signal processing circuits [18, 19]. The demand for portable devices with high-speed and long battery life is increasing rapidly in modern communication systems. CMOS technology is scaled down (below 40 nm) to fulfill the demands [22, 26, 27]. It is difficult to scale down the threshold voltage of transistors with same rate which is limited the down scaling of supply voltage with channel length. It makes difficult to work at ultra-low-voltage power supply. These challenges produce more interest toward new design ideas for high-speed and low power supply.

The basic dynamic comparator is nothing but single tail dynamically controlled comparator (STDCC) [12]. STDCC suffers from nonlinear error because of distortion in input signal which is called kickback noise [11]. It dissipates also higher power and unable to work low power supply due to stacking problem. In order to solve this problem, two-tail dynamically controlled comparator (TTDCC) [13–15] came into picture. TTDCC is designed using amplification stage, latch stage and buffer stage. Amplification stage is basically a differential amplifier and latch stage is the combination of CMOS inverters with positive feedback. The amplification stage should be designed for low power, low-offset voltage, high gain and large CMR. The latch should be designed for high speed and low power. To reduce the offset voltage of input stage, the input transistor size should be large enough. Large transistors dissipate more power. The BD technique [10] and hybrid design technique [14] can be involved to reduce the power dissipation and delay at differential stage. The conventional BD techniques suffer from low trans-conductance. So, various novel techniques are desired to overcome above said challenges. There are several TTDCC designs proposed earlier that are Conv TTDCC [12], Hybrid TTDCC [14], BDL-TTDCC [18], TTDCC with self-biased technique [22], charge sharing-based TTDCC [25, 27], UC-TTDCC [26] etc.

From the above explained designs, it is noticeable that these designs are efficient, but unable to work at very low power supply. Therefore, there is a requirement of such novel design which can work for subthreshold CMOS circuits design. In this paper, a novel high-speed low power low-voltage TTDCC is proposed using the Gain Control by Bulk Amplification (GACOBA) loads, which is an advanced version of bulk-driven method to break standstill in power consumption and delay. In the proposed TTDCC, the latch stage uses GACOBA load and the differential stage uses bulk-driven load which enhances the speed and is able to work at very low power supply. The remainder of the paper is organized as follows: the proposed design is elaborated in Sect. 2 with detailed delay and kickback noise analysis. In Sect. 3, the results are discussed and Sect. 4 infers the paper.

2 Proposed Two-Tail Dynamically Controlled Comparator (TTDCC)

2.1 Circuit Implementation

The circuit diagram of the proposed TTDCC is illustrated in Fig. 1. Here, the differential stage is designed with BDL PMOS [18] (transistors Mb1 and Mb2 inside the

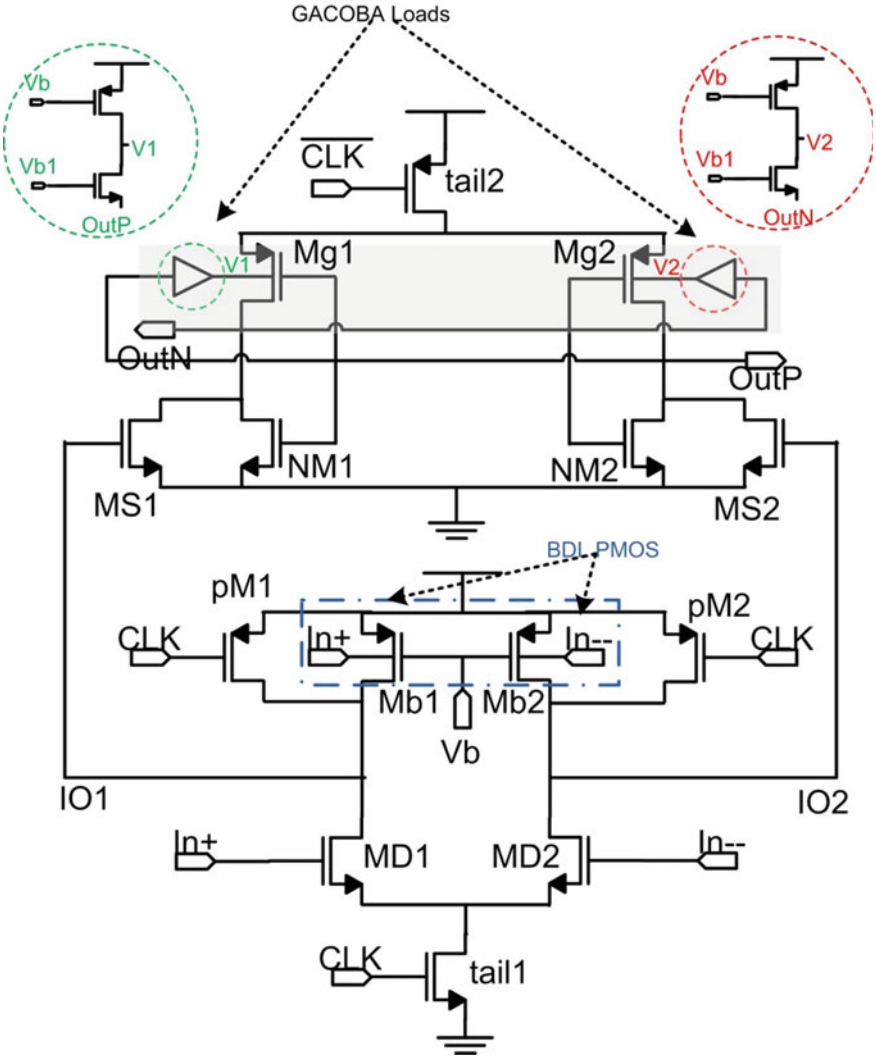

Fig. 1 The circuit diagram of the Proposed TTDCC

blue dotted region). The driver transistors are MD1 and MD2, where common mode voltage (V_{CM}) and differential inputs (ΔV_{IN}) are applied. This stage amplifies the differential input and the intermediate stage outputs (V_{IO1} and V_{IO2}) are obtained. The Vb is the biasing voltage used to bias BDL PMOS transistors as well as GACOBA loads in the subthreshold region. The bulk terminals of these transistors (Mb1, Mb2, Mg1 and Mg2) are connected separately. The bulk terminals of other transistors are connected according the conventional rule such as bulk of PMOS with power supply (V_{DD}) and bulk of NMOS with ground (GND). The combination of NM1/NM2 and Mg1/Mg2 transistors make dynamic inverters in latch stage. The effective transconductance of this stage is improved by the application of GACOBA loads PMOS (Mg1 and Mg2) [10]. The same is illustrated in Fig. 1 by the green and red dotted region. There are two-tail transistors in the circuit, *tail1* and *tail 2*, used to provide operating tail current for differential stage and latch stage, respectively.

2.2 Operation of the Proposed TTDCC

The transient behavior at $V_{DD} = 0.8$ V, $V_{CM} = 0.7$ V, $\Delta V_{IN} = 10$ mV for the proposed TTDCC is illustrated in Fig. 2. Here, the operation of the proposed TTDCC is classified into two mode, amplification mode and comparison mode, depending on the status of clock (CLK) signal. When CLK signal is low, transistors pM1 and pM2 are on; transistors tail1 and tail2 are off. The parasitic capacitors associated with nodes V_{IO1} and V_{IO2} (C_{IO1} and C_{IO2}) are charging up to the V_{DD} through pM1/pM2 and Mb1/Mb2. Simultaneously, the load capacitors (C_{Lout}) associated with the latch stage outputs OutN and OutP are discharging through NM1 and NM2. Therefore, at the end of amplification mode, the voltages of OutN and OutP nodes are low; and the V_{IO1} and V_{IO2} are high. The same can be illustrated from Fig. 2 before $t = 2$ ns.

The comparison mode starts when CLK goes high. As soon as CLK = logic '1', pM1 and pM2 are off; and transistors tail1 and tail2 are on. At the very beginning of the comparison mode, due to high V_{IO1} and V_{IO2} the transistors MS1 and MS2 are on, holding OutP and OutN nodes at low. As soon as transistor tail1 becomes on, it enables discharging path for C_{IO1} and C_{IO2}. Now depending on the input condition

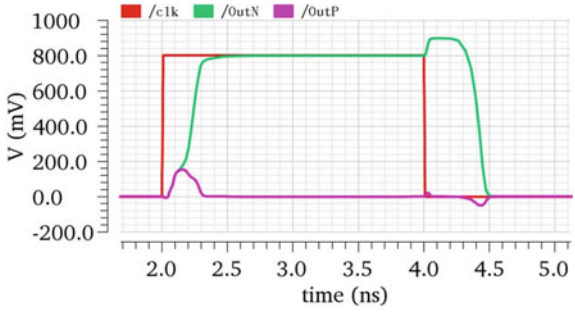

Fig. 2 The illustration of transient behavior at $V_{DD} = 0.8$ V, $V_{CM} = 0.7$ V, $\Delta V_{IN} = 10$ mV for the proposed TTDCC

(let us first consider In+ > In−), the discharging rate of V_{IO1} node is greater than V_{IO2}. Due to this phenomenon, the transistor MS1 turns off before MS2. The output nodes capacitor associated with MS1 transistor (i.e., OutN node) will start charging before OutP through the transistor Mg1. The latching property of latch stage gets activated at this point and comparison has been made. Therefore, at the end of comparison mode, OutN node is high and OutP node is low (for the input condition In+ > In−). The same operation is illustrated in Fig. 2 from $t = 2$ ns to $t = 4$ ns. The vice-versa operation will be performed by the proposed TTDCC when inputs are In+ < In−.

2.3 Delay Analysis

The BDL-TTDCC [18] is designed with the BDL PMOS differential stage. In this, the total delay (T_{Delay}) is given by following expression.

$$T_{\text{Delay}} = t_0 + T_{\text{latch}} = 2\frac{V_{\text{THN}} \cdot C_{\text{Lout}}}{I_{t2}} + \frac{C_{\text{Lout}}}{g_{m,eff} + g_{\text{mS1,2}}} \cdot \ln\left(\frac{V_{\text{DD}}}{2 \cdot \Delta V_0}\right) \quad (1)$$

where t_0 is the delay of differential stage, T_{Latch} is the delay of latch stage, $g_{m,\text{eff}}$ is effective trans-conductance of the differential stage, $g_{mS1,2}$ is the trans-conductance of transistor Ms1/Ms2, and ΔV_0 is expressed in the term of trans-conductance of several transistors.

$$\Delta V_0 = 2V_{\text{THN}} \cdot \frac{g_{\text{mS1,2}}}{I_{t2}}\left(g_{\text{m1,2}} + g_{\text{mb}L1,2}\right)\left(1 - \exp\left(-t_0/\tau_{\text{eq}}\right)\right)(r_{01,2}||r_{0L1,2})\Delta V_{\text{IN}} \quad (2)$$

where V_{THN} is the threshold voltage of NMOS transistors, the τ_{eq}, $g_{\text{m1,2}}$, $g_{\text{mbL1,2}}$, $r_{01,2}$ and $r_{0\text{L1,2}}$ are specified in [18].

From Eq. (2), it has been noticed that the large ΔV_0 can be achieved by improving trans-conductance of differential and latch stage. The large ΔV_0 reduces the latch stage delay (T_{Latch}) as detailed in Eq. (1). Therefore, ΔV_0 for the proposed TTDCC ($\Delta V_{0,\text{Prop.}}$) is derived as:

$$\Delta V_{0,\text{Prop.}} = 2V_{\text{THN}} \cdot \frac{G_{\text{mLatch,eff}}}{I_{t2}}\left(g_{m1,2} + g_{mbL1,2}\right)\left(1 - \exp\left(-t_0/\tau_{\text{eq}}\right)\right) (r_{01,2}||r_{0Lb1,2})\Delta V_{\text{IN}} \quad (3)$$

where $\text{gm}_{\text{bL1,2}}$ is the bulk trans-conductance of load transistors Mb1/Mb2, $r_{0\text{Lb1,2}}$ is the output resistance of load transistors Mb1/Mb2 and $G_{m\text{Latch,eff}} = g_{m\text{S1,2}} + \left(g_{mg1,2} + A_{V1}g_{m\text{bg1,2}}\right)$.

By including the effect of effective latch stage trans-conductance, the latch stage delay of the proposed TTDCC ($T_{\text{L,Prop.}}$) is expressed as:

$$T_{L,\text{Prop.}} = \frac{C_{\text{Lout}}}{g_{m,\text{eff}} + G_{m\text{Latch,eff}}} \cdot \ln\left(\frac{V_{\text{DD}}/2}{2V_{\text{THN}} \cdot 1\frac{G_{m\text{Latch,eff}}}{I_{t2}}\left(g_{m1,2} + g_{m\text{bL1,2}}\right)\left(1 - \exp\left(-t_0/\tau_{\text{eq}}\right)\right)\left(r_{01,2} \| r_{0Lb1,2}\right)\Delta V_{\text{IN}}}\right) \quad (4)$$

From Eqs. (3) and (4), it is clearly seen that the improvement in effective transconductance improves the total delay of the proposed TTDCC.

2.4 Reduction in Kickback Noise

In general, the kickback noise very effectively affects the input signal because of two reasons, the parasitic capacitances directly connected between output nodes and the input nodes, and the fast operating of latch stage in TTDCCs [11]. It is also known that the transient noises are much higher in fast performing dynamic circuits as compared to the static counterpart. The peaks in input voltage are generated due to this effect, called as peak input voltage (PIV) error. The simulation setup to analysis PIV error due to the kickback noise is illustrated in Fig. 3. Here, the R_{TH} is the Thevenin's equivalent resistance offered by the preceding stage and $C_{\text{P,eff}}$ is the effective parasitic capacitance directly connected between outputs and inputs node. The peaks visible in input voltage due to the effect of kickback noise (a) at $\Delta V_{\text{IN}} =$ 5 mV (b) at $\Delta V_{\text{IN}} = 10$ mV are depicted in Fig. 4. Here, the effect of kickback noise is very negligible due to the use of shielding transistors MS1/MS2. Therefore, the peaks are very small in the proposed TTDCC. If kickback noise is very effective, the peaks will be large and PIV error will affect the comparison property of latch stage.

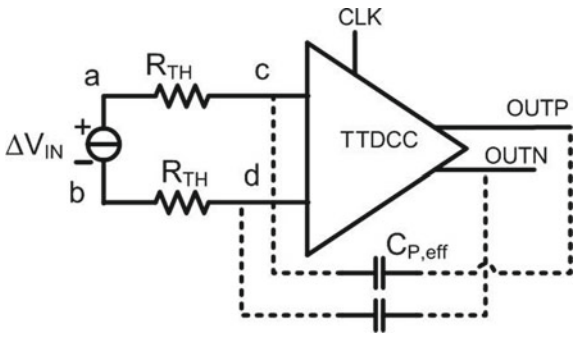

Fig. 3 The simulation setup to analysis PIV error due to the kickback noise

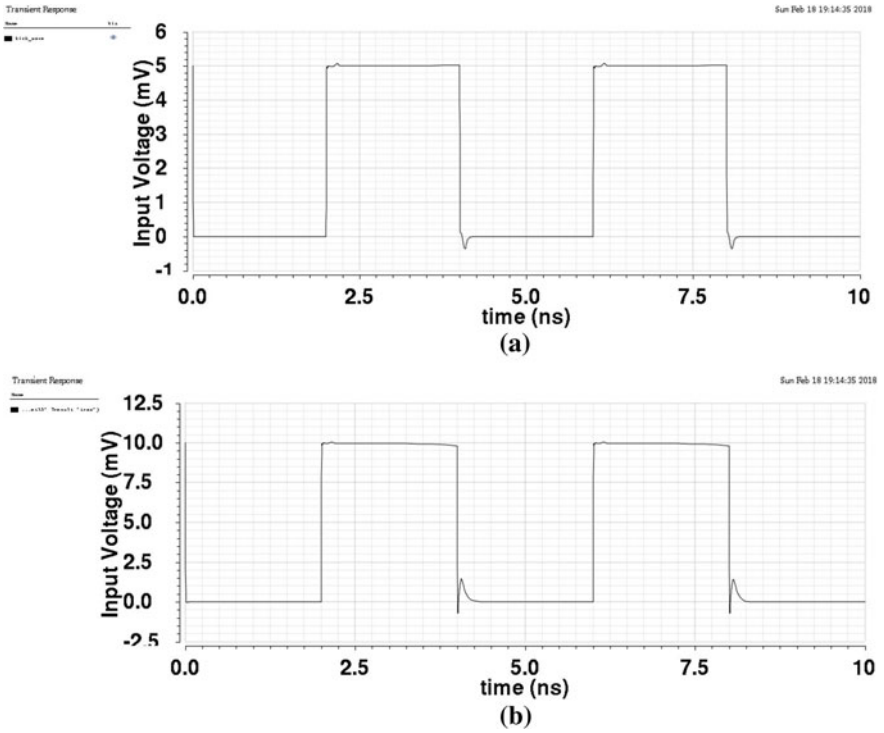

Fig. 4 The peaks visible in input voltage due to the effect of kickback noise **a** at $\Delta V_{IN} = 5$ mV, **b** at $\Delta V_{IN} = 10$ mV

3 Simulation Results and Discussions

The proposed TTDCC has been designed and simulated using the Cadence Virtuoso tool. The CMOS technology chosen for simulations is 90 nm. In the simulation, the transient part has been considered mainly as the delay and dynamic power dissipation are required to be analyzed. The power supply (V_{DD}) is varied from 0.7 to 1.2 V. Common Mode voltage (V_{CM}) is $V_{DD} - 0.1$ V. Differential input (ΔV_{IN}) applied to the TTDCC is 5 mV to 200 mV. The clock signal (CLK) has the frequency of 0.5 GHz and varying between 0 and V_{DD}. The transient behavior of the proposed TTDCC has already been discussed in Sect. 2. Now in this section the analysis of the Latch delay, total delay and power dissipation of the proposed TTDCC are discussed in detail.

The variation in latch delay and the total delay with respect to V_{DD} (a) latch stage delay (b) total delay are illustrated in Fig. 5. Here, the latch stage delay is 70 ps for $\Delta V_{IN} = 10$ mV and $V_{DD} = 0.8$ V. From Eq. (4), the latch stage delay is inversely proportional to the ΔV_{IN}. Hence, the latch stage delay will decrease with the increasing values of ΔV_{IN}. Same can be seen in Fig. 5a. The total delay is inversely

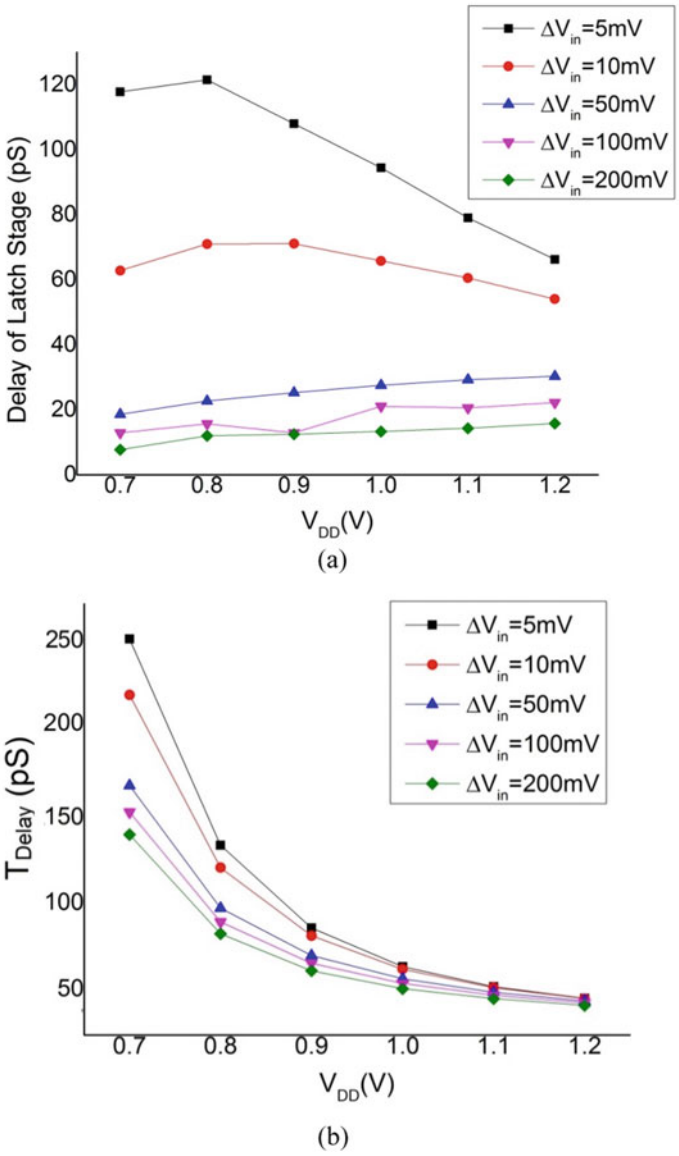

Fig. 5 The variation in latch delay and the total delay with respect to V_{DD} **a** latch stage delay, **b** total delay

proportional to the V_{DD}. Hence, the total delay will decrease with increasing V_{DD}. Same can be seen in Fig. 5b.

The variation in power dissipation and energy efficiency (a) power dissipation with respect to V_{DD} (b) energy efficiency with respect to ΔV_{IN} is depicted in Fig. 6. Here, the power dissipation follows the convention relation with V_{DD} (Power α $V_{DD}{}^2$). Now the energy efficiency is the power delay product (PDP) per conversion (i.e., PDP/2). The effect of ΔV_{IN} is negligible on the power dissipation but delay reduces. Hence, the energy efficiency will reduce with increasing ΔV_{IN}. Same behavior of the proposed TTDCC is visible in Fig. 6b. Here, it is also noticed that for higher V_{CM}, the energy efficiency decreases at constant V_{DD} (0.8 V).

The Monte-Carlo variation in offset voltage and the PIV error (a) offset voltage (b) PIV error due to effective kickback noise is shown in Fig. 7. Here, the 1-sigma error in offset voltage is 4.6134 mV for $\Delta V_{IN} = 10$ mV and $V_{DD} = 0.8$ V. The samples for Monte-Carlo analysis are 100 and the mean value of offset is 0.305 mV. The maximum random generated point on this graph is around 17 mV. The PIV error for the proposed TTDCC is varying with respect to the Thevenins' resistance R_{TH}. The larger value of R_{TH} and ΔV_{IN} increases the PIV error due to the kickback noise. Hence, if there is many preceding stage between the inputs and comparator block, the R_{TH} will be large and the kickback noise affects more and more. The similar illustration can be seen in Fig. 7b.

The corner analysis for the proposed TTDCC is shown in Table 1. Here, the corners are TT (typical values of NMOS and PMOS transistors), FF (Fast NMOS and Fast PMOS), FS (Fast NMOS and Slow PMOS), SF (Slow NMOS and Fast PMOS), and SS (Slow NMOS and Slow PMOS). The variation can be seen in the table.

The performance analysis of the proposed TTDCC compared to the conventional TTDCC simulated under similar simulation setup is shown in Table 2. Here, the simulation has be done in same simulation environments such as $V_{DD} = 1$ V, $\Delta V_{IN} = 10$ mV, $V_{CM} = 0.8$ V, input signals, CLK and sizing of the transistors etc. The conventional TTDCC [12] has delay of 208.9 pS and power dissipation of 47.4 μW. The hybrid TTDCC [14] has delay of 129.79 pS and power dissipation of 67.23 μW. The proposed TTDCC has the lowest delay and power dissipation, hence the lowest energy efficiency per conversion. However, the offset voltage of the proposed TTDCC is 4.62 mV which is comparable to the others.

The performance of the proposed TTDCC is compared in Table 3 to the recent works. Here, the proposed work TTDCC has been compared with the results of [12, 14, 19–25]. From the table, it is clear that the energy efficiency is lowest as compared to the other published works.

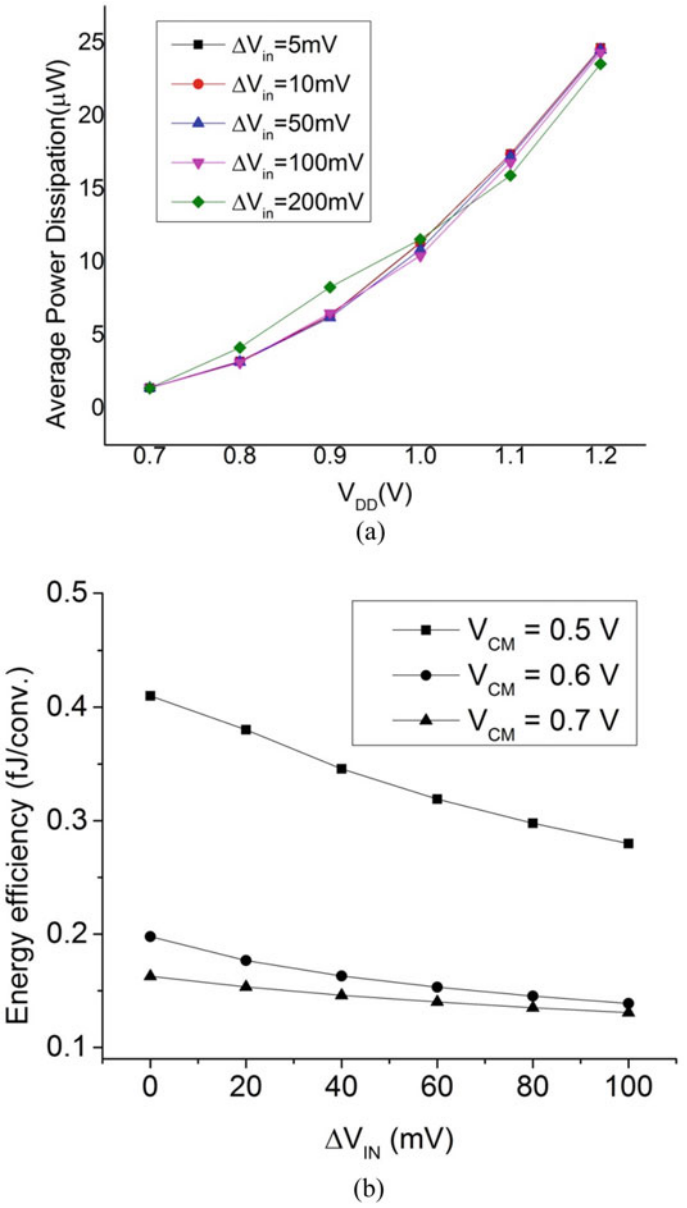

Fig. 6 The variation in power dissipation and energy efficiency: **a** power dissipation with respect to V_{DD}, **b** energy efficiency with respect to ΔV_{IN}

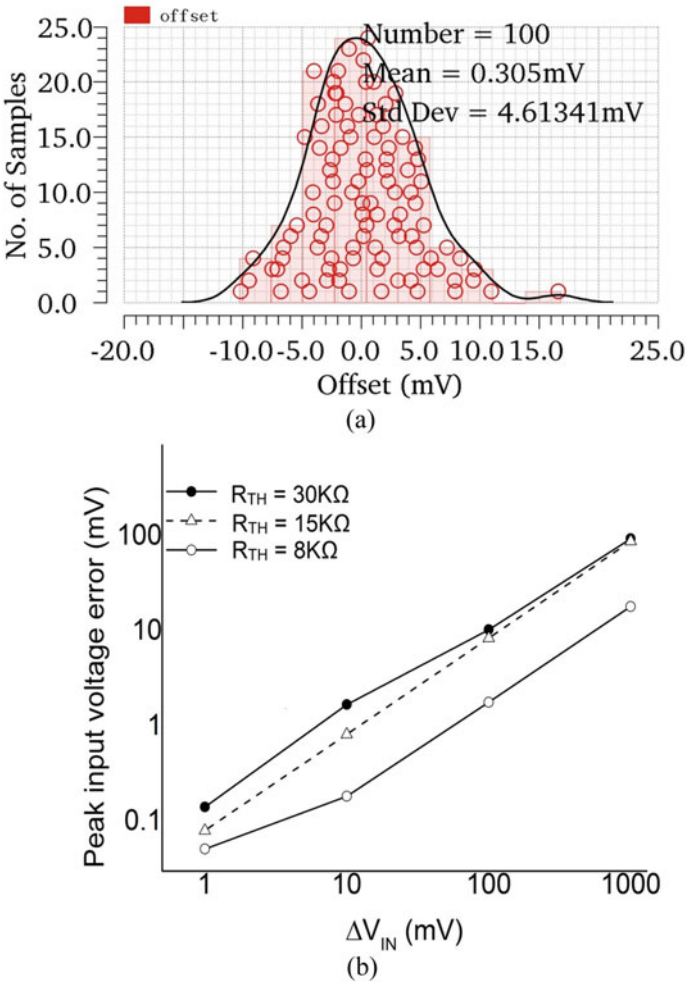

Fig. 7 The Monte-Carlo variation in offset voltage and the PIV error: **a** offset voltage, **b** PIV error due to effective kickback noise

4 Conclusion

The novel TTDCC has been proposed using BDL differential stage and GACOBA load latch stage. The design and simulation have been carried out in Cadence Virtuoso and Spectre at 90 nm CMOS technology. The results show that the proposed TTDCC has very small delay and power dissipation, 124.2 ps and 2.49 μW, respectively. Hence, it is very energy-efficient design as consume only 0.154 fJ per conversion. The offset voltage and PIV errors are also in control and can further be reduced but at the cost of delay and power dissipation. The proposed TTDCC is 63% faster and

Table 1 The corner analysis of the proposed TTDCC

Corners	Parameters				
	Total delay (ps)	Avg. PD (μW)	1-sigma Offset (mV)	PIV error (mV) @(ΔV_{IN} = 10 mV)	PDP (fJ)
TT	124.21	2.49	4.61	0.316	0.309
FF	94.85	2.74	3.97	0.412	0.259
FS	139.71	2.19	3.19	0.396	0.305
SF	114.31	2.32	4.92	0.382	0.265
SS	163.18	1.923	6.053	0.312	0.313

Table 2 The performance analysis of the proposed TTDCC compared to the conventional TTDCC simulated under similar simulation setup ($V_{DD} = 1$ V, $\Delta V_{IN} = 10$ mV)

Parameters	[12]	[14]	[17]	Proposed TTDCC
Maximum sampling rate (GHz)	5	8.3	7.7	18.2
Total delay time (pS)	208.9	129.79	135.41	76.53
Power dissipation (μW)	47.4	67.23	36.906	9.91
1-sigma offset voltage (mV)	3.49	5.93	3.14	4.61
Energy efficiency (fJ/Conv.)	4.909	4.35	2.49	0.38

92% energy efficient as compared to the conventional TTDCC [12]. The promising behavior of the proposed work can be further used to design subthreshold CMOS circuits such as VRCs, ADCs etc.

Table 3 Performance of the proposed TTDCC compared with the recent works

Parameters	[12]	[14]	[19]	[20]	[21]	[23]	[24]	[25]	Proposed TTDCC
Year	2007	2014	2016	2017	2017	2018	2018	2018	–
CMOS process (nm)	90	180	180	180	90	180	90	90	**90**
Supply voltage, V_{DD} (V)	1.2	1.2	1.8	0.8	1	1.8	0.8	1	**0.8**
V_{CM} (V)	1	1	1	0.7	0.7	1	0.6	0.7	**0.7**
ΔV_{IN} (mV)	5	5	100	5	5	1	5	20	**10**
Clock frequency (GHz)	3	0.5	4.54	0.05	1	0.5	1	1	**0.5**
Maximum sampling rate (GHz)	~ 14.3	2.4	5.2	*	*	1.5	4	3.7	**18.2**
Total delay time (ps)	~ 160	550	193	881	51.7	300	224	50.9	**124.2**
1-sigma offset voltage (mV)	13	7.8	2.5	*	*	2.4	*	7.7	**4.61**
Average power dissipation (μW)	~ 25	329	420	0.76	32.6	150	8.42	31.8	**2.49**
PDP (fJ)	40	181	81	0.67	1.69	4.5	1.9	1.62	**0.309**
Energy efficiency (fJ/Conv.)	40	240	40.5	0.33	0.5	2.2	0.95	0.8	**0.154**
PIV error (mV), @ ΔV_{IN} (mV)	*	43@ 100	*	4@ 5	*	*	*	*	**0.316**@ 10

*Not reported ~ calculated from given data

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Charge Plasma-Based Tunnel FET with Enhanced DC Performance Applicable for Ultra-low Power Applications

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1 Introduction

Ever since the innovation of the primary transistor by the trio of Shockley, Brattain and Bardeen in 1947 and then Kilby's development of Integrated Circuit (IC) in 1958 [1, 2], the effect of the advancement of electronic technology in our day by day exercises has been colossal to the point that these days it is unbelievable to survive without it. Advanced mobile phones, smart-vehicles, e-watches, smart LEDs, etc., are only a couple of models that facilitate our everyday life, for the most part because of the downscale development of the electronic transistor. The exponential development in the number of transistors on a single die, adhering to Moore's law [3–5], has been the significant motivation for the semiconductor business throughout these years.

Right up till the late 90s, the hypothesis of the scaling down of transistors by Dennard [6] was very much shadowed by the electronic industries, for example, the biasing supply voltage VDD and threshold voltage V_{TH} were scaled down directly with the decrease in channel dimensions. Thusly, with the diminishing of VDD, a quadratic lessening of the switching power utilization in the transistor and thus in the IC was seen during all these years. The effective reduction in the size of the transistors was for the most part accomplished because of the incredible material, SiO_2, and its electrical attributes. During the previous 15 years, a few adjustments

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in the transistor geometry were requisite so as to keep the innovation downscaling pattern [7, 8].

With scaled down thickness of the gate oxide, a surge of gate leakage (tunneling) because of current coursing via a thin gate insulator was introduced as the serious issue to be tackled at 45 nm nodes. The inclusion of gate dielectrics having huge dielectric constants fundamentally diminished the leakage due to gate, in this way permitting the abatement of the scaling of the technology nodes to 32 nm [9–12]. With further decrease in channel length, thermal diffusion of carriers and ensuing increment of current due to leakage necessitated changes in the orthodox CMOS structure.

To conquer the resulting increment in static power utilized in chips, diverse device design structures, for example, FinFETs and FDSOI were made and are right now under fabrication with nodes scaled down to 7 nm [13]. Transistors having multi-gate structure increment the gate control of the channel, thus, permitting the decrease of undesirable effects of short channel and ensuing decrease of dissipation of leakage power [14–16]. Notwithstanding the better control of the channel by the gate as opposed to the bulk CMOS, FDSOI permits the variation in the threshold voltage V_{TH} by altering the voltage polarity of the body [17].

During the forthcoming years, electronic devices are in prospect to be decreased to a couple of nanometers, and further, scaling down of the transistor would be beyond the bounds of possibility [18]. According to the present trend, the widths and lengths of MOSFETs are headed toward such a small scale at which they will be made out of few hundred atoms, unsolicited effects, for example, gate tunneling will forestall further enhancements in the device execution because of enormous leakage currents. So as to ward off the ensuing increment of static power consumption, development of chips with additional downscaling of technology and still keep the augmentation of density of transistors at a feasible affordable production, the business of semiconductor will inevitably push endeavors in the advancement of vertical device dimensions, hardware with numerous layers, and diverse electrical transport mechanisms [18, 19].

The process proportions of MOSFETs has kept on diminishing with the advancement of technology of microelectronics; however, the biasing voltage has not kept on reducing at the same pace [20]. Both the static power utilization and dynamic power utilization have exponential increment; hence, it becomes the primary test for MOSFETs. They utilize the thermionic emission as their primary mechanism, that can't efficaciously make the sub-limit swing under 60 mV/dec. The current present in the sub-threshold region is the principle cause of utilization of static power. Therefore, conventional MOSFETs cannot meet the necessities of better performance and reduced power utilization. To bypass the SS confinement of the orthodox transistors, devices with various carrier injection mechanisms without depending on (Boltzmann) appropriation of mobile charge carriers are the need of the hour [18, 20].

So as to confront the expansion of static power utilization pattern in chips for the upcoming technology nodes post CMOS-technology and also because of its non-thermal mechanism of carrier injection relying on Band-To-Band Tunneling (BTBT)

phenomenon, TFET, tunnel field-effect transistor is introduced as the finest promising candidate [19, 21].

With an alternate mechanism of carrier injection in contrast with the traditional thermal devices, TFETs have the ability to accomplish an inverse sub-limit slope (SS), at room temperature, with a value sub-60 mV/dec. With this unique trademark, TFETs can possibly accomplish a low working voltage, keeping up a huge current gain. The future assembly of TFETs in chips meant for low power is emphatically subject to the development of fabricating techniques as TFETs fabricated with the materials belonging to the groups III and V conquer the electrical functioning of silicon-based TFETs [2]. In light of the tunnel diodes controlled by the gate, the elementary planar TFETs possess petite ON-state current, the indirect band gap, perplexing heavy doping methods, and higher forbidden band width of the silicon material, which can restrict the large-scale use of silicon-based planar TFETs [5]. Researchers have planned some novel TFET devices with unique structures for taking care of this issue, for example, the hetero-intersection TFET, dopingless TFET, etc. [6].

The DLTFET can tackle the intensely doped technology issue. The entirety of the regions of DLTFET utilizes the intrinsic materials, and the regions comprising of source and drain are acknowledged by choosing the appropriate metal work function. In spite of the fact that the newly developed structures can take care of the issue to a limited degree, the device performance despite everything has opportunity to get better. The utilization of size scaling for TFETs is constrained by lesser on-current, higher miller capacitance and intensely doped sharp junctions [7, 8, 22].

2 Device Dimensions and Model

Figure 1 shows the schematic view of CP-TFET. The device dimensions of CP-TFET and DG-TFET are mentioned in Table 1. The models like Shockley–Read–Hall recombination model, Auger recombination model, band gap narrowing model, non-local BTBT model, field-dependent mobility model, and phonon-assisted tunneling model have been utilized throughout the numerical calculation. The spatial variation of energy bands has been considered by the non-local models.

3 Results and Discussions

In this section, we have investigated the electrical attributes of a dopingless charge plasma-based TFET (CP) in comparison with the orthodox dual-gate TFET (DG). Figure 2 portrays the graphs of energy band variations for TFET in OFF and ON state, which reflects shallower band bending for CP-TFET, practically like that of

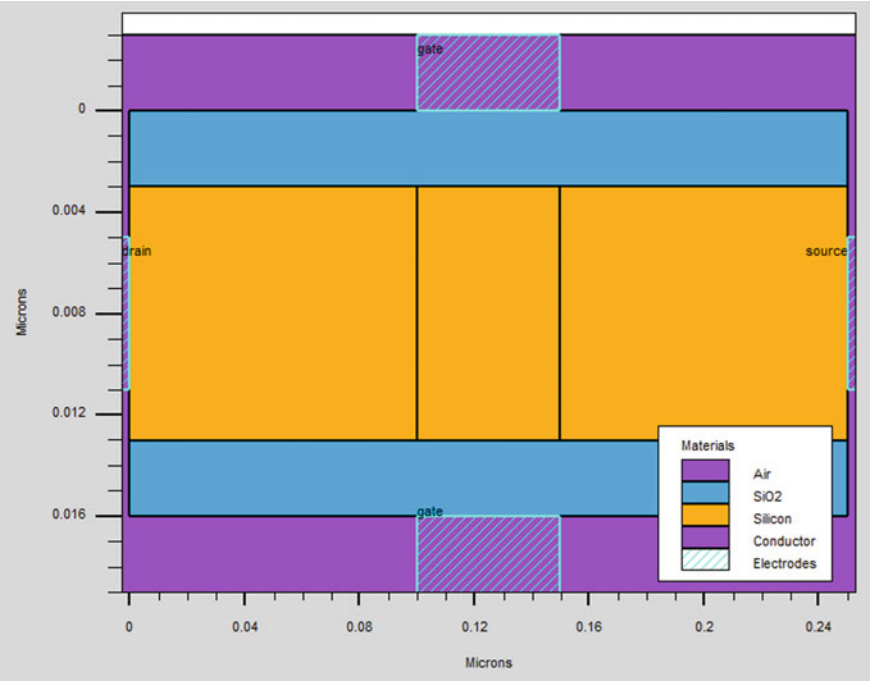

Fig. 1 Schematic view of CP-TFET

Table 1 Device dimensions of CP-TFET and DG-TFET

Parameter	CP-TFET	DG-TFET
Channel length	50 nm	50 nm
Source length	100 nm	100 nm
Drain length	100 nm	100 nm
Gate work function	4.5 eV	4.5 eV
Source electrode	5.93 eV	–
Drain electrode	3.9 eV	–
Source doping	$10^{15}/cm^3$	$10^{20}/cm^3$
Drain doping	$10^{15}/cm^3$	$5 \times 10^{18}/cm^3$
Channel doping	$10^{15}/cm^3$	$10^{17}/cm^3$

traditional DG-TFET. Notwithstanding the introduction of charge plasma, the characteristics of TFET are not unfavorably influenced in the OFF state. Junction abruptness plays the crucial role in getting a superior device characteristics for the case of doping less TFET. In Fig. 2b, it is observed that the suggested structure with charge plasma is having a precipitous band bending in the on state that allows a maximum extent of electrons to pass through the junction with no trouble and hence furnishing more suitable drain current characteristics.

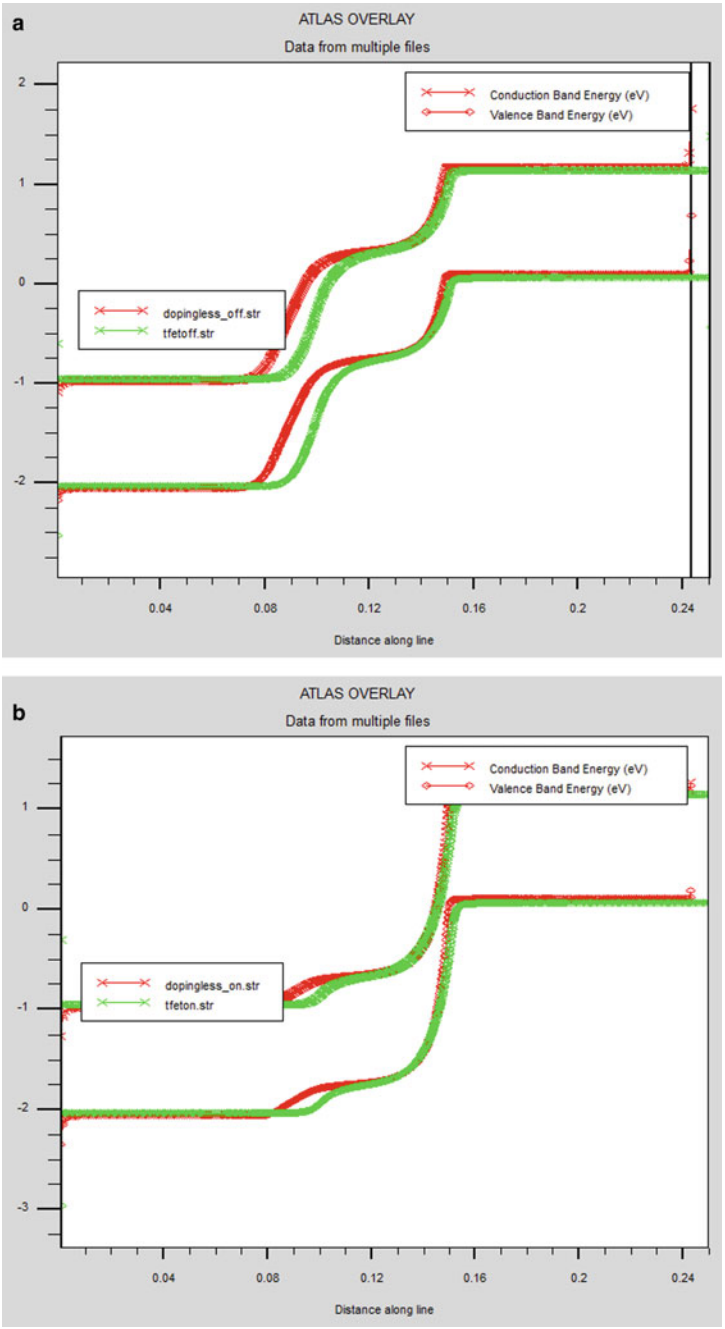

Fig. 2 Energy band diagram: **a** OFF state. **b** ON state

It is very well observed from Fig. 3, that a high potential gradient is present at the tunneling junction between the channel and source. Additionally, the tunneling band located at this junction is bent to some extent. Along these lines, having a sharp band bending aides in improving the tunneling rate of electrons and in the long run providing larger drain current.

Figure 4 shows electric field variation, which illustrates the higher electric field for CP-TFET as compared to conventional DG-TFET at interface of source and channel. The high electric field can adequately diminish the width of the tunneling barrier, and the energy band turns out to be increasingly bended which can advance the band tunneling phenomenon of electrons, thus enhancing the drain current.

Figure 5 shows the variation of electron and hole concentration along the channel in OFF state and ON state, respectively. The charge plasma method induces the electrons and holes concentration on source and drain regions of CP-TFET similar to doping done in DG-TFET. The concentration of electrons in ON state has increased in contrast to OFF state, and this enhances the drive current of CP-TFET analogous to OFF-state current. The transfer characteristics of CP-TFET and conventional DG-TFET at $V_{DS} = 1$ V are shown in Fig. 6. The OFF current obtained for CP-TFET is 1.77×10^{-18} A/μm which is less in contrast to 1.76×10^{-17} A/μm of DG-TFET. Sub-threshold swing obtained for CP-TFET is 29.1 mV/decade, whereas for DG-TFET is 35.1 mV/decade. By observing the graph, it is understood that the suggested structure exhibit enhanced drain current. This escalation in drain current is because of the introduction of charge plasma which enhances the carrier velocity at the junction of tunneling.

The augmented performance of DG-TFET contrasted with the dopingless CP-TFET can be comprehended from the electric field variation for the ON-state, portrayed in Fig. 4. We see that, for the dopingless CP-TFET because of the sheer abruptness in the energy profile of the ON-state (as appeared in Fig. 2b, the electric field at the junction between channel and source of the dopingless CP-TFET is higher contrasted with the DG-TFET. This resulting high electric field, along with a decreased tunneling width, prompts a greater band-to-band generation rate, and thus, superior drain current than its conventional counterpart.

4 Conclusion

In this work, the technique of charge plasma is utilized in order to curtail the random dopant fluctuations that occurs because of doping. The charge plasma based TFET is proposed that provides reduced OFF state current and enhanced drive current in compare to DG-TFET. Charge plasma minimizes the issues during fabrication process. It has been observed that CP-TFET has steep band bending in contrast to DG-TFET, which enhances the tunneling rate of charge carriers that leads to rise in electric field and drive current of the device. The CP-TFET has superior DC characteristics in contrast to DG-TFET which is best suited for applications of ICs of ultra-low power.

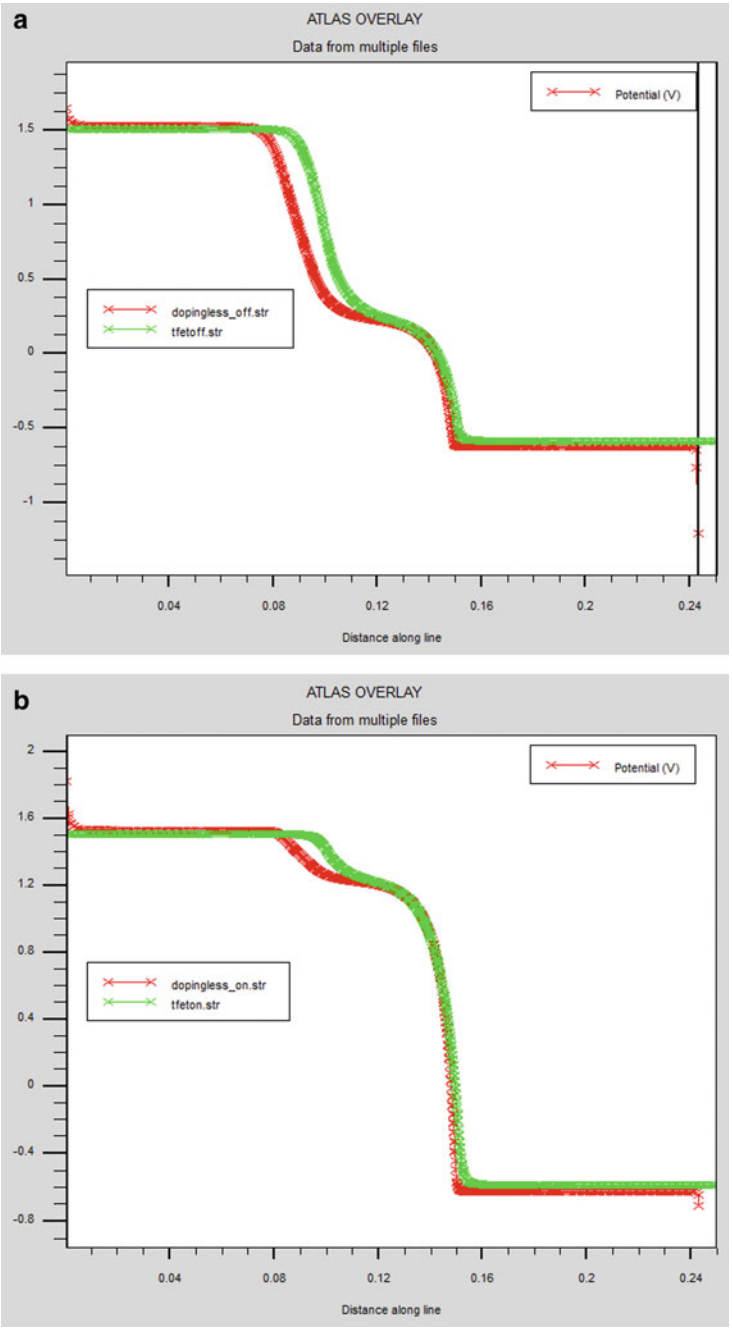

Fig. 3 Surface potential along the channel: **a** OFF state. **b** ON state

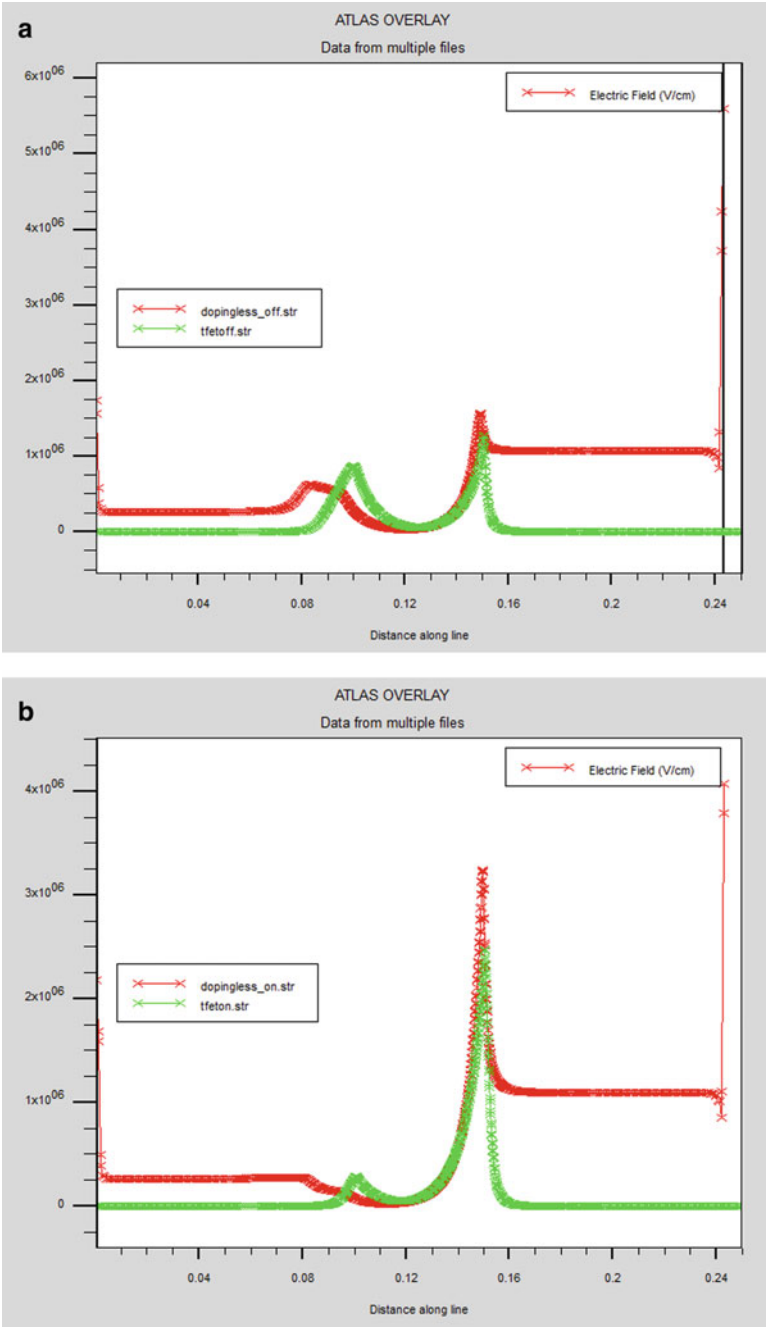

Fig. 4 Electric field along the channel: **a** OFF state. **b** ON state

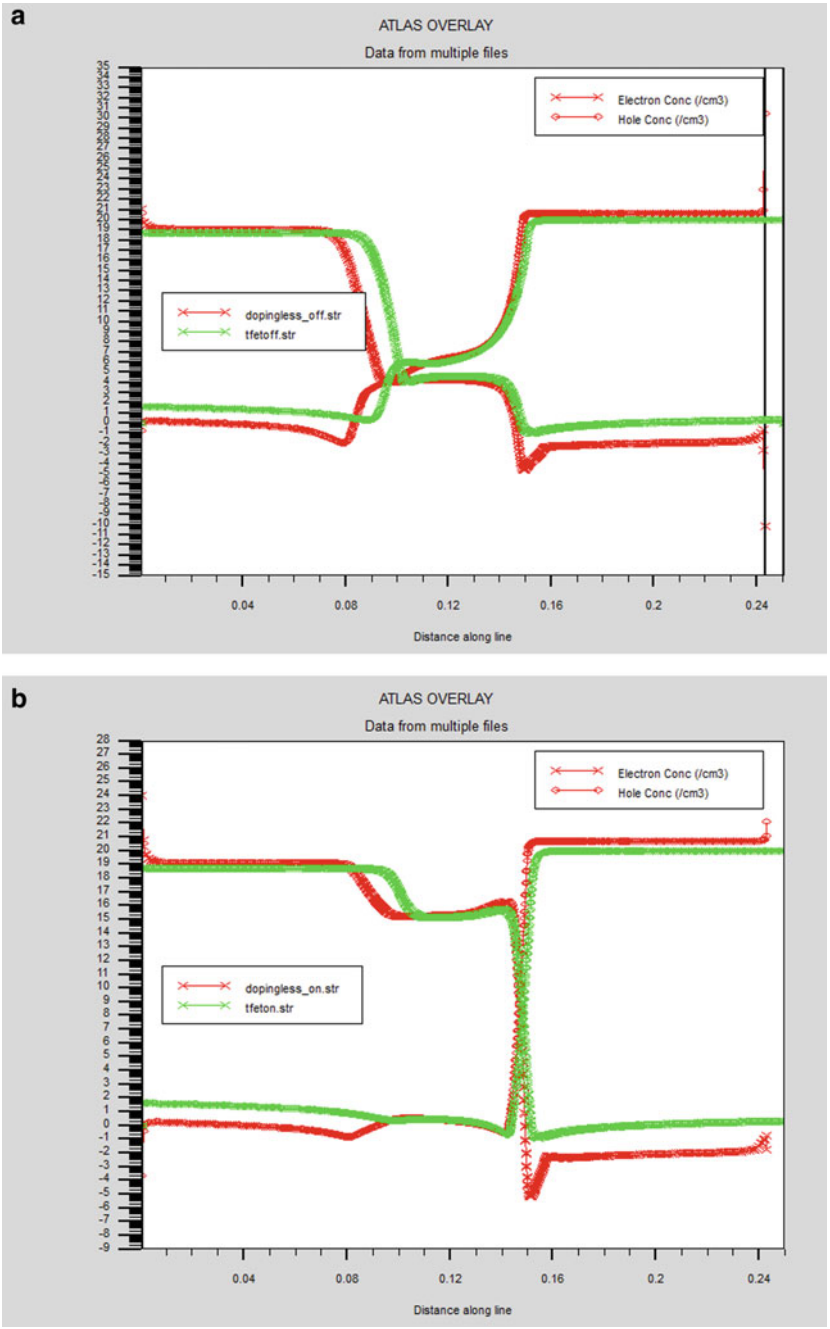

Fig. 5 Electron and hole concentration along the channel: **a** OFF state. **b** ON state

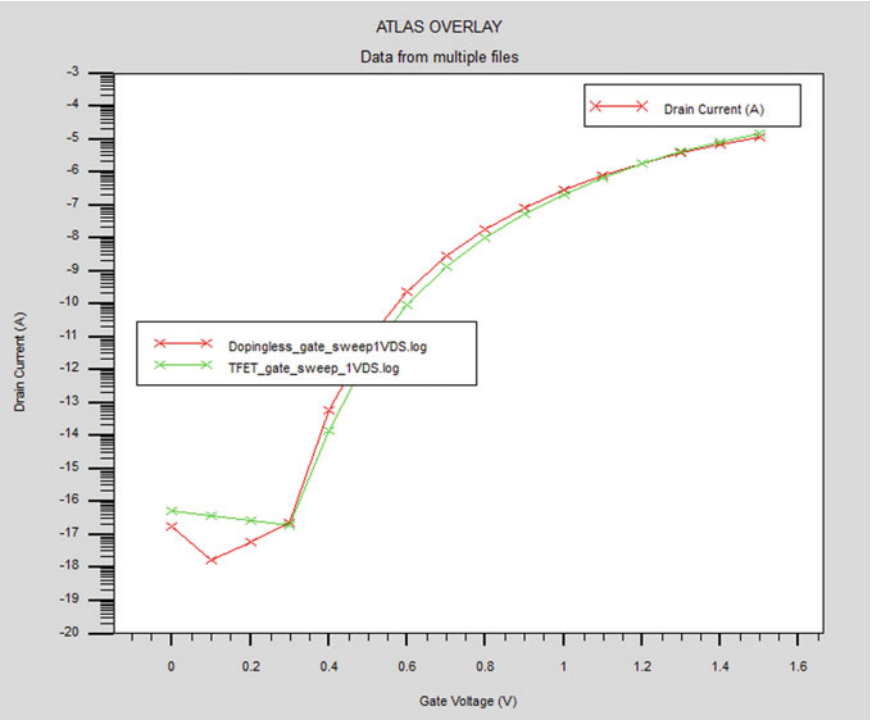

Fig. 6 Transfer characteristics of CP-TFET and DG-TFET

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Data Collection Website with Brain Tumor and Pneumonia Detection

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1 Introduction

Medical science integrated with engineering has been proved to be a great success in reducing mortality rate through accurate and early disease detection. MIC (medical image computing) is an inter-disciplinary field of medicine, information engineering, computer engineering and electrical engineering which develops mathematical models for medical image processing. ANN application embedded with image processing techniques brings automation in CAD system which helps doctors and radiologists in faster and accurate diagnosis from medical images. ANN goes through a number of steps for automatic and faster analysis which mainly require training and testing of ANN model. Thousands of patients data are required to test and train for a successful model. The drawback of this technique is that online availability of data is not sufficient enough to fulfill the requirement, and also these data size can vary from few MB to few GB making it difficult to store online altogether.

There is always a requirement of a tool designated specifically for data collection where doctors can easily submit patient-related information and also researchers who need these data for training models can easily download it. This paper provides solution to medical data shortage problem by proposing a website model designed for medical data collection. In this way, it will also help doctors by storing hospitals and patients data for future references of case study, thus reducing paper workload. Besides data collection, we also integrated brain tumor and pneumonia detection models into the website, making our website useful not only for medical data collection but also helping doctors in decision-making process. These diseases if not detected at early stage then may lead to patient's death. Prompt and accurate diagnosis and treatment plan can only lead to improved quality of life in patients.

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Brain tumor terminology is given to the abnormal growth characteristics of brain tissues which can be classified as malignant (cancerous) and/or benign (non-cancerous) [1]. Early detection of the brain tumor is possible with the advancement of MIC; one of such most practical and important model used is deep learning neural network (DNN) which is a subset of ANN [2]. Convolutional neural network (CNN) algorithms of deep learning have been used in our work which shows state-of-art performance in medical image analysis and disease detection problems through number of steps like feature extraction from ROI (region of interest), feature selection followed by disease classification. Training a CNN successfully may require large number of input data which are not available easily, thus limiting the practical applications of deep learning models in medical field. We have proposed various transfer learning techniques to train deep learning models whose idea is to take a model that has already been used for repurposing toward a new task.

Pneumonia is a bacterial, viral or fungal disease which causes infection in lungs. These germs are contagious hence communicate from person to person. Inflammation is produced in the lung's air sacs which may be filled with pus or fluid due to this infection, leading to difficulty in breathing. Bacterial and viral pneumonia are communicated to others during inhalation of nearby airborne droplets from infected cough, sneeze or exposure to contaminated surfaces. Fungal pneumonia generally is contracted from environment and doesn't spread from person to person. Deep neural network structure have been conventionally designed and tested continuously through trial-and-error method for pneumonia detection, which requires resources, enormous time and know-how. To overcome, these problems data augmentation is coupled with transfer learning. The proposed methodology uses CNN algorithm for extracting relevant features from images by convolving it with neurons set [3]. Efficacy of the method was demonstrated and compared with existing state-of-the-art pneumonia classification networks [4].

For brain tumor detection, we obtained a dataset of 253 brain MRI images and for pneumonia detection a dataset of 5500 chest X-ray images. The image dataset is pre-processed and resized using bi-cubic interpolation. The size of the dataset was then increased virtually using data augmentation. The pre-processed images are then fed into various models for feature extraction, selection and classification. For brain tumor detection, we trained three models, namely Inception V3, Resnet50 and VGG16. Out of these three models, VGG16 model performed the best against our standard. It achieved training accuracy of 97.68%, validation accuracy of 92.12% and testing accuracy of 89.72% and hence was chosen as the final model for brain tumor detection. For pneumonia detection, we trained three models, namely Inception V3, model trained from Scratch and VGG16. Out of these three models, VGG16 model performed the best against our standard. It achieved training accuracy of 96.90%, validation accuracy of 93.02% and testing accuracy of 84.8% and hence was chosen as the final model for pneumonia detection.

2 Background

2.1 Convolutional Neural Network

In neural networks, CNN is usually preferred for ROI recognition and image classifications through objects detection, recognition, extraction, etc. CNN model simply takes an image as input, performs image processing and then classifies it under certain categories. A computer understands an image as array of pixels, height x width x dimension, which depends on its resolution; e.g., an image of $6 \times 6 \times 3$ array of RGB matrix (3 refers to RGB values) and an image of $4 \times 4 \times 1$ array of grayscale images matrix. Input images pass through a series of convolution layers having pooling layers, filters (kernels), fully connected layers (FC) and softmax function for classification of object with probabilistic values between 0 and 1.

2.2 Transfer Learning

As the name suggests, transfer learning process train a model for some specific problem and transfer this knowledge to other related problems. In deep learning, this technique trains a neural network model for a problem similar to the problem that is being solved. One or more layers from the trained model are then used in a new model trained on the problem of interest [5]. The weights in re-used layers may be used as the starting point for the training process and adapted in response to the new problem. This usage treats transfer learning as a type of weight initialization scheme. This may be useful when the first related problem has a lot more labeled data than the problem of interest and the similarity in the structure of the problem may be useful in both contexts. Transfer learning has the benefit of decreasing the training time for a neural network model and can result in lower generalization error.

3 Proposed Work

The complete work performed can be broken down into three major modules: website development, brain tumor and pneumonia detection. The website model is for medical data collection to address the problems of small medical datasets. The brain tumor and pneumonia detection models are trained to assist the doctors in decision-making process. We trained several models for each task. After training all the models, two models, one from each set, were chosen as the final models for integrating into the website for prediction purpose.

3.1 Website Development

The main goal of MIC is to extract clinically relevant information from medical images. There is always a requirement of storage where large number of medical images and findings must be saved online and can be accessed whenever required. To solve this problem, we proposed a website model for data collection in Fig. 1 with following notable features keeping security factor in mind too:

- The website consists of many pages interlinked through hypertext links.
- Webpages are designed to provide links to access large number of datasets.
- Only registered users can avail the services offered by the website.
- Access rights are divided between doctors and researchers only through proper login id after admin verification.
- Different categories of users are given different access rights.
- Doctors are provided with reading, writing and editing option so they can download as well as upload datasets.
- Researchers are allowed with reading option only so they can only download datasets provided by the admin.
- Guest page and login are provided to visit the webpage.

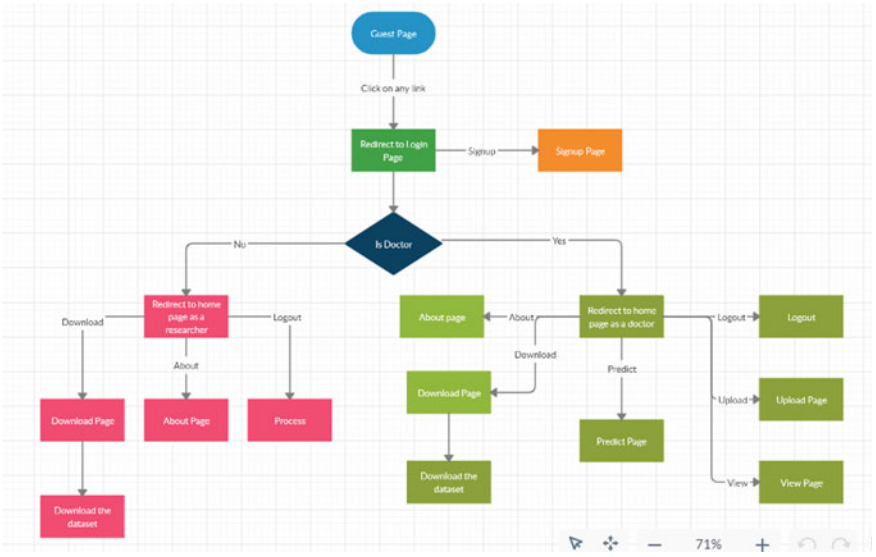

Fig. 1 Proposed website model

3.2 Clinical Dataset

For brain tumor detection, we obtained 253 MRI images from 253 different patients. Further processing on images required splitting it into training set with 155 images followed by validation set with 30 images and testing set with 30 images [6, 7]. For pneumonia detection, 5500 X-ray images dataset were obtained whose processing also followed splitting into training set with 4000 images followed by validation set with 500 images and the testing set with 500 images [8]. Although the dataset for brain tumor detection was small but applying data augmentation technique to generate more data, we have obtained satisfying results.

3.3 Image Pre-processing

After obtaining patients' dataset, pre-processing is performed over images to avoid inconsistency and maintaining high accuracy. It follows region of interest (ROI) extraction, cropping, resizing of the image and shifting the pixel range. Due to very high variation in pixel ratios, the images were cropped to extract the ROI in the first place. Image pre-processing followed the following algorithm:

- Get the original images one by one from the dataset.
- Find the biggest possible contour on the image using 'findAllContours' tool of the OpenCV library.
- 'MAX' function in the OpenCV library gives the maximum area contour in the image.
- Rectangular crop the image after locating the extreme points on this contour.
- Resize the image to the dimension (224,224,3) using bi-cubic interpolation method.
- Apply the model-specific pre-processing function on the images in the datasets to shift the range of the pixels.

3.4 Feature Extraction and Classification

For extracting the features of both datasets, we have used several pre-trained ConvNets as an initializing step for our models. The ConvNets include VGG16, Resnet50, InceptionV3 and models from scratch. For training the models, we use machine learning (ML) and transfer learning techniques. In traditional ML technique, we simply train the model from dataset that we acquire. This is also known as isolated learning. However, in transfer learning technique we transfer the knowledge of a pre-trained model to our model that we intended to train for our task of interest. For brain tumor detection, since the size of the dataset was small, we only used the transfer learning technique to train our models and, for pneumonia detection since

the size of the dataset was sufficient enough, we used ML and transfer learning both to train our models. We are discussing here transfer of knowledge in two ways:

- *ConvNets feature extractor*
  Apply pre-trained ConvNet on the ImageNet dataset but remove the fully connected last layer (i.e., the MLP layer in Fig. 1). Rest of the ConvNet is used as fixed feature extractor for other dataset. The last fully connected layers or the dense layers of the models served the purpose of a classifier. The benefit of this approach would be that, even if you have less data, this would not over-fit as you would only train the MLP layer which you added to the convolutional base (i.e., retrain the classifier only and freeze the convolutional base).
- *Finetuning of the ConvNets*
  In finetuning, we initialize the network using pre-trained weights and then train the entire network like training the model from scratch.

After both the models were trained, we integrated these models into the predicted page of the website. This enables the doctors to make decisions related to pneumonia and brain tumor diagnosis quickly and accurately saving many lives.

4 Results

Medical images obtained were categorized into two classes. Class 0 denotes that the patient is healthy and Class 1 denotes that the patient is diseased. Accuracy has been calculated as a performance parameter of the model. Firstly, we developed the website for data collection and models for brain tumor and pneumonia detection. Then, we integrated the models into the website. The results for brain tumor and pneumonia detection models are compiled below:

4.1 Brain Tumor Detection

We have trained three models for brain tumor detection, namely Inception V3, Resnet50 and VGG16. The results for each model are compiled below:

	Training accuracy (%)	Validation accuracy (%)	Testing accuracy (%)
Inception V3	89.93	63.86	60.56
Resnet50	94.32	81.94	77.48
VGG 16	97.68	92.12	89.72

Clearly, VGG16 model outperformed other models and hence was chosen as the final model for brain tumor detection.

4.2 Pneumonia Detection

We have trained three models for pneumonia detection, namely Inception V3, model from scratch and VGG16. Out of these models, the one which outperformed all the other models was chosen as the final model for pneumonia detection. The results for each model are compiled below:

	Training accuracy (%)	Validation accuracy (%)	Testing accuracy (%)
Inception V3	85.46	77.62	72.12
Model from scratch	87.88	78.32	70.42
VGG16	96.90	93.02	84.80

Clearly, VGG16 model outperformed other models and hence was chosen as the final model for brain tumor detection.

4.3 Inference

Once these models were finalized, they were then integrated into the website to help doctors take decisions. Further, doctors can upload MRI and X-ray images of the brain and chest, respectively, and click the predict button on-page to get the prediction from these models.

5 Conclusion

To solve the problem of small datasets in medical field we designed a data collection website where doctors can maintain the records of their patient and researchers can download the dataset made from the images uploaded by the doctors. The procedure of dataset formation respects the confidentiality and privacy of human subject involved in the process. Moreover, to help the doctors take quicker decisions for pneumonia and brain tumor, we integrated the machine learning models in the website. Access rights for the users in the website are carefully designed as well as taken care of. Doctors can upload images of different organs of various modalities like ultrasound, X-Ray, CT-Scan, MRI, etc., along with the data related to the image. They can also view the images that they uploaded along with its associated data. Researchers are only allowed to download datasets, not upload them. In this way, integrity and credibility of the data have been maintained.

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Preview Control for Discrete Time Systems

Akhilesh Kumar Ravat, Amit Dhawan, and Manish Tiwari

1 Introduction

Over the past several decades, the problem of preview control theory has been attracting important interest in the field of process control, autonomous vehicle guidance, signal processing, manufacturing control, etc. [1–6]. In preview control, the exogenous disturbance or reference signal is prior defined [7–13]. With the help of available future reference or given disturbance signal, the tracking quality of the system is improved. The type of control problem that make use of the future information on reference and/or disturbance signal is called preview control [2]. In the designing of control systems, the benefit of future information is termed as preview control or look ahead. In the presence of exogenous signals, it is desired that the outcome should follow the reference signal [1]. If the given future value is known, the system's output should track the reference signal. For reference tracking, the preview problem is solved in uses like robot motion, tracking of missile target, etc. In the presence of disturbance, the disturbance rejection problem is to support the output of the preview system to desired level. The quadratic performance index is used to optimize the tracking error and control input [3].

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Preview controls have following benefits [12]:

- Better progress in tracking performance.
- Disturbance rejection improvement.
- Improve in low frequency tracking.

1.1 Examples Related to Preview Control

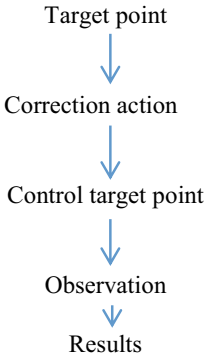
There are two examples to explain the key concept of preview control. In the first example, we think about to driving of a car move along a road. It is impossible for the driver to know complete information on the status of the road from the starting point to the destination. Now if the driver see ahead for a few distance then suddenly he apply break for turning or breaker, thus it is causes of accident possibly. To remove this problems, driver tries to look ahead with the help of future information of signal as far as possible.

In the second example, we consider outline of a continuous annealing procedure in which rightly thickness of steel strips is generated by passing them through heating. Variation in temperature and entry thickness may work as disturbances by which the performance of the system is poor. For the measurement of thickness and strip temperature can be previewed by X-ray gauge and radiation pyrometer. Thus, the system performance can be enhanced by using message [1].

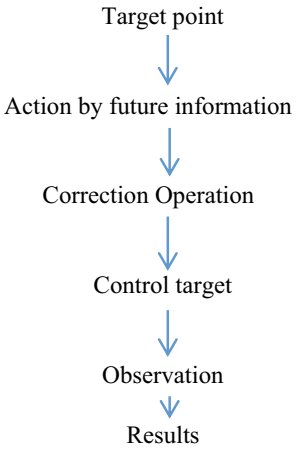
1.2 Preview Control

There is comparison between conventional servo system and preview servo system.

Conventional servo system:



Preview-featured servo system:



2 Problem Formulation

Consider the following discrete-time system:

$$\begin{aligned} x(n+1) &= \boldsymbol{A}\,\boldsymbol{x}(n) + \boldsymbol{B}\,\boldsymbol{u}(n) + \boldsymbol{w}(n) \\ y(n) &= \boldsymbol{C}\,\boldsymbol{x}(n) \end{aligned} \tag{1}$$

$x(n) \in \mathbf{R}^p$ is defined as the state vector, $u(n) \in \mathbf{R}^m$ is known as control input vector, $y(n) \in \mathbf{R}^q$ is declared as controlled output vector. $w(n) \in \mathbf{R}^{ld}$ is defined as disturbance vector, $w(n) \in ld_2$. The matrix $\boldsymbol{A}$, $\boldsymbol{B}$ and $\boldsymbol{C}$, respectively, are available real constant matrices with exact dimensions.

However, according to the key point of preview horizon control, it is important for preview and control the current information of the system is to be needed. The input cannot be influenced the output at the similar time.

3 Derivation of Augmented System

An augmented system is derived to convert the tracking issue into regulator problem. Taking a difference on both side of Eq. (1), we find that

$$x(n+1) - x(n) = A(x(n) - x(n-1)) + B(u(n) - u(n-1))$$

The subtraction of the state variable is defined as:

$$\Delta x(n+1) = x(n+1) - x(n);\ \ \Delta x(n) = x(n) - x(n-1) \tag{2}$$

The subtraction of control input is defined as:

$$\Delta u(n) = u(n) - u(n-1) \tag{3}$$

The state-space equation can be clarified as:

$$\Delta x(n+1) = A\Delta x(n) + B\Delta u(n) \tag{4}$$

To connect state $\Delta x(n)$ with output $y(n)$, a new formation of state variable vector is to be selected as

$$x(n) = [\Delta x(n)^T y(n)]^T$$

And

$$\begin{aligned} y(n+1) - y(n) &= C(x(n+1) - x(n)) = C\Delta x(n+1) \\ &= CA\Delta x(n) + CB\Delta u(n) \end{aligned} \tag{5}$$

Putting together Eqs. (4) with (5) conduct to the state-space model as given below:

$$\begin{bmatrix} \Delta x(n+1) \\ y(n+1) \end{bmatrix} = \begin{bmatrix} A & 0^T \\ CA & 1 \end{bmatrix} \begin{bmatrix} \Delta x(n) \\ y(n) \end{bmatrix} + \begin{bmatrix} B \\ CB \end{bmatrix} \Delta u(n)$$

$$y(n) = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} \Delta x(n) \\ y(n) \end{bmatrix} \tag{6}$$

4 Preview Controller

The design of preview control system is to be computed the preview plant outcome with future signal as the convertible variables. This preview is explained with an optimization.

4.1 Preview of State and Output Variables

Let the sampling instant n_i, $n_i > 0$, the state variable vector is presented through measurement, and the state describes the current plant information. The future control trajectory is represented by

$$\Delta u(n_i),\ \Delta u(n_i + 1), \ldots, \Delta u(n_i + N_{co} - 1)$$

Here, N_{co} is defined as control horizon length, with the help of state variable, the future state variable is previewed for N_p. Here, N_p is known as preview horizon length.

Here, future state variables are represented as following:

$$x(n_i + 1|n_i),\ x(n_i + 2|n_i), \ldots x(n_i + N_p|n_i),$$

The length of control horizon is selected in such a way that the preview horizon length is to be greater or equal.

On the viewpoint of state–space model, the calculation of future state variables is to be taken as sequences by the setting of future control parameters:

$$\begin{aligned}
x(n_i + 1|n_i) &= A_a x(n_i) + B_a \Delta u(n_i) \\
x(n_i + 2|n_i) &= A_a x(n_i + 1|n_i) + B_a \Delta u(n_i + 1) \\
x(n_i + 3|n_i) &= A_a^2 x(n_i) + A_a B_a \Delta u(n_i) + B_a \Delta u(n_i + 1) \\
&\vdots \\
x(n_i + N_p|n_i) &= A_a^{N_p} x(n_i) + A_a^{N_p - 1} B_a \Delta u(n_i) + \\
&\qquad A_a^{N_p - 2} B_a \Delta u(n_i + 1) + \cdots \\
&\qquad + A_a^{N_p - N_{co}} B_a \Delta u(n_i + N_{co} - 1)
\end{aligned}$$

By using preview state variables, the previewed outcome variables are given below:

$$\begin{aligned}
y(n_i + 1|n_i) &= C_a A_a x(n_i) + C_a B_a \Delta u(n_i) \\
y(n_i + 2|n_i) &= C_a A_a^2 x(n_i) + C_a A_a B_a \Delta u(n_i) + C_a B_a \Delta u(n_i + 1) \\
y(n_i + 3|n_i) &= C_a A_a^3 x(n_i) + C_a A_a^2 B_a \Delta u(n_i) \\
&\qquad + C_a A_a B_a \Delta u(n_i + 1) + C_a B_a \Delta u(n_i + 2) \\
&\vdots
\end{aligned} \tag{7}$$

$$\begin{aligned}
y(n_i + N_p|n_i) &= C_a A_a^{N_p} x(n_i) + C_a A_a^{N_p - 1} B_a \Delta u(n_i) + \\
&\qquad C_a A_a^{N_p - 2} B_a \Delta u(n_i + 1) + \cdots \\
&\qquad + C_a A_a^{N_p - N_{co}} B_a \Delta u(n_i + N_{co} - 1)
\end{aligned} \tag{8}$$

The previewed variable are designed in form of current state, and future control is given as $\Delta u(n_i + j)$, where $j = 0, 1, 2, \ldots, N_{co} - 1$.

The output vectors

$$\begin{aligned} Y &= [y(n_i+1|n_i) \quad y(n_i+2|n_i) \quad y(n_i+3|n_i) \quad \ldots \quad y(n_i+N_p|n_i)]^T \\ \Delta U &= [\Delta u(n_i) \quad \Delta u(n_i+1) \quad \Delta u(n_i+3) \quad \ldots \quad \Delta u(n_i+N_{co}-1)]^T \end{aligned} \tag{9}$$

From the above equation for SISO case, the dimension of *Y is Np* and ΔU have N_{co} dimension.

From Eqs. (7), (8), (9), we get

$$Y = Fx(n_i) + \alpha \Delta U \tag{10}$$

where

$$F = \begin{bmatrix} C_a A_a \\ C_a A_a^2 \\ C_a A_a^3 \\ \vdots \\ C_a A_a^{N_p} \end{bmatrix}; \; \alpha = \begin{bmatrix} C_a B_a & 0 & 0 & \cdots & 0 \\ C_a A_a B_a & C_a B_a & 0 & \cdots & 0 \\ C_a A_a^2 B_a & C_a A_a B_a & C_a B_a & \cdots & 0 \\ \vdots & & & & \\ C_a A_a^{Np-1} B_a & C_a A_a^{N_{p-2}} B_a & C_a A_a^{N_{p-}-3} B_a & \cdots & C_a A_a^{N_p - N_{co}} B_a \end{bmatrix}$$

4.2 Optimization

The aim of the preview control system is to obtain the preview outcome as near as available to the reference point signal; we consider that there is no change in the reference signal by an optimization. The aim is to be achieving the 'best' control point vector ΔU by which an error function can be diminished.

Consider that the reference information is given as:

$$R^T = [1 \quad 1 \quad 1 \ldots 1]\, r(n_i) = R' r(n_i)$$

Here, we consider the cost function *J*, and it contains the control aim as:

$$J = (R - Y)^T (R - Y) + \Delta U R' \Delta U$$

where $R' = r_w I_{N_{co} * N_{co}}, \quad (r_w \geq 0)$.

Here, for the desired closed-loop performance, r_w is defined as tuning parameter.

To obtain the optimal ΔU that shall minimize *J,* from Eq. (11), *J* is represented as

$$\begin{aligned} J = {} & (R - Fx(n_i))^T (R - Fx(n_i)) - 2\Delta U^T \alpha^T (R - Fx(n_i)) \\ & + \Delta U^T (\alpha^T \alpha + R') \Delta U \end{aligned} \tag{11}$$

From derivative of Eq. (11), we get

$$\frac{\delta J}{\delta \Delta U} = -2\alpha^T (R - Fx(n_i)) + 2(\alpha^T \alpha + R')\Delta U \tag{12}$$

To find the minimum value of J, we apply necessary condition given as

$$\frac{\delta J}{\delta \Delta U} = 0$$

The optimal solution can be defined for the control signal in next equation.

$$\Delta U = (\alpha^T \alpha + R')^{-1} \alpha^T (R - Fx(n_i)) \tag{13}$$

In Eq. (13), the term $(\alpha^T \alpha + R')^{-1} \alpha^T R$ corresponds to reference signal change, while the term $-(\alpha^T \alpha + R')^{-1} \alpha^T F$ corresponds to the state feedback control of preview control system. Thus,

$$\begin{aligned} \Delta u(n_i) &= [1\ 0\ 0 \ldots 0]\ (\alpha^T \alpha + R')^{-1} (\alpha^T R' r(n_i) - \alpha^T F x(n_i)) \\ &= K_y r(n_i) - K_{\text{preview gain}} x(n_i) \end{aligned} \tag{14}$$

5 Numerical Example

In system (1), let $A = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix}$, $B = \begin{bmatrix} 0.5 \\ 1 \end{bmatrix}$, $C = \begin{bmatrix} 1 & 0 \end{bmatrix}$ and $D = 0$.

We perform the simulation for different situation of previewed length and control horizon length. Here, we take the control horizon length is four and previewed length is ten, respectively.

With the help of MATLAB, we have been performed the implementation of preview control for discrete time system. In the result, the output signal follows the reference signal.

Results:

The corresponding results are given below (Figs. 1 and 2):

Rise Time = 1.7028
Settling Time = 4.2673
Settling Min = 0.9138
Settling Max = 1.0797
Overshoot = 7.9663
Undershoot = 0
Peak = 1.0797
Peak Time = 3.

The corresponding results are given below for preview length with 15 (Figs. 3

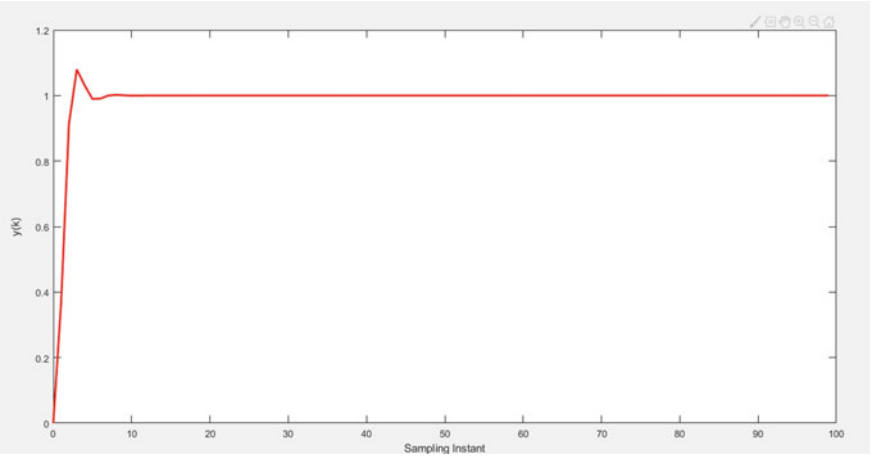


Fig. 1 The output response of the closed-loop system

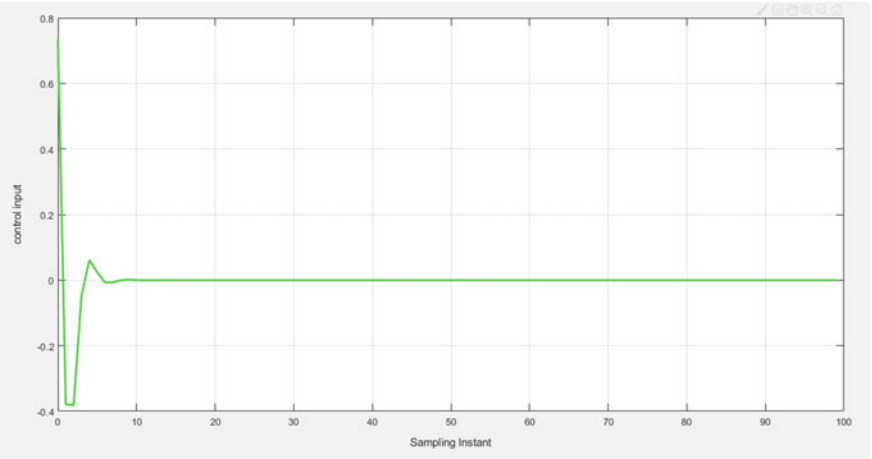


Fig. 2 The control input signal

and 4):

Rise Time = 1.7191
Settling Time = 4.2743
Settling Min = 0.9031
Settling Ma = 1.0714
Overshoot = 7.1387
Undershoot = 0
Peak = 1.0714
Peak Time = 3

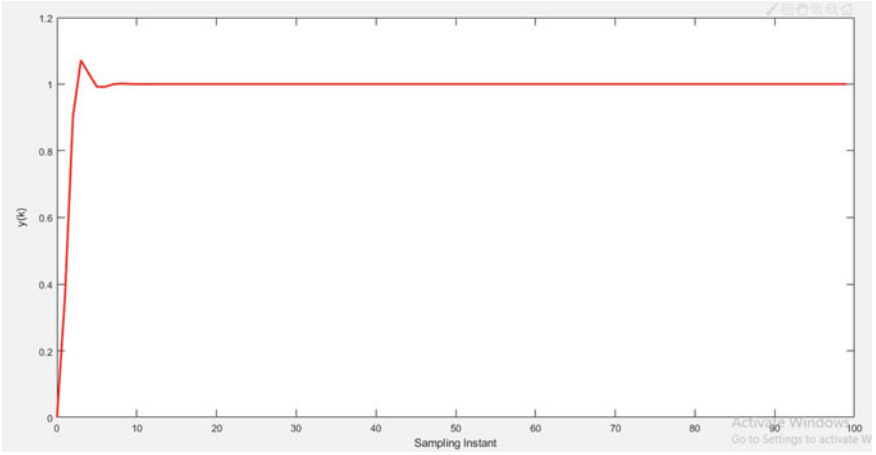


Fig. 3 The output response of the closed-loop system with different preview length

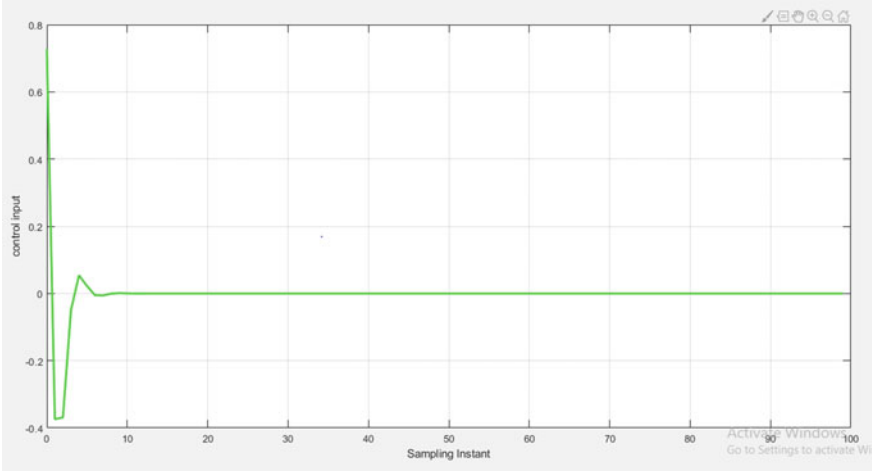


Fig. 4 The control input signal

6 Conclusion

This paper investigates the preview tracking issue for discrete-time systems. An augmented error system, taking previewed information is formulated by taking advantages of the subtraction between the system states which convert tracking issue into regulator problem. We have been implemented the preview control problem on MATLAB successfully. The numerical result for the closed-loop system with different preview length also gives the benefits of preview control in enhancing the tracking quality.

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Design of 15-4 Compressor for DSP Application

Sanjiv Kumar Gupta, Amit Dhawan, and Manish Tiwari

1 Introduction

Today, there is a need for DSP systems that fulfill the condition of low power, less area, and high speed. Hence, it becomes very important to design an energy-efficient digital signal processor because signal filtering, convolution, and correlation are done through these processors [1]. The performance of these processors depends upon its basic building blocks like adder, shifter, and multiplier.

The multiplier consumes more power and time, so design an efficient multiplier has always been an inspiring area for researchers. Multiplier operations are classified into three stages which are as follows: (I) production of partial product, (II) minimization of partial product, (III) final addition. The second stage is much more responsible for the performance of multiplier [2, 3]. A lot of methods for the reduction of partial products have been discussed in the literature [4–8]. In these methods, a compressor is very useful to reduce the partial product [9, 10].

The working of compressor logic is based on the counter property. A compressor counts the numbers of "one" in the input sequence [11, 12]. Small size compressors like 4-2 and 5-3 are not suitable for large size multiplier. Higher-order compressors are required for 16×16, 32×32 bit multipliers. These higher bit compressors are useful to increase the speed of the multiplier [13]. The paper is structured as follows: Sect. 2 is the reproduction of a conventional 5-3 compressor. A 15-4 compressor is

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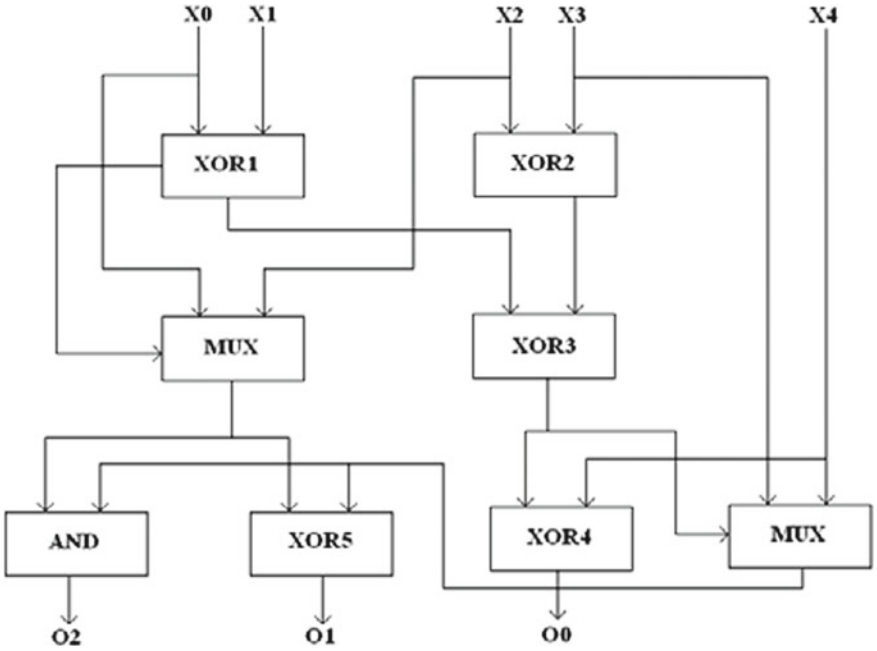

Fig. 1 A 5-3 compressor

proposed in Sect. 3. The simulation results of the designed modules are described in Sect. 4. The conclusion part is discussed in Sect. 5.

2 5-3 Compressor

Compressor is made of half adders or full adders and so works similarly to an adder. Compressor is playing a significant role to increase the speed of the multiplier by reducing partial products at the second stage. In this section, a conventional 5-3 approximate compressor has been reproduced [14–16]. Figure 1 describes the block diagram of 5-3 compressor. This compressor receives five inputs (X_0, X_1, X_2, X_3, X_4) and compresses into three outputs (O_0, O_1, O_2). Since this is an approximate circuit, so its error rate is considered [17–19].

3 Design of 15-4 Compressor

This section presents a modified 15-4 compressor. This compressor is designed using only five 5-3 compressors and one Kogge–Stone adder. The structure of this

compressor is as follows: The first stage is implemented by three 5-3 compressors that receive fifteen inputs (I_0–I_{15}) and output of this stage to apply in second stage that is designed by two 5-3 compressors and finally output of these compressors to apply Kogge–Stone adder. Here, Kogge–Stone circuit provides output (Q_3–Q_0) of 15-4 compressor.

The Kogge–Stone adder is based on parallel prefix addition. Carries are generated in a parallel manner in this adder. It is a high-performance adder, but it requires large area [20]. Figure 2 describes the architecture of 15-4 compressor.

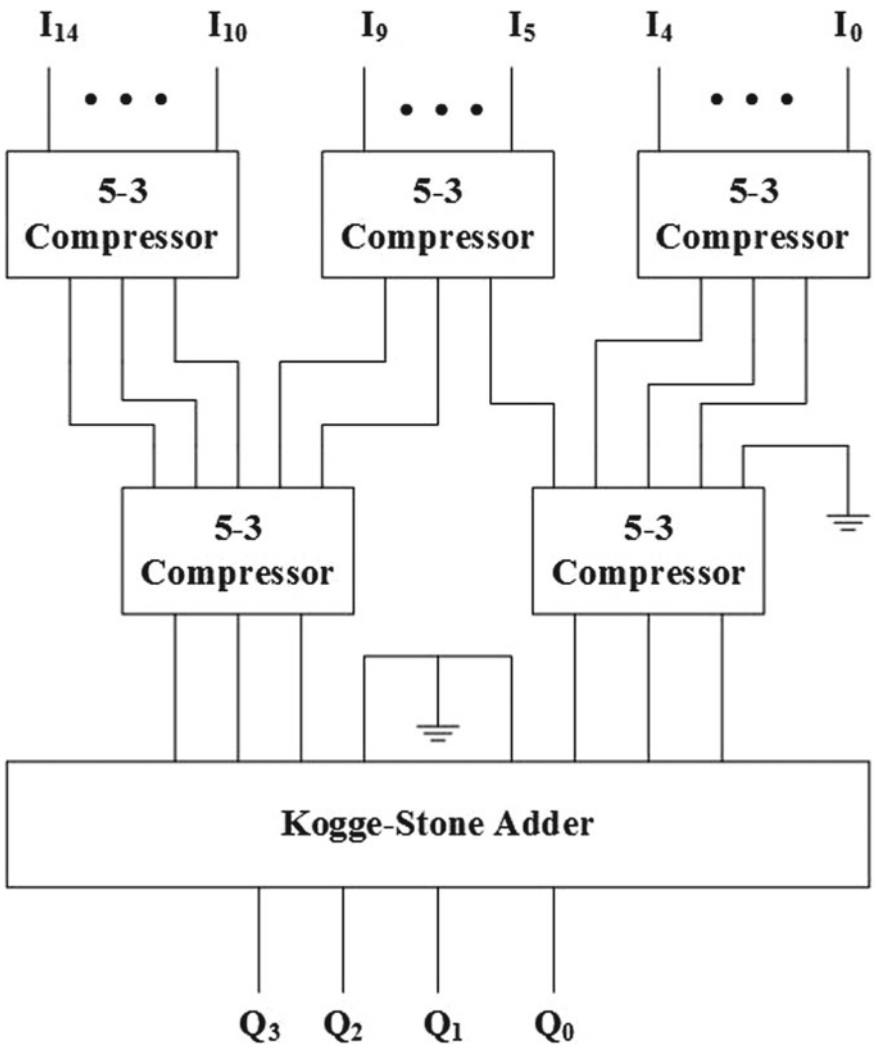

Fig. 2 15-4 compressor

4 Simulation Result and Discussion

The design of 5-3 compressor, Kogge–Stone adder, and 15-4 compressor is coded in Verilog HDL in Xilinx ISE Design Suite 14.7 and Xilinx ISim simulator is used for simulation.

4.1 5-3 Compressor

Result of simulation for 5-3 compressor is discussed in this section. Figure 3 shows RTL view of 5-3 compressor, and Fig. 4 shows functional verification where output

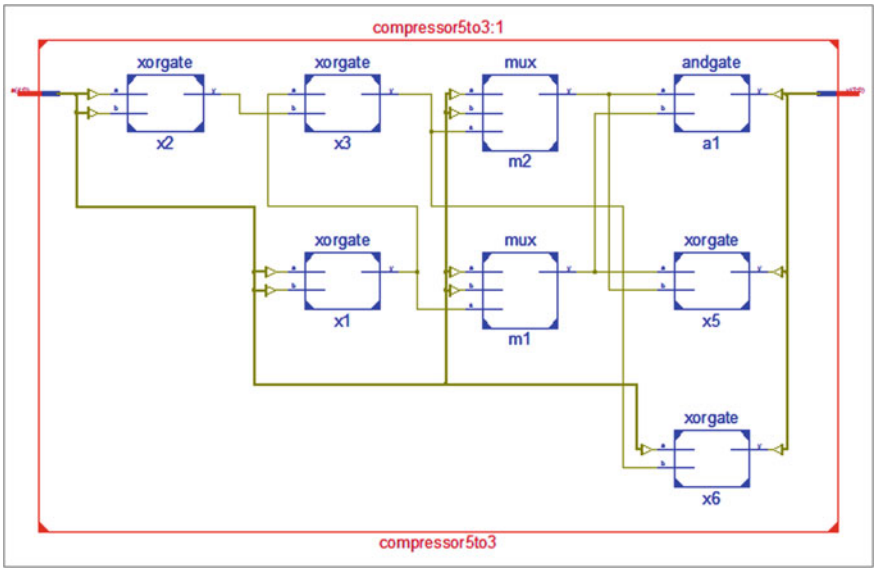

Fig. 3 RTL of 5-3 compressor

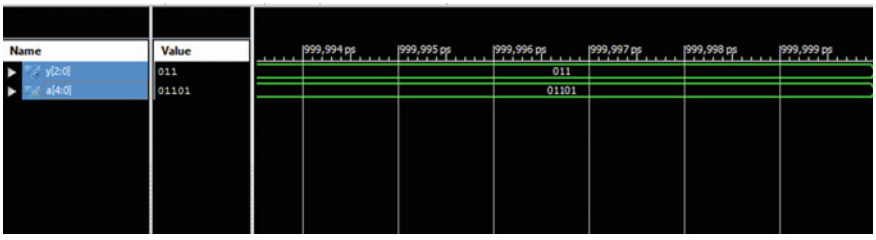

Fig. 4 Output of 5-3 compressor

Table 1 Delay analysis of 5-3 compressor

Cell:in- > out	fanout	Gate delay (ns)	Net delay (ns)
IBUF:I- > 0	2	1.218	0.622
LUT3:I0- > 0	2	0.704	0.622
LUT4:I- > 0	1	0.704	0.420
OBUF:I-. > 0		3.272	
Total delay = 7.562 ns (5.898 ns logic,1.664 ns route)			

Table 2 Device utilization of 5-3 compressor

Device utilization summary (estimated values)			
Logic utilization	Used	Available	Utilization (%)
Number of slice	3	4656	0
Number of 4 input LUTs	5	9312	0
Number of bonded IOBs	8	232	3

is 011 for input 01101. Table 1 represents delay of the circuit that is 7.562 ns, and Table 2 represents area utilization of the circuit.

4.2 Kogge–Stone Adder

RTL of Kogge–Stone adder is shown in Fig. 5, and functional verification of this adder is shown in Fig. 6.

4.3 15–4 Compressor

In this section, simulation result of 15-4 compressor is discussed. Figure 7 shows RTL view of 15-4compressor, and Fig. 8 shows functional verification. Table 3 represents delay of the circuit that is 13.69 ns, and Table 4 represents area utilization of the circuit.

5 Conclusion

In this paper, a 15-4 compressor is proposed. This 15-4 compressor is designed using five 5-3 compressor and one Kogge–Stone adder due to which it has higher speed

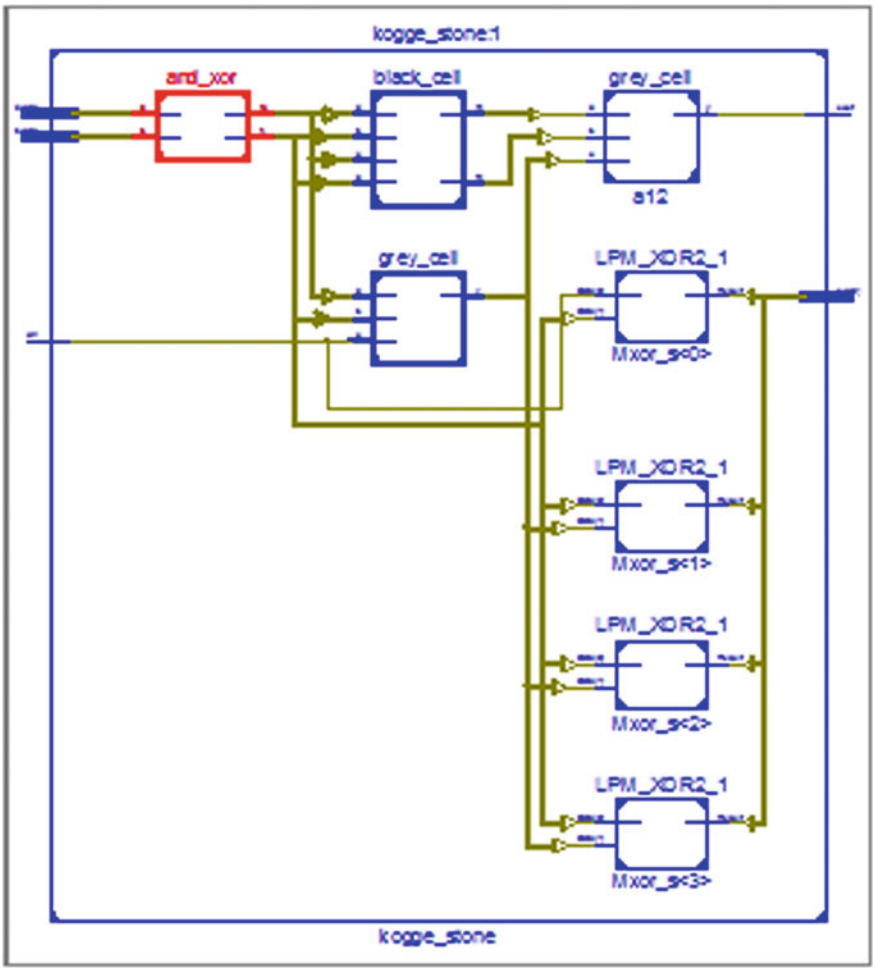

Fig. 5 RTL of Kogge–Stone adder

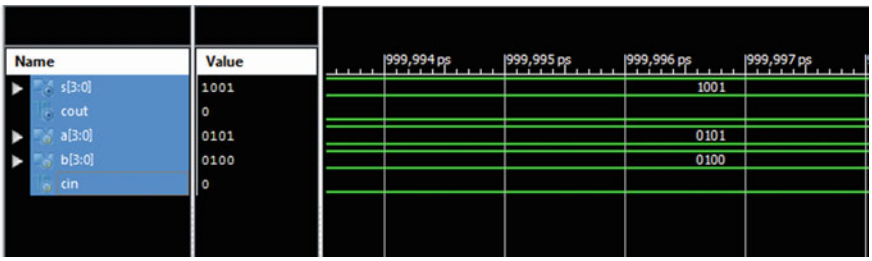

Fig. 6 Simulation result of Kogge–Stone adder

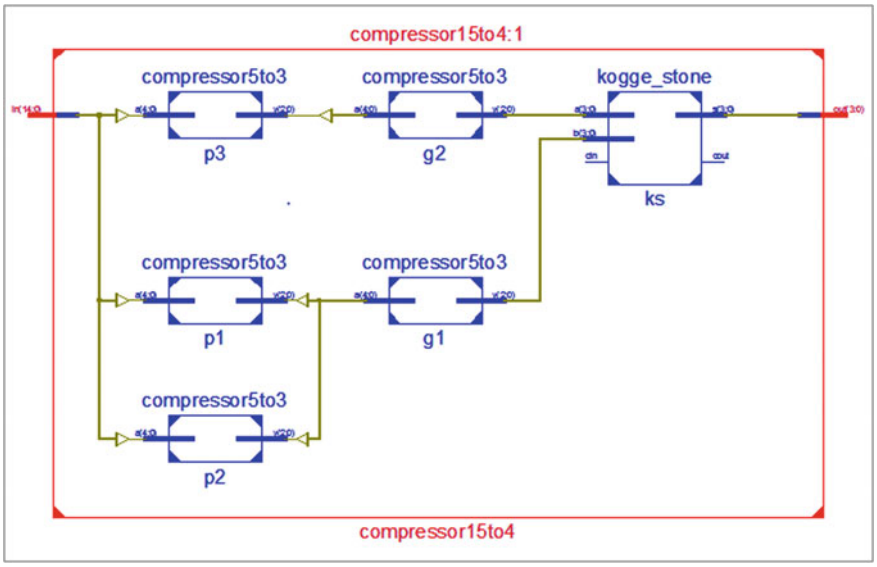

Fig. 7 RTL 15-4 compressor

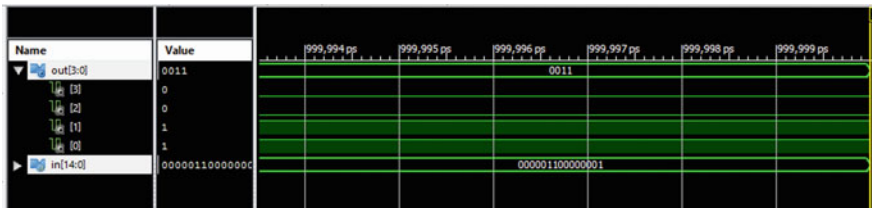

Fig. 8 Simulation result of 15-4 compressor

Table 3 Delay analysis of 15-4 compressor

Cell:in- > out	fanout	Gate delay (ns)	Net delay (ns)
IBUF:I- > 0	2	1.218	0.622
LUT4:I0- > 0	3	0.704	0.706
LUT3:I0- > 0	3	0.704	0.566
LUT4:I2- > 0	2	0.704	0.447
MUXF5:S- > 0	2	0.739	0.526
LUT2:I1- > 0	2	0.704	0.451
LUT4:I3- > 0	1	0.704	0.499
LUT3:I1- > 0	1	0.704	0.420
OBUF:I- > 0		3.272	
Total Delay = 13.690 ns (9.453 ns logic,4.237 ns route)			

Table 4 Device utilization of 15-4 compressor

Device utilization summary (estimated values)			
Logic utilization	Used	Available	Utilization (%)
Number of slice	14	4556	0
Number of 4 input LUTs	24	9312	0
Number of bonded IOBs	19	232	8

compared to conventional compressor. It has delay of 13.69 ns. Future application of this compressor is to design higher bit multiplier for DSP application.

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UWB Antenna for ITS Application

Satya Prakash Singh, Mukesh Kumar, Anil Kumar, and Rohini Saxena

1 Introduction

Transportation plays an important role in human life and economy of country. It is the backbone of the human life. The delays due to congestion, bad weather condition and other environmental hazard can affect the economy of the country. Many accidents occur and many lives are in endangered due to accidents. With help of growing wireless communication, intelligent transportation systems (ITS) can decrease the delay and avoid accidents. There are many applications of ITS with respect to security of vehicle and life. There are many applications like blind spot detection, adaptive cruise control, lane changing, etc. that came in security. These applications are achieved by long-range radar (LRR) and short-range radar antenna (SRR). The LRR and SRR should work on 24 GHz and 79 GHz frequency. Millimetre wave (MW) frequency range is also used in intelligent transportation system applications.

Brooker [1] proposed a 77 GHz and 94 GHz MW radar having bandwidth of 2 GHz and 4.9 GHz, respectively. Beer et al. [2] proposed a 77 GHz antenna having gain of 15.8 dBi. Hasch et al. [3] proposed a 77 GHz MW technology for automotive radar sensors having bandwidth of 4 GHz and half power beam width gain of 5 dBi. Artemenko et al. [4] proposed a 77 GHz beam-steerable lens antenna with bandwidth of 35 GHz. Ojaroudi et al. [5] proposed an antenna for UWB application which works in frequency range of 2.72–12.06 GHz and having impedance bandwidth of 125%. Gao et al. [6] proposed a wide slot UWB antenna for intelligent transportation application. It operates from 2.89 to 11.52 GHz frequency range. Li et al. [7] proposed a dielectric

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patch array antenna having centre frequency, impedance bandwidth and gain of 60 GHz, 23% and 17.5 dBi, respectively. Next, Zhou et al. [8] proposed a linearly polarized patch array antenna. The proposed antenna operates from frequency range of 23.2 to 24.8 GHz (6.67%) with return of 15 dB and its gain varied from 16 to 19 dBi. Ahmed Jamal Abdullah Al-Gburi [9] proposed a strawberry-shaped UWB monopole antenna. The frequency selective surface (FSS) has 10 × 10 array structure which produced bandwidth of 8.85 GHz for frequency range of 3.05–11.9 GHz. Danjuma [10] proposed a UWB antenna for body imaging applications. It works on frequency range of 3.1–10.6 GHz. Asokan [11] proposed a UWB antenna from impedance resonators. The proposed antenna works on frequency range of 2.58–10 GHz.

Mohamadzade [12] proposed a UWB antenna with monopole pattern. There are different circular rings cut to achieve wide bandwidth. It works on frequency range of 2.85 to 8.6 GHz. Sang [13] proposed a UWB Vivaldi antenna with high gain. It works on frequency range of 6–18 GHz with highest gain of 5.5 dBi. Gorai [14] proposed a notch UWB dual-band antenna for Bluetooth application. The proposed antenna works on frequency range of 3–12 GHz having a centre frequency of 2.4 GHz. It has gain of 4 dBi.

Shan and Shen [15] proposed a dual-band UWB tag antenna. It works on two different frequency bands. It has frequency range of 919–931 MHz in the lower band and 3.28–6.95 GHz in higher band. Chattha [16] proposed a UWB multi-input multi-output (MIMO) antenna. It has size of 23 × 26 × 0.8 mm3. It works from 3 to 10.6 GHz frequency range. Karmakar [17] proposed a UWB triple-band antenna. The proposed antenna has circular polarization. The proposed antenna covers frequency range of 3.1–11 GHz. Guo [18] proposed a UWB Vivaldi antenna for airborne applications. It works on frequency range from 300 to 2 GHz. It has maximum gain of 11.5 dBi. Moosazadeh et al. [19] proposed an mm-Wave antenna. It works on frequency range of 5–50 GHz. It has maximum gain of 14 dBi. Novak et al. [20] proposed an mm-Wave antenna having centre frequency of 60 GHz. It works in frequency range of 24–72 GHz. It has maximum realized gain of 13 dBi. Moosazadeh et al. [21] proposed an mm-Wave antenna. It works in frequency range of 3.4–40 GHz. It has gain of 14.3 dBi.

In this paper, proposed antenna has very large bandwidth with band range of 19–129.6 GHz. The proposed antenna has high gain. A novel antenna design is proposed based on meander line slot cut on ground plane. Parametric analysis is done in this paper. Proposed antenna is also circularly polarized in nature. The proposed antenna is used in ITS applications. The proposed antenna is designed and simulated in HFSS.

This paper is organized as follows: Sect. 2 shows design steps and process of proposed antenna. Results are discussed in Sect. 3. Finally, paper is concluded in Sect. 4.

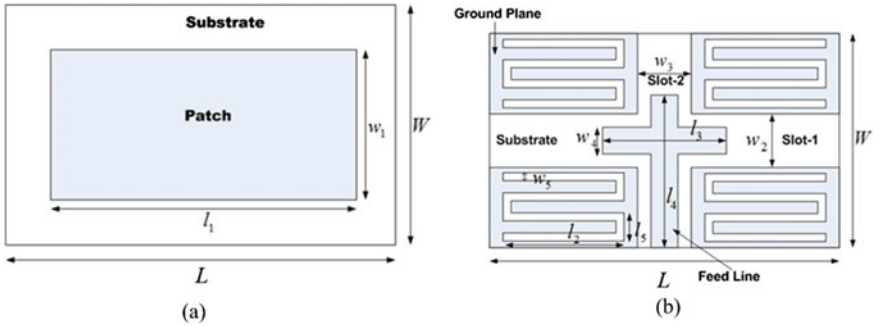

Fig. 1 Proposed structure shows **a** patch and **b** ground plane

Table 1 Values of parameter (in mm)

Parameters	Value	Parameters	Value
L	20	l_2	7
W	14	l_3	8
l_1	18	l_4	10
w_1	10	l_5	1.75
w_2	4	w_4	2
w_3	4	w_5	0.5

2 Design Specification

In this section, the proposed antenna design structure has been discussed. Figure 1 shows proposed antenna structure. The printed board used in this proposed structure is Rogers R03210 with dielectric constant of 10.2 and height of 1.28 mm. The dimension of the substrate material is $L \times W$. The patch is shown in Fig. 1a. The length and width of the patch are l_1 and w_1, respectively. Defected ground plane is shown in Fig. 1b. The two slots are cut out from ground plane with width of w_2 and w_3. The meander line slot is also etched out from the ground plane having dimension parameter of l_2, l_5 and w_3 as shown in Fig. 1b. There is cross-shape coplanar waveguide feed line. The cross-shaped feed line has dimension of l_4 and l_3. The feed line width is w_4. The parametric values are shown in Table 1.

3 Results and Discussion

The proposed design is simulated by using HFSSv13 [22]. Parametric analysis is done for proposed antenna structure. The return loss results by parametric analysis are shown in Table 2. From Table 2 result analysis, the parameter values are set for 79 GHz centre frequency as shown in Table 1.

Table 2 |S11| data by parametric analysis

Parameters	Parameter value (in mm)	f_c (in GHz)	|S11| (in dB)	Bandwidth (at −20 dB) (in GHz)
l_1	16	79.2	−25.33	11.7
	18	79	−25.25	13.4
	20	79.6	−25.46	10.7
w_1	8	79.3	−23.55	7.7
	10	79	−25.25	13.4
	12	80.8	−24.18	10.6
w_2	3	81.55	−27.06	11.71
	4	79	−25.25	13.4
	5	78.05	−30.64	10.80
w_3	3	75	−22.36	8.33
	4	79	−25.25	13.4
	5	80.1	−28.84	9.95
l_3	6	78.1	−30.5	10
	8	79	−25.25	13.4
	10	78.2	−28.5	13.06
l_4	9	80.1	−30.89	9.01
	10	79	−25.25	13.4
	11	78	−35	7.86

The |S11| result is shown in Fig. 2. This figure shows that the proposed antenna has very wide band range from 19 to 129.6 GHz having bandwidth of 110.6 GHz. The wide band covers most of the millimetre wave and intelligent transportation application frequencies. It has many centre frequency like 24.5 GHz, 30.5 GHz, 34.1 GHz, 37 GHz, 79 GHz and 114 GHz.

Figure 3 shows the vector current distribution on the surface of antenna structure. This shows that the coupling between feed line and patch makes the antenna resonates at 79 GHz. The meander line slots in ground plane to improve the band range of the proposed antenna.

The simulated radiation pattern is shown in Fig. 4. This result shows the E plane and H plane of the proposed antenna structure. This result shows that antenna is circularly polarized.

Figure 5 shows 3D radiation pattern at frequency 79 GHz. This result shows the way antenna is radiated.

Figure 6 shows the axial ratio over the frequency 10 GHz–130 GHz. The axial ratio is below 3 dB over the frequency range of 23–36 GHz and 77.5–90.5 GHz. This shows that the antenna is circularly polarized for above band. Figure 7 shows

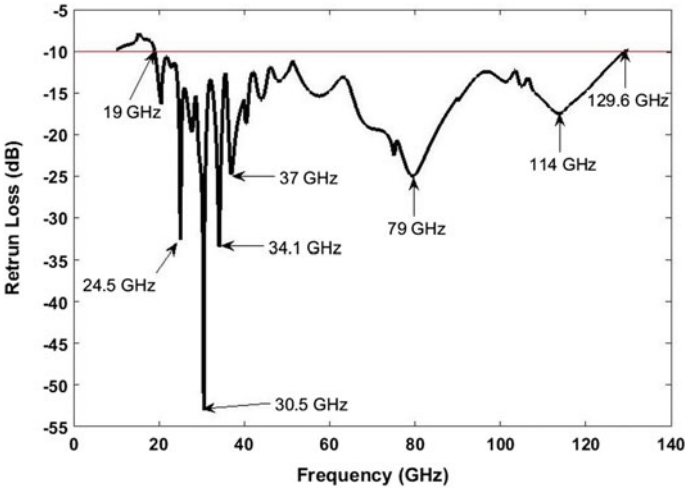

Fig. 2 A simulated return loss in dB

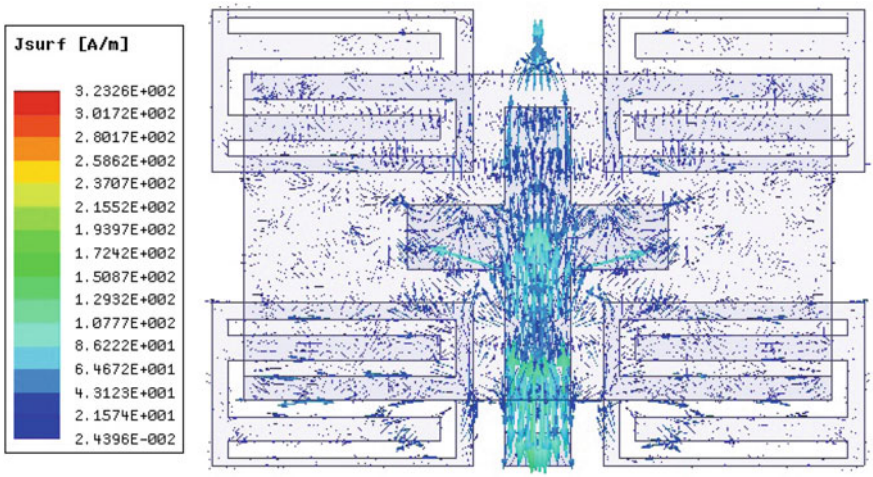

Fig. 3 Surface vector current distribution

the gain plot for frequency range 10–130 GHz. This result shows that the maximum gain of antenna is 19.26 dBi at 79 GHz resonant frequency.

Finally, the proposed work is compared with recent published work as shown in Table 3. This shows that the proposed antenna gives better result.

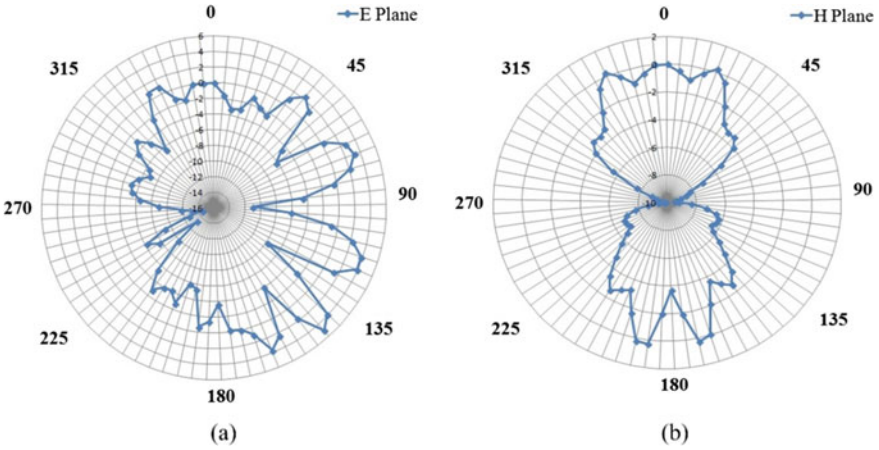

Fig. 4 Simulated radiation pattern of **a** E plane and **b** H plane at 79 GHz frequency

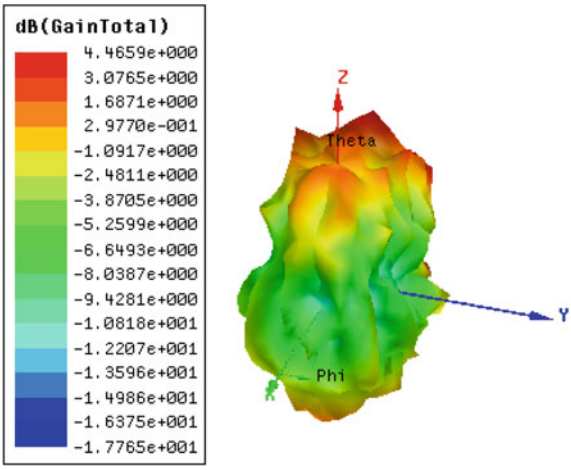

Fig. 5 Simulated radiation 3D radiation pattern at 79 GHz frequency

4 Conclusion

The proposed antenna works in millimetre wave frequency band. It has very wide band range. The measured band range is 19–129 GHz. It has bandwidth of 113 GHz. The coplanar wave guide makes antenna to work in high frequency range. The meander line slots in ground plane to improve the bandwidth of the antenna. The proposed antenna has very high gain of 19.26 dBi. The antenna is circularly polarized in nature. The proposed antenna is very suitable of intelligent transportation and millimetre wave application.

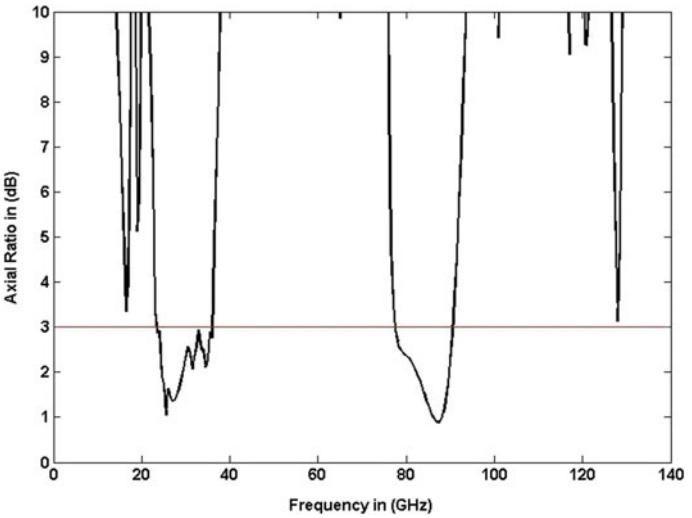

Fig. 6 Simulated axial ratio

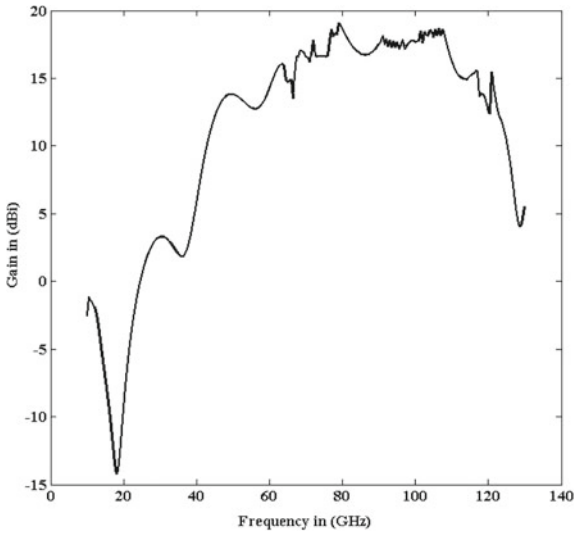

Fig. 7 Simulated gain in dBi with respect to frequency in GHz

Table 3 Values of parameter (in mm)

Parameters	Ahmed Jamal Abdullah Al-Gburi et al. [9]	Mahdi Moosazadeh et al. [20]	Markus H. Novak et al. [21]	Mahdi Moosazadeh et al. [22]	Proposed work
Centre frequency (GHz)	9	24	60	24	79
Bandwidth (GHz)	8	45	48	36.6	113
Gain (dBi)	10	14	13	14.3	19.26

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FPGA-Based Modulation Technique for Five-to-Three-Phase Ultra Sparse Matrix Converter

Tannistha Malakar, Vulavakayala Siva, and Santosh K. Singh

1 Introduction

The world is in the quest of highly efficient and economic technologies which will help to achieve automated industrial environment. For automation, there is dominance of mainly two technologies—computers and power electronics. The first electronics revolution was started with the invention of semiconductor devices, whereas the power semiconductor devices started the second electronic revolution [1]. Power electronics is enabling technology for distributed power generation.

In modern days, the power generation and transmission are done using three-phase systems. As the number of phases increases in AC machines, the phase current reduces, but the power handling capacity and efficiency of the machine increase. That is why, five-phase permanent magnet synchronous generator is being considered as wind power generator in this paper. In five-phase system, the apparent power is $2.629 V_L I_L \cos\phi$ as compared to $1.732 V_L I_L \cos\phi$, which is the apparent power of three-phase system. Thus, five-phase system has higher power handling capability. A symmetrical balanced five-phase system can be realised as five single-phase systems separated with 72° phase displacement. To integrate five-phase system with conventional three-phase system, five-to-three-phase AC-AC converter is required. As it is intended to use this converter at the generating station, bidirectional power flow capability is not necessary.

DSP and FPGA are most popular choices in designing digital controller for power electronics converters. The FPGA outperforms DSP in power converter switching applications because of its parallel computational capability. DSP devices can perform A/D conversion in sequence only, whereas FPGA can perform A/D conversions

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in parallel. This results in better sensing stage performance in FPGA than DSP. For better performance, FPGA is used to design the controller [2]. To realise the control strategy, XILINX system generator (XSG) toolbox in MATLAB Simulink is used.

2 Five-to-Three-Phase USMC

Matrix converter is one of the state-of-the-art AC–AC converter. It posses many benefits like unity power factor operation, low switching losses, reduced size, improved efficiency, no DC-link reactive elements and high reliability [3].

Matrix converters can be categorised in two types, direct matrix converter or conventional matrix converter (CMC) and indirect matrix converter (IMC), depending upon the topologies [4, 5]. IMC transforms AC voltage and frequency in two stages. At first, the input AC is transformed into DC using rectifier arrangement, and then this DC is converted into output AC with desirable voltage and frequency using inverter arrangement. Therefore, IMC involves intermediate DC-link. Further IMC can be categorised in four types depending on the number of switching devices used [6]. With the realisation of PWM buck rectifier, USMC topology is conceptualised. Due to the low number of transistors used, this topology is denoted as ultra sparse matrix converter. The reduced number of switching devices comes at the cost of restriction to the reversibility of the DC-link current. To supply highly inductive load, this limitation could be eliminated by using compensating capacitor bank.

In USMC topology, the input AC quantities are first converted into DC quantities, and then this DC quantities are converted to AC with desirable frequency. To feed the generated five-phase power to the existing three-phase system, a novel five-phase to three-phase USMC is proposed. The rectifier section of the converter contains five legs each with one transistor and four diodes. The inverter section is similar to VSI. This proposed USMC employs total of eleven transistors and twenty six diodes compared to sixteen transistors and sixteen diodes in voltage source DC-link back-to-back converter (V-BBC) used in wind energy conversion system [7]. The reduced number of controlled switches reduces the complexity of the controller and makes it cost-effective. Also the elimination of the DC-link capacitor increases the reliability of the overall converter (Fig. 1).

3 Modulation Technique for USMC

Sinusoidal pulse width modulation (SPWM) is broadly used in variable speed induction machine drive. Though this technique is easy to implement, it has the disadvantages of high THD and unable to utilise full DC-link voltage [8]. On the other hand, space vector pulse width modulation (SVPWM) technique provides more voltage output compared to other commonly used modulation strategies. Because of this reason, in this paper, SVPWM technique is used as the control strategy of five-to-

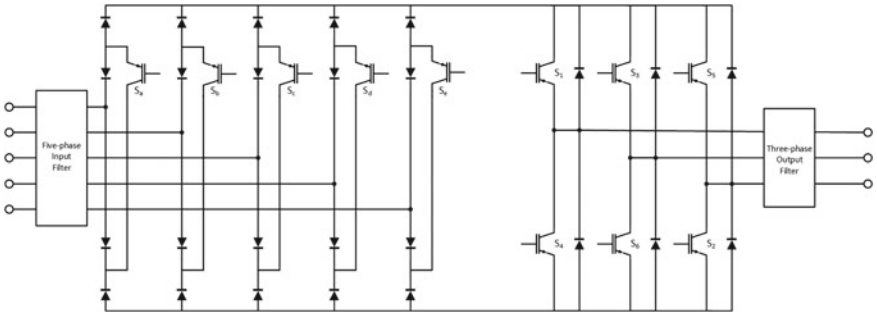

Fig. 1 Five-to-three-phase USMC Circuit Diagram

three-phase USMC. The operation and control of five-to-three-phase USMC can be analysed by the back-to-back connection of the input stage rectifier of C-BBC and the output stage inverter of V-BBC with no passive element present in the DC-link.

3.1 Five-Phase Space Vector

All the AC quantities can be considered as vectors, having both magnitude and direction (angle). Assume a five-phase balanced AC system with phase voltages,

$$v_{an} = V_m \sin \omega t \tag{1}$$

$$v_{bn} = V_m \sin\left(\omega t - \frac{2\pi}{5}\right) \tag{2}$$

$$v_{cn} = V_m \sin\left(\omega t - \frac{4\pi}{5}\right) \tag{3}$$

$$v_{dn} = V_m \sin\left(\omega t - \frac{6\pi}{5}\right) \tag{4}$$

$$v_{en} = V_m \sin\left(\omega t - \frac{8\pi}{5}\right) \tag{5}$$

$$\mathbf{v_s^*} = v_{an} + v_{bn}e^{j\frac{2\pi}{5}} + v_{cn}e^{j\frac{4\pi}{5}} + v_{dn}e^{j\frac{6\pi}{5}} + v_{en}e^{j\frac{8\pi}{5}} \tag{6}$$

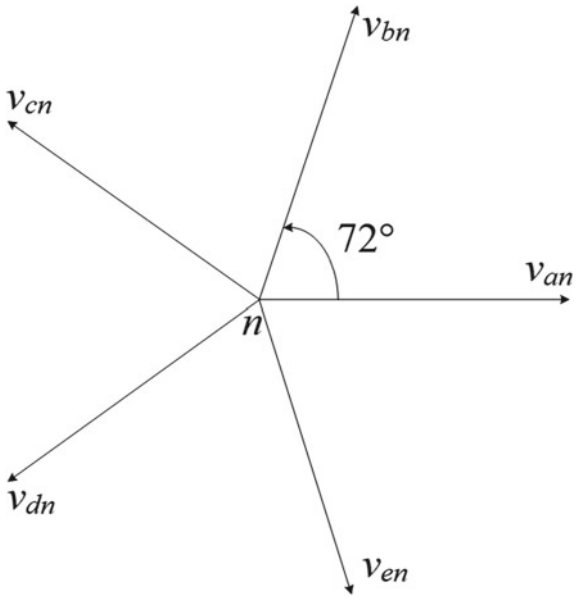

Fig. 2 Five-phase system vector representation

Substituting the values of v_{an}, v_{bn} and v_{cn} in the above equation (Fig. 2),

$$\mathbf{v_s^*} = 2.5V_m(\sin \omega t - j \cos \omega t) \tag{7}$$

3.2 SVPWM Three-Phase Inverter

In SVPWM technique, the entire inverter module is considered as a single unit. At any given time, only one phase should be switched.

$$v_{a0} = v_{an} + v_{n0} \tag{8}$$

$$v_{b0} = v_{bn} + v_{n0} \tag{9}$$

$$v_{c0} = v_{cn} + v_{n0} \tag{10}$$

$$\therefore v_{n0} = \frac{1}{3}(v_{a0} + v_{b0} + v_{c0}) \tag{11}$$

There are three switches present in the three upper limbs of the inverter, respectively. They could be in ON/OFF state. So, there are total of eight switching states, (0, 0, 0) to (1, 1, 1) representing (S_1, S_3, S_5).

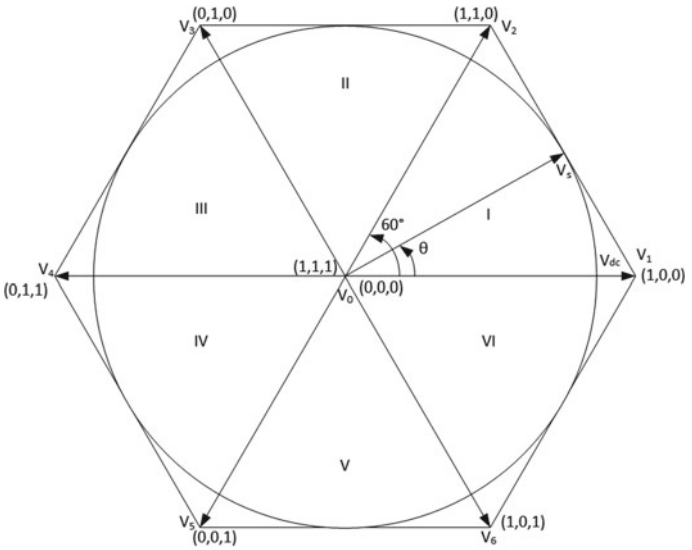

Fig. 3 Switching states of SVPWM inverter

T_0, T_1 and T_2 are the time durations of the switching states [0, 0, 0, [1, 0, 0] and [1, 1, 0], respectively. Solving the above equation (Fig. 3),

$$T_1 = aT_c \frac{\sin(60^\circ - \theta)}{\sin 60^\circ} = M_i \sin(60^\circ - \theta) \tag{12}$$

$$\text{and } T_2 = aT_c \frac{\sin\theta}{\sin 60^\circ} = M_i \sin\theta \tag{13}$$

$$\implies T_0 = T_c - (T_1 + T_2) \tag{14}$$

where $M_i = \dfrac{aT_c}{\sin 60^\circ}$. and T_c is the half of the sampling time, T_s.

Generalising Eqs. 12 and 13 for all of the six sectors,

$$T_u = M_i \sin[\frac{\pi}{3}s - \theta] \tag{15}$$

$$\text{and } T_v = M_i \sin[\theta - \frac{\pi}{3}(s-1)] \tag{16}$$

where s is the sector number in which $\mathbf{V_s^*}$ lies.

T_0 could be obtained by using the switching states either (0, 0, 0) or (1, 1, 1) or both. In any of the cases, the produced average voltage vector will be same. V_1 and

V_2 need not to be applied continuously within the sub-time period T_s. They could be divided in as many parts, but they should fall under T_s.

All the sectors should be equally used to produce symmetrical line voltages. All the samples should be positioned symmetrically about each sectors with one sample at the centre of that sector.

3.3 SVPWM Five-Phase Rectifier

SVPWM rectifier is preferred for AC–DC conversion compared to diode bridge rectifier. In SVPWM rectifier, the input side power factor could be controlled, and the sinusoidal source current is achieved.

It can be realised by the input stage rectifier of C-BBC with no freewheeling diode present in the DC-link. So, the modulation technique should always provide a path to flow the impressed DC-link current through the power transistors.

Assume a balanced five-phase system with input current $\mathbf{i_{in*}}$, defined as (Table 1)

$$\mathbf{i_{in}^*} = \hat{I}^* e^{-j\phi_{iin}^*} = \hat{I}^* e^{-j(\omega t - \phi_{in}^*)} \tag{17}$$

where $\hat{I}^*$ is the amplitude of the input current space vector, ω is the supply frequency, and ϕ_{in}^* is the required input phase displacement angle.

Similar to the SVPWM inverter, rectifier switching states are determined based on the position of the current space vector. For five-phase rectifier, there are total ten sectors depending upon the switching states. The switching sequence contains two active states and a zero state.

When the input current phase angle $\phi_{i_{in}}^*$ lies within $[-18°, +18°]$ *i.e.* sector-1, the possible switching states are aa, ac and ad. Therefore, there would be three switching sequences possible, which are

$$\ldots |_{t=0} (ad) - (ac) - (aa) |_{t=T_c} (aa) - (ac) - (ad) |_{t=T_s}$$

Table 1 Three-phase inverter switching states

No.	S_1	S_2	S_3	S_4	S_5	S_6	$\mathbf{v_s^*}$
1	0	1	0	1	0	1	$0\angle 0$
2	1	1	0	0	0	1	$V_{dc}\angle 0$
3	1	1	1	0	0	0	$V_{dc}\angle \frac{\pi}{3}$
4	0	1	1	1	0	0	$V_{dc}\angle \frac{2\pi}{3}$
5	0	0	1	1	1	0	$V_{dc}\angle \pi$
6	0	0	0	1	1	1	$V_{dc}\angle \frac{4\pi}{3}$
7	1	0	0	0	1	1	$V_{dc}\angle \frac{5\pi}{3}$
8	1	0	1	0	1	0	$0\angle 0$

$$\ldots|_{t=0}(aa)-(ac)-(ad)\,|_{t=T_c}(ad)-(ac)-(aa)\,|_{t=T_s}$$

$$\ldots|_{t=0}(ac)-(aa)-(ad)\,|_{t=T_c}(ad)-(aa)-(ac)\,|_{t=T_s}$$

The switching losses vary with the selection of the switching sequence of the rectifier. To place the zero switching state between the two active states, switching state of only one phase has to be changed. The formation of output DC-link voltage is determined by ϕ_{in}^* to maintain the power balance. The average output voltage is inversely proportional to ϕ_{in}^*.

$$I_{in}^* T_c = I_{dc} T_1 + I_{dc} T_2 + I_0 T_0 \tag{18}$$

where T_0, T_1 and T_2 are the time durations of the switching states aa, ac and ad, respectively. T_c is the half of the sampling time, T_s. Solving the above equation, it could be found that

$$T_1 = aT_c \frac{\sin(18^\circ - \phi_{i_{in}}^*)}{\sin 36^\circ} = M_r \sin(18^\circ - \phi_{i_{in}}^*) \tag{19}$$

$$\text{and } T_2 = aT_c \frac{\sin(\phi_{i_{in}}^* + 18^\circ)}{\sin 36^\circ} = M_r \sin(\phi_{i_{in}}^* + 18^\circ) \tag{20}$$

$$\Longrightarrow\ T_0 = T_c - (T_1 + T_2) \tag{21}$$

where modulation index, $a = \dfrac{\hat{I}_{in}^*}{I_{dc}} = [0, 1]$ and $M_r = \dfrac{aT_c}{\sin 36^\circ}$.

Generalising Eqs. 19 and 20 for all the sectors,

$$T_m = M_r \sin\left[\frac{\pi}{5}s - \left(\phi_{i_{in}}^* + \frac{\pi}{10}\right)\right] = M_r \sin\phi_m \tag{22}$$

$$\text{and } T_n = M_r \sin\left[\frac{\pi}{5} - \phi_m\right] \tag{23}$$

where s is the sector number in which $\mathbf{I_{in}^*}$ lies (Table 2).

Table 2 Switching states of rectifier section

No.	S_a	S_b	S_c	S_d	S_e	V_{dc}
1	1	0	1	0	0	V_{ac}
2	0	1	0	1	0	V_{bd}
3	0	0	1	0	1	V_{ce}
4	1	0	0	1	0	V_{da}
5	0	1	0	0	1	V_{eb}

3.4 SVPWM Matrix Converter

In IMC, the purpose of the rectifier stage is to produce sinusoidal input current and a positive DC-link voltage. The modulation is done in such a way that maximum voltage is available in the DC-link. The DC-link voltage is formed by the switching between two line voltages of five-phase supply. Then from this DC, three-phase AC voltage of desired frequency is produced.

At first, the input five-phase AC is sensed to calculate the rotating vector. Then according to the position of the rotating vector, ten sectors of 36° each are defined according to that. In each sector, the input line voltages used to form the DC-link voltage is different.

When the rotating vector lies in sector-1, phase-A is ON always and phase-C and phase-D are switched alternatively to form the DC-link voltage. So, the DC-link would contain the portions of v_{ac} and v_{ad}. When S_a and S_c are ON, the DC-link voltage follows the profile of v_{ac}. Similarly, when S_a and S_d are ON, the DC-link voltage follows v_{ad}. The duty cycle of the switches S_b and S_c is defined as

$$d_{ac} = -\frac{v_c}{v_a} \tag{24}$$

$$d_{ad} = -\frac{v_d}{v_a} \tag{25}$$

$$\text{and } d_{ac} + d_{ad} = 1 \tag{26}$$

The average DC-link voltage,

$$V_{dc} = d_{ac} \cdot v_{ac} + d_{ad} \cdot v_{ad} \tag{27}$$

Similarly, V_{dc} can be found for all the other sectors. After the formation of V_{dc}, the inverter could be controlled using SVPWM technique as described in *section* 3.2.

The voltage transfer ratio is defined as (Fig. 4)

$$m = \frac{\overline{V_s^*}}{\overline{V_{in}^*}} \tag{28}$$

In IMC topology, the switching of rectifier stage and the inverter stage has to be coordinated to produce balanced symmetrical input currents and output voltages. T_u, T_v and T_0 of the inverter stage are distributed among T_m and T_n of the rectifier stage maintaining the proportional ratio. The switching of rectifier stage is always done during the freewheeling period of the inverter stage to achieve zero DC-link current commutation.

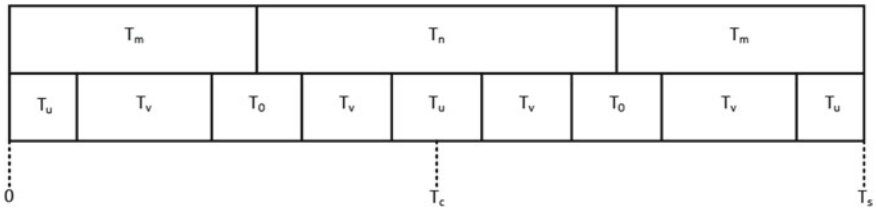

Fig. 4 Switching states within a pulse period

4 Modelling and Simulation

4.1 Filter Design

The matrix converter system dynamics are highly affected by the choice of filter design. In this topology, filter components are the only inertial elements present. That is why, a proper selection of the filter components is required so that the voltage regulation, efficiency, and the reactive current loading stay within the permissible limit [9].

Input Filter To provide path for switching frequency currents, input filter is essential in matrix converter topology. The most appropriate input filter for this topology is single stage LC filter. The value of C_{in} should be low, so that the input displacement factor (IDF) becomes minimum. However, for inductive load, a high value of C_{in} should be used. Damping resistors are used across the inductors. This arrangement provides minimum conflict between efficiency and damping requirements. The output current of the USMC decides the current rating of the input filter capacitors, C_{in} [9].

Output Filter A second-order ripple filter is also used in the output side of the USMC to provide a regulated three-phase AC voltage. The output current depends on the value of L_0. Proper selection of L_0 leads to the selection of C_{in} with low current rating [9]. The per phase representation of the input and output filter is shown in Fig. 5.

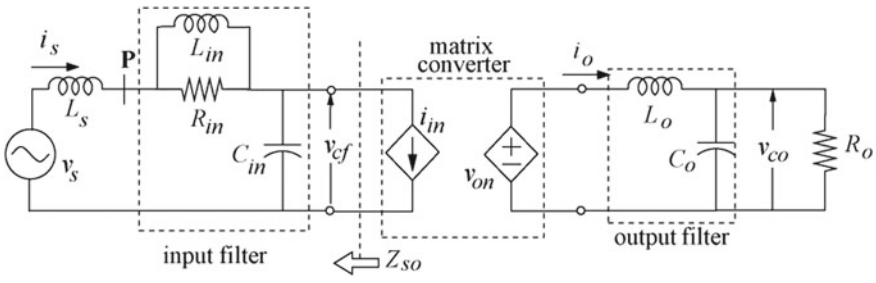

Fig. 5 Single-phase diagram of input and output filters for matrix converter [9]

4.2 Five-to-Three-phase USMC Simulation

Digital controllers can be designed and analysed in a virtual FPGA environment using XSG. Integrated platform of MATLAB-Simulink-XSG can be used for real-time FPGA-based controller designing using automatic HDL code generation functionality. Hence, it is necessary to model the controller in XSG for real-time implementation of the system using FPGA [10]. The simulation model of five-to-three-phase USMC is designed in MATLAB Simulink using XILINX blockset. The clock of the XILINX system generator is set to 10 ns. The test parameters are shown in the table 3.

At first, the phase voltages are sensed from a five-phase input voltage, and then gate pulses are generated according to that. After sensing the input phase voltages, the position of the input space vector is detected using CORDIC block from XILINX toolbox. Then the active sector is determined depending on the position of the input space vector. Then T_m and T_n are derived from the input space vector position, and the active sector for the rectifier section and T_c. T_c is calculated from the predetermined sampling time.

The determination of T_u, T_v and T_0 is same as three-phase USMC [4]. Then these T_u and T_v and T_0 are combined with T_m and T_n to determine the converter switching signals according to the input voltage space vector position. To avoid short circuiting of the DC-link voltage, finally, dead time is introduced between turn-off and turn-on of transistors in bridge legs of the inverter section [6].

Figure 6 shows the results of the simulation of FTTP USMC. With 25 Hz input frequency, the produced output frequency 50 Hz. The ripple factor of the DC-link voltage is 0.04. The output voltage THD is also less than 5% as shown in Fig. 7.

Figure 8 shows the input phase current profile corresponds to input phase voltage. The input current ripple factor can be reduced further with the use of higher order input filter.

Table 3 Simulation parameters of five-phase USMC

Input phase voltage	141.421 V
Input frequency	25 Hz
Modulation index	0.86
Switching frequency	4.5 KHz
Diode snubber resistance	1 MΩ
Damping resistance	1 Ω
Series inductance	150 μH
Shunt capacitance	150 μF
Series inductance	500 μH
Shunt capacitance	150 μF

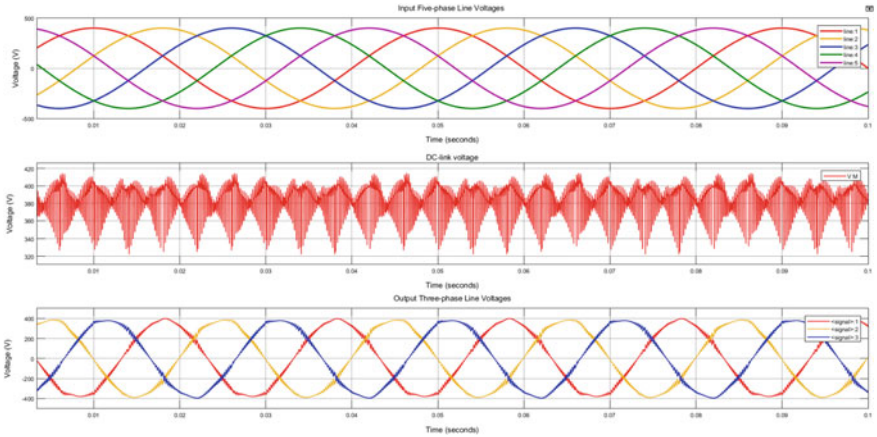

Fig. 6 Voltage profile of five-to-three-phase USMC

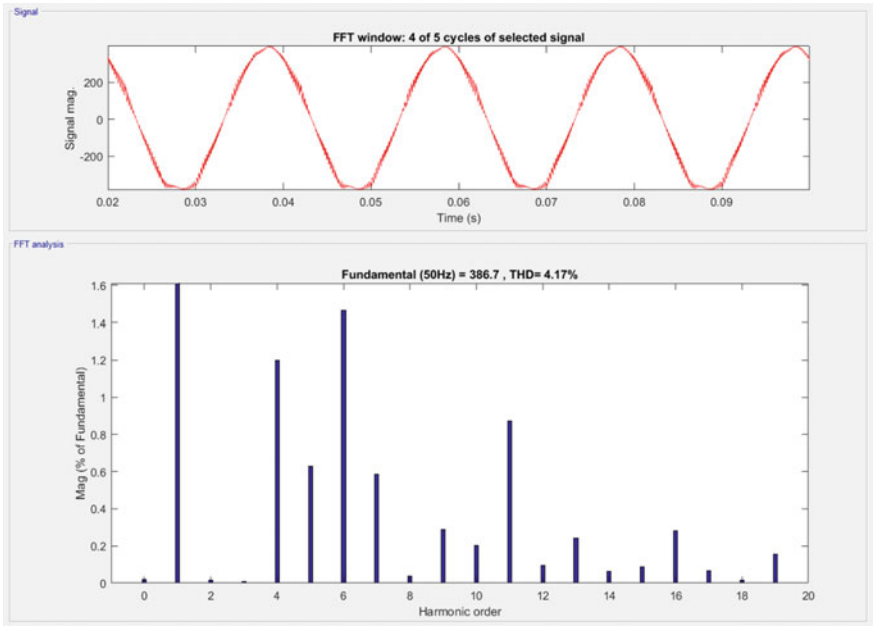

Fig. 7 FFT analysis of output voltage of five-to-three-phase USMC

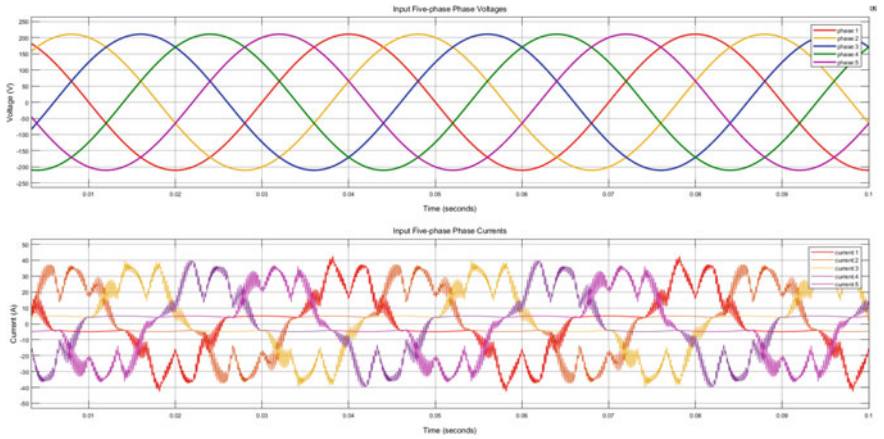

Fig. 8 Input current profile of five-to-three-phase USMC

5 Conclusion

A FTTP USMC is modelled to convert five-phase power to three-phase. The size and cost of the converter would be less than other types of converter serving same purpose. The modulation technique of FTTP USMC is derived and verified using MATLAB Simulink. The proposed modulation scheme uses space vector modulation technique to provide fixed output frequency from variable input frequency supply. The output voltage THD rating is under the permissible limit. Zero current switching of the rectifier section is achieved for FTTP USMC. The switching states symmetrically placed about the middle of a sample time. All switching sectors are used equally. As the switching frequency increases, the output voltage harmonics reduces further. In addition, the voltage output of the converter with this modulation technique could be controlled.

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Exact SER for Modulation Schemes Over Generalized Rician Fading Channel

Veenu Kansal, Rajanbir Singh, and Simranjit Singh

1 Introduction

The fading of the signal in wireless communication limits the performance of wireless systems. Fading essentially constitutes small-scale fading in which a signal rapidly changes its phase and amplitude over a small distance or time. Large-scale fading, in which signal variations observed over a large distance or time, is ignored in case of small-scale fading [1]. There are many fading distributions that characteristically define the mobile radio signal in a certain environment. The most commonly used distributions are the Rayleigh, Nakagami-*m*, and Rician fading distributions. The generalized Rician fading distribution is another interesting fading distribution, which encompasses the above-defined fading distributions as its special cases. This distribution can model the narrow-band and light-shadowed mobile radio channel [2]. The available literature on this fading distribution was exhaustively studied, and the most relevant literature is discussed below.

First-order statistics (probability density function (PDF)) and second-order statistics (level crossing rate and average duration of fade) of the generalized Rician fading distribution were derived in [3]. In [4], the authors used the moment generating function (MGF) approach to evaluate the error rate probability of the M-ary quadrature amplitude modulation (MQAM) multi-input multi-output (MIMO) orthogonal frequency division multiplexing (OFDM) systems. The BER of M-ary orthogonal modulation techniques was evaluated for the nonidentical generalized Rician fading channels, employing non-coherent equal-gain diversity in [5]. The outage probability, pairwise error probability, and bit error rate (BER) of orthogonal space–time block code OFDM systems were calculated through the MGF approach over correlated generalized Rician channels in [6]. Since the practical multipath of the signal is correlated, in order to better understand the correlated generalized Rician fading

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model, a complete study for the statistical properties of the correlated channel is presented in [7]. Exact symbol error rate (SER) analysis is quite tedious; therefore, to simplify calculations, the authors in [8] used asymptotic analysis to evaluate the SER of equal gain combining. Work done in [8] was extended to include the asymptotic SER performance of selection combining (SC) in [9]. In [10, 11], some new research papers are reported on the analysis of generalized Rician fading.

After reviewing the literature, we observed that a comprehensive analysis involving the SER of different modulation schemes was missing. However, the analysis is performed only for the M-ary modulations over this fading channel in [12]. In this work, we derived the generalized expressions of SER of various modulation schemes for the generalized Rician fading.

2 System Model

The received signal envelope is assumed to be follows: the distribution of generalized Rician fading. It is a general model that includes Rayleigh, Rician, and Nakagami-*m* as special cases. The PDF of signal to noise ratio (SNR) is obtained by using the square transformation [13]. The PDF of SNR form can be evaluated by [10]:

$$p_{\gamma}(\gamma) = \frac{\gamma^{\frac{n-2}{4}} \exp\left(-\frac{nK}{2} - \frac{\Omega\gamma}{2\sigma^2\overline{\gamma}}\right) I_{\frac{n}{2}-1}\left(\sqrt{\frac{nK\Omega\gamma}{\sigma^2\overline{\gamma}}}\right)}{2\left(\frac{\sigma^2\overline{\gamma}}{\Omega}\right)^{\frac{n+2}{4}} (nK)^{\frac{n-2}{4}}}. \tag{1}$$

where Ω denotes second moment of fading model, which is calculated by taken $k = 2$ in the below given equation [14]:

$$E\left[X^k\right] = \left(2\sigma^2\right)^{\frac{k}{2}} \exp\left(-\frac{s^2}{2\sigma^2}\right) \frac{\Gamma\left(\frac{n+k}{2}\right)}{\Gamma\left(\frac{n}{2}\right)} {}_1F_1\left(\frac{n+k}{2}, \frac{n}{2}; \frac{s^2}{2\sigma^2}\right), \tag{2}$$

The expression for second moment of this fading is given by:

$$\Omega = E\left[X^2\right] = n\sigma^2 \exp\left(-\frac{s^2}{2\sigma^2}\right) {}_1F_1\left(1 + \frac{n}{2}, \frac{n}{2}; \frac{s^2}{2\sigma^2}\right). \tag{3}$$

where $E[.]$ represents the expectation operator and denotes confluent hypergeometric function [15]. The generalized Rician K-factor characterizes the ratio of power of line of sight (LOS) signal component to the diffuse components which is given by $K = s^2/n\sigma^2$. This distribution changes to Rician for $n = 2$. It reduces to Rayleigh for $n = 2$ and $s = 0$, and this channel can also represent Nakagami-*m* for $n = 2\,m$ and $s = 0$, where m can hold only integer or half integer values [9].

3 Average Symbol Error Analysis

The average symbol error probability (ASEP) for modulation schemes can be found by integrating the conditional error probability over the PDF of the fading channel [13]:

$$P_e = \int_0^{\infty} P_e(\gamma) p_\gamma(\gamma) \mathrm{d}\gamma \tag{4}$$

where $P_e(\gamma)$ denotes the conditional symbol error probability (SEP) and $p_\gamma(\gamma)$ denotes PDF of the generalized Rician fading. There are generalized expressions of conditional SEP for various modulation schemes, which are provided as below.

(1) The general form of the conditional symbol error expression of the binary phase shift keying (BPSK), square MQAM, and quadrature phase shift keying (QPSK)/minimum shift keying (MSK) with coherent detection is:

$$P_e(\gamma) = A erfc\left(\sqrt{B\gamma}\right) + C erfc^2\left(\sqrt{B\gamma}\right) \tag{5}$$

(2) Conditional SER of differential phase shift keying (DPSK), binary frequency shift keying (BFSK), and M-ary frequency shift keying (MFSK) can be expressed as:

$$P_e(\gamma) = A \exp(-B\gamma) \tag{6}$$

(3) The conditional SER of M-ary phase shift keying (MPSK) and M-ary differential phase shift keying (MDPSK) can be represented in the form:

$$P_e(\gamma) = A \int_0^{\pi - \pi/M} \exp(-B(\theta)\gamma) \mathrm{d}\theta \tag{7}$$

The A, B, and C that depend on kind of modulations are given in Table 1 [13, 16–20, 22, 23].

3.1 The ASEP of Coherent Modulation Schemes

The modulation schemes included under coherent modulation detection are BPSK, MQAM, and QPSK/MSK. By substituting the series form of the Bessel function in (1), the PDF of the received SNR is evaluated as:

Table 1 Different values of A, B, and C for specific modulations

Modulation scheme	A	B	C
BPSK	1/2	1	0
MQAM	$2(1-1/\sqrt{M})$	$1.5\log_2(M)/(M-1)$	$-(1-(1/\sqrt{M}))^2$
QPSK/MSK	1	1	1/4
DPSK	1/2	1	0
MFSK	$\sum_{m=1}^{M-1} \frac{(-1)^{m+1}(M-1)!}{m!\,(m+1)(M-1-m)!}$	$\frac{m}{m+1}\log_2(M)$	0
BFSK	1/2	1/2	0
MPSK	$1/\pi$	$\frac{\sin^2(\frac{\pi}{M})\log_2(M)}{\sin^2(\theta)}$	0
MDPSK	$1/\pi$	$\frac{\sin^2(\frac{\pi}{M})\log_2(M)}{1+\cos(\frac{\pi}{M})\cos\theta}$	0

$$p_\gamma(\gamma) = \exp\left(-\frac{nK}{2} - \gamma\lambda\right) \sum_{l=0}^{\infty} \frac{(nK)^l \gamma^{l+\frac{n}{2}-1}(\lambda)^{l+\frac{n}{2}}}{2^l l!\Gamma\left(l+\frac{n}{2}\right)} \tag{8}$$

where $\lambda = \Omega/2\sigma^2\overline{\gamma}$.

Now we substitute (5) and (8) in (4) to get the average symbol error rate (ASER):

$$P_e = \underbrace{\int_0^\infty A erfc\left(\sqrt{B\gamma}\right).p_\gamma(\gamma)\mathrm{d}\gamma}_{I_1} + \underbrace{\int_0^\infty C erfc^2\left(\sqrt{B\gamma}\right).p_\gamma(\gamma)\mathrm{d}\gamma}_{I_2} \tag{9}$$

Now substituting the value of $p_\gamma(\gamma)$ in (9), we obtain I_1:

$$I_1 = A\exp\left(\frac{-nK}{2}\right)\sum_{l=0}^{\infty}\frac{(nK)^l}{2^{l-1}l!}\int_0^\infty \frac{1}{2}erfc\left(\sqrt{B\gamma}\right)\frac{(\lambda\gamma)^\alpha}{\alpha!}\exp(-\lambda\gamma)\mathrm{d}\gamma \tag{10}$$

where $\alpha = l + \frac{n}{2} - 1$.

The equation in (10) can be solved using the formula in [19], Eq. (17)]. We obtain I_1 as follows:

$$I_1 = A\exp\left(\frac{-nK}{2}\right)\sum_{l=0}^{\infty}\frac{(nK)^l}{2^{l-1}l!}\left(\frac{1}{2}\left(1-\sqrt{\frac{B}{\lambda+B}}\right)\right)^{\alpha+1} \sum_{a=0}^{\alpha}\frac{(\alpha+a)!}{a!\,(\alpha)!}\left(\frac{1}{2}\left(1+\sqrt{\frac{B}{\lambda+B}}\right)\right)^a \tag{11}$$

Now we solve for I_2, which is given as follows:

$$I_2 = C\exp\left(\frac{-nK}{2}\right)\sum_{l=0}^{\infty}\frac{(nK)^l\lambda^{\alpha+1}}{2^l l!\Gamma(\alpha+1)}\int_0^{\infty}\gamma^{\alpha}erfc^2\left(\sqrt{B\gamma}\right)\exp(-\lambda\gamma)\mathrm{d}\gamma \quad (12)$$

Using formula [19], Eq. (19)], I_2 becomes:

$$I_2 = C\exp\left(\frac{-nK}{2}\right)\sum_{l=0}^{\infty}\frac{(nK)^l}{l!\,2^l}\left(1-\left(\frac{\frac{4}{\pi}\sum_{a=0}^{\alpha}\frac{1}{2a+1}\left(\frac{\lambda}{B}\right)^a}{\times\,{}_2F_1\left(\frac{1}{2}+a,1+a;\frac{3}{2}+a;-1-\frac{\lambda}{B}\right)}\right)\right) \quad (13)$$

where ${}_2F_1(\cdot,\cdot;\cdot;\cdot)$ is the Gaussian hypergeometric function. The final ASEP is obtained by performing operation $I_1 + I_2$ as:

$$P_e = \xi\sum_{l=0}^{\infty}\frac{(nK)^l}{2^{l-1}l!}\left\{\begin{array}{l}A\left[\frac{1}{2}\left(1-\sqrt{\frac{B}{\lambda+B}}\right)\right]^{\alpha+1}\sum_{a=0}^{\alpha}\frac{(\alpha+a)!}{a!\Gamma(\alpha+1)}\left[\frac{1}{2}\left(1+\sqrt{\frac{B}{\lambda+B}}\right)\right]^a \\ +\frac{C}{2}\left[1-\frac{4}{\pi}\sum_{a=0}^{\alpha}\frac{1}{2a+1}\left(\frac{\lambda}{B}\right)^a{}_2F_1\left(\frac{1}{2}+a,1+a;\frac{3}{2}+a;-1-\frac{\lambda}{B}\right)\right]\end{array}\right\} \quad (14)$$

where $\xi = \exp\left(\frac{-nK}{2}\right)$.

The ASEP for QPSK can be obtained by substituting $M = 4$ in the expression of MQAM [21]. The ASER of MSK and QPSK is same [22].

3.2 The ASEP of Non-Coherent Modulations

The modulation schemes with non-coherent detection include DPSK, MFSK, etc. In order to obtain the ASEP, we substitute Eqs. (6) and (8) in (4) to obtain the ASEP as follows:

$$P_e = \exp\left(\frac{-nK}{2}\right)\sum_{l=0}^{\infty}\frac{A\lambda^{l+\frac{n}{2}}(nK)^l}{2^l l!\Gamma\left(l+\frac{n}{2}\right)}\int_0^{\infty}\gamma^{l+\frac{n}{2}-1}\exp(-\gamma(\lambda+B))\mathrm{d}\gamma, \quad (15)$$

Equation (15) can be solved using the identity in [15]; the ASEP is then reduced to

$$P_e = A\exp\left(\frac{-nK}{2}\right)\sum_{l=0}^{\infty}\frac{\lambda^{l+\frac{n}{2}}(nK)^l}{2^l l!(\lambda+B)^{l+\frac{n}{2}}}, \quad (16)$$

Now, using (3) in (16), we obtain ASEP as follows:

$$P_e = A \exp\left(\frac{-Kn}{2}\right) \sum_{l=0}^{\infty} \frac{(\mu)^{l+\frac{n}{2}} (nK)^l}{2^l l! (\mu + \overline{\gamma} B)^{l+\frac{n}{2}}} \tag{17}$$

where $\mu = \exp\left(-\frac{Kn}{2}\right) \frac{n}{2} {}_1F_1\left(1 + \frac{n}{2}, \frac{n}{2}; \frac{Kn}{2}\right)$.

The equation in (17) provided the exact ASEP for DPSK and MFSK modulation schemes over the generalized Rician fading channel. The average bit error probability (BEP) of BFSK can be obtained by substituting $M = 2$ in the ASEP of MFSK.

3.3 The ASEP of M-Ary Modulations

The modulation schemes that fall under this category are MPSK and MDPSK. The ASEP is obtained by putting Eqs. (7) and (8) in Eq. (4), which is given as [12]:

$$P_e = A\,\xi \sum_{l=0}^{\infty} \frac{\lambda^{l+\frac{n}{2}} (nK)^l}{2^l l! \Gamma\left(l + \frac{n}{2}\right)} \int_0^{\pi - \frac{\pi}{M}} \int_0^{\infty} \gamma^{l+\frac{n}{2}-1} \exp(-\gamma(\lambda + B)) \mathrm{d}\gamma \mathrm{d}\theta \tag{18}$$

Equation (18) can be solved by applying the identity [15]; the ASEP then becomes:

$$P_e = A \exp\left(-\frac{nK}{2}\right) \sum_{l=0}^{\infty} \frac{(nK)^l}{2^l l!} \int_0^{\pi - \frac{\pi}{M}} \left(1 + \frac{B}{\lambda}\right)^{-\left(l+\frac{n}{2}\right)} \mathrm{d}\theta. \tag{19}$$

The final expression obtained in Eq. (19) can be easily evaluated using software MATHEMATICA, MATLAB.

4 Analytical Results and Discussion

Numerical results are obtained from the analytical results for different values of parameters K and n. The derived results of ASEP for BPSK, MQAM ($M = 16$), and QPSK are plotted with respect to average SNR in Fig. 1. It depicts that the error performance reduces on increasing the parameter n. Thus, the performance of average BEP improves with an increase in the value of n because of the increase in the degrees of freedom of the non-central Chi-square distribution.

The ASER performance of DPSK, MFSK ($M = 4$), and BFSK is analyzed in Fig. 2 and for MDPSK ($M = 4$) and MPSK ($M = 16$) in Fig. 3. The improvement in the ASEP performance is observed in the above two cases, as compared to the first case.

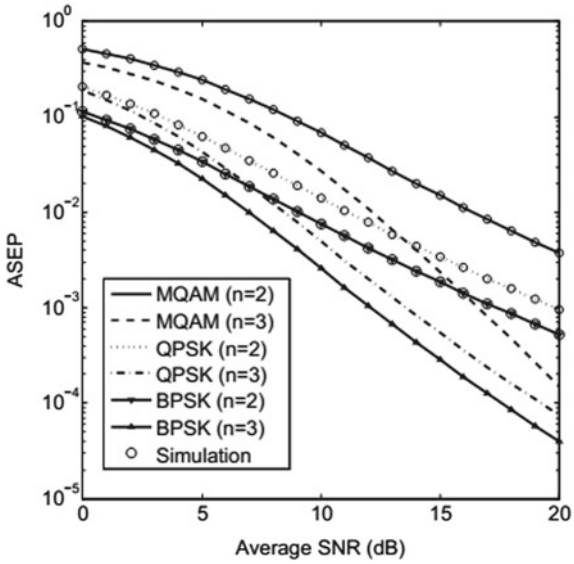

Fig. 1 Exact ASER and simulation of BPSK, MQAM with $M = 16$, and QPSK over a generalized Rician fading channel with $K = 3$ and different values of n

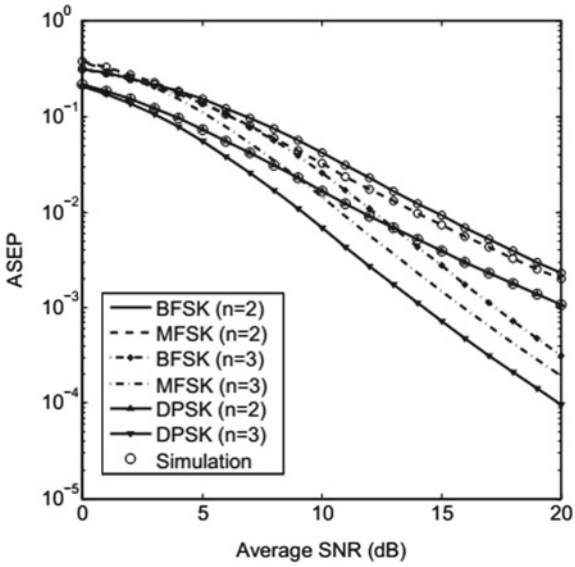

Fig. 2 Exact ASER and simulation of DPSK, MFSK with $M = 4$, and BFSK with $K = 3$ and different values of n

Another method of examining ASEP performance is by varying K and keeping the 'n' constant. The graphs of ASER expressions of BPSK, MQAM ($M = 16$), and QPSK are drawn versus the average SNR by keeping 'n' constant in Fig. 4. Figure illustrates that increase in parameter K decreases the ASEP because an increase in K increases the power of the specular component, thereby increasing SNR and hence

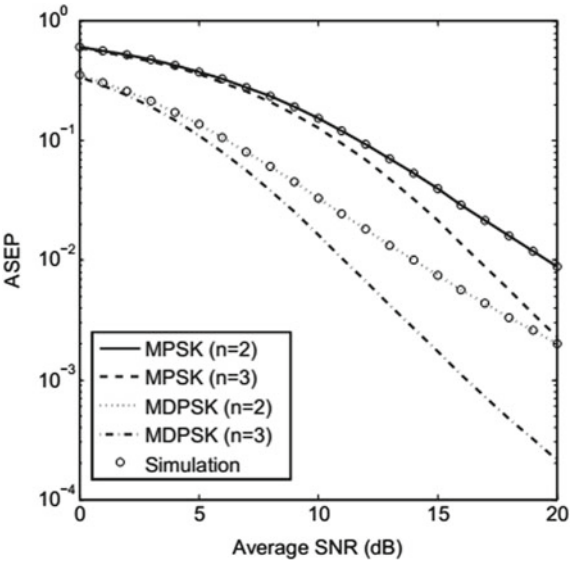

Fig. 3 ASER of MDPSK with $M = 4$ and MPSK with $M = 16$ with $K = 3$ and n

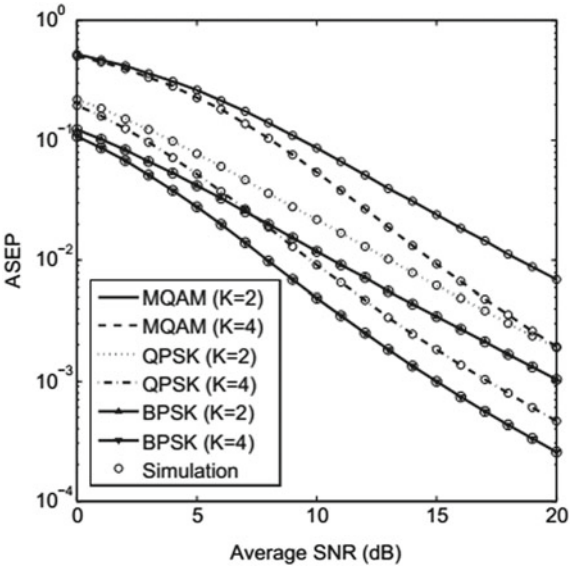

Fig. 4 Exact ASER and simulation of BPSK, MQAM with $M = 16$, and QPSK with $n = 2$ and K

reducing the ASEP. The most severe fading is when $K = 0$ dB, which represents the Rayleigh fading environment in which there is no LOS component.

In Fig. 5, the analytical ASEP results for DPSK, MFSK ($M = 4$), and BPSK are plotted in against the average SNR. Here, the ASEP also decreases as K increases. Similar results are observed for MDPSK ($M = 4$) and MPSK ($M = 16$) in Fig. 6. The

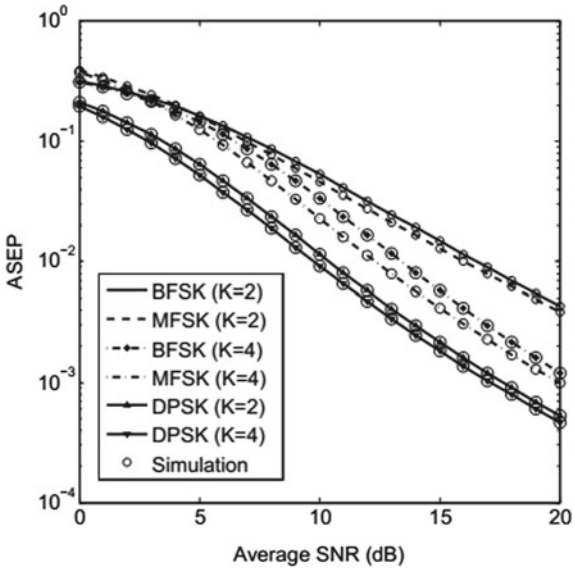

Fig. 5 ASER of DPSK, MFSK with $M = 4$, and BFSK different values of K, $n = 2$

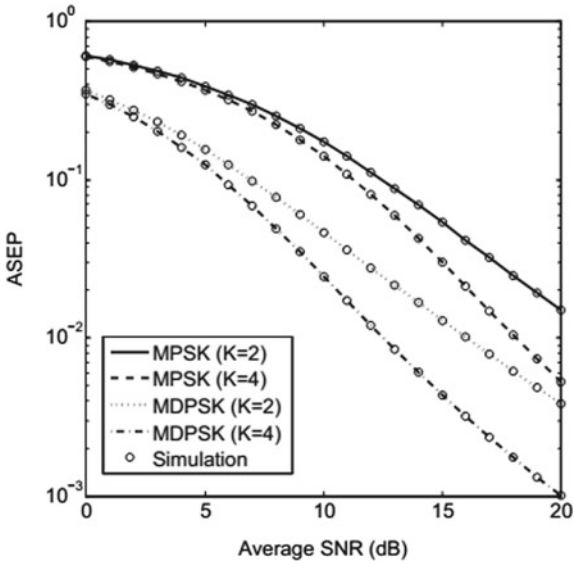

Fig. 6 Exact ASER of MDPSK with $M = 4$ and MPSK with $M = 16$ with $n = 2$ and K

MATLAB simulations of the results are also shown in the figures. The simulation results are in accordance with the numerical results.

5 Conclusion

In this work, we analyzed the performance of different modulations over a generalized Rician fading channel. We divided the modulation schemes into three different groups and performed a generalized ASEP analysis covering all the modulation schemes. Exact closed-form solutions for ASEP are derived and compared with the simulation results. We observed that, for the constant value of K, probability of error reduces as n increases and for constant n, the ASEP decreases, as K increases. The MATLAB simulation results justify the analytically derived results.

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Implementation of an Efficient Handover Algorithm on AP Using Software-Defined Wi-Fi Systems

Shruti Sujan Munde and Vinodkumar Jadhav

1 Introduction

With the increasing number of mobile users, the demand for quality services is increasing; the continuous growth in network traffic has resulted in large deployment of wireless local area networks. When a user is moving from one place to another, a frequent handover of the mobile terminal between the Wi-Fi access points has to be performed to provide uninterrupted good quality, data services to the user. A mobile terminal connects to the Internet using wireless technologies such as cellular network and IEEE 802.11 WLANs. The wireless products being vendor dependent face the inter-operability problems. SDN is the solution to this problem. It is the booming technology that has totally changed the idea of WLAN infrastructure. It has overcome the limitations of the traditional networks.

The basic idea of SDN technology is to decouple its brain that is the control plane from the forwarding plane (data plane). Control planes of all the devices in a network are logically placed together and are referred as SDN controller. The SDN controller thus gets the whole view of the network. It is placed at the middle layer of the SDN architecture out of the three layers, data plane is the lowest layer, and application layer is the upper layer. The OpenFlow protocol is used by SDN to carry the communication between the layers. The controller communicates with application layer via south bound interface (SBI) and with data plane via northbound interface (NBI). In this paper, we are using SDN technology along with WLAN technology. The SDN properties such as vendor independency, centralized control and programmability help us to get the overall view, information about the network devices present in WLAN even network control and management becomes easy.

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A heavily loaded network out-turns into low end throughput; therefore, the AP load must also be considered along with the other factors during the handover process. If a mobile terminal is put on to make a handover when it is in the overlapping area of two APs, switching of mobile terminal with heavily loaded AP will, however, degrade the quality of service provided to the user. Hence, in this paper we have proposed a handover algorithm which considers an AP load, and this algorithm is compared with the SDN-based RSSI handover mechanism. The paper is further divided into different sections accordingly; related work is explained in Sect. 2. Section 3 gives the idea about network architecture with detailed information about handover mechanisms. Section 4 gives experimentation details along with results and analysis. Section 5 concludes the paper.

2 Related Work

The software-defined wireless network is one of the emerging technology approaches that help to overcome the limitations of WLANs. The SDWN is proposed cost effective solution [1] in order to fulfill the demand of dynamic services needed by wireless networks. Motivation to research and work on SDN are [2] many some of them are (i) simplified network configuration and management (ii) evolvable networks and (iii) vendor independency.

In SDN control plane is decoupled from data plane, and data plane forwards the packets according to the logic provided by control plane [2]. Open flow is one of the popular protocols used in SDN [3], and it uses open source codes to control SDN controllers and switches. Controller in SDN is software that manages the collection of switches for traffic control. Communication in SDN takes place via NBI and SBI; the entire SDN communication is explained in [4]. There are very few network emulators available for experimenting with SDN and OpenFlow protocols, for example, NS-3 and OMNET++ [4]. But mininet-wifi is the only emulator allowing us to work with software-defined wireless networks.

In traditional networks, when the handover takes place, there is an interruption in data transmission; hence, many authors tried to add another interface so as to keep the transmission continuous [5, 6]. But the market available access points usually have only one interface, which limits this approach.

In traditional networks, delay happens due to two reasons; first is that the client station is accountable for deciding when to initiate the handover, which occurs during the detection phase [7]. But, this phase is not standardized as each equipment vendor is in charge to implement it [8]. Mobile terminals perform handoff when one of the two thresholds is reached, either poor signal strength or because of many lost frames [8]. And in traditional network the devices programmability is vendor dependent, different thresholds are decided by different vendors. Hence, there is no standardized time for AP detection and hence the detection delay varies [9]. After that during discovery phase the mobile terminal tries to search for new AP to connect, it has to

send the probe request to all the available APs and then wait for probe response from them. Hence, this time considerably depends on the traffic load on APs [10].

The existing networks consider the RSSI (received signal strength indicator) value in order to perform the handover [11]. The RSSI-based handover strategy is easy to implement; however, it does not guarantee good QoS [12]. This paper proves that a handover of the terminal from overloaded AP to underloaded AP results is improvement in throughput with low latency. Handover method by combining SDN with traditional RSSI mechanism is proposed in [13] which is called as Dispatch.

3 System Model

Software-defined wireless network (SDWN) is use of SDN features in wireless networks. Using SDN controller, SDWN helps in the formation of new techniques according to user demands, such as security, quality of service (QoS), mobility and handoff. The architecture of SDWN is shown in Fig. 1. The infrastructure layer consists of access points and OpenFlow-enabled switches. APs and OpenFlow switches both are totally responsible for information forwarding only, while the logic management units of them are attached to the controller. The controller has the sight of complete network and has information about each flow in the network. The components of the architecture are as follows:

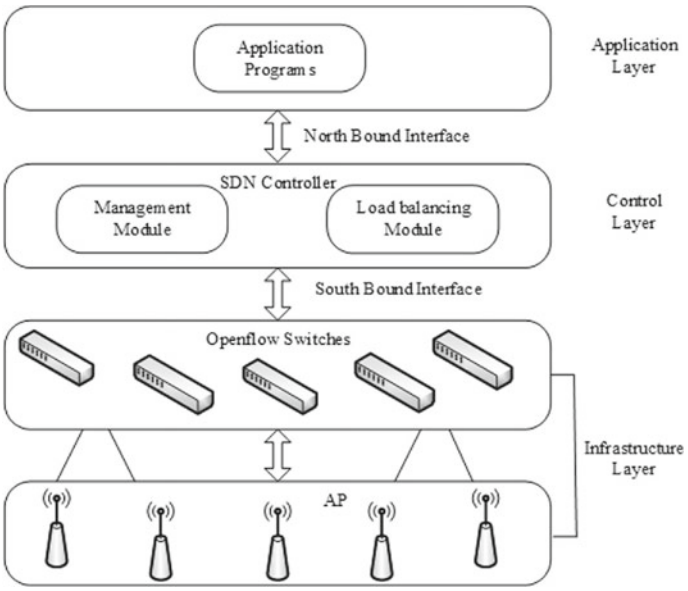

Fig. 1 Proposed SDWN architecture

- **Access point (APs)**
  The APs in this design are solely responsible for the information forwarding function, while the logic management functions are coupled with the controller. This OpenFlow protocol will not totally take into account the distinctiveness of a network and the controller cannot administer the APs. Hence, a distinct communication channel between the controller and every AP is set up from which the controller collects the status details of all APs, thereby executing control over the APs.
- **Controller**
  Controller being a unified and central logic control unit, it is accountable for the gathering of status of forwarding devices particulars, for the administration of APs OpenFlow switches, and for the flow table deliverance. It jointly provides a programmable interface that is suitable to write down applications for users by keeping into account their individual requirements.
- **Switch**
  Resembling to an AP, the OpenFlow switch has its control functions coupled with the controller and thus keep hold only on the data forwarding function along with it. Hence, this switch acts in a similar way as a pure data channel.

3.1 Handover Methods

Handover is the process of disassociating a mobile terminal from one channel and associating it to other channel in the network. Handover management allows a wireless network to maintain a mobile terminals connection to services when it is moving in the network. In this paper, two SDN-based mobile terminal handover methods have been performed; they are as follows:

SDN based RSSI handover mechanism:

(1) Pre-association and pre-authentication: This is the process in which mobile terminals link AP out of its range by use of out-of-band signaling; the existing association to the control server enables them to exchange links and authenticate messages. This allows terminals to link with all APs of limited geographical area prior to the station's arrival in that area.

(2) Scanning: The mobile terminals include the handover manager that consists of the scanning and scheduler module. It decides about when to perform the handover. To discover surrounding APs the terminal broadcasts the probe request messages to all APs and listens to the response. APs on the particular channel then reply to the mobile terminal requests. The check for new APs has to be done regularly enough to find new APs fast enough. Too frequently scanning will, however, result in a decrease in throughput and QoS, as no data can be transmitted during scanning. Min_Channel_Time and the Max_Channel_Time are the maximum and minimum times the station should wait on a channel, before rescanning.

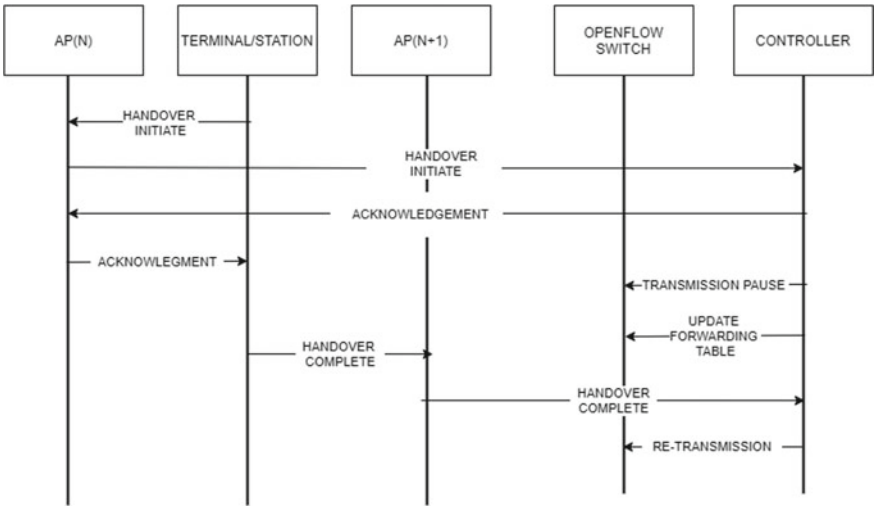

Fig. 2 SDN-based RSSI handover mechanism

(3) Handover process: Based on results obtained from scanning the handover takes place, the scheduler initiates a transfer only when the (RSSI) signal strength indicator of any AP is stronger than the RSSI of the existing AP. Transmission buffer of the station is put in a blocked state. Subsequently, the station sends a "Handover Initiate" message to its associated AP which sends the message to the controller. The controller then responds to the station with an (ACK) acknowledgement response, sends a pause message to the switch, and updates the switch forwarding table using the OpenFlow protocol to transfer future downstream packets of data through AP2 and forward upstream incoming traffic from the station through AP2 to the streaming service. The process is explained in Fig. 2.

SDN-based AP load balancing handover mechanism:

The above-explained handover mechanism provides a good quality of service (QoS) compared to the traditional network IEEE 802.11 handover mechanism. As the controller has the entire network view, it in advance gets the information of all the mobile terminals in the network through southbound interface using OpenFlow protocol. Hence, there is no need of scanning and authentication process as in traditional handover process. This helps in reducing the discovery and association delay. However, if the AP is heavily loaded, the bandwidth allocation and the quality of service provided to the terminal degrade. Hence, the load of the AP should also be considered so as to provide the good quality of service to all the mobile terminals.

In this SDN-based AP load balancing handover mechanism, the information about the load on particular AP is gathered and sent to the controller via southbound interface. The controller has the information about all the flow in the network and has

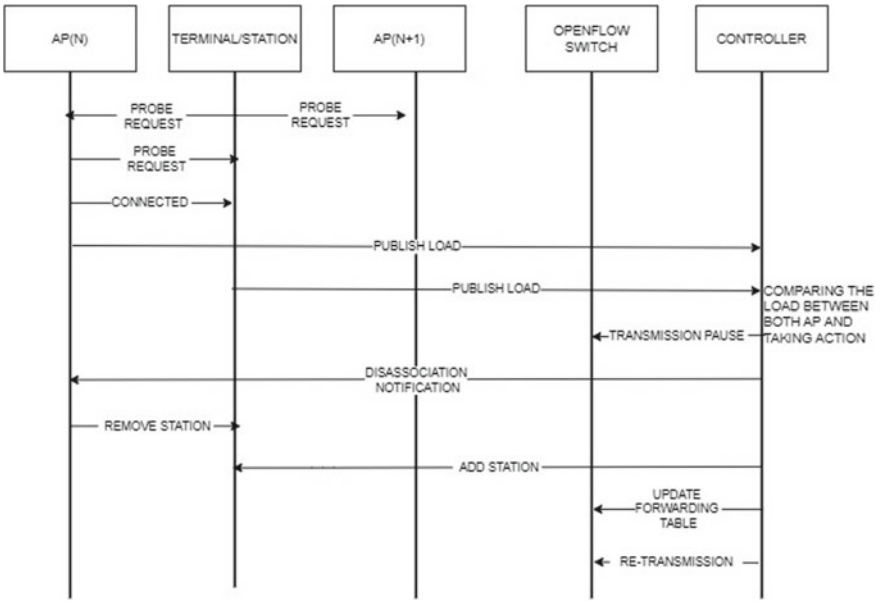

Fig. 3 SDN-based AP load balancing handover mechanism

the global view of the network. Whenever the mobile terminal enters the overlapping area of the two APs, it gets request from both the APs for connection; however, the handover process is performed depending on the load present on each AP. In this mechanism, irrespective of the RSSI value the handover in overlapping area takes place only if the load on the other AP is less than that of the AP to which the mobile terminal is currently connected, or else the terminal remains connected to same AP. The flowchart of SDN-based AP load balancing handover mechanism is shown in Fig. 3, and the algorithm is as given below:

SDN-based AP load balancing handover algorithm:

1. Controller gathers information about load on AP via southbound interface.
2. When the terminal starts moving to the overlapping region, controller compares the load present on both APs
3. **if** APLoad (current AP) < 1 + APload (reference AP)

   Reference AP over loaded
   Deny new terminal

   No handover performed.

4. **else if** APLoad (current AP) > 1 + APload (reference AP):

   Reference AP under loaded.

   Send message of disassociation to current AP

To disconnect it
Transfer terminal to new AP

5. **Else:**

No handoff

4 Experiment, Results and Analysis

To perform the experiments, a network emulator named mininet-wifi is used. Being an extended version of mininet, it supports Wi-Fi technology and adds functionality of virtualized Wi-Fi stations and access points. It is a Linux based with an ability to build a broad variety of network topologies with virtual hosts, switches and links. It has an inbuilt support for OpenFlow switches and so is widely used for experiments with software-defined network (SDN), providing reliable and consistent reports.

Case scenario 1:

This experimental setup consists of two APs which are OpenFlow-enabled and six mobile terminals which are associated with those APs, as shown in Fig. 4. All six stations are at static positions, initially only 1 station that is STA2 is associated with AP1, while all other five stations—STA1, STA3, STA4, STA5, and STA6—are associated with AP2. This makes AP2 overloaded. while AP1 is under loaded.

The aim of this experiment is to show the association of the station to one of the AP, when it is in the overlapping area of two APs. Association of the station to AP in the overlapping regions depends upon the handover mechanism used STA3 is moved from its initial position to the overlapping region using the "py sta3.setPosition" as

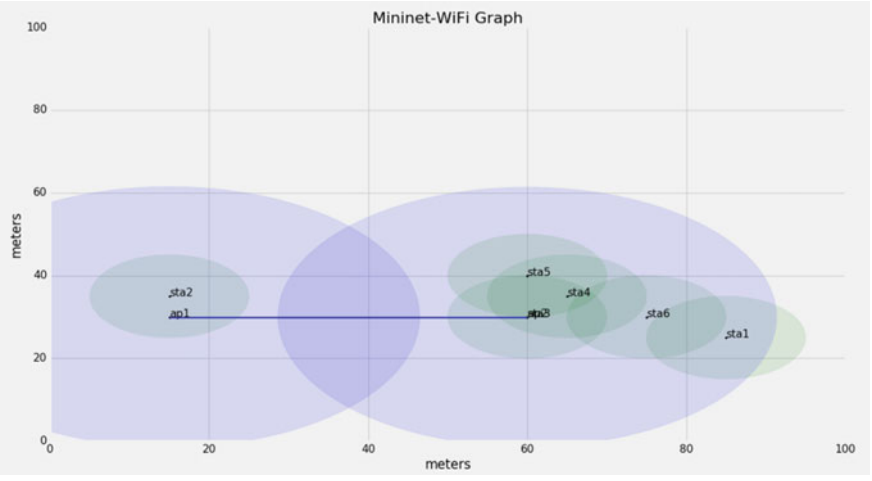

Fig. 4 Experimental scenario

shown in Fig. 5. When the handover mechanism used in the experimental setup is "SDN-based RSSI handover mechanism," STA3 remains associated with AP2, as the signal strength received from AP2 is strong than that of AP1. Figure 6 shows the association of STA3 after changing its position, command "sta3 iwconfig" is used to get the information about the connection of the station, and it shows that sta3-wlan0 is currently associated with AP2.

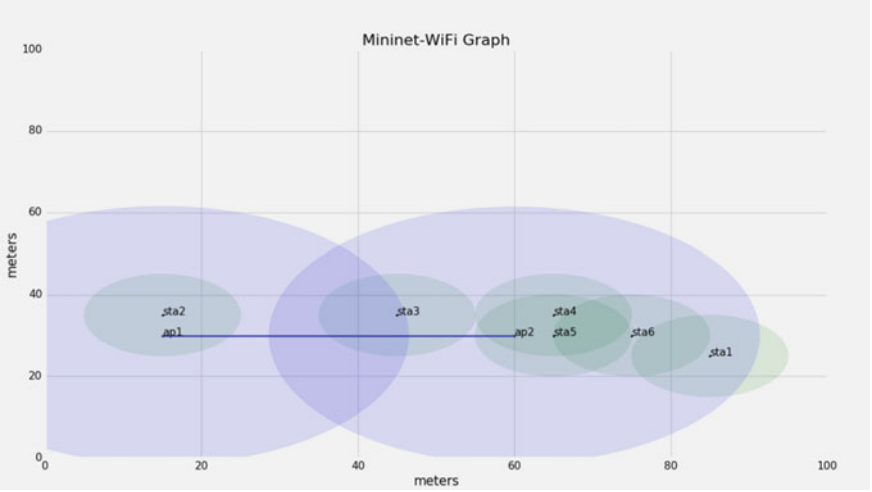

Fig. 5 Changed position of STA3

```
root@DELL: /home/dell/mininet-wifi/examples
*** Killing mac80211_hwsim
root@DELL:/home/dell/mininet-wifi/examples# python final1.py
*** Creating nodes
*** Configuring wifi nodes
*** Creating links
*** Starting network
*** Running CLI
*** Starting CLI:
mininet-wifi> py sta3.setPosition("42,35,0")
mininet-wifi> sta3 iwconfig
lo        no wireless extensions.

sta3-wlan0  IEEE 802.11  ESSID:"ssid-ap2"
          Mode:Managed  Frequency:2.437 GHz  Access Point: 02:00:00:00:07:00
          Bit Rate:1 Mb/s   Tx-Power=1 dBm
          Retry short limit:7   RTS thr:off   Fragment thr:off
          Encryption key:off
          Power Management:off
          Link Quality=70/70  Signal level=-36 dBm
          Rx invalid nwid:0  Rx invalid crypt:0  Rx invalid frag:0
          Tx excessive retries:0  Invalid misc:0   Missed beacon:0
```

Fig. 6 Association of STA3

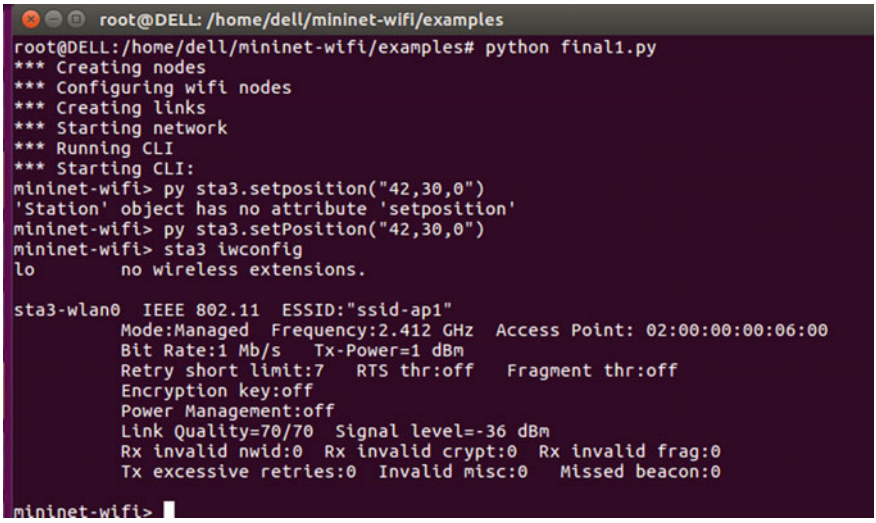

Fig. 7 Association of STA3

In other case, when "SDN based AP load balancing handover mechanism" is used, STA3 gets associated with AP1. Hence, even if sta3 is at same position as in Fig. 5, but because of AP load balancing mechanism used in this case, the station gets associated with AP1. Figure 7 shows the association of STA3 to AP1.

Case scenario 2:

The experimental setup is shown in Fig. 4; it consists of two APs which are OpenFlow-enabled and six mobile terminals which are associated with those APs, as shown in figure. All six stations are at static positions, initially only 1 station that is STA2 is associated with AP1, while all other five stations—STA1, STA3, STA4, STA5, and STA6—are associated with AP2. This makes AP2 overloaded, while AP1 is overloaded.

In this experiment, out of six stations five stations STA1, STA2, STA3, STA4, and STA6 are kept at fixed position, while the STA5 is made to move from AP2 to AP21. The starting and ending points of station STA5 are set, and even the mobility time is set.

(a) TCP THROUHPUT:

A TCP connection is set in between station SAT2 and station STA5, the "iperf –s –p 5566 –t 50 -i 1" command is run at server station, and "iperf –c 10.0.0.2 –p 5566 –t 50" is run at the client station. The traffic is measured using the iperf command. To calculate the delay a ping was made from STA5 to STA2 using command "ping 10.0.0.2." the delay produced in the scenario results in the packet loss. The same procedure was followed in both handover mechanisms. As shown in Fig. 8, the total bandwidth allocated using SDN-based RSSI mechanism is 7.59 MBits/sec, while

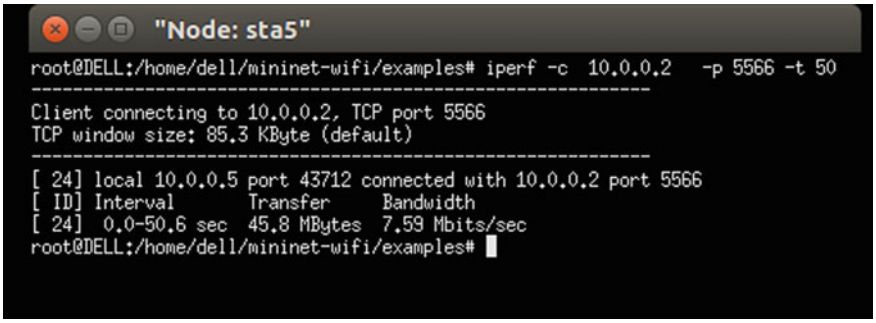

Fig. 8 TCP connection report for SDN-RSSI mechanism

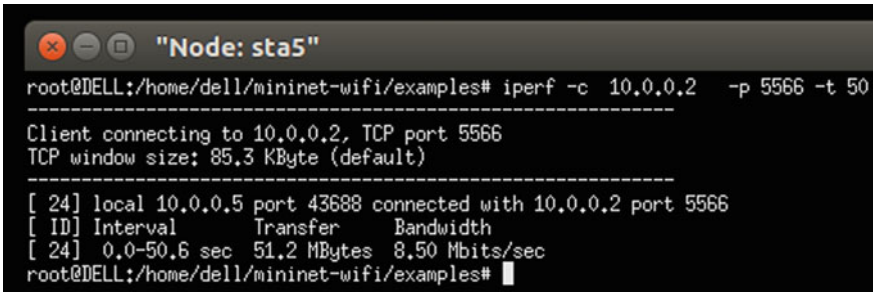

Fig. 9 TCP connection report for SDN-AP load mechanism

SDN-based AP load balancing mechanism provides 8.50 MBits/s which can be seen in Fig. 9.

Figure 10 shows the comparison between TCP throughput between both techniques. As the delay produced in the 2nd mechanism is less, the packet loss is also less in AP load balancing mechanism than that of RSSI mechanism.

(b) UDP THROUHPUT:

In this experiment, a UDP connection is set in between station SAT2 and station STA5, STA2 acts as server, while STA 5 acts client. Again the traffic is measured using iperf command. Figures 11 and 12 show that bandwidth allocated is same in both methods; however, the jitter produced in AP load balancing mechanism is '0.016 ms' which is less than that of RSSI mechanism. Figure 12 shows the comparison between UDP throughputs of both techniques.

Performance metrics table (Table 1) compares both the handover mechanism; the table shows that the results obtained from AP load balancing handover mechanism when the terminal is moving from an overloaded AP to under loaded are better than RSSI handover mechanism (Fig. 13).

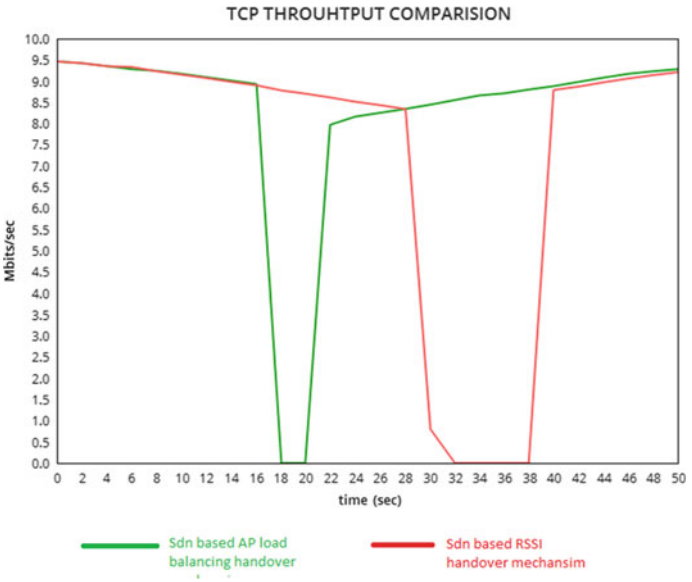

Fig. 10 TCP throughput comparison between handover mechanisms

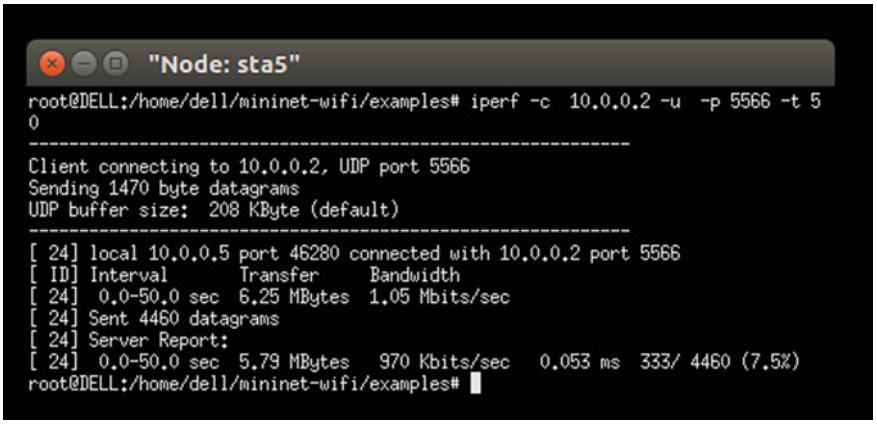

Fig. 11 TCP connection report for SDN-RSSI mechanism

5 Conclusion

Two different SDN-based handover mechanisms are proposed and tested in the paper, the required experiment setup is built and tested in the mininet-wifi network emulator, comparison between the SDN-based RSSI handover mechanism and SDN-based AP handover mechanism is made, and analysis is done on different factors—transfer, bandwidth, jitter and packet loss.

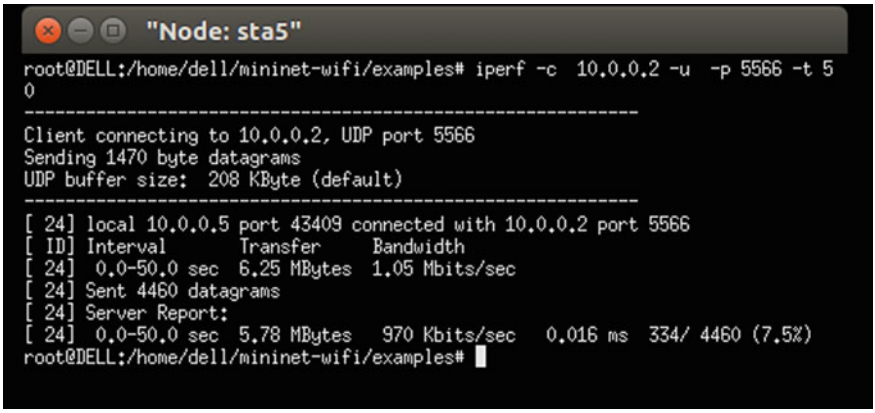

Fig. 12 TCP connection report for SDN-AP load mechanism

Table 1 Performance metrics table

Metric	SDN based RSSI mechanism handover	SDN based AP load balancing mechanism handover
Transfer	1. TCP connection = 45.8 Mbytes 2. UDP connection = 5.79 Mbytes	1. TCP connection = 51.2 Mbytes 2. UDP connection = 5.78 Mbytes
Bandwidth	1. TCP connection = 7.59 Mb/s 2. UDP connection = 970 kb/s	1. TCP connection = 8.50 Mb/s 2. UDP connection = 970 kb/s
Jitter	0.053 ms	0.016 ms
Packet loss	14%	6%

In SDN-based RSSI handover mechanism, the station is associated with AP that provides the strongest signal compared to other AP and hence can result in getting low Quos when AP is overloaded. SDN-based AP handover mechanism tries to balance the load when AP is in overlapping region, thus ensuring good QoS to all stations.

From obtained results, we can say that SDN-based AP handover mechanism gives better result than SDN-based RSSI handover mechanism in terms of transfer, bandwidth, jitter and packet loss.

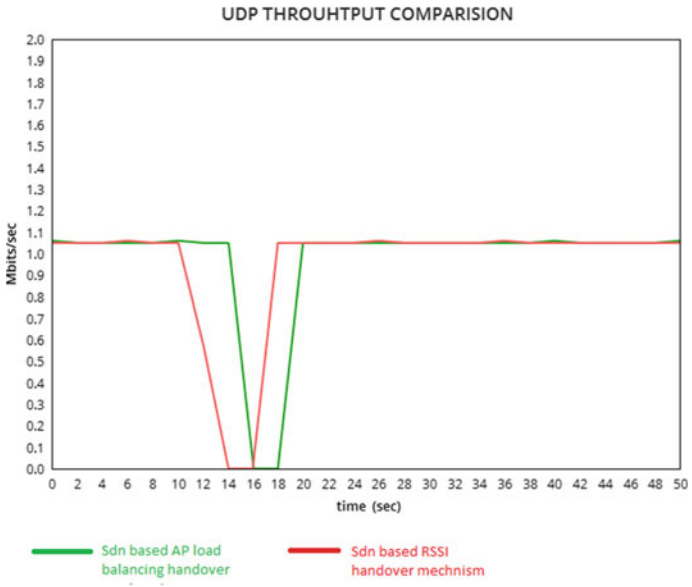

Fig. 13 UDP throughput comparison between handover mechanisms

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A Novel Technique for the Design and Implementation of a 4 × 2 All Optical Encoder Using Micro-ring Resonator Switching Mechanism

Rakesh Choudhary, Sushanta Mahanty, and Ajay Kumar

1 Introduction

Optical waveguides and switching devices are the essential elements for the processing of signals in the optical domain. An all-optical communication system requires sending, processing, and receiving the signal in the optical domain only. It means, to make all-optical systems, the entire components that are used in the optical networks should be optical elements. The reason behind focusing more on optical communication technology is that it provides wider transmission capacity and longer transmission distance. All-optical signal processing has several other advantages also, e.g., parallel processing/computing, immunity to electromagnetic interference, very fewer transmission losses, compact design, and wider bandwidth. Several studies indicate that a large number of researchers are taking interest in the area of ultra-fast optical communication systems and also obtained very significant results. Optical logic gates play a very vital role in numerous optical signal processing operations like switching, decision-making, addressing, regeneration, multiplexing/demultiplexing, coding/decoding, and simple/complex computing. The concept of linear electro-optic effect which is also known as the 'Pockels effect' has been successfully employed by several researchers to design various optical combinational and sequential functionalities. According to the 'Pockels effect,' the refractive index of a material varies directly with the applied electric field across that material. Some common examples of materials that exhibit 'Pockels effect' are lithium niobate ($LiNbO_3$) and gallium arsenide (GaAs). One of the optical devices constructed using lithium niobate substrate is Mach–Zehnder Interferometer (MZI) and it can work as a powerful optical switch by employing the concept of electro-optic effect.

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Further, various digital logic circuits either combinational or sequential can be implemented in the optical domain by properly cascading the required numbers of MZIs. An efficient method to achieve electro-optic switching using Mach–Zehnder interferometer and optical implementation of some digital logic gates using MZI has been explained in [1]. One excellent utilization of the Mach–Zehnder interferometer for constructing a 1×4 optical signal router is given in [2]. The semiconductor optical amplifier (SOA)-based MZI structure for the design and analysis of ultrafast all-optical XOR gate is explained in detail [3–5]. The detailed study and experimental implementation of Mach–Zehnder-based AND, Exclusive-OR/Exclusive-NOR logic gates [6], full adder & full subtractor [7], gray code converter and parity checker (even) [8], optical decoder circuit [9], and 4×2 optical encoder circuits [10] are very nicely explained. Another emerging technology in the area of ultrafast optical signal processing is photonic crystals. Photonic crystal devices consume very little power and at the same time, their operating speed is very high. These devices are getting much attention because of its low loss structure. An efficient technique to design OR and XOR gate using 2D photonic crystal reported in [11]. A new scheme to demonstrate a photonic crystal ring resonator-based optical encoder switch is explained in [12]. Another example of a 2D photonic crystal-based all-optical 4×2 encoder is nicely represented in [13]. The method to analyze photonic crystal ring resonator (hexagonal shaped) based on the all-optical encoder is described in [14]. Another concept which is playing a very important role in optical switching is micro-ring resonator (MRR). The switching mechanism of MRR and its utilization in designing the various logical functions is demonstrated in [15]. The concept of MRR-based switching action is efficiently used to design both combinational and sequential types of digital logic devices that are represented in [16–24]. In this article, initially, we have explained the efficient switching capability of micro-ring resonator (MRR) and then designed a novel 4×2 all-optical encoder based on this switching mechanism. Section 1 of this article explains about the relevant technical background and previous research works which has already been done related to our proposed design. Sect. 2 of the paper describes the theoretical part of micro-ring resonator (MRR) and how it can be implemented as an optical switch with detailed mathematical equations. Section 3 of the paper is a very important part of our research. Here, we explained about a new layout diagram of 4×2 optical encoder using cascaded arrangements of five similar types of ring resonators. After that the working principle of the proposed layout structure is theoretically explained and then this novel structure is experimentally verified by the MATLAB simulation software. Finally, in Sect. 4, we concluded our research work. In this way, we proved that the proposed design can be used as an all-optical 4×2 optical encoder using the switching phenomena of the micro-ring resonator. This article will be very useful for all the people exploring and doing research work in the domain of all-optical ultra-fast communication.

2 Basic Principle and Switching Mechanism of Micro-ring Resonator (MRR)

The principle underlying the optical ring resonators are the same as that of whispering galleries but unlike whispering galleries, ring resonators use the light signal and comply with the characteristics of light like total internal reflection and constructive interference. Micro-ring resonators (MRR) are a set of waveguides where minimum one is coupled in closed-loop to some light input and output. If the light signal from the input waveguide, having a resonant wavelength, travels through the loop then due to the property of constructive interference, it builds up in intensity over multiple round-trips which will appear at the output waveguide. The layout diagram of a micro-ring resonator is shown in Fig. 1.

In the MRR structure, the coupling between the ring and the input waveguide is always unidirectional. We can observe from the above figure that a total of three waveguides (two straight waveguides and one ring) has been used to construct the ring resonator diagram. The coupling coefficients between top waveguide & ring are denoted by k_1 and between ring & bottom waveguide is denoted by k_2. The term 'r' is used to represent the radius of the ring. When the optical input signal of continuous nature is provided to the input port of MRR then some portion of this signal is transferred to the ring also due to the coupling effect. The constructive interference is being formed and the ring resonator is said to be 'On Resonance' if it satisfies the condition that the total effective path length of the ring will be multiple of the operating wavelength. As a result of this, periodic fringes will appear. The signal which is now rotating in the ring is also transferred to the drop port with a fraction of k_2 due to the coupling effect. Therefore, the drop port of MRR reflects maximum transmission in this condition and the ring exhibits minimum resonance through the

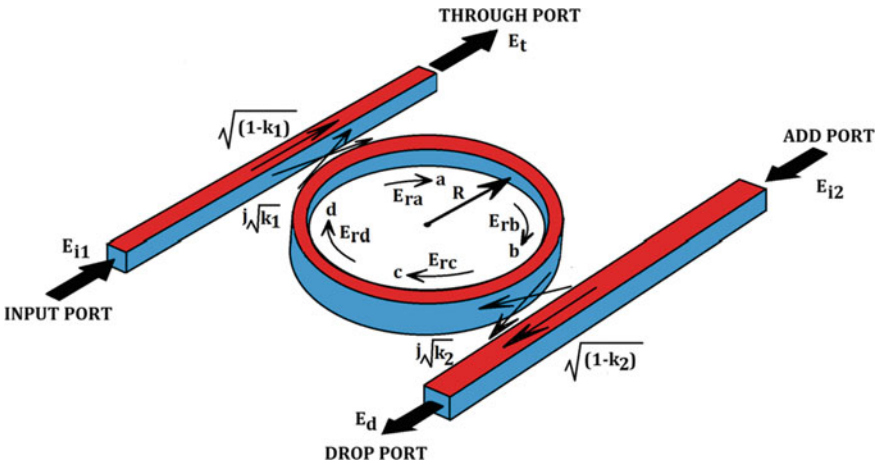


Fig. 1 Layout diagram of a single micro-ring resonator (MRR)

port. We can obtain the excellent optical switching if the MRR is designed using some nonlinear materials like gallium arsenide/aluminum gallium arsenide. Here, an effective refractive index is the function of the intensity of the light signal which is flowing in MRR. When the MRR is excited by applying the optical LASER signal from the top of the ring, carriers of high density will be generated due to the total absorption of the light signal. As a result of this, the refractive index is reduced by a significant amount which in turn leads to blue shift phenomena. Let us further assume the following parameters associated with the ring resonator structure: L denotes the circumference of the ring and it is equal to $2\pi r$, where $2r$ is the diameter of the ring. α denotes the attenuation coefficients of the ring, γ represents the insertion loss and kn denotes the wave propagation constant which is equal to $(2\pi/\lambda)n_{\text{eff}}$ where λ is the resonant wavelength. $n_{\text{eff}} = n_0 + n_2 \cdot I = n_0 + \frac{n_2}{A_{\text{eff}}} P$, where n_0 & n_2 are the linear and nonlinear refractive indexes, I & P are the intensity and power of the optical pump signal. The values of k_1 and k_2 are taken as 0. 25, attenuation coefficient $(\alpha) = 0.$ 0005 micro/meter, effective cross-sectional area $= 0.$ 25 micro/m^2 and the resonator wavelength as $\lambda = 1.$ 55 micro-meters. Again, let E_{i1} and E_{i2} are the field intensities of the input port and add the port of MRR. So, the through port (Et) and drop port (Ed) field intensity as derived in [21] is given as,

$$E_t = \frac{D\sqrt{1-k_1} - D\sqrt{1-k_2}x^2 \exp^2(j\phi)}{1 - \sqrt{1-k_1}\sqrt{1-k_2}x^2 \exp^2(j\phi)} E_{i1} + \frac{-D\sqrt{k_1 k_2}x \exp(j\phi)}{1 - \sqrt{1-k_1}\sqrt{1-k_2}x^2 \exp^2(j\phi)} E_{i2} \tag{1}$$

$$E_d = \frac{-D\sqrt{k_1 k_2}x \exp(j\phi)}{1 - \sqrt{1-k_1}\sqrt{1-k_2}x^2 \exp^2(j\phi)} E_{i1} + \frac{D\sqrt{1-k_1} - D\sqrt{1-k_2}x^2 \exp^2(j\phi)}{1 - \sqrt{1-k_1}\sqrt{1-k_2}x^2 \exp^2(j\phi)} E_{i2} \tag{2}$$

where $D = \sqrt{(1-\gamma)}$, $x = D\exp\left(-\alpha\frac{L}{4}\right)$ and $\phi = \frac{k_n L}{2}$.

We can achieve the switching characteristics of the ring resonator by using the above equations and at the same time, these equations are very important for analyzing the cascaded structure of MRRs. The MATLAB simulation output of a single MRR as shown in Fig. 1 which depicts its switching action is shown in Fig. 2.

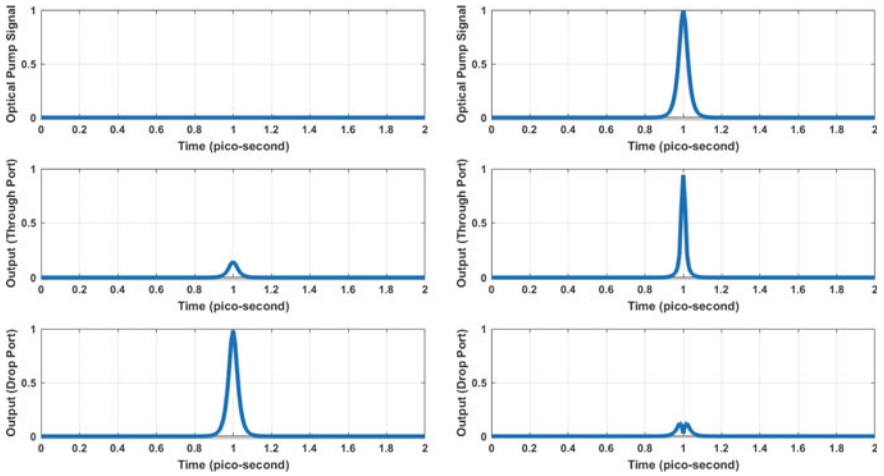


Fig. 2 Output characteristics curve of a micro-ring resonator (MRR) using MATLAB

3 Design of 4 × 2 All Optical Encoder Using Micro-Ring Resonator

3.1 Theory

The implementation of 4 × 2 all-optical encoders using micro-ring resonators is the main objective of our article. In Sect. 2, we have seen how an optical MRR can be used as a switching device. Here, we are using the switching capability of micro-ring resonator for designing the above-mentioned optical encoder. The combinational digital circuit that performs the reverse operation of the decoder is called an encoder. It has a 2*n* number of input lines and n number of output lines. It produces an active high binary code equivalent to the input combination. The enable signal is optional in an encoder, so it is not considered in our design. The block diagram, truth table, and gate-level diagram of a 4 to 2 encoder are shown in Fig. 3a–c.

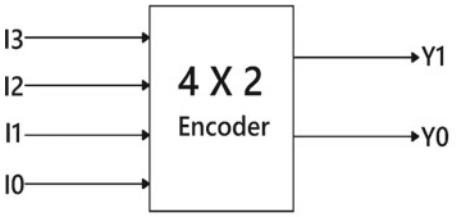
The two outputs Y1 & Y0 of the encoder from Fig. 3b can be expressed as

$$\mathbf{Y}1 = \mathbf{I}2 + \mathbf{I}3$$

$$\mathbf{Y}0 = \mathbf{I}1 + \mathbf{I}3$$

The gate-level implementation of the above logic function is shown in Fig. 3c.

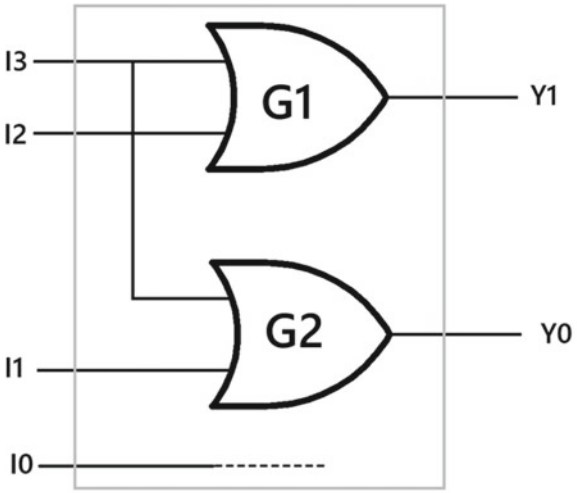
The block diagram of a 4 × 2 all-optical encoder based on cascading ring resonators architecture is shown in Fig. 4. Here, we have used five identical micro-ring resonators, namely MRR1, MRR2, MRR3, MRR4, and MRR5 in cascaded mode. The cascading of all these MRRs has been done in such a way that it will produce two



(a)

INPUT				OUTPUT	
I3	I2	I1	I0	Y1	Y0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

(b)



(c)

Fig. 3 **a** Block diagram of 4 × 2 encoder. **b** Truth table of 4 × 2 encoder. **c** Gate level diagram of 4 × 2 Encoder

optical OR functionalities at the final output through-beam couplers I&II. The first optical OR functionality is obtained by using MRR2 & MRR3 and beam coupler-I, whereas second optical OR functionalities by MRR4 & MRR5 and beam coupler-II. In this diagram, the same control signal is applied to MRR2 & MRR4 for simplicity purposes. Both the OR functionalities are controlled by the MRR1. To excite this optical circuit, an optical signal of continuous nature (E_i) is provided at the input port of MRR1. The control LASER signal for this MRR is I0.

Now from the Boolean expressions of 4 × 2 encoder as described above, it is clear that for its implementation, we need to design two optical OR functionality. This is done through the proper combinations of MRR2 & MRR3 (First optical OR functionality) and MRR4 & MRR5 (Second optical OR functionality). In the first optical OR functionality, drop port output of first MRR acts as an input wave for MRR2, and drop port output of MRR2 acts as input wave for MRR3. These two ring resonators, i.e., MRR2 & MRR3 are controlled by the optical pulse trains **'I3'** and **'I2'**. The through port outputs of MRR2 & MRR3 is then passed through the

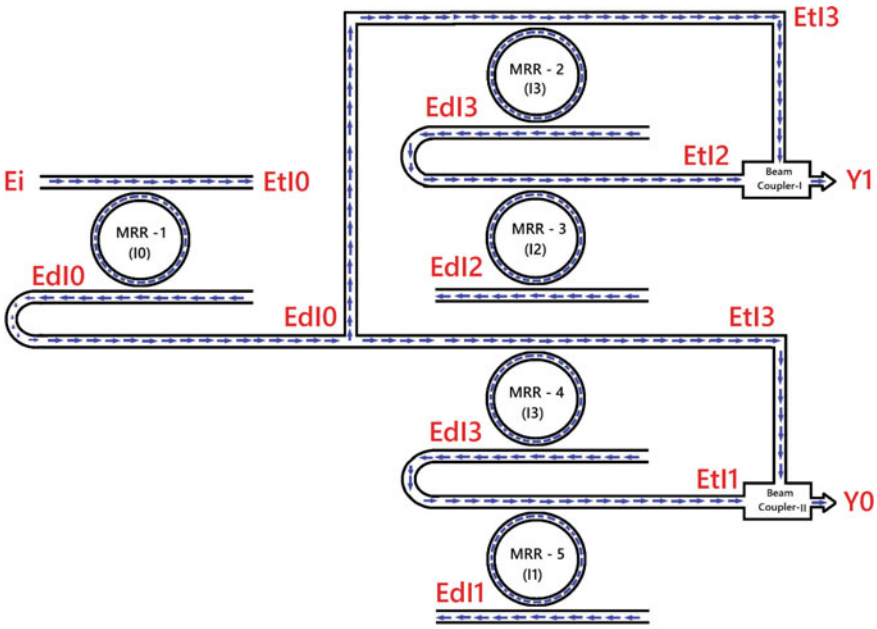


Fig. 4 The layout structure of 4 × 2 all-optical encoder based on micro-ring resonator

beam coupler-I and at the output of this coupler, we will obtain the first optical OR functionality ($\mathbf{Y}1 = \mathbf{I}2 + \mathbf{I}3$). Similarly, for obtaining the second optical OR functionality, MRR4 & MRR5 are used. The same signal EdI0 is also provided as the input wave to MRR4 and its drop port signal will act as the input signal for MRR5. The optical control pump signals **'I3'** and **'I1'** are used to modulate the MRR4 and MRR5, respectively. Finally, the through port outputs of MRR4 & MRR5 are passed through beam coupler-II which in turn produces the second optical OR functionality ($\mathbf{Y}0 = \mathbf{I}1 + \mathbf{I}3$).

3.2 Simulation and Results

In this section, we are going to explain the experimental results of the proposed 4 × 2 all-optical encoder obtained from MATLAB software. These experimental results are shown graphically for convenience. The MATLAB simulation for the proposed design (Fig. 4) is performed by considering the values of parameters and derived mathematical equations of MRR as mentioned in section-II. The detailed description of the principle of operation of 4 × 2 all-optical encoder, by considering all the four possible cases of truth table (Fig. 3b) along with the MATLAB outcomes is given as follows.

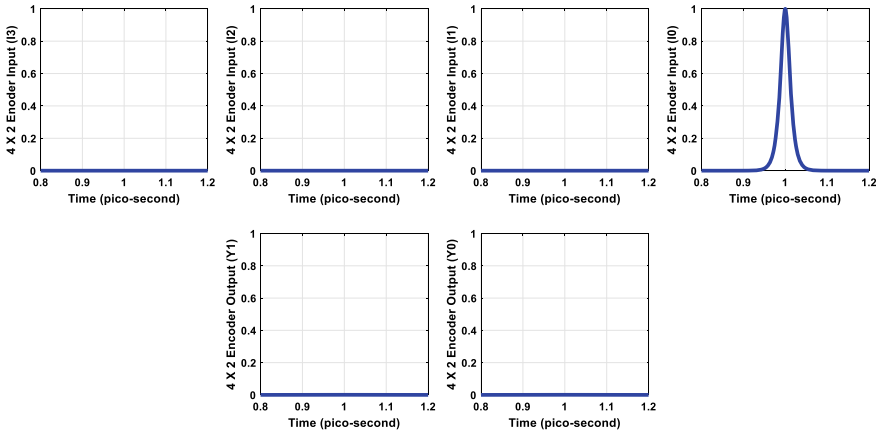


Fig. 5 MATLAB output of the proposed design for input combination (I3 = 0, I2 = 0, I1 = 0, & I0 = 1)

Case 1: When I3 = 0, I2 = 0, I1 = 0, andI I0 = 1

We know that both the outputs of the proposed encoder will be equal to zero for the above-mentioned input combination. This condition can also be verified from Fig. 4 using MATLAB. As the control signal of the first MRR for the above case (I0) = 1 so, the applied input signal will be moved to its through port (EtI0) and its drop port (EdI0) will not have any signal. Since EdI0 is the input signal for the input ports of MRR2 & MRR4, therefore, no signal will be available at their through ports. Again, as the pump signals I3 = 0, I2 = 0 & I1 = 0 therefore the through port outputs of MRR3 & MRR5 will also not have any signal. Hence the outputs of both the beam couplers I & II will be equal to zero (Y1 = 0 & Y0 = 0). The experimental output for the above condition is reflected in Fig. 5 where 1st & 2nd rows represent input & output combinations for case1.

Case 2: When I3 = 0, I2 = 0, I1 = 1, andI I0 = 0

In this case, as control signal of first MRR (I0) = 0, therefore the applied input signal will be observed at its drop port (EdI0) only. From Fig. 4, it can be seen that the signal EdI0 is applied to the input sections of both optical OR functionalities. So, the signal EdI0 will activate both the optical OR functionalities for this case. Since the values of control signals for the 2nd & 3rd MRR (I3&I2) are zero therefore signal will not be available to their through ports (EtI3 & EtI2 = 0). As a result of this, the output of beam coupler—I will also be zero **(Y1 = 0)**. Now in the 2nd OR functionality, applied input signal EdI0 will be directed to its drop port (EdI3) because I3 = 0. Further, the signal EdI3 will appear at through port of MRR5 (EtI1) because of the value of its control signal(I1) = 1. As EtI1 is high therefore the output of beam coupler-II will also be high **(Y0 = 1)**. The MATLAB output for the above condition is reflected in Fig. 6.

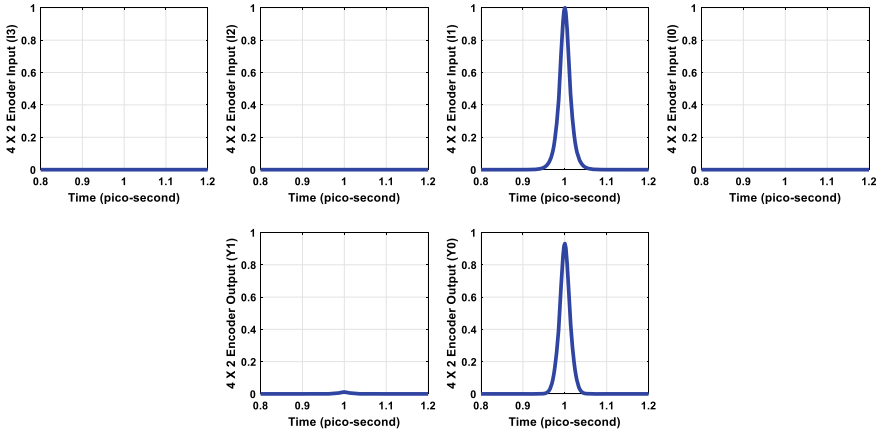


Fig. 6 MATLAB output of the proposed design for input combination (I3 = 0, I2 = 0, I1 = 1, & I0 = 0)

Case 3: When I3 = 0, I2 = 1, I1 = 0, andI I0 = 0

Similarly, if the applied control pulse I0 = 0 then we will get the applied input signal of MRR1 at its drop port (EdI0). As the value of control signal I3 = 0, through port outputs of 2nd and 4th MRRs will be equal to zero because the optical signal (EdI0) will appear to their drop ports. Now, as I2 = 1, so its input signal EdI3 will appear at EtI2 and its value will be high. Since EtI2 is one of the inputs to beam coupler-I, therefore its output will also be high **(Y1 = 1)**. The output of beam coupler will be zero **(Y0 = 0)** because both I2 & I3 = 0. This condition is reflected graphically in Fig. 7 which is obtained from MATLAB.

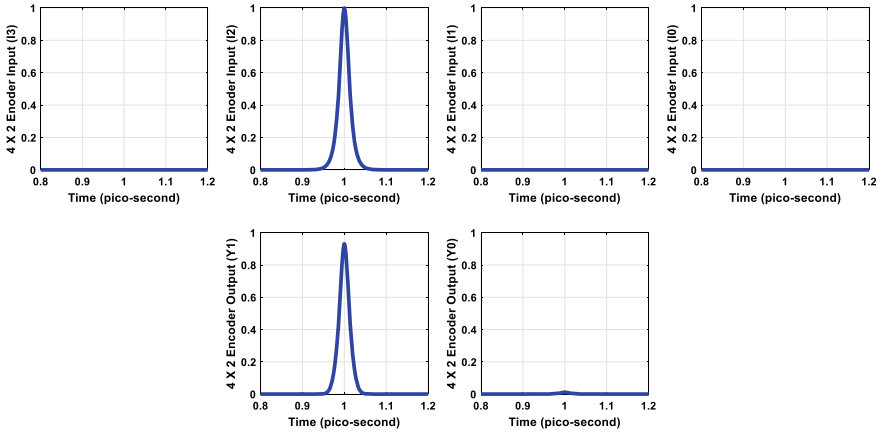


Fig. 7 MATLAB output of the proposed design for input combination (I3 = 0, I2 = 1, I1 = 0, & I0 = 0)

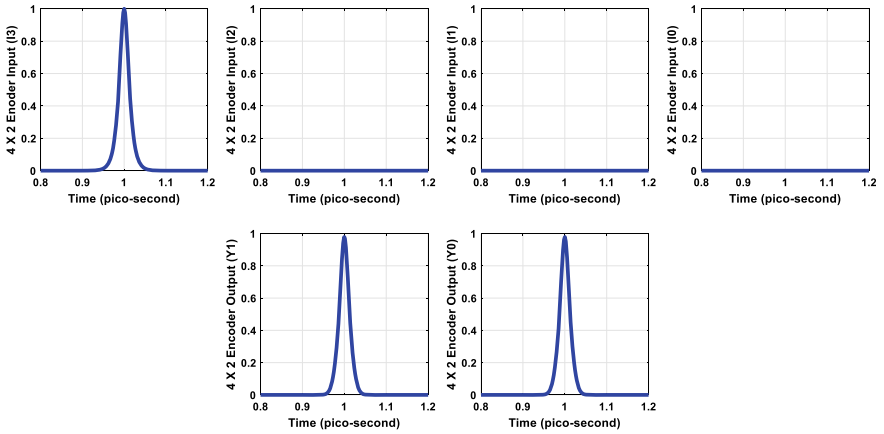


Fig. 8 MATLAB output of the proposed design for input combination (I3 = 1, I2 = 0, I1 = 0, & I0 = 0)

Case 4: When I3 = 1, I2 = 0, I1 = 0, andI0 = 0

In this case, the applied input optical signal to MRR1 comes to its drop port (EdI0) because of pump signal I0 = 0. This signal (EdI0) is further applied to the input ports of MRR2 & MRR4 and as the values of control pulses I3 = 1, I2 = 0 & I1 = 0, so the optical signal will now appear at the through ports of both the ring resonators (MRR2 & MRR4) and no signal will be obtained to their drop ports. Thus, outputs of both the beam couplers will be equal to logic 1 **(Y1 = 1 & Y0 = 0)**. The MATLAB output for the above condition is reflected in Fig. 8.

4 Conclusion

The proposed article illustrates the working principle of the MRR circuit and its application as an optical switch. The paper covers theoretical as well as mathematical derivations of optical ring resonator necessary for its switching phenomena and it is further verified using MATLAB simulation software. The switching activity of the ring resonator has been effectively utilized to design an optical encoder device in this paper. Five ring resonators in total are used here for the implementation of a 4 × 2 optical encoder. Finally, the proposed architecture has been verified using MATLAB simulation software. Therefore, for high-speed data communication system in the optical domain, this article will be very useful.

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Design of Micro-ring Resonator Based All-Optical Half Adder Using 2–4 Line Decoder Circuit

Sushanta Mahanty, Rakesh Choudhary, and Ajay Kumar

1 Introduction

The modern era communication technology focused on innovative and optimum methodology to improve the communication system. Implementation of digital computing phenomena is one of the most important aspects, which includes some added advantages of the optics. Many researchers have achieved an accurate switching activity, where the switching activities are further utilized to explore the concepts of various combinational and sequential activities. In many cases, the idea of linear electro-optic effect (EO), i.e. (Pockels effect) is applied for the improved switching activity. One of the concepts of signal selectivity in the form of 1×4 optical signal router is discussed in [1]. The paper discusses an outline of the integrated optical signal router based on the concept of the EO effect. Similarly, many researchers have employed the optical interferometer circuits, which is a combination of optical couplers and optical delay devices, which are a common element employed in all-optical devices [2–4]. Based on the EO effect and proper feedback mechanism, the implementation of optical sequential circuits is investigated [5]. Using the principle of linear EO effect, some work has been explored to observe some combinational logical phenomena. Using the concept of Pockels effect, the concept associated with basic logic gate some of the combinational logic circuits such as optical code converter and even parity checker, optical adder, and subtractor [6–8], optical universal logic gates, and some MOEMS pressure sensors [9] are widely investigated. However, all the switching activities associated with [1, 5–9] are based on the concept of the EO effect, where the semiconductor optical amplifier (SOA) has not been used for the implementation of logical functionality. In the same

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manner, many researchers are also involved with some other techniques to implement the function of sequential logic. The implementation and performance of sequential circuits have been studied in [10]. A novel design of some all-optical combinational circuits that can be involved for the functions implementing more than single value logic is described in [11]. In a similar manner, A simple and novel scheme presented (XGM) effect in wideband SOA-based Mach–Zehnder interferometer having a feedback loop for all-optical sequential circuits such as flip flop, shift registers have a quick response, having very low complexity has been investigated in [12–18]. The design of sequential circuits based on (SOA-MZI) for two stable states is reported by phase-shifting of MZI arms. In the same manner, [15] have been explored a novel all-optical T-flip-flop implemented using an element of single-optical latching consisting of an integrated (SOA-MZI), and feedback loop. In our proposed work, it has been described as an approach to realize the all-optical HA using a 2–4 line decoder circuit. In Sect. 1, we discussed the introduction of earlier relevant works associated with the technology, and Sect. 2 designates the important mathematical formulations behind MRR based switching phenomenon. In Sect. 3, we designed and analyzed the techniques to implement the half adder using a 2–4 line decoder circuit with its complete layout diagram. The discussed schemes are verified and simulated using MATLAB. Finally, we describe the conclusion in Sect. 4.

2 Micro-Ring Resonator (MRR)

The MRR is one of the optical switching devices, most of the researchers for the switching phenomenon in the optical domain are focused on the coupling principle between the I/O optical waveguide and the optical ring resonator. For that MRR comprises the optical ring resonator, i.e. the mechanism based on the resonator cavity. A portion of continuous-wave signal or logical data is permitted to transmit to the ring resonator, Fig. 1 shows the details. k_1 is the coupling coefficient of the input optical waveguide with the optical ring resonator, and r is the radius of the optical ring resonator. It has been observed that the positive interference may have occurred, if it is the total optical path length is a multiple of wavelengths. The positive interference in MRR is known as 'ON RESONANCE'. So the output port of the MRR provides fringes periodic in nature. The coupling coefficient of the optical ring resonator with the output optical waveguide is k_2. The developed wave inner ring is coupled to the output port provides the maximum transmission in drop ports.

As a result, the through ports have minimum resonance. For the proper switching activity, the nonlinear substantial has been used to produce the resonance. By applying the proper light amplitude, through the ring resonator from the top of the ring excitation is observed in the optical ring, and the effective index is varied. And finally, the refractive index may comparable decrease due to high-density carrier generated from the total absorption of intensity, which makes the blue-shift phenomenon, momentarily for the particular micro-resonance wavelengths. Different resonant wavelength occurs due to variation in the refractive index (R.I.) then this

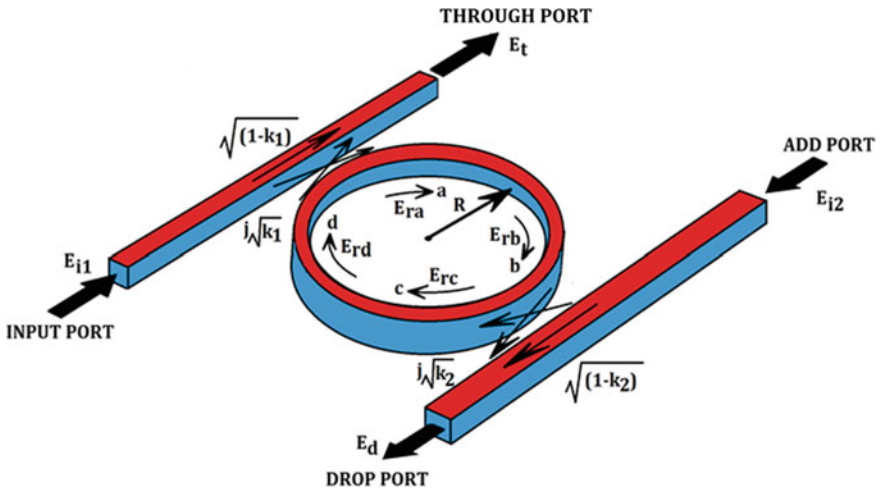

Fig. 1 Single micro-ring resonator

phenomenon is used as switching activity for ON or OFF for a signal. Considering L is the circumference of the optical ring. k_1 is the coupling coefficient of the input optical waveguide with the optical ring resonator, whereas coupling coefficient of the optical ring resonator with the output optical waveguide is k_2, intensity attenuation coefficients of the optical ring is α, γ is the intensity insertion loss coefficients and wave propagation constant is k_n, where $k_n = \frac{2\pi}{\lambda} n_{\text{eff}}$, the resonant wavelength of the ring is $\lambda . n_{\text{eff}} = n_0 + n_2 . I = n_0 + \frac{n_2}{A_{\text{eff}}} P$, where n_0 is linear R.I. and n_2 are nonlinear R.I. in an optical pump, signal intensity is I, and power is denoted by P. Let us consider E_{i1} is input port field and E_{i2} is the add port field. In the optical ring, the field at different points named as a, b, c, and d are E_{ra}, E_{rb}, E_{rc}, and E_{rd}, respectively, can be written as [13, 19, 20],

$$E_{ra} = (1-\gamma)^{1/2}\left[j\sqrt{k_1}E_{i1} + \sqrt{(1-k_1)}E_{rd}\right] \tag{1}$$

$$E_{rb} = E_{ra}\exp(-\alpha L/4)\exp(jk_n L/2) \tag{2}$$

$$E_{rc} = (1-\gamma)^{1/2}\left[j\sqrt{k_2}E_{i2} + \sqrt{(1-k_2)}E_{rb}\right] \tag{3}$$

$$E_{rd} = E_{rc}\exp(-\alpha L/4)\exp(jk_n L/2) \tag{4}$$

The through port field is given by

$$E_t = (1-\gamma)^{1/2}\left[\sqrt{(1-k_1)}E_{i1} + j\sqrt{k_1}E_{rd}\right] \tag{5}$$

The drop port field is given by

$$E_d = (1-\gamma)^{1/2}\left[\sqrt{(1-k_2)}E_{i2} + j\sqrt{k_2}E_{rb}\right] \tag{6}$$

For the generalization, it is assumed,

$$D = (1-\gamma)^{1/2}, \quad x = D\exp\left(-\alpha\frac{L}{4}\right) \quad \text{and} \quad \phi = \frac{k_n L}{2}$$

By solving Eqs. (1)–(6), we develop the E_t(TP) and the E_d(DP) field as:

$$E_t = \frac{D\sqrt{1-k_1} - D\sqrt{1-k_2}x^2\exp^2(j\phi)}{1-\sqrt{1-k_1}\sqrt{1-k_2}x^2\exp^2(j\phi)}E_{i1} + \frac{-D\sqrt{k_1k_2}x\exp(j\phi)}{1-\sqrt{1-k_1}\sqrt{1-k_2}x^2\exp^2(j\phi)}E_{i2} \tag{7}$$

$$E_d = \frac{-D\sqrt{k_1k_2}x\exp(j\phi)}{1-\sqrt{1-k_1}\sqrt{1-k_2}x^2\exp^2(j\phi)}E_{i1} + \frac{D\sqrt{1-k_1} - D\sqrt{1-k_2}x^2\exp^2(j\phi)}{1-\sqrt{1-k_1}\sqrt{1-k_2}x^2\exp^2(j\phi)}E_{i2} \tag{8}$$

The generalized equations E_t and E_d are the key terms for switching activity in ring resonator and helps in various design and analysis for any combinational and sequential logic circuits. It also assists to design the cascaded ring resonator. The cascaded structure for GaAs-AlGaAs based MRR is done having a wavelength (λ) for the COS input and having without any input in add port. Considering coupling coefficient $K_s = 0.25$, $(\alpha) = 0.0005\,\mu\text{m}^{-1}$, effective cross-sectional area $= 0.25\,\mu\text{m}^2$ and the $\lambda = 1.55\,\mu\text{m}$.

3 Design of All-Optical Half Adder Using 2: 4 Line Decoder Circuit Using the MRR Structure

In the data transmission system, binary data is transmitted from source to destination, the decoder plays an important role in secure transmission when the transmitter has to transmit the data over a multiple output path the function of the decoder is to select any one of the paths and the rest are disabled. Therefore, it is necessary to know the status of data at the receiver end which path carries the transmitted data. In other words, the receiver should be able to know whether the received information is appearing or not. To detect such type of occurrence, a decoder is one of the combinational circuits in digital communication is shown in Fig. 2. And truth table of the 2:4 line decoders is presented in Table 2. As our objective in this paper is confined with the design of

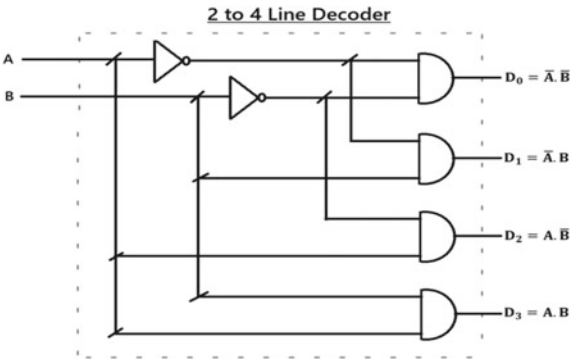

Fig. 2 2:4 line decoder circuit diagram

a two-bit adder (HA) using 2:4 line decoder part only so, the truth table of an HA and 2:4 line decoder are represented in Tables 1 and 2, respectively.

Figure 2 shows the logical diagram of 2:4 decoders where it is supposed to help the design of HA. Now, the suitable layout diagram describing the all-optical implementation of half adder/subs tractor using 2:4 decoders using the 3 identical MRR structures. Figure 3 explores the basic layout of all-optical HA/HS using 2:4 decoders using the proper layout of three identical MRR structure. In the input port E_i of MRR1 (COS) of wavelength (λ) $= 1.55\,\mu$m is applied. In the all-optical HA circuit addition of two single-bit binary numbers (A, B) and gives results in two single-bit binary output, represented as sum (S) and carry (C_{out}). The implementation of HA circuit using the 2–4 line decoder and beam coupler, MRR based optical switch is shown in Fig. 3. Maximum possibilities of the two variables (A, B) the four output terminals

Table 1 Truth table of half adder

Input		Output	
A	B	Sum (S)	Carry (C_{out})
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 2 Truth table of 2:4 line decoders

A	B	$D0$	$D1$	$D2$	$D3$
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

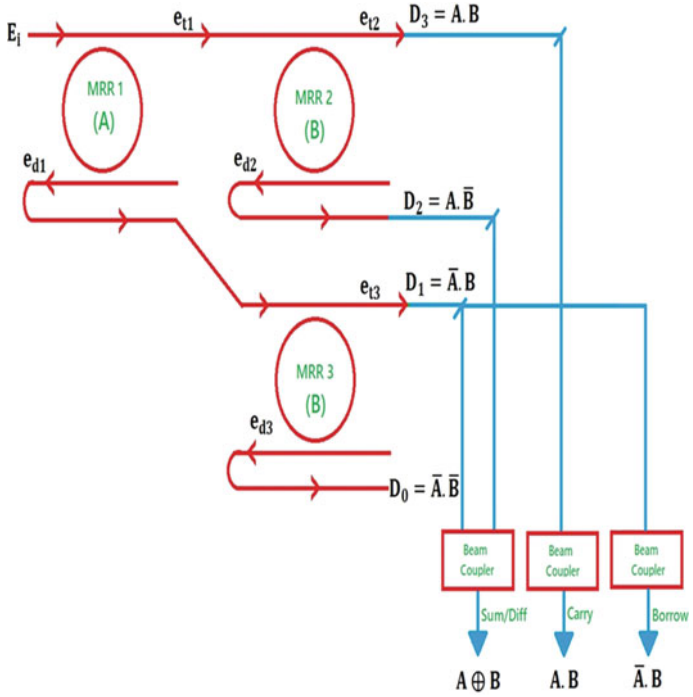

Fig. 3 The layout of all-optical HA/HS using 2:4 decoders using the 3 identical MRR structures

(*D*0–*D*3) one of the four outputs is obtained. All four possible cases are described in detail below.

Case-1: when the optical light comes from the COS is applied to the input port of MRR1. Here, in this case $A = 0$, $B = 0$; pumped signal (A) is in a low state; the light appears at the drop port of MRR1 and forwarded to the input of MRR 3. At the same time, pumped signal (B) is also in a low state; the signal propagates the same theory and goes to the drop port of MRR 3. As a result, light beam appears at the output $D0$. So here, in this case, the output $D0$ is in a high state (logic one), and the rest output nodes are in a low state (logic zero). The output of $D0$ after passing through the beam coupler appears at the logical sum (S) as well as carry (C_{out}) for the all-optical HA unit. Hence, here we observed, $S =$ '0' and $C_{\text{out}} =$ '0'.

Case-2: $A = 0$, $B = 1$; Similarly, when MRR1 pumped signal (A) is a low state, and MRR 3 pumped signal (B) is a high state, the light appears at the drop port of MRR1 and goes to the input port of MRR 3. At the same time, pumped signal B is a logic high state; the signal propagates and goes through port of MRR 3. As a result, light beam appears at the output $D1$. So here, in this case, the output $D1$ is in a high state (logic one), and the rest output nodes are in a low state (logic zero). The output of $D1$ after passing through the beam coupler appears at the logical sum (S) as well as

carry (C_{out}) for the all-optical HA unit. Hence, here we observed, S = '1' and C_{out} = '0'.

Case-3: $A = 1$, $B = 0$; Similarly, when MRR1 pumped signal (A) is a high state and MRR 2 pumped signal (B) is a low state, the light appears at the through port of MRR1 and goes to the input port of MRR 2. At the same time, pumped signal B is low state; the signal propagates goes to drop port of MRR 2. As a result light beam appears at the output $D2$. So here, in this case, the output $D2$ is in a high state (logic one), and the rest output nodes are in a low state (logic zero). The output of $D2$ after passing through the beam coupler appears at the logical sum (S) as well as carry (C_{out}) for the all-optical HA unit. Hence, here we observed, S = '1' and C_{out} = '0'.

Case-4: $A = 1$, $B = 1$; Similarly, when MRR1 pumped signal (A) is a high state and MRR 2 pumped signal (B) is also in a high state, firstly the light appears at the through port of MRR1 and forwarded to the input port of MRR 2. At the same time, pumped signal B is also in the high state; the signal propagates and goes through port of MRR 2. As a result, light beam appears at the output $D3$. So here, in this case, the output $D3$ is in a high state (logic one), and the rest output nodes are in a low state (logic zero). The output of $D3$ after passing through the beam coupler appears at the logical sum (S) as well as carry (C_{out}) for the all-optical HA unit. Hence, here we observed, S = '0' and C_{out} = '1'.

Finally, the proposed structure is simulated using MATLAB software. Using Eqs. (7) and (8), the appropriate simulated result using MATLAB is as follow.

Figure 4 shows the suitability of the proposed MRR based HA using a 2:4 line decoder circuit. In Fig. 4a, 2:4 line decoder represents the different combinations of optical input bit sequences A, B where the bit sequences acquire the value from 00, 01, 10, *and* 11. The first-row of Fig. 4a input of AB is 00, in the third-row reflects the input of AB is 01, in the fifth-row of Fig. 4a input of AB is 10, and in the seventh-row input of AB is 11 the corresponding 2:4 decoder outputs are shown in the second-row where decoder output appears in $D0$ and rest of the outputs ports are at a logic low level, similarly in fourth-row, where decoder output appears in $D1$ and rest of the outputs ports, are at a logic low level, in the sixth-row we observe where decoder output appears in $D2$ and rest of the outputs ports are at a logic low level and finally in the eighth row, where decoder output appears in $D3$ and rest of the outputs ports, are at logic low level, respectively. In Fig. 4b, we observed that for the all possible two-bit combinations of inputs AB in half adder, e.g. 00, 01, 10, and 11 respective output comes from the $D0$, $D1$, $D2$, and $D3$ are generated and finally, the half adder outputs are collected from the beam coupler as sum and carry Fig. 4a, b describes the corresponding optical equivalent of 2:4 line decoder and half adder.

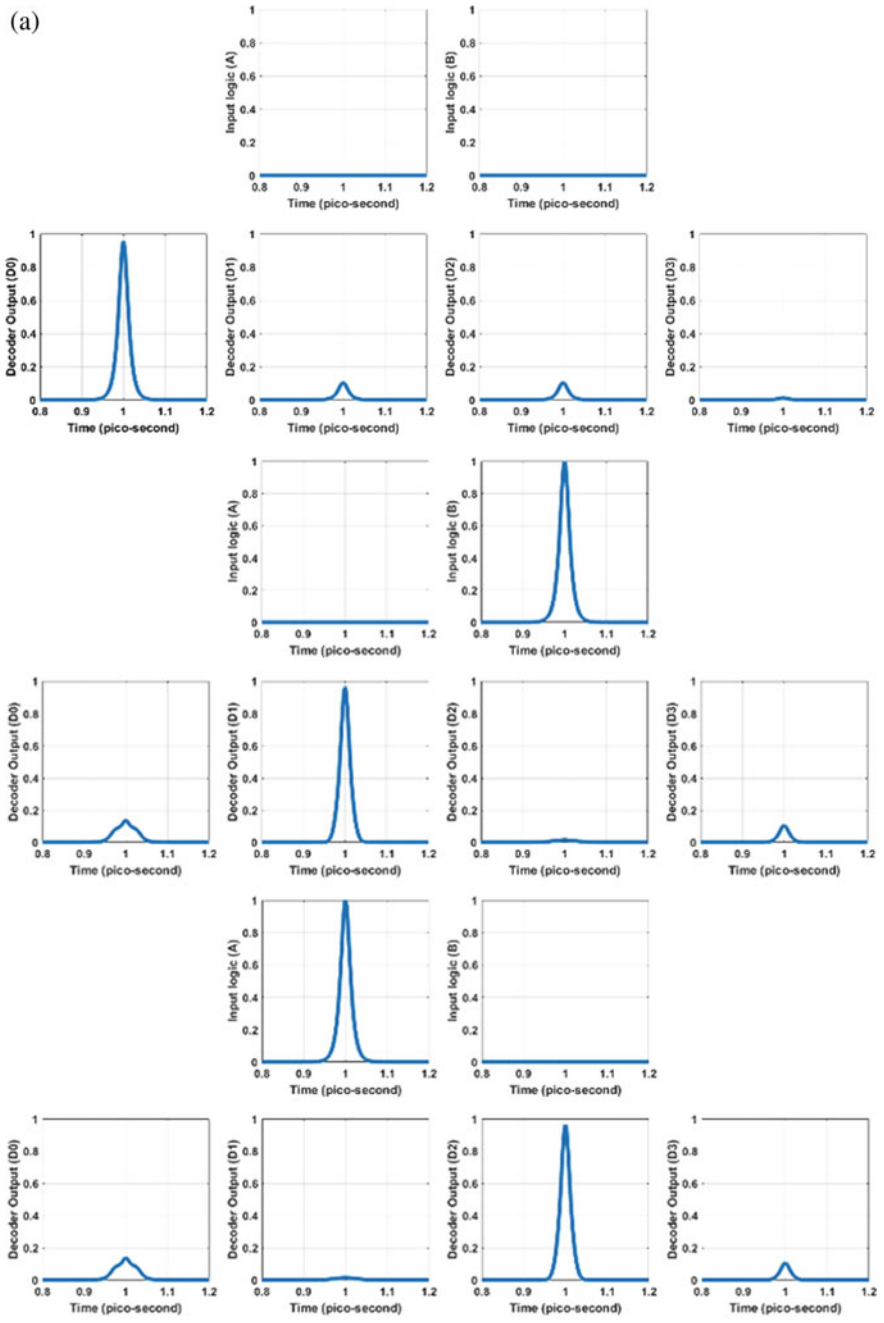

Fig. 4 **a**, **b** Simulated result using MATLAB for the proposed half adder using 2:4 line decoder circuit

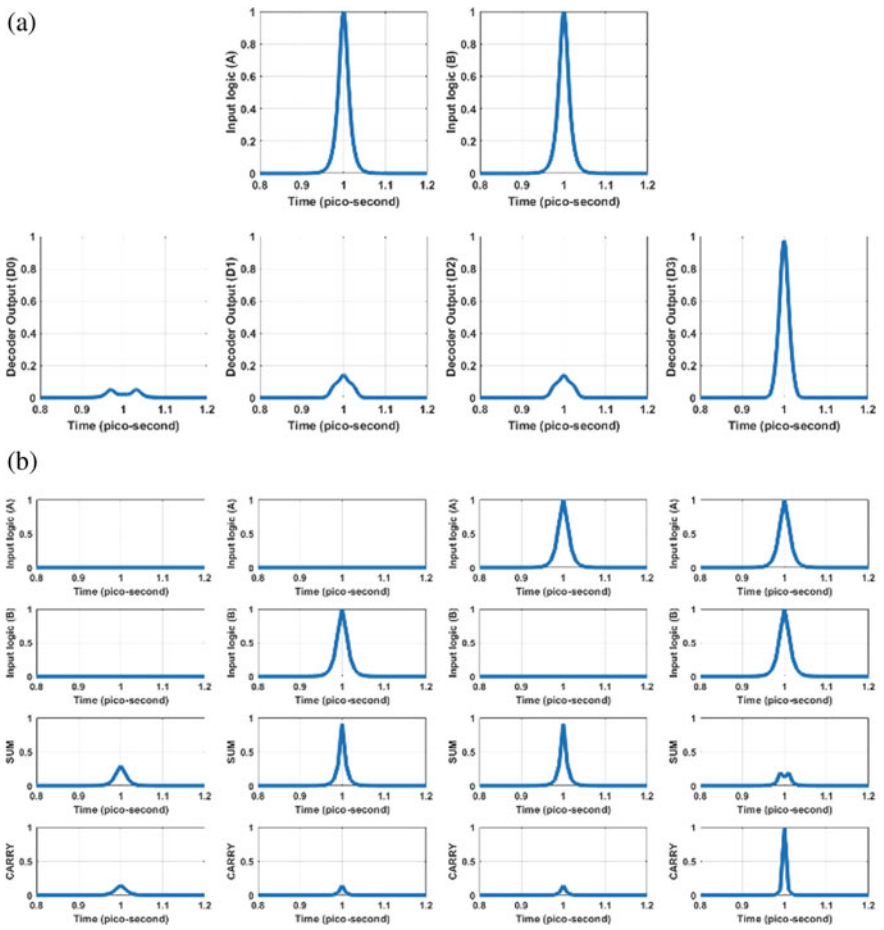

Fig. 4 (continued)

4 Conclusion

The paper shows some useful applications of the MRR structure for designing as well as implements the all-optical proposed HA using 2:4 line decoder circuit. In the paper, we have represented a detailed discussion about the single micro-ring resonator arrangement with all the device and simulation parameters. The proper structure of the optimum number of micro-ring resonator arrangements provides the layout of the proposed HA using 2:4 line decoder circuit. The conventional truth table of proposed all-optical half adder using 2 to 4 line decoder circuits are being verified with the MATLAB simulation results. The paper involves some optimistic approaches to implement some digital circuits, e.g. the HA using 2:4 line decoder circuit in the domain of optical communication. Finally, the discussed

scheme serves some added advantage in the field of optical communications, e.g. miniature size, secure signal transmission, greater bandwidth, etc. Hence, for the ultra-speed communication systems, the proposed scheme can be preferable.

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Image Restoration of Landslide Photographs Using SRCNN

Amrita Mohan, Ramji Dwivedi, and Basant Kumar

1 Introduction

In the last, few years CNN and deep learning-based algorithms have build-up power to solve different machine learning (ML) problems, and also, research areas related to computer vision are benefited. The most frequently used framework is the SRCNN, which manifest the application of deep learning knowledge to enhance images. The task of attaining a high-resolution image from the low-resolution image is referred to as Image Super-Resolution [1]. In many research areas, there has been a requirement for high-resolution images so that they can be utilized with various state-of-the-art deep learning algorithms to perform object detection and image classification in different domain. The term high resolution signifies more pixel information that can be extracted from images. The two main reasons for the need for resolution enhancement of landslide photographs: (i) To improve the performance of deep learning-based algorithms by using the concept of data labelling. (ii) Enhancement of landslide-related information in the photograph for individual analysis.

Initially, the term SRCNN was proposed by *C. Dong* et al. having several tempting properties. The proposed deep CNN has lightweight structure, fast speed and also have the state-of-the-art image restoration capabilities. Different types of parameter settings and network structures are examined, achieving trade-offs between speed and performance [1]. The term super-resolution [2] aims to retrieve high-resolution image from a specific poor resolution image.

Reconstructed-SRCNN was implemented by *C. M ward* et al., and three parameters, i.e. BRISQUE, SSIM and PSNR, were applied to the image, and it is concluded that expected image was reconstructed by SRCNN successfully [3].

A comprehensive review of super-resolution reconstruction methodology for remote sensing images, several categories for super-resolution, along with challenges

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associated with remote sensing images is given in [4]. Techniques suggested by [4] include interpolation-based super-resolution (SR), probability theory-based SR and learning-based SR.

Exhaustive literature of SR implementation methods with challenges associated with its implementation and various techniques to implement SR of an image with details along with comparative analysis of technologies is presented in [5].

For improving the spatial-resolution of remote sensing images, a new single image-SR method was implemented, i.e. DGANet-ISE (deep gradient-aware network with image-specific enhancement) by *M. Qin* et al. The proposed method was applied to remote sensing images generating significant results. It is also concluded that the proposed method is superior in terms of a visual and quantitative context [6].

Performance evaluation parameters, open-source datasets, along with three significant categories of super-resolution, i.e. supervised, unsupervised and domain-specific SR methods, are presented in [7]. A detailed survey on existing deep learning-based super-resolution methods along with the remark that the state-of-the-art methods still has certain limitations, restricting their use in real-world scenarios is given in [8].

A software algorithm is proposed by *P. Li* et al. for enhancement of image resolution by considering faulty sub-pixel matching. The proposed algorithm can reduce the effect of matching error dramatically and has good stability [9]. To achieve the super-resolution (SR) reconstruction of images, a new method is proposed by *N. Sun & H. Li*. The proposed method is validated using the publicly available online dataset, and it is also analysed that the proposed method has a powerful effect on PSNR and MSE. It is revealed after analysis that the proposed method is suitable for obtaining a high-quality image, and it performs better as compared to a single deep learning-based algorithm and traditional approaches [10].

Self-learning method for image super-resolution is proposed by using sparse representation [11]. The leverage of the proposed method is that it utilizes information related to the input image for training LR/HR dictionaries. Results of the proposed methods reveal that it regenerates the details and high-frequency information with satisfying accuracy [11].

Discrete contrast enhancement ranging from traditional to the new innovative method will be given by [12]. Also, 2D-based image enhancement method is proposed while preserving the mean brightness up to some degree.

1.1 DIP Based Resolution Improvement Approaches

In the field of image processing, the most common method of low-level image processing is “Resolution Improvement”. The main objective of the resolution of an image is to enhance the visual debut of an image. Images like aerial and satellite images in remote sensing domain, medical images may endure from standard and low contrast [13]. Image enhancement method can be categorized into two main categories: (I) Spatial Domain, (II) Frequency Domain [13].

(I) ***Spatial Domain*** [14]: The term "spatial domain" means an accumulation of pixels constituting an image. Methods of the spatial domain directly perform on the image pixel, i.e. image pixels are manipulated directly [14]. It is further classified into subcategories:

(a) Histogram equalization [14]: It is the most essential part image processing method. It can be applied either on the whole image or any particular part of an image resulting in improved visualization [14].

(b) Image Smoothing [14]: The main objective of this method is to reduce the effects like noise generated form camera, missing digital numbers, specious pixel values, etc. [14]. There are many techniques exist or image smoothing, neighbourhood averaging, etc.

(c) Image Sharpening [14]: The fundamental purpose of this method is to feature fine details present in the image or details that are blurred due to noise and another type of effects. In this method, high-frequency components are enhanced, implying that spatial filter having high positive feature at the central position [14].

(d) High Boost Filtering [13, 14]: It is a sharpening operator used in the image processing domain. It is applied for amplification of high-frequency components in the image. The amplification of an image is accomplished with a process which subtracts a low-pass filter image from the scaled input image [14, 15].

(II) ***Frequency Domain*** [14, 15]: In this type of method, Fourier transformation of the image is calculated first, after that obtained result is multiplied by the filter, then inverse transform of the image is taken for producing the enhanced image [14]. Further, it is classified in the following classes:

(a) Low Pass Filter (LPF) [15]: It removes high-frequency components and keeps low-frequency components. LPF is used for image smoothing, and it is achieved by constricting high-frequency component and preserving low-frequency components [14]. Mathematically mechanism is expressed as [14]:

$$G(U, V) = H(U, V).F(U, V) \tag{1}$$

where F(U, V) is Fourier transformation of the image and H(U, V) is Fourier transform of filtering mask.

(b) High Pass Filter (HPF) [14, 16]: This filter removes low-frequency component keeping high-frequency components. It is applied to image sharpening. This type of filter is achieved by attenuating low-frequency components while retaining high-frequency components [14]. It is written as [14]:

$$H(U, V) = 1 - H'(U, V) \tag{2}$$

where H(U, V) is Fourier transform of high pass filter and H′(U, V) is Fourier transform of low-pass filter.

(c) Band Pass Filter (BPF) [14]: It keeps frequencies of constrain range and removes the very low and the very high-frequency components. It is also utilized for edge enhancement reducing the noise at the same time.

This paper presents a deep learning-based advanced method for resolution improvement of landslide photographs using the current state-of-the art approach, i.e. SRCNN. To attain this objective, the SRCNN is expanded using Keras. The newly implemented deep CNN-based SRCNN has the capability to perform sequential mapping ranging from low-resolution landslide image to high-resolution landslide image.

The rest of the paper is organized as follows: Section 2 is a description of the dataset used. Section 3 introduces the methodology adopted by SRCNN algorithm. Section 4 includes results, table and performance evaluation parameters of SRCNN algorithm on landslide images. Section 5 is the conclusion summarizing findings in the proposed work.

2 Dataset Used

The dataset used in this research work has been freely downloaded from the available search engines (Bing, Google) and other sources. A python script is implemented for downloading landslide data from Bing and Google search engines. A huge number of images are downloaded from these sources, and some specific images that belong to particular terrain having landslides were manually selected by visual inspection to identify those photos which are most representative for landslides in the hilly region. It can be seen that most landslide images include mountains, having vegetation cover, landscapes, forests, roads and other man-made objects. At the same time, during the selection of representative landslide photos, the scene completeness, i.e. a variety of object types, landslide in the specific hilly region was considered. For example, side-view of any particular cliff with landslide was excluded, and landslides that only represents mud were excluded. Landslide belonging to particular terrain, having vegetation, waterbody, buildings, etc., was kept. On the other side images that are completely irrelevant (for ex: ads, book cover pages), post-hazard resilience images without the specific landslide (like diggers, peoples, rescue team), flooding photographs and images with extreme small sizes were also discarded while preparing training datasets.

The total number of 30 landslide photographs is used with pre-trained model. In the proposed work, the number of training images is 22, and testing is 10 along with pre-trained weights of SRCNN.

3 Methodology

The pre-trained SRCNN model involves three convolutional layers with activation function: (a) Convolved Feature/Patch Extraction and Representation: having filter size 9×9, (b) Multidimensional Scaling with the spatial filter of size 1×1 and (c) Reconstruction from high-resolution patches with the spatial filter of size 5×5, respectively. The input image used with SRCNN is a bilinear interpolation image of a low-resolution landslide image. The first layer in pre-trained SRCNN extracts feature (patches) and representation of low-resolution landslide images. The second convolutional layer maps the feature map with n_1 dimension, having several patches to n_2 dimension making a multidimensional scaling or nonlinear mapping. For mapping, the number of patches depends on the filter size of the second CNN layer. Then the last layer is responsible for the reconstruction of the desired HR image from HR patches. Therefore, it is concluded that SRCNN mainly serves two purposes: (i) Transferring input image to end layer and (ii) Reconstruction of residuals.

Workflow:

(i) **Pre-processing**: We have some landslide photographs as shown in Fig. 1; low-resolution version of these landslide photographs is achieved by resizing using OpenCV. Several approaches exist for resizing images; in the proposed work, bilinear interpolation is used.
(ii) **Patch Extraction**: Set of feature maps extracted, i.e. feature maps 1 and 2 as shown in the Fig. 2 from low-resolution landslide photograph.
(iii) **Non-Linear Mapping**: In this step, feature map depicting low-resolution to high-resolution patches is mapped.
(iv) **Reconstruction**: High-resolution landslide photograph is produced from high-resolution patches as shown in Figs. 2 and 3.

Steps (ii)–(iv) can be considered as a convolutional layer in a CNN that obtain the pre-processed landslide photographs from above step 1 and results in high-resolution (HR) landslide image. The SRCNN structure consists of three convolutional layers [1]:

Fig. 1 Sample images used with SRCNN

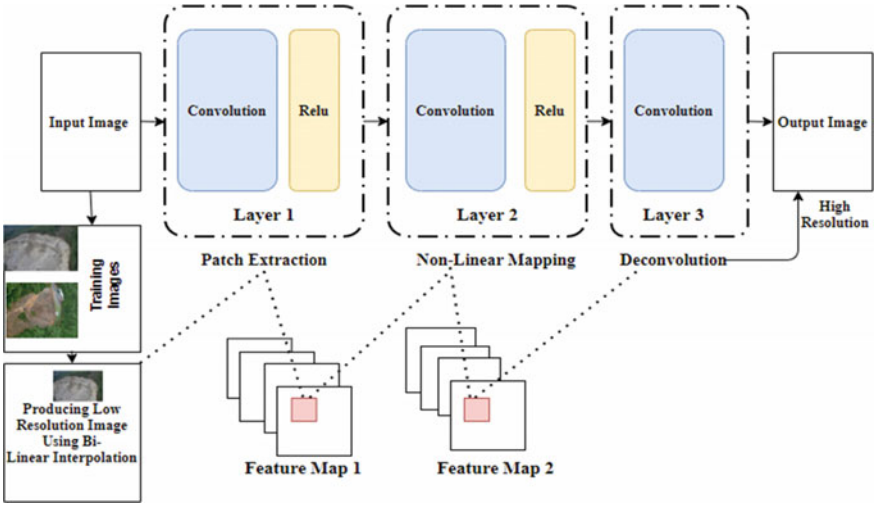

Fig. 2 Workflow diagram for SRCNN

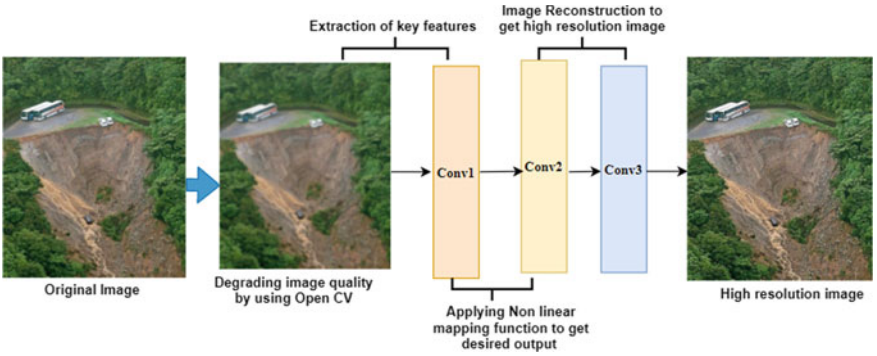

Fig. 3 Sample images used with SRCNN

Input Landslide Photograph: Low-resolution landslide photograph upsampled to desired high-resolution landslide photograph, C channels (the colour component of the landslide photograph).

Layer 1: Patch or Feature Extraction:

- Filter n_1, having size $c \times f_1 \times f_1$
- ReLU (Rectified Linear Unit): Nonlinear activation function
- Output: Feature Map 1
- Parameters to enhance: $c \times f_1 \times f_1 \times n_1$ weights and n_1 biases.

Layer 2: Nonlinear mapping:

- Filter n_2, having size $n_1 \times f_2 \times f_2$

Table 1 PSNR, MSE and SSIM after applying SRCNN

Image	PSNR		MSE		SSIM	
	Degraded	Improved	Degraded	Improved	Degraded	Improved
Image 1	31.14	32.40	149.94	112.13	0.81	0.87
Image 2	26.56	26.95	430.46	393.25	0.78	0.81
Image 3	25.51	26.96	547.79	391.94	0.72	0.82
Image 4	28.69	29.84	263.17	201.97	0.77	0.83
Image 5	23.96	24.38	782.06	710.02	0.72	0.77
Image 6	24.81	25.32	643.27	571.85	0.75	0.79

- ReLU: Nonlinear activation function
- Output: Feature Map 2
- The parameter to enhance: $n_1 \times f_1 \times f_1 \times n_2$ weights and n_2 biases.

Layer 3: Reconstruction of Image:

- The single filter of size $n_2 \times f_3 \times f_3$
- Identity: Activation function
- Output: High-resolution image
- Parameters to optimize: $n_2 \times f_3 \times f_3 \times c$ weights and c biases.
- In the next step, importing required packages and libraries and printing them with their versions forex. Keras, cv2, matplotlib, skimage, etc.
- Exemplify the performance metrics, i.e. PSNR, MSE and SSIM. Essential functions are also defined to calculate the three metrics. SSIM is directly specified from "sci-kit library". For PSNR and MSE, own function is defined.
- Building and deploying SRCNN model in Keras. The architectural detail and hyperparameter can be obtained from reference [1].
- After applying SRCNN approach to the input landslide images, PSNR, MSE and SSIM are calculated for degraded and high-resolution landslide image as shown in Table 1.

4 Performance Evaluation Metrics and Results

For evaluation model performance, following image quality metrics are used:

(i) *PSNR (Peak Signal to Noise Ratio)* [17]: It is the ratio between the highest possible power of an image and the power of corrupting noise that affects the image quality representation. It is given as:

$$\mathbf{PSNR} = 20 \log_{10}\left(\frac{\mathbf{MAX}_I}{\sqrt{\mathbf{MSE}}}\right) \tag{3}$$

where MAX_I the maximum possible pixel value of the image and MSE is the ratio of the sum of all squared value differences and image size, i.e. 3.

(ii) *SSIM (Structural Similarity Index)* [1]: It is capable of measuring the perceptual difference between the two images of the same type. It depends on the visible structures present in the image.

$$\mathbf{SSIM} = \frac{(2u_x u_y + C_1)(2\sigma_{xy} + C_2)}{(u_x^2 + u_y^2 + C_1)(\sigma x^2 + \sigma y^2 + C_2)} \tag{4}$$

where (X, Y) = Common size window.
μ_x = Average of X, μ_y = Average of Y, σ_x^2 = Variance of x, σ_y^2 = Variance of Y, σ_{xy} = Covariance of X and Y, $C_1 = (K_1 L)^2$, $C_2 = (k_2 L)^2$ two variables to stabilize the weak denominator, L = dynamic range of the pixel value, $K_1 = 0.01$ and $K_2 = 0.03$ by default.

(iii) *MSE (Mean squared Error)* [17]: It is the measurement of average squares of error, i.e. average of the squared difference between the estimated value and actual value.

$$\mathbf{MSE} = \frac{1}{n}\sum_{i=1}^{n}(f_i - y_i)^2 \tag{5}$$

where N = number of data points, f_i = Value returned by the data model and y_i = the actual value of the data point y_i (Fig. 4).

5 Conclusion

To achieve improved resolution of landslide photographs, an innovative deep learning-based method single image super-resolution is used. The state-of-the art SRCNN method is capable of learning the end-to-end mapping between low- and high-resolution images. In the proposed work, we applied three different metrics, i.e. PSNR, MSE and SSIM, for the objective quality assessment of the output high-resolution landslide photograph using SRCNN. After deploying SRCNN, it is revealed that it performs well in image restoration. The future work includes the implementation of different interpolation techniques on multispectral and multimodal remote sensing images using different variants of the CNN model.

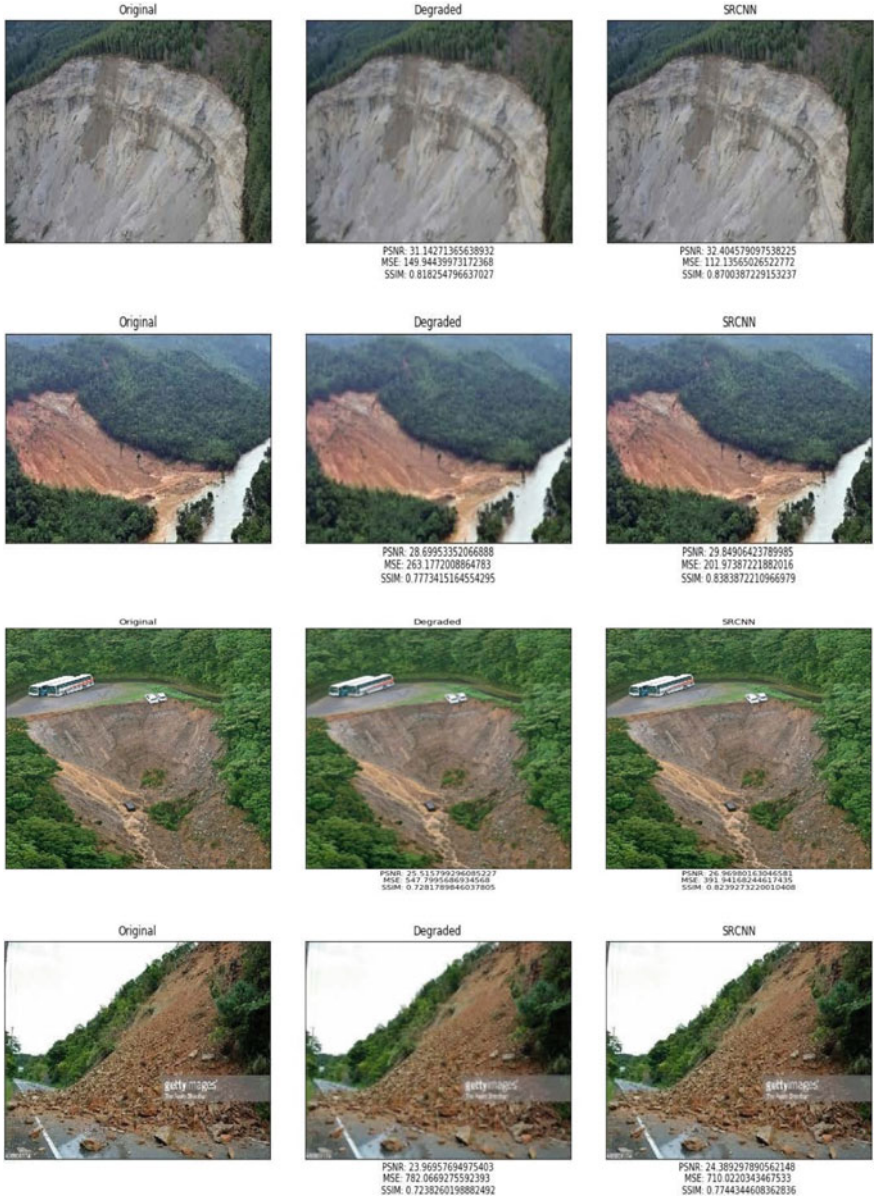

Fig. 4 Results obtained from SRCNN on landslide photographs

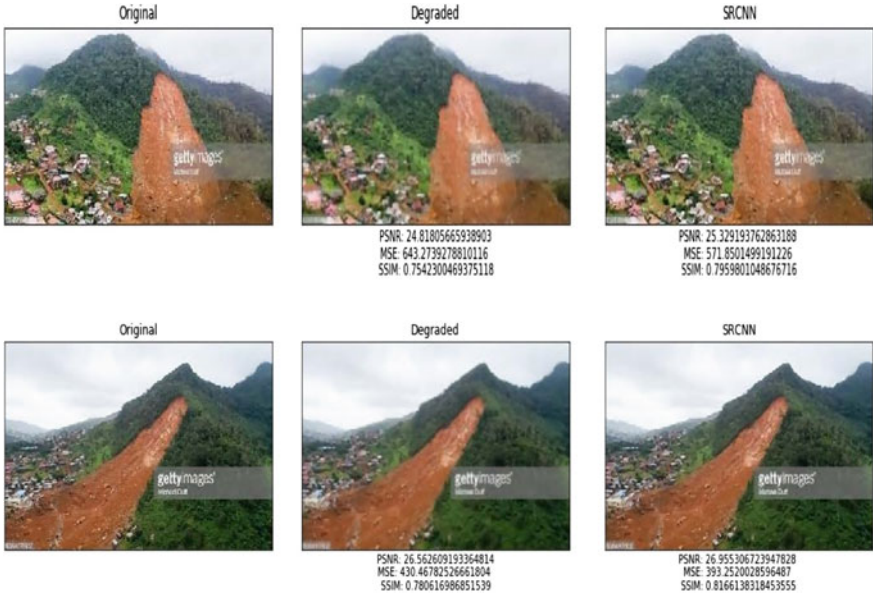

Fig. 4 (continued)

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Classification Techniques for Binary Motor Imagery Signal for Brain-Computer Interfaces

Piyush Kant, S. H. Laskar, and Jupitara Hazarika

1 Introduction

Motor imagery (MI) classification has been a very significant issue in brain-computer interfaces (BCI). The need for better classification accuracy is the paramount for the development of assistive technologies for people with neuromuscular disorders. With the need for classification of mind signal interpretations, electroencephalogram (EEG) is considered as an optimal solution for non-invasive brain signal analysis for communication and control of devices such as wheelchair and the robotic arm. The ability to interpret brain signals can enable users with motor disabilities to interact with the outside environment without using conventional motor pathways. Since the subject is related to humanitarian assistance, better accuracies can play a vital role in providing correct outcomes for particular movement imagination. EEG patterns are generated due to event-related potentials (ERP) [1, 2]. ERP(s) can further be subdivided into event-related synchronization (ERS) and event-related desynchronization (ERD) [3]. Event-related desynchronization is the event where rain cells are desynchronized with each other, and they result in the lower potential of EEG waves. On the other side, event-related synchronization results in the higher potential, due to synchronization in brain cells' potential.

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Brain-computer interfaces based on motor imagery systems have wide applications in medical and non-medical fields [4], such as real-time control in the robotic arm, rehabilitation of a person with stroke. To operate a robotic arm [5, 6] in coordination with MI-BCI, a scheme was proposed by Cantillo-Negrete et al. Generally, the raw EEG signal of the subject was analyzed using computational models to classify various imagination task related to motion. That was performed using various pattern recognition algorithms such as feature extraction, feature selection, and classification using various machine learning methods. Various machine learning methods [7] were proposed for the classification of motor imagery tasks for BCI applications. However, it is still open for further research to get higher classification accuracy and dimensional features from EEG data.

The data used in the present study is acquired using the international 10-20 system for EEG acquisition [8] which is shown in Fig. 1. The 10-20 system is an arrangement to locate EEG electrodes evenly on the brain scalp. The human motor cortex [9] is the brain region that controls movement-related activities in the human brain as shown in Fig. 1. This region is a central part of the brain scalp.

This work demonstrates a comparison of two motor imagery (MI) classification techniques. Preprocessing steps for both techniques are kept the same for comparison. Both techniques employ filtering the signal and wavelet denoising for each signal. In the first technique, conventional feature extraction techniques with statistical features especially Shannon entropy [10] was done, and it was claimed to be a very prominent feature as it outperformed mean, variance energy, log-energy entropy, kurtosis, and skewness [11]. The given feature was then fed to Support Vector Machine (SVM), K-Nearest Neighbor (KNN), and Linear Discriminant Analysis (LDA) classifier for classification. For the second one, the EEG signals were processed using continuous wavelet transform (CWT) [12] to transform the signal into CWT Filterbank.

The first approach for motor imagery classification has been shown in Fig. 2. In this approach, the data has been collected from the C3 and C4 electrodes as they lie just over the motor cortex. Both the electrodes combine into one dipole for the motor

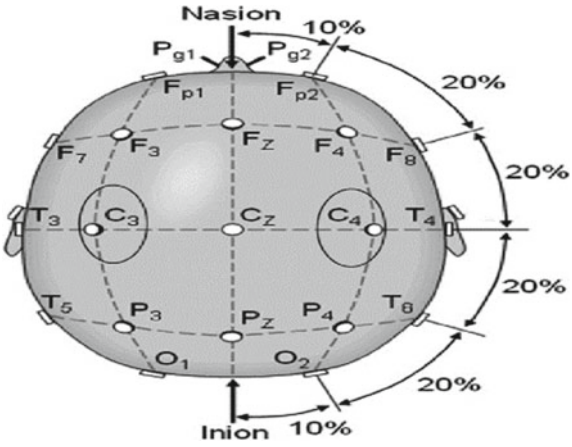

Fig. 1 Artifacts empowered by artificial intelligence (*Source* LNCS 5640, p. 115)

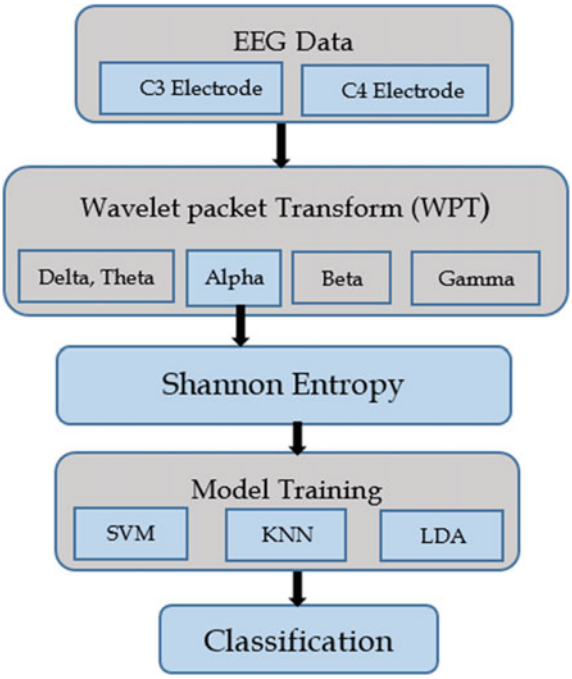

Fig. 2 Process flow of first approach

imagery related to the movement imagined. Shannon entropy was then evaluated using different classifiers for evaluation of the best performing method.

The second approach is shown in Fig. 3 employs the transfer learning method. Here, the signals from both the electrodes were combined, and continuous wavelet transform (CWT) was used to convert 1-Dimensional EEG signals into 2-Dimensional time–frequency images.

The main advantage of CWT is the time–frequency representation of the time-domain EEG signals. The time–frequency image generated by CWT has continuous frequency information embedded with continuous time. Moreover, the 2-D image is most suitable for transfer learning using available deep neural networks [13]. Many available deep learning models use Convolutional Neural Networks (CNN). The CNN extracts image features such as edge and curves and detects patterns in the given image. Automatic feature extraction by pre-trained deep learning models makes 2-d images the most suitable for our study. In a recent study, it has been observed [14] that for the data used linear models such as alexnet, vgg16, and vgg19 performed best for two-class motor imagery classifications. Thus, for our study, we used these three models to evaluate algorithm performance.

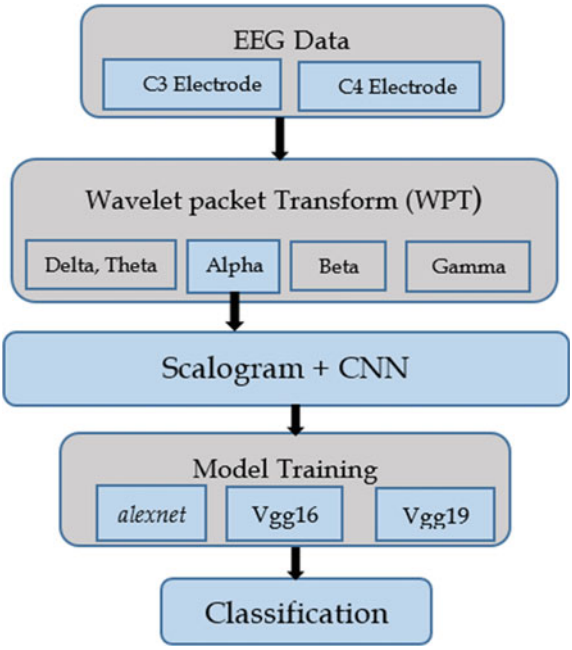

Fig. 3 Process flow of the second approach

2 Methodology

2.1 Data Description

The dataset used in this study is BCI competition II dataset III [15], also known as Graz 2003 data. The dataset has been used in several studies for MI-based BCI algorithms. The data was recorded by the University of Technology Graz, Institute of Biomedical Engineering. Data is acquired from a 25-year-old healthy female participant. Tasks during data acquisition were motor imagery of left and right hand movement. The task was based on the imaginary movement of a block based on a cue that was shown on the screen randomly.

The timing scheme for data acquisition is shown in Fig. 4. The duration for EEG data for each sample was 9 s. The subject was asked to relax in the beginning. After two seconds, a fixation cross was shown which marks the beginning of the trial and from three to nine-second, a cue showing the movement direction was shown to the subject which represents the movement direction for the hand MI. Hence, the data recorded has motor imagery for six seconds.

A total of 280 trials were recorded out of which 140 samples were taken for training the data and the remaining 140 samples were kept for testing. The data was recorded for electrodes on the motor cortex which were C3, C4, and CZ electrodes as described in Fig. 1. For our algorithms, we have chosen C3 and C4 electrodes as

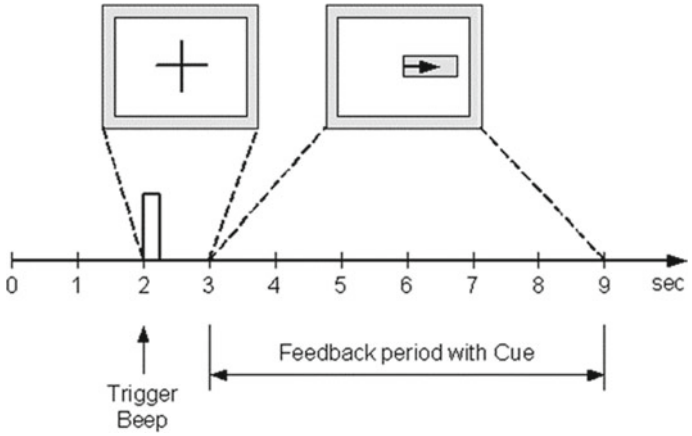

Fig. 4 Timing schemer for data acquisition

CZ has not been very much effective in our study. This approach is the same for both the approaches that have been used in this study.

2.2 Preprocessing

The EEG data processed for different bands [16, 17] which are Delta (0.5–4 Hz), Theta (4–8 Hz), Alpha/Mu (8–16 Hz), Beta (16–24 Hz), and Gamma band (24 Hz and above). The EEG signal was filtered to 0–30 Hz using a bandpass filter. The bands were decomposed using wavelet packet transform (WPT). Alpha or Mu band is proven to be the most effective in MI classification [18, 19] in several studies hence, both the approaches were implemented on the Mu band in our study.

2.3 Feature Extraction

Brain waves or EEG are time-varying, non-stationary signals. It contains different frequencies at different times even for a short amount of time [20]. In comparison with FFT and STFT, wavelets can decompose the signals [21]. Therefore, to extract accurate EEG signal feature both the approaches employs wavelet packet transform (WPT). In our study, we have used Daubechies 4 or popularly known as db4 as it has been recognized for good results [22]. The signals were then decomposed on the various level to extract a specific band of frequencies. A wavelet packet transforms at different level down-samples the signal into detail coefficients (High-pass) and approximation coefficients (Low-pass) [23]. These coefficients are further down-sampled for more details and approximation on the next level. WPT produces 2^n

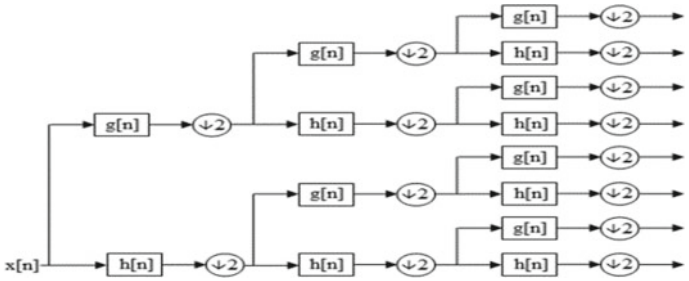

Fig. 5 Wavelet packet transform tree

different sets of coefficients at level *n*. Thus, depending upon the requirements, we can extract different frequency bands details on different levels. The typical wavelet packet tree is shown in Fig. 5.

The data had a sampling frequency of 128 Hz, resulting in maximum frequency contents 0–64 Hz. Signal was decomposed at a different level to obtain down-sampled frequency content. The signals were decomposed up to three levels detail coefficient at the third level were chosen to extract Mu band frequencies.

For the first approach, feature extraction required Shannon entropy [10], which is a statistical feature. Equation 1 shows the formula to calculate Shannon entropy.

$$\mathrm{SE} = -\sum_{i=0}^{N-1} P_i \log_2 P_i \tag{1}$$

Here, P_i is the probability in a given sample class. N is the number of samples in each trial.

Shannon entropy provided entropy values for each class per electrode. The process is repeated for all the trials.

For the second approach, a two-dimensional image is generated out of one-dimensional EEG data. CWT extracts various frequencies available in the signal at any particular point of time. The CWT image contains time and frequency features. In contrast to STFT which is inefficient in interpreting MI signals because of trade-off in resolution between frequency and time [24]. When the width of the time window is short, it shows better resolution in time, but frequency resolution is deteriorated. A large time window results in just the opposite. This issue is addressed using continuous wavelet transform (CWT). Methods used in fourier transform and CWT are similar, but as the fourier transform correlates coefficients between the sinusoidal signal and the original signal on the other hand CWT correlates the original signal with the mother wavelet. However, CWT decomposes signals in the time–frequency domain by scaling and translating the mother wavelet, whereas fourier transforms decomposed the signal just in the frequency domain. In our study, we have used Morlet as mother wavelet. Equation 2 shows a typical CWT operation.

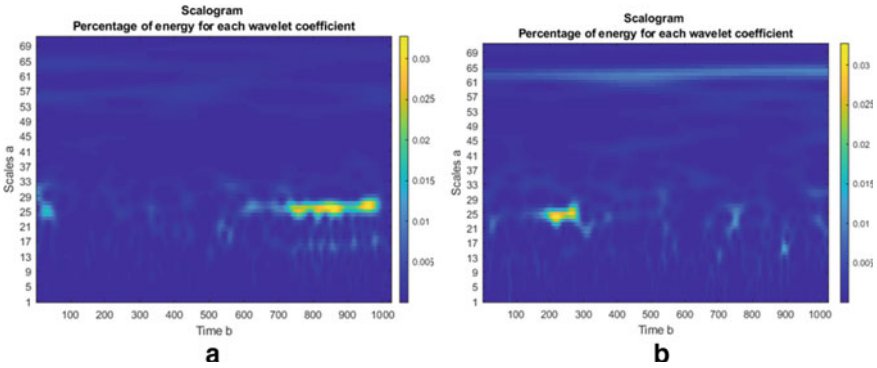

Fig. 6 Scalogram for motor imagery. **a** Right imagery and **b** left hand imagery

$$\mathrm{CWT}(\omega, s) = \frac{1}{\sqrt{|s|}} \int_{-\infty}^{\infty} x(t)\psi\left(\frac{t-\omega}{s}\right)\mathrm{d}t \tag{2}$$

Here, $x(t)$ is motor imagery signal, ψ is the mother wavelet, ω shows time-shifting parameter or translation, and s represents the scaling parameter. The left hand side $CWT(\omega, s)$ denotes the correlation coefficients of the continuous wavelet transform.

After going through CWT, each EEG signal is converted into image representation and saved with their class labels.

Figure 6 shows 2-dimensional images generated from 1-dimensional EEG MI signals for right and left hand, respectively.

Convolutional neural network (CNN) extracts features from the signal image. Every two-dimensional image has some certain features such as curves, edges, and corners, etc. These low-level features then build-up to determine high-level features [25] such as a pattern on a specific location. These features enable the algorithm to identify structures present in the images. Again the process is repeated for each trial.

2.4 Model Training

Both the approaches train model differently. The first approach uses conventional machine learning through which three supervised machine learning classifiers (i) Support Vector Machine (SVM), (ii) K-Nearest Neighbor, and (iii) Linear Discriminant Analysis (LDA). On the other hand for the second approach, we have used transfer learning on top of CNN based deep neural networks. In this approach, we have employed three models (i) alexnet, (ii) vgg16, and (iii) vgg19 and modified them to suit our dataset.

3 Classification

The performance of both approaches was evaluated based on the classification accuracies of the same dataset. Different supervised machine learning techniques used in this study are described below. Both the approaches used 140 trials for training and 140 trials for the testing of the trained model as available in the BCI competition dataset. For the second approach classification techniques, we have used three pre-trained deep learning models. The basic building blocks of most of the deep neural networks are more or less the same as they employ similar layers with some tweaks in parameters and layers arrangement. These differences can be observed by observing their architecture. Our study includes the following pre-trained deep learning models:

All the training data available was used to make results more reliable. The classification methods used in the study are described below:

3.1 Support Vector Machine

Support Vector Machine (SVM) is a classification algorithm that generates a hyperplane in N-dimensional space. Where, N is the number of features in a sample. The objective of hyperplane is to distinctly classify data points. The SVM algorithm tries to maximize the margin between data points and hyperplane.

3.2 K-Nearest Neighbors

K-Nearest Neighbors (KNN) algorithm is based on assumptions that similar things can be classified based on their proximity. Thus, for each new data point, the KNN algorithm looks for the neighboring data points and the class to which they belong. A new data point according to KNN lies in the same class to which its neighbor belongs.

3.3 Linear Discriminant Analysis

Linear Discriminant Analysis (LDA) is a technique for dimensionality reduction. It reduces the number of variables/dimensions in the given dataset as well as retains much of the meaningful information intact. LDA creates a new axis or plain reducing the dimensionality to make different classes separate.

3.4 Alexnet

Alexnet is a deep learning model which consists of 8 main layers (5 convolution layers and 3 fully connected layers). It uses data augmentation to reduce overfitting. It used several different kernel sizes for convolution.

3.5 Vgg16

VGG net was formulated to address the need to reduce the number of parameters used in convolution layers which in turn provides improved training duration. Vgg16 used a fixed kernel of size 3 × 3. Kernel size used in alexnet (11 × 11, 5 × 5, and 3 × 3) were replicated by using multiple 3 × 3 kernels in vgg net.

3.6 Vgg19

Vgg19 is an improved version of vgg16. These networks differ only in the number of layers. vgg19 has 3 more convolution lavers than vgg16. Vgg19 has the same convolution kernel, which is 3 × 3.

4 Results

The results of the study are observed separately for the first and second approaches. Figure 7 shows the comparison of Shannon entropy for both hands in either electrode

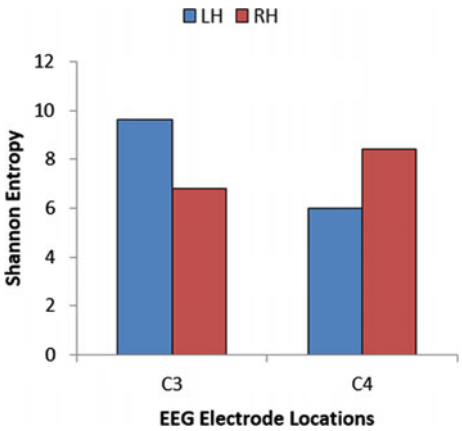

Fig. 7 Comparison of Shannon entropy for both C3 and C4 electrodes for left hand (LH) and right hand (RH) motor imagery

Table 1 Kappa values for classification technique

Classification technique	Vgg19	Vgg16	Alexnet	SVM	KNN	LDA
Kappa	0.89	0.89	0.87	0.73	0.69	0.74

obtained during the first approach.

The results for the first approach were obtained and recorded in Table 2. As table shows LDA has performed the best in terms of classification accuracy but SVM and KNN also performed very well. Even if the accuracies such as 87.1% are high enough, still scope of improvement is there as the human implementation of BCI requires the highest possible accuracy.

In the second approach, the results obtained are shown in Table 3. Obtained results were promising and found out to be as high as 94.29% for the vgg19 model. The results show that the transfer learning approach using deep networks are proven to be more effective than conventional machine learning approaches. Kappa values, which is used to estimate the interrater reliability of an algorithm. Based on the obtained results, Kappa values for all six classification methods were compared and summarized in Table 1. Table 1 also visualizes the effectiveness of transfer learning methods for the aforementioned datasets. All the transfer learning methods have Kappa values more than 0.87 which is a great improvement over conventional methods having the most Kappa value 0.74.

5 Discussion and Conclusion

In the present study, aforementioned features were extracted from EEG dataset BCI competition II dataset III. After preprocessing the data, two different approaches were used to compare their classification efficiency of both the approaches separately for both the datasets. Different feature extraction techniques were used for respective approaches. Shannon entropy and CWT along with CNN were used, respectively, to extract features, respectively. Finally, the features were then used to train classification models. The total sample size of 280 was divided into half for training and testing purposes. The results were shown in Tables 1, 2, and 3. Table 4 shows some previous works based on the same dataset.

The study shows that deep learning methods (alexnet, vgg16, and vgg19) worked better than conventional machine learning (SVM, KNN, and LDA). The Kappa values in Table 1 show deep learning methods have outperformed conventional methods for the same dataset. It should be noted that deep learning methods have larger training

Table 2 Classification accuracies for different classifier using Shannon entropy

Feature	Classification accuracy (%)		
	SVM	KNN	LDA
Shannon entropy (SE)	86.4%	84.3%	87.1%

Table 3 Classification accuracies for different classifier using Shannon entropy

Feature	Classification accuracy (%)		
	Alexnet	Vgg16	Vgg19
CNN	93.57%	94.29%	94.29%

Table 4 Notable previous research work is done with the same dataset

Authors	Method used	Classification acc. (%)
Bhattacharyya et al.	Average band power of alpha and beta with KNN	84.29
Liu et al.	Common spatial pattern (CSP) with SVM	82.86
Tae-Ung Jang et al.	STFT with K-nearest neighbor	83.57
Tabar and Halici	STFT with deep learning	90
Samira Vafay Eslahi et al.	Genetic Algorithm based optimization with FKNN, LDA	84
Kant et al.	Wavelet transform with Shannon entropy using SVM and KNN	86.4

time for a particular model. In our work with the first approach, all three classifiers took less than 15 s and the second approach with deep learning took 2 min and 29 s at most [alexnet (1 min 39 s), vgg16 (2 min 13 s), and vgg19 (2 min 29 s)] for training. However, once trained the model can classify a new sample within seconds for each classification technique. And with the arrival of faster and faster processors, deep networks are best-suited techniques for BCI implementation.

The works have also determined the efficient classifiers for each of the first, and the second approach. LDA (87.1%) has classified better than SVM (86.4%) and KNN (84.3%) in their experiment, while vgg19, vgg16 provided the same classification accuracy (94.29%) and proven better than alexnet (93.57%) in our particular experiments. The work establishes the effectiveness of deep neural networks over conventional machine learning techniques that have at least a 6% improvement over the first approach's the best classification accuracy.

It may be noted that the accuracy of these classifiers may also differ for different datasets and some other preprocessing or filtering techniques. Alpha/Mu band in our case provided conclusive pieces of evidence for our study to determine the effectiveness of particular approaches in order to be used in further studies.

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