Comparative Analysis of a Gradationally Controlled Voltage Inverter

V. Aishwarya and K. Gnana Sheela

Abstract This paper describes a high-efficiency gradationally controlled voltage inverter (GCVI) that outputs a high-quality waveform at very low switching frequencies. This inverter employs multiple inverters with a DC-link voltage that holds a binary/ternary ratio with each other and is series-connected to output the arithmetic summation of their voltage outputs. The resultant output voltage waveform approaches a near sinusoidal shape with an increase in voltage output levels. The properties of GCVI are reduced output voltage distortion, decreased power-loss, small output filters, reduced electromagnetic noise due to reduced dV/dt, and an AC voltage output much greater than the input DC voltage the GCVI. The MATLAB simulation of a 13-level GCVI is presented, and the advantages of a 13-level GCVI over the conventional 13-level cascaded H-bridge inverter are highlighted. The proposed 13-level GCVI achieves a greater voltage output of 130 V, with 97.74% fundamental component and a near sinusoidal wave-shape with voltage distortion of 3.11%, inside the tolerable range of IEEE 519-2014 standard.

Keywords Asymmetrical cascaded H-bridge inverter · Bit-to-bit energy transfer control · Gradationally controlled voltage inverter · Multilevel inverter · Power loss · Total harmonic distortion

1 Introduction

Multilevel inverters (MLIs) are popularly employed in sustainable energy systems, including solar and wind, speed control of motor drives, static VAR compensation, etc. Multilevel inverters are considered as the state-of-the-art technology due to its innumerable advantages like improved waveform quality, reduced switch count, higher voltage output, minimal passive filter requirement, reduced dV/dt stress, lesser electromagnetic interference, reduced torque ripple in motor drives, ability to operate at higher voltages with reduced active switches, and fault-tolerant operation [1–4].

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The active switches of the MLI topologies are triggered using a broad range of modulation techniques. These techniques include space vector PWM, pulse width modulation (PWM), selective harmonic elimination, etc. [5]. The quality of the voltage output waveform depends directly on the harmonic content. The harmonic content varies depending on the MLI topology and modulation methods [1, 5–8].

The objective of an MLI is to develop a voltage output with a near sinusoidal waveshape with proper switching of the active switches and selection of isolated/non-isolated DC sources [9]. With an increase in voltage output waveform levels, a purely sinusoidal voltage is obtained, eliminating the need for bulky transformers and high-cost filters [9, 10]. In the current scenario, achieving a higher voltage output with the highest quality waveform is the need of the hour.

The comparative analysis of the proposed gradationally controlled voltage inverter (GCVI) with different conventional MLIs is presented in this paper. GCVIs find numerous applications as voltage sag compensators, UPS, power conditioners, etc. This novel inverter is an asymmetric cascaded H-bridge inverter that holds a binary (1:2:4)/ternary (1:3:9) voltage ratio with each of its bits, i.e., the DC-link voltages of the individual cells have a binary ratio relationship with each other. The net voltage output is regulated by altering the combinations of these voltages [11].

The organization of the paper is as follows: Sect. 2 deals with the drive schematic; Sects. 3 and 4 describe the working of the SCBB converter and drive control. Section 5 describes the simulation results and discussions, and Sect. 6 presents the conclusion of the paper.

2 Gradationally Controlled Voltage Inverter

The GCVI comprises multiple voltage-fed inverters connected in series, with different DC output voltages. The inverter DC voltages have binary (1:2:4)/ternary (1:3:9) ratios with one another [12]. It generates a voltage with a sinusoidal waveform by summing these voltage outputs. The net voltage output is regulated by altering the combinations of these voltages [11, 13, 14]. In a 3-bit binary GCVI, it generates 15 bipolar-levels of voltage, and in 3-bit ternary GCVI, it generates 27 levels of voltage [11, 14, 15]. Figure 1 depicts the circuit schematic of a GCVI. Gradational voltage control is a new technique to minimize energy losses in inverters. Gradationally controlled voltage inverter is a type of asymmetrical cascaded H-bridge with one main inverter and two sub-inverters, each one with double (or triple) the voltage, connected in series. Their outputs are combined to get a near sine wave. It has a better response than conventional MLI; here, a single unit controls a whole voltage range, decreasing power-loss. Unlike PWM, which alters the voltage by turning the semiconductor on and off to change the output time without changing the size of the DC source voltage, gradational voltage control provides extremely high power conversion efficiencies. Hence, it has captured attention as the next-generation inverter capable of accelerating energy conservation efforts.

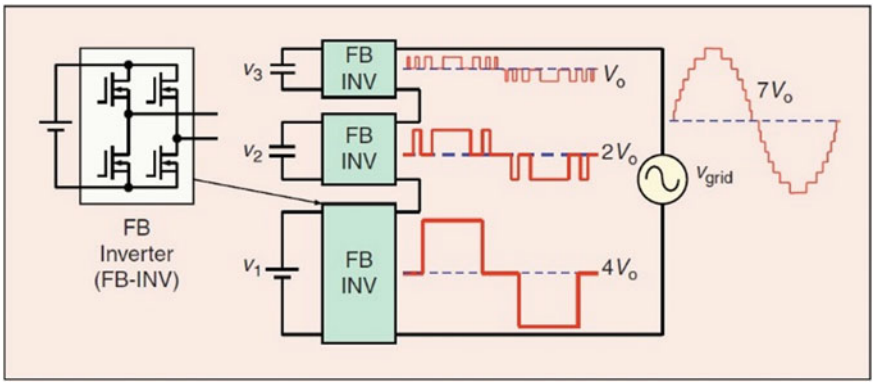

Fig. 1 Gradationally controlled voltage inverter (GCVI) [13]

3 Operating Principle of a GCVI

A GCVI includes the main inverter and a few sub-inverters. The inverter cells are known as bit-inverters and are known as Bit 1 (1B), Bit 2 (2B), etc., in the ascending order of voltage [12, 15]. The steps in the voltage output waveform of a GCVI are called gradations.

A binary 3-bit GCVI outputs 7-voltage levels in one half-cycle or a total of 15-voltage levels, including 0 in one full-cycle of AC voltage output. A ternary 3-bit GCVI output 13-voltage levels in one half-cycle or 27-voltage levels, including 0 in one full-cycle of AC voltage output [12]. The most highlighting characteristic of a GCVI is its capability to decrease the switching frequencies significantly. For example, in a binary 3-bit GCVI, 3B conducts one time in each fundamental AC output voltage cycle. 2B and 1B conducts 3 times and 7 times, respectively. Thus, the switching loss is significantly minimized relative to conventional PWM inverters [11, 12]. As the bit-inverters are rated at different input DC voltages, a separate power device that achieves the smallest possible loss for bit-inverter is used [11, 12]. Since harmonic components are minimal in the voltage output of the GCVI, noise filters are eliminated [15].

3.1 Concept of Energy Transfer and Control

While generating a stepped AC wave, the GCVI executes energy transfer control when transferring energy from the highest-voltage bit-inverter to the fellow bits [12, 15]. By employing this control, only the highest-voltage bit requires a DC source. It leads to equipment simplicity and economization. Table 1 presents the concept of energy transfer control among the bits. Figure 2 depicts a 3-bit, ternary GCVI. It outputs seven voltage levels in a half-cycle of AC voltage output. For example,

Table 1 Total voltage output level and bit-inverter voltages of a 2-bit binary GCVI

Output level		B3:$4V_o$	B2:$2V_o$	B1:V_o
I	1	0	0	V_o
	2	0	$2V_o$	$-V_o$
	3	$4V_o$	$-2V_o$	$-V_o$
II	1	0	$2V_o$	0
	2	$4V_o$	$-2V_o$	0
III	1	0	$2V_o$	V_o
	2	$4V_o$	0	$-V_o$
	3	$4V_o$	$-2V_o$	V_o
IV	1	$4V_o$	0	0
V	1	$4V_o$	0	$-V_o$
	2	$4V_o$	$2V_o$	$-V_o$
VI	1	$4V_o$	$2V_o$	0
VII	1	$4V_o$	$2V_o$	V_o

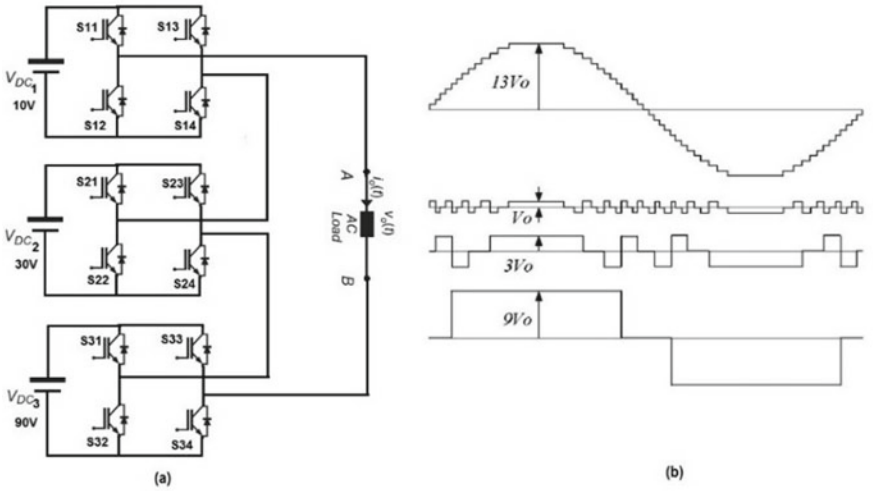

Fig. 2 **a** Circuit schematic of a ternary GCVI. **b** Waveforms of a ternary GCVI

when the inverter outputs V_o, the three selected combinations are (0, 0, V_o), (0, $2V_o$, $-V_o$), and ($4V_o$, $-2V_o$, $-V_o$) [14]. When the combination ($4V_o$, $-2V_o$, $-V_o$) is selected, the main inverter delivers energy to the bit-inverters. In this way, the GCVI delivers energy from the main inverter to the bit-inverters while it generates AC output power [14]. As presented in Table 1, there is a plurality of combinations of bit-inverter voltage outputs for each of the inverter voltage output. The polarity of load current is assumed positive. The bit-inverters that output a positive voltage and

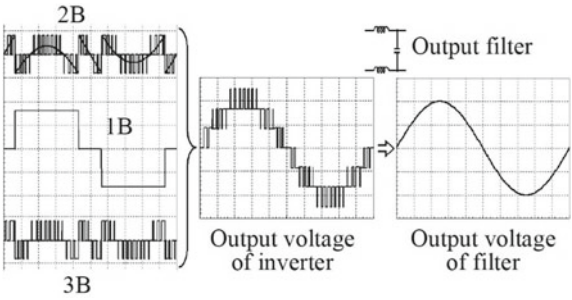

Fig. 3 Generation of voltage output in a GCVI [14]

a negative voltage behave like they discharge energy from and charge energy into the DC capacitor, respectively [12, 15]. By gradationally regulating these two working modes of charging and discharging, it is possible to cede the mean output power of the bit-inverters zero [13]. The switching sequence for the active switches in the main inverter and sub-inverters is generated using the level-shifted PWM method [5]. A gradationally controlled voltage inverter has the following features [14]:

1. Reduced power-loss and electromagnetic noise relative to a traditional PWM inverter.
2. Small output filter size as the voltage switched by each cell is less. It makes the GCVI lightweight and compact.
3. A GCVI generates a high AC output voltage greater than the input DC voltage.

3.2 Ternary Gradationally Controlled Voltage Inverter

The ternary number GCVI (Fig. 3) comprises three series-connected H-bridge inverters whose voltage outputs are different. The DC-link voltages of the bit-inverters have ternary (1:3:9) ratios with each other. The net voltage output is regulated by altering the combinations of the bit-inverter DC-link voltages [11].

Figure 2 depicts the circuit schematic and associated waveforms of a ternary GCVI. Table 2 presents the total voltage output level and the voltage outputs of the bit-inverters. In a ternary GCVI, the inverter generates 13-levels in one half-cycle or 27 levels, including zero in one full-cycle of the fundamental AC output voltage wave [11]. Hence, the inverter outputs a stair-cased waveform, and the harmonic contents in the voltage output are significantly decreased. It, in turn, reduces the size of the LC filter [12, 15].

The most highlighting characteristic of a GCVI is its capability to minimize the switching frequencies considerably. When outputting a simple sinusoidal voltage, the main H-bridge inverter with $9V_o$ conducts only once. For each cycle, bit-inverter with $3V_o$ and the bit-inverter with V_o conduct 5 times and 17 times, respectively [11, 12, 15]. Therefore, relative to traditional PWM inverters, there is a drastic reduction in the switching power losses. Since the bit-inverters have different DC-link voltages, a power device that achieves the least power-loss for each bit-inverter is employed.

Table 2 Total output voltage and bit-inverter voltages of a 3-bit, ternary GCVI

Output voltage level	B1:V_o	B2:3V_o	B3:9V_o
V_o	$+V_o$	0	0
$2V_o$	$-V_o$	$+3V_o$	0
$3V_o$	0	$+3V_o$	0
$4V_o$	$+V_o$	$+3V_o$	0
$5V_o$	$-V_o$	$-3V_o$	$+9V_o$
$6V_o$	0	$-3V_o$	$+9V_o$
$7V_o$	$+V_o$	$-3V_o$	$+9V_o$
$8V_o$	$-V_o$	0	$+9V_o$
$9V_o$	0	0	$+9V_o$
$10V_o$	$+V_o$	0	$+9V_o$
$11V_o$	$-V_o$	$+3V_o$	$+9V_o$
$12V_o$	0	$+3V_o$	$+9V_o$
$13V_o$	$+V_o$	$+3V_o$	$+9V_o$

Hence, the power-losses in all the switches decrease, and the heat sink's size is minimized [11, 12, 15]. Table 2 portrays the total output voltage and bit-inverter voltages of a 3-bit ternary GCVI.

3.3 Techniques of Delivering Energy to Bit-Inverters

The GCVI comprises three series-connected inverters. The main inverter (Bit inverter 1B) receives energy directly from the DC/DC converter output terminals, whereas the bit-inverters (2B, 3B) receives energy using an indirect method [14].

The voltage of a bit-inverter is regulated within a particular set value by switching the small DC/DC converter formed between each bit-inverter and the main inverter and controlling the conducting time of the main inverter [14]. Since each bit-inverter's output power is zero, by varying the conduction-time of the main inverter (1B), the size of the DC/DC converter required and power-loss is greatly minimized [14]. Figure 3 depicts the method of generation of voltage output in a GCVI.

As represented in Fig. 4, the main inverter (1B) generates an output voltage one time in a half-cycle. The DC-link voltages of the bit-inverters 2B and 3B are equal, and they employ PWM control to generate their voltage output, so that the difference between these voltages and main inverter voltage output (1B) is compensated for [14].

The output power (P_o) of GCVI is made equal to that of the main inverter (1B) output power (P_{in}) by adjusting the pulse width of the main inverter (1B). This condition of the pulse width yields total bit-inverter energy as zero [14].

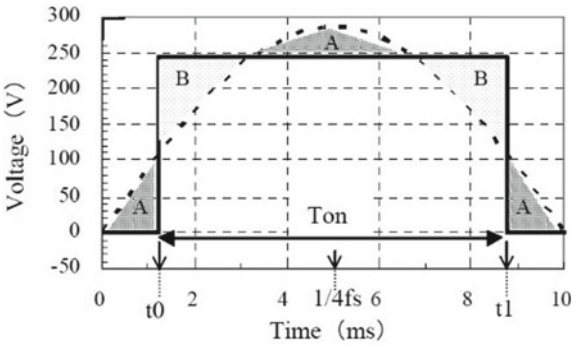

Fig. 4 Method of generation of output voltage in a GCVI [14]

$$P_{\mathrm{o}} = \frac{V_{\mathrm{m}} I_{\mathrm{m}}}{2} \tag{1}$$

$$P_{1\mathrm{B}} = 4 f_{\mathrm{s}} \int_{t_{\mathrm{o}}}^{1/4 f_{\mathrm{s}}} V_{\mathrm{in}} I_{\mathrm{m}} \sin(2\pi f_{\mathrm{s}} t) \tag{2}$$

where V_{m} is the peak output AC voltage, I_{m} is the peak output AC current, V_{in} is the input voltage supplied to inverter 1B, and f_{s} is the voltage output frequency.

4 Simulation Results and Discussions

The conventional 3-bit cascaded H-bridge inverter, binary number 3-bit GCVI, and the Ternary GCVI are simulated using MATLAB/Simulink software. Figure 5 represents the voltage output waveforms of the 27-level GCVI, respectively. As the number of output voltage levels increases, the harmonic contents in the output voltage decrease, and there is a sharp increase in the value of the fundamental component of the output voltage. It is validated by the Fourier analysis of the 27-level voltage

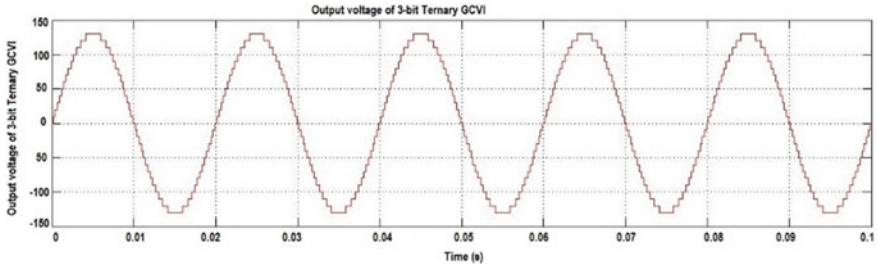

Fig. 5 Output voltage of 3-bit ternary GCVI

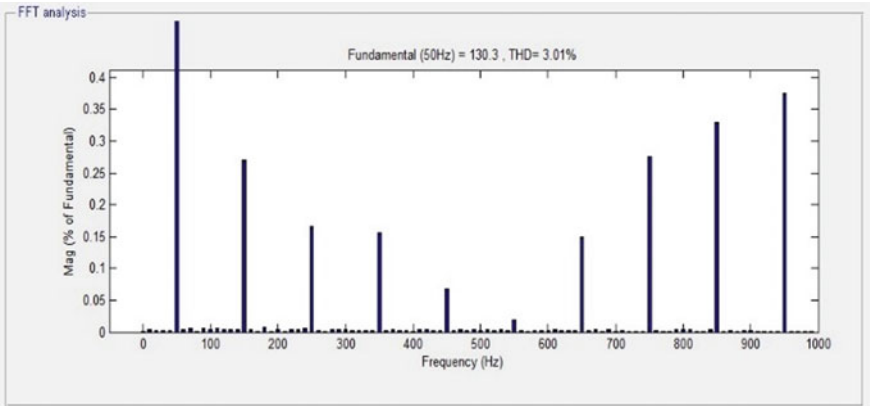

Fig. 6 FFT analysis of 3-bit ternary GCVI

output waveform of a ternary GCVI shown in Fig. 2a. Figure 6 illustrates the selected signal and FFT analysis of the 27-level ternary GCVI, respectively.

It is observed that the 27-level 3-bit GCVI has the least total harmonic distortion (THD) of 3.00%, and a fundamental component of 130.3 V (peak value) in the output voltage, compared to that of the conventional 3-bit cascaded H-bridge (CHB) inverter, which has a THD% of 13.14% with a fundamental component of 21.42 V (peak value).

5 Comparative Analysis

A simulation study was conducted on the four types of MLIs, namely proposed 27-level 3-bit ternary GCVI, conventional 7-level 3-bit CHB-MLI, traditional 3-level diode-clamped MLI, and flying capacitor MLI. Table 3 presents a detailed comparative analysis of these four types of MLIs based on no. of voltage output levels, no. of DC sources, no. of switches, no. of clamping diodes, no. of clamping capacitors, and no. of DC-bus capacitors. It is observed that the proposed 27-level, 3-bit ternary GCVI has the least harmonic distortion of 3.01% in the output voltage, relative to other types of MLIs. Also, the GCVI achieves 27 levels in the voltage output, which is four times the output voltage levels of its counterparts, utilizing a minimum number of passive and active components. Relative to a conventional 7-level 3-bit CHB-MLI, the GCVI achieves a greater output voltage of 130 V, lowest THD% of 3.01%, with the same count of DC sources and active switches.

Table 3 Comparison of proposed GCVI with different multilevel inverters (MLI)

S. No.	Parameters	7-level 3-bit cascaded H-bridge MLI [4]	7-level diode-clamped MLI [1]	7-level flying capacitor MLI [6]	27-level 3-bit ternary GCVI
1	No. of levels in output voltage	7	7	7	27
2	No. of switches	12	12	12	12
3	No. of clamping diodes	0	30	0	0
4	No. of clamping capacitors	0	0	30	0
5	No. of DC-bus capacitors	0	6	6	0
6	No. of DC sources	3	1	1	3
7	Output voltage if $V_{dc} = 10$ V (V)	30	30	30	130
8	Harmonic distortion of output voltage (%)	13.14	12	16	3

6 Conclusion

This paper explains the comparative analysis of a GCVI with conventional MLI topologies. The concept and operating principle of a GCVI are described. Simulation and analysis of the three types of inverters have also been explained. A GCVI offers reduced power-loss, lesser electromagnetic noise, small and compact output filters, and produces an AC voltage output larger than the DC voltage input of the GCVI. Moreover, the technique of delivering energy from the DC input power to the bit-inverters floating from a ground electric potential is also obtained. It is shown that a 27-level, 3-bit GCVI has a high fundamental component of 130.3 V (peak value) and a very low THD of 3.01%, with a near sinusoidal wave-shape. The harmonic voltage distortion is inside the tolerable range of IEEE 519-2014 standard. Based on the comparative analysis of a 27-level 3-bit ternary GCVI with different existing multilevel inverter topologies, it is observed that the GCVI attains a least output voltage distortion of 3.01%, higher output voltage of 130 V with the same number of switches and no additional components, compared to its other MLI counterparts. Thus, the performance of the proposed 27-level 3-bit ternary GCVI supersedes the performance of its existing MLI counterparts.

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