

20W Multi-output Isolated Power Supply Using Secondary Regulated Flyback Topology



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1 Introduction

In linear power supplies, semiconductor devices operate in the linear region. To maintain the constant voltage across the load, the load current is varied by changing the base or gate drive of the semiconductor devices. This results in increased power dissipation across the device, thus increasing the conduction losses resulting into poor system efficiency. Thus, the linear power supplies are suitable only for low-power applications [1].

In switched-mode power supplies (SMPS), the power semiconductor device operates in cut-off or saturation region. Thus, the major disadvantage of linear power supplies regarding lower efficiency is overcome by SMPS [2]. So, the flyback topology is preferred in low and medium power offline applications which provides higher efficiency compared to linear power supplies [3]. A secondary regulated current-controlled closed loop 20 W, 200–400 V, flyback-based SMPS suitable to drive an H-bridge is designed and developed.

The closed loop configuration consists of a flyback transformer, output filter, PWM IC UCC28C44DR and opto-isolator LIA130S. In the proposed system, opto-isolator monitors the secondary winding voltage, and if it deviates from the reference voltage due to changes in the supply voltage, output current variation due to change in load, temperature variation is considered as error. This error is fed back to PWM IC, and duty cycle is varied to maintain the constant output voltage.

The paper organized in VII sections. Section 1 gives introduction, and Sect. 2 deals with basics of flyback converter. System overview and design considerations

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are discussed in Sect. 3. Section 4 deals with protection circuits and designing a closed loop converter. Section 5 provides the simulation and hardware results. Section 6 will conclude the design.

2 Flyback Converter

The basic block diagram of flyback converter is as in Fig. 1. The DC input voltage is obtained by rectifying sinusoidal alternating voltage. Flyback converter works on the principle of coupled inductor mechanism due to which the induced voltage depends on inductance and rate of change of current. Since in the DC supply rate of change of current is zero, voltage will not be induced. Thus, a switch is included in the primary of the flyback converter and is triggered such that induced voltage is nonzero. For the generation of pulsating DC supply in the converter, the primary switch is switched on and off at certain switching frequency using gate pulses. The coupled inductor configuration helps to adopt the necessary polarity by changing the dot position and diode orientation. This also provides the galvanic isolation between the mains and connected loads. By adjusting the turns ratio of the flyback transformer, the output voltage could be stepped up or down with respect to the input voltage.

The flyback operation can be classified into two modes of operation, i.e. continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

In CCM, transformer does not dissipate all the stored energy to secondary. So, the current in the primary side of inductor never falls to zero. This mode is used in high-current, low-voltage applications.

In DCM transformer dissipates all the stored energy to secondary. So, the current in the primary side of inductor falls to zero during each cycle. This mode is used in low-current, high-voltage applications.

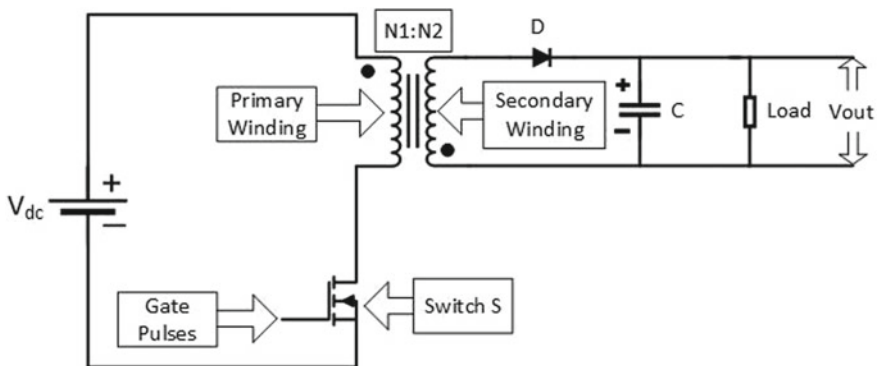


Fig. 1 Basic diagram of flyback converter

In proposed design, flyback is implemented using DCM operation. This DCM operation depends on the on and off condition of primary switch as well as secondary diode.

3 System Overview

The block diagram of the proposed system is as in Fig. 2; it is specifically designed to drive an H-bridge switches used to drive a stepper motor. Since the H-bridge switches require the gate turn-on voltage between 15 and 20 V, flyback auxiliary supply is designed for 15 V.

The purpose of each flyback winding is listed in Table 1. The PWM IC UCC28C44DR can withstand a maximum supply voltage of 18 V, and an auxiliary

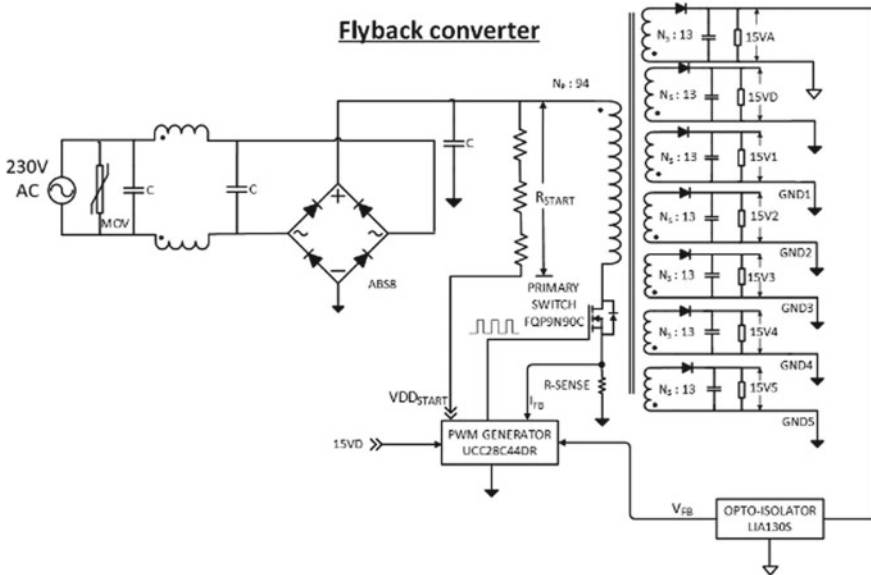


Fig. 2 Block diagram

Table 1 Purpose of flyback windings

S. No	Winding	Power	Purpose
1	15VD	1 W	Supply for PWM IC
2	15VA	1 W	Feedback to opto-isolator
3	15V1,15V2,15V3,15V4	1 W	For H-bridge TOP switches
4	15V5	4 W	For H-bridge BOTTOM switches

supply of 15VD is generated to power the PWM IC. However, in order to protect the PWM IC from over voltage, a Zener diode of 18 V is used. The regulation winding, 15VA, is fed back to opto-isolator LIA130S.

The proposed system has the DC input voltage range from 200 and 400 V. The system is operated with a switching frequency of 50 kHz and is capable of delivering 20 W.

The universal AC input is given to the rectifier through EMI filter to minimize the high-frequency noise present in power lines. It also protects the circuit from noise in the signal transmission and ensures the intended performance of electrical equipment. The diode bridge rectifier converts AC supply to DC. Metal Oxide Varistor (MOV) is used to protect the system from transient voltages.

The proposed flyback converter has two control loops. The first being the outer voltage loop and later is inner current loop. The instantaneous current of the circuit is sensed using R_{SENSE} resistor. R_{START} is the star-tup circuit that provides the initial supply to PWM IC till it gets sufficient voltage from auxiliary winding of the converter.

To regulate the output to 15 V irrespective of input voltage or load variations, feedback is provided to a PWM IC via LIA130S opto-isolator as in Fig. 2. The PWM controller has error amplifier which provides the control signal to the current mode controller. For the stable and satisfactory dynamic response, precision feedback components must be used in the design.

The parameter specification for flyback converter is as in Table 2.

Converter with higher switching frequency, size of magnetics and filters become smaller. However, core loss, gate charge current and switching losses increase. Lower switching frequency results in higher peak currents and conduction losses. A compromise between component size, current levels and losses must be made by the designer in choosing the switching frequency. In this design, a switching frequency of 50 kHz is chosen.

Leakage inductance is caused by imperfect coupling between primary and secondary of the transformer. Leakage inductance appears in series with the MOSFET when it is turned off. This results in turn-off spikes and ringing across the device and might cause damage to the MOSFET. The design procedure followed and values obtained for 20 W flyback converter are listed in Table 3.

Based on inductance requirement, EE 30/15/7 core with $A_c A_w$ of 7700 mm⁴ and A_e of 57.3 mm² is chosen. Based on A_e value, primary and secondary turns calculated for each winding as listed in Table 4.

Table 2 Parameter specification for flyback converter

Parameter	Specification
Input voltage	200–400 V DC
Maximum output power (P_o)	20 W
Switching frequency (f_s)	50 kHz
Output voltage	15 V

Table 3 Design calculation

S. No.	Component	Formula	Value
1	Primary side inductance	$L_m = \frac{(V_{dc(min)} D_{max})^2}{2P_{in} F_s K_{rf}}$	1.92 mH
2	Maximum peak current of MOSFET	$I_{d(peak)} = I_{EDC} + \frac{\Delta I}{2}$	0.834 A
3	Core window product area	$A_c A_w = \frac{V_1 I_1}{2K_w B_m J F_s}$	2213 mm ⁴
4	Primary turns	$N_{p(min)} = \frac{L_m I_{over}}{B_s A_e}$	94
5	Turns ratio	$n = \frac{N_p}{N_{s1}} = \frac{V_{RO}}{V_{O1} + V_{F1}}$	7.45
6	Secondary turns 15 V	$N_{S1} = \frac{N_p}{n}$	13
7	Cross-sectional area of winding	$A = \frac{I}{J}$	0.0166 m ² (Primary) 0.022 m ² (1 W) 0.089 m ² (4 W)
8	Strands for primary winding	$P_{strand} = \frac{A}{0.0591}$	1 (Primary) 1 (1 W) 2 (4 W)

Table 4 Winding parameters with EE core of 30/15/7

S. No.	Winding	Voltage	No. of turns	Wire gauge
1	Primary	400	94	SWG32X1
2	Secondary	15 (1 W)	13	SWG32X1
3	Secondary	15 (4 W)	13	SWG32X2

Lower forward drop of Schottky diodes improves the converter efficiency due to reduced conduction losses in comparison with silicon diodes. Schottky is selected based on peak reverse voltage rating, peak repetitive forward current and average forward current rating of the device.

The peak reverse voltage that the device will be subjected to is as in (1):

$$V_{rpk} = n V_{in(max)} - V_{drop(FET)} \quad (1)$$

Winding technique is another important and critical parameter in flyback converter. Poorly designed flyback transformer will reduce the converter efficiency. The winding pattern followed in the design is as in Fig. 3.

The major consideration in the EE core bobbin is to ensure the proper creepage distance between primary and secondary pins. The procedure followed for the winding is as follows:

1. Primary winding is the first winding on the bobbin. Since this winding is connected to the drain of the MOSFET, this ensures the point with maximum voltage swing will be shielded by other winding so that EMI is reduced. Primary

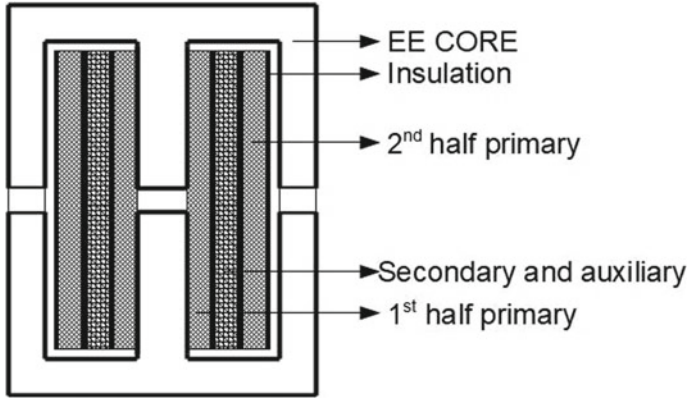


Fig. 3 Flyback transformer layout

winding is split into two separate windings so that leakage inductance is reduced by increasing coupling between primary and all bias windings.

2. Three layers of insulation are placed between primary and secondary windings in order to reduce the possibility of breakdown between the layers and also to reduce the interwinding capacitance between primary.
3. All the bias windings are placed on top of the primary insulation.
4. Three layers of basic insulation are placed on top of the secondary windings in order to pass the safety standards for electrical strength requirements.
5. Remaining primary winding is wound, and three layers of basic insulation are placed.

By following the above procedure, leakage inductance measured is less than 2% of primary inductance.

4 Protection Circuits and Design of Closed Loop

During the primary switch turn off process, ringing in the voltage across MOSFET will be observed due to primary inductance, leakage inductance and output capacitance. The ringing frequency could be written as in (2):

$$f_{\text{ring}} = \frac{1}{2 * \pi * \sqrt{((L_{\text{leak}} + L_m) * C_{\text{out(MOSFET)})}} \quad (2)$$

Since the output capacitance and primary inductance are fixed, leakage inductance will contribute more to the amplitude and ringing frequency.

MOSFET snubber circuit is necessary in order to clamp the ringing voltage caused by leakage inductance. The snubber should be designed such that the voltage across

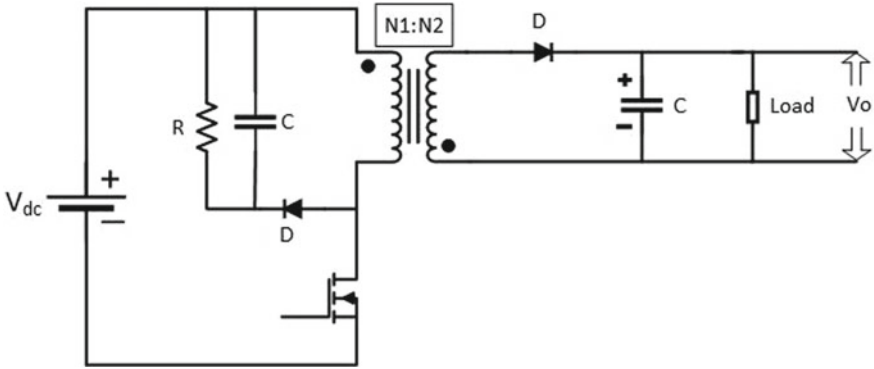


Fig. 4 RCD snubber clamping

the switch is less than the breakdown voltage. Two widely used snubber circuits are RCD clamping and Zener or transil clamping.

The RCD snubber consists of high voltage diode D, high voltage capacitor C and resistor R as in Fig. 4. RCD network absorbs the current in the leakage inductance by turning on the snubber diode after particular voltage, and thus, it will charge the capacitor C. Thus, the ringing may be damped to a level lower than the circuit without snubber. The snubber capacitor C is large enough that its voltage does not change significantly during one switching cycle. RCD clamp is a cheaper solution; however, it dissipates power even under no-load conditions. There is at least the reflected voltage V_R across the clamp resistor at all times.

Another easy solution is Zener clamping in which TVS diode is used to clamp the ringing voltage as in Fig. 5. The TVS diode is connected in series with a reverse polarity diode. The TVS must clamp the voltage to sum of reflected voltage and input voltage. It will dissipate all the power as clamping resistor. However, the cost

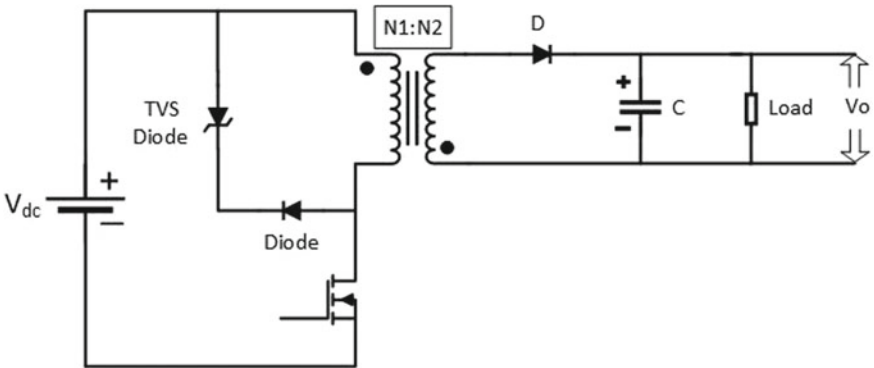


Fig. 5 TVS diode clamping

of the components is more compared to RCD clamping. It gives a better and defined clamping level but dissipates more power at full load.

In flyback converter, the clamping circuit is connected across primary winding, and the device rating must be larger than the sum of reflected voltage and voltage caused by leakage inductance. The RCD clamping frequently fails during transient conditions, and TVS clamping gives good dynamic response. In the proposed circuit, TVS diode clamping is employed.

The transformer leakage inductance also causes ringing and overshoot in the secondary diode. Leakage inductance and diode output capacitance form the resonant circuit. In order to damp out the oscillations, RC snubber is used across the secondary diode. The ringing frequency on the secondary side (without snubber) is determined by the resonant tank frequency created by the reflected leakage inductance and the junction capacitance of the output diode. The ringing frequency is written as in (3):

$$f_{\text{ring}} = \frac{1}{2 * \pi * \sqrt{(L_{\text{leak}} * C_{\text{junction(diode)}})}} = 3.82 \text{ MHz} \quad (3)$$

where $C_{\text{junction(diode)}} = 12 \text{ pF}$ and $L_{\text{leak}} = 2\%$ of L_m .

For making Q factor near to 1, snubber capacitance must be at least three times the output capacitance of the diode as in (4), and to provide critical damping, the snubber resistor could be computed as in (5):

$$C_{\text{snub}} = 3 * C_{\text{out(diode)}} = 135 \text{ pF} \quad (4)$$

$$R_{\text{snub}} = \sqrt{\frac{L_{\text{leak}}}{N^2} \frac{1}{C_{\text{out(diode)}}}} = 19 \Omega \quad (5)$$

Switching frequency of the converter decides the filter requirement of any converter. To achieve higher power density and reduced system size, converter needs to operate with higher frequency. The rapid switching of currents in the converter leads to conducted and radiated electromagnetic interference (EMI).

Conducted EMI is classified as common mode and differential mode. Common mode noise essentially occurs by electromagnetic coupling, and differential noise occurs by pulsating currents. In the proposed system, Π filter is used at the input and output in order to reduce the noise.

In this design, two ICs such as PWM controller UCC28C44DR of Texas Instruments and Littlefuse opto-isolator LIA130S are used. PWM controller is used to provide the gate signals to the primary switch as well as maintain the constant output voltage by adjusting the duty ratio, and opto-isolator is used to provide the isolation between measured signal and the controller.

Start-up circuit is used to provide the supply to the controller until MOSFET gets the required pulses from PWM IC. At power on, the current is delivered to the IC by start-up resistors, and once the capacitor voltage reaches under voltage lockout level,

the IC starts to give gate pulses. Then, the controller takes the supply from auxiliary winding. PWM IC UCC28C44DR has RT/CT pin to select the necessary switching frequency, and system has been designed to operate at a switching frequency of 50 kHz.

The current in the primary winding is converted to voltage signal by connecting R_{SENSE} resistor and given to CS pin of PWM IC. The IC will stop generating the gate pulses if set overcurrent limit is reached. The R_{SENSE} resistor is calculated as in (6):

$$I_{SENSE} = \frac{V}{R_{SENSE}} \quad (6)$$

Slope compensation is required in closed loop current-controlled systems when the duty cycle exceeds 50% else inductor current will oscillate at half the switching frequency.

Slope compensation fixes these problems by adding ramp to the current signal and helps in damping out the oscillations.

Regulated output of winding is calculated using potential divider circuit as in Fig. 6.

To select potential divider values, (7) and (8) are used

$$R_{upper} > \frac{V - V_{ref}}{80 \mu A} \quad (7)$$

where $V_{ref} = 1.24 \text{ V}$ and $80 \mu A$ is input offset current for LIA130S.

$$\frac{R_{upper}}{R_{lower}} = \frac{V}{V_{ref}} - 1 \quad (8)$$

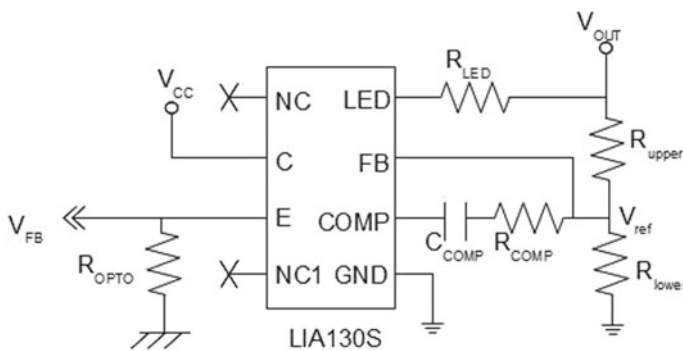


Fig. 6 Opto-isolator circuit diagram

5 Simulation and Hardware Results

To validate the proposed design considerations, simulation as well as experimental tests is carried out. The proposed system works well at input DC voltage of 400 V. Feedback control is necessary in order to remove the error in the output. The closed loop simulation is carried out as in Fig. 7.

The output voltage of 15 V is as in Fig. 8. It is clearly seen that the curve is smooth and oscillations are removed. Error in the output voltage is removed using closed loop configuration.

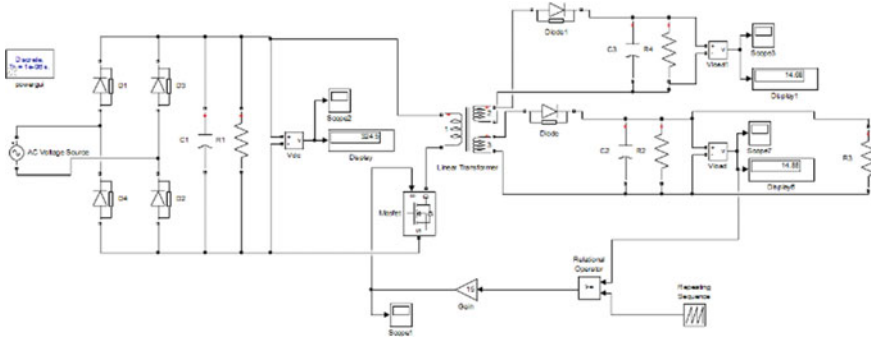


Fig. 7 Simulink model of closed loop flyback converter

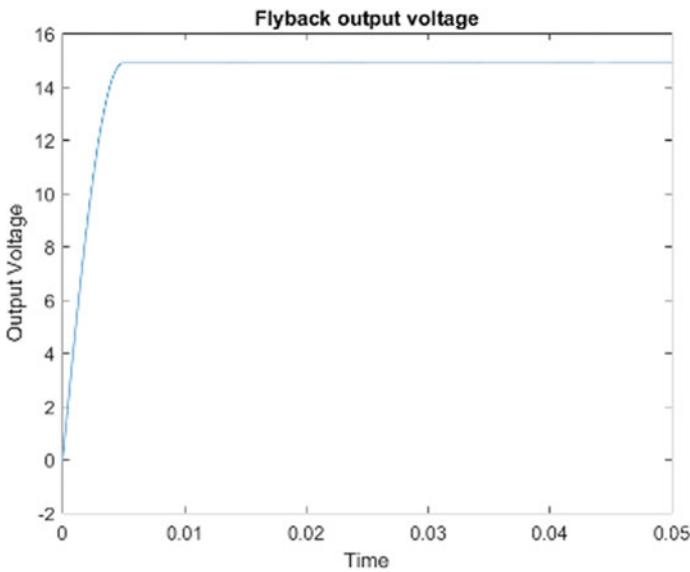


Fig. 8 15 V output voltage

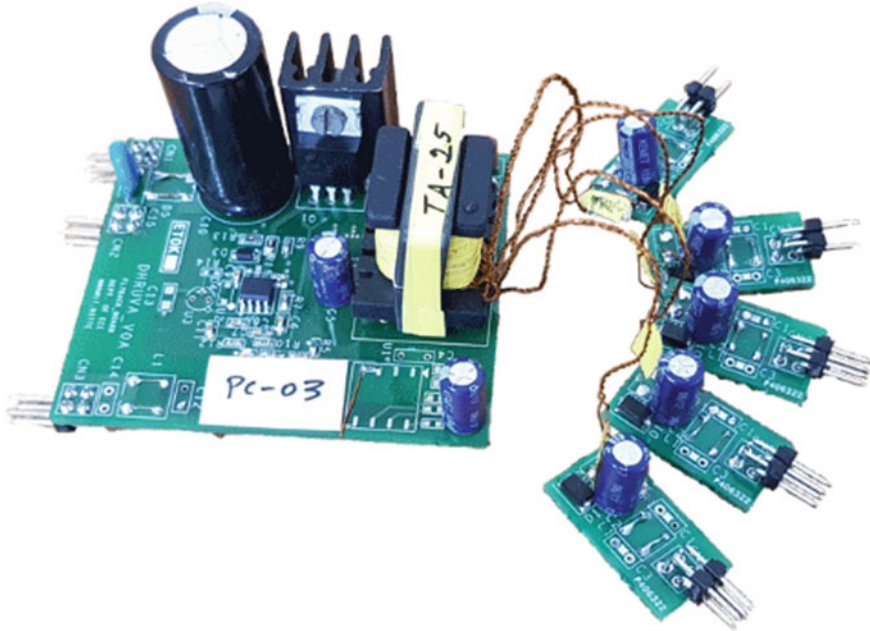


Fig. 9 Hardware set-up of flyback

The hardware approach in this design includes schematic entry using Orcad Capture and layout using PCB Editor tool. The hardware prototype of proposed system is as in Fig. 9. It is a four-layer PCB that consists of top, Vcc, ground and bottom layers. Daughter boards have two layers consisting of Vcc and ground. The size of main board is 6.5 cm × 5.5 cm and daughter board is 2.5 cm × 1.35 cm.

The flyback converter implements UCC28C44DR IC to accomplish constant output voltage by varying the duty cycle. The drain to source voltage of primary switch with TVS diode protection is shown in Fig. 10. It can be observed that maximum V_{DS} is 625 V with TVS diode protection.

The 18 V regulated winding voltage and unregulated winding voltage waveform is as in Fig. 11. The regulated winding is provided to opto-isolator, and full load is applied to unregulated winding. It can be seen that the proposed converter system is able to regulate the output when the load jumps from no load to full load. This flyback output voltages are used to drive the H-bridge switches.

Without EMI filter, the noise in the output voltage is 150mv peak to peak as in Fig. 12. By putting the common mode and differential mode filter, the noise is reduced to 30 mV as in Fig. 13.

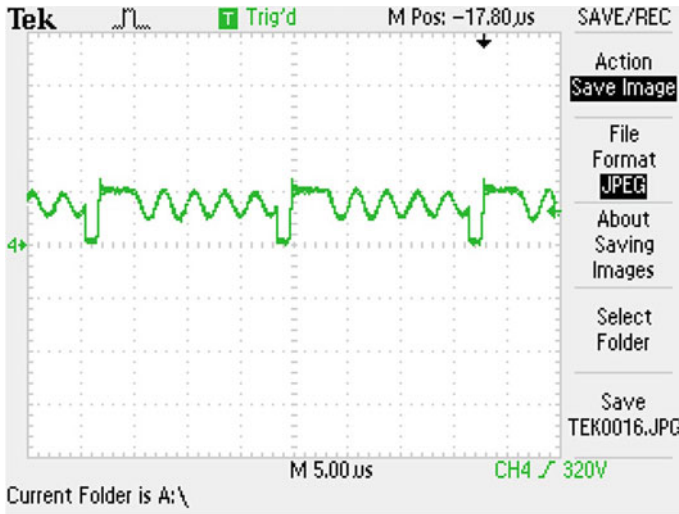


Fig. 10 Drain to source voltage of primary switch waveform

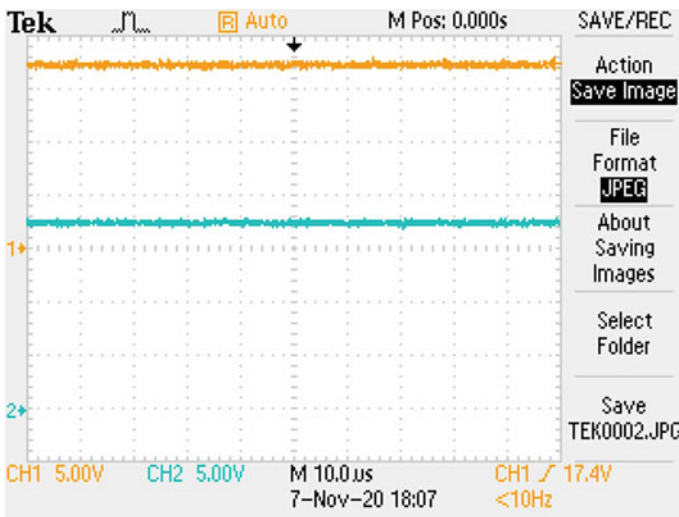


Fig. 11 Regulated winding voltage (blue colour) and unregulated winding voltage (orange colour) waveform

6 Conclusion

This paper deals with design and development of secondary regulated flyback converter. The proposed system was simulated using MATLAB Simulink tool to

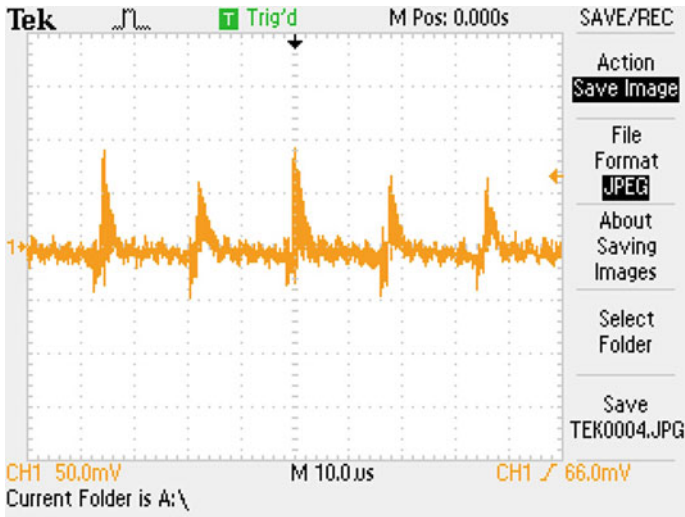


Fig. 12 Output waveform without EMI filter

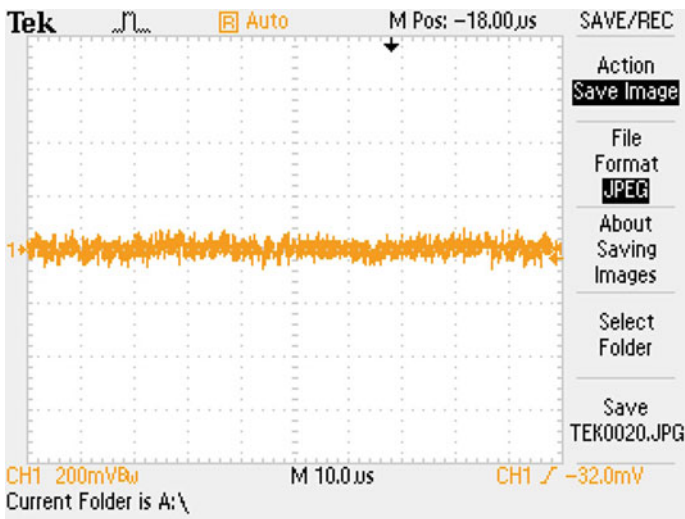


Fig. 13 Output waveform with EMI filter

obtain the theoretical results. Hardware implementation is done using OrCAD Capture tool, and obtained practical output is similar to theoretical results obtained.

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