

Radiation Immune SRAM Cell for Deep Space Applications



Sparsh Koushik, Pawan Kumar Sahu, Shashank Kumar Dubey,
and Aminul Islam

1 Introduction

There exist a large number of highly energized particles in the space environment. Unexpected errors or even failure of the complete system may come about if these highly excited particles hit the integrated circuits. The Static Random Access Memory, abbreviated as SRAM, carries with it a substantial amount of data, which unfortunately are extremely vulnerable to the radiations. Since the SRAM is a very crucial part of the aerospace electronics system, the study of radiation hardening and its impact on these memory cells become very important.

In deep submicron technologies, virtue of aggressive dimension scaling in the MOSFETs, SRAM cells are more prone to radiation-induced single event upsets due to large sensitive volume and low storage node capacitances. Earlier, the error-correcting codes are used to limit the soft error in SRAM. However, due to longer processing time and larger area overhead, error-correcting codes protected SRAM are not appropriate for aerospace applications. Due to smaller silicon area, lower power dissipation and shorter access delay are better options to enhance the single event upset (SEU) immunity as compared to traditionally used error-correcting codes. This motivates to design a radiation [1] hardened SRAM cell to provide robust operation even under process, voltage and temperature (PVT) variations and severe radiation environment in space with the help of double exponential current source. SRAM [2] cells occupy more than half of the chip area of modern-day high-performance ICs. As transistor dimension and spacing between the transistors is reduced due to CMOS technology scaling, multiple transistors are susceptible to the charge deposited from a single particle causing single event multiple node upsets [3]. This encourages

S. Koushik · P. K. Sahu · S. K. Dubey (✉) · A. Islam
Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra,
Ranchi, Jharkhand, India

A. Islam
e-mail: aminulislam@bitmesra.ac.in

the need for soft-error resilient SRAM cells that can function even under extreme radiation conditions.

A variety of structures have been proposed that address the problem of radiation-induced soft errors. Authors in [4] have proposed two radiation-hardened-by-design (RHBD) memory cells (PS-10T and NS-10T) by using a stacked structure. However, these memory cells cannot provide fully single event upset (SEU) protection. NS-10T cell can only recover $0 \rightarrow 1$ SEU, whereas PS-10T cell has the capability of tolerating only $1 \rightarrow 0$ SEU. In [5], the authors proposed a differential read cell. 12T Dual Interlocked storage Cell (DICE-12T) was proposed in [6], which uses dual node feedback control to make it fully immune against SEU on a sensitive node. However, it is unable to recover single-event-multiple-node upsets (SEMNUs), which is becoming more critical reliability issue for emerging nanometer CMOS technology. The 12-transistor radiation hardened by design (RHD-12T) memory cell was proposed in [7]. Besides providing SEU immunity on any of its internal single nodes, it can also provide the SEMNUs immunity to some extent. Another RHBD-10T cell is recently proposed in [8] to provide area-efficient solution to SEU immunity. However, its radiation hardness performance in terms of SEMNUs is yet to be investigated. The previous solutions either show larger area overhead or limited SEU immunity. Therefore, they may not be suitable for aerospace applications where both area-efficient and highly reliable performances are required. Hence, radiation hardness by design is preferred for enhanced performance.

The remaining part of the paper has been organized as follows. Section 2 explains the proposed WARH12T memory cell structure and behavior, SEU recovery analysis, MEMNU recovery analysis. Section 3 explains the evaluation of the different parameters of the proposed cells and comparison cells. This includes access time evaluation and comparisons, cost comparison, SEU robustness verification and comparison, stability comparison (RSNM, WSNM and HSNM), read power comparison, write power comparison and hold power comparison. Section 4 contains the conclusion.

2 Proposed WARH12T Memory Cell

2.1 Cell Structure and Behavior

Figure 1 shows the schematic diagram of the proposed WARH12T SRAM cell. The proposed cell has four storage nodes Q, QN, VL, VR, four PMOS (P1, P2, P3, P4) and eight NMOS (N1, N2, N3, N4, N5, N6, N7, N8) to form a latch. Q and QN nodes are the storage nodes, VL and VR are the intermediate storage nodes. The transistors N5 and N6 are the access transistors, which are controlled by row-based WL signal and used for read and write operations. The transistors N7 and N8 are also the access transistors, which are connected with the intermediate node VR and VL, also connected with the bit lines BL and BLB, respectively, for easy write operations. The four transistors N5, N6, N7 and N8 improve the write capability of

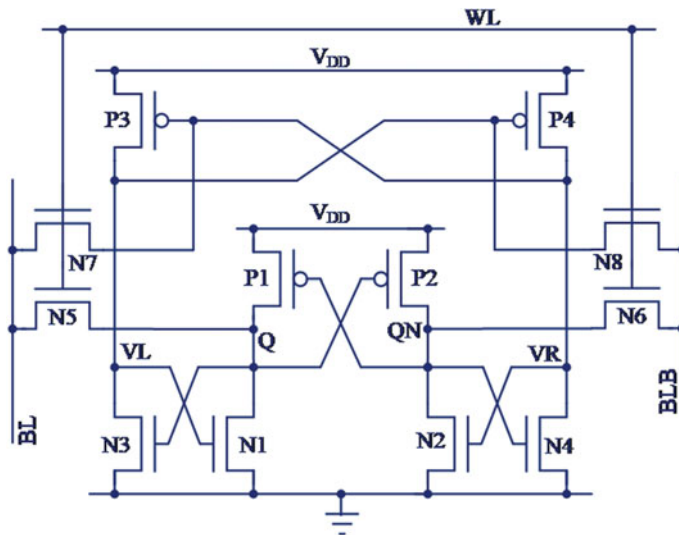


Fig. 1 Proposed WARH12T memory cell

the proposed cell. In order to achieve balance read and write operation, the cell ratio $(WN_1/LN_1)/(WN_5/LN_5)$ or $(WN_2/LN_2)/(WN_6/LN_6)$ is set to be 2.4 for better read stability. The pull-up ratio $(WP_1/LP_1)/(WN_5/LN_5)$ or $(WP_2/LP_2)/(WN_6/LN_6)$ is set to be 1.2. The second pull-up ratio $(WP_3/LP_3)/(WN_3/LN_3)$ or $(WP_4/LP_4)/(WN_4/LN_4)$ is set to be 4.5 for providing the better feedback and easy recovery of the storage nodes Q and QN. The NMOS transistors N3 and N1 or N2 and N4 are cross-coupled to pass the output storage node value to the feedback path, the PMOS transistor P3 and P4 are also cross-coupled and it is used as a positive feedback, which helps to recover the storage node value at Q and QN.

2.2 SEU Recovery Analysis

Taking the case when the state of the sensitive nodes Q, QN, VL and VR is 0, 1, 1 and 0, respectively.

- (1) When the output storage node Q is affected by an SEU, and its potential changes from 0 to 1. Transistor P2 is OFF and transistor N3 is ON momentarily, as P2 is OFF QN is at high impedance state and keeps its state as logic 1. Meanwhile N3 is ON and P3 is already ON making VL node unstable for a while and its potential is decided by the strength of P3 and N3 as we kept the strength of P3 is more than the strength of N3. So, the value of node VL becomes 1 and it will switch ON the transistor N1, which will help to recover the value at node Q immediately.

- (2) When the output storage node QN is affected by an SEU and its potential changes from 1 to 0, transistor N4 is OFF and transistor P1 is ON temporarily. As N4 is OFF, node VR is at high impedance state and keeps its value as logic 0. Meanwhile P1 is ON and N1 is already ON, which will make node Q unstable for a while and its potential is decided by the strength of transistor P1 and N1, As we kept the strength of N1 is higher than P1, so the logic is decided by the pull-down transistor N1 and value at node Q is 0. It will switch ON the transistor P2 again and the node voltage of QN is recovered back to logic 1.

2.3 MEMNU Recovery Analysis

Multiple events $0 \rightarrow 1$ and $1 \rightarrow 0$ can occur at multiple nodes. Nodes Q and QN are capable of handling both 0 to 1 and 1 to 0 multiple events simultaneously. Taking the case when the state of all the nodes Q, QN, VL and VR is 0, 1, 1 and 0, respectively. When the Node Q and QN change from $0 \rightarrow 1$ and $1 \rightarrow 0$, respectively, transistor P2 is OFF and transistor N3 is ON momentarily, transistor N4 is OFF and transistor P1 is ON. As transistor N4 is OFF, VR is at high impedance state and keeps its state as logic 0. Meanwhile N3 is ON and P3 is already ON making VL node unstable and its potential is decided by the strength of P3 and N3, as we kept the strength of P3 more than the strength of N3. So the value at node VL becomes 1 and it will again switch ON the transistor N1 and try to pull down the potential at Q to zero but P1 is also ON due to upset at QN from $1 \rightarrow 0$, so the potential at node Q is now decided by the strength of P1 and N1 and as we kept the strength of N1 more than the strength of P1, node value of Q becomes 0 and it will switch ON the PMOS transistor P2, which will help to recover the value at node QN. In this way, with the help of feedback transistors P3 and P4, the node voltage of Q and QN is recovered very fast. This proposed WARH12T is capable enough to handle simultaneous upset at both the output-sensitive nodes Q and QN.

2.4 Implementation

The proposed WARH12T memory cell is implemented in 22 nm CMOS technology. The operating voltage for simulation is used as 1.2 V. The layout of the proposed cell WARH12T as well as the comparison cells is implemented in Microwind Version 3.1. All the measurement simulations of proposed cell and comparison cells are performed using SPICE. Double exponential current is also modeled in the SPICE, which mimics the same upsets as occurred in the SPACE. The layout of the proposed cell is shown in Fig. 2.

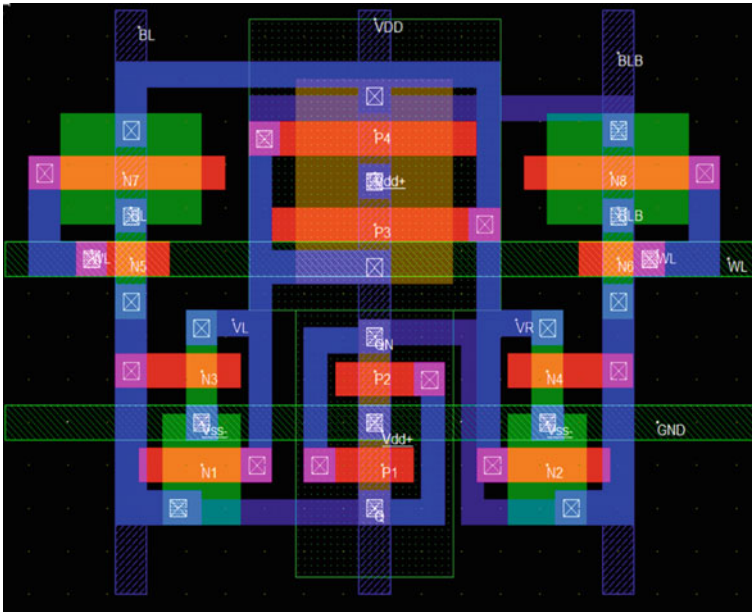


Fig. 2 Layout of the proposed WARH10T memory cell

3 Simulation Results and Discussion

3.1 Access Time Comparison

The read access time (TRA) is measured as the time taken for the voltage of BLB line to fall by 50 mV in the read condition, this time measurement starts from the time when WL starts to be asserted. Write access time is measured as the time taken for the voltage of a given storage node of the given SRAM to reach 90% of the V_{DD} when a write is attempted for that node, this time measurement starts from the time when the word line selected for the given SRAM starts to be asserted.

The TRA and TWA for the proposed structure are calculated at the supply voltages of 1.08, 1.14, 1.2, 1.26 and 1.32 V. The supply voltage of design is 1.2 V. The other values of supply voltage used are to account for supply voltage variation by 5 and 10%. Similarly, TRA and TWA have been calculated for all the comparison structures namely 6T, PS-10T, NS-10T, RHBD10T, RHD-12T and UTSC-12T at these five voltage values. The values of TRA and TWA of all these structures at different supply voltages can be visualized in Fig. 3a and b, respectively, to gain some insights.

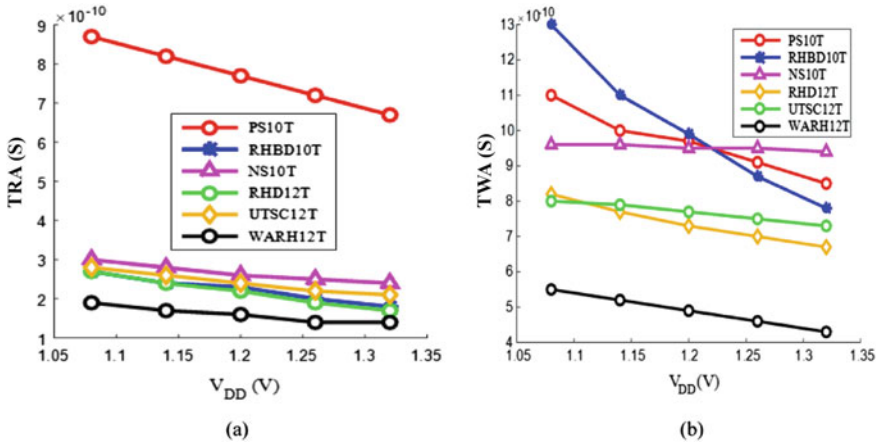


Fig. 3 Plot of **a** TRA, **b** TWA of proposed and comparison cells with V_{DD}

3.2 SEU Robustness Comparison

The SEU robustness was verified by using a double exponential current source. A double exponential current source was injected at the sensitive nodes. This was done to simulate the radiation strike or single event upset at these nodes. These sensitive nodes are characterized as the nodes, which are reverse biased [1].

To check the relative stability of the different structures to single event, we checked the maximum current, the circuit can tolerate before the stored data at the storage nodes of the SRAM cell changes or flips. The maximum value of the peak current for which the proposed WARH12T cell operated correctly is 870 μ A. This maximum current tolerance for different comparison cells was found to be 91.63% smaller for PS-10T, 87.35% smaller for RHBD-10T, 90.52% smaller for NS-10T, 48.39% smaller for RHD-12T and 91.82% smaller for UTSC-12T as compared to the proposed cell at the proposed supply voltage of 1.2 V. It can be noticed that the radiation handling capability of the proposed WARH12T cell is significantly larger than the other comparison cells due to strong cross-coupled PMOS (P3 and P4) feedback, which does not allow to change the voltage at nodes VL and VR even if the output storage nodes Q and QN get affected by SEU, SEMNU and MEMNU.

3.3 Stability Comparison

Static noise margins for read, write and hold states have been used to quantify the stability of the proposed cell and hence for the comparison of the stability of the proposed cell with that of the existing or comparison cells. The static margins calculated are Read Static Noise Margin (RSNM), Write Static Noise Margin (WSNM)

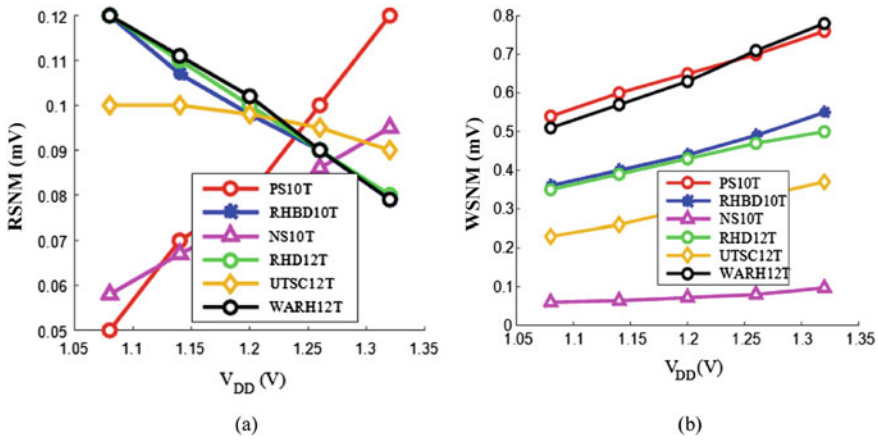
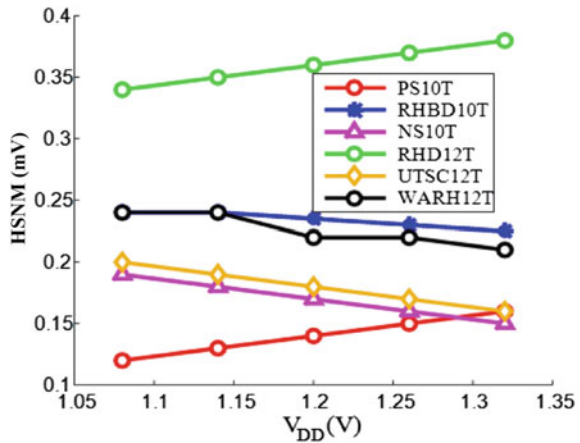


Fig. 4 Plot of a RSNM and b WSNM of proposed and comparison cells with V_{DD}

Fig. 5 Plot of HSNM of proposed and comparison cells with V_{DD}



and Hold Static Noise Margin (HSNM). The RSNM, WSNM and HSNM were calculated for the proposed and comparison cells at supply voltages of 1.08, 1.14, 1.20, 1.26 and 1.32 to study the behavior of the stability of the cells with voltage variation. The variation of the RSNM, WSNM and HSNM with voltage has been plotted in Figs. 4a, b and 5, respectively.

3.4 Power Comparison

For comparing the power consumption of the proposed cell WARH12T with that of existing cells, the power consumed by the proposed cell and the comparison

cells was calculated during a read operation, write operation and hold state. These powers are termed as read power (RPWR), write power (WPWR) and hold power (HPWR). The read power quantifies the power dissipated during a read operation similarly the WPWR and HPWR represent the power dissipated during a write and hold operation. The values obtained for the RPWR, WPWR and HPWR for the proposed and comparison cells for different supply voltages are shown in Figs. 6a, b and 7, respectively.

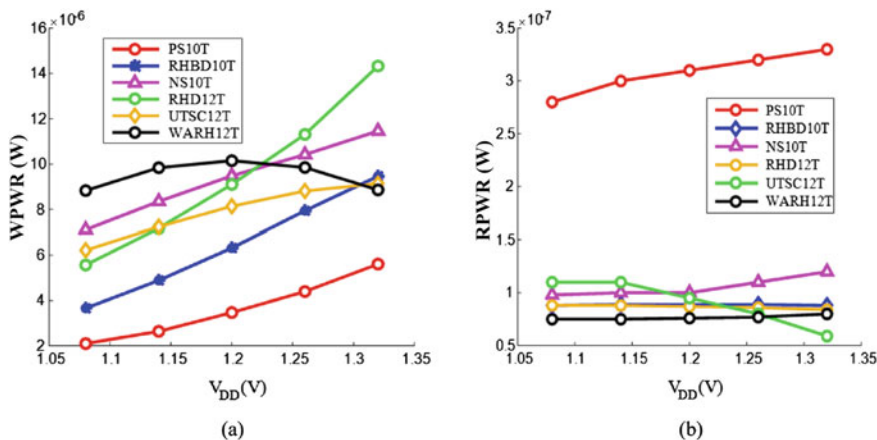
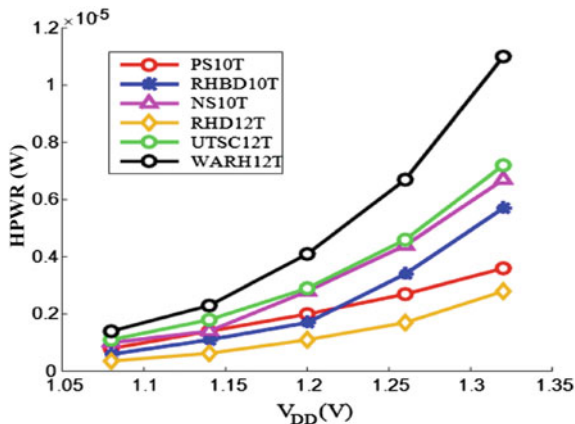


Fig. 6 Plot of a WPWR and b RPWR of proposed and comparison cells with V_{DD}

Fig. 7 Plot of HPWR of proposed and comparison cells with V_{DD}



3.5 TRA and TWA Variability

This section talks about the standard deviation of read access time and write access time. This standard deviation is calculated using Monte Carlo simulations. The Monte Carlo simulations are run for 5000 iterations. This parameter gives an idea of how the read access time and write access time of the circuit deviate under PVT variations. The values of the standard deviation for TRA and TWA of the proposed and comparison cells at different supply voltages are represented in Figs. 8 and 9.

The standard deviation for the TRA of the proposed cell WARH12T at 1.2 V supply voltage is calculated to be 52 ps. From Fig. 8, it can be observed that the TRA variability of the proposed cell is similar in value to other comparison cells, although its value is slightly greater than that of the best performing cells. The standard deviation for the TWA of the proposed cell WARH12T at the proposed supply voltage of 1.2 V was found to be 51 ps. From Fig. 9, it can be concluded that

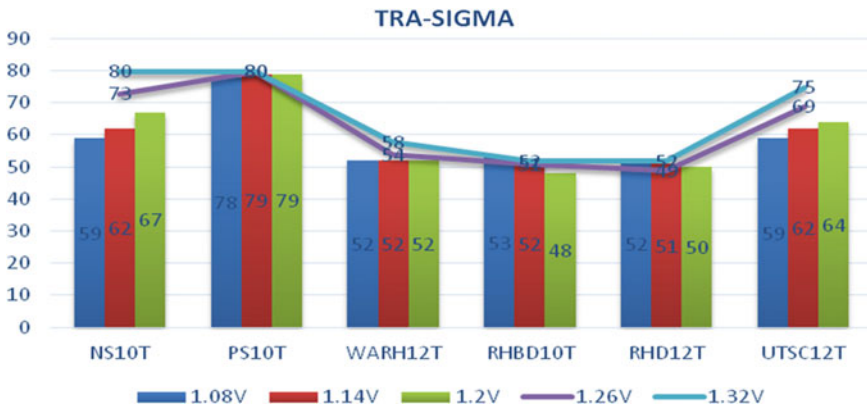


Fig. 8 TRA-SIGMA variation with voltages of the proposed WARH12T memory cell

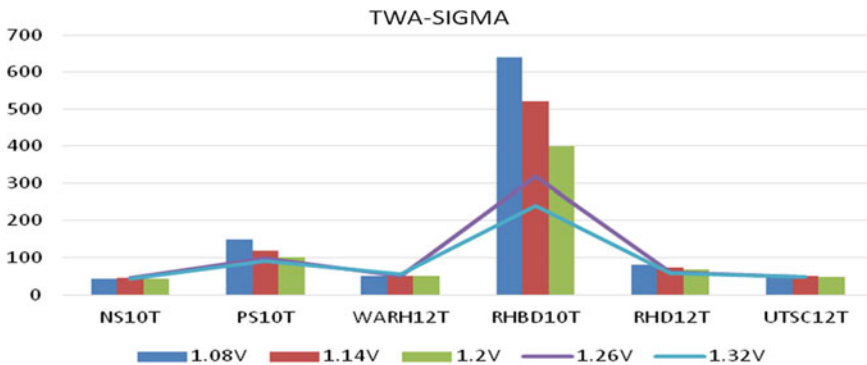


Fig. 9 TWA-SIGMA variation with voltages of the proposed WARH12T memory cell

the TWA variability of the proposed cell is similar in value to the best-performing comparison cells. Its value is slightly higher than the best-performing cells but is comparable and similar in magnitude.

4 Conclusion

This work proposed a high radiation-tolerant 12 transistor SRAM cell. The minimum charge required to change the data of the proposed cell is significantly higher than any other previously proposed cells. The radiation tolerating capacity of the proposed cell is very high compared to any other existing cell. The power requirement of the cell is also reasonably low and comparable to other cells. The read and write static noise margin of the transistor is superior to almost all preexisting structures. The hold static noise margin is also similar to comparison cells. Although the area is not good, this is a trade-off between higher radiation tolerance, write ability and area requirement. Hence, we can conclude that the proposed WARH12T cell is suitable for a very high radiation environment.

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