Low-Cost FPGA-Based On-board Computer

Dirk van Wyk and Vipin Balyan

Abstract This paper discusses the feasibility for the use of commercially available reconfigurable field-programmable gate arrays as the main system processor for small satellite systems and subsystems. FPGAs are in high demand as the space industry and applications are rapidly increasing and evolving. The use of FPGAs within the design of spacecraft systems reduces the design cost, as well as the turnaround time. It is anticipated that the single-board computer can be used as a configurable on-board computer with high flexibility allowing in-orbit reconfiguration (Thai in Applications for FPGAs on nanosatellites, 2014 [1]). Modern FPGAs are designed with embedded processing systems integrated inside the core allowing monotonous performance task to execute more easily with flexibility. One single printed circuit board with the computing power will handle all the challenging requirements for performance and functionality of the payload data handling.

Keywords On-board computer · FPGA · Small satellite · LEO

1 Introduction

The small satellite industry has grown rapidly over the past few years with designs for a variety of applications and missions. The satellite system structure can be considered as the core structure and a varying one. The payload of the satellite will be the variable component specific to the mission at hand. The development of small satellites can be of great advantage for low earth orbit (LEO) space applications at a lower cost and less development time. The typical small satellite structure consists of several subsystems, namely the OBC as the main component of the satellite for control and data handling (CDH) [2]. Additional structures include the communication system used amid the ground station and with the OBC, making it probable to retrieve remote control as well as sending commands to the satellite. The satellite will have a power control unit (PCU) for all the power demands and the application-specific payload firmware with the actual hardware.

D. van Wyk · V. Balyan (✉)
Cape Peninsula University of Technology, Cape Town, South Africa

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Most on-board computers that have been used in the space environment are based on the microcontroller architecture, although these MCUs provide robust and predictable performance outcomes in the harsh space environment. Factors that will affect electronics in space include single event radiation effects and charged particles, which need to be considered when choosing the main components of the SBC [3].

The overwhelming demand for performance and functionality of new on-board computers creates more complex challenges. The FPGA technology allows for comprehensive functionality of the OBC on a single PCB, with highly integrated and configurable system-on-chip approach. The whole concept is to have a fully reconfigurable system within the OBC in orbit due to the high flexibility of the FPGA technology. The digital FPGAs are used as the main processor for the OBC to compute rigorous tasks and commands that can be done in parallel [4].

The COTS FPGA platform designed in this paper is used as a reconfigurable computing processor in small satellite systems for low-cost development and high-speed computing. This paper mainly introduces the OBC board development using the Xilinx Spartan-3E device and the architecture for this platform and simulations are done for the processes to read and write into memory, as well as the communication interface through UART. The use of commercially off-the-shelf (COTS) components is to build small satellites, CubeSats, at lower costs with endless mission possibilities. The standard CubeSat is 100 mm $\times$ 100 mm $\times$ 100 mm in structure known as a 1U satellite. These satellites can be stacked for greater flexibility of applications with structures as 2U or 3U. Nanosatellites or picosatellites are extremely small in physical size and consist of lightweight structures [5].

The internal electronic hardware is based on the PC/104 form specifications. The OBC's printed circuit board will have a PC/104 format with all the peripheral support and functionality. The OBC includes the memory subsystem while being the centre of all communication through the serial bus interface.

The remaining of the work in this article is arranged as follows, where Sect. 2 gives an overview and refers to related work done. The OBC interface layout is given in Sect. 3. The memory access and UART communication interface are explained in Sect. 3. In Sect. 4, the simulation results are demonstrated and explained. Finally, the article is concluded in Sect. 5.

2 Related Work

The FPGA-based on-board computer for a small satellite acts as the primary source for all the monitoring of various subsystems and commands to payload systems. The architecture embraces a system-wide I2C and UART bus from which numerous sensors and payloads are interfaced. A universal asynchronous receiver/transmitter, UART, interface is used between the on-board processor and payload systems which will transfer all the required data for housekeeping, payload data and further required information [6]. Figure 1 illustrates the board's layout and interfacing.

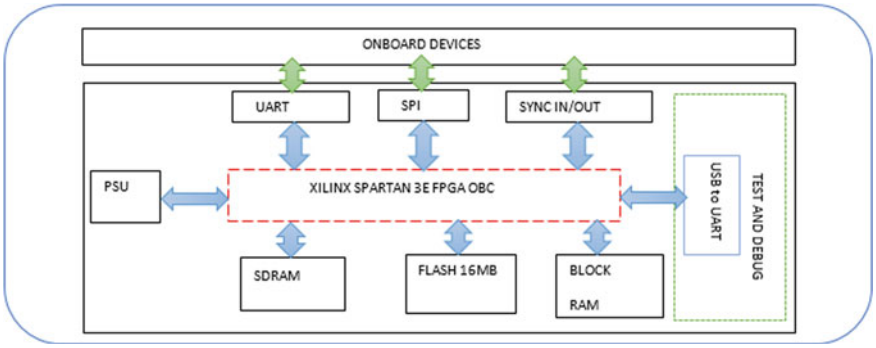

Fig. 1 Proposed OBC interface layout

Previous implementation has been done where the satellite functions on different modes of operation and can be modelled as a finite state machine, where the modes are the states of the FSM and the state transitions are the changes in the operation modes that depend on certain health conditions and parameters as measured by the various on-board sensors.

Satellites have many applications in the new space age, with earth observation (EO) being one of the most popular missions and primary applications. EO satellites use smart image sensors to monitor and capture data from the earth's surface, with infrared for in-depth data collection. This data may then be utilized to monitor urban development, vegetation growth, natural disaster, etc. The use of satellite imaging technology is constantly evolving and improving, the capture information provides more informations due to the improvement in resolution of the images captured. It is all achieved through the use of a wide range of spectral band cameras [7]. Earth observation has been performed since the mid 1900s by the US meteorological satellite. The purpose of earth observation is to measure the earth's characteristic to better understand weather patterns, natural disasters, water behaviour and pollutions [8].

3 Proposed Work

Detailing the hardware components is used to design the FPGA-based OBC platform. The design and development are aimed at providing support for most of the standard devices used on board a small satellite such as various payload systems and mission-specific applications. This board is designed to be used as a development board as there are no specified requirements for the board during the research and project period; therefore, it is customizable and can be integrated into commercial small satellite components to control and read/send data. The board is designed on the PC/104 form factor for small satellites. The proposed testing and verification of the

platform are done by testing the memory and communication interfaces through HIL simulations.

For the hardware development, a commercial FPGA is used as the processing system (PS), namely the Xilinx Spartan-3E with an on-board flash memory component from Atmel with a rich set of peripheral connectivity interfaces. It was found that in comparison with general-purpose processors (GPPs), the FPGAs are definitely more versatile and configurable when compared to application-specific integrated circuits (ASICs) [6]. The software development and simulations are done using the VHDL programming language for the test bench of the external flash memory and the communication interface. The type of storage is dependent on the application at hand. It is during storage that errors are most likely to arise. Errors usually occur when radiated particles penetrate the memory cells contained within the RAM. These types of errors are defined as bit flips in the memory [9].

4 Results and Simulations

Focus is on the hardware being utilized for the main processor of the OBC as well as the design structure. The simulations and verification of the memory system and communication of the FPGA are discussed with simulated results.

First In First Out (FIFO) helps in data transfer and cross clock domains. FIFOs are used within FPGAs mostly throughout and ASIC designs as basic building blocks [10]. FIFOs have various purposes which include crossing clock domains, storing data and buffering data prior to sending it to the RAM modules. The on-board memory is from Atmel, model AT45DB161E, Fig. 2. This module allows for simple in-system programmability and re-programmability which does not necessitate high

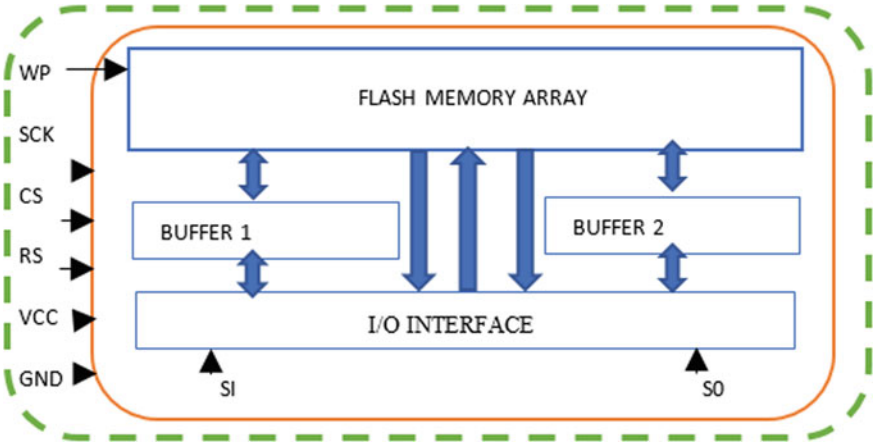

Fig. 2 16 MB flash memory block diagram

input voltages, where the flash memory operates off a single 2.5 V power source for the erase, write and read commands. This flash memory is ideal for the use within various applications to store data, images and program code. Rapid serial interface through the three-wire interface is done using the serial input (SI), serial output (SO) and the serial clock (SCK) pins [11].

The FPGA OBC needs to be programmable and configurable to suite an end user's requirements. Therefore, it has been designed to be able to connect to the Xilinx XC3S250E FPGA through the on-board JTAG connection or via the micro-USB port. The FT2232D is used in for the USB interface which incorporates the functionality of two second-generation BM chips into a single device. The stand-alone downstream USB port is converted to two IO channels which can be individually configured as a UART interface or as a FIFO interface. This makes it more convenient to programme the FPGA through an on-board USB port. For additional support, the FPGA may be programmed through the JTAG configuration as an alternative. To programme the FPGA using the JTAG, a USB blaster module is required. The Xilinx Spartan-3E family FPGAs and the Platform Flash PROMs all make use of a four-wire JTAG port compliant with the international IEEE 1149.1/1532 standard. They divide the JTAG TCK, USB_TCK, clock input and the select input function through TMS mode. These components can connect in any order with the TDO output on the JTAG string of one device transmitting the TDI/USB_TDI input from the other device in the sequence. The TDO output from the last device in the JTAG string leads the JTAG connector. This programming interface on the FPGA is powered through the VCC_AUX supply. Subsequently, the PROM's VCC supply must additionally be 2.5 V [12]. For the HIL simulation, a local computer with Xilinx IDE is used. The FPGA board is programmed through the use of a USB blaster via the JTAG pins. Figure 3 illustrates the basic flow of the hardware-in-the-loop simulation set-up. The UART mode of communication transfers data in blocks of 8 bits, also known as frames, which are user-configurable in terms of contents. The USART can function in either synchronous or asynchronous modes, which are application dependent [13].

The Write Enable (WR_EN) is used to write data into the FIFO with the Write Data (WR_DATA) holding the data that is sent to the FIFO. The FIFO model has a clock and reset trigger points. The clock is used for every action to execution upon trigger of the clock on the rising (high) edge or falling (low) edge of the clock frequency based on your application. As the name states, reset is the signal used to reset the FIFO memory when a high signal is transmitted.

From the read side, there is the Read_Enable (RD_EN) which allows the reading of the current data from the FIFO memory. To read data, the RD_EN input must receive a high input during one clock cycle and the data that is stored first will be read first from the Read_Data (RD_DATA) pin. When reading data constantly or at a high rate, the RD_EN pin's state may be set high for a longer period than one clock cycle.

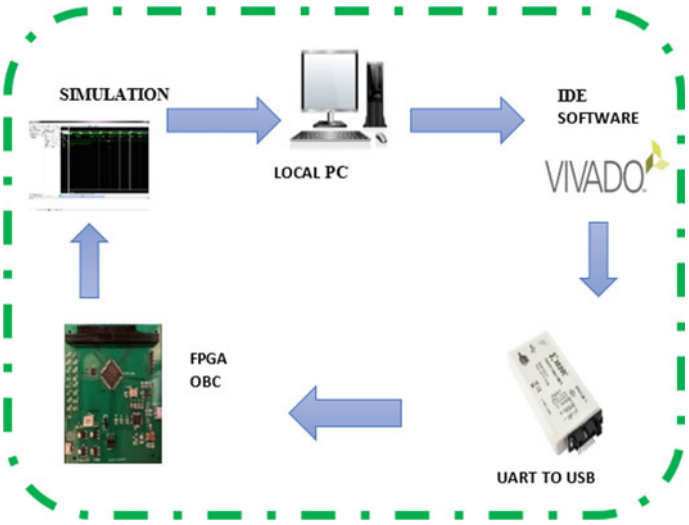

Fig. 3 HIL set-up sequence flow diagram

The write and read functions are implemented on the designed FPGA Spartan-3E board. This verifies the memory operation of the OBC with 16 MB flash memory on board. A basic write sequence is done in VHDL using the Xilinx IDE platform to configure the OBC. Figure 4 shows the read and write sequence on the flash memory through a FIFO model from the simulated VHDL code in the flow diagram illustrated in Fig. 5. The is done through every clock pulse, and the write of data is enabled.

Figure 4 shows the outcomes of the write/read operation for a full cycle where the FIFO buffer is full. In simultaneous read and write FIFOs, there is no dependency between the write and read operations of the data. Instantaneous reading and writing are possible in an overlapping manner or continuously. In other words, the two systems with different frequencies can be connected to the FIFO buffer. When designing a platform, you do not need to concern regarding harmonizing these two

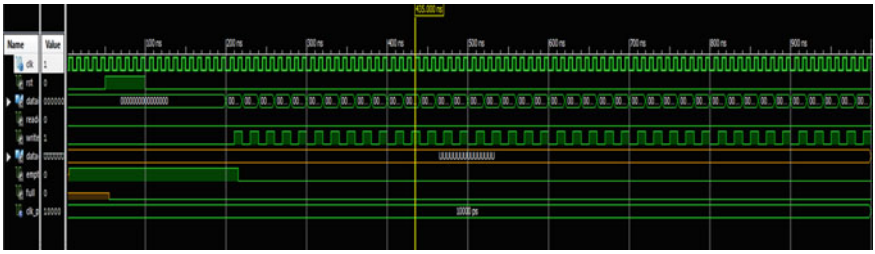

Fig. 4 Full FIFO cycle simulated on FPGA OBC

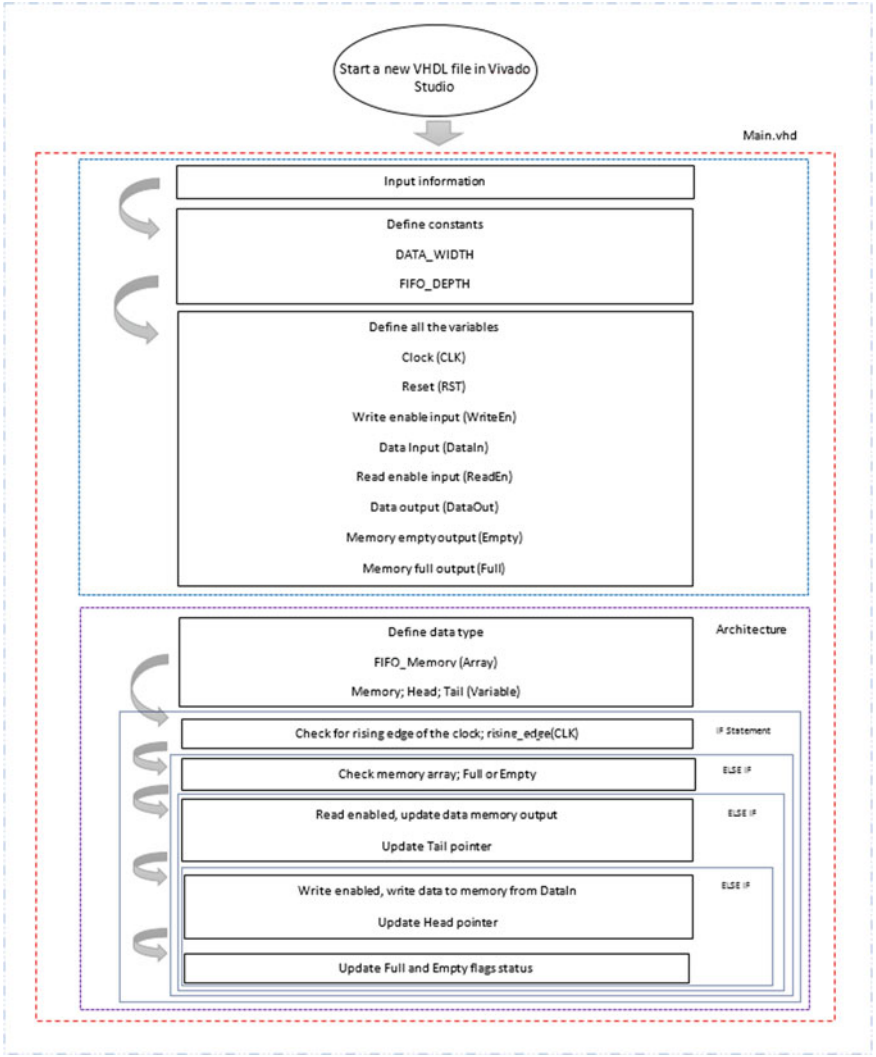

Fig. 5 VHDL memory test flow sequence

systems as this is taken into consideration by the FIFO. Parallel read and write operations of the FIFOs depend on the command signals for reading and writing which are based in two groups, synchronous and asynchronous FIFO banks.

For this simulation, the synchronous standard FIFO was used. The DATA_IN signal is the input to the FIFO with the DATA_OUTPUT as the output. WR_EN is the signal used to write data into the FIFO memory when the CLK is triggered on the positive edge. RN_EN is used for reading data from the FIFO buffer and is able to be reset through RS as high. The FIFO buffer will indicate when it is full with the

FULL signal at high and the same for the EMPTY signal when the buffer is empty, the signal will be high.

There are numerous ways to optimize VHDL code. Some of the main topics when it comes to optimization are efficient adder implementation, state machines, signal selection, storage structure, placement and routing [14]. In this paper, the Vivado package is used to code, analyse, compile and optimize the VHDL code.

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The UART transmission is of a serial-type communication. Nonconcurrent transmission suggests that both the receiver and the transmitter have singular local clock signals which are established before the proceeding of the communication instead of simultaneous, where the communication transmission is synchronized on both ends through a common clock (Fig. 7).

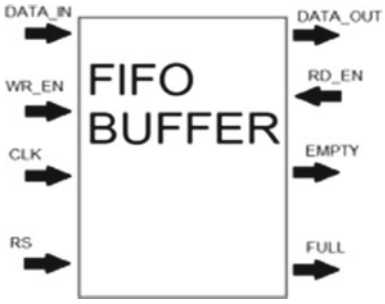

Fig. 6 FIFO memory read/write sequence

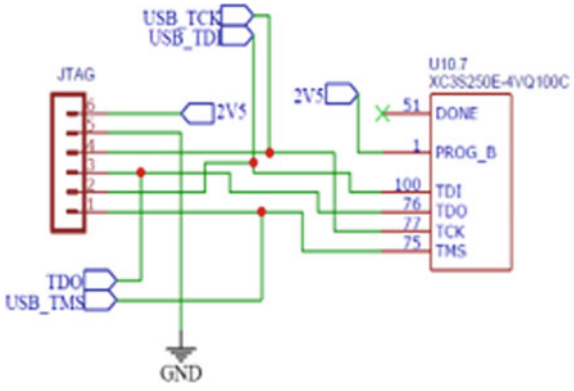

Fig. 7 JTAG in-circuit schematic

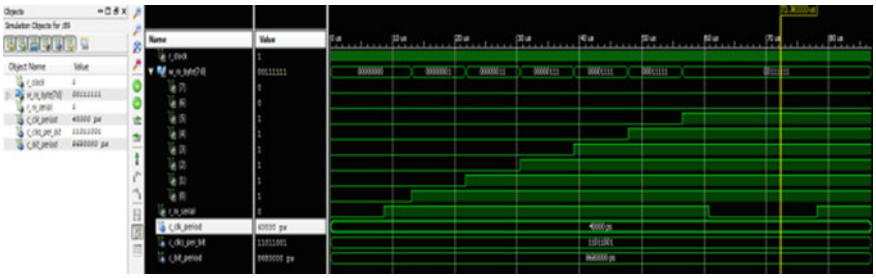

Fig. 8 UART simulation from VHDL test bench file

The UART communication for the FPGA-based on-board computer is also tested through the HIL simulation using a small VHDL script file to test the transfer of data between the OBC and the IDE platform. Figure 8 shows the UART communication between the FPGA-based OBC designed platform with successful WRITE and READ commands of 8 bits.

5 Conclusion

The first step presented for this research was to establish the various parameters governing an on-board computer for small satellites within low earth orbit and the space environment. Emphasis was put on the main components that are proposed for the OBC by using commercially available electronic components. The FPGA device had to be of commercial grade for the operating temperature and durability that will most likely survive in the space environment, as well as the current systems and electronic components being used in the small satellite industry that are of space grade and/or radiation-hardened components. Research was done on various FPGA manufacturers and current commercial OBC platforms available for satellite systems. A comparison is done on the most feasible and readily available FPGA packages as to which one will be used for the design implementation and verification of the OBC.

The final FPGA that was used is one from Xilinx Spartan-3E family manufactured in 2018 which has been available by Xilinx for several years now. The Spartan chip has 250 K system gates with a distributed RAM 38 K and 68 differential I/O pairs. This processor was designed to operate in temperature ranges of -40 °C to $+100$ °C which is suitable for low earth orbit missions and applications, at low voltage. The FPGA can be programmed through the USB interface and the JTAG header pins. Programming can be stored on the on-board external 16 MB flash memory. Generic programming is done using Verilog or VHDL to configure payloads or subsystems to control and/or read data from. The designed OBC has an on-board power supply unit to power the various electronic components from the FPGA to the flash memory.

This FPGA OBC was tested under a semi-controlled environment and not simulated under conditions similar to that of the space environment. The reliability will

only be confirmed upon vacuum testing and vibration testing under heat. The electronic components are susceptible to radiation damage or SEE from the cosmic rays, as the electronic component used is COTS components. In future, work will be compared with results from hardware.

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