A Novel Low-Voltage High-Performance Current Mirror

Ashok D. Vidhate and Shruti Suman

Abstract Current mirror is utilized to produce replica of current flowing through active devices, from one end to other end of the circuit irrespective of loading effect. It is an indispensable part of an analog and mixed signal system and is popular due to its wide range of applications. In this paper, new CM circuit which consists of biasing amplifier provides sustainable voltage is proposed. This CM provides low input impedance, low power consumption, high output impedance with high accuracy and bandwidth. The proposed circuit is designed at 0.18 μm technology having high output resistance of 54 GΩ with 2 GHz BW at 100 μA input current.

Keywords Self-biased current mirror · MOS current mirror · Nano-scale MOSFET · Power dissipation · CMOS integrated circuit · Amplifier · Resistance · Cascode current mirror

1 Introduction

Current mirror is the basic building block of analog/mixed mode ICs. It is extensively used for manufacturing operational transconductance amplifiers (OTA), analog-to-digital converters, digital-to-analog converters, amplifiers and filters. CM provides constant output current without dependency of loading. In CM, the output current is the mirror image of input current. The characteristic parameters of the CM are accuracy, input resistance, output resistance, input/output compliance voltage, and operating frequency range of CM. Nowadays in circuit design MOS channel length is scaling down. This adversely affects CM parameters, hence improvement required in the design of CM for low-power high-performance operation.

The remaining part of the paper is subdivided in the following sections: Sect. 2 deals with basic MOS CM. CCM are discussed in Sect. 3. All the current mirrors that have been reviewed are discussed in Sect. 4 with proposed circuit in Sect. 5.

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Based on this performance parameters, simulation outcomes are added in Sect. 6 and finally the conclusion is derived in Sect. 7.

2 Basic Current Mirror

The current mirror circuit is the basic building block of analog circuit design. The circuit which is forced, output current equal to input current. The designs which can be formed by current mirror are analog converters, oscillators, and amplifiers [1–3]. Important characteristic of integrated circuit design is low-voltage operation, low power consumption, wide bandwidth, and minimum are requirements; therefore, there is a growing need for new low-voltage analog circuit design [4, 5]. The VCO and delay locked loops are important circuits operated at low power with current mirror [6–8]. The basic block diagram of current mirror is as shown in Fig. 1.

Ideal current mirror has zero input resistance and infinite output resistance, which implies that the input voltage does vary with the input currents and the output currents are independent of applied voltage [9]. In reality, a CM requires minimum voltage at the output to ensure that the device operate in saturation [10]. This called the output compliance voltage. Accurate mirroring of the signal requires perfect matching of the mirroring transistor M_1 and M_2.

From Fig. 2 it is observed that if a transistor is biased at I_{REF}, then it produces $\mathrm{VGS} = f^{-1}(I_{\mathrm{REF}})$. Thus, if this voltage is applied to the gate and source terminals of second MOSFET, the resulting current is $I_{\mathrm{OUT}} = f \cdot f^{-1}(I_{\mathrm{REF}}) = I_{\mathrm{REF}}$ as shown in Fig. 2. From another point of view, two identical MOS devices that have equal gate source voltage and operate in saturation carry equal current (if $\lambda = 0$). From the figure having M_1 and M_2, neglecting channel length modulation, the current relations can be expressed as,

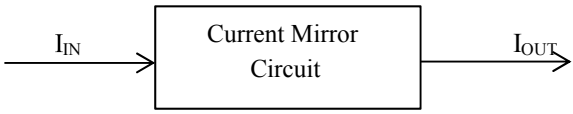

Fig. 1 Block diagram of current mirror

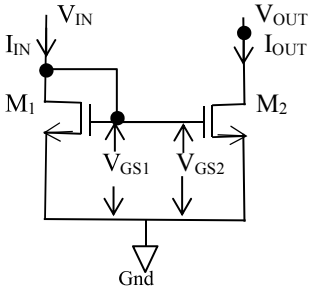

Fig. 2 Basic MOS current mirror

$$I_{\mathrm{REF}} = (1/2)\mu_n C_{\mathrm{ox}}(W/L)_1\left(V_{\mathrm{gs}} - V_{\mathrm{th}}\right)^2 \tag{1}$$

$$I_{\mathrm{OUT}} = (1/2)\mu_n C_{\mathrm{ox}}(W/L)_2\left(V_{\mathrm{gs}} - V_{\mathrm{th}}\right)^2 \tag{2}$$

Dividing Eq. (2) by Eq. (1), the relation between I_{OUT} and I_{REF} is obtained as,

$$I_{\mathrm{OUT}} = I_{\mathrm{REF}}\left[(W/L)_2/(W/L)_1\right] \tag{3}$$

If width-to-length ratio of both transistors is same mirroring of current from input to output takes place.

3 Cascode Current Mirror

To remove out the drawback of basic current mirror, the new structure is cascode current mirror. In cascode current mirror, the two basic CM circuits are connected one above one, i.e., in stacked form. This structure increases output resistance as well as increases gain of the CM. The cascade CM is as shown in Fig. 3.

The cascade structure is formed by using n-p-n MOSFET. In the previous circuit, the effect of channel length modulation is not considered due to that accuracy of basic CM is less. This problem is overcome by cascode CM. For cascode CM, small-signal output resistance is given as,

$$r_{\mathrm{OUT}} = r_{03} + r_{02}(1 + r_{03}(g_{m3} + g_{mb3})) \approx g_{m3} r_{03} r_{02} \tag{4}$$

Hence, the output resistance of cascode CM is equal to output resistance of simple CM multiplied by gain of MOSFET M_3. This means by increasing cascode levels the

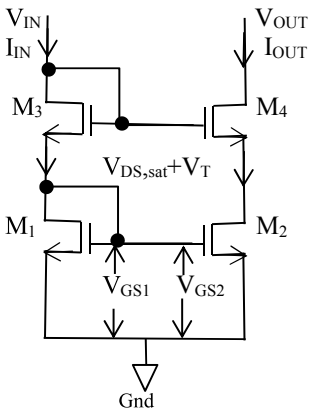

Fig. 3 Cascode current mirror

output resistance of CM increases. But the main drawback is that this also increases the voltage headroom which not applicable for power saving structures.

4 Literature Survey

In 2012, Bradely Minch worked on low-voltage current mirror. The proposed work implementation in a stacked MOS formation by making use of quasi-floating gate circuit, the capacitor functions as control gate to operate MOS in saturation boundaries. The dynamic performance gained due to stacked mirror. It also provides much higher output resistance than basic current mirror circuit but the voltage headroom increases by $V_{\text{diode}} + V_{\text{DSat}}$ which is slightly higher irrespective of current levels [11].

In August 2016, Yasin Bastan, Elach Hamzehil, Parniz Amiri worked on body-driven low-voltage current mirror. This body-driven technique gives higher output impedance by modifying the effective g_m of MOSFET. This also changes circuit parameters. This technique is useful in low-power application as low voltage requirement. The parameter improvements achieved are accuracy, bandwidth, low input resistance, and high output resistance. As compared to basic current mirror, it has just extra signal path having bulk MOSFET [12, 13].

In 2014, N. Raj, A. K. Singh and A. K. Gupta worked on self-biased bulk-driven low-voltage current mirror. This quasi-floating gate technique is combined with bulk-driven technique. This reduces threshold voltage at input side. The input resistance is less but the method suffers low transconductance. This gives limited bandwidth, complex twin-well fabrication process, and low gain [14, 15].

In 2014, Nidhi Tarun, Shruti Suman, and P. K. Ghosh worked on low-voltage current mirror. In this, CM biasing amplifiers are used to achieve low input resistance and high output resistance. This also proposes low compliance voltage requirement for CM [16, 17].

In December 2012, Maneesha Gupta and Bhawna Aggarwal proposed self-biased cascade current mirror. In this CM due to supercascode formation, the output resistance and BW get increased. The leakage current limits output resistance [18, 19].

In 2019, M. Doreyatim et al. proposed low voltage gain boosting CM which gives high voltage swing and better accuracy as mismatch between the devices is minimized by using internal amplifiers. The boosting structure is used to increase output resistance without limitation of input–output swing [20–22].

In 2020, K. Monfaredi and H. F. Baghtash extremely low voltage and high compliance CM in this current compensation scheme utilized which provides positive and negative feedback. The negative feedback is utilized to provide constant current at output side irrespective of increase in output resistance, whereas positive feedback is utilized to provide constant current at low voltage. But stability is the major concern as positive feedback is used [23, 24]. Due to use of cascaded inverters and inductive peaking, the bandwidth of the circuit increased [25].

5 Proposed Current Mirror

The proposed amplifier-biased current mirror (ACM) consists of biasing amplifier which provides sustainable voltage to keep transistor M_3 and M_4 in saturation. To obtain low input resistance along with basic current mirror, the transistor M_3 is connected in series. An amplifier having gain of '$-A_1$' is connected to transistor M_3 to control the gate voltage. Also, if input voltage is increased then due to amplifier combination input voltage to m_3 is decreased by 'A_1' results decrement in input resistance by some value of amplifier gain. Hence, supply voltage requirement gets decreased [26, 27].

Figure 4 shows amplifier-biased CM. In the output stage, supercascade configuration consists of amplifier having gain of ($-A_3$), transistor M_4 and M_5. The inverting amplifier A_3 provides biasing current I_{B1} to transistor M_5. This combination provides high output resistance as negative feedback loop forms in the circuit through transistor M_4, M_5 and M_6 [28]. This improves output resistance, accuracy, and gain of the current mirror.

5.1 Small-Signal Analysis of Amplifier-Biased CM

5.1.1 Input Resistance

Figure 5 shows transistor-level implementation of ACM. In this, the amplifiers are replaced by transistors which act as simple inverters. In the implementation M_3 is

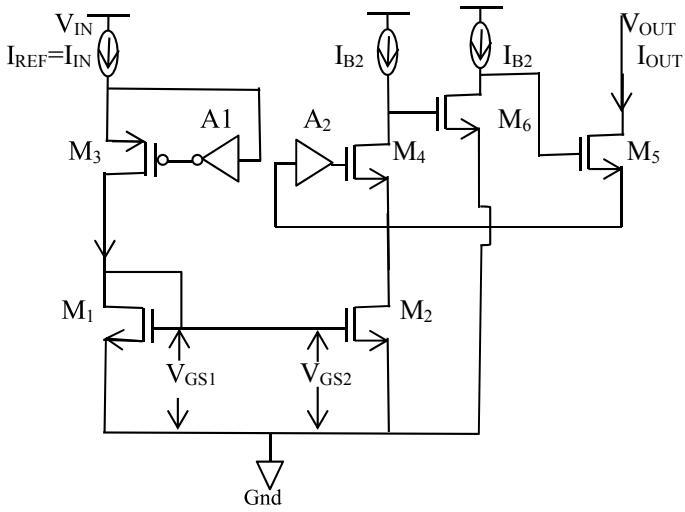

Fig. 4 Proposed amplifier-biased current mirror (ACM)

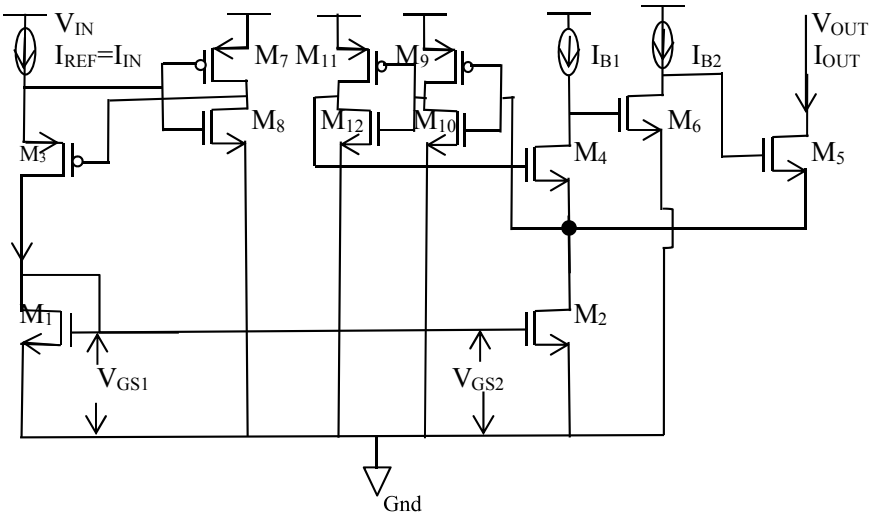

Fig. 5 Transistor-level implementation of proposed ACM circuit

p-type for this input is from inverting amplifier so only two transistors are enough for inverter input. But transistor M_4 is n-type so back to back two inverter structures are connected to produce required input for transistor M_4. To operate transistor circuit perfectly, the transistors M_7 and M_8 should work in saturation region. If any one of these transistors not work in saturation, then gain of the circuit gets reduced significantly.

Figure 6 shows small-signal equivalent model for input port of amplifier-biased CM.

By Kirchhoff's current law at differential node gives,

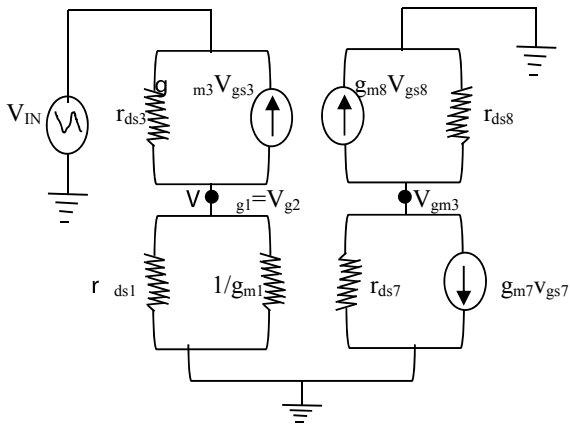

Fig. 6 Small-Signal equivalent model to calculate input resistance of ACM

$$I_{\mathrm{IN}} = (V_{\mathrm{IN}} - V_1)/R = (V_1 - V_2)/r_{ds3} - g_{m3}V_{gs3} = \left(V_{g1}/r_{ds1}\right) + \left(V_{g1}/r_{gm1}\right) \quad (5)$$

The resistance r_{IN} is derived as

$$R_{\mathrm{IN}} = V_{\mathrm{IN}}/I_{\mathrm{IN}} \quad (6)$$

$$r_{IN} = (1 + r_{ds3})/(g_{m1} + g_{m3}g_{m1}r_{ds3}(A_1 + 1)) \quad (7)$$

From the above equation, it is observed that input resistance is inversely proportional to amplifier gain A_1. Hence, as value of amplifier gain is high the input resistance is low [29].

5.1.2 Output Resistance

Figure 7 shows the small-signal equivalent circuit to calculate output resistance. In the output side, negative feedback loop gives $V_{ds1} = V_{ds2}$, hence decreased effect of channel length modulation and accuracy maintains high [30].

By KCL at output side

$$V_{\mathrm{OUT}} = I_{\mathrm{OUT}} \cdot r_{ds5} + g_{m5}V_{gs5} + \left(V_{\mathrm{OUT}} - V_{gs4}\right)/r_{ds2} \quad (8)$$

$$I_{\mathrm{OUT}} = V_{gs5} \cdot g_{m5} + \left(V_{\mathrm{OUT}} - V_{gs4}\right)/r_{ds5} = V_{gs4}/r_{ds2} \quad (9)$$

$$r_{\mathrm{OUT}} = V_{\mathrm{OUT}}/I_{\mathrm{OUT}} = r_{ds5}[1 + r_{ds2}(g_{m5}r_{ds6}(1 + g_{m4}r_{ds4}) + (1/r_{ds5}) + g_{m5})] \quad (10)$$

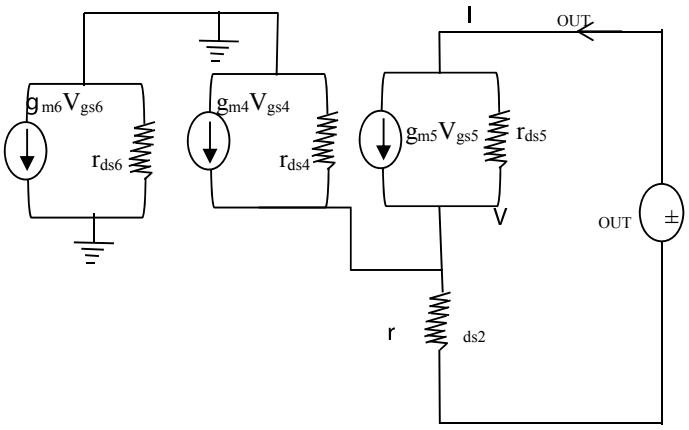

Fig. 7 Small-signal equivalent model to calculate output resistance of ACM

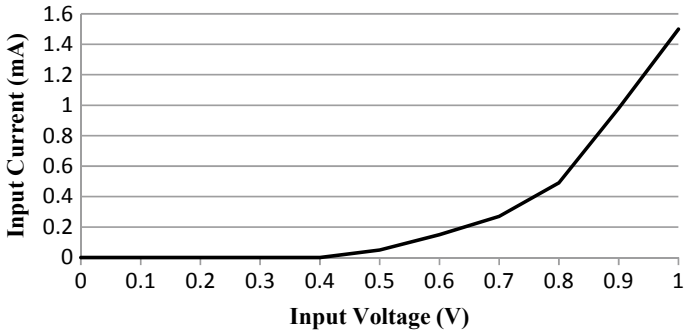

Fig. 8 Input characteristics of ACM

As g_m is large $g_m r_{ds} \gg 1$

$$r_{\text{OUT}} \approx g_{m4} r_{ds4} g_{m5} r_{ds5} g_{m6} r_{ds2} \tag{11}$$

r_{OUT} is proportional to g_m of the transistor. If g_m is large then r_{OUT} is also large.

6 Simulation Results for Proposed Current Mirror

To find out results, the Tanner EDA tool is utilized. The 1 V input power supply is used. Simulations are carried out to find out input characteristic, output characteristic, and frequency response.

6.1 Input/Output Characteristic of ACM

Figure 8 shows input characteristics of ACM. Due to application of input voltage current starts to flow in the ACM. The current value is zero up to 0.5 V as input beyond this current starts increasing exponentially. The minimum compliance voltage obtained at the input side is 0.6 V; this implies that ACM has low input resistance.

6.2 Output Characteristics of ASCCM

Figure 9 shows output characteristics of ACM. In VLSI output resistance should be high. The minimum compliance voltage obtained for the ACM is 0.2 V.

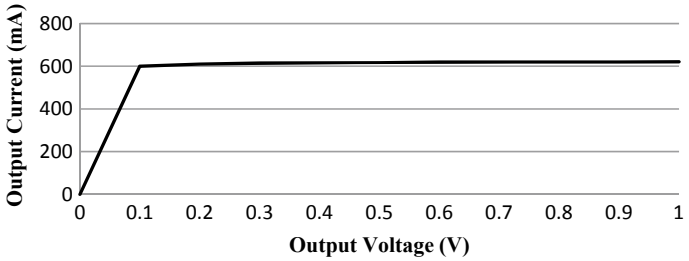

Fig. 9 Output characteristics of ACM

6.3 Frequency Response of ACM

The bandwidth enhancement obtained in ACM by adding super cascode configuration to primary current mirror. This gives bandwidth of 2 GHz at 100 μA (Fig. 10).

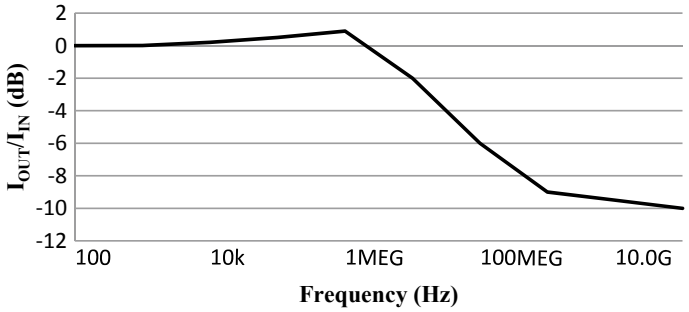

Fig. 10 Frequency response of proposed current mirror circuit

Table 1 Summary of current mirrors with ACM

References	[12]	[13]	[14]	[16]	Proposed ACM
Input resistance, R_{in}	13 GΩ	240 kΩ	675 kΩ	0.18 kΩ	180 Ω
Output resistance, R_{out}	39.5 GΩ	115 kΩ	485 kΩ	6.25 kΩ	54.68 GΩ
Input current, I_{in} (μA)	15 μA	447 μA	500 μA	–	100 μA
Bandwidth (MHz)	216 MHz	655 MHz	2.5 MHz	98.50 MHz	1.15 GHZ
Power	42.5 μW	0.825 mW	–	46 μW	340 μW
Supply voltage (Volt)	1 V	± 5 V	−1 V	0.8 V	1 V
Number of transistors used	7	11	10	10	12
Technology	0.18 μm	0.13 μm	0.18 μm	90 nm	0.18 μm

The specification of proposed ACM is given in Table 1 and the values are compared with related CM circuit. It can be seen the output resistance significantly increased with minimum input resistance. In addition, its bandwidth is increased without sacrificing any performance.

7 Conclusion

A novel self-biased CM with very high-performance characteristics has been introduced and verified with the help of simulations. Using this technique, input resistance and input compliance voltage get reduced to 180 Ω and 0.6 V, respectively. The frequency response is stable in nature and relatively high. Simulation result supports the utility of ACM for low voltage, high output resistance, and high performance. Improvement in output resistance has been carried out by implementation of transistor configuration at the output side. The active realization of the resistances, to overcome the drawbacks of passive components, has also been discussed. The proposed saturation region CM, where all required resistances have been replaced by active components, shows high degree of accuracy over a wide input current range. Small-signal analysis has been carried out at each step and the results have been validated using Mentor Graphics Eldospice based on TSMC 0.18 μm CMOS technology using 1 V supply voltage.

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