Two-Dimensional Analytical Expression of Threshold Voltage for Un-doped Double Gate MOSFET

Vikas Maheshwari, Somashekhar Malipatil, Narendra K. Garg, and Rajib Kar

Abstract In this work, new two-dimensional (2-D) analytical solution of threshold voltage (V_{th}) for un-doped Double Gate MOSFETs is proposed. In this research work, Green's function based techniques are applied to solve the Poisson equations in 2-dimensional and we derived the threshold voltage (V_{th}) expression by using the concept of surface potential. This design is supposed uniform doping profile in Si area. The design is compared with existing experimental results and we got better solutions compared to existing works.

Keywords Minimum surface potential · Green's function · Symmetric DG-MOSFET · Threshold voltage · 2D Poisson equations and Un-doped

1 Introduction

In last two decades, VLSI (very large-scale integration) Technology CMOS has been used as a fundamental building block for low power system designs. Double-Gate (DG) MOSFET is emerging as a latest research domain in VLSI because the scaling of these devices is possible to the minimum channel length L possible for provided process technology parameters [1]. The scaling of MOSFET at deep submicron level has shown new and serious challenges for the designing and fabrication of future integrated circuits. When the MOSFET dimensions are scaled down, both the supply voltage and the gate t_{ox} be scaled down. The short channel effects [2] are controlled by scaling down both the gate-oxide thickness and channel length. The

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scaling of gate-oxide thickness is limited to about 1 nm because of high gate tunneling current [3, 4]. Scaling down the device dimension in nanometer regime, leakage currents plays an important role which needs more attention from the designer. Scalability of DG-MOSFETs is limited by sub-threshold swing which is an important design parameter. Formation of two channels in the symmetric DG MOSFET [5] provides steep sub-threshold swing, high drive current, and trans-conductance. The sub-threshold swing and other short channel effects can be optimized by using appropriate gate dielectric [6]. Therefore new MOSFET structures such as Dual Gate and Tri-Gate MOS transistors [7] are proposed to replace conventional planer MOSFET. It is also important that these new structure of MOSFETs are compatible with latest designing and fabrication techniques [8] of silicon integrated circuits. Dual gate MOSFETs also referred to as inversion charge transistors have many advantages over conventional MOSFETs. First, there is a considerable reduction in the device area. Second, DG MOSFET's miller capacitance and output conductance can be further considerably reduced which makes it useful device for the designing of analog integrated circuits. Third, the breakdown voltage of the device can be made very high by using proper design methodology. Fourth, short channel effects in scaled devices are drastically minimized. Comparable to conventional MOSFET, in case of Dual Gate MOSFET, both gates control the properties of channel. Thus more scaling of gate length can be performed in DG MOSFETs. DG MOSFETs is better alternative of conventional MOSFETs because DG MOSFETs have improved on short channel effects. Also DG MOSFET has higher current density. Therefore performance of the devices can be maintained low leakage and higher current density by employing DG MOSFETs. In DG MOSFETs better manage short channel effects and V_{th} is achieved ideally without altering the concentration of channel dopants. This technique diminished the statistical dopant fluctuations [9] an also reduces the phenomena of impurity scattering. Many structures and techniques were used SOI devices with less short channel effects [10, 11]. Using DG MOSFETs can minimize short channel effects. The conventional MOSFET cannot be scaled down below 10 nm process technology. Therefore DG MOSFETs are widely employed in the analog electronic circuits where reduced short-channel effects, electronic gain control capability, high breakdown voltages are required. DG MOSFETs are fabricated in below 20 nm fabrication process technology by using metal gate technology for both the gates that diminished the poly depletion effects. The effects are degradation [12] and mobility of dopant atoms are eliminated of DG MOSFETs. Due to these advantages, an analytic and simple threshold-voltage model is highly desirable for un-doped DG MOSFETs as one of the key point parameters for the design of such nano-scale devices. More advantages of Dual Gate MOSFETs are improved trans-conductance, early voltage, and carrier transport efficiency. Accurate and physics-based formulations are required for implementation of high-speed VLSI circuits comprising of compact MOSFET model. Due to these requirements for the device, the un-doped symmetric DG MOSFETs are best-suited device structure because of the thin and undoped nature of the channel. In the situation of surface inversion near oxide-silicon interface, the energy band bends up to $2\Phi_{\mathrm{B}}$ at the silicon-oxide interface. The same

phenomena can be utilized for the analysis of the uniformly doped carrier concentration in the substrate. For the analytical modeling of the 2-D characteristics of DG MOSFETs, the two-dimensional Poisson's equations are analyzed by using suitable initial and final boundary conditions. Concept of Green's function techniques are used to get the solution for the two-dimensional Poisson's equation considering the uniform doping profile. The modeling of DG MOSFET's reported by authors [13–19]. For the optimization of the performance of the devices in nanometer regime for low power applications, V_{th} of the DG MOSFETs should be properly modeled. The analytical expression for 2-Dimensional V_{th} in the substrate is derived explicitly and verified by previous existing 2-Dimensional analytical models.

2 Structure of DG MOSFET

Figure 1 discusses the general structure of DG MOSFETs. In this structure of DG MOSFET 2 gates are used. Coupling is enhanced between gate to channel and hence short channel effects are considerably suppressed. DG MOSFETs are categorized as either symmetric DG MOSFET or asymmetric depends upon the voltages are applied to both gates. These two metal gates may or may not have same work functions. In this research work, analysis is done for symmetric DG MOSFETs. The symmetric DG MOSFETs means work function is similar for both gates. The thickness of the gate oxide is equal with same bias voltage is applied. After application of V_{ds}, V_{gs}, and with constant Quasi-Fermi level is shown in Fig. 1.

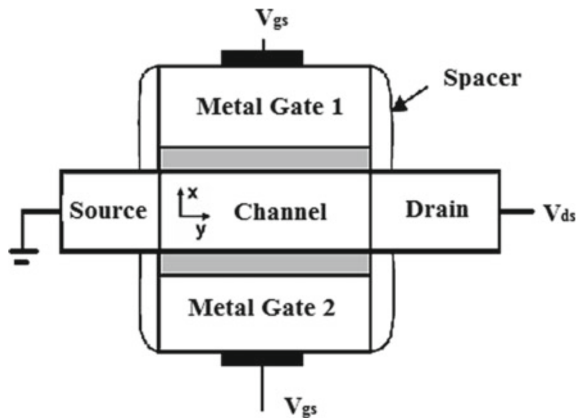

Fig. 1 Structure of general DG-MOSFET

3 Modeling of DG-MOSFET

3.1 he Basic Analysis

The cross-sectional view of a thin-film Dual Gate MOS device for two-Dimensional analytical model is shown in Fig. 2. The simplified domains for the analytical solution for the 2D Poisson's equations [20–23] along with the suitable boundary conditions are shown in Eq. (1). The below equation shows the 2D Poisson's equation with respect to rectangular coordinate system.

$$\Delta^2\varnothing(x, y) = -\frac{\rho(x, y)}{\varepsilon_{si}} = \frac{qN_A f(y)}{\varepsilon_{si}}, 0 \le y \le t_{si}, 0 \le x \le L$$

where N_A is substrate acceptor and $f(y)$ is doping profile in Si area. The 2-D Poisson's equations are converted into 2-D Laplace equations in the back and front oxide regions.

$$\left.\begin{array}{ll} \emptyset(0, y) = V_{bi}(y) & 0 < y < t_{si} \\ \emptyset(L, y) = V_{bi}(y) + V_{ds} & 0 < y < t_{si} \\ D_{sf}(x, 0) = \epsilon_{si}\ E_y(x, 0) & 0 < x < L \\ D_{sb}(x, t_{si}) = \epsilon_{si}\ E_y(x, t_{si}) & 0 < x < L \end{array}\right\} \tag{1}$$

$$\begin{aligned} E_y(x, 0) &= \frac{\partial\phi(x, y)}{\partial y} = \frac{C_{ox}}{\varepsilon_{si}}\left[V_{gs} - V_{fb} - \phi_s - \frac{Q_0}{C_{ox}}\right], \\ E_y(x, t_{si}) &= \frac{\partial\phi(x, y)}{\partial y} = -\frac{C_{ox}}{\varepsilon_{si}}\left[V_{gs} - V_{fb} - \phi_s - \frac{Q_0}{C_{ox}}\right] \end{aligned} \tag{2}$$

The concept of Green's function technique is utilized for solution of the 2-Dimensional Poisson's potential distribution. Simplifying the Green's function

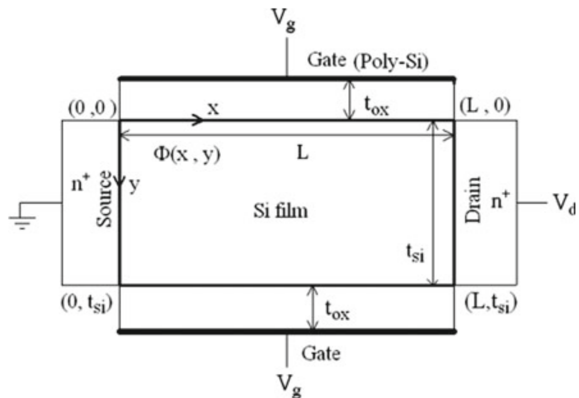

Fig. 2 Cross section view of DG-MOSFET

solution into Green's theorem [16], this is shown below

$$\emptyset(x,y)=\iint\frac{\rho(x',y')}{\varepsilon}G(x,y;x',y')\mathrm{d}x'\mathrm{d}y' + \int G(x,y;x',y')\frac{\partial\phi}{\partial n'}\mathrm{d}s' - \int\Phi(x',y')\frac{\partial G}{\partial n'}\mathrm{d}s' \tag{3}$$

where $G(x, y; x', y^{'})$ is the Green's function satisfying $\Delta^2 G = -\delta(x-x^{'})\delta(y-y^{'})$, $n^{'}$ is the outward direction.

$$G_x(x,y;x',y')=\frac{2}{L}\sum_{n=1}^{\infty}\frac{\sin(K_n x')\sin(K_n x)\sinh(K_n y)\sinh K_n(t_{si}-y')}{K_n\sinh K_n t_{si}}, y<y' \tag{4}$$

$$G_x(x,y;x',y')=\frac{2}{L}\sum_{n=1}^{\infty}\frac{\sin(K_n x')\sin(K_n x)\sinh(K_n y')\sinh K_n(t_{si}-y)}{K_n\sinh K_n t_{si}}, y>y' \tag{5}$$

$$G_y(x,y;x',y')=\frac{2}{t_{si}}\sum_{m=1}^{\infty}\frac{\sin(K_m y')\sin(K_m y)\sinh(K_m x)\sinh K_m(L-x')}{K_m\sinh K_m L}, x<x' \tag{6}$$

$$G_y(x,y;x',y')=\frac{2}{t_{si}}\sum_{m=1}^{\infty}\frac{\sin(K_m y')\sin(K_m y)\sinh(K_m x')\sinh K_m(L-x)}{K_m\sinh K_m L}, x>x' \tag{7}$$

Equation (3) is expression for electrostatic potential distribution and $\rho(x', y^{'}) = -qN_A f(y^{'})$ defined as the charge density of Si region. Assuming uniform doped $(f(y^{'}) = 1)$. 2D potential equation is shown below.

$$\emptyset(x,y)=\frac{(-qN_A)}{(2\varepsilon_{si})}x(L-x)+V_{bi}+V_{ds}\frac{x}{L} + \sum_{n=1}^{\infty}\frac{(\sin K_n x)}{\varepsilon_{si}k_n\sinh k_n t_s i}\left[D_{sf}^m\cosh k_n(t_{si}-y)-D_{sb}^m\cosh k_n y\right] \tag{8}$$

where D_{sf}^m and D_{sb}^m is electric displacement of front & back gate. The $\varnothing(x, y)$ have to satisfy the boundary conditions,

$$\left.\frac{\partial\phi(x,y)}{\partial x}\right|_{y=0^+}-\left.\frac{\partial\phi(x,y)}{\partial x}\right|_{y=0^-}=0 \tag{9}$$

$$-\varepsilon_{si}\frac{\partial\phi(x,y)}{\partial y}\bigg|_{y=0^+}+\varepsilon_{ox}\frac{\partial\phi(x,y)}{\partial y}\bigg|_{y=0^-}=0 \tag{10}$$

After solving Eqs. (9) and (10) and we can obtain

$$D_{sf}^{m}=\frac{\varepsilon_{ox}[B.D\varepsilon_{si}k_n\sinh k_n t_{si}-C.\sin K_n x]}{[B.\varepsilon_{si}\sinh k_n t_{si}+B.\varepsilon_{ox}\cosh k_n t_{si}-A.\varepsilon_{ox}].\sin K_n x} \tag{11}$$

where coefficients

$$A=\frac{\sin K_n x}{K_n}\left\{\frac{1}{\varepsilon_{ox}}+\frac{1}{\varepsilon_{si}\tanh k_n t_{si}}-\frac{1}{\varepsilon_{si}\sinh k_n t_{si}}\right\},$$
$$B=\frac{\sin K_n x}{K_n}\left\{\frac{1}{\varepsilon_{si}\sinh k_n t_{si}}-\frac{1}{\varepsilon_{si}\tanh k_n t_{si}}-\frac{\tanh k_n t_{ox}}{\varepsilon_{ox}}\right\} \tag{12}$$

$$C=\frac{2\sin K_m t_{ox}}{t_{ox}K_m\sinh k_m L}\{V_{bi}\sinh K_m(L-x)+(V_{bi}+V_{ds})\sinh K_m x\}$$
$$D=\frac{4(V_{gs}-V_{fb})\sinh K_n x}{n\pi\cosh k_n t_{ox}}+\frac{qN_A}{2\varepsilon_{si}}x(L-x)-V_{bi}-V_{ds}\frac{x}{L} \tag{13}$$

3.2 Threshold Voltage Model

The location of X_{min} lies on Si surface

$$\frac{\partial\Phi(x,y)}{\partial x}\bigg|_{x=x_{\min},y=0,t_{si}}=0 \tag{14}$$

From Eq. (9), the position of the minimum surface potential x_{min} is

$$\frac{\varepsilon_{ox}\cosh k_n t_{si}}{E}\left\{\frac{qN_A}{\varepsilon_{si}}\frac{x_{\min}(L-x_{\min})K_n}{\tan K_n x_{\min}}-\frac{qN_A}{2\varepsilon_{si}}x_{\min}(L-2x_{\min})\right.$$
$$\left.-\frac{V_{ds}}{L}-\frac{2V_{ds}}{L}\frac{x_{\min}K_n}{\tan K_n x_{\min}}-\frac{2V_{bi}K_n}{\tan K_n x_{\min}}+\frac{4(V_{gs}-V_{fb})}{L.\cosh k_n t_{ox}\tan K_n x_{\min}}\right\}$$
$$-\frac{qN_A}{2\varepsilon_{si}}x_{\min}(L-2x_{\min})+\frac{V_{ds}}{L}=0 \tag{15}$$

the expression for minimum surface potential $\phi_{sf,\min}$ is simplified as from above Eq. (15)

$$\Phi_{\min}(x_{\min},0)=\frac{-qN_A}{2\varepsilon_{si}}x_{\min}(L-x_{\min})+V_{bi}+V_{ds}\frac{x_{\min}}{L}$$

$$+\sum_{n=1}^{\infty}\frac{\sin K_n x_{\min}}{\varepsilon_{si}k_n \sinh k_n t_{si}}\left[D_{sf}^{m}\cosh k_n t_{si}-D_{sb}^{m}\right]=\Phi_{s,\min} \tag{16}$$

The V_{th} for the DG-MOSFET is derived from [24]. The V_{th} in terms of surface potential is expressed by

$$V_{\text{th}}=V_{fb}+\left\{2\Phi_f+\frac{-qN_A}{2\varepsilon_{si}}x_{\min}(L-x_{\min})-V_{bi}-V_{ds}\frac{x_{\min}}{L}\right\}\frac{\{\sin K_n x_{\min}\}^{-1}}{2G_f}-\frac{P}{2G_f} \tag{17}$$

where

$$G_f=\left[1-(-1)^n\right]\frac{R}{d_0}\left[\frac{2}{m\pi\cosh k_n t_{ox}}+\sum_{m=1}^{\infty}\frac{t}{(m-.5)\pi}\left[(-1)^m-\frac{1}{(m-.5)\pi}\right]\right],$$
$$R=-\frac{\varepsilon_{si}}{\varepsilon_{ox}}\frac{\tanh k_n t_{ox}}{\sinh k_n t_{si}},\ t=\frac{4}{n\pi}\left[1+\frac{L^2(m-.5)^2}{t_{ox}^2 n^2}\right] \tag{18}$$

$$d_0=\frac{1}{(\sinh k_n t_{si})^2}-\left\{\frac{\varepsilon_{si}\tanh k_n t_{ox}}{\varepsilon_{ox}}+\frac{1}{\tanh k_n t_{si}}\right\}^2,$$
$$P=\frac{1}{d_0}\left\{\left[1-(-1)^n\right]\frac{qN_A L^2}{2\varepsilon_{si}}\frac{8R}{(n.\pi)^3}+T\left[V_{bi}\left(1-(-1)^n\right)+V_{ds}(-1)^{n+1}\right]\right\} \tag{19}$$

$$T=\sum_{m=1}^{\infty}2Rt((m-.5)\pi)^{-2}-\frac{4R}{n\pi} \tag{20}$$

$$V_{th,\text{long}}=V_{fb}-\frac{P}{2G_f} \tag{21}$$

The threshold voltage roll-off ΔV_{th} expression is the difference between the values of threshold voltage for short channel and long-channel devices given as

$$\Delta V_{\text{th}}=\left\{2\Phi_f+\frac{-qN_A}{2\varepsilon_{si}}x_{\min}(L-x_{\min})-V_{bi}-V_{ds}\frac{x_{\min}}{L}\right\}\frac{\{\sin K_n x_{\min}\}^{-1}}{2G_f} \tag{22}$$

4 Results and Discussion

Figures 3 and 4 shows the various levels of threshold voltage roll-off ΔV_{th} in the substrate the length of the channel length for various values of *Si* film t_{si}= (1.5, 5,

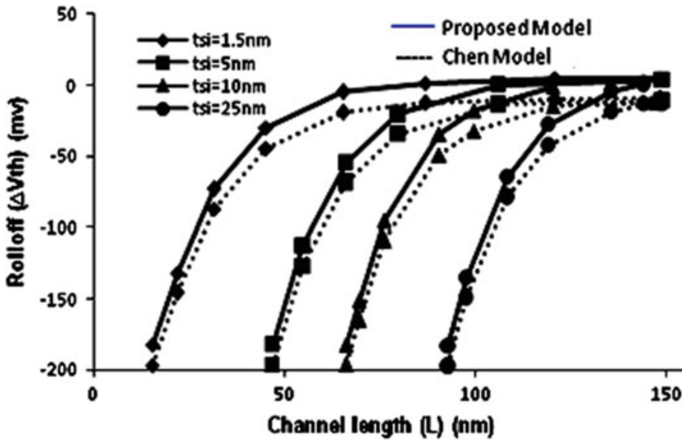

Fig. 3 Proposed design compared with Chen [24], $t_{ox} = 1$ nm

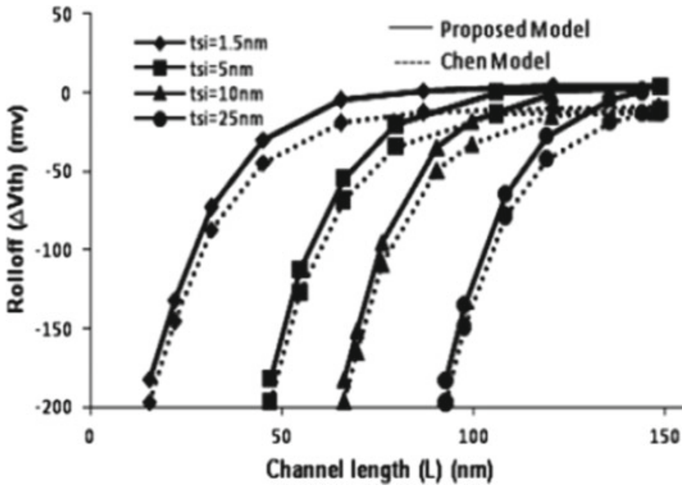

Fig. 4 Proposed design compared with Chen [24], $t_{ox} = 1.5$ nm

10, and 25 nm) at Gate $t_{ox} = 1$ nm and $t_{ox} = 1.5$ nm at same $V_{ds} = 0.05$ V and $N_a = 10^{17}$ cm^{-3} for proposed analytical model and Chen [24]. The V_{th} roll-off increases with increase in t_{si}. With the increase in silicon film thickness, the curves are shifted towards right side for constant $V_{ds} = 0.05$ V and constant gate $t_{ox} = 1$ nm and $t_{ox} = 1.5$ nm. The proposed model shows Threshold Voltage roll-off ΔV_{th} is 5–7% greater than Chen design.

Figure 5 shows the parametric analysis for threshold voltage roll-off for various drain bias voltages V_{ds}= (0.005, 1.0 V) and the parameters are $t_{ox} = 1.5$ nm and silicon film thickness $t_{si} = 10$ nm. Figures 3, 4, and 5 shows the threshold voltage

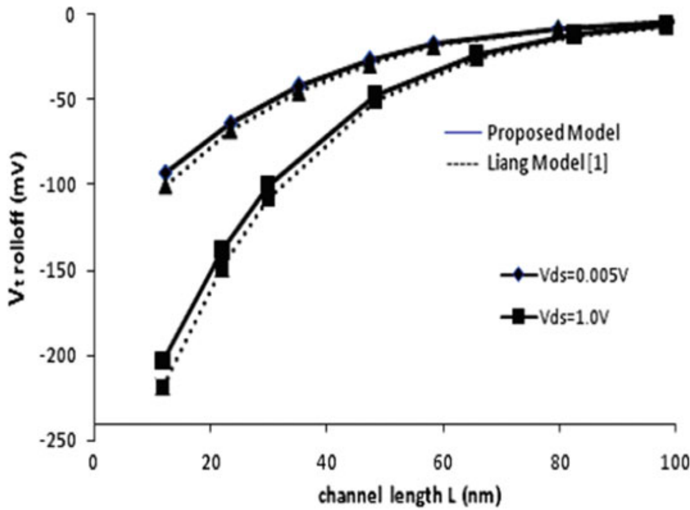

Fig. 5 Proposed design compared with Liang [1], $t_{si} = 10$ nm and $t_{ox} = 1.5$ nm

roll-off ΔV_{th}. The proposed model accurately predicts the device behavior compared with the existing works Liang [1] and Chen [24], with 3–5% more accurate.

5 Conclusion

The two-dimensional Poisson's equations have been analytically derived using the concept of Green's function incorporating suitable initial and final boundary conditions in Silicon area. The accuracy of the proposed model in the substrate (Si-film) is analyzed and verified by existing models. This design is valid for uniform doping profile in Si area. Due to the symmetry of DG-MOSFETS, the distributions of analytic potential for both sides of the surfaces in the substrate are same. It is obvious from simulation results so as to iterative method can only be used to find the minimum surface potential. It can be easily analyzed that better results are produced between the proposed and Chen [24] design analysis for parametric analysis of device structure for various biasing. The proposed analytic voltage model can be applied as a basic concept for high-speed physical analysis of the short-channel effects. It will define the deep-sub micrometer optimized scaling rule for thin-film Silicon on Insulator based MOS transistor in ULSI Technology.

References

1. Jiang, C., Liang, R., Wang, J., Xu, J.: A two-dimensional analytical model for short channel junctionless double-gate MOSFETs. AIP Adv **5**(5), 0571223-13 (2015)
2. Gupta, K.A., Anvekar, D.K., Venkateswarlu, V.: Modeling of short channel MOSFET devices and analysis of design aspects for power optimization. Int. J. Model. Optim. **3**(3), 266–271 (2013)
3. Avci, U.E., Morris, D.H., Young, I.A.: Tunnel field-effect transistors: prospects and challenges. J. Electr. Dev. Soc. **3**(3), 88–95 (2015)
4. Narendiran, A., Akhila, K., Bindu, B.: A physics-based model of double-gate tunnel FET for circuit simulation. IETE J. Res. **62**(3) (2016)
5. Hosseini, R.: Analysis and simulation of a junctionless double gate MOSFET for high-speed applications. **67**(9), 1615–1618 (2015)
6. Salmani-Jelodar, M., Ilatikhameneh, H., Kim, S., Ng, K., Klimeck, G.: Optimum high-k oxide for the best performance of ultra-scaled double-gate MOSFETs. IEEE Trans. Nanotechnol. 1–5 (2015)
7. Ture, E., Brückner, P., Godejohann, B.-J., Aidam, R., Alsharef, M., Granzner, R., Schwierz, F., Quay, R., Ambacher, O.: High-current submicrometer tri-gate GaN high-electron mobility transistors with binary and quaternary barriers. J. Electr. Dev. Soc. **4**(1), 1–6 (2016)
8. Bauman, S.J., Novak, E.C., Debu, D.T., Natelson, D., Herzog, J.B.: Fabrication of sub-lithography-limited structures via nanomasking technique for plasmonic enhancement applications. IEEE Trans. Nanotechnol. **14**(5), 790–793 (2015)
9. Saha, S.K.: Modeling statistical dopant fluctuations effect on threshold voltage of scaled JFET devices. IEEE Access J. **4**, 507–513 (2016)
10. Xie, Q., Lee, C.-J., Xu, J., Wann, C., Sun, J.Y.-C., Taur, Y.: Comprehensive analysis of short-channel effects in ultrathin SOI MOSFETs. IEEE Trans. Electr. Dev. **60**(6), 1814–1819 (2013)
11. Colinge, J.-P.: Multiple-gate SOI MOSFETs. Solid-State Electron. **48**(6), 897–905 (2004)
12. Cros, A., Romanjek, K., Fleury, D., Harrison, S., Cerutti, R., Coronel, P., Dumont, B., Pouydebasque, A., Wacquez, R., Duriez, B., Gwoziecki, R., Boeuf, F., Brut, H., Ghibaudo, G., Skotnicki, T.: Unexpected mobility degradation for very short devices : a new challenge for CMOS scaling. IEEE Int. Electr. Dev. Meet. 663–666 (2006)
13. Rajabil, Z., Shahhoseini, A., Faez, R.: The non-equilibrium green's function (NEGF) simulation of nanoscale lightly doped drain and source double gate MOSFETs. In: IEEE International Conference on Devices, Circuits and Systems (ICDCS), pp. 25–28 (2012)
14. Karatsori, T.A., Tsormpatzoglou, A., Theodorou, C.G., Ioannidis, E.G., Haendler, S., Planes, N.G.: Development of analytical compact drain current model for 28nm FDSOI MOSFETs. In: 4th International Conference on Modern Circuits and Systems Technologies, Thessaloniki Greece, pp 1–4,14–15 (May 2015)
15. Tripathi, S.L., Kumar, M., Mishra, R.A.: 3-D channel potential model for doped symmetrical ultra-thin quadruple gate-all-around MOSFET. J. Electr. Dev. **21**, 1874–1880 (2015)
16. Ávila-Herrera, F., Cerdeira, A., Paz, B.C., Estrada, M., Íñiguez, B., Pavanello, M.A.: Compact model for short-channel symmetric double-gate junction-less transistors. Solid-State Electron. **111**, 196–203 (2015)
17. Zhang, G.-M., Su, Y.-K., Hsin, H.-Y., Tsai, Y.-T.: Double gate junctionless MOSFET simulation and comparison with analytical model. In: IEEE Regional Symposium on Micro and Nanoelectronics (RSM-2013), Langkawi, Malaysia, pp. 410–413, 25–27 (2013)
18. Yadav, V.K.S., Baruah, R.K.: An analytic potential and threshold voltage model for short-channel symmetric double-gate MOSFET. In: International Symposium on VLSI Design and Test, Coimbatore, India, 16–18 July, 2013
19. Bhartia, M., Chatterjee, A.K.: Modeling the drain current and its equation parameters for lightly doped symmetrical double-gate MOSFETs. J. Semicond. **36**(4), 1–7 (April 2015)
20. Liang, X., Taur, Y.: A 2-D analytical solution for SCEs in DG MOSFETs. IEEE Trans. Electr. Dev. **51**(9), 1385–1391 (2004)

21. Lo, S.-C., Li, Y., Shao-Ming, Yu.: Analytical solution of nonlinear poisson equation for symmetric double-gate MOSFET. Math. Comput. Model. **46**(1–2), 180–188 (2007)
22. Chiang, T.K.: A novel scaling-parameter-dependent sub threshold swing model for double-gate (DG) SOI MOSFETs: including effective conducting path effect (ECPE). Semicond. Sci. Technol. **19**(12), 1386–1390 (2004)
23. Huaxin, Lu., Taur, Y.: An analytic potential model for symmetric and asymmetric DG-MOSFETs. IEEE Trans. Electr. Dev. **53**(5), 1161–1168 (2006)
24. Chen, Q., Harrell, E.M., Meindl, J.D.: A physical short-channel threshold voltage model for undoped symmetric double-gate MOSFETs. IEEE Trans. Electron Dev. 50(7) (2003)
25. Maheshwari, V., Malipatil, S., Gupta, N., Kar, R.: Modified WKB approximation for Fowler-Nordheim tunneling phenomenon in nano-structure based semiconductors. In: 2020 International Conference on Emerging Trends in Information Technology and Engineering (ic-ETITE), Vellore, India, 2020, pp. 1–5. https://doi.org/10.1109/ic-ETITE47903.2020.460