Chapter 15
Power Quality Enhancement in Single Stage Non-inverted Output Bridgeless Buck–Boost Converter

J. Gnanavadivel, S. Muralidharan, and S. Joe Magellah

Abstract This research manuscript proposes a bridgeless single phase buck–boost power factor correction converter providing non-inverted DC load voltage. Proposed topology has two power switches in the current path over every switching period, and moreover, this topology does not have bridge rectifier at the input side. Therefore, it leads to improved thermal management and reduced conduction losses. This further increases the efficiency of the system. The suggested converter offers unity input as it is operated in discontinuous conduction mode. Harmonic content in supply current is greatly reduced improving the power quality indices to the recommended standard. In this manuscript, performance analysis of the proposed converter is observed, and its implementation is compared with standard buck–boost converter.

Keywords Power factor correction (PFC) · Discontinuous conduction mode · (DCM) · Bridgeless buck–boost converter · Total harmonic distortion (THD)

15.1 Introduction

In recent years, in order to stoke up the power factor, in AC-DC conversion, the roles of power factor correction converters are predominant. Harmonic present in line current is reduced greatly [1]. With the intention to enhance the efficiency of the system or a transmission line, the power factor at the load side has to be maintained near unity. If power factor gets diminished outside certain limits, then the consumer has to pay additional cost as the active power utilized by the consumer will get increased.

In the conventional AC-DC converter, the presence of diode bridge rectifier (DBR) induces a high conduction loss which in turn reduces the system efficiency. Therefore, we go for bridgeless PFC converter with more modest quantity of active switches operated during every switching period. Also, the abolition of input DBR in bridgeless topology trim down the conduction losses, size and cost associated

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R. Seyezhai et al. (eds.), *Recent Trends in Renewable Energy Sources and Power Conversion*, Springer Proceedings in Energy,
https://doi.org/10.1007/978-981-16-0669-4_15

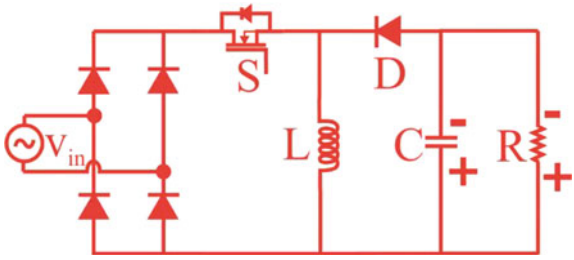

Fig. 15.1 Buck–boost converter of conventional nature

with the system. In this context, various AC-DC power converters-based bridgeless configuration have been analysed in [2].

For power factor correction, the conventional boost [3] and buck converter are the most popular front-end converters. However, they have issues like inadequate feature in current shaping and cycle restrictions. The PFC converter at the power conversion always offers a high voltage in output side comparative to the entry side and does not give wide range of input voltage regulation, deprived load efficiency while operating in universal input voltage. This creates challenge while operating boost converter as universal PFC converter [4, 5]. The buck PFC converter can step down the voltage to support small output voltage applications, but they cannot bear the input current during the course of the cycle and highly distort the line current. But the buck–boost PFC bridgeless converter does both the buck and boost operation offering a wide span of input voltage regulation, low distortion of line current with high efficiency, improved power factor and reliable operation. There are various topologies of buck–boost converter available for PFC applications. Buck–boost converter of conventional nature is shown in Fig. 15.1 with the presence of DBR.

15.2 Proposed System

A new single stage buck–boost PFC converter offering positive output voltage is introduced in this paper. The suggested converter is made to operate discontinuous conduction mode (DCM). Usually, the PFC converters are considered to function in (CCM)/(DCM) [6]. Sensing of line voltage/current and DC link voltage is needed in the PFC operating in CCM mode for PFC operation. However, PFC converter in DCM operation needs one sensor needed towards DC link voltage control, and on higher stresses on the switch, the PFC mode operation is realized at the AC mains. Thus, converter for PFC functioning in DCM is chosen for reduced power requirement applications. Venkatesh et al. [6] brief about a novel AC-DC converter with discontinuous conduction mode.

In [6, 7], the PFC converters of buck–boost operation are employed which have output voltage of negative nature. Therefore, an inverting amplifier circuitry which is meant to converter negative voltage to non-inverted voltage is additionally needed [8]. This requirement of extra inverting amplifier circuit increases the cost. In [8, 9],

modified AC-DC sepic converter for power quality correction has been implemented with boost operation only.

In contrary, the authors have implemented a unique buck–boost converter. This manuscript introduces a buck–boost converter of bridgeless nature for PFC applications with positive output voltage, high efficiency, less line current distortion and high power density. DCM operating mode is chosen for this proposed converter topology. Figure 15.2 shows the circuit configuration of single stage buck–boost converter for PFC with inverted output voltage.

To achieve the output voltage of positive nature exclusive of inverse amplifier circuit, polarity of devices involved in the circuit needs to be reassigned in Fig. 15.2, so that we get the proposed bridgeless operation buck–boost converter for PFC as provided in Fig. 15.3. This makes the feedback control circuit simpler with reduced cost compared with buck–boost PFC converter having negative side output voltage requiring an inverse amplifier circuit for feedback control. The proposed PFC-based

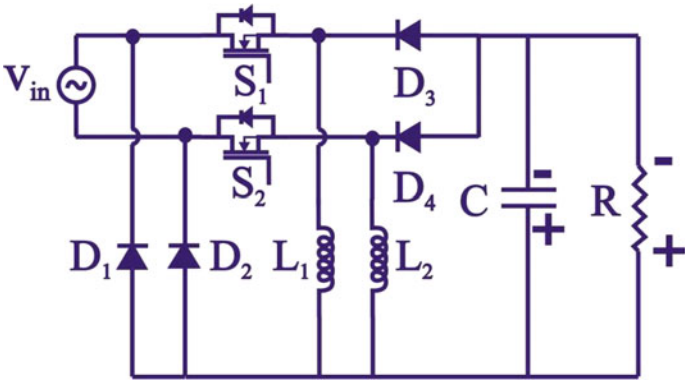

Fig. 15.2 Single stage inverted buck–boost PFC converter

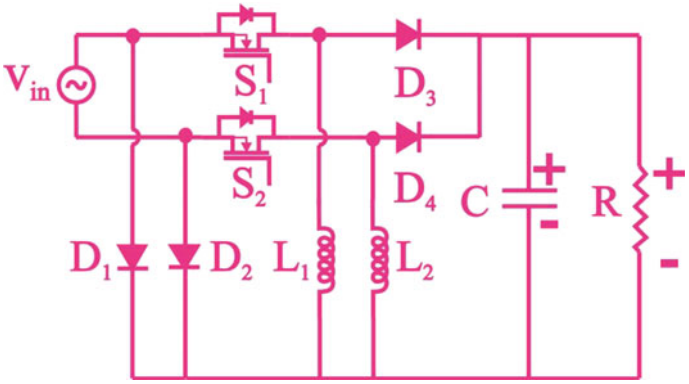

Fig. 15.3 Single stage non-inverted buck–boost PFC converter

single stage buck–boost converter in Fig. 15.3 is made up of diodes ($D3, D4$), switches ($S1$, $S2$) and two inductors ($L1$, $L2$), which are recognized as two buck–boost cells.

15.3 Proposed Single Stage Non-inverted Buck–Boost Converter Providing PFC Operation

Performance of the proposed PFC converter is rendered into two sections. One is input voltage line cycle operation, and another is operation during complete switching cycle.

15.3.1 Input Voltage Line Cycle Operation

In upper half cycle of AC, the S_2 switch is active, and switch S_1 is idle. In other half cycle of AC waveform, the S_1 switch is active, and switch S_2 is inactive. Thus, in positive cycle of AC, the diode D_1, switch S_2 and inductor L_2 are in conduction, and in negative cycle, the diode D_2, switch S_1 and inductor L_1 are in conduction. This proposed converter has three ways of action in AC. Discontinuous nature of inductor current in the proposed converter is shown in Fig. 15.4. In the waveform, the current in inductor is discontinuous for a certain period.

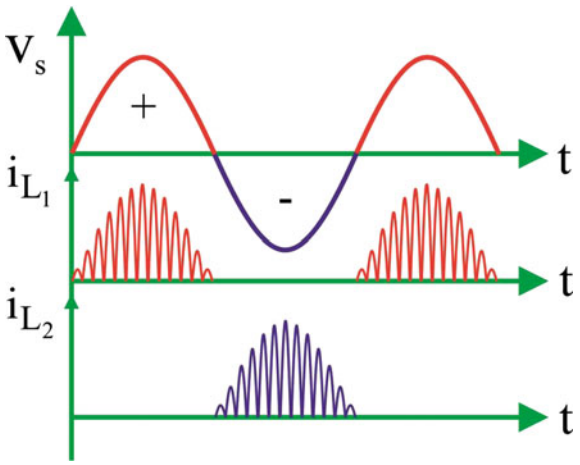

Fig. 15.4 Waveform of supply voltage during upper and lower half cycles

15.3.2 Operation Over a Complete Switching Cycle

The operating cycle of the PFC converter presented has three modes during positive half cycle as well as during negative half cycle.

Mode I: In this Mode I, the diode D_1 gets forward biased and charges the inductor L_2. Then, the current in inductor (i_{L2}) rises. Then, switch S_2 gets closed so that DC link capacitor C_1 discharges to load as presented in Fig. 15.5.

Mode II: Here, stored energy of inductor L_2 gets transferred to C_1, as switch S_2 remains off conditions. This process continues until inductor L_2 completely discharges its stored energy, and so the current via L_2 diminishes and goes to zero as given in Fig. 15.5.

Mode III: Here, current through L_2 turns into zero for the leftover switching interval as no inductor energy is left out. Here, none of the components are conducting except for output side DC link capacitor C_1 which is feeding the DC load. This operating sequence is repetitive whenever S_2 is turned during completion of every switching cycle.

Likewise the identical operation happens in negative cycle of the voltage in supply side with the switch S_1, diode D_2 and inductor L_1 in the conduction state.

15.4 Design of Bridgeless Buck–Boost PFC Converter

The proposed single stage buck–boost PFC converter providing non-inverted DC load voltage is designed to function in DCM in such a way that inductors current becomes discontinuous in switching phase. The bridgeless converter presented is intended for a DC link voltage of 50 V and the power rating of 100 W. For a supply

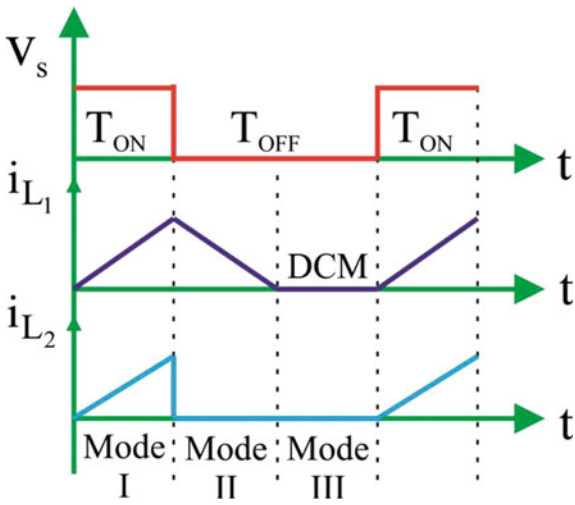

Fig. 15.5 Complete switching cycle waveforms

Table 15.1 Values of parameter for the proposed PFC converter

Parameters	Values
Line voltage (V_{in})	230 V
Output voltage (V_{dc})	50 V
Frequency of switching (f_s)	20 kHz
Duty cycle (D)	18%
Source frequency (f)	50 Hz
Inductor values (L_1, L_2)	50 μH
DC link capacitor ($C1$)	4000 μF
Resistance	23.04

voltage of 230 V, buck–boost converter duty cycle (D) is given as [5], in which V_{dc}—Load voltage and V_{in}—RMS input voltage.

$$D = \frac{V_{dc}}{V_{dc} + V_{in}} \tag{15.1}$$

in which, V_{dc}—Load voltage and V_{in}—RMS input voltage.

The value of input inductors L_1, L_2 of suggested converter that operates in critical mode of conduction is given as [8]

$$L_1, L_2 = \frac{R(1-D)^2}{2f_s} \tag{15.2}$$

where D—duty ratio, R—equivalent resistance in load, representing the duty ratio and f_s—switching frequency.

The DC link capacitor C_1 is given as [8]

$$C_1 = \frac{1}{2\omega\Delta V_{dc}} \tag{15.3}$$

in which ΔV_{dc} is the ripple voltage in DC link. Value of DC link capacitor with permitted ripple of 3% is numerically calculated for obtaining desired values of DC link voltage.

The design parameters required for the converter to manage the DC link voltage are shown in Table 15.1.

15.5 Simulation Results

With an objective to validate the implementation of the proposed system, a comparative simulation study between the conventional and the proposed system is conducted.

15.5.1 Control of Converter

In this system, the control parameter is the voltage. Here, a proportional integral (PI) controller is used for this purpose. The reference voltage (V_{dc}^{*}) is given as

$$V_{dc}^{*} = K_{v} V_{ref}^{*} \tag{15.4}$$

The error voltage generated from the comparator is given as

$$V_{e}(n) = V_{dc}^{*}(n) - V_{dc}(n) \tag{15.5}$$

where n stands for nth sample.

To generate regulated PFC output (VCC) using the error signal (Ve), the expression is given as follows

$$V_{cc}(n) = V_{cc}(n-1) + K\{V_{e}(n) - V_{e}(n-1)\} + K_{i} V_{e}(n) \tag{15.6}$$

in which K_{p} and K_{i} are controller gains of proportional and integral part.

By using Ziegler Nichols method of tuning, the Kp and K_{i} values of the controller are obtained as 0.0001 and 0.25. Implementation of this PI controller helps in getting regulated output voltage from the converter.

15.5.2 Results

The converter topology is simulated using MATLAB implementing the design parameter. Figures 15.6 and 15.7 depict the waveforms obtained from simulation results pertaining to the planned and the conventional converter supplying for 100 W load with a 230 V AC as input. Figures 15.6a and15.7a show the waveforms of supply side current/voltage of proposed power converter and buck–boost PFC converter of conventional nature. Figures 15.6b and 15.7 show the total harmonic distortion of the projected PFC converter and conventional buck–boost PFC converter. Hereby, it is inferred that the planned PFC converter has harmonic distortion of about 1.9% which is less compared to that of the conventional converter which has harmonic distortion about 5.55%.

Graph depicting the effectiveness of the proposed PFC converter for various load power against classic configuration is shown in Fig. 15.8.

The conduction losses are high in diode bridge rectifier-based PFC converter. As the proposed topology does not have any diode bridge, the conduction losses have come done. This results in improved efficiency of the proposed converter. The high value of efficiency for a given load in Fig. 15.8 clearly shows the reduction in losses.

Table 15.2 compares the source current THD of conventional and proposed buck–boost converter with Refs. [10, 11]. It clearly favours the proposed converter as the

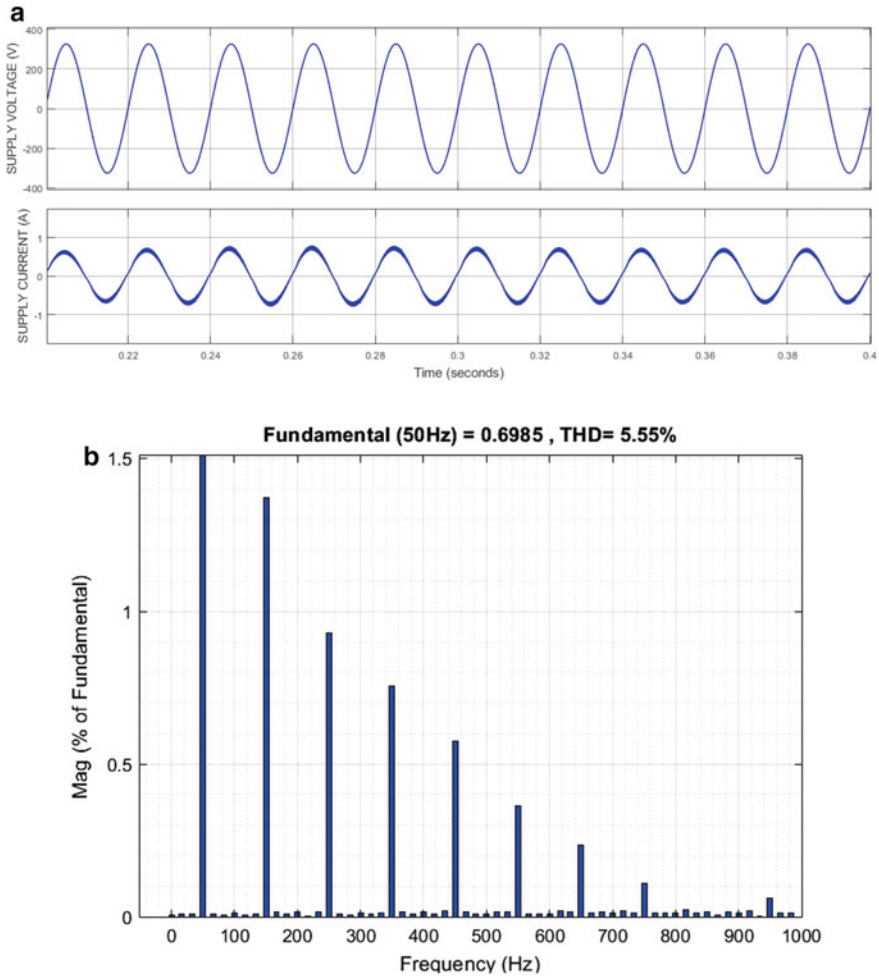

Fig. 15.6 **a** Simulated waveforms of supply voltage/current for buck–boost PFC conventional converter. **b** FFT analysis of total harmonic distortion of the conventional buck–boost PFC converter

THD level is very low compared to others. This reduction in THD level addresses the power quality issues cited in [12–18].

15.6 Conclusion

In this research paper, an innovative topology belonging to buck–boost type bridgeless configuration of PFC converter is proposed and discussed. It is inferred from the implementation of the proposed topology, and due to lower value conduction

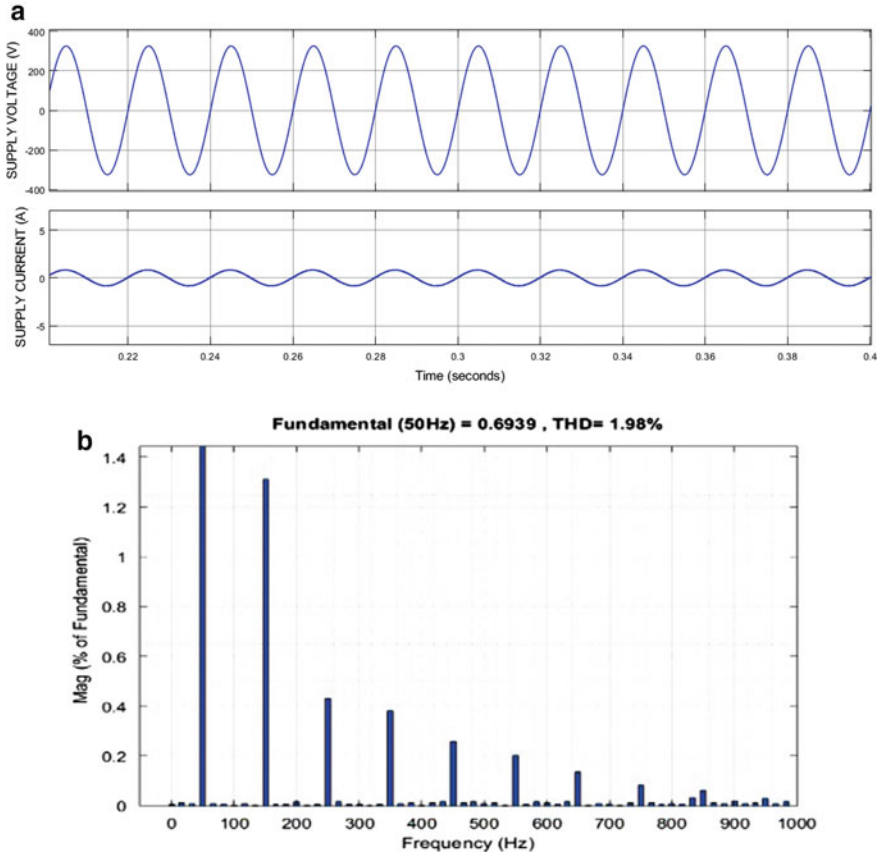

Fig. 15.7 **a** Simulated waveforms of line voltage/ current of the proposed converter. **b** FFT analysis of total harmonic distortion of the proposed bridgeless buck–boost PFC converter

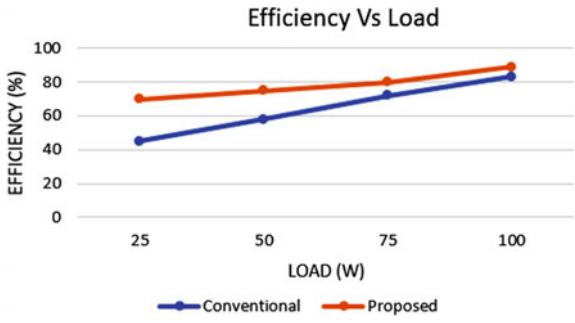

Fig. 15.8 Graph showing the comparison of proposed and the conventional buck–boost PFC converter

Table 15.2 Performance comparison

Parameter	Conventional buck–boost converter	Ref. [10]	Ref. [11]	Proposed buck–boost converter
Source current THD	5.55%	3.39%	14%	1.98%
Input Power Factor	0.98	1	0.98	1

as well as switching losses, there is an increase in the conversion efficiency while comparing with the classical type buck–boost converter for power factor correction. This proposed topology gives positive output voltage eliminating the need of inverse amplifier circuit at the feedback control. The THD is also reduced to below 2%. Thus, the proposed system proves to be more efficient compared to the conventional converters.

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