Design and Performance Analysis of FinFET Based SRAM Cell Stability

Gurpurneet Kaur, Sandeep Singh Gill, and Munish Rattan

1 Introduction

Recently, several minute devices have been developed to satisfy the demand for low power, low cost, reduced area, and high performance. The fabrication and performance analysis of Double-gate (DG) Fin shaped field-effect transistor (FinFET) has been demonstrated for the smaller gate length [12]. The obtained results proved that a FinFET device has been considered as a strong competitor as compared to classical CMOS [3, 7]. The adoption of semiconductor on insulator (SOI) technology for fabricating of microprocessors has become adorable research. Therefore, it is a convenient device for the mobile industry with features of better switching performance to satisfy the need for efficient battery life. Moreover, low power circuit design is a basic requirement in portable devices [8]. A nanoscale FinFET based SRAM cells with appropriate read and write stability are required for satisfying the increasing demand for large data storage, low power dissipation, and high performance [5, 13, 14]. The SRAM cells stability has been greatly affected by process variations, voltage, and temperature fluctuations. The degradation of stabilities has been examined for scaled dimensions and low power behavior of circuits[10, 11].

The endeavor of designing an improved n-FinFET and p-FINFET devices have been taken. The proposed devices demonstrate great improvements for SCEs and

G. Kaur (✉) · S. S. Gill
Guru Nanak Dev Engineering College, Ludhiana, Punjab 141006, India
e-mail: gurpurneetkaur@gmail.com

S. S. Gill
e-mail: ssg270870@yahoo.co.in

M. Rattan
National Institute of Technical Teachers Training and Research, Chandigarh, Punjab 160019, India
e-mail: rattanmunish@gndec.ac.in

© The Author(s), under exclusive license to Springer Nature Singapore Pte Ltd. 2021

H. Singh et al. (eds.), *Sustainable Development Through Engineering Innovations*, Lecture Notes in Civil Engineering 113,
https://doi.org/10.1007/978-981-15-9554-7_50

transconductance. NanoscaleFinFET based SRAM cell devised with six transistors has been simulated using 3D cogenda Technology Computer-Aided Design (TCAD) simulator for low power applications. The stability parameters read static noise margin (RSNM) and write static noise margin (WSNM) have been evaluated using the butterfly method. The dependence of static noise margin (SNM) metrics on voltage and temperature has also been realized for SRAM circuit. This work is organized as follows: Sect. 2 explains the simulation methodology used for designing the device and its circuit; Sect. 3 illustrates the device and circuit performance; Sect. 4 concludes the work done.

2 Design Description and Simulation Methodology of Finfet and Sram Cell

The specifications of nanoscale FinFET device and the SRAM cell have been delineated in Tables 1 and 2, respectively. The three-dimensional simulator cogenda TCAD has been used for devising the device and its circuit. Figure 1 shows the 3D structure of designed n-FinFET and p-FinFETdevices. The gate electrodes, n-polysilicon (4.5 eV), and p-ploysilicon (4.85 eV)have been used for n-FinFET and p-FinFET respectively at 300 K. The SiO_2 is considered as interfacial oxide; aluminium& tungsten is used as metal contacts. Figure 2 outlines the schematic and layout structure of nanoscaleFinFET based SRAM cell. The flow chart of simulation procedure done in visual TCAD has been shown in Fig. 3 [2].

The set of performance metrics have been calculated for the designed FinFET device namely, drain current at maximal value of gate voltage (on-current, I_{ON}), drain current at minimum gate voltage (off-current, I_{OFF}), I_{ON}/I_{OFF} current ratio, drain induced barrier lowering (DIBL) and subthreshold swing (SS). These parameters have been computed with gate voltage (V_g)variation of 0 to 1.0 V and drain voltage (V_d) of 50 mV and 1.0 V as boundary conditions. SS indicates the gate potential requisite for altering the drain current by one decade. Equation (1) states the formula for the evaluation of the SS.

Table 1 Device parameters used in TCAD

Design parameters	n-FINFET	p-FINFET
Gate length, L_g (nm)	24	24
Oxide thickness, T_{ox} (nm)	1.1	1.1
Transistor Fin pitch (nm)	50	50
Transistor Fin width (nm)	12	12
Transistor Fin height (nm)	28	28
Supply voltage (V)	1	1

Table 2 Parameters for an SRAM design

Process parameters	Value
Design rule unit lambda (μm)	0.012
Substrate region thickness (μm)	0.03
Fin height (μm)	0.028
Gate oxide thickness (μm)	0.0011
S/D doping concentration (donor) for nMOS (cm^{-3})	3×10^{20}
S/D doping concentration (acceptor) for pMOS (cm^{-3})	3×10^{20}
Supply voltage, V_d (V)	0.9 V
Thickness of buried oxide (μm)	0.02
Poly-silicon gate thickness (μm)	0.002
ILD dielectric thickness (μm)	0.008
ILD Metal 1 thickness (μm)	0.008
Lateral characteristic length of S/D doping of nMOS (μm)	0.004
Vertical characteristic length of S/D doping of nMOS (μm)	0.003
Doping concentration in *p*-type substrate (cm^{-3})	1×10^{16}
Doping concentration in body (cm^{-3})	1×10^{17}

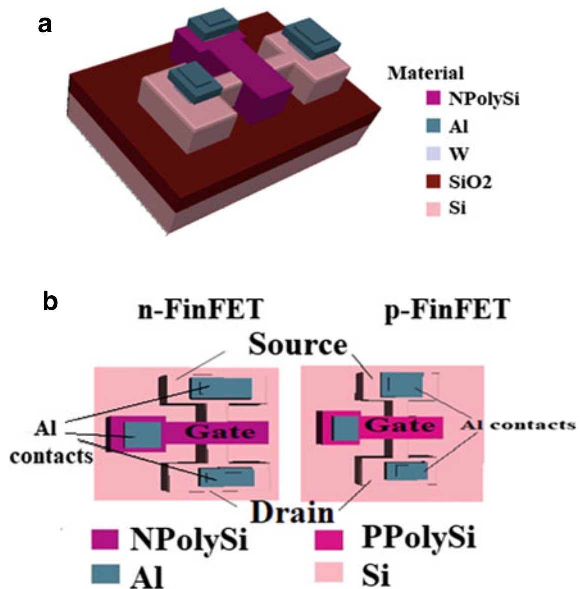
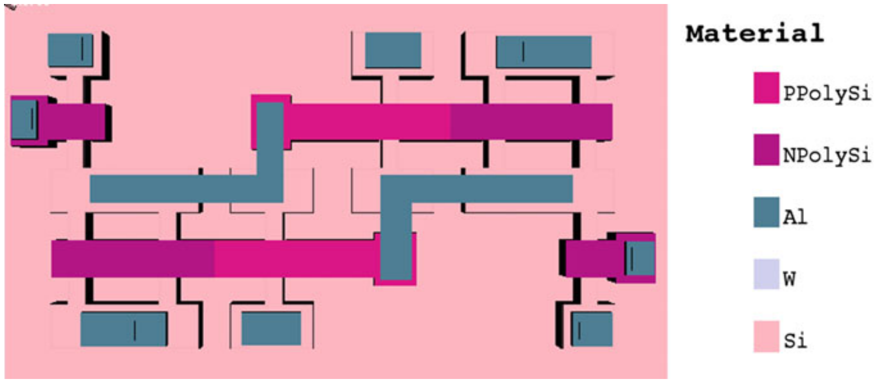
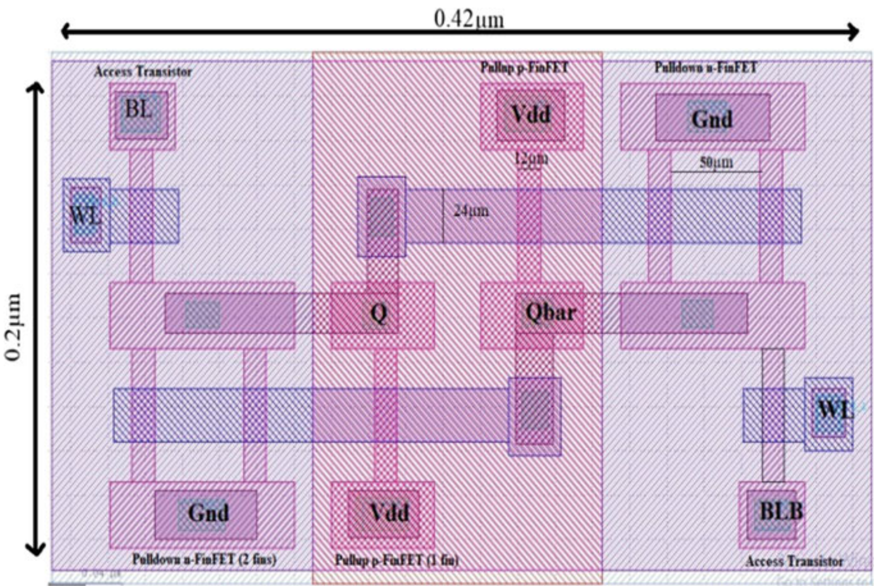


Fig. 1 Bird eye view of 3D SOI FinFET structure: **a** n-FinFET. **b** Top view of n-FinFET& p-FinFET



(a) Schematic



(b) Layout

Fig. 2 Nanoscale FinFET based SRAM cell implemented in TCAD environment. **a** Schematic. **b** Layout

$$SS = \frac{\partial V_g}{\partial \log_{10} I_d} \tag{1}$$

where I_d indicates drain current in amperes. Subthreshold swing manifests the capability of the transistor to overcome the subthreshold regime. DIBL is calculated as the difference of gate voltage corresponding to both 50 Mv and 1 V drain voltage (V_d) at drain current (I_{DIBL}) of 2.83×10^{-7} A which is determined with the formulae

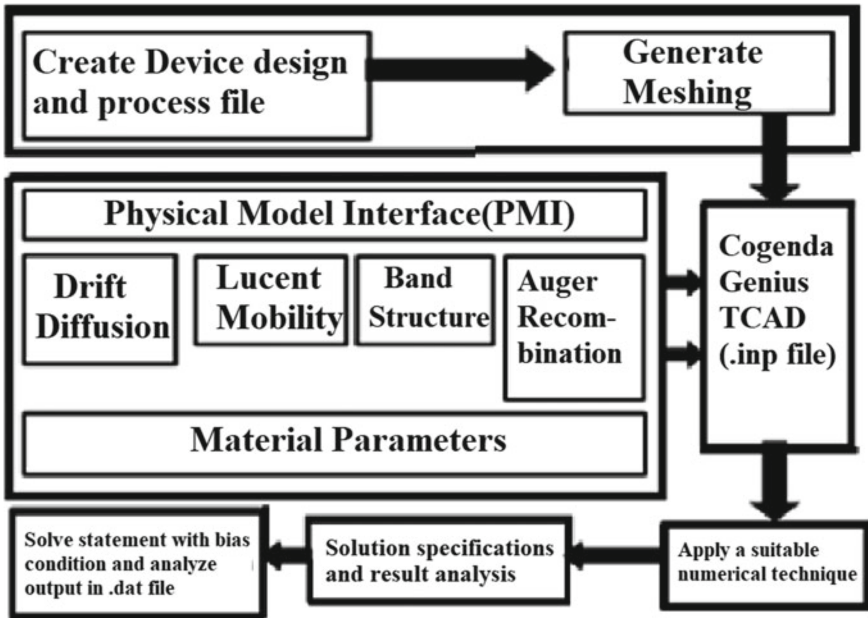


Fig. 3 Flow chart of simulation procedure of visual TCAD

stated in Eq. (2).

$$I_{\mathrm{DIBL}} = \frac{\mathrm{Weff}}{Lg} \times 10^{-7}\ \mathrm{A} \tag{2}$$

$$\mathrm{Weff} = 2H_{\mathrm{Fin}} + W_{\mathrm{Fin}} \tag{3}$$

where L_g is length of gate and Weff is the channel effective width which employs the fin height and fin width as in Eq. (3). Transconductance is evaluated by dividing the changing drain current and the changing gate voltage keeping drain voltage constant. It is expressed as $g_m = (\partial I_{d/}\partial V_g)$ Siemen [1, 6].

The memory circuit performance metrics based on voltage transfer curve include RSNM and WSNM. The ability to read data from SRAM circuit without flipping is characterized by RSNM. It also describes the robustness of SRAM. WSNM is another stability parameter that measures the writing ability of SRAM cells [5, 13, 14].

3 Results and Discussions

(A) *Device Performance*:

The input and output characteristic curves of SOI nanoscale n-FinFET and p-FINFET for different drain voltages are shown in Fig. 4a, b. The VI characteristic of n-FINFET is plotted on the right side of the figure where the similar VI curve for p-FINFET is shown on left side of the figure. It is observed from Fig. 4a that almost the same I_{ON} and I_{OFF} currents are obtained for two devices for similar dimensions in two operating regions i.e. saturation region at $V_d = 0.75$ and linear region at $V_d = 50$ mV. The extracted SCE metrics and transconductance values are mentioned in Table 3[1, 6].

(B) *Circuit Performance*:

(i) The schematic of SRAM cell for read operation is outlined in Fig. 5a. In read operation, the bit-lines (BL and BLB) are biased to supply voltage (V_d) and wordline (WL) is connected to V_d. In this situation, access transistors M5 and M6 are switched on. Let us assume, "1" data is saved at Q, and "0" is saved at Q_{bar}, M1 and M4 devices are switched off and M3 and M2 are switched on. Therefore, current will flow through BLB-M6-M2 as shown in Fig. 5a. Hence, voltage level of bit-line BLB discharges and voltage level of BL maintains at V_d. Figure 6 demonstrates the waveforms for read operation implemented

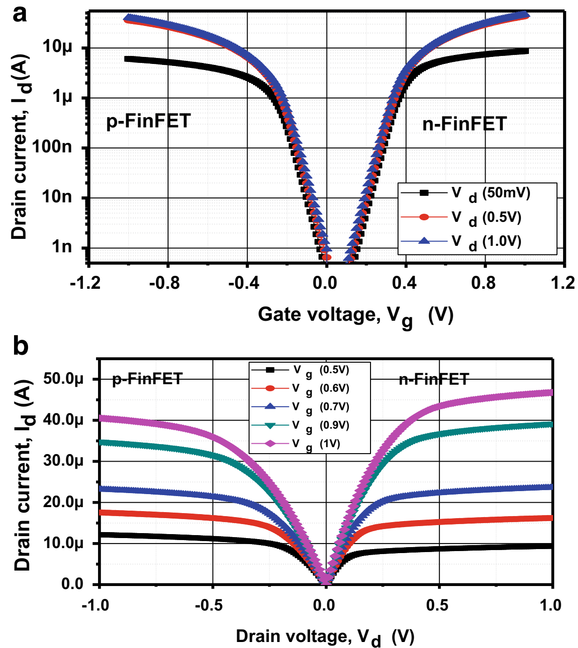


Fig. 4 VI characteristics of n-FINFET and p-FinFET. **a** Input. **b** Output

Table 3 Extracted electrical characteristics of FinFETs

Designed devices	Gate length (nm)	Supply voltage, V_d (V)	I_{ON} (μA)	I_{OFF}	I_{ON}/I_{OFF}	SS (mV/dec)	DIBL (mV/V)	g_m (S) [μA]
n-FINFET	24	1 V	46.8	13.4pA	3.49×10^6	66.5	40	78
		50 mV	8.64	4.71pA	1.83×10^6	65.5		27.3
p-FINFET	24	−1 V	−40.5	95.4nA	4.24×10^4	68.5	42	58
		−50 mV	6.04	33.1nA	1.82×10^4	67		13.2

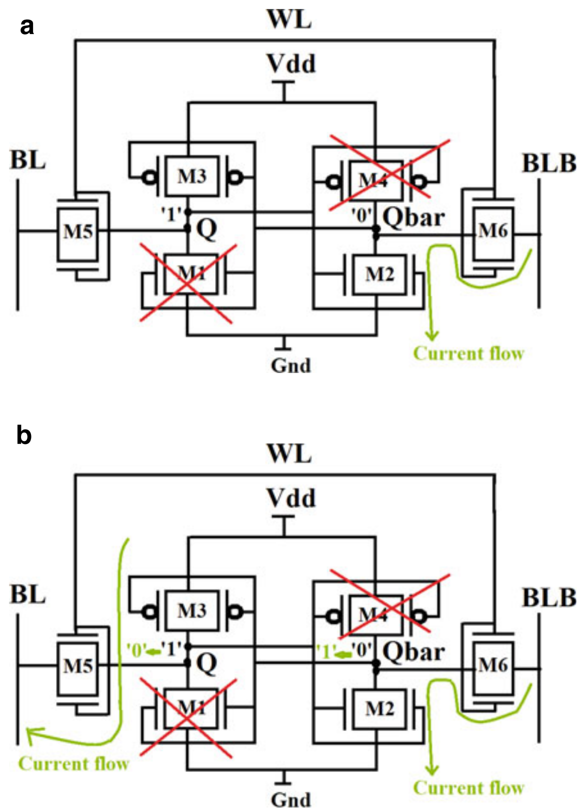
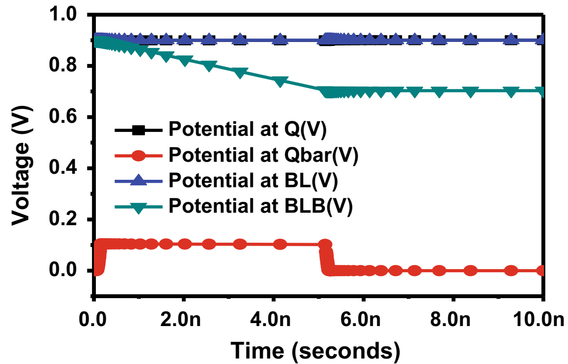
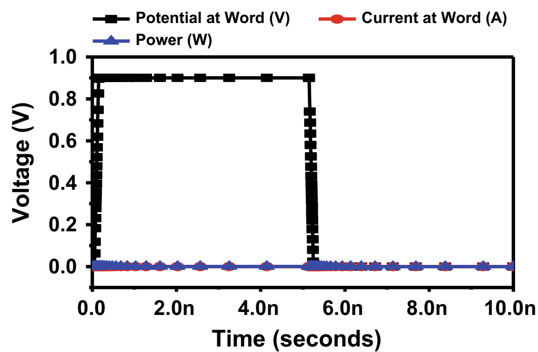


Fig. 5 Operations of 6T SRAM cell using nanoscale FinFET. **a** Schematic diagram for Read operation. **b** Schematic diagram for Write operation

Fig. 6 Waveforms for read operation performed in TCAD for FinFET based 6T SRAM cell



(a) Waveforms showing potential at Q and Qbar output

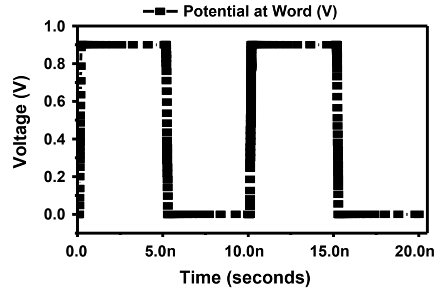


(b) Waveforms showing potential and current at wordline

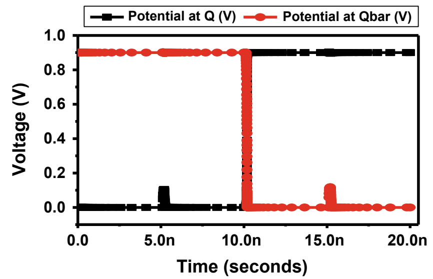
in TCAD environment. Figure 6a displays the potential at different nodes of SRAM cell during read operation where Fig. 6b delineates the current, potential, and power at wordline (WL). Therefore, a successful read operation has been realized for simulated circuits. Figure 5b shows the schematic of designed cell for write operation. In write operation, the voltages of bit-lines (BL and BLB) are opposite to each other, and wordline (WL) is connected to V_d. In this situation, access devices M5 and M6 are switched on. This will drop the voltage level of Qnode and raises the voltage level of Q_{bar} node until the voltage level of Q node is enough to switch on M4 and switch off M2or the voltage level at node Q_{bar} is good enough to switch on M3 and switch off M1. Finally, the voltage level of nodes Qbar and Q will be turned over to '1' and '0', respectively. Figure 7 delineates the waveforms obtained after a successful write operation performed in TCAD for nanoscale FinFET based 6T SRAM cell [9].

(ii) The SRAM circuit stability has been measured by SNM. It is stated as the largest DC margin for which the cell condition does not flip during its access. The butterfly curve method is used for estimating SNM of a bit cell as shown in Fig. 8b corresponding to setup outlined in Fig. 8a. The square fitting method is utilized for determining RSNM. It is the largest square to be fitted in

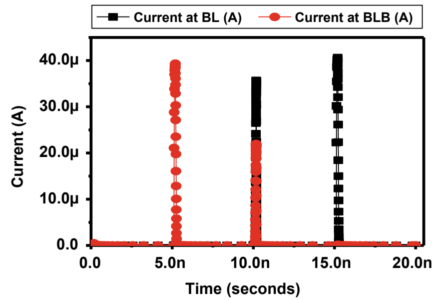
Fig. 7 Waveforms for write operation performed in TCAD for FinFET based 6T SRAM cell



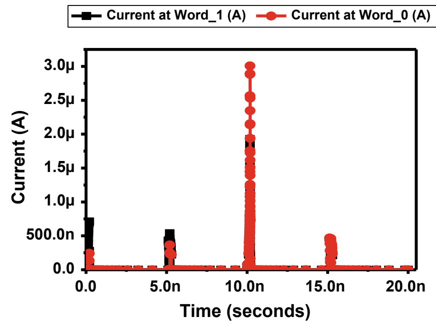
(a) Waveform shows Potential at wordline



(b) Output potential at node Q and Qbar

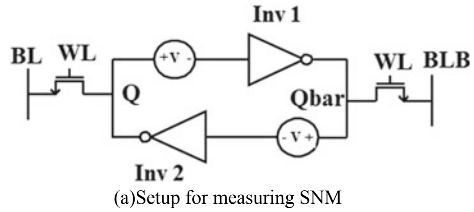


(c) Current waveforms at Bit-lines (BL and BLB)

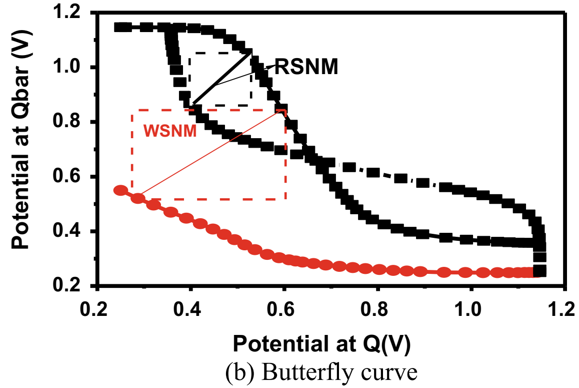


(d) Current waveforms at wordline (WL)

Fig. 8 Butterfly curve method of FinFET based 6T SRAM cell for measuring RSNM and WSNM



(a)Setup for measuring SNM



(b) Butterfly curve

between overlapped plot of inverter transfer characteristics and its inverse characteristics. Similarly, WSNM is extracted as displayed in Fig. 8 [5, 13, 14].

(iii) The dependence of stability on temperature is shown in Fig. 9a. It is noticed that with the increase in temperature, RSNM and WSNM decreases due to increment of the random variation effects because of exponential dependence of current on sub-threshold operation. It is observed that RSNM and WSNM are reduced by 56% and as 16% as temperature varies from 253 to 450 K. The dependence of stability on voltage is illustrated in Fig. 9b. It can be clearly seen that both RSNM and WSNM are degrading for reduced supply voltage which explains the effects of voltage scaling [10, 11].

4 Conclusion

- In this work, the electrical characteristics of nanoscale FinFET devices have been discussed for low supply voltage. It has been noted that simulated devices show 47.4% improvement for DIBL and 7.32% enhancement for SS as compared to results extracted by authors [4].
- Further, low power and miniaturized FinFET based 6T SRAM cell have been demonstrated along with the calculation of SNM values using the butterfly curve method. The progress of WSNM for designed SRAM cell is 8.6% as compared to results demonstrated by researchers [4].

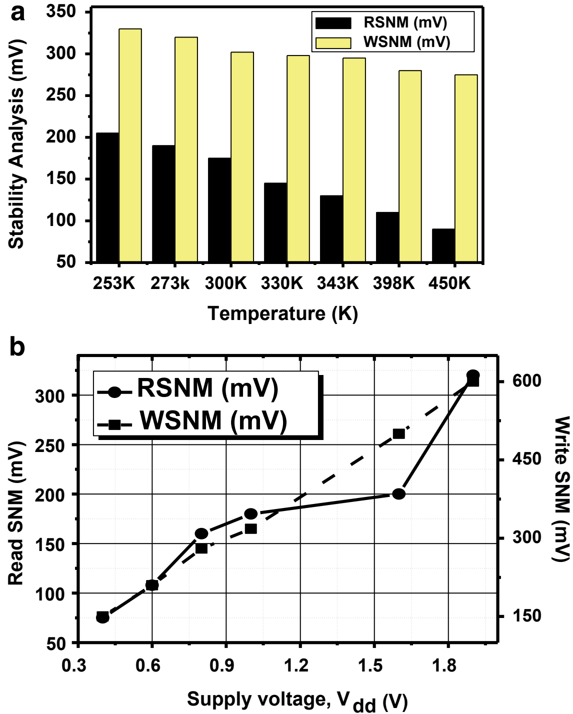


Fig. 9 Dependence of SRAM cell stabilities on temperature and supply voltage. **a** Impact of temperature on stability. **b** Impact of supply voltage on stability

- The impact of voltage and temperature variations on the stability of SRAM cell has also been discussed. The obtained values show improvement as compared to previous work.
- The miniaturized FinFET devices have lower leakage current and reduced power consumption as compared to the planar transistors. Therefore, nanoscaled FinFET technology has been considered as economical, reliable, sustainable, and energy-efficient for future generations. These devices could become an essential part of microprocessors in the future.

Acknowledgements The authors are grateful to MHRD, Govt. of India for sanctioning the grant for the purchase of software used for research work through TEQIP-III to Guru Nanak Dev Engineering College, Ludhiana. Authors would also like to extend gratitude to I. K. Gujral Punjab Technical University, Kapurthala for support in completion of this research work.

References

1. Aujla SK, Kaur N (2019) Optimization of dual-K gate dielectric and dual gate heterojunction SOI FinFET at 14 nm Gate Length. IETE J Res 1–9

2. Cogenda TCAD Tool Suite [Online] (2019). Available http://www.congendatcad.com
3. Colinge JP (ed) (2008) FinFETs and other multi-gate transistors, vol 73. Springer, New York
4. Farkhani H, Peiravi A, Kargaard JM, Moradi F (2014, September) Comparative study of FinFETs versus 22 nm bulk CMOS technologies: SRAM design perspective. In: 2014 27th IEEE International System-on-Chip Conference (SOCC). IEEE, pp 449–454
5. Grossar E, Stucchi M, Maex K, Dehaene W (2006) Read stability and write-ability analysis of SRAM cells for nanometer technologies. IEEE J Solid-State Circ 41(11):2577–2588
6. Kaur G, Gill SS, Rattan M (2020) Whale optimization algorithm for performance improvement of silicon-on-insulator FinFETs. Int J Artificial Intell 18(1):63–81
7. Kim TTH, Vaddi R, Agarwal RP, Dasgupta S (2011) Design and analysis of double-gate MOSFETs for ultra-low power radio frequency identification (RFID): device and circuit co-design
8. Kumar R, Babulu K (2018) Design and performance analysis of low power SRAM using modified MTCMOS G
9. Limachia M, Kothari N (2020) Characterization of various FinFET based 6T SRAM cell configurations in light of radiation effect. Sādhanā 45(1):31
10. Pattanaik M, Birla S, Singh RK (2012) Effect of temperature & supply voltage variation on stability of 9T SRAM Cell at 45 nm technology for various process corners
11. Reddy KN, Jayasree PVY (2019) Low power process, voltage, and temperature (PVT) variations aware improved tunnel FET on 6T SRAM cells. Sustain Comput Inf Syst 21:143–153
12. Solomon PM, Guarini KW, Zhang Y, Chan K, Jones EC, Cohen GM, Krasnoperova A, Ronay M, Dokumaci O, Hovel HJ, Bucchignano JJ (2003) Two gates are better than one [double-gate MOSFET process]. IEEE Circ Devices Mag 19(1):48–62
13. Saun S, Kumar H (2019, October) Design and performance analysis of 6T SRAM cell on different CMOS technologies with stability characterization. In: IOP conference series: materials science and engineering, vol 561, No. 1. IOP Publishing, p 012093
14. Takeda K, Hagihara Y, Aimoto Y, Nomura M, Nakazawa Y, Ishii T, Kobatake H (2005) A read-static-noise-margin-free SRAM cell for low-VDD and high-speed applications. IEEE J Solid-state Circ 41(1):113–121