Achieving Low Resistance Ohmic Contacts to Transition Metal Dichalcogenides (TMDCs)

Anirudh Gajula, Wes Wen Jun Lee, Calvin Pei Yu Wong, and Kuan Eng Johnson Goh

Abstract Transition metal dichalcogenides (TMDCs) harbor great potential for use in high performance electronic devices. However, their practical usage has been hindered by a lack of suitable low resistance ohmic contacts, resulting in high contact resistances and low electron mobilities. Our study aims to investigate the performances of alternative contacts strategies such as exfoliated graphite contacts, bottom-up gold (Au) contacts and evaporated gold-capped indium (In-Au) contacts to exfoliated tungsten disulfide (WS_2) by first fabricating field-effect transistors (FET) and later, conducting transfer line measurements (TLM). Our results show that evaporated gold-capped indium/WS_2 contacts achieved the best ohmic performance out of the three contact strategies with a significantly higher field effect electron mobility of 114 cm^2V^{-1} s^{-1} and a lower contact resistance of 462 k Ω μm to few layer WS_2 and a mobility of 5.45 cm^2V^{-1} s^{-1} and contact resistance of 169 M Ω μm to monolayer WS_2 at room temperature, while graphite/WS_2 contacts and bottom up Au/WS_2 contacts yielded poor non-ohmic characteristics with a field effect electron mobility of 0.0409 and 0.00542 cm^2V^{-1} s^{-1} respectively. Our results also show that low resistance ohmic contacts for WS_2 can be achieved through the direct evaporation of gold-capped indium (In–Au) contacts. This is of current relevance and importance as WS_2 has been found to have a plethora of applications from high mobility field-effect transistors to quantum information processing and the formation of the low resistance ohmic contact is a fundamental step towards achieving these goals.

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1 Introduction

Tungsten disulfide (WS_2), a transition metal dichalcogenide (TMDC), has recently shown great promise in the pioneering field of ultrathin 2D semiconductors. Bulk WS_2 has an appreciable band gap of 1.32 eV, which increases to 1.8 eV for monolayer WS_2 [1] and contributes significantly to its distinct electronic properties and potential to act as ultrathin transistors in various digital circuits. For example, WS_2 has been shown to work as a high mobility field effect transistor [2, 3] and also shown promise in quantum information processing, with the tunable valley polarization that provides an opportunity to control the valley pseudospin [4].

Despite the great promise brought about by the advent of TMDCs, the field remains plagued by significant challenges in the largely unexplored field of solid-state physics. The contacts between 2-dimensional monolayer TMDCs and 3-dimensional metal contacts are known to have high contact resistance, which hinders their potential for practical usage in high-performance devices and microelectronics [5, 6]. Thus, some studies have attempted alternative methods, such as chemical doping methods using lithium fluoride or F4TCNQ to successfully reduce the contact resistance by an order of magnitude [7, 8]. However, it is not clear if these dopants are stable in the long term upon device fabrication.

Recently, it has been shown that weakly interacting van der Waals contacts to TMDC have low contact resistances [5, 9]. Hence, the objective of this study is to investigate van der Waals contacts to WS_2 devices fabricated using 3 different strategies (1) bottom-up graphite contacts, (2) bottom-up gold (Au) contacts, and (3) top-down (evaporated) gold-capped indium (In–Au) contacts. We analyzed these fabrication methods using electron mobilities extracted from field effect transistor measurements and contact resistance extracted from the transfer line measurements. We found that the top-down gold-capped indium (In–Au) contacts resulted in the best device performance with an electron mobility of 114 cm^2V^{-1} s^{-1} and a contact resistance of 462 k Ω μm for few layer WS_2, and an electron mobility of 5.45 cm^2V^{-1} s^{-1} and a contact resistance of 169 M Ω μm for monolayer WS_2.

2 Experimental Design

The first method to achieve van der Waals contacts to WS_2 involves the positioning of the exfoliated WS_2 on top of the two graphite contacts, which are contacted using chromium palladium gold (Cr-Pd-Au) contacts. We expect to have a low contact resistance van der Waals contact between the WS_2 monolayer and the graphite contact. We exfoliated WS_2 monolayers onto Polydimethylsiloxane (PDMS) and transferred

them onto the graphite contacts using a microscope transfer station. The second method involves the direct contact of the monolayer WS_2 on the gold contacts, also using the microscope transfer station. The third method involves the direct metallization of gold-capped indium (In–Au) contacts onto the wafer, using In as a soft non-invasive contacting metal, which has been shown to have a lower contact resistance than directly evaporated titanium gold (Ti–Au) contacts [5]. The direct metallization of gold-capped indium (In-Au) contacts allows for a simple fabrication method for multiple contacts of different channel lengths for the transfer length measurements, which are difficult to achieve using bottom up contacts.

3 Methodology

Figure 1 above shows the device fabrication process for the three types of devices. The exfoliation of WS_2 monolayer flakes was carried out using an adhesive tape (Ultron) onto a polymer layer of polydimethylsiloxane (PDMS, Gelpak X4) from a WS_2 crystal (2D semiconductors, Inc). The identification of the WS_2 monolayers was carried out with an optical microscope (Olympus BX60) using the optical contrast method. Graphite flakes were exfoliated from highly oriented pyrolytic graphite (SPI) onto a 285 nm SiO_2 coated silicon wafer and similarly identified through an optical microscope (Olympus BX60).

Contacts to the graphite flakes were fabricated using electron beam lithography (EBL). First, Polymethyl methacrylate (PMMA) A5 was spin coated onto the exfoliated flakes at 4000 rpm for 90 s. Next, the PMMA was patterned by electron beam lithography (EBL), using an ELS-7000 Elionix at 100 kV, and developed in a 1:3 ratio of methyl isobutyl ketone (MIBK) and isopropyl alcohol (IPA) for 70 s. Then, Cr-Pd-Au contacts were deposited using a Denton Explorer 14 e-beam evaporator at a base pressure of 2E-7 mbar. Lift off was carried out in acetone for 2 h. The graphite break junction of 5 μm for contacting WS_2 was fabricated by etching the exfoliated graphite flake. The exposed areas of the graphite flakes through the PMMA mask were etched off via oxygen-plasma etching at 50 W and 50 mTorr for 60 s. This created graphite contacts that were separated by a 5-micron gap.

The transfer of the WS_2 flakes from the PDMS polymer to the silicon wafer or the graphite break junction was done through a PDMS dry transfer method [10], which involved the mounting of the glass slide containing the WS_2 flakes onto a micromanipulator. The receiving substrate was then heated to a temperature of 80 °C, and the glass slide was carefully lowered down onto the silicon wafer to initiate the transfer process. Lastly, electrical measurements were carried out in a Janis vacuum probe station (pressure 5E-5 mbar), using two Keithley 2450 for the source-drain-gate measurements, as illustrated in Fig. 2.

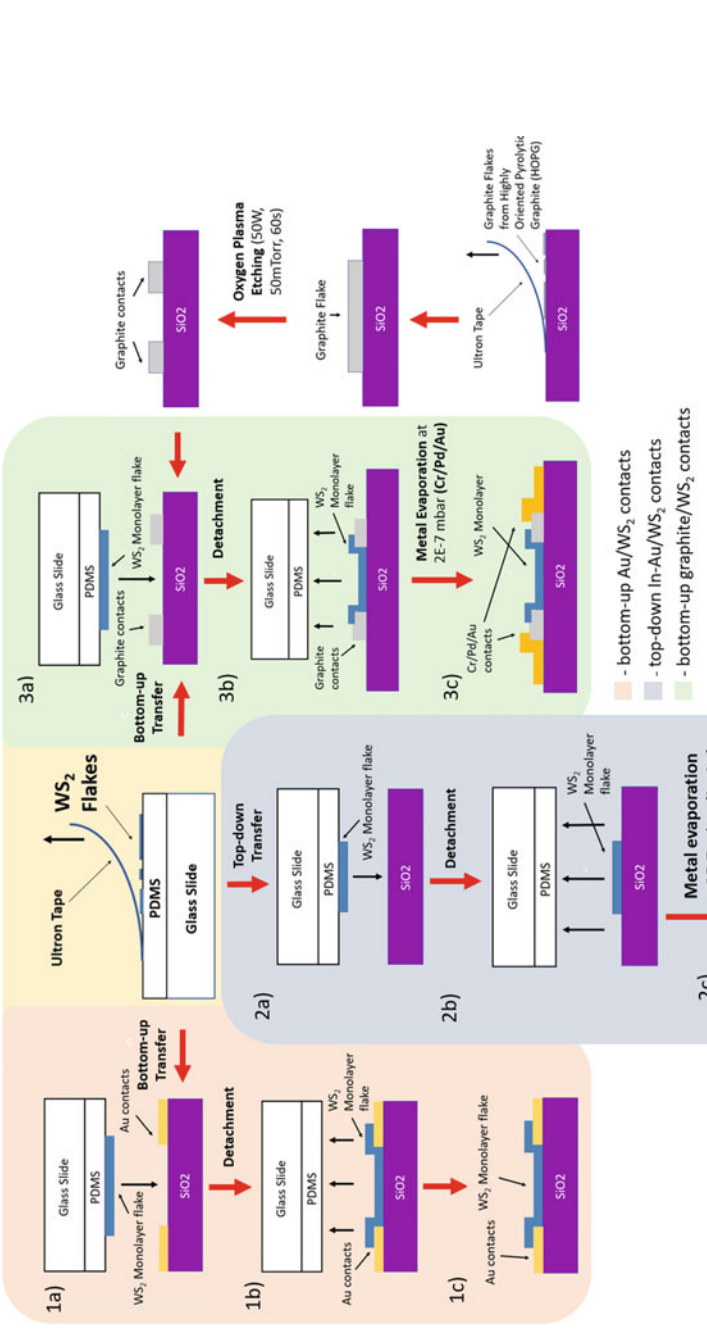

Fig. 1 A schematic diagram representation of the device fabrication process. Process 1, denoted by **a**, **b** and **c**, depicts the fabrication process of the bottom-up gold/WS_2 contacts. Process 2, denoted by **a**, **b** and **c**, depicts the fabrication process of the top-down gold-capped indium/WS_2 contacts. Process 3, denoted by **a**, **b** and **c**, depicts the fabrication process of the bottom-up graphite/WS_2 contacts

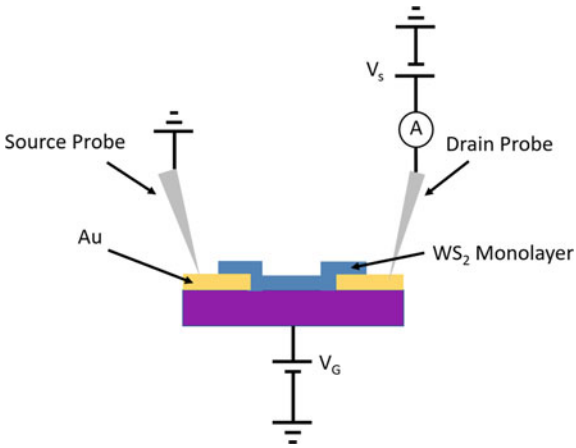

Fig. 2 A schematic diagram representation of the electrical measurement process. Conventional current flows from the source probe to the drain probe

4 Results and Discussion

4.1 Optical Images

Figure 3 shows the optical micrographs of the fabricated devices. For the bottom-up gold (Au) contacts (Fig. 3a), the few layer exfoliated WS_2 was placed onto the contacts across the 5 μm gap, achieving a 2-terminal contact. The thickest regions of the WS_2 were not contacted, so current is flowing through the few layer regions in the device in Fig. 3a. For the bottom-up graphite contacts (Fig. 3b), the exfoliated monolayer WS_2 was placed across the 5um gap between the 2 graphite contacts, similarly achieving a 2-terminal contact. The top-down gold-capped indium (In-Au) contacts (Fig. 3c) are placed across multiple contacts exfoliated WS_2 to obtain the results for the transfer line measurement analysis.

4.2 Carrier Mobilities

Figure 4 shows the transfer curves (I_s–V_g) of the fabricated devices, from which the field effect mobility is extracted from. The field effect mobility is extracted from (Eq. 1), where μ_{FE} refers to the field-effect carrier mobility, L_{CH} refers to the channel length, g_m refers to the intrinsic transconductance, W_{CH} refers to the channel width, C_G refers to the gate capacitance per unit area, and V_S refers to the source voltage. C_G can be further calculated from $C_G = \varepsilon_0 \varepsilon_r / d_{ox}$, where ε_0 is the permittivity of free space, ε_r represents the relative dielectric constant of 3.8 for SiO_2, and the thickness of the oxide layer, $d_{ox} = 285$ nm.

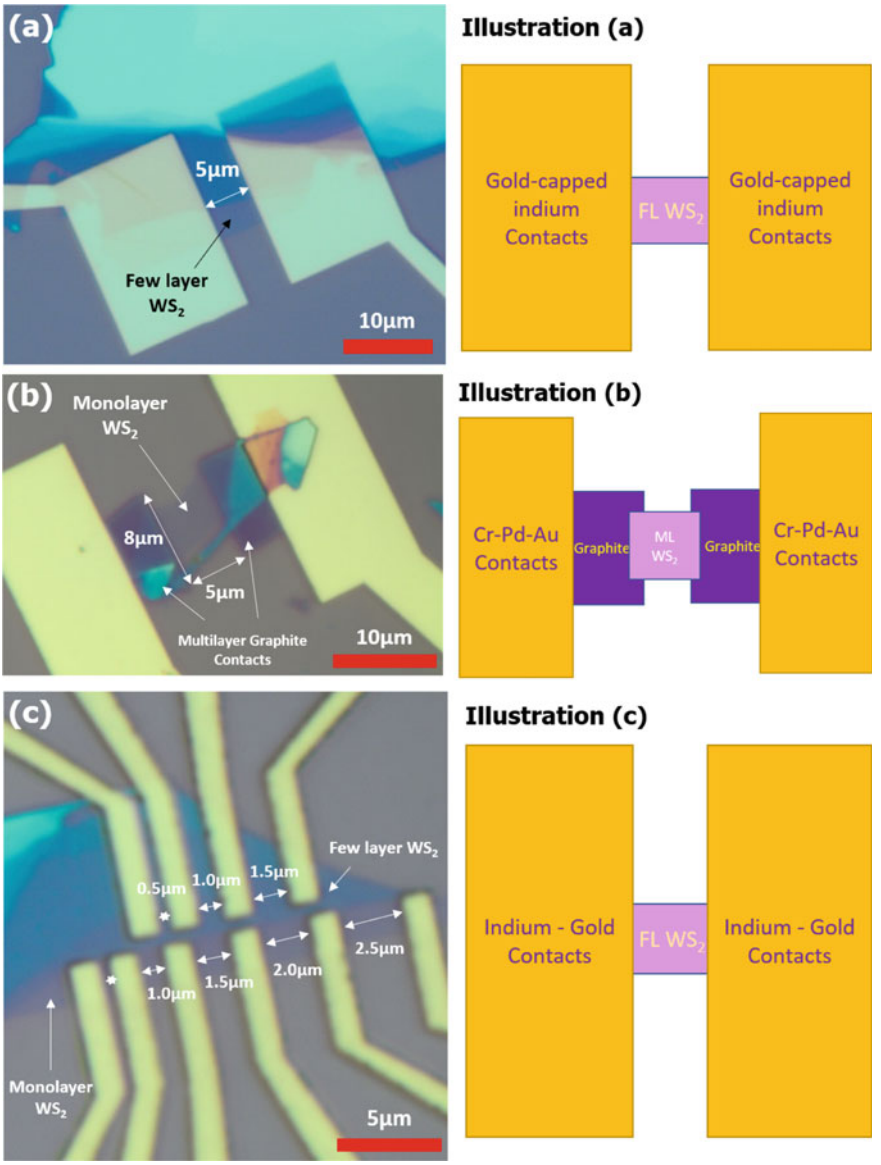

Fig. 3 Optical microscopy images of the devices. **a** Optical image of bottom-up gold contacts to WS_2 (gold/WS_2). The WS_2 monolayer was 6um by 12um. **b** Optical image of bottom-up chromium palladium gold (Cr–Pd–Au) contacts to WS_2 (graphite/WS_2). The WS_2 monolayer was 5 by 8 um. **c** Optical image of evaporated gold-capped indium contacts to few layer & monolayer WS_2 (gold-capped indium/few layer WS_2 and gold-capped indium/monolayer WS_2) for transfer line measurements. The lengths ranged from 0.5 to 2.5 um for the WS_2 monolayer; the lengths ranged from 0.5 to 1.5 um for the WS_2 few layer

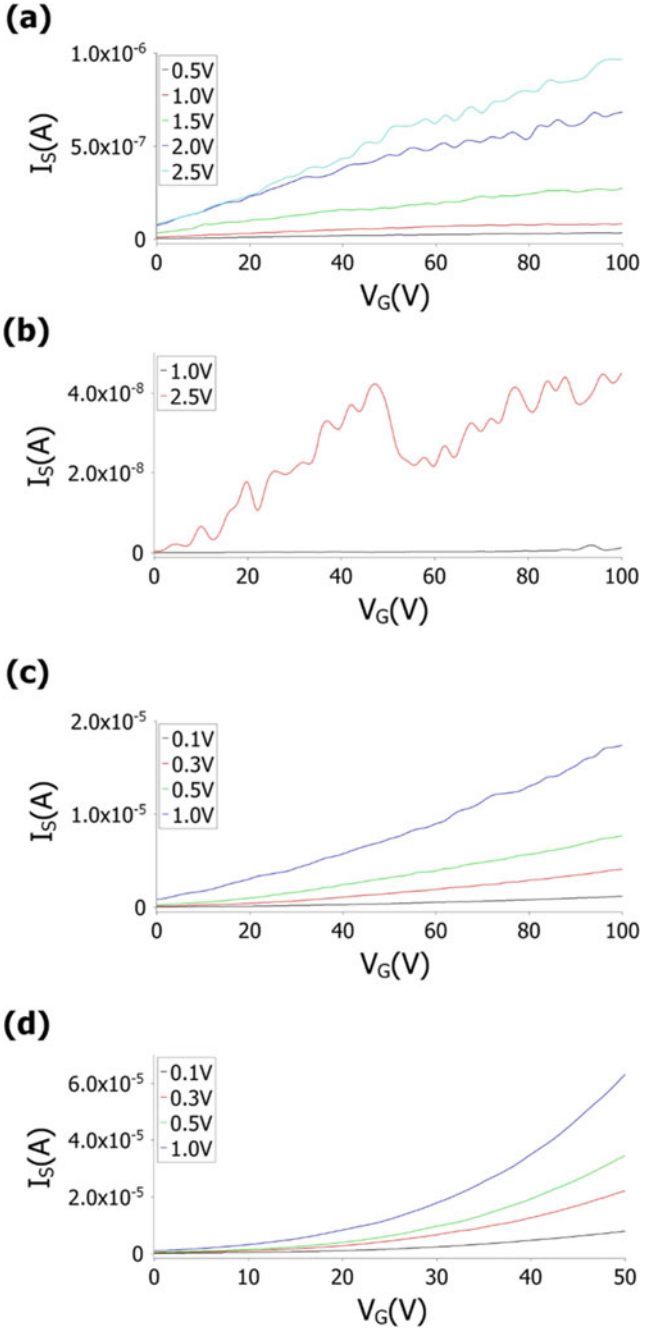

Fig. 4 Graphs of source current (I_S) against gate voltage (V_G) used to determine the field-effect mobilities for each of the devices. **a** Graph of I_S against V_G for gold/WS_2. The extracted electron mobility was 0.00542 cm^2V^{-1} s^{-1}. **b** Graph of I_S against V_G for graphite/WS_2. The extracted electron mobility was 0.0409 cm^2 V^{-1} s^{-1}. **c** Graph of I_S against V_G for gold-capped indium/monolayer WS_2. The extracted electron mobility was 5.45 cm^2 V^{-1} s^{-1}. **d** Graph of I_S against V_G for gold-capped indium/few layer WS_2. The extracted electron mobility was 114 cm^2 V^{-1} s^{-1}

$$\mu_{FE} = \frac{L_{CH} g_m}{W_{CH} C_G V_S}. \tag{1}$$

The gate voltage induced carrier density, n_{2D}, was extracted using the parallel-plate capacitor model from (Eq. 2), where C_G refers to the gate capacitance per unit area, V_G refers to the gate voltage, $V_{G,th}$ refers to the threshold voltage, and e refers to the unit charge (Fig. 4).

$$n_{2D} = \frac{C_G\left(V_G - V_{G,\text{th}}\right)}{e}. \tag{2}$$

The electron mobilities were computed and compared at carrier densities of approximately 2.2×10^{12} cm^{-2}. Thus, the derivative of the I_S against V_G curve (g_m) was taken at V_G values which corresponded to the carrier density of 2.2×10^{12} cm^{-2} for each of the devices. This is to conduct a valid comparison between the electron mobilities that were obtained for each of the devices.

The gold-capped indium (In–Au) contacts to few layer WS_2 yielded the highest electron mobility of 114 cm^2V^{-1} s^{-1}, 5 orders of magnitude larger than the electron mobility of the gold/WS_2 contacts. Other studies have also found that evaporated gold-capped indium (In-Au) contacts offer higher electron mobilities than pure gold (Au) or gold-capped titanium (Ti-Au) contacts for TMDCs [5]. However, the graphite contacts to WS_2 yielded lower than expected electron mobilities of 0.0409 cm^2V^{-1} s^{-1}, even though they were shown to form low resistance contacts to TMDCs [11]. Nonetheless, the electron mobility of WS_2 with the graphite contact was nearly 10 times that of bottom-up gold (Au) contact even though the graphite/WS_2 device is a monolayer device which has typically shown lower mobilities than the few layer WS_2 devices. Since only one graphite contact was functional, of the 11 graphite contacts produced, fabrication of more graphite contacts to WS_2 is required to confirm if graphite contacts indeed offer, on average, higher electron mobilities than gold (Au) contacts.

4.3 Contact Resistance Determination

Figure 5 shows the output curves (I_s–V_s) of the bottom-up gold/WS_2 contacts, gold-capped indium (In–Au) contacts to monolayer WS_2, and gold-capped indium (In–Au) contacts to few layer WS_2. The output curves of the gold/WS_2 contacts (Fig. 5a) are not linear, from which we can conclude that the contact is not ohmic, and a large Schottky barrier exists at the interface. The output curves of (Fig. 5b) is approximately linear, implying that a small Schottky barrier exists for the gold-capped indium/monolayer WS_2 contact. The linear output curves of gold-capped indium/few layer WS_2 (Fig. 5c) shows that the contact is ohmic.

Using the transfer line measurement readings, the contact resistance and sheet resistance for the gold-capped indium (In–Au) contacts to WS_2 were determined by

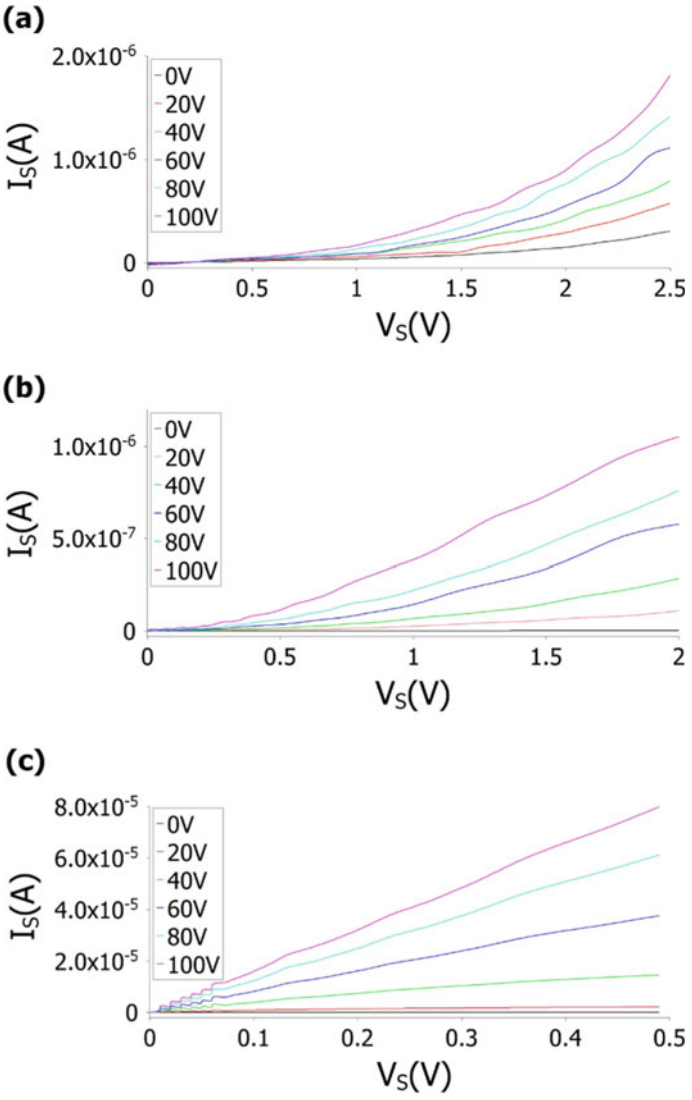

Fig. 5 Graphs of source current (I_S) against source voltage (V_S) for devices at constant gate voltage (V_G). **a** Graph of I_S against V_S for gold/WS_2. It is evident that the gold/WS_2 contact does not display ohmic behavior, and a large Schottky barrier exists at the interface. **b** Graph of I_S against V_S for gold-capped indium/monolayer WS_2. It is evident that the gold-capped indium/monolayer WS_2 contact displays slight Schottky behavior. **c** Graph of I_S against V_S for gold-capped indium/few layer WS_2. The linear behavior shows that the gold-capped indium/few layer WS_2 contact displays extensive ohmic behavior

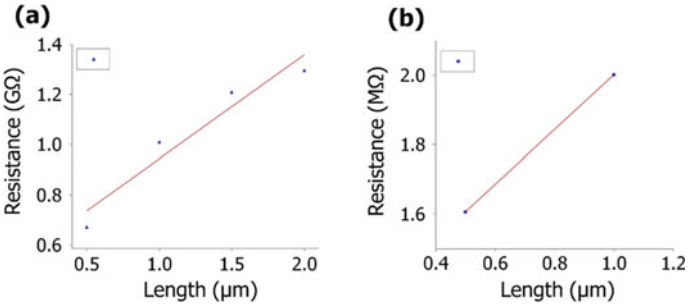

Fig. 6 Graphs of resistance against channel length (obtained from transfer line measurements). **a** Graph of resistance against channel length for gold-capped indium/monolayer WS_2. The extracted contact resistance was 169 M Ω μm. **b** Graph of resistance against length for gold-capped indium/few layer WS_2. The extracted contact resistance was 462 k Ω μm

taking the limit of the trend lines in the graphs of Fig. 6a and Fig. 6b to a zero-length resistor. We obtain the contact resistances for the gold-capped indium/monolayer WS_2 and the gold-capped indium/few layer WS_2 as 169 M Ω μm and 462 k Ω μm respectively.

The contact resistance of 462 k Ω μm for the gold-capped indium/few layer WS_2 is much higher than those obtained in the latest studies, where Yan Wang et al. reported low contact resistances of 2.4 k Ω μm [5]. They used Ar/H_2 gas annealing to reduce the Schottky barrier and interface contamination. We did not subject our samples to Ar/H2 annealing due to the lack of facilities. Hence the higher contact resistances could arise either from the current having to tunnel through a wider Schottky barrier or scattering by the contaminants.

Only 2 terminal measurements were taken for gold/WS_2 and graphite/WS_2 contacts as the WS_2 flakes obtained from exfoliation are typically very small, ranging from 10 to 20 μm in length. Since it is much more difficult to align flakes of such small structures under the microscope, this method was not attempted for gold/WS_2 and graphite/WS_2 contacts. Nonetheless, as we used WS_2 flakes that were exfoliated from the same bulk crystal, it can be inferred from the lower field-effect mobilities for gold/WS_2 and graphite/WS_2 contacts that gold/WS_2 and graphite/WS_2 have significantly higher contact resistances than gold-capped indium/WS_2. Our 2D transfer yield for the bottom up graphite and gold (Au) contacts was poor (only 1 out of 10 devices work), showing the difficulty of this fabrication method. Although an experienced and well-trained practitioner can have higher fabrication yield, this method is not suitable for scaling up and the top down (evaporation) method is preferred.

5 Summary of Values

See Table 1.

Table 1 Summary of values obtained for each device

Device	Electrical properties			
	Electron mobility (cm^2V^{-1} s^{-1})	Contact resistance (M Ω μm)	Sheet resistance (M Ω)	Contact resistivity (Ω cm^2)
Gold/WS_2	0.00542	–	–	–
Graphite/WS_2	0.0409	–	–	–
Gold-capped Indium/WS_2 monolayer (ML)	5.45	169	580	2.36
Gold-capped Indium/WS_2 few layer (FL)	114	0.462	1.11	0.00647

6 Future Work

To further improve the reliability of the results, the monolayer WS_2 and few layer WS_2 should be etched into rectangular strips, so that the widths and lengths are well defined. This would also enable the isolation of the monolayer regions from the few later WS_2 and ensure that current is passing through the monolayer WS_2 or few layer WS_2 only. Next, more data points should be collected for the transfer line measurements of gold-capped indium/few layer WS_2. In addition, temperature dependent measurements can be carried out to determine the Schottky barrier height, which would further validate our claim that In-Au contacts offer the lowest contact resistance and highest mobilities of the 3 methods proposed. Lastly, contact resistances and carrier mobilities may be improved by conducting a hydrogen annealing step together with h-BN capping [5, 12].

7 Conclusion and Applications

We have shown that low resistance ohmic van der Waals contacts for the TMDC WS_2 can be achieved using the direct metallization of gold-capped indium (In-Au) contacts onto WS_2. In contrast, the transfer of the few layer WS_2 on pure gold (Au) contacts or graphite contacts produced poorer contacts, which we attribute mainly to gold (Au) having a higher work function than Indium (In) by 1.38 eV, or by the presence of more contamination on the gold (Au) or graphite surface. Our findings are of current relevance and importance as electrical metal contacts formed are known to strongly affect device performance and the successful development of a low contact resistance van der Waals contact is imperative for the next-generation development of energy-efficient electronics and opto-electronics applications of WS_2.

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