Chapter 24
Practical Design Considerations of DC/DC Converter Used in MPPT for Solar PV Systems

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1 Introduction

The solar PV system not only consists of PV panels but also uses a power electronic converter for connecting its output to the grid or to the local load. The power electronics converters normally used are, the DC–DC converter and the DC–AC inverter for AC conversion. To extract the maximum power from the SPV module, the Maximum Power Point Tracking (MPPT) algorithm is incorporated with the DC–DC converter to step up/down the level of the solar PV array output voltage. The power semiconductor devices are used as switches where the internal resistance switch and internal resistance of practical inductors introduce new challenging problems like power loss, electromagnetic interference (EMI). Due to these problems, efficiency and power quality go down. To mitigate these issues, it is essential to create efficient DC–DC converter and effective algorithms for the MPPT.

The boost converter is used to uplift the level of DC voltage as per requirement. In literature, many authors have been worked out on simulation and hardware realization of the boost converter with and without solar photovoltaic application.

Kollimalla et al. [1] have presented the hardware prototype. They found the dynamic performance and stability of DC–DC boost converter using variable perturbation size adaptive P&O MPPT algorithm for rapid changes in solar insolation. In this algorithm, they used current perturbation, adaptive control and variable perturbation. The converter efficiency was not available in terms of numerical number but proposed in terms of dynamic performance of DC–DC boost converter with rapid

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changes in irradiation. Singh et al. [2] have been demonstrated the boost converter-based solar PV fed brushless DC motor driven the water pump. In this, they have used the DC–DC boost converter to achieve the MPPT of the PV array. The input PV parameters (Panel voltage and panel current) have sensed and fed to the INC MPPT algorithm to generate the desired PWM signal in MATLAB/Simulink. In this, the MATLAB-based simulation work has been carried out. They did not discuss the efficiency of the DC–DC boost converter.

To operate the AC appliances using Solar PV array, the voltage of DC link capacitor at the input side of the inverter should be greater than or equals to 2 $\sqrt{2}$ time of phase voltage, as determined by Popa et al. [3]. In this, they have investigated that DC–DC boost converter can be the best choice to reduce the number of SPV modules are being connected in series. Balamurugan et al. [4] have proposed the design of boost converter for PV application. In this, to track the MPP point of solar PV panel, the Perturb and Observe (P&O) method has been used. The ATmegha328 microcontroller has used to extract the maximum power from the solar PV panel.

Saxena et al. [5] have proposed an integration of solar photovoltaic with battery to single-phase grid in which the boost converter has used to step-up the DC voltage for the dc-link capacitor. Sathya et al. [6] have designed and implemented a 12 V/24 V boost converter for the solar-powered LED lighting system. The output voltage has controlled by the use of a closed-loop feedback system. In this, they have observed a 95% efficient boost converter in hardware realization.

Many authors have tried to address the DC–DC converters interfacing a load with either solar PV panel/module/array or rectified DC supply in order to extract the maximum power from the given source. But is found that no single literature is there to present the hardware realization of the proposed DC–DC boost converters. The objective of this paper is to propose step-by-step design method to develop the hardware prototype for the proposed DC–DC boost converter.

2 Basics of Boost Converter

As the name implies, a step-up (Boost) converter produces a higher average output voltage than the DC input voltage V_{PV}. Many times, this converter can be used to match the load impedance with impedance of solar photovoltaic panel ($R_{\text{opt}} = V_{mp}/I_{mp}$) to transfer the maximum power or to operate the SPV panel at MPP point. Figure 1 shows the SPV panel and this is interfaced to R_L load with the help of DC–DC boost converter. The boost converter consists of an inductor at input, semiconductor switch (it could be BJT, IGBT, and MOSFET), diode and a capacitor.

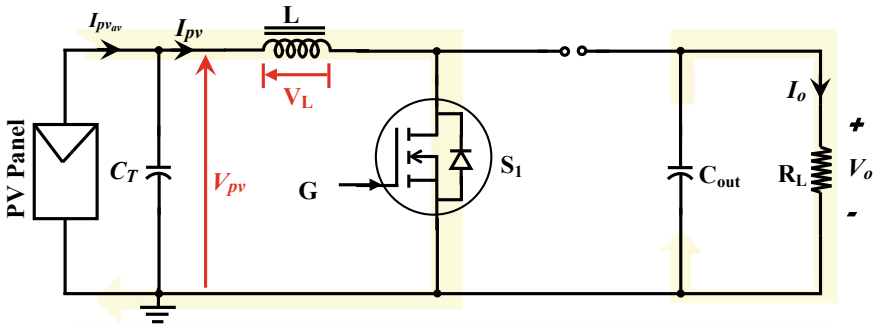


Fig. 1 Working of boost converter during DT_s time

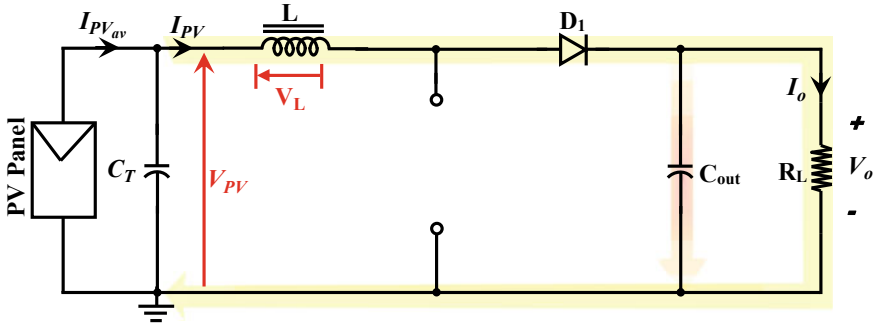


Fig. 2 Current paths during $(1 - D)T_s$ time in boost converter

2.1 Working of Boost Converter

During ON-Time

- During ON-time, the terminal current $\boldsymbol{I_{PV}}$ flows from PV module to an inductor and through the switch-Q as depicted in Fig. 1.

  The capacitor C_{out} continues to discharge through the load while the inductor L charges by extracting the energy from the SPV module.
  During ON-time, the voltage across the inductor is V_{PV} and current through it, rises linearly from a non-zero value to a peak value.

During OFF-Time

- During off-time, the inductor current flows continue and therefore the polarity of inductor voltage reverses and diode *D* conducts. And this current will charge the capacitor C_{out} and supply the load current I_o.

- The voltage across the inductor is $V_{PV} - V_o$. As $V_o > V_{PV}$, the voltage across the inductor is negative and this is expected because we need the positive portion to balanced out by negative portion.
- The current through inductor will decay because this is discharging now into the capacitor and discharging into the load. The capacitor is charging up.
- The average inductor current is the terminal current $\boldsymbol{I_{PV}}$ (Fig. 2).

Input–Output Voltage Relationship:

$$V_{pv} \times DT_s + \left(V_{pv} - V_o\right) \times (1 - D)T_s = 0$$

$$\boldsymbol{V_o = V_{PV}\left(\frac{1}{1 - D}\right)}$$

Input–Output Current Relationship:

The average current through the capacitor should have to be zero. Meaning that there is no charge building up in capacitor or capacitor is in steady state. Discharging capacitor current is taken as negative value.

$$(-I_o)DT_s + (I_{PV} - I_o) \times (1 - D)T_s$$

$$\mathbf{I_o = I_{PV}(1 - D)}$$

On dividing the equations,

$$R_L = \frac{V_o}{I_o} = \frac{V_{PV}\left(\frac{1}{1-D}\right)}{I_{PV}(1 - D)} = \frac{V_{PV}}{I_{PV}}\left(\frac{1}{(1 - D)^2}\right) = \frac{R_T}{(1 - D)^2}$$

$$\boldsymbol{R_L = \frac{R_T}{(1 - D)^2}}$$

2.2 Effect of Boost Converter on MPPT

The terminal resistance

$$\boldsymbol{R_T = R_L(1 - D)^2}$$

The terminal resistance or input resistance to the boost converter can be changed by varying the duty ratio. Let us draw the *I–V* characteristic and power curve of PV module as depicted in Fig. 3.

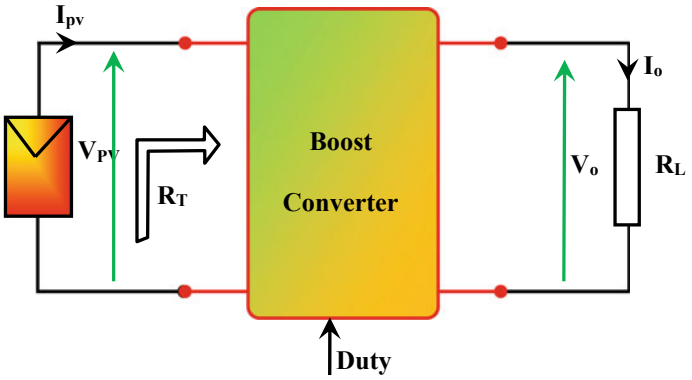
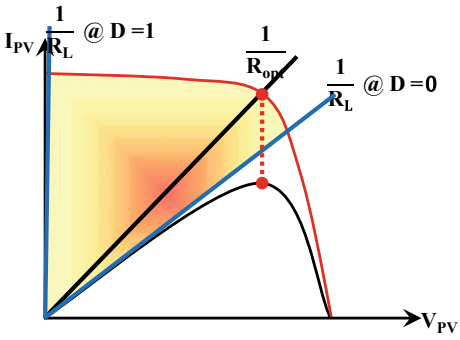


Fig. 3 PV module with MPP block for boost converter

Fig. 4 PV module I–V characteristics for boost converter



If duty $D = 1$, then.
$R_T = 0$, i.e., vertically short circuited and the load line is along with y axis.
If duty D = 0, then.
$R_T = R_L$.

With Boost converter the following point on PV curve can be traced. There is limitation with load line; consequently, there is limited load line (Fig. 4).

Hence, in boost converter the reachable points are lying between the load line corresponding to $D = 0$ and corresponding to $D = 1$ as shown in Fig. 5. From the above, it can be concluded that the maximum power point is not traced with Boost converter.

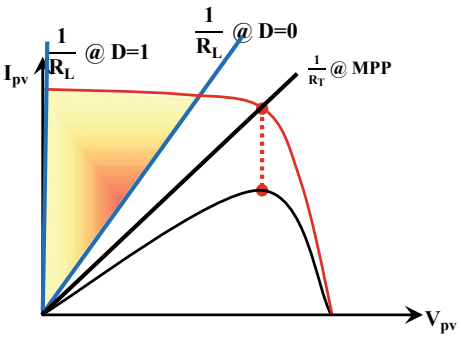


Fig. 5 PV module I–V characteristics with limited load line for boost converter

3 Design of Boost DC–DC Converter

The estimation of inductor L and capacitor C, where f_s is the switching frequency of boost converter; I_L is the average inductor current; ΔI_L is ripple content in the inductor current; $I_{L\,\mathrm{Max}}$ is a maximum value of inductor current; $I_{L\,\mathrm{Min}}$ is a minimum value of inductor current; ΔV_o is ripple content in the capacitor voltage.

Step 1: Consider the values of P_{mpp}, V_{mpp}, I_{mpp}, I_{sc}.

Step 2: If converter has zero internal losses then output voltage will be

$$V_{\mathrm{in}} I_{\mathrm{in}} = V_o I_o = \frac{V_o^2}{R_L} = P_{mpp}$$

$$\frac{V_o^2}{R_L} = P_{mpp} \;\Rightarrow V_o = \sqrt{P_{mpp} * R_L}$$

Step 3: For given output voltage, the duty of converter will be

$$V_o = \frac{V_{\mathrm{in}}}{1-D} \quad \Rightarrow D = 1 - \frac{V_{\mathrm{in}}}{V_o}$$

Step 4: The inductor current is given by

$$I_L = \frac{V_{\mathrm{in}}}{(1-D)^2 R_L}$$

If the change in inductor current $\Delta \mathrm{I_L}$ is 5% then

$$\Delta I_L = 0.05^* I_L$$

Since,

$$\Delta I_L = \frac{V_{\text{in}} D}{L\, f_s}$$

Determine L from the above expression.

Step 5: Maximum and Minimum Inductor Currents.

The maximum current through the inductor in Boost DC–DC converter is given by

$$I_{L\ \max} = I_L + \frac{\Delta I_L}{2}$$

The minimum current through the inductor in Boost DC–DC converter is given by

$$I_{L\ \min} = I_L - \frac{\Delta I_L}{2}$$

Step 6: Value of Output capacitance, if the ripple is not more than 1% then

$$C = \frac{D}{R_L f_s \frac{\Delta V_o}{V_o}}$$

3.1 Designing of Practical Inductors (L) and Selection of Capacitors (C) for Proposed Converter Topologies

The practical inductor consists of a wound conductor coil on a ferromagnetic material. This combination yields an inductance (L) that offers reluctance to a change in current, and therefore the current through an inductor cannot change instantaneously. The rate of change of current through an inductor ($\mathrm{d}i_L/\mathrm{d}t$) is determined by the inductance and the voltage dropped across the inductor, given by the expression: $V = L * \mathrm{d}i_L/\mathrm{d}t$. Furthermore, the use of ferromagnetic material as the inductor core allows energy to be stored in the inductor. When a positive voltage has appeared across the inductor, the current increases and meanwhile energy is dumping into the inductor. It is an essential characteristic that makes the inductor useful in the DC–DC converter since it acts as both a current-ripple filter and an energy-storage element.

When the switch is closed, the current flowing to the load increases and energy is also stored in the inductor. When the switch is opened and the output is disconnected from the input, the stable output current is maintained by drawing energy from the inductor. Since inductance determines the $\mathrm{d}i_L/\mathrm{d}t$, its value is selected to achieve desired limits to the ripple current (I_{ripple}), providing a steady output current. The inductor can only hold a finite amount of energy before the ferromagnetic material

will saturate, the inductance decreases, and ripple current increases. When making an inductor selection, it is important to check that the current at which the core saturates (I_{sat}) is greater than the application's peak inductor current, ($I_{pk} = I_{\text{out}} + I_{\text{ripple}}/2$). In this thesis, all topologies work in continuous conduction mode (CCM). For CCM, the practical value of inductor should be greater than the minimum value of required inductor values.

3.1.1 Design of Inductors

The inductor is the energy storing element and practical inductor has some value of its wire resistance. The wire resistance should be very small as possible therefore; the proper design of practical inductor plays an important role in MPP of SPV panels or modules. The following steps are used to design the inductors used in DC–DC converter.

Step 1 (Inductor Value): the value of the inductor has to be calculated. The calculation of inductors is done for DC–DC converter topologies.

Step 2 (Area Product): From the current waveform through the inductor, the energy-storage requirement for the inductor is estimated. The energy that needs to be stored in the inductor is given as

$$E_L = \frac{1}{2} L I_m^2$$

where E_L is the maximum energy in joules that needs to be stored in the inductor and I_m is the peak inductor current in amperes. Based on the energy to be handled by the inductor core, the area product is given as

$$A_p = A_c A_w = \frac{2E_L}{K_w K_c J B_m}$$

where:

$K_w = 0.6$ for single-winding inductor and $0.3-0.4$ for multiple-winding inductors

$$K_c = 1$$

J = Current density for copper $= 3 \times 10^6 \text{A/m}^2$

B_m = Flux density in Tesla = 0.25 T for ferrites, 1 T for CRNGO and 1.2 T for CRGO.

The selected core should have an area product greater than that calculated by the above equation.

Step 3 (Permeance): The permeance of a core with air gap l_g is given by

$$\wedge = \frac{\mu_o \mu_r A_c}{l_m + \mu_r l_g}$$

where:

$$A_c = \text{core cross-sectional area of the selected core (in m}^2\text{)}$$

$$\mu_r = \text{relative permeability of the selected core material, for ferrite core it is generally 2000}$$

$$l_g = \text{introduced air gap length (in meter)}$$

$$l_m = \text{magnetic path length of the selected core (in meter)}$$

Step 4 (Number of turns): The number of turns required for desired value of inductance is given by

$$N = \sqrt{\frac{L}{\wedge}}$$

Step 5 (Gauge of Wire): the cross-section area of the wire can be calculated as

$$\mathrm{a} = \frac{\mathrm{I_{rms}}}{\mathrm{J}}$$

where, I_{rms} is the RMS value of the current flowing through the inductor which is equal to I_m/K_c and $K_c = I_m/I_o$. The gauge of wire (SWG) selected should have a cross-section area that is greater than that calculated by the above expression.

Step 6 (Available Window Area check): The inequality $A_W K_W > aN$ should be satisfied or else repeat the calculation for the number of turn and gauge of wire after choosing the next bigger core. Note that the value 'a' used for checking the above inequality should be the actual cross-section area of the wire and not the calculated value in step-5.

3.2 Selection of MOSFET Switch and Driver Circuits

Most DC–DC converters are designed for continuous current operation. Note that as the switching frequency increases, the minimum size of the inductor to produce continuous current and the minimum size of the capacitor to limit output ripple both

decrease. Therefore, high switching frequencies are desirable to reduce the size of both the inductor and the capacitor. The tradeoff for high switching frequencies is increased power loss in the switches. Increased power loss in the switches means that heat is produced. This decreases the converter's efficiency and may require a large heat sink, offsetting the reduction in the size of the inductor and capacitor. The selection of power MOSFET based on that the r_{dON} should be very low and voltage, current ratings of MOSFET.

Electrical isolation is provided with the use of integrated circuit (IC) package TLP250, TLP350 manufactured by TOSHIBA. This IC consists of a GaAlAs light emitting diode and an integrated photo detector. The schematic and pin configuration diagrams of TLP250 are depicted in Fig. 6.

Figure 6a clearly shows the input LED side and the receiving photodetector as well as the totem-pole driver stage. Pins 1 and 4 are not internally connected to anything and hence are labeled NC meaning no connection. Pin 8 is V_{CC}—the positive supply. Pin 5 is GND—the ground supply or the return path for the driving power supply. The supply voltage must be at least 10 V. The maximum voltage is dependent on the operating temperature. If the temperature is lower than 70 °C, up to 30 V can be used. For temperatures between 70 and 85 °C, up to 20 V can be used. However, there should not be a need to use higher than 20 V anyways (Fig. 7).

The Pins 2 and 3 are the inputs to the LED, anode and cathode, respectively. Like regular LEDs, it has an input forward voltage and a peak forward current. The

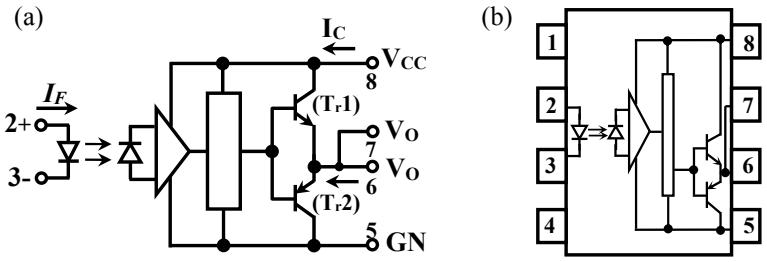


Fig. 6 **a** Schematic diagram and **b** pin configuration of TLP250

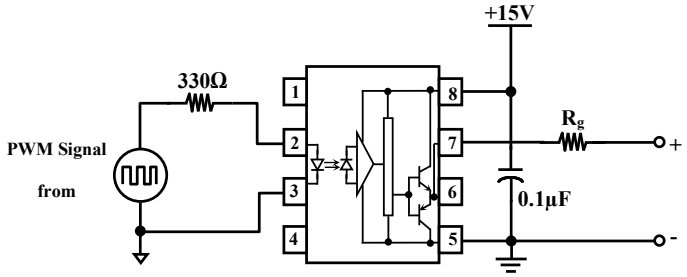


Fig. 7 Gate driver circuit using TLP-250

forward voltage will typically be between 1.6 and 1.8 V. The forward current should be less than 20 mA. The threshold input current for output transition from low to high is typically 1.2 mA but may be as high as 5 mA. Thus, 10 mA current should be good. Even though pins 6 and 7 are shown to be internally connected, the output should be taken from pin 6 as the image—datasheet—shows pin 6 labeled as V_o (Output). The output voltage will tend to rise to supply voltage when high (it will actually be slightly lower) and fall to ground level when low.

3.3 Design of Snubber Circuit for MOSFET

There is a danger of exceeding the voltage and the current rating of the MOSFET switch during turn-OFF and turn-ON instants, respectively. If there is an inductive load in the source side or if there is a significant amount of lead inductance associated with the source or drain terminal, then when MOSFET is being turned OFF, the current through the device could decrease rapidly to zero within the fall time of the device. As a consequence, a large voltage spike due to $L\mathrm{d}i/\mathrm{d}t$ will occur across the device and cause V_{DS} of the MOSFET to have a large spike during the fall time. This may damage the device. Therefore, it becomes necessary to limit the voltage spike during fall time.

On the other hand, during turn-ON of the device, due to the presence of any capacitive load or parasitic capacitance across the switch, there will be a huge surge current through the device which could damage the device. Therefore, it becomes mandatory to limit the current spike through the device during turn-ON.

The Snubber circuits modify the device switching characteristics and in doing so, reduce the device transients. The main task of the Snubber circuit is to absorb energy from the reactive elements. The parasitic capacitance and inductance cause large turn-on/off oscillation in the PWM input signal. The Snubber circuit improves the input signal shape.

In the MPPT operated DC–DC converter, the input current is fairly constant and it can be seen that the switch (MOSFET) is connected in the line or between the line and ground terminal. When the MOSFET is turned OFF, the input current or switch current i_T will fall to zero in a period of time corresponding to the fall time t_f mentioned in datasheet of MOSFET. Due to this, the voltage across MOSFET V_{ds} will shoot up to a large value because of the $L\mathrm{d}i/\mathrm{d}t$ phenomenon where L could be the lead inductances associated with the drain and source leads. Therefore, it is required to limit the voltage across the drain-source of the MOSFET and it should be made to rise gradually during the fall time t_f as depicted in Fig. 8b. To decrease the rate of rise of voltage V_{ds}, one can connect a capacitor C_s across MOSFET as indicated in Fig. 8a. Sometimes this Snubber circuit is also called as shunt Snubber because the capacitor C_s is connected in shunt with the device or MOSFET. Without loss of generality, one can assume that the switch current is falling linearly as shown in Fig. 8c during the t_f time and the drain-source voltage across the device is rising linearly as depicted in Fig. 8c during the fall time when the shunt Snubber is connected. From Fig. 8a,

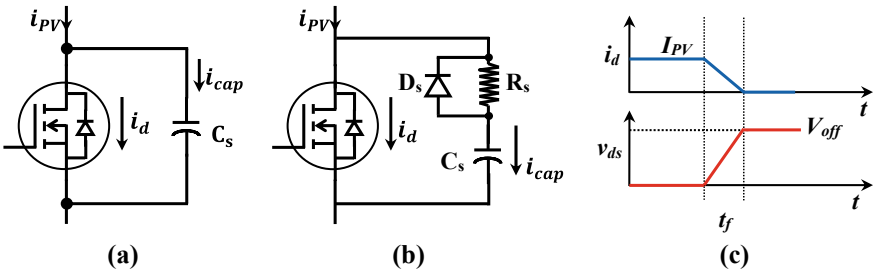


Fig. 8 Turn-off or shunt Snubber circuit for power MOSFET

$$i_{PV} = i_d + i_{\text{cap}}$$

where i_d is the current through the MOSFET and i_{cap} is the current through the shunt capacitor. During the fall time period of t_f, the current i_d through MOSFET is given by

$$i_d = i_{PV} - i_{PV}\frac{t}{t_f}$$

$$i_d = i_{PV}\left(1 - \frac{t}{t_f}\right)$$

The current through the capacitor is given by

$$i_{\text{cap}} = i_{PV} - i_{PV}\left[1 - \frac{t}{t_f}\right] = i_T \times \frac{t}{t_f}$$

The voltage V_{ds} across the device is the same as the voltage across the capacitor C_s. therefore

$$v_{\text{ds}} = \frac{1}{C_s} i_{\text{cap}} \cdot dt$$

$$v_{\text{ds}} = \frac{1}{C_s} i_{PV} \times \frac{t}{t_f} \cdot dt$$

The voltage across MOSFET or capacitor can be obtained during fall time by integrating the above equation within the fall time and then applying the boundary condition. At the end of fall time, the voltage across the MOSFET should be V_{PV} or V_{in} then the value of capacitor will be

$$C_s = \frac{i_{PV} t_f}{2V_{\text{in}}}$$

The problem of voltage spike during turn-off process of the MOSFET is resolved by the circuit of Fig. 8a but it will create a serious problem during the turn-ON of the MOSFET. When the MOSFET is turned ON again, the capacitor C_s will discharge through MOSFET and will result in a large current spike through the MOSFET which can damage the power MOSFET. Therefore, to control the current through MOSFET, a resistor R_s is introduced in series with capacitor C_s.

The resistor R_s should provide the function of current limiting only during turn-ON of the MOSFET. However, during turn-OFF of MOSFET, R_s is not needed. Therefore, to deduce the dissipation in R_s during turn-OFF, a diode is placed across R_s as shown in Fig. 8b so that R_s comes into effect only during turn-ON when C_s discharges through R_s and MOSFET.

3.4 *Choose a Snubber Capacitance Value Which Meets Two Requirements*

(1) It can provide a final energy storage greater than the energy in the circuit inductance
$\frac{1}{2}C_s V_{\text{off}}^2 > \frac{1}{2}L_i i_{PV}^2$, and therefore $C_s > \frac{L_i\, i_{PV}^2}{V_{\text{off}}^2}$.
Where, L_i is circuit inductance and V_{off} is the voltage across the device when it is turn-OFF.

(2) It produces a time constant with the Snubber resistor that is small compared with the shortest expected on-time for the MOSFET switch.

$$R_s\, C_s < \frac{t_{\text{ON}}}{5}$$

4 Selection of Snubber Resistor R_s

When the MOSFET is turned on, it should carry the load current plus the capacitive current discharge from C_s which is equal to V_{off}/R. therefore,

$$\frac{V_{\text{off}}}{R_s} + i_{PV} < I_{dm}$$

where, I_{dm} is the maximum drain-current rating of the MOSFET.

Rearranging the above inequality, the following inequality is obtained

$$R_s > \frac{V_{\text{off}}}{I_{dm} - i_{PV}}$$

It is also important to ensure that the capacitor discharges fully before the next charging when the MOSFET turn-OFF. Therefore, there is a minimum duration of time during which time the MOSFET should remain ON so that the capacitor can fully discharge. Therefore

$$t_{\text{ON}} > 5R_sC_s$$

where, t_{ON} is the minimum time for which MOSFET should remain in the ON-state.

Rearranging the above inequality, the following inequality is obtained:

$$R_s < \frac{t_{\text{ON}}}{5C_s}$$

From the above two inequalities, the range of choice of R_s is given by

$$\frac{V_{\text{off}}}{I_{dm} - i_L} < R_s < \frac{t_{ON}}{5C_s}$$

The power rating of Snubber resistor is given by

$$P_{R_s} = \frac{1}{2}C_s V_{\text{off}}^2 f_{sw}$$

where, f_{sw} is the switching frequency of the MOSFET.

5 Conclusions

The significant contributions of the presented paper are as follows:

1. The need of DC–DC converter in between solar PV module and resistive load has been investigated through mathematical calculation.
2. The investigation on need of DC–DC converter revealed that DC–DC converter with MPPT technique modifies the effective resistance being faced by Solar PV module.
3. The parameters (Value of L, C and Duty) of the proposed DC–DC converters have been determined keeping in mind that these converters must work in linear region and in continuous conduction mode (CCM).
4. The most important parameter of DC–DC converter interfacing SPV module with load is the internal resistance of inductor. The internal resistance of inductor may

restrict the maximum power transfer. Hence, the internal resistance of inductor can be lowered by using Litz wire or large cross-sectional copper wire.
5. The internal resistance of high speed switch (MOSFET/IGBT) must be low. The careful selection of power MOSFET plays a major role in energy extraction from SPV module.
6. To drive the Power MOSFET, a robust optocoupler (TLP-250) based driver circuit has been developed in the laboratory. The ringing effect has been minimized by connecting a snubber circuit across the power MOSFET.

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