UPFC Modelling for Augmentation of Voltage Stability and Reduction of Active Power Losses

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1 Introduction

Transmission systems of present power network are reliably crashed into increasingly focused on level because of the ascent in load requests and limitations of developing new lines. The result of such an accentuated framework would be gaining instability trailed by interference because of a fault. Use of FACTS devices has ended up being an exceptionally viable strategy to cut down the pressure of the power system grid and consequently issues in better usage of concerned accessories in power framework without bargaining the appropriate margin of stability [1]. Position of FACTS controllers play a crucial role in congestion management, and FACTS controllers used for the problem of reactive power compensation can be solved. Flexible AC transmission system (FACTS) was first brought into light by Hingorani [2] in 1988. Power flow control method has been presented by Gothana and Heydt [3]. A brief search for the optimal position of FACTS controllers is discussed by Lie and Dang [4]. This paper deals with improvement in operational performance of power system using UPFC FACTS devices. The simulation is executed using PSAT in the MATLAB. The area for the situation of UPFC is purposefully utilising an index termed as network branch index (NBI) [5]. Voltage stability improvement is assessed by extension power flow method present in [6]. UPFC is used with the optimal variables which are reducing

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J. Kumar and P. Jena (eds.), *Recent Advances in Power Electronics and Drives*, Lecture Notes in Electrical Engineering 707,
https://doi.org/10.1007/978-981-15-8586-9_38

the real power loss and the system running cost [7]. Various optimization methods are explained in [8]. Increase in the loadability with FACTS devices is described in [9]. In [10], author describes the reactive power compensation. In this paper, voltage crash point using the load flow jacobian matrix is presented [11]. The authors in [12] presents gravitational search algorithm (GSA)-based enhancement strategy for the ideal coordination of FACTS controller with the current imaginary power sources present in an associated power grid. Basic principle of the UPFC is described in [13]. Power system analysis toolbox (PSAT) gives graphical consolidate of power flow analysis, and PSAT toolbox detects the most precise node [14]. In this paper, [15] shows how to the improve voltage stability using shunt devices. All the parameters are concluded for voltage collapse using the PSAT MATLAB and description of weak node with the help of voltage stability index [16].

2 Problem Formulation

2.1 Improvement of Bus Voltage

It is very essential to manage normal voltage profile constantly. The first objective is the minimization of the voltage deviation expressed as follows:

$$M_{2=\sum_{i=1}^{n1}\left[U_a - U_{\text{specified}}\right]} \tag{1}$$

where $U_{\text{specified}}$ is the magnitude of bus voltage and nl is the total bus no. U_a is the voltage magnitude at a_{th} bus.

2.2 Reduction of Real Power Loss

Because of transmission loss, redistribution of reactive power in transmission network occurs firstly. So real power loss reduction changes the active power generated by slack bus.

Real power loss minimization is mathematically expressed as follows:

$$M_L = P_L \sum_{j=1}^{nl} G_{ij}\left[U_i^2 + U_j^2 - 2U_i U_j \cos(\beta_{ij})\right] \tag{2}$$

where

nl no. of transmission lines
G_{ij} Conductance of ith and jth bus in transmission line

U_i bus ith voltage
U_j bus jth voltage
B_{ij} Power angle at bus ith and jth
P_L Real power loss.

Equality limits: Imaginary and real power equation for nl bus system.

$$Q_{gi}^{''} - Q_{di}^{''} - U_i^{'} \sum_{j=1}^{nl} U_j^{'}[G_{ij}^{'} \sin\varphi + B_{ij}^{'} \cos\varphi] = 0 \tag{3}$$

where $i = 1, 2, 3 \ldots nl$

$$P_{gi}^{''} - P_{di}^{''} - U_i^{'} \sum_{i=1}^{nl} U_j^{'}[G_{ij}^{'} \cos\varphi + B_{ij}^{'} \sin\varphi] = 0 \tag{4}$$

where $j = 1, 2, 3 \ldots nl$

where $\varphi = \beta_i - \beta_j$

nl Total bus number.
$P_{gi}^{'}$ **a**nd $P_{di}^{'}$ is real power generation and ith bus demand, respectively
$Q_{di}^{'}$ and $Q_{gi}^{'}$ is and VAR demand and VAR Generation of the ith bus
$G_{ij}^{'}$ represents transfer conductance of ith and jth bus
$B_{ij}^{'}$ represents the transfer susceptance of ith and jth bus

Inequality limits: Maximum and minimum limit must be defined for the generator voltage magnitude and reactive power

$$P_{gx,\min} \le P_{gx} \le P_{gx,\max},\ x = 1, 2, \ldots M_{PV} \tag{5}$$

Generator bus voltage and reactive power restraints are express as

$$Q_{gx,\min} \le Q_{gx} \le Q_{gx,\max},\ x = 1, 2, 3, \ldots M_{PV} \tag{6}$$

$$U_{gx,\min} \le U_{gx} \le U_{gx,\max}, x = 1, 2, 3 \ldots M \tag{7}$$

Taps limits of Transformer: maximum and minimum limit

$$t_{x,\min} \le t_x \le t_{x,\max}, x = 1, 2, 3 \ldots \tag{8}$$

M_{PV} PV buses locations M buses locations

3 UPFC Circuit Modelling

The regular UPFC arrangement is as appeared in Fig. 1. The circuital model of the UPFC is acquired from the STATCOM and SSSC. The model representation fundamentally comprises shunt and series converters. A voltage source converter is existing in branch of series type whose principle work is to infuse a voltage, with variable extent and edge, in arrangement by means of a transformer. Thus, it has a capacity to trade real power with the lines of transmission network. Be that as it may, the shunt part of the converter is answerable for the compensation of any active power provided furthermore, drawn by the series type branch just as the losses. The shunt type converter arrangement has a solid capacity to freely trade a imaginary power with the framework by means of the transformer through which it is associated with the network.

From Fig. 1. The source voltage can be represented as

$$E_{sh} = V_{sh}(\cos\delta_{sh} + j\sin\delta_{sh}) \tag{9}$$

$$E_{se} = V_{se}(\cos\delta_{se} + j\sin\delta_{se}) \tag{10}$$

where δ_{sh} presents the voltage source of controllable phase angle and V_{sh} presents the magnitude at the shunt type of converter area.

The viability of this methodology is exhibited in the area that is subsequent to utilising an example of 6 bus and 14 bus system as a case study.

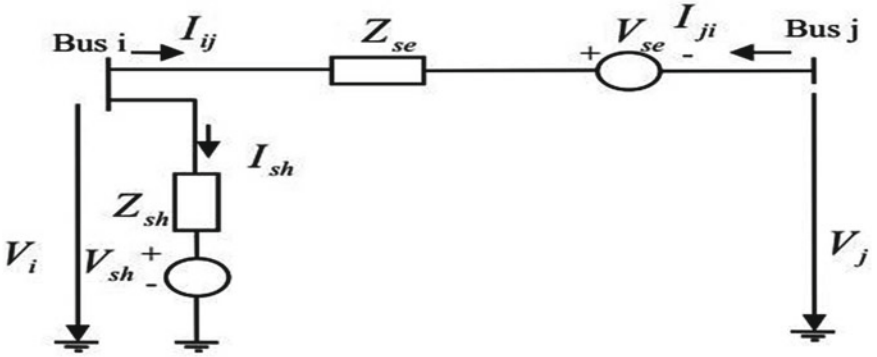

Fig. 1 UPFC configuration model

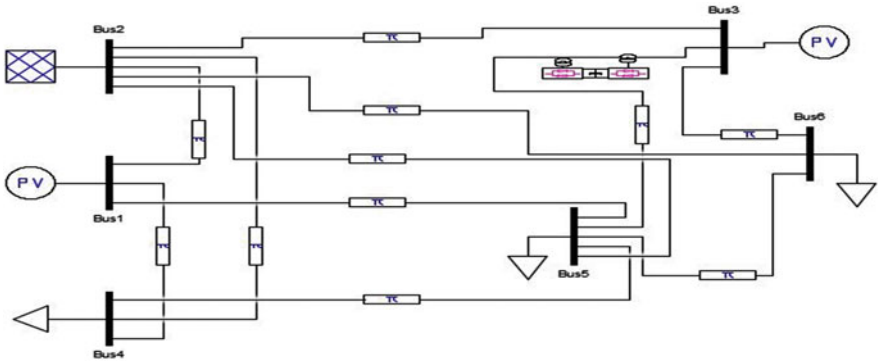

Fig. 2 A 6 bus modified system recreated in PSAT after the establishment of UPFC

4 Methodology

4.1 Psat

As the name suggests, PSAT effectively analyses the power system with the advantages of toolbox which is anything but difficult to get to. PSAT additionally empowers the capacities identified with various power flows locked in. When contrasted to other MATLAB toolboxes, PSAT gives wide scope of highlights that puts forth power system investigation accomplished with not so much attempt but rather more precise. The use of PSAT for the displaying of the test bus framework and its examination appeared as designing of test bus system.

4.2 IEEE 6 and 14 Test Bus System

The test system being analysed is 6 Bus Test System which involves of one slack bus, 2 generators at 2, 3 and remaining nodes are supposed to be load buses at 4, 5 and 6. It has 9 lines. IEEE-14 bus comprises one slack bus, 4 generators and 9 load buses. Utilising PSAT the model of IEEE 6 and 14 test bus system which was made is shown in Figs. 2 and 3.

5 Results and Discussion

The authors presented the bus voltage profile and real power loss before and after establishment of UPFC. The simulations are executed using PSAT in the MATLAB environment. Figures 2 and 3 show the single line diagram, and Figs. 4 and 5 shows

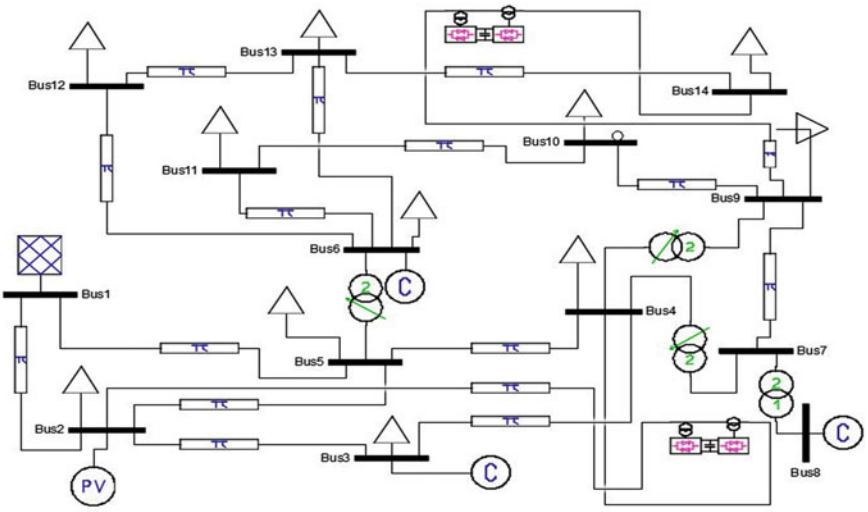

Fig. 3 A modified 14 bus system recreated in PSAT after the incorporating of UPFC

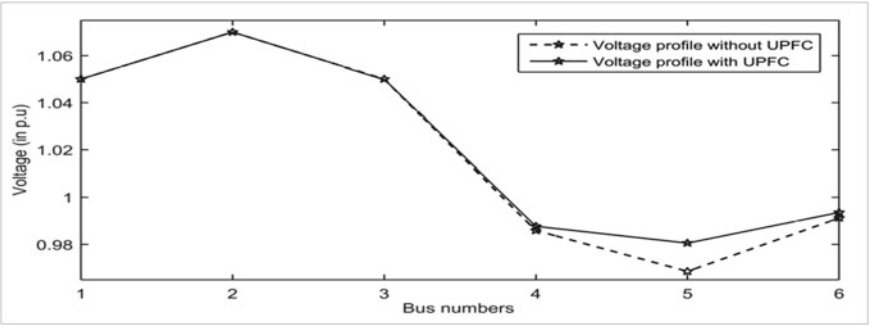

Fig. 4 Bus voltage due to absence and presence of UPFC for IEEE 6 bus system

the bus voltage due to absence and presence of UPFC for IEEE 6 and 14 bus network, respectively. It is detected that the bus voltage is low at node 6, 4 and 5 for 6 bus network and node 9, 10, 14 for 14 bus networks. Table 1 presents Bus voltage magnitude, and Table 2 presents active power losses due to absence and presence of UPFC for IEEE 6 bus system. Table 3 presents Bus voltage magnitude, and Table 4 presents real power losses due to absence and presence of UPFC for 14 bus system, respectively. It is clear that after using UPFC voltage magnitude increases and real power losses reduces. And in Table 5, the authors present the comparative analysis of total active power loss with and without using UPFC in both test bus system and also show the reduction of real power loss.

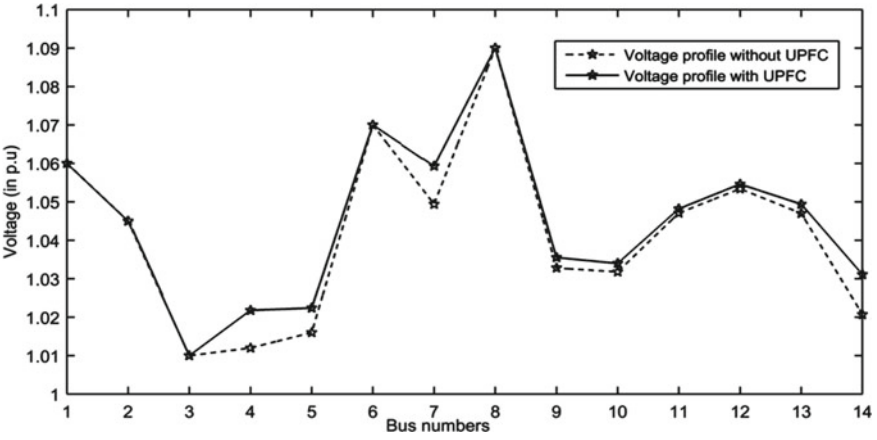

Fig. 5 Bus voltage due to absence and presence of UPFC in IEEE-14 test bus system

Table 1 Bus voltage due to absence and presence of UPFC for IEEE 6 bus system

Bus No.	01	02	03	04	05	06
Bus voltage due to absence of UPFC (pu)	1.05	1.07	1.05	0.9859	0.9685	0.9912
Bus voltage due to presence UPFC (pu)	1.05	1.07	1.05	0.9877	0.9806	0.9936

Table 2 Active power loss value due to absence and presence of UPFC for IEEE 6 bus

From node to node	Active power loss value due to absence of UPFC (pu)	Active power loss value due to presence of UPFC (pu)	From node to node	Active power loss value due to absence of UPFC (pu)	Active power loss value due to presence of UPFC (pu)
2–3	0.00106	0.00093	2–4	0.02326	0.02254
6–3	0.00957	0.00926	2–1	0.00142	0.00137
2–5	0.01199	0.01079	1–4	0.01013	0.00988
4–5	0.00128	0.00124	1–5	0.01360	0.01271
3–5	0.01178	0	2–6	0.01415	0.01353
5–6	0.00051	0.00018			

6 Conclusion

For the aforesaid system, Newton–Raphson algorithm is used for the minimization of active power loss in PSAT MATLAB software. We have presented two test system IEEE 6 bus and 14 bus system. In this proposed work, shunt series FACTS controller UPFC is placed in weak bus. The results got to signify a critical upgrade in the voltage outline of the test bus systems just as convincing decrement in the losses of lines after incorporating of UPFC. The result acquired by without UPFC is compared

Table 3 Bus voltage due to absence and presence of UPFC for IEEE-14 bus system

Bus no	Bus voltage due to absence of UPFC (pu)	Bus voltage due to presence UPFC (pu)	Bus no	Bus voltage due to absence of UPFC (pu)	Bus voltage due to presence UPFC (pu)
1	1.06	1.06	8	1.09	1.09
2	1.045	1.045	9	1.033	1.036
3	1.01	1.01	10	1.032	1.034
4	1.012	1.0218	11	1.047	1.0482
5	1.016	1.0224	12	1.053	1.0546
6	1.07	1.07	13	1.047	1.0494
7	1.049	1.053	14	1.0207	1.0311

Table 4 Active power loss value due to absence and presence of UPFC for IEEE-14 test bus system

From node to node	Active power loss value due to absence of UPFC (pu)	Active power loss value due to presence of UPFC (pu)	From node to node	Active power loss value due to absence of UPFC (pu)	Active power loss value due to presence of UPFC (pu)
1–2	0.04311	0.04201	4–9	0	0
2–3	0.02337	0.02108	7–9	0	0
2–4	0.01672	0	9–10	0.00006	0.00005
1–5	0.02771	0.02505	6–11	0.00114	0.00107
2–5	0.00921	0.00702	6–12	0.0008	0.0007
3–4	0.00397	0.00376	6–13	0.00248	0.00212
4–5	0.00478	0.00389	9–14	0.00091	0
5–6	0	0	10–11	0.00046	0.00041
4–7	0	0	12–13	0.00011	0.00007
7–8	0	0	13–14	0.00099	0.00055

Table 5 Comparison of total active power losses due to absence and presence of UPFC

Bus system	Active power loss value due to absence of UPFC (pu)	Active power loss value due to presence of UPFC (pu)	Active power loss reduction in %
IEEE 6 bus system	0.09875	0.08243	16.53
IEEE-14 bus system	0.13581	0.11046	18.67

with result acquired from with UPFC. It is clear that after using UPFC active power losses reduces to 15–20% and enhances the voltage stability.

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