New Symmetric 9-Level Inverter Topology with Reduced Switch Count and Switching Pulse Generation Using Digital Logic Circuit

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1 Introduction

Multilevel inverter is one of the most promising and highly reliable voltage source power converters which interconnect the dc system with ac system [1]. Several power electronic switches and dc sources are connected together to create multistep output voltage waveform [2]. The output waveform looks similar to the sinusoidal waveform with minimum harmonic content for a higher number of output levels, and thus eliminates the filter requirements [3]. Multilevel inverters had gained remarkable attractiveness in terms of structure and control techniques due to its better electromagnetic compatibility, less total harmonic distortion, smaller common mode voltage, less dv/dt stress, reduced switching losses, high efficiency and improved power quality [4, 5]. In addition, multilevel inverters have a modular structure, capable of transformerless operation and fault tolerant operation by utilizing multiple redundant switching states with suitable control schemes [5, 6]. Due to these significant capabilities, the multilevel power converters have attracted various industrial applications such as electric traction, electric aircraft power system, uninterrupted power supply system, flexible AC transmission system, photovoltaic power system, electric drives, hybrid electric vehicles and distributed generation [6, 7]. Different classifications of the multilevel inverters used in commercial applications include flying capacitor, neutral point clamped and cascaded H-bridge [6–8]. Among these conventional inverter topologies, cascaded H-bridge inverters have an exact modular structure for a higher number of output levels. There are certain issues in these conventional topologies such as greater number of switches and its associated gate driver circuits, isolated dc sources, voltage balancing problem and so on [8]. Practically, flying capacitor and

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neutral point clamped inverters are not suitable for higher output levels, because they have complex inverter structure and higher ratings for power semiconductor devices which make tedious to implement these inverter structures.

Different multilevel inverters using a reduced number of switches were presented in the literature [1–8]. A new symmetric and asymmetric type multilevel inverter with two dc sources and four switches is proposed in [1]. In this, a separate polarity changing unit is used to obtain the negative output levels. This inverter requires a higher number of switches to generate a staircase waveform. Moreover, complex control is implemented even for low rating power switches with a separate driver circuit. A reduced switch count based multilevel inverter to generate all possible combinations of input dc sources is presented in [2]. This inverter has the capability to operate in both lower and higher switching frequencies. However, high spikes may occur in the voltage waveform due to the lack of path for reverse current flow. In [3], a new basic unit with three sources and five unidirectional switches is proposed to generate only positive levels at the output. To obtain the negative levels, H-bridge is used as a polarity changing unit. This would results in higher voltage stress across the switches for higher output results and need higher rate power semiconductor devices. Another multilevel inverter topology with an array of voltage sources in additive nature is proposed in [4]. This inverter produces all levels of the output voltage by switching the appropriate power semiconductor devices. This topology lacks modularity and restrictions on modulation strategy and control method. The basic unit of the inverter proposed in [5], consists of four dc sources and ten switches and create 17-level during asymmetric operation. To create higher output levels, several basic circuits can be connected in series across the load terminals. The main drawback of this topology is not suitable for high voltage applications because of high variety of voltage sources and TSV value. In [6], a new extendable type multilevel inverter with various ratings of both unidirectional and bidirectional switches is presented. This topology reduces the number of switches for higher output levels and extending the use for low voltage and high power application. However, this topology lacks the attribute of combining two dc sources in parallel and does not own the equal load sharing capability. Other inverter topologies using an efficient fundamental switching technique are presented in [7, 8].

This paper aims to develop more reliable 9-level inverter topology with a minimum number of circuit components. Section 2 presented the operation of the proposed symmetrical 9-level inverter topology. A comparison study is done in Sect. 3. The switching strategy using digital logic circuit based multicarrier pulse width modulation (PWM) technique to obtain the switching signals for the proposed 9-level inverter is explained in Sect. 4. Section 5 presents the simulation results of the 9-level inverter and the conclusion is given in Sect. 6.

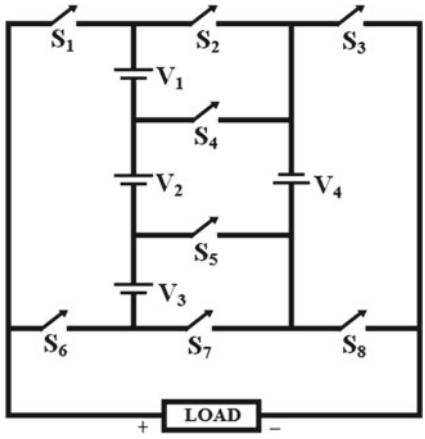


Fig. 1 Proposed 9-level inverter

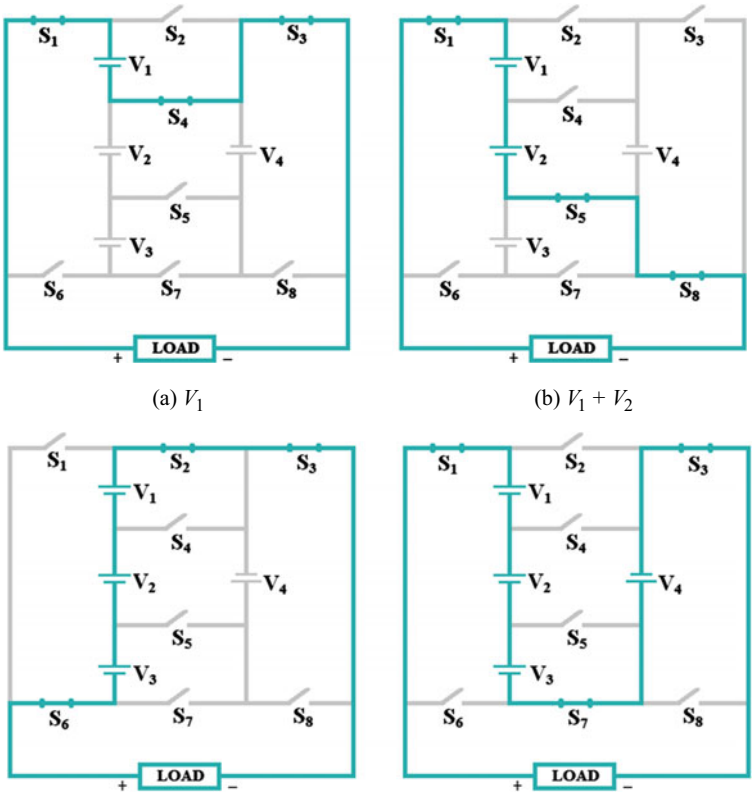
2 Proposed 9-Level Inverter

The proposed 9-level symmetrical multilevel inverter topology with four dc voltage sources and eight power electronic switches is shown in Fig. 1. Here, the voltage sources V_1, V_2, V_3 are connected in series and the combination is connected in parallel with the source V_4. In order to avoid short circuit across the dc sources, the pairs of switches (S_1, S_6), (S_2, S_4, S_5, S_7), (S_3, S_8) should not be turned ON simultaneously. To create 9-output levels, the magnitude of all dc sources V_1, V_2 and V_3 should be equal. The important feature of the proposed symmetric topology is its inherent ability to create negative levels without additional H-bridge.

Some of the sample output levels obtained at the inverter output terminals are shown in Fig. 2. The blocking voltage across the switches S_3 and S_8 is V_{dc}. For switches S_2 and S_7, the blocking voltage is $4V_{dc}$ and for the remaining switches, this value is equal to $3V_{dc}$. Therefore, the total standing voltage (TSV) across the switches of the proposed 9-level inverter topology is $22V_{dc}$.

3 Comparison Study

Table 1 presents the comparison between the proposed 9-level symmetric inverter with other symmetrical topologies presented in the literature. This comparison study is presented based on the total number switches, ON-state switches and value of TSV. As shown in Table 1, the proposed 9-level inverter topology inherently creates negative output levels, however, the topologies presented in [4–6], need an additional H-bridge circuit as a polarity changing unit to produce negative output levels. The comparative study shows that the proposed inverter topology creates a 9-level output with a minimum number of switches. The proposed inverter uses only eight switches, however, the topology presented in [1], needs 12 switches, the inverter presented in



(a) V_1 (b) $V_1 + V_2$

(c) $-V_1 - V_2 - V_3$ (d) $V_1 + V_2 + V_3 + V_4$

Fig. 2 Different output voltages

Table 1 Comparison study

Topology	No. of switches	ON-state switches	TSV	Negative level
[1]	12	4	$28V_{dc}$	H-bridge
[2]	16	8	$29V_{dc}$	H-bridge
[3]	11	4	$27V_{dc}$	H-bridge
[4]	10	5	$28V_{dc}$	Inherent
[5, 6]	10	4	$25V_{dc}$	Inherent
Proposed	8	3	$22V_{dc}$	Inherent

[2], needs 16 switches and the 11 switches are needed for the topology presented in [3]. Additionally, the proposed topology need only three ON-state switches to create 9-output levels. But, the topologies presented in [1, 3, 5, 6], needs four ON-state switches, the topology presented in [4], needs five ON-state switches and the

inverter shown in [2], needs eight ON-state switches. The reduction in the number of conducting switches reduces the inverter losses and increases its efficiency. Also, it is noted that the TSV value for the proposed inverter is $22V_{dc}$. Therefore, the inverter size, cost and complexity is significantly reduced.

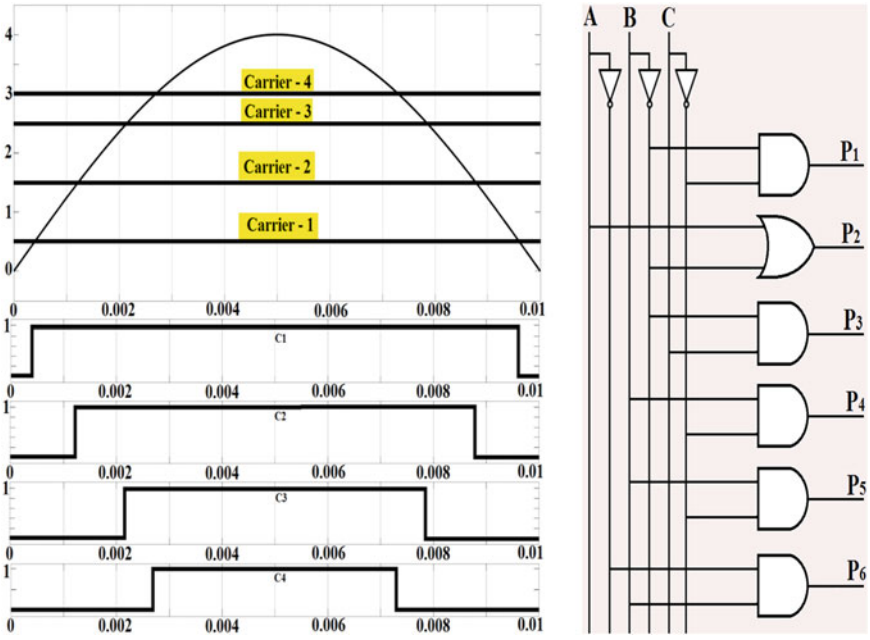
4 Switching Pulse Generation

A modified multicarrier based digital logic technique is used to obtain the switching pulses. In this technique, the stage-1 signals C_1, C_2, C_3, C_4 are generated by comparing the sinusoidal reference signal with four different carrier signals. The magnitude of the carrier signals are determined by

$$V_{Ck} = \frac{2k-1}{2} \text{ where, } k = 1, 2, 3, 4$$

The generation of stage-1 signals during a positive cycle is shown in Fig. 3a.

The following equation helps to obtain the intermediate signals *A*, *B* and *C* from the stage-1 signals:



(a) Stage -1 (b) Stage -2

Fig. 3 Switching pulse generation

$$A = C_4$$
$$B = C_2$$
$$C = C_1 - C_3$$

In the next stage, using fundamental digital logic gates such as AND, OR and NOT gates, different stage-2 signals $P_1 - P_6$ are generated as shown in Fig. 3b. Finally, the required switching pulses for the proposed symmetric inverter is obtained by

$$\begin{aligned} S_1 &= T_1 & S_5 &= P_4T_1 + P_3T_2 \\ S_2 &= P_1T_1 + P_5T_2 & S_6 &= T_2 \\ S_3 &= P_2T_1 + P_6T_2 & S_7 &= P_5T_1 + P_1T_2 \\ S_4 &= P_3T_1 + P_4T & S_8 &= P_6T_1 + P_2T_2 \end{aligned}$$

where, T_1 is the signal which is logic-1 during the positive cycle and logic-0 during the negative cycle and T_2 is the signal which is logic-0 during the positive cycle and logic-1 during the negative cycle.

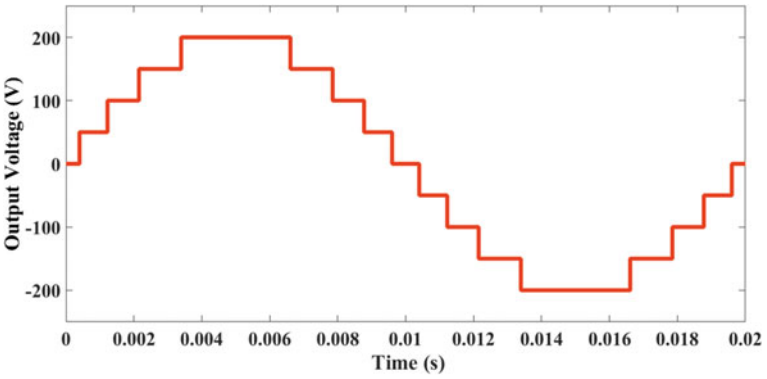
5 Simulation Results

The magnitude of the voltage sources are $V_1 = V_2 = V_3 = V_4 = V_{dc} = 50\,\text{V}$. The 9-level inverter output voltage waveform and its THD are shown in Fig. 4a and b, respectively.

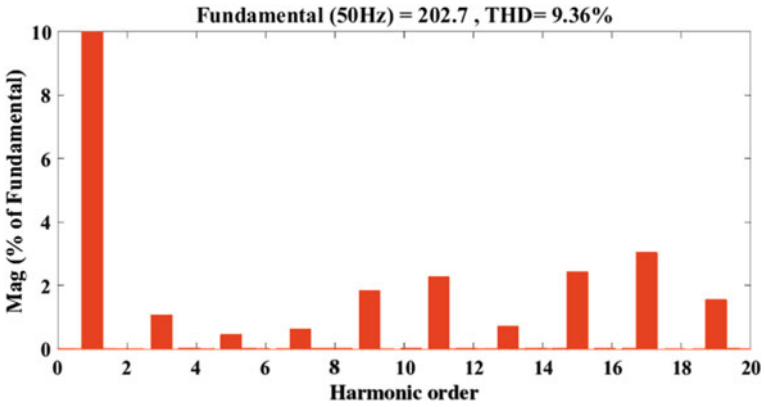
As expected, the output voltage is of staircase waveform with THD as 9.36%. The output voltage and current waveforms for the proposed 9-level inverter for different series RL load parameters are shown in Fig. 5. For pure resistive load, $R = 35\ \Omega$, the load voltage THD and load current THD are equal to 9.36%. Also, it is observed that the load current THD is varying between 2.35 and 9.36% as the power factor of the load varies from 0.5 to 1.

6 Conclusion

In this paper, a new symmetrical 9-level inverter topology with reduced number of switches is recommended. The proposed inverter uses four dc voltage sources and eight power switches to generate a 9-level voltage across the series RL load. The proposed inverter structure is compared with several other symmetrical topologies



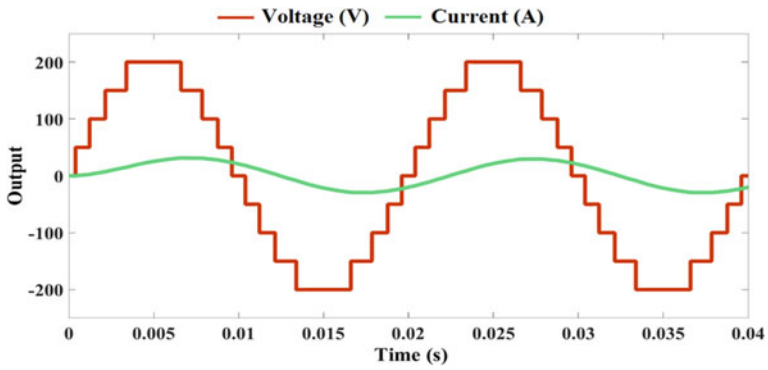
(a) Output voltage



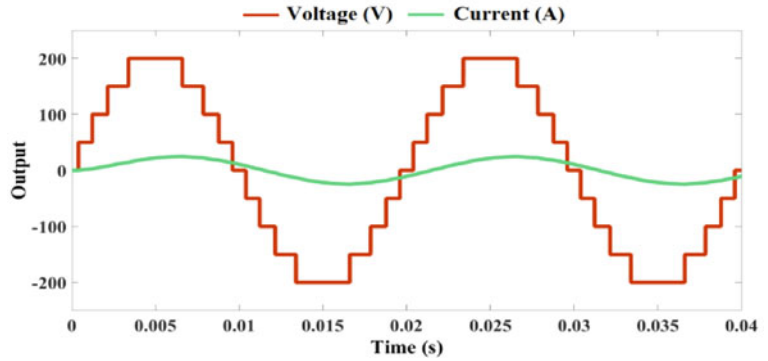
(b) THD

Fig. 4 Simulation results

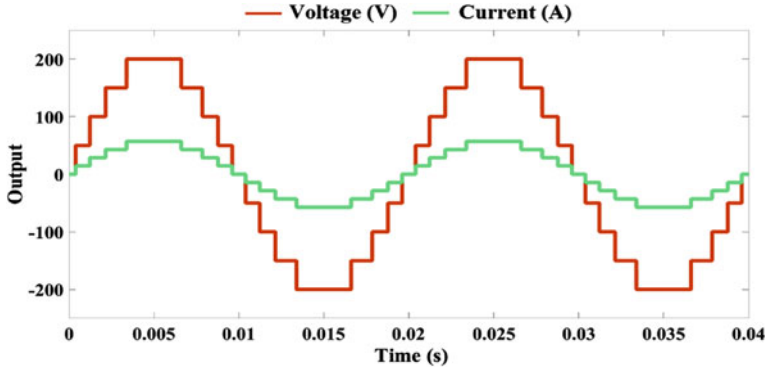
which indicate the reduction in the number of switches, total number of conducting switches and TSV value, which in turn, achieves higher inverter efficiency and lower switching losses. Finally, the inverter performance is analyzed by generating a 9-level output voltage using Matlab/Simulink.



(a) *pf=0.5*



(b) *pf=0.8*



(c) *pf=1*

Fig. 5 Output waveforms

References

1. V. Thiyagarajan, P. Somasundaram, Multilevel inverter topology with modified pulse width modulation and reduced switch count. Acta Polytechnica Hungarica **15**(2), 141–167 (2018)
2. N. Prabaharan, Z. Salam, C. Cecati, K. Palanisamy, Design and implementation of new multilevel inverter topology for trinary sequence using unipolar pulse width modulation. IEEE Trans. Industr. Electron. **67**(5) (2020)
3. E. Babaei, S. Laali, Z. Bayat, A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches. IEEE Trans. Industr. Electron. **62**(2), 922–929 (2015)
4. M. Jayabalan, B. Jeevarathinam, T. Sandirasegarane, Reduced switch count pulse width modulated multilevel inverter. IET Power Electron. **10**(1), 10–17 (2017)
5. V. Thiyagarajan, P. Somasundaram, Modeling and analysis of novel multilevel inverter topology with minimum number of switching components. CMES **113**(4), 461–473 (2017)
6. V. Thiyagarajan, P. Somasundaram, K. Ramash Kumar, Simulation and analysis of novel extendable multilevel inverter topology. J. Circuits Syst. Comput. **28**(06), 1950089-1-25 (2020)
7. P.K. Kar, P. Anurag, S.B. Karanki, Development of an enhanced multilevel converter using an efficient fundamental switching technique. Int. J. Electr. Power Energy Syst. **119**, 1–13 (2020)
8. D.S. Vanaja, A.A. Stonier, A novel PV fed asymmetric multilevel inverter with reduced THD for a grid-connected system. Int. Trans. Electr. Energy Syst. **30**(4), 1–15 (2020)