Chapter 8
FinFET: A Beginning of Non-planar Transistor Era

Kajal and Vijay Kumar Sharma

Abstract Aggressive scaling of metal–oxide–semiconductor field-effect transistor (MOSFET) is a barrier in the progress of very large-scale integration (VLSI) technology, and new innovative devices and techniques are always required to boost the electronics industry. Fin-shaped field-effect transistor (FinFET) is the appropriate device to eliminate the limitations of MOSFET devices. FinFET is a three-dimensional (3D) multi-gate transistor with improved channel stability, less short channel effects (SCEs) and excellent isolation compared to the MOS transistor. The best qualities of FinFET that attracts research designers are better SCEs, improved subthreshold slope, less random doping fluctuation and independent gating. Process, voltage and temperature (PVT) variation is one of the scaling problems in MOSFET devices, and due to PVT variations, the circuit shows abnormal power consumption and performance degradation. In this chapter, we concentrate on the influence of PVT variations on different FinFET-based circuits. PVT variations can cause deviation in power consumption, delay and leakage current which finally degrade the performance of FinFET devices.

Keywords FinFET · PVT variations · Ultra-low-power VLSI technology · CMOS

8.1 Introduction

Improvement in VLSI technology is necessary for the betterment of electronic devices. MOSFET device dominated the entire VLSI technology from many years, but now due to further scaling of MOS devices it leads the severe SCEs, subthreshold leakage, more standby power dissipation and reliability variations which drastically affects the circuit performance and reliability of the system (Turi and Delgado-Frias 2017). The main challenge faced by future bulk MOS scaling is process and material technology limitations. Continuous efforts are made by the researchers to expand

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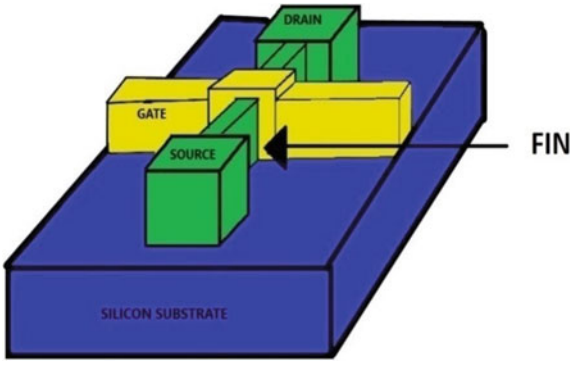

Fig. 8.1 Basic FinFET structure

the silicon scaling results into innovative material and device structures to overcome the limitations of bulk MOSFET. A FinFET is one of these innovations, and FinFET becomes a popular transistor due to its front and back gate structure. The transistor's current and threshold voltage can monitor by biasing these gates properly which helps to manage the problem of standby power dissipation. Figure 8.1 represents the structure of FinFET device (Gupta et al. 2019). Multi-gate transistors are a considerable option for nanoscale VLSI technology. FinFET gains the limelight among all multi-gate MOSFET devices due to its better control to SCEs, lower leakage, excellent isolation and more driving capability for both low-power and fast speed applications.

Most of FinFETs are double-gate devices with vertical fins in the gate. In FinFET, channels are created on both sides of the fin and at the top end. There are no free carriers available because of the finlike structure, so this particular FinFET structure is the main reason for suppressing SCE in FinFET (Zimpeck et al. 2015). Better subthreshold slope, excellent SCE control, independent gating and less random doping fluctuation are the best qualities of FinFET that makes it more superior to MOS technology (Bagheriye et al. 2018). The front and back gate of FinFET provides better control over the channel which in turn reduces the leakage current and SCE, so FinFET is the suitable device to replace the MOS technology in the future VLSI technology (Taghipour and Asli 2017; Mukhopadhyay et al. 2018). Due to the low leakage power of FinFET, it becomes a very popular choice for memories. Memories are used most commonly in digital systems, and a large amount of power is saved in memories with FinFET devices.

8.1.1 Scaling Challenges in MOSFET

Aggressive scaling of MOSFET causes various challenges in VLSI technology, and one of the most prominent drawbacks of MOS scaling is SCE. In a deep submicron region, when the channel length of device is less than 100 nm, SCEs start to degrade

the circuit performance and are also known as second-order effects. The key SCEs are hot carrier effect, threshold voltage variations, gate-induced barrier lowering, velocity saturation.

Due to short channel length, subthreshold or weak conduction current occurs between the drain and source in MOS transistor when the gate voltage (V_{GS}) is less than the threshold voltage (V_T). This small leakage current is known as subthreshold leakage current and affects the performance of the transistor. Detail of scaling challenges and its impact on CMOS performance is studied in reference (Jacob et al. 2017). Most portable devices, such as mobile devices, laptops and various communication devices, have long downtime and run in standby mode if not in use. But there is a small leakage current flow through the circuit due to short channel length which causes the standby power dissipation. The researcher had suggested various techniques for overcoming the shortcomings of CMOS transistors (Sharma and Pattanaik 2014). Figure 8.2 represents the main scaling challenges in MOS technology.

Currently, one of the extremely challenging areas of research is to minimize the leakage power consumption, mostly in on-chip devices which are doubling in every two years. It is more challenging to minimize the static leakage power than the dynamic leakage power because, in dynamic power, the leakage power depends on transistors count, their operating status and type without taking into consideration the switching operation. On the other hand, when a transistor is in the OFF state, there are no input applied to a transistor, it has reached a stable state, and a small amount of leakage current flows through the transistor and causes power dissipation

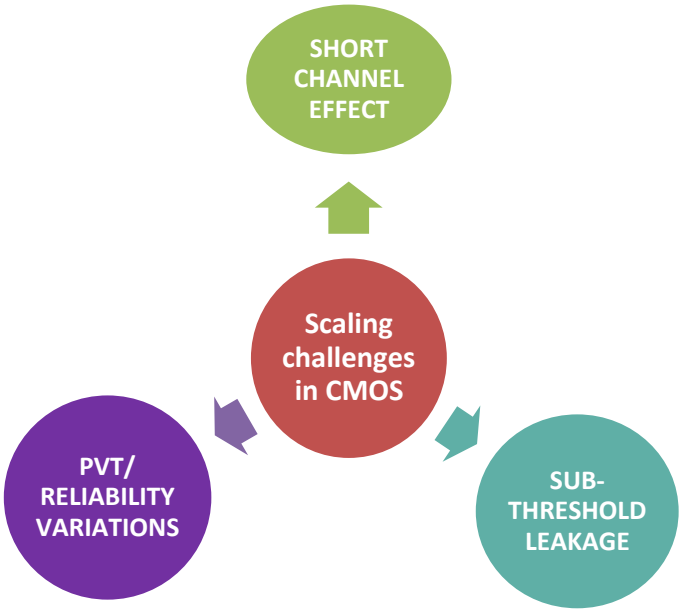

Fig. 8.2 Scaling challenges in MOS technology

(Upasani et al. 2010). There are many advantages of scaling like the compact size of the devices and high speed. Despite this, there are some limitations of scaling in terms of SCEs which cause leakage current hence increasing power dissipation.

Subthreshold leakage current harms the characteristics of the devices and affects the reliability of the devices. PVT variability and reliability effect are major issues in present VLSI technology. One of the most critical and common problems of reliability is negative temperature bias instability (NBTI). NBTI directly challenges the reliability of digital VLSI devices. As a result, the circuit delay exceeds the design specification and there may be timing violations or logic failure (Mahapatra et al. 2013; Khoshavi et al. 2017). Nowadays, electronic devices are facing a problem of PVT variations and it affects the various performance parameters. The electronics industry is moving from MOS transistor to FinFET, but the problem of PVT variations is still present (Sharma and Pattanaik 2014; Yang and Jha 2014).

In this chapter, we are focusing on PVT variations and consider the impact of PVT variability on FinFET devices and various techniques or methodologies adopted by the researcher to mitigate the PVT variability effect.

8.1.2 FinFET Structure and Operation

The further scaling of MOS transistors is not much profitable for both the research community and the VLSI industry. FinFET is an appropriate transistor to take the position of the MOS transistor. Dr. Chenming Hu has been known as the father of the 3D transistor because he has proposed the concept of FinFET in 1999 (Gupta et al. 2019). FinFET is a type of non-planar or 3D multi-gate transistor in which the channel has a thin vertical fin and the gate is fully enclosed around the channel between the drain and the source. It looks like a fin of fish when viewed so its name has been derived from this fact. FinFET channels are created at the topside and two sidewalls of a fin which provide better control on the channel and give better electrostatic control and electrical characteristics (Zimpeck et al. 2015). High channel doping is required for low leakage current in MOS devices, but this degrades the carrier mobility of a transistor. Gate dielectric with high ON current and good channel control is highly on demand for low-power applications. The gate leakage current through thermal oxide becomes escalated as oxide thickness approaching 2 nm (Rosner 2003).

The working operation and fabrication process of FinFET are almost identical to MOS except for some modifications (Walke et al. 2017; Chen et al. 2018). One of the challenges of manufacturing the FinFET is doping of the drain–source junction in the fin region. Uniformly distributed doping is needed along the fin height and width so that angled implantation is required on the side of the fin. In the case of planar device junction formation, there are various standard techniques for analyzing and monitoring the implantation of dopant on the planar surface, but these methods are not suitable for FinFET junction formation due to the 3D structure of a fin (Pham et al.

2006; Lee et al. 2010). Fin height is the most important parameter for the FinFET fabrication process because it determines the minimum FinFET width (W_{min}). A minimum transistor width of two gates FinFET is given below (Gupta et al. 2019):

$$W_{min} = 2H_{fin} + T_{fin} \tag{8.1}$$

Here, H_{fin} is the fin height and T_{fin} silicon body thickness. A fin height has more impact on transistor width than the T_{fin} component as seen from Eq. (8.1). H_{fin} is fixed in a FinFET, so to increase the FinFET width we can create multiple parallel fin structures. The total physical transistor width (W_{total}) of a tied FinFET gate with n parallel fins can be calculated as shown in Eq. (8.2) (Gupta et al. 2019)

$$W_{total} = nW_{min} = n(2H_{fin} + T_{fin}) \tag{8.2}$$

FinFET is designed with multiple parallel fins to achieve larger channel widths (Colinge 2008). The number of fins at FinFET should be increased to increase the current through the transistor (Sinha et al. 2012; Tawfik et al. 2007). A multiple fin structure of FinFET achieved superior performance but increases the device degradation due to hot carrier effect. When FinFET has multiple fins, then coupling effect in the steep and silicon fin decreases the conduction of the inversion channel carrier and degrades the FinFET performance (Yeh et al. 2018). Double-gate FinFET structure is more preferable due to this reason because it improves the electrostatic integrity, reduces the SCE and minimizes leakage current (Yang and Jha 2014).

The three types of FinFET structures are: shorted gate (SG) FinFET, independent gate (IG) FinFET and asymmetric gate work function shorted gate (ASG) FinFET. In SG FinFET, two gates at the top are shorted together and provide a large drive current. ASG FinFET is the same as SG FinFET in case of a layout area, but ASG FinFET having a different work function for both the gates. ASG FinFET provides a lower leakage current but degrades around 26% of ON state current (I_{ON}). If both FinFET gates are controllable independently, then FinFET is called IG FinFET. IG FinFET has less leakage current than SG FinFET, but it increases the layout area and causes severe degradation in ON state current (Bhattacharya et al. 2015; Yang and Jha 2013).

8.2 PVT Variations

PVT variations are one of the scaling challenges faced by the FinFET technology, show abnormal power consumption due to PVT variations and accelerate the degradation of the circuits (Zimpeck et al. 2015). Variations are classified into two categories: process variation and environmental variation. Additional environmental variability involves variation in temperature and supply voltage across the circuit. The key source of variation in supply voltage variation and temperature variation is voltage (IR) drop in power grid and switching activity deviation across the chip, respectively.

The principal cause of process variation (PV) is variations in the physical parameters of devices that take place during a manufacturing process.

8.2.1 Process Variations

PV is introduced during the fabrication process due to unavoidable errors. As VLSI technology moves toward the deep submicron regime, integrated circuits (ICs) become more sensitive to PV. Process variation is divided into two parts: non-systematic and systematic. A variation in the electrical characteristics of two transistors with the same length and width is recognized as systematic variations and can be adjusted by detailed layout analysis during the manufacturing process. On the other hand, non-systematic variation is a non-predictable part of process variation, and these variations are an unexplainable component of the fabrication process. Non-systematic variations are further classified into two parts: intra-die variation and inter-die variation. Inter-die variation is due to the lack of manufacturing control and induced by technical constraints. Deviation in some parameter value over nominally equivalent manufactured dies refers to inter-die variation. Inter-die variations may occur on the different wafers, or same wafer or different lots (Ezz-Eldin et al. 2015). Figure 8.3 shows the classification of variations. Among all these variations, voltage,

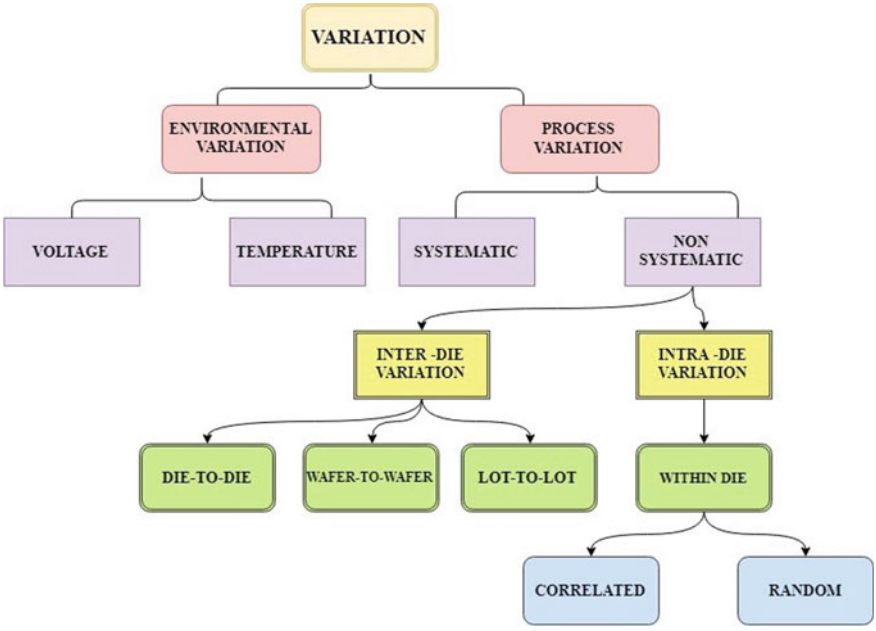

Fig. 8.3 Classification of variation

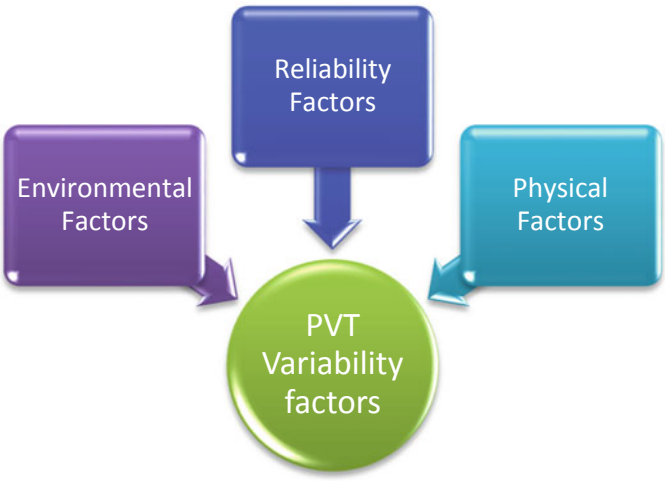

Fig. 8.4 Main factor of PVT variation

temperature and systematic variations can be evaluated and improved by researchers. On the other hand, non-systematic variations are difficult to identify and become unpredictable parts of variations. Intra-die variation affects the various devices on the same die differentially and is further categorized into correlated and random variation. Correlated variation depends on the location of the devices. This closely spaced device has more similar variations than those located far apart. Etching, layout and lithographic information can be required to design, estimate and reimburse for correlated variation. Random variation is considered statistically independent of all other variation components.

Random variation results from edge roughness of gate line and fluctuation of random dopant. Figure 8.4 shows the main factor of PVT variation. During the manufacturing process lithography phase, process variations are mostly induced and the variability in PVT can be divided into three factors:

- Environmental factors: Power supply and temperature fluctuations are the main causes of environmental variations and mainly appeared during the circuit operations.
- Reliability factors: Mainly caused by a transistor aging and the high electrical field in modern circuits.
- Physical factors: Variations in geometric and electrical parameters which induce a lag in transistor performance also trigger process variation.

8.2.2 Supply Voltage Variation

Voltage drops or noisy power sources are the main source of supply voltage variations. Supply voltage variations have a great impact on leakage power, dynamic power and logic gate timing (Yang and Jha 2013). One of the most important parameters of the circuit is supply voltage because it affects the system performance. The gate delay depends upon the saturation current, and saturation current depends upon the supply voltage. FinFET technologies use high-*k*/metal gate stack to boost gate control over channel region, the main source of statistical variations is metal gate granularity, and this contributes to grain orientations that have different work functions. These imperfections can influence the various parameters of FinFET, and the entire block of cells compromises due to variations in transistor structure. Therefore, circuits also suffer from some electrical deviations (Zimpeck et al. 2018; Ban et al. 2014).

8.2.3 Temperature Variations

The temperature of the blocks in IC depends on the power consumption of a block itself and on lateral heat transfer; it also depends on adjacent blocks. A temperature variation comes under the environmental variation factor and mainly causes due to deviations in switching activities of the device. Fluctuations in temperature are dictated by the leakage current and timing characteristics. Due to the unpredictable dopant fluctuation and the sub-wavelength lithography, nanodevices are more susceptible to variability effect. PV directly affects the threshold voltage of FinFET varying various aspects of transistor cells (Almeida et al. 2018). PVT variations are inherent, and essential steps must be taken during the early design step. Figure 8.5 presents the geometric parameters of FinFET which include drain, source and gate (Lee and Jha 2014). To reduce leakage current (I_{OFF}) and improve ON current (I_{ON}), fin engineering is the most essential part during the fabrication process (Yang and Jha 2014). A previous study shows that fin width and gate length have a major impact on I_{ON} and I_{OFF}, but the greatest variance in both currents is due to work function fluctuations (WFFs) that creates a significant deviation in total power that must be considered in the design of VLSI.

PV is inherent in the fabricating processes of semiconductors and impacts on circuit performance and reliability. It is becoming more difficult to determine the circuit performance with the constant change in the circuit elements (logic gates and interconnections). Interconnect variation and gate variation appear to be considering in random variations. Uncertainties in metal line dimensions lead to interconnect variations. A variation in gate process causes change in MOS parameters which create the gates manufactured different from the ones designed. Gate width (W_{GATE}), gate oxide thickness (T_{OX}), gate length (L_{GATE}) and threshold voltage (V_T) are mostly affected parameters by the process variation during the fabrication process (Zimpeck et al. 2015). PV impact translates into variation in device and interconnects electrical

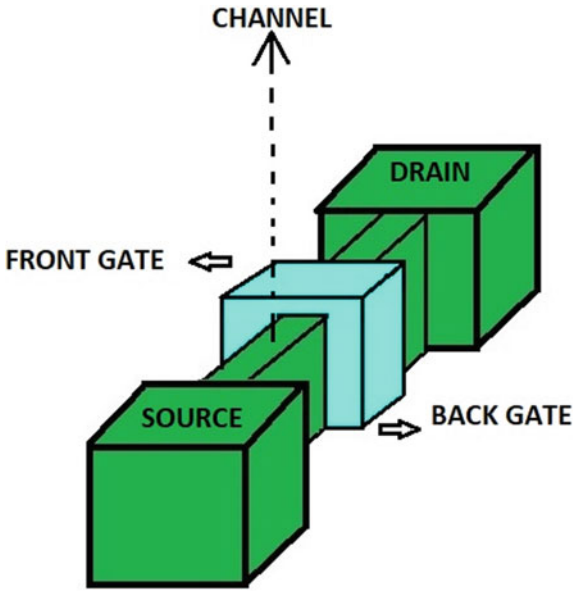

Fig. 8.5 Geometric parameters of FinFET

parameters such as delay, throughput and leakage power variation. FinFET is one of the newest transistors in VLSI technology, and many works are going on.

8.3 Literature Review

Continuous scaling of the MOSFET leads to an increase in aging effect, leakage current and soft error that compels the VLSI technology to move toward the multi-gate devices. FinFET is the best multi-gate device because of its outstanding isolation and high driving capacity for both low-power and high-speed applications. PVT variation is a challenging problem in FinFET and degrades the circuit performance, so researchers have adopted various techniques and methodologies to alleviate this effect. In this part, we are discussing the impact of PVT variations on FinFET devices and various techniques/methodologies adopted by researchers to improve the performance of FinFET devices.

8.3.1 Impact of PVT Variations on FinFET-Based Memories

Memories are always a big part of VLSI digital technology, and applying the FinFET technology to memories introduces an evolution in digital technology due to a huge amount of power-saving. Static random access memory (SRAM) is one of

the commonly used memories in VLSI technology, and it always demanded faster design and lower power consumption. Data stability is the biggest problem in the SRAM cell, and this problem becomes more severe with scaling of MOSFET in the sub-nanometer regime. Intra-die and inter-die variations are the main cause of instability in SRAM, so multi-gate devices like FinFET become a better choice for SRAM cell (Kushwah et al. 2016). The impact of FinFET technology on SRAM cells, back gate biasing strategies and performance of SRAM cell under temperature, voltage and parameter variations can be seen in Turi and Delgado-Frias (2017). Leakage power can be reduced up to 65X in a six-transistor FinFET SRAM cell (Tawfik and Kursun 2008).

Researchers proposed IG FinFET SRAM cells that used back gate biasing and PMOS access transistors to achieve high stability performance (Bagheriye et al. 2018). Designers find that FinFET is more appropriate than MOS in deep submicron region especially after 22 nm because of its excellent SCEs, improved sub-threshold slope, independent gating, and less random doping fluctuations. Researchers proposed an architecture-level approach to improve the array robustness, but this type of approach results in area overhead and makes complex circuit design. Researchers also suggested design of FinFET SRAMs based on asymmetric structures like asymmetric drain and source, having different work functions and oxide thickness for the FinFET front and back gate. Those structures are highly sensitive to fluctuations in process parameters. There are various techniques to improve SRAM performance in reference (Bagheriye et al. 2018) and given as:

- Front and back gates are operating independently as they offer flexibility in design as a substitute for threshold voltage control for improving the cell stability of FinFET SRAM.
- A write static noise margin (WSNM) and read static noise margin (RSNM) are enhanced by decreasing and increasing the threshold voltage of an access transistor, respectively, using the independent gate.
- To dynamically increase the RSNM without increasing the area overhead, built-in feedback technique is used in which the back gate of the access transistor is connected to corresponding nodes.
- In some approaches, the p-channel metal–oxide–semiconductor (PMOS) is used in place of the n-channel metal–oxide–semiconductor (NMOS) to improve circuit stability and reduce the risk of leakage current.
- To reduce an access time, strain effect is incorporated with PMOS access transistor in the SRAM cell.
- Schmitt's trigger-based feedback system was used to increase the RSNM, WSNM and tolerance to PV in the subthreshold region, but these cells suffer from low read current and area overhead in this procedure.

The author proposed two cells in reference (Bagheriye et al. 2018); first cell consumes low power and enhances the read and write margins. The second cell provides high write and read margins with high read current. Aging effect due to BTI influences, PVT variations and single event upset is the main issue in nanometer IC design. Read noise margin is the most sensitive SNM and is deeply affected by

PVT variation and aging effect (Almeida et al. 2018). Read operation is performed by a P-type gate and write operation performed with the help of transmission gate to achieve high switching activity in 7T FinFET SRAM. This type of configuration of SRAM provides up to 60.8% of supply voltage reduction (Sneha et al. 2017).

Standard MOS scaling technology driven by higher operating speed, integration density and lower power dissipation has faced many barriers. Now, it is facing a severe variability problem. The researcher introduces a technique for the design of SRAM cell that is aware of variability. The proposed cell's architecture is identical to that of the regular 6T SRAM cell apart from that the access pass gates are replaced with transmission gates. The impact of variation on most of SRAM cell's design metrics degrades circuit efficiency. Comparative analysis based on Monte Carlo simulation shows that the proposed design is capable of greatly mitigating the impact of variation (Islam and Hasan 2012). The detailed comparative investigation of CMOS and FinFET-based 10T SRAM cells is given and can be studied in reference (Pal et al. 2014).

On the other hand, content addressable memory (CAM) used for lookup table based application which enables high speed parallel search operations. Researchers evaluate the design space for FinFET CAMs for symmetric and asymmetric gate work functions (Bhattacharya et al. 2015). Researchers proposed diverse designs and conducted their transient and DC analysis for various mismatch conditions using the computer-aided design (CAD) tool with 22-nm FinFET devices. CAMs are often used in signal processing and in wireless sensor network applications requiring very low power consumption and extremely high speed so that this can be accomplished by developing a CAM using 22-nm and 14-nm PMOS access transistors based on the PTM-MG transistor model. From the available literature, we conclude that IG FinFET displays increased speed and lower power consumption (Arulvani and Mohamed Ismail 2018).

8.3.2 FinFET Standard Cells Under PVT Variability

Researchers evaluate the impact of PVT variations on power off predictive standards and timing at 20-nm FinFET technology node. The main factors in PVT variations are environmental factors, physical factors and reliability factors. Variations in electrical and geometrical parameters also provoke a delay in a transistor's performances. Fin height, gate length, fin thickness and metal gate work function fluctuations are the main causes of process variability in FinFET devices. Researchers use more than 10,000 Monte Carlo simulations with work function parameters for PVT variability investigation. Work function fluctuations have a huge impact on OFF state leakage current, and it causes a significant deviation on the static power of standard cells (Zimpeck et al. 2015).

8.3.3 Flip-Flop Performance in FinFET Technology

The impact of aging effect and PVT variations on different flip-flops in FinFET and CMOS technologies and their comparative performance analysis can be seen in reference (Taghipour and Asli 2017). Hot carrier injection (HCI) and bias temperature instability (BTI) mainly affect the heftiness of high-performance FinFET. Researchers acknowledged that temperature and VDD variations are the main causes of power–delay product (PDP) degradation and propagation delay for different FinFET structures.

An average increase of performance is obtained from the following equation (Taghipour and Asli 2017)

$$\text{Average increase}(\%) = \frac{\text{aged} - \text{Fresh}}{\text{Fresh}} \times 100 \tag{8.3}$$

The long-term model can be utilized to estimate the V_T variations, and then the updated V_T is applied to the transistor model file to evaluate the BTI and HCI aging mechanism for reliability analysis. Continuous scaling of a transistor increases the consequence of process variations and aging in circuits. The effect of PV and NBTI aging over the years on the WNMs and the consequent statistical occurrence of write failures in several types of flip-flop cells is presented in reference (Khalid et al. 2015). An analysis based on the statistical characterization of WNMs is using transistor-level Monte Carlo simulations to evaluate the write failure probability as a result of an input voltage change in flip-flop cells.

8.3.4 Impact of Time Zero Variability and BTI on FinFET Devices

Time zero variation or prestress variations of the device are the main unease in scaled technology, and detailed study of time zero variability performance of the device helps to improve the circuit performance. Researchers evaluated that device degradation occurs due to time zero PV and BTI stress conditions and also studied the variations in a threshold voltage of a planar 10-nm FinFET system on chip, 16-nm FinFET and 20-nm FinFET device. The following points are studied in reference (Mukhopadhyay et al. 2018):

- An impact of BTI and time zero V_T variations on V_T.
- Evaluate NBTI and positive bias temperature instability (PBTI), and their statistical performance is compared.
- SNM degradation in SRAM cell due to bias temperature instability.
- At last, bit- and chip-level high-temperature operating life (HTOL) test results are studied.

8.3.5 Impact of PVT Variations on FinFET Under Different Sizing Techniques

Different transistor arrangements can cause variations in gate variability. We can find a most suitable topology which increases the robustness of cells regarding PV. Any obviously occurring variations in the attributes of transistor like length, width and oxide thickness during the fabrication of IC are related to PV issue. The best approach for reducing the PV issue is to utilize the network which has transistors in series and as far as possible to the output (Zimpeck et al. 2018). Researchers investigate the impact of variation on power consumption and performance for various transistor sizing approaches applied to circuits in FinFET technologies and evaluate PVT variations separately. Temperature and voltage variations are united to get an insight into their contributions. Results are beneficial to describe the variability effect in the initial design steps to choose suitable transistor sizing technique for an application (Zimpeck et al. 2016).

8.3.6 Energy-Efficient Compressor Based on FinFETs

Multiplier is one of the important required arithmetic blocks in digital signal processing (DSP) applications and also the major energy and time-consuming block for an enormous variety of applications. So, we can improve the efficiency of these circuits by introducing FinFET in it. A designer has introduced a new energy-efficient 4:2 compressor that has less transistors, smaller areas and superior energy efficiency. This compressor provides an improvement in terms of energy efficiency and has less area overhead than the previous design (Arasteh et al. 2018).

8.3.7 Impact of Multiple Parallel Fins on FinFET

The unique structure and geometry of FinFET as compared to CMOS makes FinFET more reliable and efficient than CMOS. 3D fin structure of FinFET contains the current conduction between source and drain. Multiple parallel fins can be fabricated between source and drain that increases the channel width. The number of fins on FinFET shows a great impact on circuit performances and reliability. Multiple parallel fins can be used to increase the total drive current but in this case, FinFET suffers from severe degradation. A multiple parallel fin structure of FinFET reduces the inversion charge by creating charge repulsion between the fins. This increases the coupling effect between fins, and HCI is always an issue in a deep submicron region (Yeh et al. 2018).

8.3.8 *Multicore Power, Area and Timing (McPAT)-PVT: Modeling Framework for FinFET Under PVT Variations*

FinFETs have become an appropriate transistor to replace the conventional MOS transistor due to their better scalability, efficiency and a better SCE control. FinFETs have some lithographic, fabrication and environmental limitations which lead to PVT variations in FinFET IC. So, due to these variations, delay and leakage are introduced into the FinFET ICs. McPAT-PVT is an integrated framework that is considered for analysis of delay, power and PVT variations of FinFET devices. This framework consists of FinFET logic, design library and memory cells to represent circuit-level characteristics and PVT variations. Both SG and ASG FinFET-based processors are modeled by McPAT-PVT. ASG mode implementation provides the same performance but, it increases the area and more beneficial with temperature variations (Tang et al. 2015).

8.3.9 *FinFET Performance Under Various Design Strategies*

Designers varied the source and drain junction placement, punch-through stop implant and gate work function to investigate the new design approaches for 10-nm FinFET technology to satisfy low power and extremely low power requirements and to know the impact of I_{OFF}, gate capacitance, transconductance and intrinsic frequency (Walke et al. 2017). Research extraction and analysis of external resistance have become important in modern CMOS technology. By adding some assumptions in shift-and-ratio methods, it can be explored for use in short channel devices and also find application in FinFET devices (Zhang et al. 2018). A transistor with reduced size and fin gate has led to important change and add a set of constructive layout design rules. Additional layers and 3D structure of FinFET changed the parameters of a parasitic element, so a comparative analysis of 28-nm planar and 7-nm FinFET CMOS is performed (Ilin et al. 2018). A FinFET with a modified drain extension exhibits a better analog and radio frequency (RF) behaviors. We can boost the cutoff frequency of power FinFET from 30 to 53 GHz by changing the drain extension from narrow fin to a planar layout. Researchers investigated the analog and radio frequency parameters of power FinFETs with diverse drain extension structures for microwave applications.

Researchers replace the bipolar junction transistor diodes with FinFET diodes in some cases and evaluate the device output without degradation. Minimum voltage headroom and less power dissipation are two benefits of using the FinFET diodes in subthreshold operation (Prilenski and Mukund 2018). New self-aligned double-gate silicon on insulator (SOI) structure FinFET is proposed as a nano-MOS device. This proposed structure suppresses SCE, even with 17-nm gate length, provides a proper V_T for ultra-thin body and reduces the parasitic resistance (Hisamoto et al. 2000).

The author has explored the FinFET's best suitability for low-power applications in very short gate-length future technologies (Rosner 2003). This paper shows that the proposed FinFETs offer low-power output for the state-of-the-art bulk MOSFETs, even with relaxed gate oxide thickness. A new method of estimating the leakage is being studied in Gu et al. (2008), and the results show that the effect of the quantization of the width on the estimate of the statistical leakage is important for FinFET devices. This approach can reliably determine the statistical characteristics of the leakage current under process variation.

Designers often try to create an innovative design and structures to remove the disadvantages related to FinFET including gate buckling, fin bottom erosion, structural instability and less uniformity between fin shapes. Inverted T (IT) FinFET is an innovative design that can be used to increase a drive current with limited size (Yu 2002; Mathew 2005). IT FinFET is more beneficial than SOI FinFET because it requires wider fin width and less fin height as compared to SOI FinFET. IT FinFET is a mechanically stable structure and reduces the random dopant fluctuation and fin bottom erosion, but suffers from high OFF state current. Fin width and ultra-thin body height parameters can be used to optimize the performance of the IT FinFET, and outcomes manifest that fin width should be less than 10 nm for better immunity against SCE (Yu et al. 2018).

In the new era of VLSI technology, the compact size of devices is the primary requirement and maintaining the good performance of devices with compact size is one of the biggest challenges for research designers. Nowadays, FinFET is the most promising transistor and it is the most competent device to substitute the MOS transistors because of its outstanding controllability of the SCE, great insulation, high driving efficiency and reduced leakage current for both high-speed and low-power applications. But, some scaling challenges faced by FinFET devices and improvement are required for the betterment of VLSI technology. The impact of PVT variation is mainly on the nanotechnologies and degrades the performance of FinFET, so relevant methods and techniques are needed to improve the FinFET technology.

8.4 Results and Discussion

With the advancement of technology, further scaling of MOS transistors is a challenging task for research designers. FinFET is one of the best alternatives to be used for the scaling process. The main reason for FinFET's success is its excellent SCE controllability compared to a conventional planar system. The fin like geometry of FinFETs, where the regions of depletion enter the body region from the gates, indicates that there are no free charge carriers available, making it possible to suppress SCE. Furthermore, FinFET technology dominates because it offers great isolation, less current leakage and higher driving capability.

Nonetheless, FinFET technologies face many scaling challenges. For example, fin engineering (channel length, fine thickness, oxide thickness and balancing height) is important to minimize I_{OFF} and maximize I_{ON}. PVT variation also exacerbates circuit

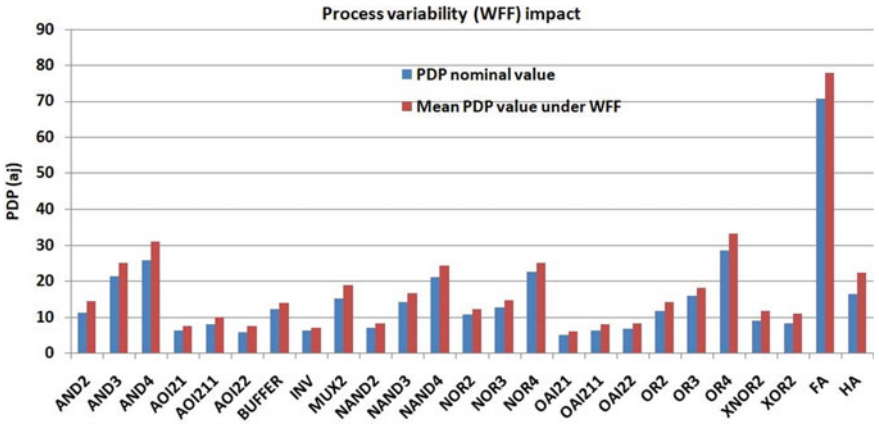

Fig. 8.6 Nominal PDP outcomes for standard cell gates under the WFF compared to mean values

degradation which makes the circuit inadequate for its initial purpose. A PVT variation causes a severe effect on the delay, leakage and performance of FinFET devices. Any variations in temperature affect the leakage current that leads to increases in energy–delay product (EDP) by up to 4X and 7X for full VDD operation and near-threshold voltage schemes, respectively (Turi and Delgado-Frias 2017). Researchers studied the 8T FinFET SRAM cell that reveals there are up to 42% of variations in EDP due to supply voltage variation. Temperature variability influences leakage current and the increase of up to 32X, and from the literature we noticed that a low-power inverter scheme is the highest rated 8T FinFET SRAM scheme (Turi and Delgado-Frias 2017). Fabrication of FinFET is a critical step for improvement in the performance of the device in deep submicron regime. Small variations during fabrication completely alter the circuit behavior, so we can conclude that nanoscale devices are becoming very sensitive to process variations. Figure 8.6 shows nominal PDP outcomes for standard cell gates under the WFF compared to mean values.

AND4, half adder and full adder standard cells exhibit more sensitivity due to WFF variations and show deviations of 19.76, 10.33 and 35.36% above the nominal PDP value, respectively. INV, NAND2 and AOI21 standard cells are less sensitive to WFF deviations. Figure 8.7 indicates the differences in power, PDP and timing due to voltage fluctuations (Zimpeck et al. 2015). Supply voltage variations play a very crucial part in the performance of FinFET. Figure 8.7 shows the total power, timing and PDP values for a voltage range from 0.9 to 0.3 V.

NAND4, AND4 and NOR3 standard cells show about 70% of PDP reduction by using FinFET devices. The main drawback of voltage variations is timing violations. The total power consumption parameter is mainly affected by temperature variations that can increase power consumption 5X higher than the nominal value in case of high temperature (Zimpeck et al. 2015). We can examine that WFF can considerably influence leakage current of the FinFET from the above results.

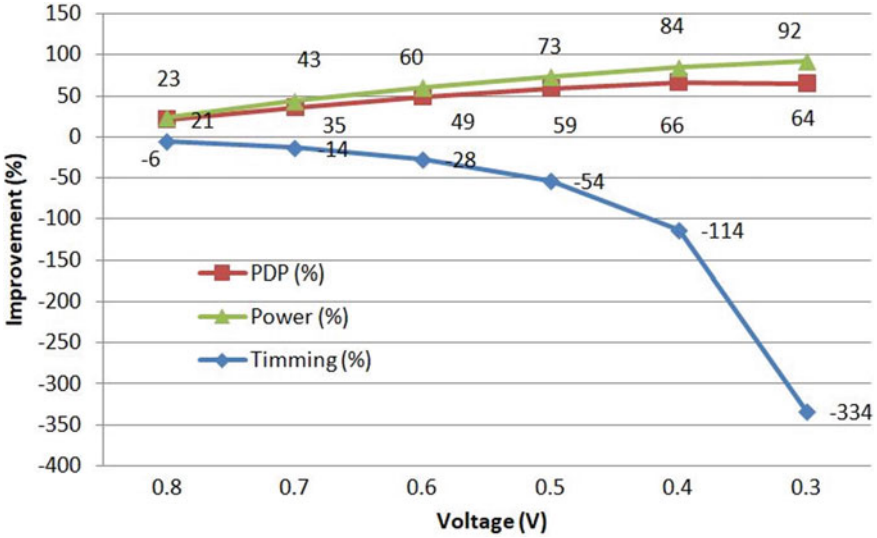

Fig. 8.7 Differences in timing, power and PDP due to voltage fluctuations

Diverse transistor arrangements for the similar logic function can reveal the different electrical and physical characteristics under PVT variations. To mitigate the impact of PVT variations, complex cells can be implemented in various transistor arrangements that can provide the most suitable topology for evaluation. Different transistor arrangements show a distinct impact on gate variability and concluded that far topology is best for OAI211 and OAI221 complex gates (Zimpeck et al. 2018). PDP determines the impact of process variability on complex cell by evaluating the delay and power of various circuits under the influence of WFF variations. Close arrangement is better for remaining complex gate. Far topology having three or more inputs provides better performance but causes the power penalty, i.e., increasing the power consumption mean value. Table 8.1 shows the mean and standard deviation of power consumption, worst-case delay and PDP (Zimpeck et al. 2018).

Impact of PVT variations on different transistor sizing techniques is also scrutinized in the previous literature in which transistor sizing techniques like optimized transistor sizing (OTS), logical effort (LE) and minimum transistor sizing (MTS) are largely utilized. LE-based technique cells exhibit the highest deviation in PDP. On the other hand, the OTS-based technique cells represent higher nominal values. Voltage variations mostly influence the OTS worst cases that cause maximum energy consumption. The impact of temperature variations is very less in OTS-based technique cells. LE technique shows the largest deviation. It is also important to consider environmental variation when choosing the appropriate approach for defining the correct transistor sizes for standard cell libraries, considering variability (Zimpeck et al. 2016).

Table 8.1 Mean and standard deviation of the power consumption, worst-case delay and PDP

Metrics	AOI21		OAI21		AOI211		OAI211		AOI221		OAI221	
	Close	Far	Close	Far	Close	Far	Close	Far	Close	Far	Close	Far
Delay (ps)	4.2	6.4	4.4	6.4	9.3	10	9.4	8	11.6	12	9.9	10.7
σ/μ (%)	34.3	33.8	32.7	33.4	33.6	34.3	31.6	35	35	35.6	34.4	32.2
Power (nW)	274.2	297.8	255.6	270.8	278.5	306.4	302.8	308	308	328.5	393.4	307.5
σ/μ (%)	24	22.1	26	24.2	27.8	25.4	29.7	27.3	28.9	27.3	31.2	29.8
PDP (a_j)	2.3	2.6	2.1	2.2	3.4	4	3	3.2	4.7	5.2	3.9	4.1
σ/μ (%)	27	26	26.7	27.8	29.7	28.1	30.5	31.4	30.3	28.2	31.8	31.4

The process variability will introduce a power deviation of up to 100 percent. RSNM shows about 20% variation under PV which is the worst case dramatically reduced cell noise robustness (Almeida et al. 2018). The author introduced FinFET CAM architecture focused on parasitic aware nature in Bhattacharya et al. (2015). All asymmetric gate work function shorted gate (ALL-ASG) bit cell was more superior to all shorted gate (ALL SG) and core ASG bit cells in terms of DC metrics. Leakage power assumes slightly greater significance with decreasing mismatch probability. When the BJT diode is replaced with FinFET diode, it shows the less voltage headroom and power dissipation (Prilenski and Mukund 2018). But, the biggest disadvantage of a FinFET diode is enlarged vulnerability to PV. The traditional method of estimating the leakage will greatly underrate the average leakage current by 43%, while the approach makes less error than 5% (Gu et al. 2008). The PV remains the main source of power and timing deviation in new technologies. CAD tools may play a significant role in assessing the impact of variability and reliability. Various tools like Cadence Virtuoso, Synopsys and ELDO simulator are the best way to implement any design philosophy (Alam 2008).

8.5 Conclusion

Scaling challenges of MOSFET technology such as SCE, an aging effect and a variability effect are becoming a barrier in the progress of VLSI technology; therefore, an appropriate alternative is the best way for evolution in VLSI technology. FinFET is the best option for substituting MOS technology because of better SCE controllability, lower leakage, perfect isolation and high driving capability. In this chapter, we outline various challenges faced by MOSFET technology and various factors which explicate the superiority of a FinFET as compared to MOS transistor. Researchers adopted various methodologies to mitigate the impact of PVT variations, but the

PVT variation is still a dominant factor in FinFET devices, especially in deep submicron regimes. Nowadays, for better performance of FinFET, various techniques are necessitated to mitigate the impact of PVT variations.

References

Alam M (2008) Reliability- and process-variation aware design of integrated circuits. Microelectron Reliab 48(8–9):1114–1122

Almeida RB, Marques CM, Butzen PF, Silva FRG, Reis RAL Meinhardt C (2018) Analysis of 6 T SRAM cell in sub-45 nm CMOS and FinFET technologies. Microelectron Reliab 88–90:196–202

Arasteh A, Moaiyeri MH, Taheri MR, Navi K, Bagherzadeh N (2018) An energy and area efficient 4:2 compressor based on FinFETs. Integration 60:224–231

Arulvani M, Mohamed Ismail M (2018) Low power FinFET content addressable memory design for 5G communication networks. Comput Electr Eng 72:606–613

Bagheriye L, Toofan S, Saeidi R, Moradi F (2018) Highly stable, low power FinFET SRAM cells with exploiting dynamic back-gate biasing. Integration. ISSN 0167-9260

Ban Y, Choi C, Shin H, Lee J, Kang Y, Paik W (2014) Analysis of dynamic voltage drop with PVT variation in FinFET designs. In: 2014 International SoC design conference (ISOCC), 2014

Bhattacharya D, Bhoj AN, Jha NK (2015) Design of efficient content addressable memories in high-performance FinFET technology. IEEE Trans Very Large Scale Integr (VLSI) Syst 23(5):963–967

Chen B, Chen K, Chiu C, Huang G, Chen H, Chen C, Hsueh F, Chang EY (2018) Analog and RF characteristics of power FinFET transistors with different drain-extension designs. IEEE Trans Electron Devices 65(10):4225–4231

Colinge J-P (2008) The SOI MOSFET: from single gate to multigate. In: FinFETs and other multi-gate transistors. Springer, US, pp 1–48

Ezz-Eldin R, El-Moursy MA, Hamed HFA (2015) Analysis and design of networks-on-chip under high process variation. Springer International Publishing, 2015 [Online]. Available: http://dx.doi.org/10.1007/978-3-319-25766-2

Gu J, Keane J, Sapatnekar S, Kim CH (2008) Statistical leakage estimation of double gate FinFET devices considering the width quantization property. IEEE Trans Very Large Scale Integr (VLSI) Syst 16(2):206–209

Gupta A, Mathur R, Nizamuddin M (2019) Design, simulation and comparative analysis of a novel FinFET based astable multivibrator. Int J Electron Commun 100:163–171

Hisamoto D, Lee W-C, Kedzierski J, Takeuchi H, Asano K, Kuo C, Anderson E, King T-J, Bokor J, Hu C (2000) FinFET-a self-aligned double-gate MOSFET scalable to 20 nm. IEEE Trans Electron Devices 47(12):2320–2325

Ilin S, Ryzhova D, Korshunov A (2018) Comparative analysis of standard cells performance for 7 nm FinFET and 28 nm CMOS technologies with considering for parasitic elements. In: 2018 IEEE conference of Russian Young researchers in electrical and electronic engineering (EIConRus), Moscow, 2018, pp 1360–1363

Islam A, Hasan M (2012) A technique to mitigate impact of process, voltage and temperature variations on design metrics of SRAM Cell. Microelectron Reliab 52(2):405–411

Jacob AP, Xie R, Sung MG, Liebmann L, Lee RTP, Taylor B (2017) Scaling challenges for advanced CMOS devices. Int J High Speed Electron Syst 26(01n02):1740001

Khalid U, Mastrandrea A, Olivieri M (2015) Effect of NBTI/PBTI aging and process variations on write failures in MOSFET and FinFET flip-flops. Microelectron Reliab 55(12):2614–2626

Khoshavi N, Ashraf RA, DeMara RF, Kiamehr S, Oboril F, Tahoori MB (2017) Contemporary CMOS aging mitigation techniques: survey, taxonomy, and methods. Integration 59:10–22

Kushwah CB, Vishvakarma SK, Dwivedi D (2016) A 20 nm robust single-ended boost-less 7T FinFET sub-threshold SRAM cell under process–voltage–temperature variations. Microelectron J 51:75–88

Lee C-Y, Jha NK (2014) FinCANON: a PVT-aware integrated delay and power modeling framework for FinFET-based caches and on-chip networks. IEEE Trans Very Large Scale Integr (VLSI) Syst 22(5):1150–1163

Lee C-W et al (2010) Performance estimation of junctionless multigate transistors. Solid-State Electron 54(2):97–103

Mahapatra S et al (2013) A comparative study of different physics-based NBTI models. IEEE Trans Electron Devices 60(3):901–916

Mathew L et al (2005) Inverted T channel FET (ITFET)—fabrication and characteristics of vertical-horizontal thin body multi-gate multi-orientation devices ITFET SRAM bit-cell operation. A novel technology for 45 nm and beyond CMOS. In IEDM technical digest, Washington, DC, USA, pp 713–716

Mukhopadhyay S, Lee Y-H, Lee J-H (2018) Time-zero-variability and BTI impact on advanced FinFET device and circuit reliability. Microelectron Reliab 81:226–231

Pal S, Bhattacharya A, Islam A (2014) Comparative study of CMOS- and FinFET-based 10T SRAM cell in subthreshold regime. In: 2014 IEEE international conference on advanced communications, control and computing technologies, 2014

Pham D, Larson L, Yang J-W (2006) FINFET device junction formation challenges. In: 2006 international workshop on junction technology, 2006

Prilenski L, Mukund PR (2018) A sub 1-volt subthreshold bandgap reference at the 14 nm FinFET node. Microelectron J 79:17–23

Rosner W et al (2003) Nanoscale finFETs for low power applications. Int Semicond Device Res Symp

Sharma VK, Pattanaik M (2014a) Techniques for low leakage nanoscale VLSI circuits: a comparative study. J Circuits, Syst Comput 23(5):1450061

Sharma VK, Pattanaik M (2014b) Process, voltage and temperature variations aware low leakage approach for nanoscale CMOS circuits. J Low Power Electron 10(1):45–52

Sinha S, Yeric G, Chandra G, Cline B, Cao Y (2012) Exploring sub-20 nm FinFET design with predictive technology models. In: Proceedings of the 49th annual design automation conference on—DAC'12, 2012

Sneha G, Krishna BH, Kumar CA (2017) Design of 7T FinFET based SRAM cell design for nanometer regime. In: 2017 International conference on inventive systems and control (ICISC), 2017

Taghipour S, Asli RN (2017) Aging comparative analysis of high-performance FinFET and CMOS flip-flops. Microelectron Reliab 69:52–59

Tang A, Yang Y, Lee C, Jha NK (2015) McPAT-PVT: delay and power modeling framework for FinFET processor architectures under PVT variations. IEEE Trans Very Large Scale Integr (VLSI) Systems 23(9):1616–1627

Tawfik SA, Kursun V (2008) Portfolio of FinFET memories: innovative techniques for an emerging technology. In: 2008 international SoC design conference, 2008

Tawfik SA, Liu Z, Kursun V (2007) Independent-gate and tied-gate FinFET SRAM circuits: design guidelines for reduced area and enhanced stability. In: 2007 International conference on microelectronics, 2007

Turi MA, Delgado-Frias JG (2017) Full-VDD and near-threshold performance of 8T FinFET SRAM cells. Integration 57:169–183

Upasani DE, Shrote SB, Deshpande PS (2010) Standby leakage reduction in nanoscale CMOS VLSI circuits. Int J Comput Appl 7(5)

Walke A, Schlenvogt G, Kurinec S (2017) Design strategies for ultra-low power 10 nm FinFETs. Solid-State Electron 136:75–80

Yang Y, Jha NK (2013) Fin Prin: analysis and optimization of FinFET logic circuits under PVT variations. In: 2013 26th international conference on VLSI design and 2013 12th international conference on embedded systems, 2013

Yang Y, Jha NK (2014) FinPrin: FinFET logic circuit analysis and optimization under PVT variations. IEEE Trans Very Large Scale Integr (VLSI) Syst 22(12):2462–2475

Yeh W, Zhang W, Chen P, Yang Y (2018) The impact of fin number on device performance and reliability for multi-fin tri-gate n- and p-type FinFET. IEEE Trans Device Mater Reliab 18(4):555–560

Yu B (2002) Fabrication of a field effect transistor with an upside down T-shaped semiconductor pillar in SOI technology

Yu E, Heo K, Cho S (2018) Characterization and optimization of inverted-T FinFET under nanoscale dimensions. IEEE Trans Electron Devices 65(8):3521–3527

Zhang C, Liu Z, Miao X, Yamashita T (2018) FinFET external resistance analysis by extended shift-and-ratio method. IEEE Trans Electron Devices 65(8):3127–3130

Zimpeck AL, Meinhardt C, da Luz Reis RA (2015) Impact of PVT variability on 20 nm FinFET standard cells. Microelectron Reliab 55:1379–1383

Zimpeck AL, Meinhardt C, Posser G, Reis R (2016) FinFET cells with different transistor sizing techniques against PVT variations. In: 2016 IEEE international symposium on circuits and systems (ISCAS), Montreal, QC, pp 45–48

Zimpeck AL, Meinhardt C, Artola L, Hubert G, Kastensmidt FL, Reis RAL (2018) Impact of different transistor arrangements on gate variability. Microelectron Reliab 88–90:111–115