A New Current Mode Multiplier Using Single CCCII Without Passive Components

Syed Zahiruddin, Avireni Srinivasulu, and Musala Sarada

Abstract A current mode multiplier is a valid structured block in many signal processing operations, such as modulation and demodulation schemes in communications, in development of bio-medical equipments, in analog computations, and fuzzy logic controllers. A single second generation current controlled conveyor (CCCII) based current mode multiplier without passive components is designed. CCCII has the eccentricity of intrinsic resistance in between the two input ports which are tunable by the external bias current. PSPICE simulator is utilized to examine the proposed design. The topology yields a simple structure and highly suitable for monolithic IC fabrication. Simulation results are confirmed with a voltage requirement of ± 2.5 V, the non linearities, total harmonic distortion (THD), and power dissipation are anticipated. Comparison of the proposed design with the existing methods is also performed. The parametric sweep and temperature analysis are also determined. The simulated results very well agree with the theoretical expectancy.

Keywords Multiplier · Current conveyor · CCCII · Total harmonic distortion · Parametric sweep

1 Introduction

Analog multipliers ascertain in various fields like signal processing, communication systems, instrumentation, and measurement systems. Several multiplier configurations are proposed previously using translinear bipolar transistors, MOS square law

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characteristics, and switching capacitors. However, they are bounded to voltage mode operations and therefore not suitable for current mode. The current mode designs have several advantages such as large dynamic range, greater linearity, large signal bandwidth, simple configuration, and low power consumption [1–8].

In contemporary world, the analog VLSI has arised as a exceptional technology for the imminent demands of large bandwidth and less power requisites. A number of multiplier topologies as such is designed based on voltage mode. The eminent fact is that the dynamic range of voltage dependent devices is uttered by the frequency dependent gain. This glitch can also be elucidated by the current mode devices. Many voltage mode and current mode multipliers based on different active building modules have been proposed in the literature, but they involve two or more active devices, having the drawback of large area constraint and dissipation of more power. Abuelma'atti [2] has developed the current mode multiplier design possessing two CCCIIs without external passive components. The configuration proposed by Erkan Yuce [3] implies a single CCCII for realization along with a current controlled grounded resistor (CCGR), which is then realized with four-bipolar junction transistors (BJTs). Many such techniques using various active devices exist in the literature that uses operational transconductance amplifier (OTA), current controlled current differencing buffered amplifier (CCCDBA), current differencing transconductance amplifier (CDTA), current controlled current differencing transconductance amplifier (CCCDTA), current follower transconductance amplifier (CFTA), current controlled current conveyor transconductance amplifier (CCCCTA), digitally programmable current conveyor (DPCCII) [9–19]. In this manuscript, current mode CCCII-based multiplier utilizing only one CCCII without passive components is proposed with two input current signals and one controllable bias current. Compared with the existing current mode multipliers, the main advantage of the proposed topology is that it occupies less area and low power dissipation because of having only one CCCII with no passive components for realization.

2 Second Generation Current Controlled Conveyor

Basically, CCCII is a mixed translinear loop, current mode active structured block for several analog applications. It has the additional advantage of intrinsic resistance (R_B) that can be observed at input terminal X that can be varied by tuning the external bias current and thus avoids the usage of external resistor which is more preferred for IC fabrication.

The matrix relationship between input and output currents, by considering the intrinsic resistance R_B into account of an basic CCCII is given in matrix form (1).

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_B & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{1}$$

Conventionally, using (1), the plus and minus sign signify the direction of current between input port X and output port Z. If the direction of current is same, then it is a positive current conveyor (CCCII+). If the direction of current is in opposite direction, then it is a negative current conveyor (CCCII-). At port X, R_B denotes the input intrinsic resistance, tuned with bias current, ($R_B = V_T/2I_B$), where $V_T \approx 26$ mV is the voltage equivalent of temperature, and $I_B \geq 0$ is the external bias current of the CCCII. At node Y, the current I_Y is zero since the impedance at the input of node Y is infinite. Therefore, the current applied at input node X is transformed to output node Z.

Several applications and other methods of realizing a multiplier topology are available by applying bias current to the CCCII [9–14]. Figure 1 shows the symbolic depiction of CCCII.

Transistor model of CCCII is shown in Fig. 2 in which the translinear loop is realized using bipolar junction transistors to achieve a wide frequency range. The transistor loop (M_1–M_4) forms a mixed translinear, DC biased by means of current mirrors (M_5–M_6, and M_9–M_{10}). The transistors (M_{11}–M_{12}, and M_{13}–M_{14}) are helpful to produce output current $Z+$ in response to the X terminal input current. The output Z- terminal is realized using additional current mirrors (M_{15}–M_{17}, and M_{18}–M_{20}), and the transconductance gain can be varied by I_B.

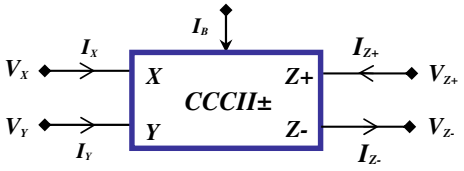

Fig. 1 Symbolic representation of the CCCII±

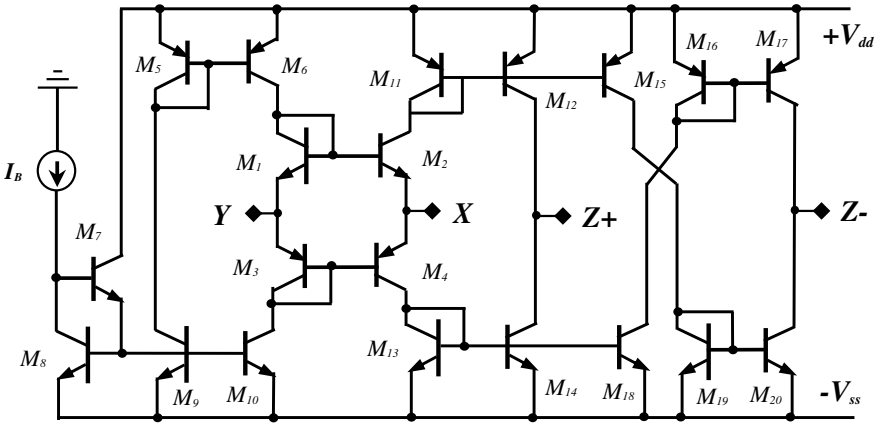

Fig. 2 Internal structure of CCCII±

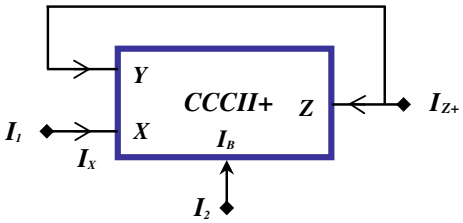

Fig. 3 Proposed multiplier circuit using CCCII

3 Proposed Current Mode Multiplier

The work is organized to design a new current-based multiplier using a single CCCII, with no passive components and has various applications in current mode signal processing circuits. The proposed design of Fig. 3 can multiply two current signals and is able to operate at a broad range of frequencies. The design is insensible to temperature variations, and the output current (I_Z) can be inhibited by varying the input bias current. The main advantage of the developed circuit is that it uses only one CCCII for construction which ultimately requires less area and low power. The internal structure of CCCII is as shown in Fig. 2.

Using routine design analysis for the multiplier configuration of Fig. 3, the simplified output current expression is:

$$I_Z(t) = \frac{I_1(t) \times I_2(t)}{I_B} \tag{2}$$

Considering non-idealities, the above expression is denoted by

$$I_Z(t) = \frac{\alpha_0 \times \beta_0 \times I_1(t) \times I_2(t)}{I_B} \tag{3}$$

where α_0 is the DC gain with current tracking error, and β_0 is the voltage gain with voltage tracking error, which are ideally equal to unity.

4 Simulation Results

The proposed design of Fig. 3 has been simulated by using PSPICE simulator. Figure 4 shows the simulated results with the specifications shown as under. The CCCII was realized by the transistor schematic shown in Fig. 2; PR100N for PNP and NP100N for NPN transistors of bipolar group ALA400 of AT and T are utilized. The supply voltage is $\pm V_{cc} = 2.5$ V, and the value of bias current is $I_B = 50$ μA ($R_X = 260\ \Omega$). The input signal frequencies are $I_1 = 10$ Sin $(2 \times \pi \times 10 \times 10^3 t)$ μA and $I_2 = 10$ Sin $(2 \times \pi \times 100 \times 10^3 t)$ μA. The total harmonic distortion (*THD*) of the proposed multiplier circuit is 1.876%, and the total power dissipation is 3.74 mW.

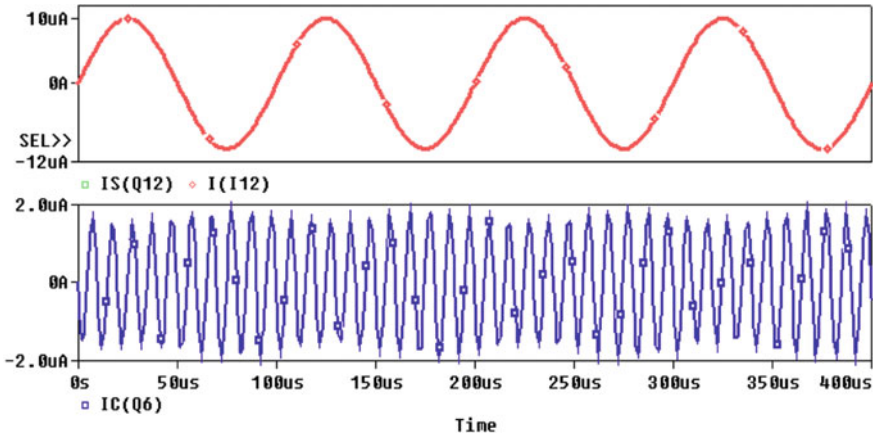

Fig. 4 The simulated outcome of Fig. 3 represents the multiplication of two sinusoidal currents

The harmonic distortion and power dissipation values are quite low and reasonably good.

Figure 5 is the frequency spectrum of the proposed design, and Fig. 6 shows the variation of bias current versus the output current; the input signal frequencies are $I_1 = 10$ Sin $(2 \times \pi \times 10 \times 10^3 t)$ μA, and $I_2 = 10$ Sin $(2 \times \pi \times 100 \times 10^3 t)$ μA are preserved constant. The graph imitates the closeness of theoretical and simulated results for the variation of bias current over a range of 50–250 μA.

Figure 7 is the graphical representation of total harmonic distortion versus the bias current. The bias current is varied over a range of 50–250 μA, and the observed distortion is in the range of 3.912×10^{-3} to 0.7824×10^{-3}. The THD is 1.876%, which is very low. Figures 8 and 9 are also the graphical interpretation confirming

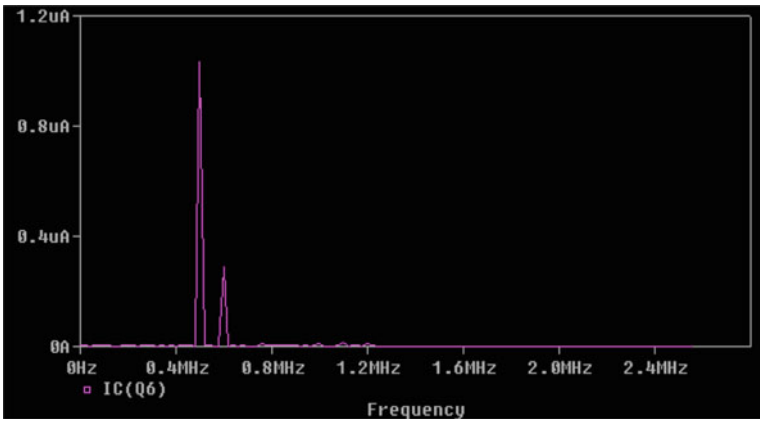

Fig. 5 Simulated output frequency spectrum of the proposed circuit

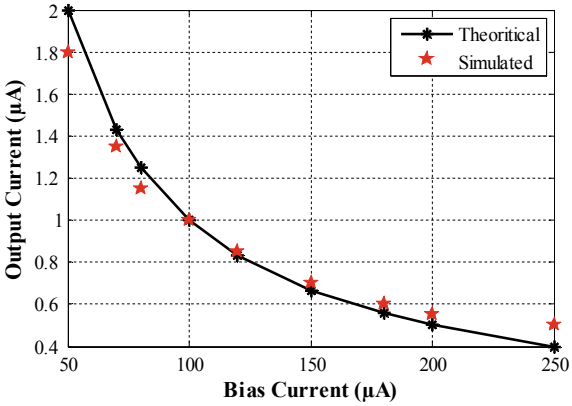

Fig. 6 The simulation results of output current versus bias current

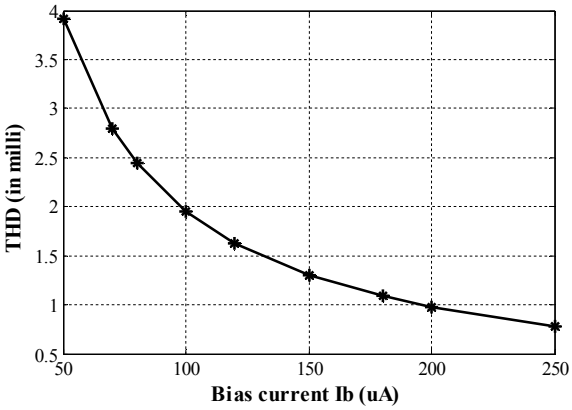

Fig. 7 Simulated outcome of the total harmonic distortion versus bias current

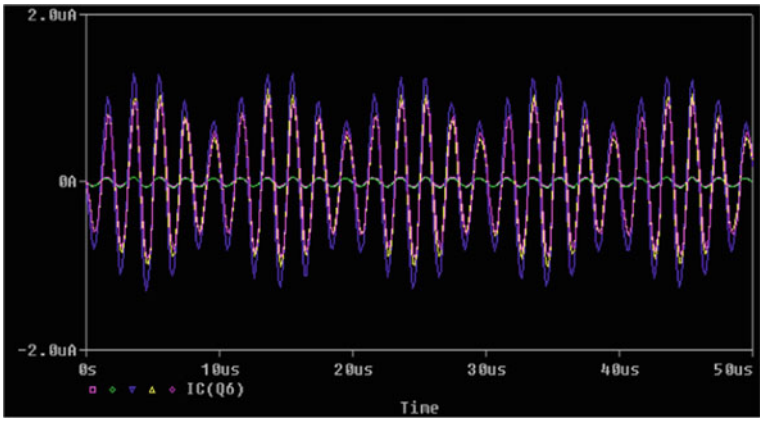

Fig. 8 Simulated outcome of the multiplier circuit for the variation of temperatures from 0 to 150 °C

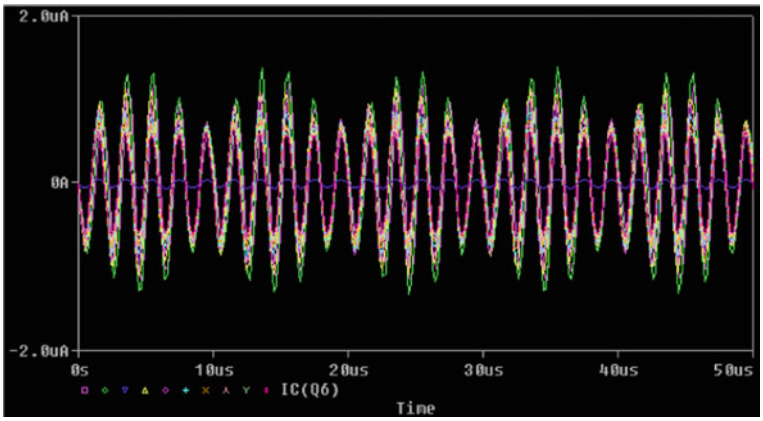

Fig. 9 Simulated outcome of the multiplier circuit showing the parametric sweep over the temperatures from 0 to 150 °C

the variation of amplitudes of output current over the variation of temperature from 0 °C to a maximum of 150 °C. It reflects the insensitiveness over the temperature variations, keeping the input signal frequencies $I_1 = 10\,\mu\text{A Sin}\,(2 \times \pi \times 10 \times 10^3\text{t})$, and $I_2 = 10\,\mu\text{A Sin}\,(2 \times \pi \times 100 \times 10^3\text{t})$ unaltered (Table 1).

The proposed multiplier employs a single CCCII with no passive components for the realization. The design of [3] consists of a single CCCII and one current controlled grounded resistor (CCGR), which is then realized with four BJTs and is able to produce a total harmonic distortion up to 5%. The design of [9] has been involved with 3 CCDDCCs along with a capacitor, and its distortion is 0.8% for a 0.6 V_{PP}. The configuration of [10] has the advantage of using a single CFCTA with no passive components, but suffers a distortion of 4% which is less preferred. Whereas the design of [12] has the advantage of having less distortion of 1.21%, but at a cost of 3 op-amps, 6 resistors, and 2 CMOS transistors for its construction. It requires 1 CDBA and 6 MOS transistors for the implementation of the design of

Table 1 Comparison of proposed method with the existing methods

Topology (ref.)	Number of active elements	Type of active element	Number of passive components	THD
[3]	1	CCCII	1 resistor	5%
[9]	3	CCDDCC	1 capacitor	0.8% within 0.6 Vpp
[10]	1	CFCTA	0	4%
[12]	3	OP-AMPs	6 resistors and 2 CMOS transistors	1.21%
[13]	1	CDBA	6 MOS transistors	NA
This work	1	CCCII	0	1.876%

[13]. Referring to all the above designs, the advantages of the proposed design are that it requires only one CCCII with no passive components and offers low distortion and also highly suitable for monolithic IC fabrication.

5 Conclusion

A current mode multiplier design is developed, having no capacitors or resistors involved which is suitable for IC fabrication. The total harmonic distortion and power dissipation are evaluated that are 1.876% and 3.74 mW, respectively. To improve the potency of the design, the non-linearity, frequency spectrum, and temperature insensitivity are determined. The simulation results for the variation of bias current with respect to the THD are verified and found satisfactory. The proposed design is compared with the existing methods and tabulated. Thus, the reported multiplier design has a simple structure that requires small area and dissipates low power over the other existing technologies.

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