Chapter 8
Direct Cu to Cu Bonding and Alternative Bonding Techniques in 3D Packaging

Tadatomo Suga, Ran He, George Vakanas, and Antonio La Manna

8.1 Introduction

Reliable, high-throughput, low-cost, low-temperature bonding processes have always been in high demand in industrial, electronics and semiconductor manufacturing. Multiple techniques and processes have been demonstrated in different domain applications, with distinct advantages and disadvantages that we will explore in this chapter. With the trend towards further device scaling and applications-driven roadmaps, three-dimensional (3D) integration has evolved with bandwidth, power, performance, and form factor advantages over planar, side-by-side, electronic packaging architecture. To enable 3D technology, high-density interconnects (sub-40 um pitch) and high-throughput and reliable stacking/bonding processes are required. Cu–Cu bonding is a promising candidate as a 3D interconnect method, since Cu is a well-studied and well-understood metallurgy for back-end-of-line (BEOL) layers and for through-silicon vias (TSVs). Cu also offers mechanical, electrical, and thermal advantages based on its material properties compared to aluminum, transition metals and noble metals. Comparing to solder-based pillar/bump processes with solder

T. Suga · R. He
The University of Tokyo, Tokyo, Japan

G. Vakanas (✉)
Intel Corporation, Santa Clara, CA, USA
e-mail: george.p.vakanas@intel.com

A. La Manna
IMEC, Louvain, Belgium

Y. Li and D. Goyal (eds.), *3D Microelectronic Packaging*,
Springer Series in Advanced Microelectronics 64,
https://doi.org/10.1007/978-981-15-7090-2_8

reflow or thermo-compression bonding (TCB) in the temperature range of 250–275 °C, the Cu–Cu bonding process should target lower temperature range (from room temperature to 250 °C).[1]

The study of Cu–Cu bonding as a method for interconnection started in universities around the world approximately in year 2000 [1, 2], soon after the announcement of Cu interconnects for integrated circuits by IBM in the late '90s. For high-density interconnects (HDI), Cu–Cu bonding has been demonstrated since 2006 by Morrow et al. [3] of Intel (with 5 × 5 μm^2 Cu pads) and by Suga's group [4] at the University of Tokyo (with ~3 μm diameter Cu pads) respectively. For 3D stacking in case of extremely thinned dies with 10 μm pitch TSVs, bonding has been demonstrated also in 2006 by Swinnen et al. at IMEC [5]. Cu–Cu bonding for 3D prototypes such as memories, sensors, processors, and memory/processor stacks has been demonstrated by Intel [3] and Tezzaron [6]. Cu/SiO_2 hybrid bonding by Ziptronix[2] has also been demonstrated in a 3D stacking configuration by Fermilab [7, 8], Sony [9], and Tezzaron/Novati.

In summary, in this chapter, we introduce the pros and cons of Cu–Cu bonding and stacking/bonding schemes for different applications. We review various methods of Cu–Cu bonding: (a) thermo-compression bonding (an example of diffusion bonding), (b) Cu–Cu bonding with passivation capping layers, (c) surface activated bonding (SAB), and (d) alternative bonding methods (e.g. Cu/dielectric hybrid and Cu–Cu insertion bonding). We also discuss the effects of surface activation, surface microstructures, surface characteristics, and surface passivation for Cu–Cu bonding to understand how bonding behavior depends on Cu surface cleanness, diffusion, temperature, compression pressure, and bonding atmosphere. Lastly, we summarize the state-of-the-art and recommendations for future directions.

8.2 Solder-Based versus Solder-Less Bonding: Pros and Cons

Solder-based bonding is prevalent in 3D interconnects usually employing one-sided scheme of solder microbump (e.g. Cu/x/solder, where x would be a diffusion barrier like Ni (or no barrier at all) and solder would be SnAg, SnCu or other binary solder (e.g. typically electroplated) bonded on metal pad (e.g. Cu with a passivation layer or other capping layer, or pre-cleaned/pre-treated to prevent/remove oxidation). The key advantages of solder-based schemes are process robustness given that

[1] Process times targets depend on stacking process e.g. chip-on-chip (CoC), chip-on-wafer (CoW) or wafer-on-wafer (WoW) processes, equipment configuration and manufacturing embodiment and resulting throughput and Model of Record (MoR). For Cu–Cu process to be adopted in high-volume manufacturing (HVM), higher throughput and lower cost is required compared to established (and depreciated) solder-based processes.

[2] Acquired by Tessera, now consolidated in Xperi and TiVo merger end of 2019.

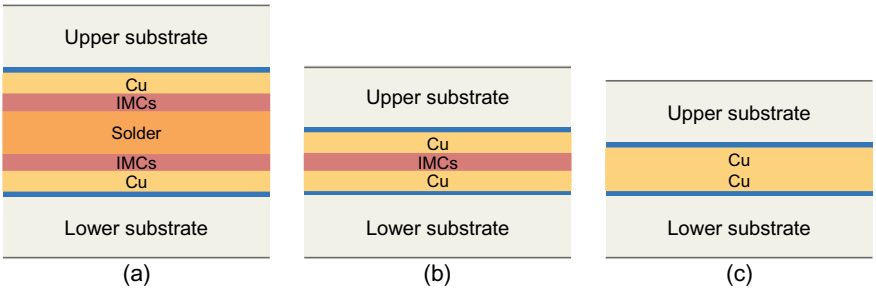

Fig. 8.1 Schematic diagram of the bonded structures using (**a**) soldering, (**b**) SLID/SSID bonding, and (**c**) Cu–Cu bonding methods

solder is malleable and more forgiving in terms of bump height uniformity and coplanarity. However, a solder-based process is time-consuming, more costly, due to the additional material stack up (usually involving photoresist, lithographic exposure and development, plating, etch and clean/strip processes). Moreover, a solder-based process is more prone to mechanical damage of solder bumps (e.g. scratching due to lower hardness) in handling/friction/shipping situations. Also, the process temperatures for solder-based processes are driven by the melting point of the solder (for instance, 232 °C for 100% Sn and ~221 °C for eutectic SnAg). Solder-based bonding forms intermetallic compounds (IMC's) and results in an IMC/solder/IMC structure, as shown in Fig. 8.1a. By controlling the thickness of the solder, bonding can be achieved through solid-liquid interdiffusion (SLID) bonding or solid-state interdiffusion (SSID) bonding reactions between Cu and solder, consuming all the solder and forming IMC's at the bonding interface, as shown in Fig. 8.1b. Comparing to the conventional solder reflow and SLID bonding, SSID bonding is performed at lower temperatures (below the melting point of solder) but under higher bonding pressures (~50–150 MPa).

Solder-based bonding limits the electrical conductivity, reliability (since cracks are prone to occur at solder-IMCs interface or inside IMCs), and the minimum pitch of interconnects. Direct Cu–Cu bonding without use of solder and formation of IMC's at the bonding interface, as shown in Fig. 8.1c, has been developed to solve these concerns. Comparing to other direct metal bonding such as Al–Al bonding, Cu–Cu bonding interconnects exhibit higher electrical conductivity, lower power consumption, lower resistive-capacitive (RC) delay, and higher electromigration resistance. In addition, Cu interconnects also provide excellent heat dissipation and thermomechanical reliability, which meets requirements of a number of key applications such as power electronics with an operation temperature as high as 250 °C [10].

Thus, solder-less, Cu–Cu bonding technology has the prospects to simplify processing, lower costs, and result in higher reliability and performance than solder-based bonding. A main challenge of Cu–Cu bonding is that Cu surface is readily oxidized by O_2 and H_2O during exposure to air, and the resulting thick (>10 nm) Cu oxides (CuO and Cu_2O) prevent bonding formation at below 300 °C. Unlike

Al oxide, Cu oxide growth is not self-limiting, hence grows thicker than traditional Aluminum oxide and requires cleaning treatment to generate pristine Cu surfaces suitable for bonding. Depending on the bonding environment (vacuum, inert, reducing, or ambient atmosphere), surface preparation and passivation, and handling of warpage and flatness, Cu–Cu bonding processes have been demonstrated at temperatures lower than the usual lead-free solder melting temperatures, down to 100–150 °C range with some demonstrations also down to room temperature. Variants of the Cu–Cu bonding processes include: thermo-compression bonding (an example of diffusion bonding), surface activated bonding (SAB), Cu–Cu bonding with assist processes (surface cleaning, treatment, and passivation with noble and non-noble capping layers), and hybrid bonding and insertion bonding. We will revisit such process conditions in more details in subsequent sections of this chapter.

8.3 Stacking and Bonding Schemes, Technologies and Applications

Stacking and bonding schemes and technologies are classified based on the form factor of bonding surfaces, the geometry and topology of the active electronic devices and packages and target applications. With respect to form factor, processes are distinguished as chip-on-chip (CoC), chip-on-wafer (CoW) or wafer-on-wafer (WoW). Benefits of the CoC and CoW bonding schemes include use of known-good-dies (KGD's[3]) for high yield and integration of chips of different sizes with high flexibility. However, the disadvantages are low throughput (especially CoC) and low alignment accuracy. WoW enables high throughput and high alignment accuracy, however it suffers from yield loss ("fall out") due to lack of KGD's and inflexibility with different sizes of stacked layers. To solve these drawbacks, multi-CoW bonding has been developed for bonding of multiple chips temporary assembled on a carrier wafer (e.g., through liquid-assisted self-assembly [11]) onto a wafer.

Bonding schemes can also be distinguished based on how the active surfaces (having devices) are brought into contact, e.g. face-to-face (F2F), and back-to-face (B2F) or face-to-back (F2B) and back-to-back (B2B). The face side refers to the front side of wafers where active devices are fabricated; backside refers to the opposite side of the face side and is usually obtained after thinning and insulation/metallization. In case of passive silicon interposer that has no active devices, the surface processed first is commonly termed as face side and the opposite as backside. F2F bonding uses Cu pads on the top metal layer above the active devices, and wafers are brought into contact between the face sides of both wafers, as illustrated in Fig. 8.2a. F2F bonding is widely used for two-layer 3D stacking. Morrow et al. [3] at Intel employed F2F bonding for 3D stacking of wafers having active devices such as 65-nm MOSFETs and 4-MB SRAMs using Cu bonding pads with size ranging between 5 μm $\times$ 5 μm and 6 μm $\times$ 40 μm. Subsequently, one of the F2F bonded wafers can be thinned

[3] Pre-tested and sorted chips, hence the nomenclature: "known good dies" (KGD's)

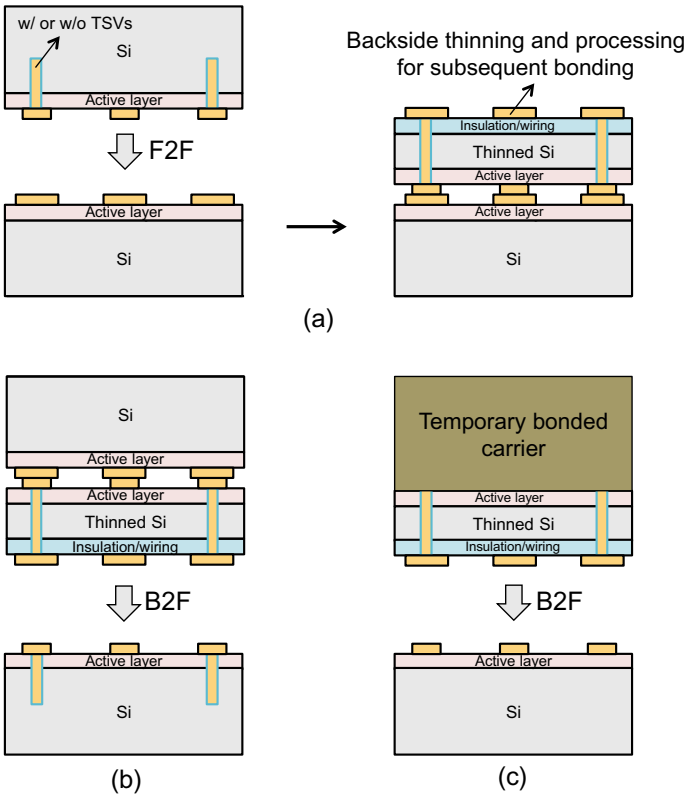

Fig. 8.2 Stacking schemes: (**a**) F2F before wafer backside processing, (**b**) B2F for bonding of third layer, and (**c**) B2F with temporary bonding

and processed for insulation/metallization from the backside for a follow-up bonding process through either B2F or B2B bonding schemes. The B2F bonding brings wafers into contact between the backside and face side of the two wafers, as illustrated in Fig. 8.2b; the B2B bonding brings wafers into contact between backsides. A wafer can also be thinned and backside processed with the help of temporary bonded carrier before B2F bonding, as illustrated in Fig. 8.2c, or B2B bonding. The B2F and B2B bonding is usually used for 3D stacking of more than two layers together with the F2F bonding.

8.4 Thermo-Compression Bonding (Example of Diffusion Bonding)—Material Fundamentals and Microstructure Effects

The basis of Cu–Cu thermo-compression bonding (TCB) is inter-diffusion and self-diffusion at elevated temperatures and under an external compression, depending on the cleanness of the mating Cu surfaces and potentially additional passivation or capping layers. The compression pressure, which is mainly dependent on the surface topography and roughness, can be in order of 100–150 MPa for as-plated Cu films/pillars, and <2.5 MPa for thin smooth Cu films or CMP (Chemical-Mechanical Polishing) polished Cu films. Typically, Cu–Cu TCB is performed at 300–400 °C in vacuum or protecting/reducing gas environment (or preceded by plasma clean), followed by a post-bonding annealing at 300–400 °C to improve the bond strength [12]. However, such high process temperatures and high heating/cooling rates may cause large thermal expansion and stress, which degrade or even damage thermal- and stress-sensitive materials and devices. Moreover, formation of interfacial voids were observed when bonding temperature is higher than 300 °C [13].

In order to lower the bonding temperature, surface treatments such as wet chemical cleaning and gas/vapor-phase thermal treatments have been researched and employed. For instance, forming gas (H_2 + Ar or N_2) treatment has been studied for Cu–Cu bonding at below 200 °C. After treatment at 175 °C for 30 min, wafers were bonded with thermo-compression at 175 °C for 30 min followed by 200 °C 1 h annealing [14, 15]. W. Yang et al. [16, 17] at the University of Tokyo studied Cu–Cu bonding by using formic acid (HCOOH) vapor treatment combined with Pt-catalyzed dehydrogenation for in situ generation of hydrogen (H) radicals/molecules. In this combined process, H radicals/molecules are generated by heating Pt foils exposed to HCOOH vapor through the following reaction.

$$\mathrm{HCOOH} \xrightarrow{\mathrm{Pt}} \mathrm{CO_2} + 2\mathrm{H} \tag{8.1}$$

The generation of H contained in the HCOOH vapor was confirmed by ex situ gas chromatography analysis [16]. The detected H_2 peak area was almost the same as standard 0.1% H_2 spectra. Compared to the forming gas, the H-containing HCOOH vapor appears to be more effective for Cu oxide reduction because of the presence of highly reactive H radicals, resulting in strong Cu–Cu bonding (shear strength of above 10 MPa) at 200 °C. As summarized in Table 8.1, comparing to the forming gas treatment, the HCOOH vapor treatment enables Cu–Cu bonding with very short treatment and bonding time and without the need of post-bonding annealing.

Most of the existing studies on Cu–Cu TCB were based on diffusion between randomly oriented Cu films. Diffusion, as known from materials fundamentals, is not only temperature-dependent but also microstructure-dependent. Cu–Cu bonding by using Cu layers that have special microstructures, such as Cu nanorod array [18], Cu particles [19], and highly (111)-oriented nano-twinned Cu films [20], has also been investigated in order to lower the bonding temperatures. Table 8.2 summarizes

Table 8.1 Thermal budget of Cu–Cu bonding by forming gas and formic acid vapor surface treatments

Process/references	Cu treatment (T, time)	Bonding and annealing (T, time)
Forming gas (H_2 + Ar or N_2) [14, 15]	175 °C 30 min	175 °C 30 min + 200 °C 1 h anneal
Formic acid vapor [16, 17]	200 °C 1–10 min	200 °C 5 min without annealing

Table 8.2 Cu surface diffusion coefficients on 3 crystal planes as function of temperature [20]

Temperature (°C)	Cu surface diffusivity, $D_{surface}$ (m^2/s)		
	(111)	(100)	(110)
150	6.85×10^{-10}	2.15×10^{-14}	6.61×10^{-16}
200	9.42×10^{-10}	1.19×10^{-13}	5.98×10^{-15}
250	1.22×10^{-9}	4.74×10^{-13}	3.56×10^{-14}
300	1.51×10^{-9}	1.48×10^{-12}	1.55×10^{-13}

data of Cu surface diffusion coefficients, $D_{surface}$ [m^2/s], on 3 crystal planes as a function of temperature in the range of 150–300 °C [20]. Because of the larger surface diffusivity on (111) plane than (100) and (110) planes, the Cu–Cu bonding temperatures can be reduced by using (111)-oriented Cu surfaces. Liu et al. [20] studied the Cu–Cu bonding of highly (111)-oriented nano-twinned Cu films and good bonding was obtained under thermo-compression at 150–250 °**C** for 10–60 min. Figure 8.3a presents TEM image of the cross-sectional Cu–Cu interface at 200 °**C** for 30 min, showing a void-free bonding interface. Figure 8.3b presents an electron backscattered diffraction (EBSD) orientation image of the bonding interface, showing all the Cu grains near the bonding interface were oriented in the < 111 > direction. The surface diffusion also occurs even at room temperature if the surfaces are free of oxides. Shimatsu et al. demonstrated Cu–Cu bonding between clean nanocrystalline Cu films in UHV (Ultra High Vacuum) immediately after sputtering deposition [21]. TEM result showed that the bonding interface become invisible, as shown in

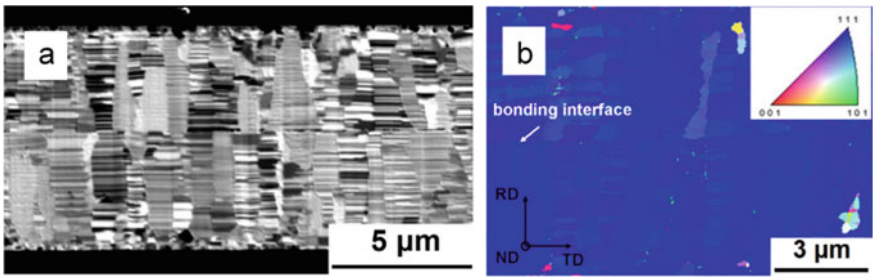

Fig. 8.3 Bonding between two electroplated (111)-oriented Cu films at 200 °C for 30 min: **a** TEM cross-sectional image and **b** electron backscattered diffraction (EBSD) orientation image [20]

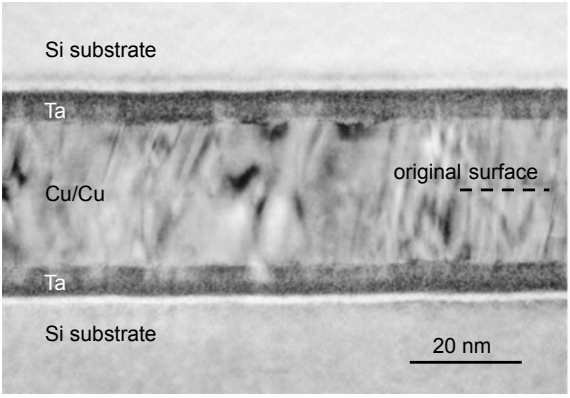

Fig. 8.4 TEM cross-sectional image of nanocrystalline Cu films bonded at room temperature in UHV immediately after sputter deposition. The original interface is invisible owing to Cu self-diffusion, indicating seamless bonding [21]

Fig. 8.4, which is attributed to the rapid Cu self-diffusion at room temperature. The Cu nanocrystalline thin films were also successfully bonded in air at temperature as low as 100 °C [22].

8.5 Passivation with Capping Layers: Self-assembling Monolayers (SAM's) and Metals

Since Cu is readily oxidized by O_2 and H_2O when exposed to air, Cu surface passivation with capping layers has been studied to protect Cu surfaces from oxidation and to improve the Cu–Cu bonding quality. Typical surface finishes such as electroless nickel/immersion gold (ENIG), immersion silver (ImAg), and immersion tin (ImSn), and organic solderability preservatives (OSP), were mainly developed for solder-based bonding. Researchers have also developed ENIG capping for solderless chip-to-substrate assembly by using thermo-compression at <200 °C and under ~300 MPa for 2.5D packaging [23]. This section will focus on emerging capping layers including organic self-assembled monolayers (SAM's) and metals such as sputtered Ti or Pd and electroless Ni- or Co-based alloys, as summarized in Table 8.3.

SAM's have been used as temporary capping layers for Cu film surface passivation. Tan and coworkers studied SAM of alkane-thiol for Cu–Cu bonding at 250–300 °C [24–27]. The wafers were immersed into the solution of 1-hexanethiol [CH_3–$(CH_2)_4$–CH_2–SH, C-chain length of 6C] after Cu film deposition. The thiol(−SH) head groups bind to Cu surface and form a densely packed SAM cap; the methyl ($-CH_3$) tail groups make the Cu surface hydrophobic [27]. After 3–5 days of storage, the SAM was desorbed with annealing at 250 °C for 10 min in vacuum or N_2 ambient to expose the Cu surfaces for bonding. The exposed Cu surface remained hydrophobic and clean for strong bonding, with shear strength of ~60 MPa comparing to ~10 MPa without use of the SAM.

Table 8.3 Various capping layers used for Cu surface passivation and bonding temperatures

Capping layer	Bonding temperature	Features
SAM	250–300 °C	Pre-bonding annealing is needed for SAMs desorption [24–28]
Ti	160–180 °C	Ti diffuses away from the interface [29] Thickness of Ti is important for passivation, surface roughness, and TiO_x content (optimal 3 nm) [30]
Pd	150 °C	Pd diffuses away from the interface Lower contact resistance than Ti passivation [31]
Au	250 °C	Poor bond strength and formation of IMC's [25]

Researchers at IMEC applied thiol-based SAM's as passivation of electroplated Cu pads/pillar/bumps in 3D interconnects. SAM types with different Carbon chains (length of 3, 10, and 18 Carbon) were studied in flat and 3D patterned/microbumped samples on silicon test vehicle (TV) at 50 μm bump pitch [28]. Cyclic voltammetry was used to compare oxidation resistance qualitatively on standalone samples. After chip-on-chip (CoC) stacking electrical probing was used to measure full daisy chain and sub-chain continuity and electrical resistance. C18-SAM (which was deposited in liquid phase $\leq$24 h of immersion on electro-deposited Cu) demonstrated better layer stability and lower oxidation compared to C10-SAM, which was in turn better than C3-SAM. C18-SAM passivation degrades fast in ambient at room temperature conditions regardless of immersion time (based on comparison of 1 day versus post-1 week cyclic voltammetry). Thus, "sit times" of materials in the manufacturing process queue should be of the order of days, otherwise materials need to be stored in vacuum/inert atmosphere and "time critical loop" needs to be set up and controlled. C18-SAM samples yielded electrically ~20% higher in terms of connected daisy chains compared to C10 SAM (Fig. 8.5). Based on electrical probing of two-die stacks, C18-SAM passivation resulted in lower electrical resistance ~500 Ω compared to three times higher resistances for C10 SAM stacks with order-of-magnitude wider variance (Fig. 8.6). It was also found that microwave plasma cleaning prior to SAM deposition is more effective than citric acid cleaning, based on voltammetry on flat samples and electrical resistance and daisy chain continuity of two-die stacks.

Unlike SAM's which are desorbed during bonding (given their atomic layer thicknesses), metal capping layers are present and involved in interfacial reaction during the bonding. Huang et al. [29, 31] studied Cu–Cu bonding by using sputtered Ti and Pd capping layers. Due to lower activation energy at the surface, Cu has a tendency to diffuse toward the bonding interface. In contrast, Ti(TiO_x) diffuse toward Si substrate [29]. This diffusion behavior results in a Ti(TiOx)/Cu–Cu/Ti(TiOx) bonded structure. Similar behavior was also found by using the Pd capping layer. Figure 8.7a presents the TEM images and EDX composition profiles of the bonded structure, showing the interface mainly contains Cu and the oxygen content using Pd capping is smaller than that using Ti capping. Electrical measurements also resulted in much lower contact resistance with Pd than Ti, as illustrated in Fig. 8.7b. Panigrahi et al.

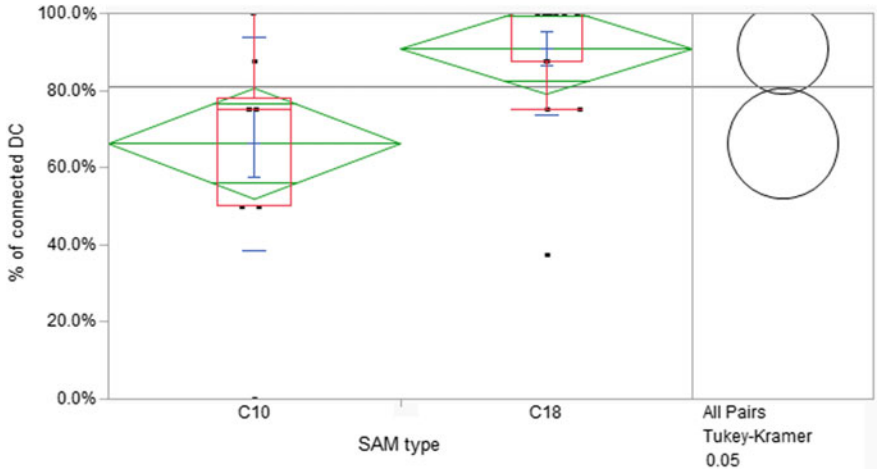

Fig. 8.5 C18 SAM exhibited ~20% higher daisy chain continuity than C10 SAM samples [28]

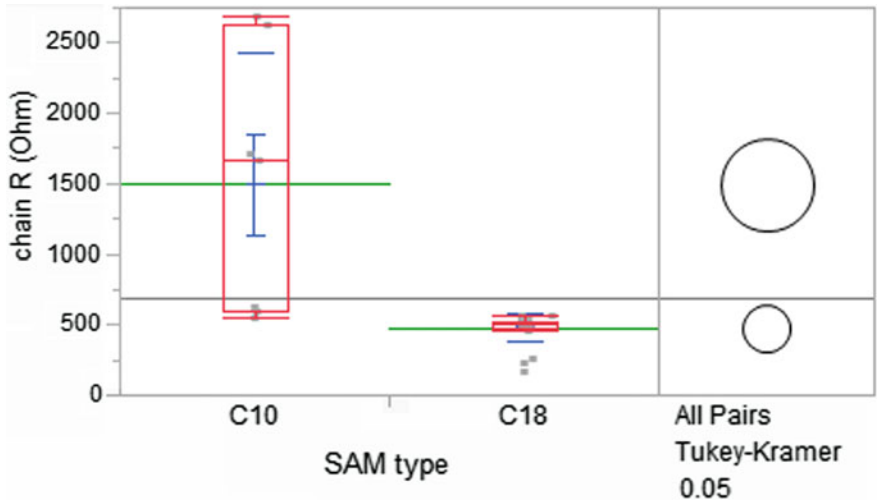

Fig. 8.6 Full-chain electrical resistance distribution of C18 SAM is much tighter and "statistically significantly different" than that C10 SAM's [28]

[30] also investigated the influence of the thickness of the Ti capping layers on passivation and bonding results. They demonstrated that 3 nm Ti capping layer is effective for passivation of Cu surface with small surface roughness and low TiO_x content. The Au capping layer is not suitable for Cu–Cu bonding because of the poor bond strength, which may be owing to formation of IMCs in absence of barriers between Cu and Au layers [25].

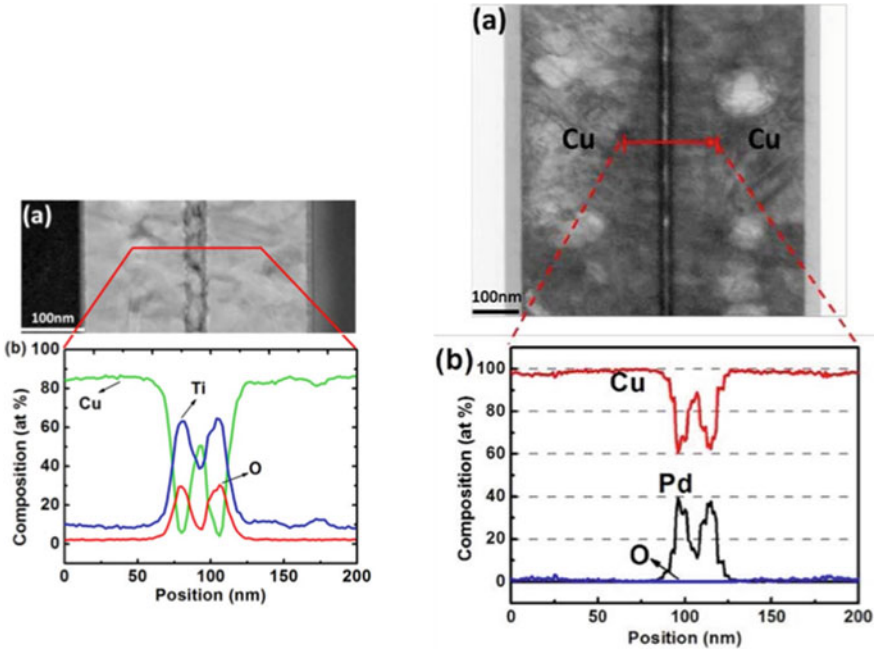

Fig. 8.7 Results of Cu–Cu bonding with Ti (left) and Pd (right) capping layers: (**a**) TEM images and (**b**) EDX composition profiles [29, 31]

Work at IMEC has demonstrated an approach to use non-noble capping layers (e.g. electroless NiB and CoB) to passivate Cu surfaces and enable better bonding [32]. The B in the non-noble capping layers fits into the spaces in the Ni or Co lattice and acts as an interstitial element thereby preventing oxidation of the Ni or Co present in the capping layer. As such, NiB or CoB alloy with an atomic concentration percentage of B from 10 to 50% behaves as a noble metal for surface passivation and at a lower cost (Fig. 8.8).

8.6 Surface Activated Bonding (SAB) Processes

The SAB method is a room-temperature bonding method which uses pre-bonding surface activation in ultra-high-vacuum (UHV). The origin of the SAB dates back to experiments on adhesion in the UHV conducted by NASA in the 1970s. Professor Suga's group at the University of Tokyo made considerable progress in UHV bonding in the 1980s and the technique was extended to apply to homo-/heterogeneous bonding between metals, Si/III-V semiconductors, glasses and polymers.

In addition to the diffusion and reactions at elevated temperatures, there are also always chemical interactions between atoms on the mated clean surfaces. The origin

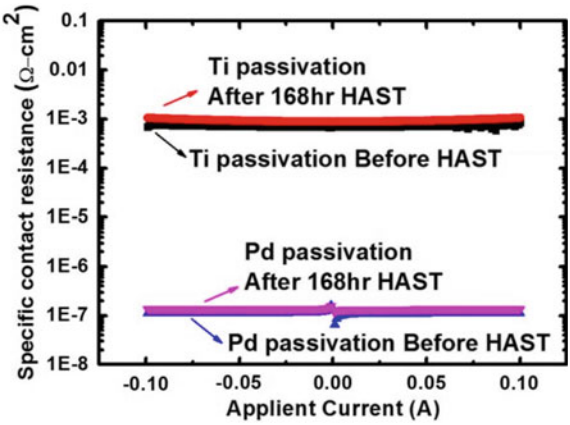

Fig. 8.8 Electrical characteristics comparison of bonded Cu interconnects with Pd and Ti passivation under unbiased highly accelerated stress test (HAST) [31]

of these interactions is the cohesive and adhesive energy of solids, which enables solid state bonding even if there is no high-temperature reaction. The SAB method removes surface oxides and contaminants by utilizing a pre-bonding surface activation by Ar atom beam bombardment in UHV, which prevents rapid re-oxidation and re-contamination of the surfaces prior to bonding. Therefore, the SAB in principle can enable bonding of various materials (metal-to-metal, metals-to-ceramics, metal-to-semiconductors and semiconductors-to-semiconductors) at room temperature, i.e., without either heating or post-bonding annealing [2, 33, 34]. Figure 8.9 shows the TEM images of Cu–Cu bonding interface prepared by using SAB at room temperature. The visible interface implies that no significant diffusion and Cu grain

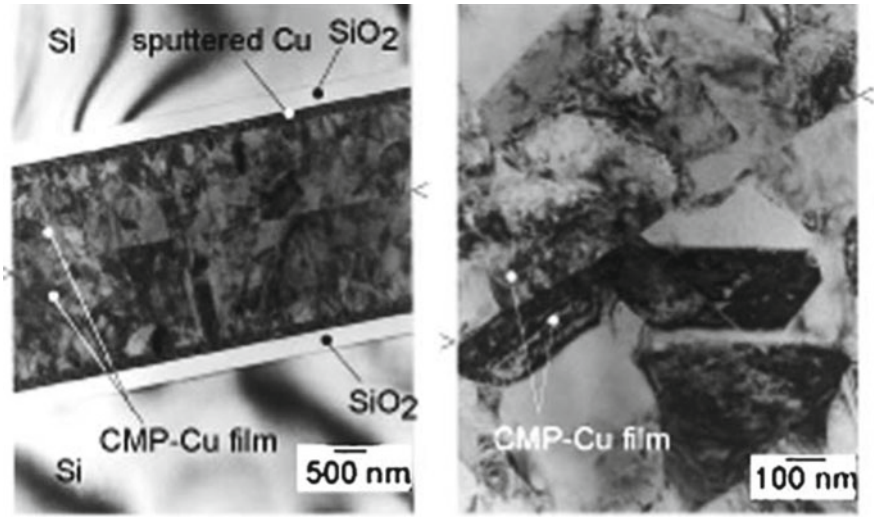

Fig. 8.9 TEM images of the interface between Cu films bonded at room temperature [34]

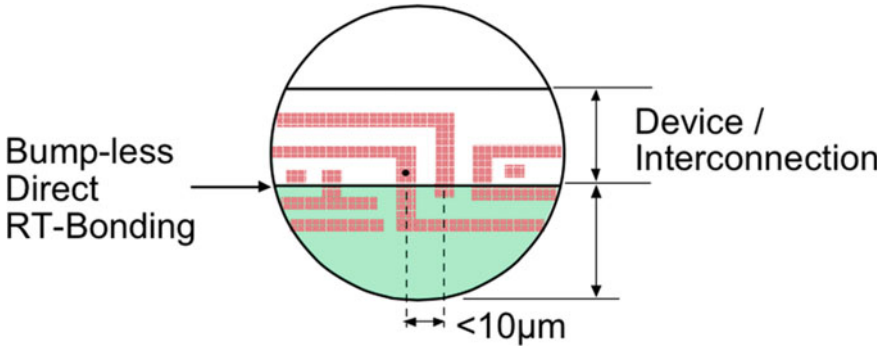

Fig. 8.10 Schematic representation of coplanar, bump-less direct bonding [35]

growth occurred across the bonding interface. It is also indicated that the SAB is less dependent on the Cu diffusion and microstructures of the Cu grains. The SAB avoids the thermal-related issues such as thermal stress, thermal expansion, and expansion-induced bonding misalignment.

Based on the SAB method, Suga proposed the concept of bump-less interconnect in 2000 [35, 36], which is defined as two layer structures bonded directly with metallic interconnections and insulating layer in a plane, as illustrated in Fig. 8.10. The layer structures represent either combinations of LSI chip and substrate, two different devices (RF, digital, analog, logic, memory, etc.) or wiring layer and device layer.

Especially, this structure is expected to be applied to:

(1) Bonding of wiring layer for global interconnections and device layer on chip
(2) Improvement of yield by dividing the wiring layer
(3) Improvement of signal transmission rate by transmission line structure and shortening distance between devices
(4) interconnecting two different device layers, such as separation of analog and digital devices, and
(5) Bonding of optical device to Si substrate, and bonding for hetero-junction of semiconductors [35].

Bump-less Interconnect is a generalized concept and has evolved into "Cu/dielectric hybrid bonding" .

The SAB method demonstrated chip-scale bump-less Cu–Cu bonding interconnects of 1,000,000 electrodes at 3 μm critical dimension and 6 μm pitch, as shown in Fig. 8.11 [4, 37]. To date, SAB has also enabled high-volume industrial applications for metal laminates and MEMS packaging.

SAB was also modified (namely modified diffusion bonding [38] and vapor-assisted SAB [39]) for Cu–Cu bonding in ambient air at 150 °C. Figure 8.12 shows the TEM images of Cu–Cu bonding interfaces obtained with the two processes: by using Ar beam irradiation followed by dry O_2 and humid N_2 exposure, respectively [40, 41]. Void-free bonding with O-containing interlayer of ~15 nm thickness was

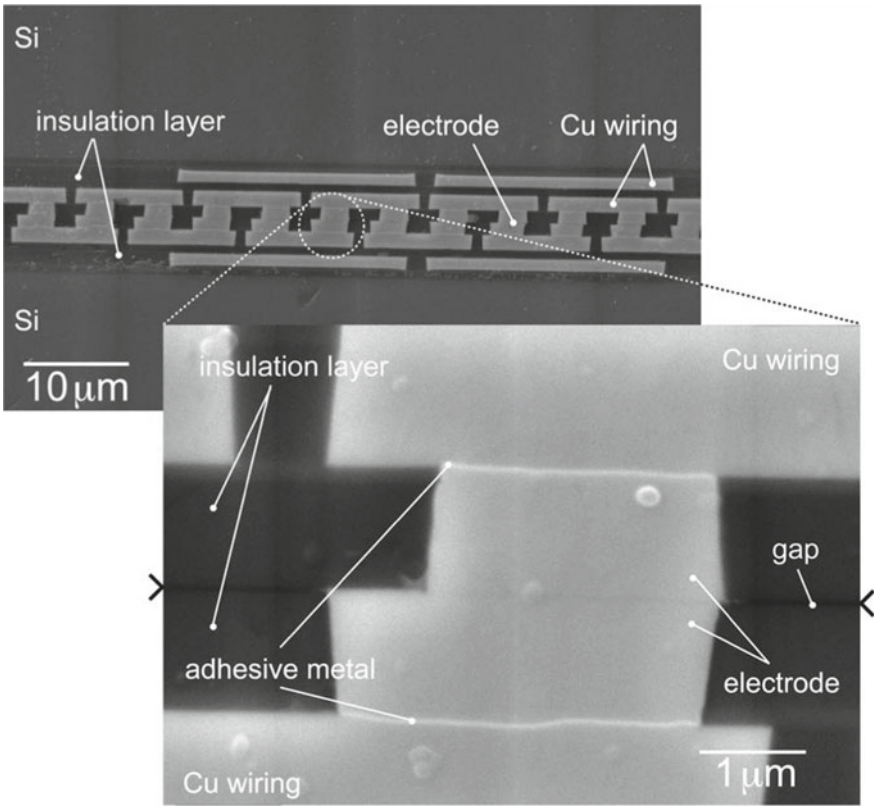

Fig. 8.11 SEM cross-sectional image of bump-less Cu–Cu bonded structure with 6 μm pitch [37]

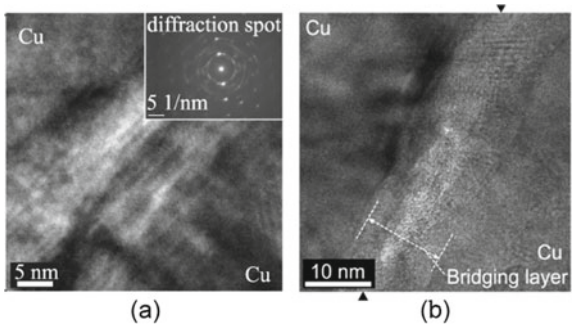

Fig. 8.12 TEM images of the Cu–Cu bonding interface prepared by modified SAB processes at 150 °C: (**a**) modified diffusion bonding using dry O_2 and (**b**) vapor-assisted SAB using humid N_2 gas [40, 41]

achieved by both methods. The bonded interconnects exhibit low resistances that are only slightly higher than that obtained by using conventional SAB in UHV, as compared in Fig. 8.13.

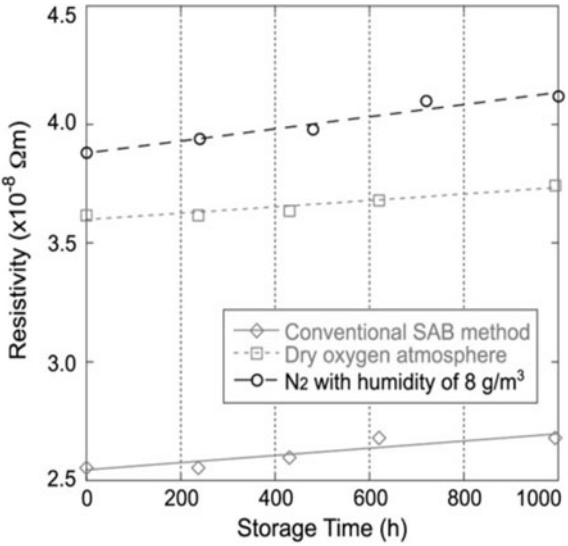

Fig. 8.13 Electrical resistivity of Cu–Cu bonding interconnects by using conventional SAB and modified SAB with dry O atmosphere (modified diffusion bonding [38]) and humid N_2 atmosphere (vapor-assisted SAB [39]) after high-temperature storage testing at 150 °C

SAB also comes with disadvantages, mainly its difficulty of bonding some ionic materials to each other, like glass and silicon dioxide (SiO_2). The reason for this is still not clear but it is assumed that the surface of ionic materials is spontaneously polarized at different levels by ion beam bombardment, which is performed prior to bonding. To overcome the challenge of traditional SAB a modified method was developed. In this approach, the surfaces to be bonded are sputter cleaned by Ar beam and simultaneously deposited with Fe and subsequently Si layer. The metallic thin layer may shield the surface polarity of the ionic materials and enable room temperature bonding of SiO_2, glass and various single crystalline wafers and polymer films at room temperature with high bond strength. Industrial application that were enabled by this modified SAB method are sealing of glass and polymer devices such as organic electro-luminescent display (OELD) or lightening devices since there is no other suitable method for good sealing agent against permeation of water and oxygen from the atmosphere into those devices.

8.7 Cu/Dielectric Hybrid Bonding

Bump-less interconnect promises high-density direct vertical electrical interconnects with very short length between 3D stacked chips or wafers [35, 36]. At the same time, the dielectric passivation area (e.g. oxide/nitride, polymer adhesives) should be bonded so as to enhance the bond strength, heat dissipation, and Cu corrosion protection with a seamless interface. Although such hybrid bonding of metals and dielectric materials has been investigated by, for instance, Au/adhesive, Au/SiO_2,

and Cu–Sn/adhesive combinations, Cu/SiO_2 and Cu/adhesive hybrid bonding are the most promising options for high electrical performance.

The methods used for Cu/SiO_2 and Cu/adhesive hybrid bonding are different because of the different mechanisms of SiO_2–SiO_2 bonding and polymer adhesive bonding. The SiO_2–SiO_2 bonding is typically based on the hydrophilic bonding mechanism, which requires hydrophilic surface modification prior to bonding; the adhesive bonding usually uses thermosetting polymer adhesives, for instance, benzocyclobutene (BCB), polyimide (PI), and polybenzoxazole (PBO), and the bonding is based on TCB.

8.7.1 Cu/SiO_2 Hybrid Bonding

Cu/SiO_2 hybrid bonding can be done through hydrophilic surface modification of the chips or the wafers followed by bonding and then post-bonding annealing. Because of possible CMP dishing of the Cu surface, chips or wafers can be initially bonded only through the SiO_2–SiO_2 bonding at room temperature, as shown in Fig. 8.14a–i. Post-bonding annealing (typically at 200–400 °C) is required to enhance the SiO_2–SiO_2 bonding and to induce thermal expansion of Cu for Cu–Cu bonding, as shown in Fig. 8.14a–ii. The as-bonded SiO_2–SiO_2 strength must be sufficiently high to sustain the stress induced by Cu thermal expansion. Cu/SiO_2 hybrid bonding can be also

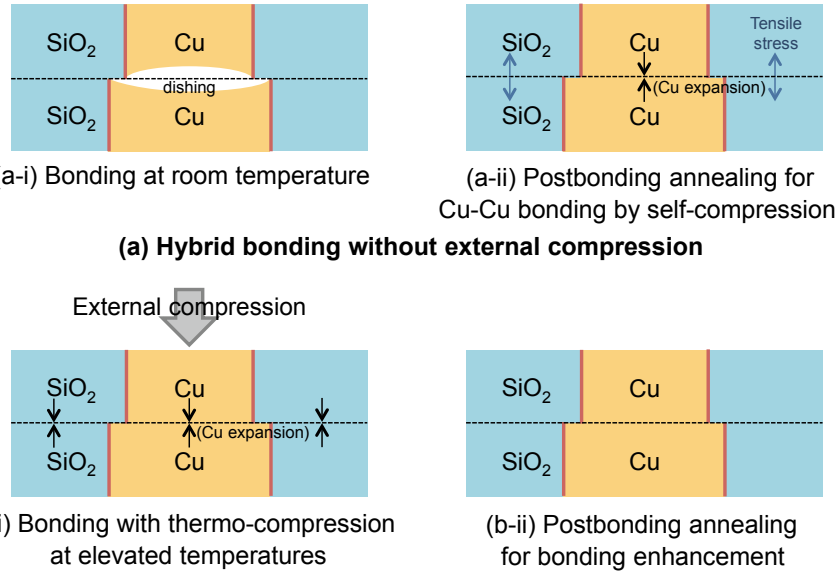

Fig. 8.14 Cu/SiO_2 hybrid bonding (**a**) without and (**b**) with external compression

conducted with TCB, in which the external compression is applied on both the Cu–Cu and SiO_2–SiO_2 interfaces during bonding (Fig. 8.14b–i), before post-bonding annealing to further enhance bonding (Fig. 8.14b–ii).

Table 8.4 compares some methods that have been investigated for Cu/SiO_2 hybrid bonding. The efficiency of plasma activation for SiO_2–SiO_2 and Cu–Cu bonding is still questionable, although it has been shown to be very effective for hydrophilic Si–SiO_2 bonding. By using the plasma activation, the bond strength of the SiO_2–SiO_2 pairs is significantly lower than the Si–SiO_2 pairs [42, 43]. For metal bonding, the plasma activation has been developed for low-temperature bonding of solder [44], Au films [45], and Au particles [46]. However, the benefit still remains unclear for Cu–Cu bonding at below 300 °C. The residual H_2O and O_2 in the plasma chamber, whose pressure is typically in range of 0.1–100 Pa, could oxidize the Cu surfaces even though the Ar or N_2 plasma can be used. M. Park et al. reported formation of Cu_2O and increase in the electrical sheet resistance after Cu surface treatment by Ar plasma [47]. Their bonding results also showed poor bonding quality with obvious

Table 8.4 Comparison of bonding methods for Cu/SiO_2 hybrid bonding

Methods	SiO_2–SiO_2	Cu–Cu
Plasma activation bonding	(1) Significantly lower bond strength than Si–SiO_2 and Si–Si bonding at <300 °C (2) Difficult to remove interfacial H_2O	(1) Cu oxide [47] and nitride [14, 48] formation (2) Surface roughening [47] (3) Sheet resistance increase [47] (4) Post-activation storage decreases the bond strength [48]
Direct Bond Interconnect (DBI®) [49, 50]	(1) High bond strength at 200 °C (2) Small amount of interfacial H_2O [51, 52]	Low resistances are obtained at low temperatures—technical details are rarely disclosed in proprietary processes
Special CMP treatment of Leti-CEA [53–55]	(1) Low bond strength at < 300 °C; (2) Difficult to remove interfacial H_2O (3) Bond strength at low temperature depends on the film deposition process [56]	(1) Ultra-smooth surface is essential (2) Bond strength at room temperature depends on the Cu film deposition method [57] (3) Post-activation storage (e.g. more than 2 h) decreases the Cu–Cu bond strength [58]
Vapor-assisted SAB [39, 59]	Details not reported	High bond strength and low resistance with bonding at 150 °C
Combined SAB [60, 61]	(1) Bonding in vacuum to reduce interfacial H_2O (2) High bond strength at 200 °C	(1) High bond strength at 200 °C (2) Ultra-thin interfacial CuO_x for low resistance

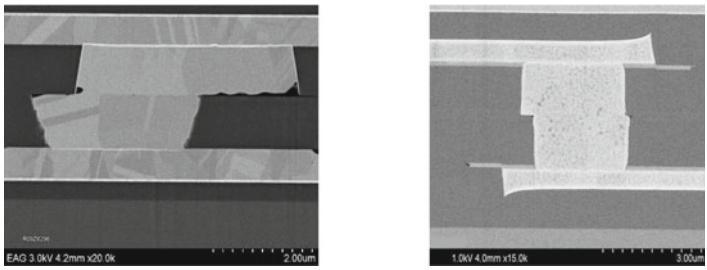

Fig. 8.15 Micrographs of DBI bonded interfaces for different pitches and temperature [63]

large voids with bonding at 300 °C after the Ar plasma activation [47]. Furthermore, some other influences of the plasma treatment on Cu surface, such as pimples and delamination induced by N_2 plasma treatment [14], needs further investigation.

The Direct Bond Interconnect (DBI®) is an industry-reputable hybrid bonding technique utilizing Cu/SiO_2 (or SiN_x) developed by researchers at Ziptronix, Inc. (acquired by Tessera Technologies, Inc. in 2015) [49, 50]. In this technique, after surface plasma activation and chemical treatments for bonding species (e.g., Si–OH and $Si–NH_2$ groups) termination, wafers are bonded in ambient at room temperature without external compression (resulting in considerably high SiO_2–SiO_2 strength through interfacial Si–O–Si and Si–N–N–Si bonds) [51, 52, 62], followed by post-bonding annealing at elevated temperatures (125–400 °C [63]) for Cu–Cu bonding facilitated by internal compression induced by Cu thermal expansion [49]. By using fluorinated oxide, the oxide-oxide strength can be further improved because of the improved absorption of interfacial H_2O by the fluorinated oxide. Fermilab and Sony, respectively, have applied this process in 3D stacked image sensors in recent years [7–9]. An eight-layer wafer stack, containing 8 layers of transistors and 80 layers of interconnect, bonded by the DBI® technique was demonstrated by Tezzaron Semiconductor and Novati Technologies in the 2015 IEEE 3DIC conference. Examples of hybrid bonded structures are shown in Fig. 8.15.

Researchers at CEA-Leti[4] developed a direct bonding method for Cu/SiO_2 hybrid bonding by making Cu and SiO_2 surfaces ultra-smooth and hydrophilic using optimized CMP [53–55]. The bonding is conducted in air at room temperature and without external compression. Figure 8.16 shows the interface of the Cu/SiO_2 hybrid bonded structure reported by researchers of CEA-Leti. The bonding behaviors were studied in detail by Cu–Cu and SiO_2–SiO_2 bonding experiments using blanket films. For Cu–Cu bonding, bond-strengthening behavior at low temperatures was found depending on the Cu film deposition method [57]. Using Cu films electrodeposited on Si wafers, the Cu–Cu bonding energy is around 0.8 J/m^2 as-bonded and increases to around 2.8 J/m^2 after 60 days of storage; Using physical vapor deposited Cu films, the Cu–Cu bonding energy is around 0.5 J/m^2 as-bonded and slightly increases to

[4] http://www.leti-cea.com/cea-tech/leti/english/Pages/Welcome.aspx.

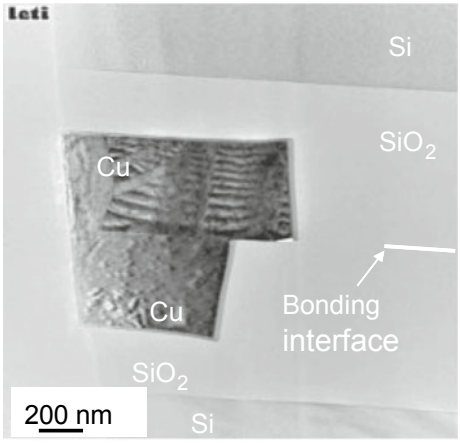

Fig. 8.16 TEM image of the Cu–Cu bonded interface obtained by CMP treatment [53]

0.7 J/m^2 after 120 days of storage [57, 64]. The SiO_2–SiO_2 bonding energy is around 0.2 J/m^2 at room temperature. Typically, post-bonding annealing at 200–400 °C is employed to improve the bonding energy and to close the gaps between CMP-dished Cu surfaces [54], which is the same as the DBI concept. After 200 °C annealing, the SiO_2–SiO_2 bonding energy is comparable to that by using plasma activation bonding but still lower than the Si bulk fracture energy [65]. Literatures suggest the SiO_2–SiO_2 bonding quality can be limited by the presence of excess interfacial H_2O molecules. It has been reported that voids are generated owing to the excess H_2O at the SiO_2–SiO_2 bonding interface [56, 66]. Furthermore, Fournel et al. [67] reported that the SiO_2–SiO_2 bond strength can be decreased by the water stress corrosion effect induced by the interfacial H_2O, which is difficult to remove at temperatures below 400 °C. In case of annealing at 400 °C, the strength of the Cu/SiO_2 hybrid bonded wafer is significantly improved [54], however voids are generated at the Cu–Cu bonding interface and in the Cu films [68, 69]. This technique has been demonstrated in a 3D stacked image sensor on a logic die [70].

It is also feasible to realize hybrid bonding by using the vapor-assisted SAB and combined SAB methods. Although the conventional SAB methods is effective for Cu–Cu bonding at room temperature, it was shown to be ineffective for the SiO_2–SiO_2 bonding [71]. The vapor-assisted SAB method was developed not only for low-temperature Cu–Cu bonding in ambient atmosphere, but also for hybrid bonding with material combinations of Cu, SiO_2 and polyimide [38, 39, 59]. However, this method also faces the concern of low SiO_2–SiO_2 bonding quality due to the water stress corrosion effect and generation of voids owing to trapping of excess H_2O. The combined SAB method was recently proposed to improve the SiO_2–SiO_2 bonding quality for Cu/SiO_2 hybrid bonding, based on bonding in vacuum for pre-bonding removal of excess H_2O molecules adsorbed on the wafers and for prevention of gas trapping [60, 61]. The combined SAB involves a combination of surface irradiation using a Si-containing Ar beam and pre-bonding attach-detach process prior to bonding in vacuum. The Si atoms added in the Ar beam are expected to increase

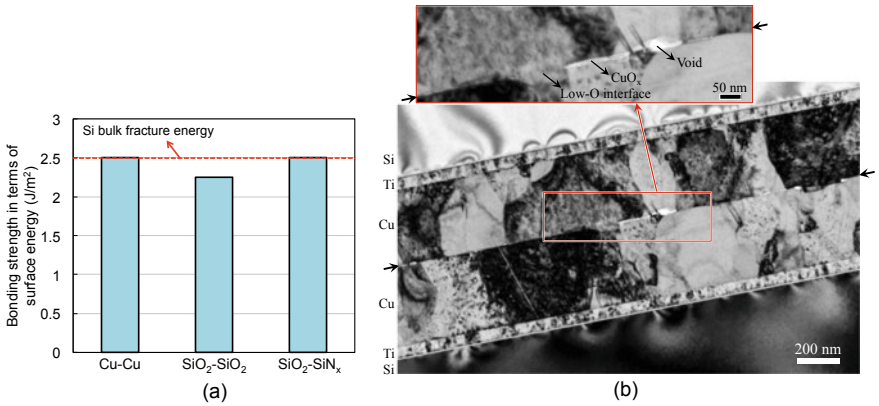

Fig. 8.17 Results of the combined SAB method for (**a**) bond strength of various blanket films at 200 °C and (**b**) TEM image of the Cu–Cu bonded interface [60]

the number of reactive Si sites on SiO_2 surface, while the pre-bonding attach-detach process is used to enhance the OH adsorption and to remove excess H_2O prior to bonding in vacuum. As a result of the combined procedure, high Cu–Cu, SiO_2–SiO_2, and SiO_2–SiN_x bond strength has been realized by bonding in vacuum of 10^{-2} Pa under an external compression of 2.5 MPa at 200 °C for 30 min followed by 200 °C annealing in ambient for 2 h [61]. The external compression is applied to ensure the wafers are tightly contacted even in the presence of large surface roughness, Cu dishing, and wafer warp and bow. Figure 8.17a shows the bond strength of various blanket bonded pairs, which is close to the Si bulk fracture strength of 2.5 J/m^2. Figure 8.17b shows the microstructure of the Cu–Cu bonding interface, containing low-O interface, ultrathin CuO_x interlayer and several small voids.

Since it is also demonstrated that high SiO_2–SiO_2 bond strength can be obtained with bonding at room temperature followed by 200 °C annealing without thermo-compression [61], it can be interesting to optimize the combined SAB for Cu/SiO_2 hybrid bonding without compression. Based on Suga's group experience, strong Cu–Cu bonding can also be achieved at 200 °C by combining Ar plasma activation (in low vacuum of ~60 Pa) with pre-bonding attach-detach process. Since the plasma activation has been widely studied for SiO_2–SiO_2 bonding, this combined approach holds promise for development of Cu/SiO_2 hybrid bonding without the use of high vacuum.

In summary, Cu/SiO_2 hybrid bonding is more complex than Cu–Cu bonding due to the need for simultaneous surface activation of Cu and SiO_2, more complex bonding conditions and risk mitigation of Cu dishing. Further research is needed to increase the bond strength obtained at <250 °C, to better understand and control Cu dishing (due to wafer warp and bow and planarization process) in order to ensure high yield of low-resistance bonded interconnects.

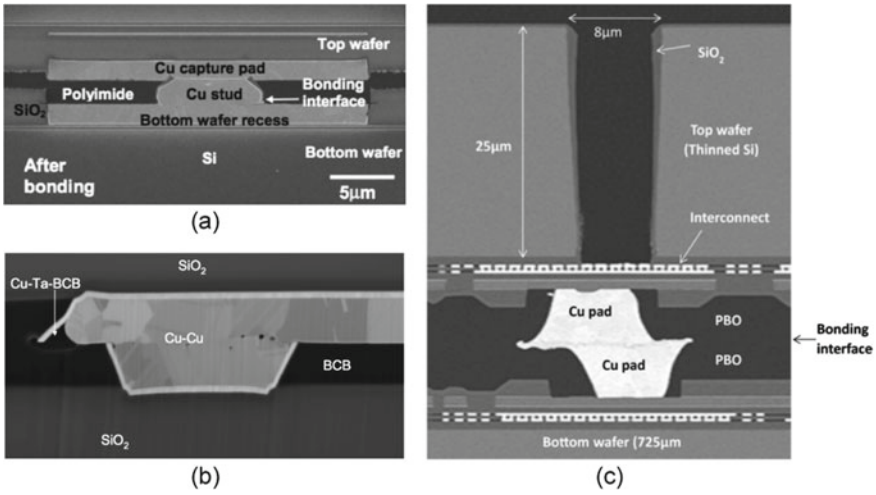

Fig. 8.18 Cu/adhesive hybrid bonded structures of (**a**) IBM [72], (**b**) RPI [73] and **c** ASET [74]

8.7.2 Cu/Adhesive Hybrid Bonding

Besides Cu/SiO_2 hybrid bonding, Cu/adhesive hybrid bonding using polymer adhesives instead of SiO_2 has also been investigated for 3D integration. Figure 8.18 shows the micrographs of Cu/adhesive hybrid bonded structures using adhesives of polyimide (PI), benzocyclobutene (BCB), and polybenzoxazole (PBO). Researchers at IBM developed Cu/adhesive (PI) hybrid bonding by using lock-and-key bonding structures [72]. Researchers at RPI (USA) [73] and ASET (Japan) [74] developed Cu/adhesive hybrid bonding with BCB and PBO adhesives prepared by CMP, respectively.

Cu/adhesive hybrid bonding is typically performed through an "adhesive-first" bonding approach, as shown in Fig. 8.19a, in which the adhesive is thermocompression bonded (TCB) and cured at a lower temperature (material-dependent e.g. ~250 °C for 1 h for BCB) before Cu–Cu TCB at a higher temperature (350–400 °C) [75, 76]. This two-step bonding sequence is employed because the high Cu–Cu bonding temperature may damage the adhesive if it is not fully cured beforehand. The "adhesive-first" hybrid bonding approach is challenging due to limited choice of adhesive materials (having high thermal stability during high-T Cu–Cu bonding), low throughput (long-duration TCB) and high thermal stress due to high Cu–Cu bonding temperature. In addition, relative slip between upper/lower substrates during adhesive bonding/curing may cause misalignment of the final bonded structure [77]. To address such issues, it is highly desired to develop a "Cu-first" hybrid bonding approach, in which Cu–Cu bonding is performed at low temperature (lower than the adhesive bonding/curing temperature ($<200\ °C < T < 250\ °C$) and with shorter duration (e.g. ≤ 10 min) prior to the longer-duration adhesive curing step, as shown in Fig. 8.19b.

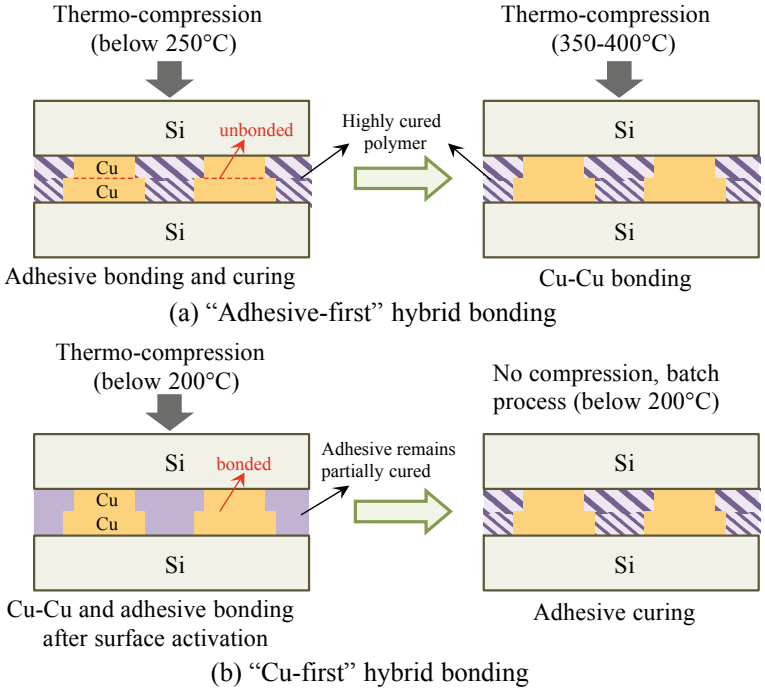

Fig. 8.19 Cu/adhesive hybrid bonding: (**a**) "adhesive-first" hybrid bonding process and (**b**) "Cu-first" hybrid bonding process

Effective surface activation methods for low-temperature (<250 °C) Cu/adhesive hybrid bonding are still rarely studied, although various physical and chemical surface activation methods have been studied for Cu–Cu bonding, as described above in this chapter. The presence of adhesive in the Cu/adhesive hybrid bonding requires the surface activation to be adhesive-compatible, i.e., introducing acceptable chemical/thermal damages and Cu contaminants to the adhesive materials. For instance, Ar atom beam and Ar plasma irradiation are considered to be unfriendly for Cu/adhesive surface activation, mainly because they may induce Cu impurities on the adhesive owing to adsorption of physically sputtered Cu atoms onto the adhesive surface [78].

It seems promising to reduce the thermal budget for the Cu/adhesive hybrid bonding and to avoid the sputtering induced Cu impurities on adhesives by using H-containing HCOOH vapor treatment. The H-containing HCOOH vapor treatment enables strong Cu–Cu bonding (shear strength of >10 MPa) at 200 °C with considerably short pre-bonding treatment time (≤10 min) and thermo-compression time ~5 min [16]. Since several adhesives are capable of sustaining 200 °C heating for a certain time duration, it should be possible to realize the "Cu-first" hybrid bonding through optimization of the H-containing HCOOH vapor treatment by controlling temperature and time for Cu/adhesive surface treatment. More experimental demonstrations are needed in this area.

8.8 Alternative Cu–Cu Bonding Techniques: Insertion Bonding

Cu–Cu insertion is a bonding process approach for low-temperature bonding and has been applied to Cu-TSVs bonding schemes. The method relies on applying high shear stresses to yield large local plastic deformation of the Cu–Cu bonding surfaces [79]. The high shear stress is achieved by design of a sloped sidewall landing pad (instead of the usual flat pad) and by applying force/pressure on TSV nails inserted into the sloped pads (refer to Fig. 8.20).

To enable the insertion process, the landing pads have sloped sidewalls plated with Cu. This can be realized either by modifying the back-end-of-line (BEOL) passivation process, or by additional passivation steps. The latter approach can offer more flexibility at the price of additional lithography and etching steps. Figure 8.21 indicates images of the landing pads after key processing steps like lithography, etch and final Cu CMP.

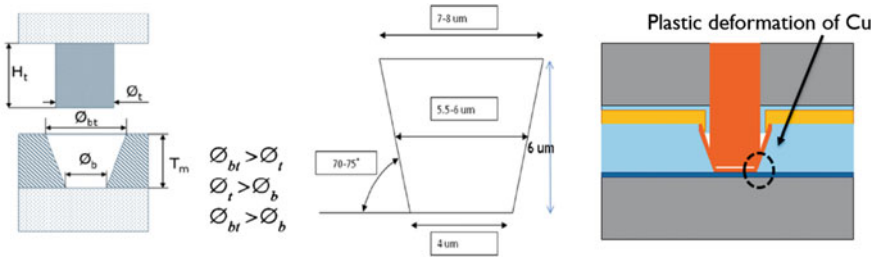

Fig. 8.20 Cu–Cu Insertion bonding (Cu-TSV scheme)

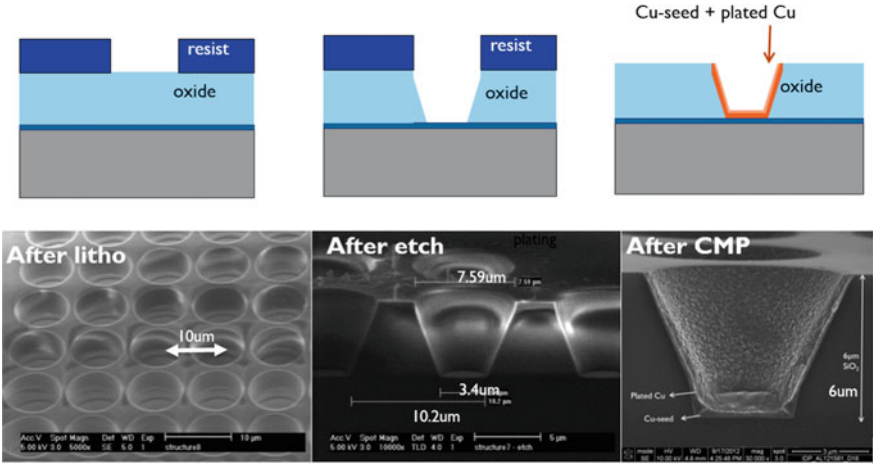

Fig. 8.21 Cu–Cu Insertion bonding: landing pad processing steps

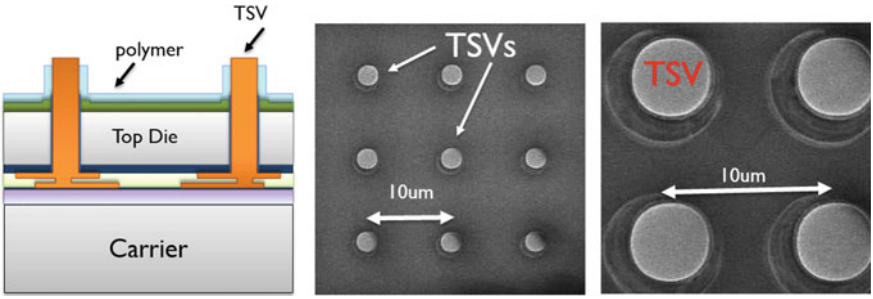

Fig. 8.22 Cu–Cu Insertion bonding: Schematic (left) and Top die prior to stacking (right)

The processing of the top die is based on a temporary bonding system, with the wafer bonded on a temporary carrier while TSV's are exposed from backside. The wafer backside is standardly passivated with a SiN layer, this is necessary to avoid any possible Cu diffusion from exposed TSV. A polymer layer is than applied and developed in order to expose TSVs and act as filling layer between top and bottom dies during the stacking step (refer to Fig. 8.22).

A process with bonding temperature of 100 °C was demonstrated at IMEC/Belgium with a seamless bond interface [79], while at room temperature the bonding interface was visible. Figure 8.23 shows some stacking images based on Cu–Cu insertion bonding where both dies have TSVs.

Potential process improvements include Cu–Cu insertion bonding variant processes in the presence of cleaning agent, optimization of sidewall angle, and microstructure considerations. This approach can be used for different stacking schemes (die-to-wafer, die-to-die) and can also be extended to multi die stacking.

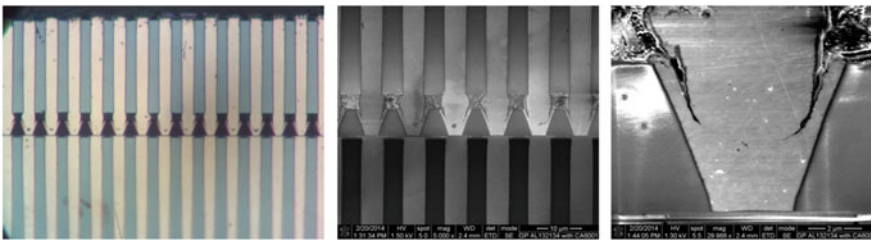

Fig. 8.23 Cu–Cu Insertion bonding: X-section after stacking of two dies with TSV's

8.9 Cu–Cu Bonding—Equipment Landscape and State of the Art

In terms of high-volume manufacturing (HVM) there is a limited number of 300 mm WoW bonding equipment, while the supply chain grows more with CoW and definitely further for CoC thermo-compression bonding (TCB) equipment. Key equipment suppliers for 300 mm wafer-level Cu–Cu bonding equipment suppliers are: EVG (Austria) and Suss Microtech (Germany). Mitsubishi Heavy Industries Group (Japan) developed standard SAB equipment and Bondtech (Japan) developed and integrated SAB equipment with plasma cleaning/activation, alignment and pre-bonding, bonding and heating chambers, both for 300 mm wafer bonding. For CoC or CoW, a number of flip chip bonder equipment suppliers have adopted prior toolsets or designed new TCB tools to accommodate faster heat ramp times, improved alignment and handling of multiple input materials (wafers, substrates/sub-panels/strips in metal carriers or trays. Key TCB bonder suppliers/toolsets are: Toray (Japan), ASM (Singapore), BeSi/Datacon (Austria) and K&S (USA), however this is not a comprehensive list. In terms of applications and commercialization, surface activated bonding (SAB) has been applied in volume production in metal laminates, MEMS packaging, and OELD devices to ensure hermetic sealing against permeation of water and oxygen from the atmosphere into these devices. Cu/SiO_2 hybrid bonding (DBI®) has been applied by Sony for 3D stacked back-illuminated image sensors (IMX260 used in Samsung Galaxy S7 Edge) [9], while new applications have been reported for hybrid bonding for 3D stacked hybrid pixel detectors for X-rays at Fermilab [80–82].

8.10 Chapter Summary and Recommendations for Future Research

In this chapter, we reviewed various Cu–Cu bonding methods and fundamental material and surface characteristics aspects of bonding mechanisms. The effects of Cu surface activation, diffusion, microstructure and surface passivation by capping layers (e.g. metal, passivation and SAM's) were discussed. Surface activation is of great importance in obtaining seamless Cu–Cu bonding at below 250 °C or even at room temperature. Cu/dielectric hybrid bonding using DBI®, CMP and combined SAB methods was also discussed. We introduced insertion bonding for Cu-TSV's leveraging high compression due to the "Cu nail-in-cavity" shape and configuration resulting in Cu plastic deformation and seamless bonding. Equipment for Cu–Cu bonding for HVM has been briefly introduced. Scaling to large surface area chips, wafers or panels with higher warpage and high-density interconnects remains a challenge especially in meeting lower compression pressure, lower process times and thermal requirements. In the near term, for higher Cu–Cu bonding adoption, more effort is needed to drive lower process times, seamless bonding quality and reliability

meeting requirements for various interconnect domains (e.g. sensors, memory-on-logic and higher-IO density logic-on-logic) and applications (automotive, mobile, client, server). Adoption of new technology is not solely a technical challenge but also a business challenge which involves new equipment investments and timely introduction to enable adequate product volumes for high volume manufacturing (HVM). Eliminating solders and solder intermetallic compounds (IMC's) seems promising, however Cu-only interconnects are also prone to electromigration. Cu alloying and doping evolving from SAB methods, new protective layers and novel processing [83] and Cobalt demonstrations have been researched [84] and in special cases also deployed [85]. In the long term, advanced materials (e.g. 2D/nanomaterials) may be introduced as auxiliary materials for Cu–Cu enabling or even as key interconnect materials with potential to replace Cu altogether [86]. As Prof. Feynman once said: "There is plenty of room at the bottom."

Acknowledgements The editors would like to thank Hualiang Shi and Debendra Mallik of Intel Corporation for their critical review of this Chapter.

References

1. A. Fan, A. Rahman, R. Reif, Copper wafer bonding. Electrochem. Solid-State Lett. **2**, 534–536 (1999). https://doi.org/10.1149/1.1390894
2. A. Shigetou, N. Hosoda, T. Itoh, T. Suga, Room-temperature direct bonding of CMP-Cu film for bumpless interconnection, in *2001 51st Electron Electronic Components and Technology Conference* (Orlando, FL, 2001), pp 755–760
3. P.R. Morrow, C.-M. Park, S. Ramanathan, M.J. Kobrinsky, M. Harmes, Three-dimensional wafer stacking via Cu–Cu bonding integrated with 65-nm strained-Si/low-k CMOS technology. IEEE Electron Device Lett. **27**, 335–337 (2006). https://doi.org/10.1109/LED.2006.873424
4. A. Shigetou, T. Itoh, M. Matsuo, N. Hayasaka, K. Okumura, T. Suga, Bumpless interconnect through ultrafine Cu electrodes by means of surface-activated bonding (SAB) method. IEEE Trans. Adv. Packag. **29**, 218–226 (2006). https://doi.org/10.1109/TADVP.2006.873138
5. B. Swinnen, W. Ruythooren, P. De Moor, L. Bogaerts, L. Carbonell, K. De Munck, B. Eyckens, S. Stoukatch, D.S. Tezcan, Z. Tokei, J. Vaes, 3D integration by Cu–Cu thermo-compression bonding of extremely thinned bulk-Si die containing 10 μm pitch through-Si vias, in *2006 International Electron Devices Meeting* (IEEE, 2006), pp. 1–4
6. Tezzaron Company History. http://www.tezzaron.com/about-us/company-history. Accessed 18 Jun 2016
7. G.W. Deptuch, M. Demarteau, J.R. Hoff, R. Lipton, A. Shenai, M. Trimpl, R. Yarema, T. Zimmerman, Vertically integrated circuits at Fermilab. IEEE Trans. Nucl. Sci. **57**, 2178–2186 (2010). https://doi.org/10.1109/TNS.2010.2049659
8. R. Yarema, G. Deptuch, J. Hoff, F. Khalid, R. Lipton, A. Shenai, M. Trimpl, T. Zimmerman, Vertically integrated circuit development at Fermilab for detectors. J. Instrum. **8**, C01052 (2013). https://doi.org/10.1088/1748-0221/8/01/C01052
9. Chipworks, Samsung Galaxy S7 Edge Teardown Report, 2016
10. M. Higashiwaki, K. Sasaki, T. Kamimura, M.H. Wong, D. Krishnamurthy, A. Kuramata, T. Masui, S. Yamakoshi, Depletion-mode Ga2O3 metal-oxide-semiconductor field-effect transistors on β-Ga2O3 (010) substrates and temperature dependence of their device characteristics. Appl. Phys. Lett. **103**, 123511 (2013). https://doi.org/10.1063/1.4821858

11. T. Fukushima, Y. Yamada, H. Kikuchi, M. Koyanagi, New three-dimensional integration technology using self-assembly technique, in *IEEE International Electron Devices Meeting, 2005. IEDM Technical Digest.* (IEEE, 2005), pp. 348–351
12. Y.-S. Tang, Y.-J. Chang, K.-N. Chen, Wafer-level Cu–Cu bonding technology. Microelectron. Reliab. **52**, 312–320 (2012). https://doi.org/10.1016/j.microrel.2011.04.016
13. C.S. Tan, R. Reif, N.D. Theodore, S. Pozder, Observation of interfacial void formation in bonded copper layers. Appl. Phys. Lett. **87**, 201909 (2005). https://doi.org/10.1063/1.2130534
14. B. Rebhan, T. Plach, S. Tollabimazraehno, V. Dragoi, M. Kawano, Cu–Cu wafer bonding: An enabling technology for three-dimensional integration. In: *2014 International Conference on Electronics Packaging (ICEP)* (IEEE, 2014). pp 475–479
15. B. Rebhan, S. Tollabimazraehno, G. Hesser, V. Dragoi, Analytical methods used for low temperature Cu–Cu wafer bonding process evaluation. Microsyst. Technol. **21**, 1003–1013 (2015). https://doi.org/10.1007/s00542-015-2446-2
16. W. Yang, M. Akaike, M. Fujino, T. Suga, A combined process of formic acid pretreatment for low-temperature bonding of copper electrodes. ECS J. Solid State Sci. Technol. **2**, P271–P274 (2013). https://doi.org/10.1149/2.010306jss
17. W. Yang, M. Akaike, T. Suga, Effect of formic acid vapor in situ treatment process on Cu low-temperature bonding. IEEE Trans. Compon. Packag. Manuf. Technol. **4**, 951–956 (2014). https://doi.org/10.1109/TCPMT.2014.2315761
18. P.-I. Wang, S.H. Lee, T.C. Parker, M.D. Frey, T. Karabacak, J.-Q. Lu, T.-M. Lu, Low temperature wafer bonding by Copper Nanorod Array. Electrochem. Solid-State Lett. **12**, H138–H141 (2009). https://doi.org/10.1149/1.3075900
19. T. Ishizaki, R. Watanabe, A new one-pot method for the synthesis of Cu nanoparticles for low temperature bonding. J. Mater. Chem. **22**, 25198–25206 (2012). https://doi.org/10.1039/C2JM34954J
20. C.-M. Liu, H.-W. Lin, Y.-S. Huang, Y.-C. Chu, C. Chen, D.-R. Lyu, K.-N. Chen, K.-N. Tu, Low-temperature direct copper-to-copper bonding enabled by creep on (111) surfaces of nanotwinned Cu. Sci. Rep. **5**, 9734 (2015). https://doi.org/10.1038/srep09734
21. T. Shimatsu, M. Uomoto, Atomic diffusion bonding of wafers with thin nanocrystalline metal films. J. Vac. Sci. Technol., B **28**, 706–714 (2010). https://doi.org/10.1116/1.3437515
22. T. Shimatsu, M. Uomoto, Room temperature bonding of wafers with thin nanocrystalline metal films. ECS Trans. **33**, 61–72 (2010). https://doi.org/10.1149/1.3483494
23. V. Smet, M. Kobayashi, T. Wang, P.M. Raj, R. Tummala, A new era in manufacturable, low-temperature and ultra-fine pitch Cu interconnections and assembly without solders, in *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)* (IEEE, 2014), pp. 484–489
24. C.S. Tan, D.F. Lim, S.G. Singh, S.K. Goulet, M. Bergkvist, Cu–Cu diffusion bonding enhancement at low temperature by surface passivation using self-assembled monolayer of alkane-thiol. Appl. Phys. Lett. **95**, 192108 (2009). https://doi.org/10.1063/1.3263154
25. D.F. Lim, J. Wei, K.C. Leong, C.S. Tan, Surface passivation of Cu for low temperature 3D wafer bonding. ECS Solid State Lett. **1**, P11–P14 (2012)
26. D.F. Lim, J. Wei, K.C. Leong, C.S. Tan, Cu passivation for enhanced low temperature ($\leqslant$300 °C) bonding in 3D integration. Microelectron. Eng. **106**, 144–148 (2013). https://doi.org/10.1016/j.mee.2013.01.032
27. L. Peng, L. Zhang, J. Fan, H.Y. Li, D.F. Lim, C.S. Tan, Ultrafine pitch (6 μm) of recessed and bonded Cu–Cu interconnects by three-dimensional wafer stacking. IEEE Electron. Device Lett. **33**, 1747–1749 (2012). https://doi.org/10.1109/LED.2012.2218273
28. S. Armini, Y. Vandelaer, A. Lesniewska, V. Cherman, I. De Preter, F. Inoue, J. Derakhshandeh, G. Vakanas, E. Beyne, Thiol-based self-assembled monolayers (SAMs) as an alternative surface finish for 3D Cu microbumps, in *TMS 2015 Proceedings Supplements*, (Wiley, London, 2015), pp. 1355–1360
29. Y.-P. Huang, Y.-S. Chien, R.-N. Tzeng, M.-S. Shy, T.-H. Lin, K.-H. Chen, C.-T. Chiu, J.-C. Chiou, C.-T. Chuang, W. Hwang, H.-M. Tong, K.-N. Chen, Novel Cu-to-Cu bonding With Ti passivation at 180 °C in 3-D integration. IEEE Electron. Device Lett. **34**, 1551–1553 (2013). https://doi.org/10.1109/LED.2013.2285702

30. A.K. Panigrahi, S. Bonam, T. Ghosh, S.G. Singh, S.R.K. Vanjari, Ultra-thin Ti passivation mediated breakthrough in high quality Cu–Cu bonding at low temperature and pressure. Mater. Lett. **169**, 269–272 (2016). https://doi.org/10.1016/j.matlet.2016.01.126
31. Y.-P. Huang, Y.-S. Chien, R.-N. Tzeng, K.-N. Chen, Demonstration and electrical performance of Cu–Cu bonding at 150 °C with pd passivation. IEEE Trans. Electron Devices **62**, 2587–2592 (2015). https://doi.org/10.1109/TED.2015.2446507
32. E. Beyne, V.J. De, J. Derakhshandeh, L. England, G. Vakanas, Thin Nib or Cob capping layer for non-noble metallic bonding landing pads (2015)
33. T.H. Kim, M.M.R. Howlader, T. Itoh, T. Suga, Room temperature Cu–Cu direct bonding using surface activated bonding method. J. Vac. Sci. Technol., A **21**, 449–453 (2003). https://doi.org/10.1116/1.1537716
34. A. Shigetou, T. Itoh, T. Suga, Direct bonding of CMP-Cu films by surface activated bonding (SAB) method. J. Mater. Sci. **40**, 3149–3154 (2005). https://doi.org/10.1007/s10853-005-2677-1
35. T. Suga, Feasibility of surface activated bonding for ultra-fine pitch interconnection-a new concept of bump-less direct bonding for system level packaging, in *2000 Proceedings. 50th Electronic Components and Technology Conference (Cat. No. 00CH37070)* (IEEE, 2000), pp. 702–705
36. T. Suga, K. Otsuka, Bump-less interconnect for next generation system packaging. in *2001 Proceedings. 51st Electronic Components and Technology Conference (Cat. No. 01CH37220)*, (IEEE, 2001), pp. 1003–1008
37. A. Shigetou, T. Itoh, K. Sawada, T. Suga, Bumpless Interconnect of 6-μm-Pitch Cu Electrodes at Room Temperature. IEEE Trans. Adv. Packag. **31**, 473–478 (2008). https://doi.org/10.1109/TADVP.2008.920644
38. A. Shigetou, T. Suga, Modified diffusion bonding of chemical mechanical polishing Cu at 150 °C at ambient pressure. Appl. Phys. Express **2**, 056501 (2009). https://doi.org/10.1143/APEX.2.056501
39. A. Shigetou, T. Suga, Vapor-assisted surface activation method for homo- and heterogeneous bonding of Cu, SiO_2, and polyimide at 150 °C and atmospheric pressure. J. Electron. Mater. **41**, 2274–2280 (2012). https://doi.org/10.1007/s11664-012-2091-9
40. Shigetou, A. and Suga, T., Modified diffusion bond process for chemical mechanical polishing (CMP)-Cu at 150 °C in ambient air, in *2009 59th Electronic Components and Technology Conference* (IEEE, San Diego, CA, 2009) pp. 365–369
41. A. Shigetou, T. Suga, Homo/heterogeneous bonding of Cu, SiO_2, and polyimide by low temperature vapor-assisted surface activation method, in *2011 IEEE 61st Electronic Components and Technology Conference (ECTC)* (IEEE, Lake Buena Vista, 2011), pp. 32–36
42. T. Plach, K. Hingerl, S. Tollabimazraehno, G. Hesser, V. Dragoi, M. Wimplinger, Mechanisms for room temperature direct wafer bonding. J. Appl. Phys. **113**, 094905 (2013). https://doi.org/10.1063/1.4794319
43. T. Suni, K. Henttinen, I. Suni, J. Mäkinen, Effects of plasma activation on hydrophilic bonding of Si and SiO_2. J. Electrochem. Soc. **149**, G348–G351 (2002). https://doi.org/10.1149/1.1477209
44. Y.-H. Wang, K. Nishida, M. Hutter, T. Kimura, T. Suga, Low-temperature process of fine-pitch Au–Sn bump bonding in ambient air. Jpn. J. Appl. Phys. **46**, 1961 (2007). https://doi.org/10.1143/JJAP.46.1961
45. K. Okumura, E. Higurashi, T. Suga, K. Hagiwara, Influence of air exposure time on bonding strength in Au-Au surface activated wafer bonding, in *2015 International Conference on Electronics Packaging and iMAPS All Asia Conference (ICEP-IAAC)* (IEEE, 2015), pp. 448–451
46. H. Ishida, T. Ogashiwa, Y. Kanehira, S. Ito, T. Yazaki, J. Mizuno, Low-temperature, surface-compliant wafer bonding using sub-micron gold particles for wafer-level MEMS packaging, in *2012 IEEE 62nd Electronic Components and Technology Conference* (IEEE, 2012), pp. 1140–1145

47. M. Park, S. Baek, S. Kim, S.E. Kim, Argon plasma treatment on Cu surface for Cu bonding in 3D integration and their characteristics. Appl. Surf. Sci. **324**, 168–173 (2015). https://doi.org/10.1016/j.apsusc.2014.10.098
48. S.L. Chua, G.Y. Chong, Y.H. Lee, C.S. Tan, Direct copper-copper wafer bonding with Ar/N_2 plasma activation, in *2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)* (IEEE, 2015), pp. 134–137
49. P. Enquist, G. Fountain, C. Petteway, A. Hollingsworth, H. Grady, Low cost of ownership scalable copper direct bond interconnect 3D IC technology for three dimensional integrated circuit applications, in *2009 IEEE International Conference on 3D System Integration* (IEEE, 2009), pp. 1–6
50. P. Enquist, Metal/silicon oxide hybrid bonding, in P. Ramm, J.J.-Q.Lu, M.M.V. Taklo, Handb. *Wafer Bond* eds by (Wiley, Weinheim, Germany, 2012), pp. 261–278
51. Y.-L. Chao, Q.-Y. Tong, T.-H. Lee, M. Reiche, R. Scholz, J.C.S. Woo, U. Gösele, Ammonium hydroxide effect on low-temperature wafer bonding energy enhancement. Electrochem. Solid-State Lett. **8**, G74–G77 (2005). https://doi.org/10.1149/1.1857671
52. Q.-Y. Tong, G. Fountain, P. Enquist, Room temperature SiO_2/SiO_2 covalent bonding. Appl. Phys. Lett. **89**, 042110 (2006). https://doi.org/10.1063/1.2240232
53. L. Di Cioccio, S. Moreau, L. Sanchez, F. Baudin, P. Gueguen, S. Mermoz, Y. Beilliard, R. Taibi, Cu/SiO2 Hybrid Bonding, in P. Garrou, M. Koyanagi, P. Ramm, eds by Handb. *3D Integr* (Wiley, KGaA, 2014), pp 295–312
54. L.D. Cioccio, P. Gueguen, R. Taibi, D. Landru, G. Gaudin, C. Chappaz, F. Rieutord, F. de Crecy, I. Radu, L.L. Chapelon, L. Clavelier, An overview of patterned metal/dielectric surface bonding: mechanism, alignment and characterization. J. Electrochem. Soc. **158**, P81–P86 (2011). https://doi.org/10.1149/1.3577596
55. I. Radu, D. Landru, G. Gaudin, G. Riou, C. Tempesta, F. Letertre, L. Di Cioccio, P. Gueguen, T. Signamarcheix, C. Euvrard, J. Dechamp, Recent Developments of Cu-Cu non-thermo compression bonding for wafer-to-wafer 3D stacking, in *2010 IEEE International 3D Systems Integration Conference (3DIC)* (IEEE, Munich, 2010), pp. 1–6
56. C. Sabbione, L.D. Cioccio, L. Vandroux, J.-P. Nieto, F. Rieutord, Low temperature direct bonding mechanisms of tetraethyl orthosilicate based silicon oxide films deposited by plasma enhanced chemical vapor deposition. J. Appl. Phys. **112**, 063501 (2012). https://doi.org/10.1063/1.4752258
57. P. Gondcharton, B. Imbert, L. Benaissa, V. Carron, M. Verdier, Kinetics of low temperature direct copper–copper bonding. Microsyst. Technol. **21**, 995–1001 (2015). https://doi.org/10.1007/s00542-015-2436-4
58. P. Gueguen, L. Di Cioccio, P. Gergaud, M. Rivoire, D. Scevola, M. Zussy, A.M. Charvet, L. Bally, D. Lafond, L. Clavelier, Copper direct-bonding characterization and its interests for 3D integration. J. Electrochem. Soc. **156**, H772 (2009). https://doi.org/10.1149/1.3187271
59. A. Shigetou, T. Suga, Modified diffusion bonding for both Cu and SiO 2 at 150 °C in ambient air, in *2010 Proceedings 60th Electronic Components and Technology Conference (ECTC)* (IEEE, Las Vegas, NV, USA, 2010), pp. 872–877
60. R. He, M. Fujino, A. Yamauchi, Y. Wang, T. Suga, Combined surface activated bonding technique for low-temperature cu/dielectric hybrid bonding. ECS J. Solid State Sci. Technol. **5**, P419–P424 (2016). https://doi.org/10.1149/2.0201607jss
61. R. He, M. Fujino, A. Yamauchi, T. Suga, Combined surface-activated bonding technique for low-temperature hydrophilic direct wafer bonding. Jpn J Appl Phys 55:04EC02 (2016). https://doi.org/10.7567/jjap.55.04ec02
62. Q.-Y. Tong, J.G.G. Fountain, P.M. Enquist, Method for low temperature bonding and bonded structure. US Patent 6,902,987, 2005
63. C. Sanders, Continued adoption of low temperature direct bond technology for high volume 3D commercial applications. *3D Architectures for Semiconductor Integration and Packaging (3D ASIP)* (2012)
64. L.D. Cioccio, F. Baudin, P. Gergaud, V. Delaye, P.-H. Jouneau, F. Rieutord, T. Signamarcheix, Modeling and integration phenomena of metal-metal direct bonding technology. ECS Trans. **64**, 339–355 (2014). https://doi.org/10.1149/06405.0339ecst

65. C. Rauer, H. Moriceau, F. Fournel, A.M. Charvet, C. Morales, N. Rochat, L. Vandroux, F. Rieutord, T. McCormick, I. Radu, Treatments of deposited SiOx surfaces enabling low temperature direct bonding. ECS J. Solid State Sci. Technol. **2**, Q147–Q150 (2013). https://doi.org/10.1149/2.004309jss
66. C. Ventosa, C. Morales, L. Libralesso, F. Fournel, A.M. Papon, D. Lafond, H. Moriceau, J.D. Penot, F. Rieutord, Mechanism of thermal silicon oxide direct wafer bonding. Electrochem. Solid-State Lett. **12**, H373–H375 (2009). https://doi.org/10.1149/1.3193533
67. F. Fournel, C. Martin-Cocher, D. Radisson, V. Larrey, E. Beche, C. Morales, P.A. Delean, F. Rieutord, H. Moriceau, Water stress corrosion in bonded structures. ECS J. Solid State Sci. Technol. **4**, P124–P130 (2015). https://doi.org/10.1149/2.0031505jss
68. P. Gondcharton, B. Imbert, L. Benaissa, M. Verdier, Voiding phenomena in copper-copper bonded structures: role of creep. ECS J. Solid State Sci. Technol. **4**, P77–P82 (2015). https://doi.org/10.1149/2.0081503jss
69. P. Gondcharton, B. Imbert, L. Benaissa, F. Fournel, M. Verdier, Effect of copper-copper direct bonding on voiding in metal thin films. J. Electron. Mater. **44**, 4128–4133 (2015). https://doi.org/10.1007/s11664-015-3992-1
70. S. Lhostis, A. Farcy, E. Deloffre, F. Lorut, S. Mermoz, Y. Henrion, L. Berthier, F. Bailly, D. Scevola, F. Guyader, F. Gigon, C. Besset, S. Pellissier, L. Gay, N. Hotellier, M. Arnoux, A.-L. Le Berrigo, S. Moreau, V. Balan, F. Fournel, A. Jouve, S. Chéramy, B. Rebhan, G.A. Maier, L. Chitu, Reliable 300 mm wafer level hybrid bonding for 3D stacked CMOS image sensors. In *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)* (IEEE, 2016), pp. 869–876
71. H. Takagi, J. Utsumi, M. Takahashi, R. Maeda, Room-temperature bonding of oxide wafers by Ar-beam surface activation. ECS Trans. **16**, 531–537 (2008). https://doi.org/10.1149/1.2982908
72. F. Liu, R.R. Yu, A.M. Young, J.P. Doyle, X. Wang, L. Shi, K.N. Chen, X. Li, D.A. Dipaola, D. Brown, C.T. Ryan, A 300-mm wafer-level three-dimensional integration scheme using tungsten through-silicon via and hybrid Cu-adhesive bonding, in *2008 IEEE International Electron Devices Meeting* (IEEE, 2008), pp. 1–4
73. J.J. McMahon, E. Chan, S.H. Lee, R.J. Gutmann, J.Q. Lu, Bonding interfaces in wafer-level metal/adhesive bonded 3D integration, in *2008 58th Electronic Components and Technology Conference* (IEEE, 2008), pp. 871–878
74. Hozawa K, Aoki M, Furuta F, Takeda K, Yanagisawa A, Kikuchi H, Mitsuhashi T, Kobayashi H (2013) 3D Integration Technology using Hybrid Wafer Bonding and its Electrical Characteristics. In: 13th Int. Symp. Electron. Packag. ICEP2013. Osaka, Japan, pp 118–122
75. J.J. McMahon, J.Q. Lu, R.J. Gutmann, Wafer bonding of damascene-patterned metal/adhesive redistribution layers for via-first three-dimensional (3D) interconnect, in 55th *Proceedings Electronic Components and Technology, 2005. ECTC'05.* (IEEE, 2005), pp. 331–336
76. Z.-C. Hsiao, C.-T. Ko, H.-H. Chang, H.-C. Fu, C.-W. Chiang, C.-K. Hsu, W.-W. Shen, W.-C. Lo, *Cu/BCB Hybrid Bonding With TSV for 3D Integration by Using Fly-Cutting Technology* (IEEE, Kyoto, Japan, 2015), pp. 834–837
77. T. Sakai, N. Imaizumi, S. Sakuyama, Hybrid bonding technology with Cu–Cu/adhesives for high density 2.5D/3D integration. (IEEE, Big Island, HI, 2016), pp 1–6
78. R. He, T. Suga, Effects of Ar plasma and Ar fast atom bombardment (FAB) treatments on Cu/polymer hybrid surface for wafer bonding, in *2014 International Conference on Electronics Packaging (ICEP)* (IEEE, 2014), pp. 78–81
79. C. Okoro, R. Agarwal, P. Limaye, B. Vandevelde, D. Vandepitte, E. Beyne, Insertion bonding: a novel Cu-Cu bonding approach for 3D integration, in *2010 Proceedings 60th Electronic Components and Technology Conference (ECTC)* (IEEE, 2010), pp. 1370–1375
80. G.W. Deptuch, G. Carini, P. Grybos, P. Kmon, P. Maj, M. Trimpl, D.P. Siddons, R. Szczygiel, R. Yarema, Design and tests of the vertically integrated photon imaging chip. IEEE Trans. Nucl. Sci. **61**, 663–674 (2014). https://doi.org/10.1109/TNS.2013.2294673
81. G.W. Deptuch, G. Carini, T. Collier, P. Gryboś, P. Kmon, R. Lipton, P. Maj, D.P. Siddons, R. Szczygieł, R. Yarema, Results of tests of three-dimensionally integrated chips bonded to

sensors. IEEE Trans. Nucl. Sci. **62**, 349–358 (2015). https://doi.org/10.1109/TNS.2014.2378784
82. G.W. Deptuch, G. Carini, P. Enquist, P. Gryboś, S. Holm, R. Lipton, P. Maj, R. Patti, D.P. Siddons, R. Szczygieł, R. Yarema, Fully 3-D integrated pixel detectors for X-Rays. IEEE Trans. Electron Devices **63**, 205–214 (2016). https://doi.org/10.1109/TED.2015.2448671
83. F. Inoue, J. Bertheau, S. Suhard, A. Phommahaxay, T. Ohashi, T. Kinoshita, Y. Kinoshita, E. Beyne, Protective layer for collective die to wafer hybrid bonding, in *2019 International 3D Systems Integration Conference (3DIC)* (IEEE, 2019), pp. 1–4
84. G. Vakanas, O. Minho, B. Dimcic, K. Vanstreels, B. Vandecasteele, I. De Preter, J. Derakhshandeh, K. Rebibis, M. Kajihara, I. De Wolf, E. Beyne, Formation, processing and characterization of Co–Sn intermetallic compounds for potential integration in 3D interconnects. Microelectron. Eng. **1**(140), 72–80 (2015)
85. SiP/Heterogeneous Integration Roadmap (HIR), Materials and Emerging Research (Chapter 15), 2019 edn. http://eps.ieee.org/hir
86. K. Banerjee et al., (UCSB), CMOS-compatible graphene, (IEEE IEDM (International Electron Devices Meeting), 2018)