

Chapter 4

Microstructure and Mechanical Reliability Issues of TSV



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4.1 Introduction

Following Chap. 3 on materials, processing and assembly, this chapter discusses the microstructural and reliability issues of TSVs. This chapter begins with microstructural characterization and stress measurement; it then discusses detailed reliability issues associated with TSVs; finally it presents promising techniques towards atomistically-informed reliability modeling of TSVs.

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4.2 Microstructural Characterization and Stress Measurement

4.2.1 Microstructural Characterization

The microstructure of TSV can be characterized at four levels, i.e., crystal structure, phase structure, grain structure and defect structure. Bunge introduced a function

$$G(x) = \begin{matrix} i(x), & \text{phase} \\ g(x), & \text{orientation} \\ D(x), & \text{defects, lattice strain} \end{matrix} \quad (4.1)$$

and mathematical methods to quantitatively describe microstructure [1, 2]. For experimental characterization, standard metallographic techniques can also be applied to TSV structures. However, preparing TSV samples for microstructural characterization to investigate precise locations through the TSV sample structures using standard metallographic polishing is tedious and unpredictable due to the small size of TSVs and presence of soft materials (e.g., Cu, Ag paste, etc.) adjacent to hard and brittle Si. Focused ion beam (FIB) milling, which allows precise machining at small length scales, is widely used for preparing TSV samples for microstructural characterization. FIB can also be used to prepare ultra-thin samples, suitable for observation under transmission electron microscope (TEM). Machining samples using FIB is both a slow and an expensive process. Emerging Xe⁺ plasma FIB systems, with optimized control over milling parameters, promise faster removal rates [3]. Another method for characterization of the microstructure of filler material is by via revealing: in this process, Si is wet-etched using hydroxides, which do not affect metal fillers, thus revealing the pillar [4, 5]. However, this is also a slow process and it does not allow observation of the Si-filler interface. Therefore, sample preparation, especially over the entire height of the TSV, for microstructural characterization is often very slow. The important microstructural features of TSV assemblies that are often characterized and quantified are the size and shape of filler grains, micro-texture and grain orientation, the presence of twin boundaries in Cu fillers, shapes and sizes of voids or cavities in the filler, micro-cracks, interfacial structure, etc.

Grain size, which can be measured using scanning electron microscope (SEM) and TEM, is important for the estimation of the strength of the metal filler (generally, the smaller the grain size, the greater the strength of the material). The hardness and hence strength of the TSV fillers can be measured using nano-indentation. Interestingly, as shown in Fig. 4.1, nano-indentation studies have shown that TSV fillers with smaller grain size may not always show an enhanced strength. Furthermore, as also shown in Fig. 4.1, the strength versus grain size behavior often does not follow the Hall-Petch relationship; in other words, the increase in the strength is not strictly proportional to the inverse of the square root of the grain size [6, 7]. These deviations can be attributed to the fact that TSV fillers contain relatively few grains across the via-diameter, as

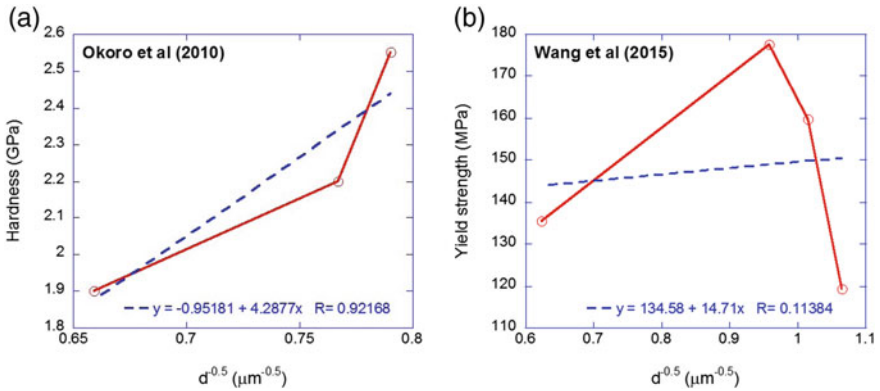


Fig. 4.1 Variation of (a) average hardness and (b) yield strength of filler material with average grain size of Cu. The broken line shows the best curve fit using Hall-Petch type of relationship between hardness in a and yield strength in b and the inverse of the square root of grain size. The data for (a) and (b) are taken from Refs. [6, 7], respectively

shown in Fig. 4.2, and hence do not display generalized polycrystalline behavior. It has been shown that electrolytes with impurities can enhance the yield strength of the fillers [15]. Therefore, attention should be paid to the methods used to estimate the mechanical behavior of TSVs [8, 9]. In addition, the conventional parameter of an average grain size may not be sufficient to characterize the grain structure of TSV fillers. In the current materials genome initiative [10], new methods that consider

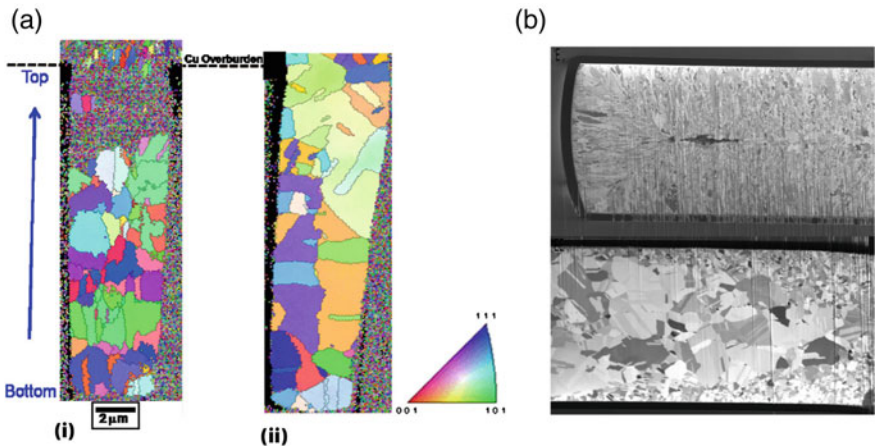


Fig. 4.2 (a) Electron back scatter diffraction (EBSD) patterns showing inverse pole figure (IPF) maps of cross-section of Cu fillers: (i) as-deposited and (ii) after annealing at 420 °C for 20 min followed by annealing at 300 °C for additional 15 min [6]. (b) FIB micrographs showing grain structure of Cu filler: (i) as-deposited and (ii) after annealing at 400 °C for 1 h [13]

more parameters including phase morphology and distribution have been proposed for quantification of microstructure [11, 12].

Figure 4.2 shows that the grain size of the Cu via-filler increases significantly upon annealing at elevated temperatures [6]; for example, annealing at 450 °C for 30 min leads to an increase in the grain size from 0.84 to 1.26 μm [14]. However, as shown in Fig. 4.2b, the grain growth during annealing is often inhomogeneous [13]. Furthermore, impurities in the filler material slow down the grain growth during annealing [15]. Electroplating at lower current density may lead to fillers with large grain size; for instance, plating current densities of 1 and 9 A/cm^2 resulted in Cu fillers with average grain sizes of 2.57 and 0.88 μm , respectively [7]. Annealing has also been noted to induce twinning in Cu fillers [6, 16].

The micro-texture of TSV fillers is often measured by electron back-scattered diffraction (EBSD) conducted in SEM (see Fig. 4.2a). However, if the filler grains are very small, as found in the seed layer, diffraction-scanning transmission electron microscope (D-STEM) can also be used to map the micro-texture [17]. It has been noted that although annealing increases the grain size, it does not have any other noticeable effect on the texture of the filler material [6]. The micro-texture of filler materials appears to depend on the orientation of the seed layer, electroplating conditions, e.g., current density, bath chemistry, bath temperature, etc., impurity concentration, etc. [17]. However, to date, the dependence of the crystallographic texture of the via-filler on various process and geometrical parameters has not been unambiguously determined.

The general microstructural characterization techniques, such as STEM, energy dispersive X-ray spectroscopy (EDXS), electron probe microanalysis (EPMA), etc., can be used to identify the chemical species in TSVs and map their concentration profile. Time-of-flight secondary ion mass spectrometry (TOF-SIMS) may also be used to study the chemical species in TSVs [15]. X-ray diffraction (XRD) can also be used to identify the phases present in the TSV structures [18].

4.2.2 Measurement of Stress State

Substantial stresses are produced in the TSV assemblies, as a result of processing and during thermal cycling. The sources and implications are discussed in Sect. 4.3. These stresses affect the overall reliability of microelectronic packages comprising these TSV structures, and therefore various approaches have been utilized to understand the nature of these stresses. Three main techniques that been used to measure the stress state in TSVs are briefly discussed below.

4.2.2.1 Wafer Curvature Method

If a layered assembly of two or more materials having different coefficient of thermal expansion (CTE) are joined together and then heated, the assembly bends with a

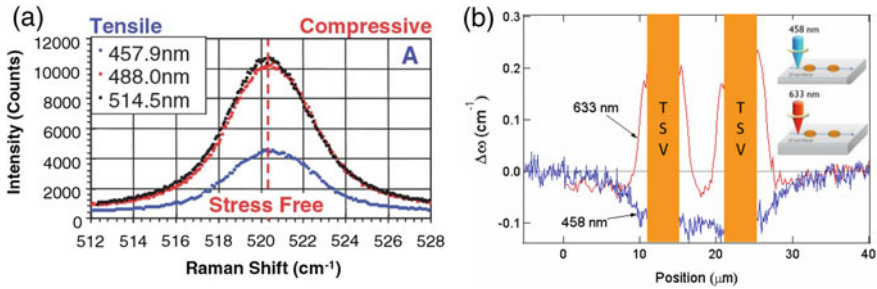


Fig. 4.3 (a) Representative Raman spectrum of Si wafer using lasers with wavelengths of 457.9, 488.0, and 514.5 nm, showing correlation between shift and stress [24]. (b) Measured stress profiles at different depths of the Si wafer near Cu-TSVs, using two different wavelengths of laser beams [25]

curvature proportional to the in-plane stresses generated in the individual components [19]. Although TSV assemblies are more complex, they also bend due to generation/relief of residual stresses during thermal excursions [15, 20–22], and measurement of the curvature of the wafer can be used to determine stresses in the TSVs. However, the stress state in TSV structures is more complex than simple film-substrate systems, and as such, stress analysis based on the curvature method has usually been supplemented by FEA [21]. Although this method is meant to provide only an overall or average stress (as only one curvature is measured), FEA may be used regressively to predict the 3-D state of stress. Moreover, this method can be easily adapted for in situ measurement of stress (e.g., during thermal cycling).

4.2.2.2 Micro-Raman Spectroscopy

Since Si is Raman-active, the stress in the Si wafer can be measured using micro-Raman spectroscopy (μ RS) [20, 23–25]. The most common case involving usage of μ RS in backscatter mode resolves the longitudinal vibrational mode (i.e., mode 3), which can then be used to determine the sum of the two in-plane principle stresses [23, 25]. However, if a high numerical aperture (NA) (say, ≥ 0.4 [23]) is used, then it is possible to resolve all three modes of vibration and hence tensorial nature of the stresses in TSV structures [23]. As shown in Fig. 4.3a, compressive and tensile stresses in Si lead to forward and backward shifts in the Raman signal (e.g., a shift by a wavenumber of 1 cm^{-1} corresponds to a stress of $\sim 434 \text{ MPa}^1$), the shift being directly proportional to the stress in Si [24]. Since a laser beam with long wavelength can penetrate deeper in Si, it can provide information from a deeper depth than a beam with a longer wavelength, and thus, depth-sensitive information can be obtained.

¹It should be noted that the exact value of the stress for a wavenumber shift may depend on the materials properties used in secular equation (i.e., set of equations in the reference axes which may be different than that of materials crystallographic reference system). It can lie in the range of 430–520 MPa [25].

Nevertheless, the penetration depth of μ RS in the backscatter configuration is still very small and hence this method can be used to obtain stress information from near surface regions only. As shown in Fig. 4.3b, the stress in Si around a TSV strongly depends on the distance from the via-end: at very near the surface (as measured using short wavelength laser), the stress becomes less tensile away from the via end, whereas at slightly below depth (as measured using long wavelength laser), the stress transitions from being compressive to tensile as one moves away from the via end. Since the stress-state in the Si wafer is generally tri-axial, it is challenging to measure all stress-components via Raman spectroscopy. Nevertheless, by combining with FEA, μ RS has been utilized to yield good estimates of the three-dimensional stress state in the wafer [23–25]. It should be noted that metals are not Raman-active and therefore the stress state of Cu cannot be measured using this technique and has to be derived indirectly from measurements on Si.

4.2.2.3 X-Ray Diffraction (XRD) Based Techniques

To directly measure the localized strain, and hence the stress-field in Cu TSVs, X-ray diffraction, used in conjunction with a cross-section TEM or a synchrotron radiation source, may be used to determine stress-induced changes in unit cell parameter from the equilibrium [26–28]. This can also be used to measure stress in Si non-destructively with very high resolution. Although XRD typically yields only average stress values, by focusing high energy X-rays in a synchrotron to a small beam size and rastering it on the sample, full strain and stress tensors from submicrometer sample volumes in the TSV structures may be obtained [26, 29–31]. Figure 4.4 shows an example of spatially resolved stress variation in a TSV assembly, determined using high energy X-rays.

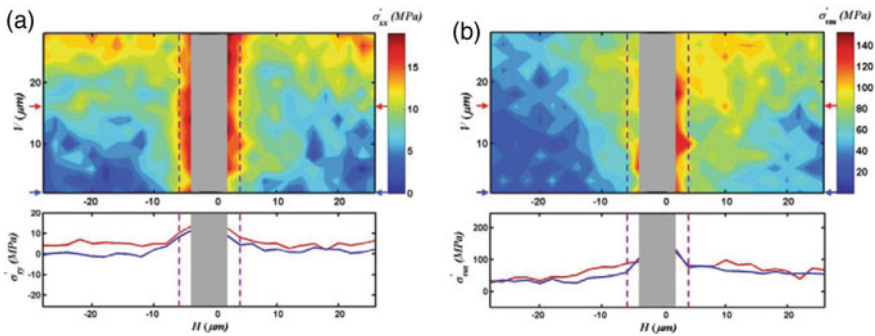


Fig. 4.4 Stress distribution on a plane as determined using synchrotron x-ray micro-diffraction: (a) the deviatoric σ_{xx} and (b) von-Mises stress [26]. The dotted vertical lines represent the effective size of the Cu TSV whereas the grey shaded region represent “non-indexable” region where the diffracted intensities from Cu are comparable with that from Si

4.2.2.4 Stress Metrology Challenges

Although the synchrotron X-ray micro-diffraction is by far the most powerful technique for stress analysis, it is the most expensive and requires access to a synchrotron radiation source [28]. None of these aforementioned techniques can directly measure stress in Si or Cu. In Raman spectroscopy phonon frequency shifts are converted into stress values [28]; in diffraction-based techniques strain tensors are mathematically converted to stress tensor using linear elastic properties of bulk single crystalline samples [28]. Although μ RS can provide stress profiles in the depth direction, the penetration depth is within a submicrometer range. Therefore, the complete picture of the stress distribution in TSVs is still unavailable. However, this information is critical to elucidate the root cause for the metal pumping phenomenon as discussed in Sect. 4.3.1.3. The modeling techniques discussed in Sect. 4.4 may provide a solution towards this direction.

4.3 Reliability Issues Associated with TSVs

Reliability complications in TSVs typically arise either from stress-related or electrical sources, and are often convoluted with microstructural effects. In the following, we discuss the cause and effects of each of these reliability issues, along with potential approaches to circumvent or minimize these.

4.3.1 Stresses in TSVs

4.3.1.1 Origin and Effect of Stresses

Stresses in TSVs, and therefore in the neighboring Si, arise from two sources: (i) growth stresses, that arise as a result of via-filling by electroplating, and (ii) thermo-mechanical stresses that arise due to thermal expansion mismatch between Cu in the via and the surrounding Si.

Growth stresses arise when the electrodeposited Cu grows radially inwards on the Cu-seed layer from the via side-walls, and abut itself, often resulting in a seam along the TSV axis. Such a seam may leave a thin void-line along the TSV axis (Fig. 4.5), which can grow during post-deposition annealing, and result in mechanical and electrical performance loss. Electroplated copper undergoes significant grain growth by self-annealing at room temperature, which results in volume shrinkage of the Cu TSVs by elimination of grain boundaries [32]. This may allow any existing void to grow during both self-annealing, as well as during the pre-CMP (chemical-mechanical polishing) annealing step. During annealing, hydrostatic stress gradients generated around pre-existing defects in the Cu may be relieved by diffusion of lattice vacancies towards the existing void near the axis, causing the void to grow [33].

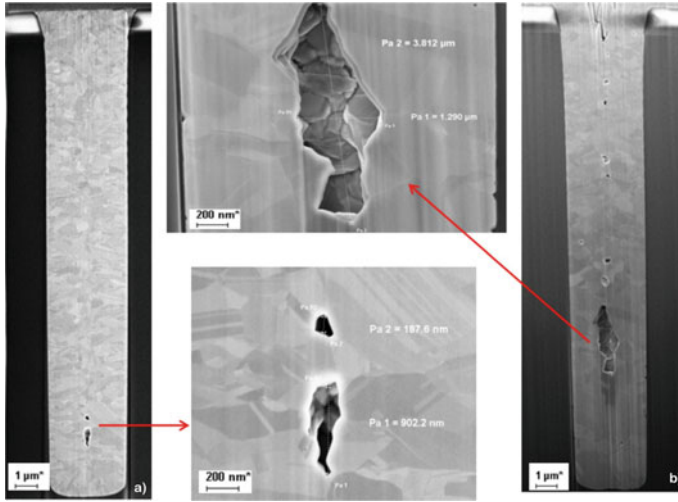


Fig. 4.5 SEM images of TSVs showing centerline void after annealing at 150 °C (a) and 300 °C (b) [33]

Thermo-mechanical stresses arise because of differential thermal expansion or contraction of Cu and Si during heating or cooling of the device as a result of their large difference in the CTE ($\alpha_{Si} = 2.8 \times 10^{-6}/K$, $\alpha_{Cu} = 17 \times 10^{-6}/K$). Thermal cycling resulting from fluctuating Joule heating occurs continually during the service life of electronic devices, and 3D devices are no exception. Typically, electroplated Cu deposited on Si is under residual tension to begin with (at ambient temperature). During heating, the tension is first elastically relieved, following which a compressive stress builds up. As temperature increases, the yield strength and creep resistance of Cu decrease, resulting in stress relief by plastic yielding and creep, such that at the highest temperature, there is little stress remaining (Fig. 4.6). During subsequent cooling, a tensile stress builds up, resulting in stresses in the neighborhood of 200–500 MPa (biaxial for thin films and hydrostatic for TSVs). Further cycling repeats the same behavior, although because of substantial plasticity during the first cycle, the yielding and stress-relaxation start at a higher temperature, and are therefore lower. This is shown for a Cu film on Si, measured by wafer curvature testing, in Fig. 4.6 [34]. The details of this behavior depend on the temperature range and rate of thermal cycling, but the overall behavior is qualitatively replicated in TSVs. In contrast to thin films, however, the TSV stress-state is triaxial, and the TSV is typically in triaxial (i.e., hydrostatic) tension at ambient temperature.

As noted earlier, the stress state in Cu-TSVs may be studied either by measuring the stress in Si via Raman spectroscopy, or that in Si or Cu by X-ray microdiffraction. Depth-sensitive Raman measurements, using various excitation wavelengths of an Ar⁺ laser, show that Si surrounded by TSVs has a compression hydrostatic stress at ambient temperature, with the stress varying significantly along the length of the TSV [24, 25]. The hydrostatic stress in Si becomes less negative nearer the ends

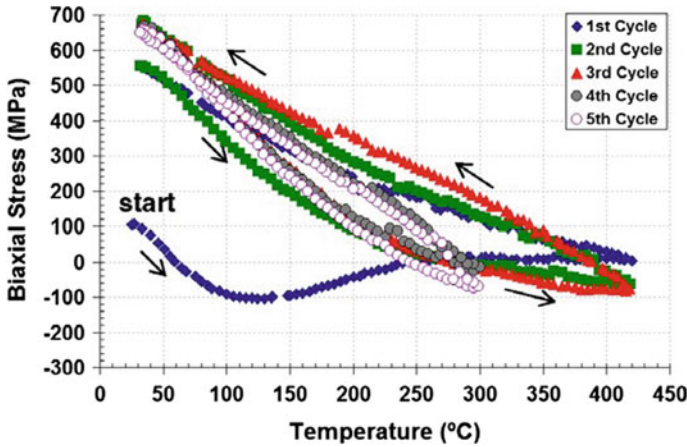
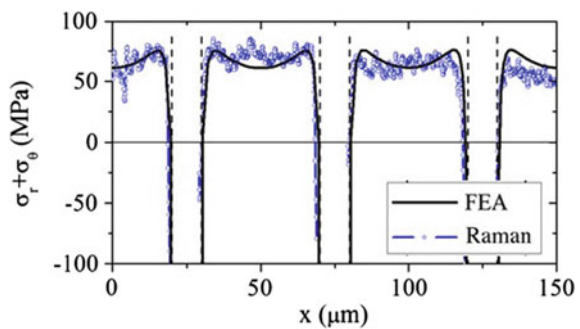


Fig. 4.6 Evolution of equibiaxial stress in a blanket Cu film deposited on Si during thermal cycling [34]

of the TSV. Assuming that the radial and circumferential stresses (σ_{rr} , $\sigma_{\theta\theta}$) in the Si surrounding the TSVs are either weakly or not dependent on the axial position relative to the TSVs, one may infer that at ambient temperature, the axial stress σ_{zz} in Si is negative (i.e., σ_{zz} is positive in Cu) near the middle of the TSV, and becomes ~ 0 at the surface. It was also noted that the stress-variation along the depth is larger for smaller TSV diameters (i.e., larger TSV aspect ratios). Furthermore, the stress in Si surrounded by an array of TSVs is typically larger than that outside of TSV-arrays, and these stresses change from tensile immediately after Cu electrodeposition (where the stress is due to growth and self-annealing), to increasingly compressive when annealed at increasing temperatures [35]. Raman peak-shift measurements near the surface of the chip next to TSV-ends show that the biaxial hydrostatic stress state (i.e., $[\sigma_r + \sigma_\theta]/3$, since $\sigma_z \sim 0$) is negative at the TSV-chip interface, and rises sharply and becomes positive mid-way between TSVs (Fig. 4.7). After annealing, the hydrostatic stress in Si becomes even more compressive at the interface due to

Fig. 4.7 Plot of the stress state in Si near the ends of TSVs. Three TSVs are shown, each as a vertical band with intervening Si [20]



Cu volume expansion, and more tensile away from the interface [20]. Conversely, in addition to increasing the grain size, annealing lowers the compressive stresses in the Cu.

Thermal cycling also leads to accumulation of hydrostatic stress in Cu TSV or filler [27]. In addition, TSVs with high impurity levels appear to lead to high residual stresses [15]. It has been reported that large tensile radial stresses exist at the Si–Cu interface [25]; this may make these sites prone to failure in TSV assemblies. The radial stress at the Cu-filler/Si interface generally increases with the length of the TSV for a given diameter [25]. The TSV diameter also seems to affect the stress state in the TSV assembly, although the dependence of the hydrostatic stress on TSV diameter is not monotonic [36].

The stresses induced near the surface of Si next to the Cu-filled TSVs have an adverse impact on the electrical performance of devices in the immediate neighborhood of the TSVs due to induced piezoresistivity, which results in degradation of carrier mobility [37, 38]. This necessitates a keep-out zone (KOZ) in the Si, typically a few micrometers in width, in the immediate vicinity of each TSV, where active devices cannot be placed. The KOZ, which scales with the square of the TSV diameter, is also greater for high aspect-ratio TSVs, and places a significant overhead on the area available in the chip for active devices, particularly with the increasing density of TSVs in chips. Based on FEA of the stress-state in Si next to TSVs, it has been inferred that Cu microstructures with smaller yield strengths reduce the KOZ size, which increases with increasing yield strength until the via yields plastically, and then remains stable [39].

FEA of TSVs in free-standing chips shows that after both heating and cooling, maximum von Mises stress, and hence plastic deformation of the copper occurs near the interface close to TSV-ends, which is a root cause of copper-pumping [40]. It is further observed that the maximum principal stress (tensile) is in the radial direction at the interface near the middle of the TSV, and in the circumferential dielectric layer surrounding the TSV [41]. Evidence of dielectric cracking at the circumferential Cu–SiO₂–Si interface, as well as roughening (due to voiding) of the metal-line at the top of the TSV has been noted after thermal cycling, as shown in Fig. 4.8 [42].

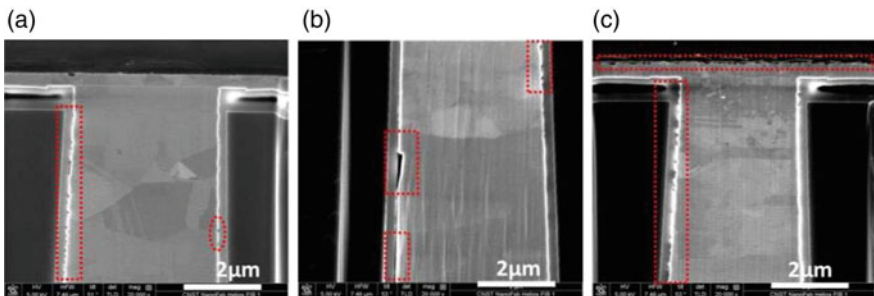


Fig. 4.8 TSV (a) prior to cycling, and after (b) 500 and (c) 2000 cycles between 30 and 150 °C, showing development of dielectric cracks and top-line roughening [42]

However, FE analysis of a stacked-die package shows that each die undergoes convex curvature when the package is cooled from the stress-free temperature (150 °C), which fundamentally alters the stresses and displacements relative to the free standing die [41]. The convex curvature alters the radial interfacial stress to compressive, reducing the proclivity towards interfacial fracture as well as dielectric cracking, and shifting the critical failure location to the copper-pillar near the solder-microbump interface in 3D packages [41]. In fact, the failure probability near the silicon–Cu pillar-microbump junction (as indicated by the maximum equivalent strain), as well as the required KOZ diameter, increase with increasing diameters of both the TSV and the copper-pillar in a 3D package [43].

In addition to producing defects (e.g. voids) in TSVs, including complications in electrical performance and potentially causing interfacial and or dielectric fracture, induced stresses also give rise to a plasticity-related phenomenon commonly referred to as copper-pumping, which can have serious reliability implications. Because of the pervasiveness of this phenomenon, it is discussed separately in Sect. 4.3.1.3.

4.3.1.2 Microstructure and Stresses

Direct measurement of stresses in Cu-TSVs with X-ray micro-diffraction reveal a significant tensile hydrostatic stress (~ 234 MPa) at room temperature, which goes to compression (-196 MPa) during annealing at 200 °C, and becomes a smaller tensile stress when the sample is cooled to the ambient (167 MPa). The large initial tensile stress is caused by grain boundary elimination during self-annealing and device fabrication, and as noted previously, is undesirable from the reliability perspective, since this causes large stresses in Si. A subsequent annealing treatment lowers the tensile hydrostatic stress in Cu, even though the zone of initially larger grains expands during annealing, as shown in Fig. 4.9 [29], possibly because of relaxation associated with plasticity and creep at the high temperature.

EBSD studies have shown that during annealing, large grains remain stable when there is a preponderance of $\Sigma 3$ twin boundaries, but grains without twins and smaller grains grow rapidly [44]. It has also been noted that the Cu-TSV has random texture both before and after annealing. However, microvoids or small cracks have been noted to form during annealing, thereby reducing stress, as shown in Fig. 4.10. This is possibly because of vacancy diffusion to pre-existing defects under hydrostatic stress gradients within the TSV during annealing, as noted in the discussion associated with Fig. 4.5.

FEA based modeling work has also reported the linkage between the microstructure of copper grains and the stress in Cu-TSVs. The results from a linear elastic mechanical model clearly demonstrate that the stress distribution is rather heterogeneous inside the TSV filler, as show in Fig. 4.11, considering the anisotropy of the elastic compliance tensor of copper. Depending on the texture, morphology and distribution of the copper grains, stress concentrations may occur at the grain boundaries [45]. Elastoplastic models have also been conducted directly on copper grain structures with the aim of explaining the formation of copper-pumping [46, 47]. However,

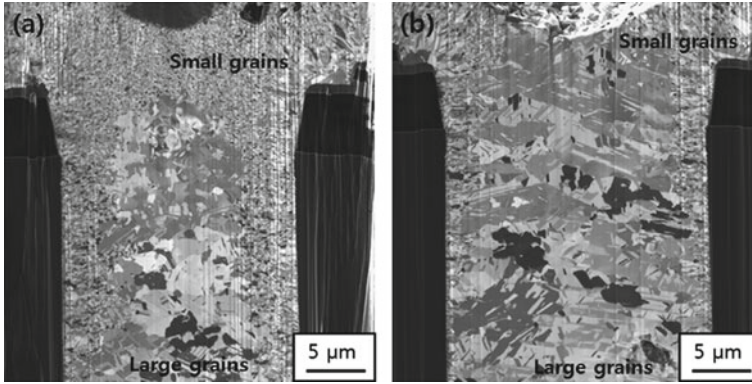


Fig. 4.9 Cross sections of Cu-filled TSVs in: (a) the as- received state, showing a zone of large grains in the center surrounded by smaller grains; and (b) after annealing, showing an expanded central zone with large grains [29]

the drawbacks of this kind of model is clear. First, although the mechanical analysis is conducted directly on copper microstructure, the microstructure is assumed to remain unchanged during the mechanical loading process. Second, the plastic deformation mechanisms at the atomic scale, e.g. the motion of dislocations, have not been considered. However, the dislocation involved processes such as recovery, recrystallization and grain growth have been reported to occur in electrodeposited copper and can significantly influence its mechanical properties [48]. Recrystallization has also been suspected to account for the copper-pumping phenomenon [15, 36, 49]. Considering the limitation of the current modeling techniques, more robust simulation methodologies that take into account the polycrystalline nature of Cu TSVs and their complex deformation and stress relaxation mechanisms are needed [36]. Section 4.4 will introduce atomistically-informed modeling techniques to address this limitation.

4.3.1.3 Metal Pumping: Extrusion or Intrusion of TSVs

During service and consequent thermal cycling, the CTE mismatch between Cu and Si results in residual stresses in each material (σ_{Cu} , σ_{Si}), as well as significant interfacial shear stresses (T_i) near the extremities of the via. The induced stresses, if high enough, may cause plastic deformation of the filler [39, 47, 50, 51] with the differential straining between Cu and Si sometimes accommodated by interfacial sliding [52–54]. This results in extrusion (and sometimes, intrusion) of Cu relative to the Si. Generally, the extrusion of the Cu occurs due to plastic deformation of the metal near the via-ends (typically, towards the top or mouth of the via), and can be enhanced by creep and grain boundary sliding. Two examples of this phenomenon are illustrated in Fig. 4.12.

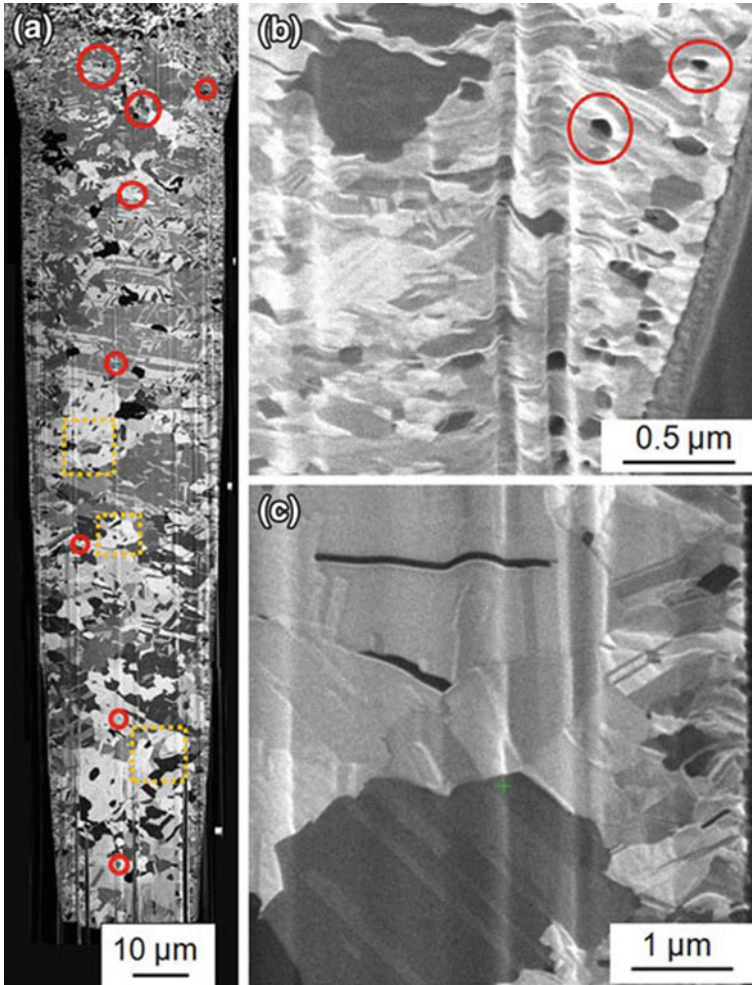


Fig. 4.10 (a) Voids and cracks form at various locations in a TSV after annealing (red circles). (b) Voids near the top of the TSV, and (c) grain boundary cracks near one of the side-walls [44]

When heated up relatively rapidly and kept at a constant elevated temperature for a period, the protrusion observed is generally associated with plastic deformation of the copper, with no relative displacement observed at the interface between Cu and Si, as observed in Fig. 4.12. Generally, the extrusion increases with increasing temperature, and occurs during any pre or post-CMP annealing, as well as heating associated with dielectric-deposition for fabricating the back end of line (BEOL) or redistribution layer (RDL). FEA shows that following heating to a high annealing/fabrication temperature (425 °C) and cooling down, the Von Mises stress exceeds the yield strength over the entire upper part of the TSV, resulting in yielding of the top part of the via (Fig. 4.13a). As a result, inelastic (plastic and creep) strains accrue in the top

Fig. 4.11 Distribution of the von Mises stress in a Cu-TSV structure from a linear elastic mechanical model with Cu grain microstructure [45]

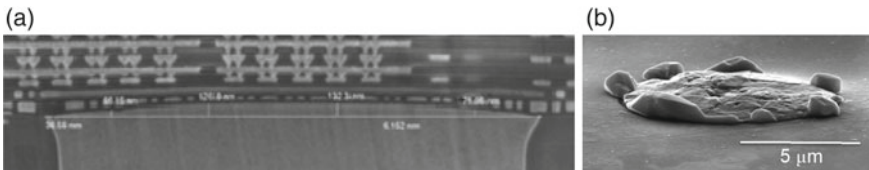
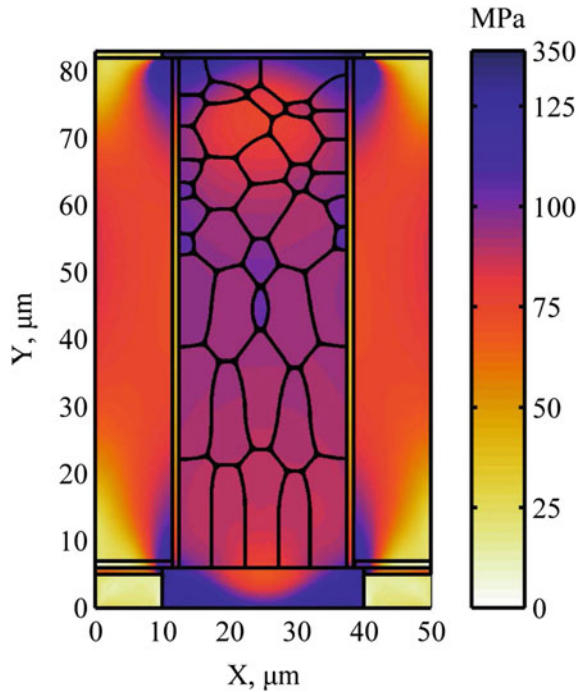


Fig. 4.12 Examples of Cu pumping. (a) Uniform pumping, showing a cross-sectional image displaying curvature of the top of a TSV, resulting in deformation of the RDL structure above [50]; (b) non-uniform pumping showing a few Cu grains protruding out of the Si surface [54]. The sample in (a) was annealed at 400 °C for 60 min, and the sample in (b) was annealed at 425 °C for 90 min

part of the via, with strain concentrations adjacent to the interface near the TSV-end (Fig. 4.13b, c). This accrual of plastic and creep strain at the top of the TSV leads to copper pumping, or protrusion of the Cu from the top. This is particularly acute for blind vias, where any expansion of the Cu must necessarily occur at the open end of the via.

EBSD studies show that Cu grains in a TSV typically have random grain boundary misorientations, and the via has little crystallographic texture, and no correlation between orientation and extruded grains has been noted [44]. This is evident from Fig. 4.14, which clearly shows a random texture in the TSV. It has been suggested that the protrusion observed is uniform when the grain size near the TSV ends is

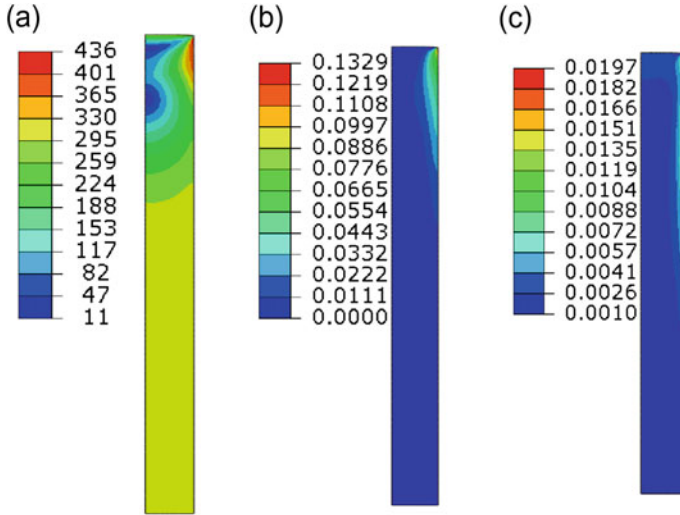
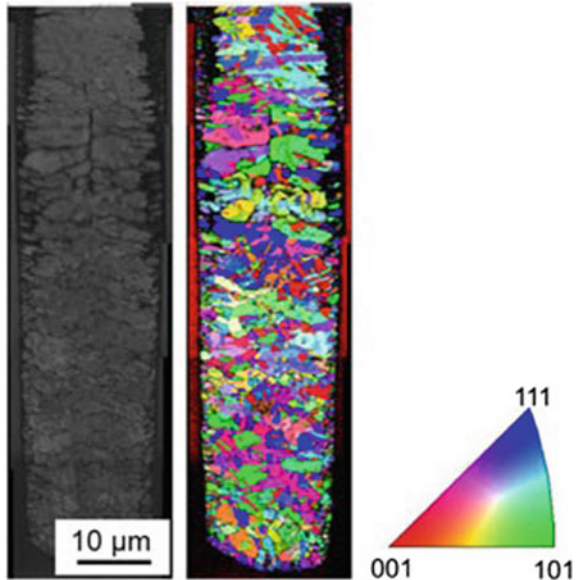


Fig. 4.13 Von Mises stress in MPa (a), and equivalent plastic (b) and creep strains (c) in a Cu-TSV following fabrication at 425 °C and cooling to -25 °C (prior to thermal cycling). The figures show one quadrant of the TSV, with the interface at the right, the axis of the TSV at the left, and TSV mid-plane at the bottom. Although the plastic strain plot highlights only the strain concentration near the interface, most of upper part of the TSV, where Von Mises stress > ~250 MPa, has yielded

Fig. 4.14 EBSD orientation map of a TSV, showing a random grain texture [44]. This is typical of most TSV structures reported in the literature



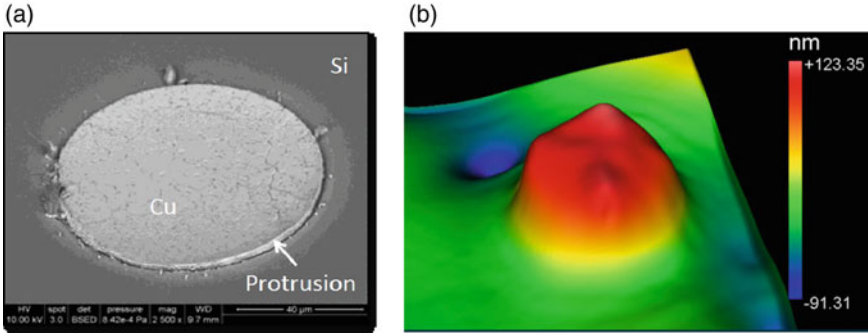


Fig. 4.15 Evidence of relative displacement between Cu and Si at the interface. (a) SEM image of Cu protrusion in an 80 μm diameter via, and (b) scanning white light interferometry image of Cu protrusion in a 10 μm diameter via. In both, the majority of protrusion occurs at the interface [54]

large, but non-uniform when there are smaller grains near the TSV ends [47]. In general, it is noted that the extent of protrusion is larger when there are high angle grain boundaries at the TSV ends that promote creep processes, but not when there are coherent twin boundaries [55].

It is useful to note that for adherent Cu–Si interfaces, when TSVs undergo uniform protrusion, the top of the Cu typically attains a convex curvature, as shown in Fig. 4.12a, with minimal or no relative displacement between the Cu and Si (or the barrier layer) at the interface. This is particularly true when the die is either cycled rapidly, or held at a constant temperature. On the other hand, when the die is cycled slowly, shear stresses are repeatedly generated and relieved at the interface near the ends of the TSV, allowing sufficient time to drive diffusively accommodated interfacial sliding, which results in a significant, step-like interfacial displacement [52–54], as illustrated in Fig. 4.15.

Diffusively accommodated interfacial sliding at hetero-interfaces (i.e., interfaces between dissimilar materials) is akin to grain boundary sliding, and may be driven by interfacial shear stresses (T_i) that occur at the extremities of a TSV. In addition, it may be enhanced or mitigated by an electric current flowing through the TSV due to associated electromigration along the interface. The resultant displacement rate is given by [57–59]:

$$\dot{U} = \frac{8\Omega\delta_i D_i}{kTh^2} \tau_i = \frac{4\delta_i D_i}{kTh} Z^* e E \quad (4.2)$$

where Ω is the atomic volume, h is the roughness of the topographically periodic interface, k and T are the Boltzmann constant and temperature, respectively, D_i is the interfacial diffusion coefficient, δ_i is the thickness of the interfacial region, and Z^* and e are the effective charge number of the diffusing ion and the charge of an electron, respectively. Thus, \dot{U} depends linearly on both T_i and the electric field E (which equals j , where $\rho =$ resistivity of the filler and j is the current density), the relative signs of which determining whether they augment or mitigate each others

contributions. In Eq. 4.2, the first term gives the effect of shear stress, while the second term gives the impact of superimposed electromigration (EM). Since Z^* is negative, the second term (due to EM) acts against the first term (due to stress-driven creep) when both driving forces (T_i and E) are positive, and thus reduce the interfacial sliding rate. Conversely, if T_i and E have opposite signs, the two terms in Eq. 4.2 augment each other and increase the interfacial sliding kinetics. Figure 4.15 shows the effect of interfacial sliding due to T_i only (i.e., when $E = 0$), and Fig. 4.16 schematically shows the origin of T_i in through and blind vias after a thermal excursion. The impact of superimposed current on interfacial sliding is discussed separately, in conjunction with electromigration in Sect. 4.3.2.

In through-vias, the interfacial shear stress generated after cooling from the fabrication temperature is symmetric about the length of the via and is concentrated at both ends. As a result, the interfacial sliding, and hence copper-extrusion, would also be symmetric at the two ends for straight (i.e. untapered) vias. For blind-vias, the interfacial shear stress rises from the blind end towards the open end, and therefore, the resultant protrusion at the open end is greater. It should be noted that interfacial sliding, which occurs due to interfacial diffusion under the applied shear stress, is a mechanism that accommodates differential deformation of the Cu and Si at the

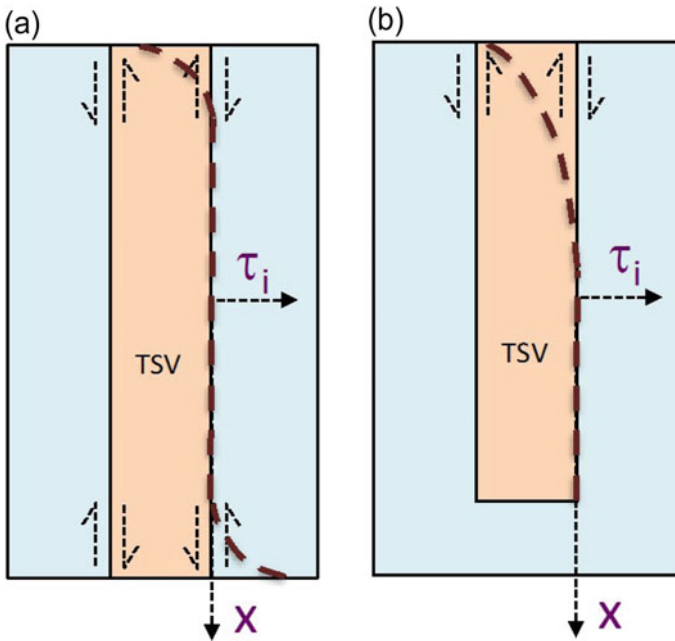


Fig. 4.16 Schematics showing shear stress distribution at the TSV-Si interface in **a** through-via, and **b** blind-via. The interfacial shear stress (dashed line) is symmetric about the length of the TSV for the through-via **(a)**, and is non-zero only near the TSV-ends. T_i is zero at the blind-end of the via in **(b)**, and rises monotonically towards the open end

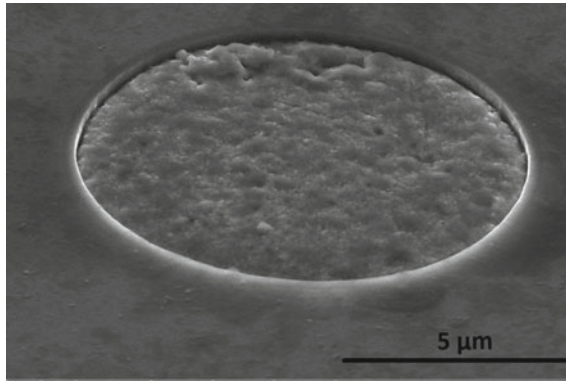


Fig. 4.17 The end of a TSV intruding into the Si, following 5 thermal cycles from -25 to 150 °C at 0.1 °C/min. Prior to cycling, the TSV end protruded out by ~ 30 nm from the Si surface

interface and therefore a thermal excursion as well as a high enough temperature and sufficient time to make diffusional processes active are needed. This is why, under rapid cycling conditions, Cu pumping typically occurs uniformly due to inelastic deformation of Cu without significant contribution from interfacial sliding, whereas when cycled slowly over a larger temperature range, steps emerge due to sliding at the interface.

Since CTE of Cu is much larger than that of Si, when cooled from an elevated temperature, significant relative shrinkage of Cu can occur, which can also be accommodated at the interface by sliding. In this case, instead of protrusion, the ends of Cu vias may intrude into the Si with a sharp step at the interface, as illustrated in the SEM image in Fig. 4.17. Again, the shrinkage is due to deformation of the Cu, but the interfacial step is due to diffusionally accommodated interfacial sliding. It should be noted, however, that the rate of protrusion or intrusion of the via-ends during thermal cycling decreases with increasing number of cycles, as the stresses generated in the metal filler reach saturation due to progressive strain hardening. Therefore, after several cycles, protrusion/intrusion due to Cu pumping levels off [52–54].

Since the ends of a TSV are typically connected to a RDL or BEOL layer, protrusion or intrusion of the Cu via poses a significant risk to the integrity of these layers. Distortion of the RDL/BEOL structures, as shown in Fig. 4.12a, or delamination of a capping layer at the end of the TSV, as shown in Fig. 4.18 due to stresses associated by even a small protrusion of the via ends, can pose serious reliability challenges. Because of the potentially serious reliability complications, the role of Cu pumping has been widely studied, and the effects of various process parameters such as TSV spacing, diameter, Cu overburden after electroplating, and annealing conditions have been noted [50]. Generally, a majority of Cu-pumping is noted to be uniform or global (~ 10 – 30 nm protrusion), with relatively few TSVs showing extrusion of individual grains after a high temperature anneal. Spacing appears to

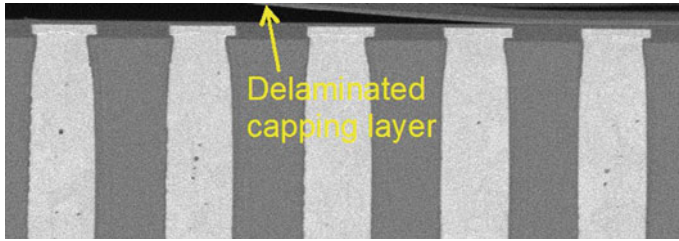


Fig. 4.18 SEM micrograph showing delamination of the capping layer at the top of a row of TSVs following thermal excursions

have little if any effect, but the pumping is greater on average for larger via diameters [50, 56]. However, although the average protrusion of an array of TSVs is larger for larger TSVs, the maximum copper pumping appears to be independent of the TSV diameter, which suggests that TSV diameter has little effect on BEOL reliability [56]. Copper overburden typically has no effect, but a higher pre-CMP annealing temperature (~ 430 °C) reduces pumping. Finally, an additional annealing step, following pre-CMP anneal, reduces pumping significantly [50].

Recent work has demonstrated that the surface relief that is often seen on the end-surface of the TSVs after thermal cycling (e.g., Figure 4.12b), is associated with grain boundary sliding along incoherent $\Sigma 3$ boundaries of the copper [60]. As noted earlier, EBSD typically reveals no strong preferred orientation (texture) in the Cu-TSV, along with the presence of numerous high angle grain boundaries. In particular, the presence of $\Sigma 3$ boundaries (both coherent and incoherent) are particularly prolific in the electroplated Cu TSVs. However, the incoherent $\Sigma 3$ boundaries with misorientations of $\sim 59^\circ$ (e.g., the boundaries between B and C, C and D, and D and E in Fig. 4.19) are the ones susceptible to sliding because of their high interfacial energy [60]. The coherent $\Sigma 3$ boundaries, which have much lower energy, do not slide. This implies that if the electroplating process for TSVs can be controlled to yield only coherent $\Sigma 3$ boundaries near the top surface, copper-pumping due to boundary sliding can be largely eliminated.

4.3.1.4 Heating Rate Dependence of Copper Pumping

The extent and mechanisms of copper-pumping during thermal cycling depend on the heating/cooling rate, as well as the range of temperatures over which the package is thermally cycled. The influence of heating rate during in situ heating has been reported [60] on dies with 200 μm pitch TSV arrays, where the samples were rapidly heated at a rate of 0.1 °C/sec to 300 °C, and then heated further to 425 °C at various heating rates.

No change in the TSV surface occurs up to 300 °C, but during holding at 425 °C for 90 min, the existing surface features start protruding. As shown in Figs. 4.20 and 4.21, little change occurs during holding at 425 °C following heating at 0.02 °C/sec;

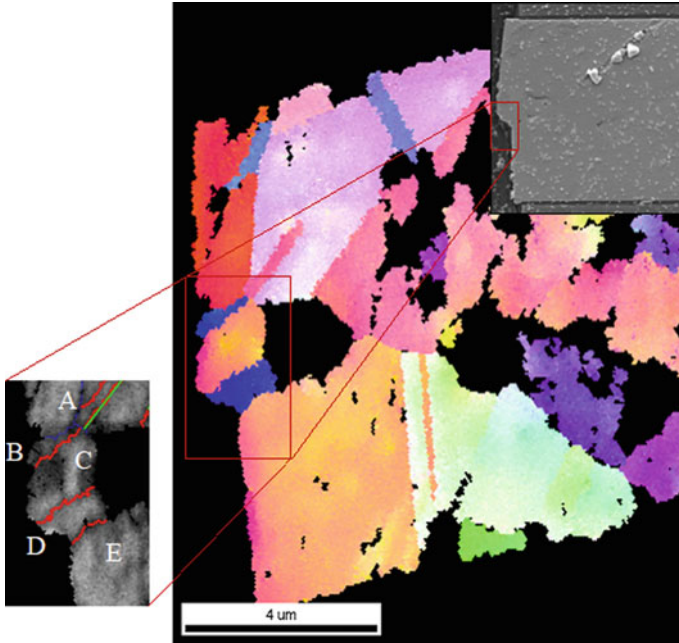


Fig. 4.19 Grain orientation map of the cross-section in the vicinity of the top surface of a TSV, and the corresponding SEM image (inset), showing a distinct surface step. The EBSD image of the region of the step is also shown, with the red lines marking the incoherent $\Sigma 3$ boundaries, and the green line representing a coherent $\Sigma 3$ boundaries (twin plane)

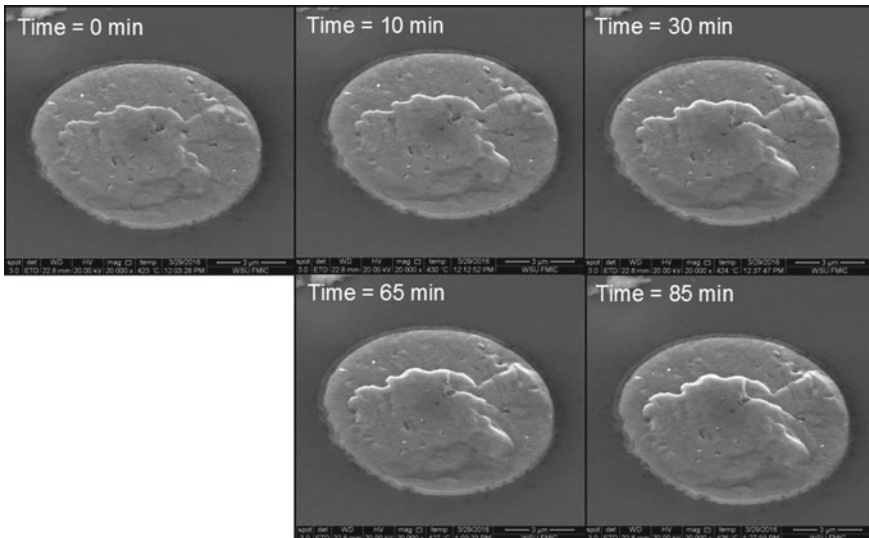


Fig. 4.20 Interposer surface single Cu-TSV SEM in situ observation during holding at 425 °C. TSV sample thermal cycling heating rate is 0.02 °C/sec [60]

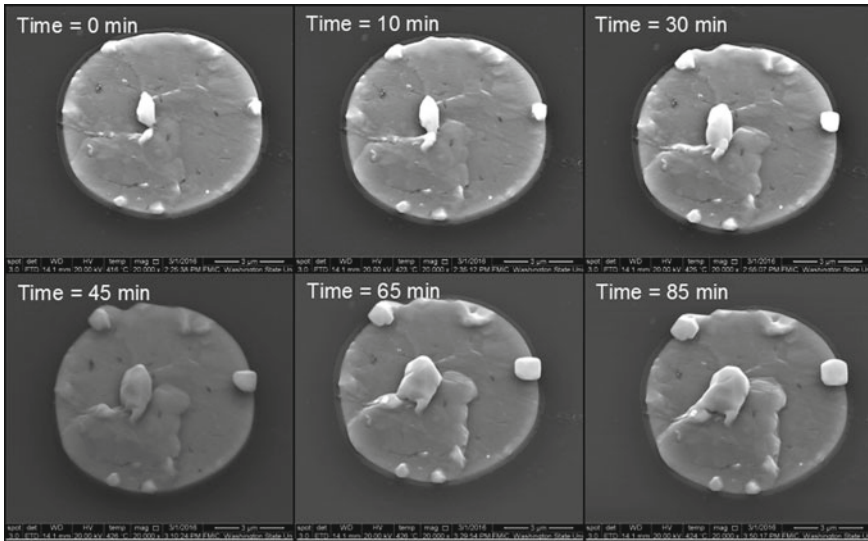


Fig. 4.21 Interposer surface single Cu-TSV SEM in situ observation during holding at 425 °C. TSV sample thermal cycling heating rate is 0.05 °C/sec [60]

but at a higher heating rate (0.05 °C/sec), grains protrude along both the edges and at the center of the TSV due to grain boundary sliding. These features continue to become exaggerated as time progresses. It is to be noted that multiple mechanisms (including grain boundary sliding, interfacial sliding, and plasticity/creep) operate at all heating rates, although the dominant mechanism(s) are different at different rates and over different temperature ranges. The heating rate dependence is attributable to the fact that grain boundary sliding, interfacial sliding and creep are all rate dependent (i.e., diffusion dependent) processes. Because of this diffusion-dependence, as well as the dependence on the stress state of the TSV and the interface (i.e., the driving forces for these processes) at any instant, the relative kinetics of these mechanisms depend on both the temperature, as well as the heating rate.

Figure 4.22a, b show the top of two representative TSVs following five thermal cycles from room temperature to 300 °C and 425 °C, respectively, at a heating rate of 0.01 °C/sec [60]. It is clear that even at the same heating rate, the temperature range of thermal cycling has significant impact on the predominant mechanism of copper-pumping (grain boundary sliding for 300 °C, and interfacial sliding for 425 °C). At this slow heating rate, the creep mechanisms (i.e., grain boundary sliding and interfacial sliding) dominate, with the former dominant at lower temperatures, and the latter at the higher temperatures.

Based on this, Fig. 4.23 schematically shows a summary of the regions of dominance of the various mechanisms, in the heating rate vs. thermal-cycling temperature range plot. As noted in the figure, rate-independent plastic deformation of the TSV dominates when the heating rate is high and the temperature range, and in particular, the maximum temperature is low. At intermediate heating rate and intermediate

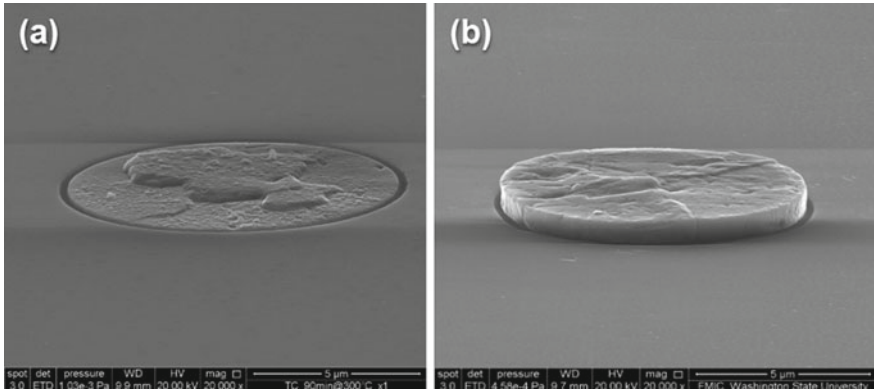


Fig. 4.22 TSV top after five thermal cycles between room temperature and **a** 300 °C and **b** 425 °C, both with a heating rate of 0.01 °C/sec

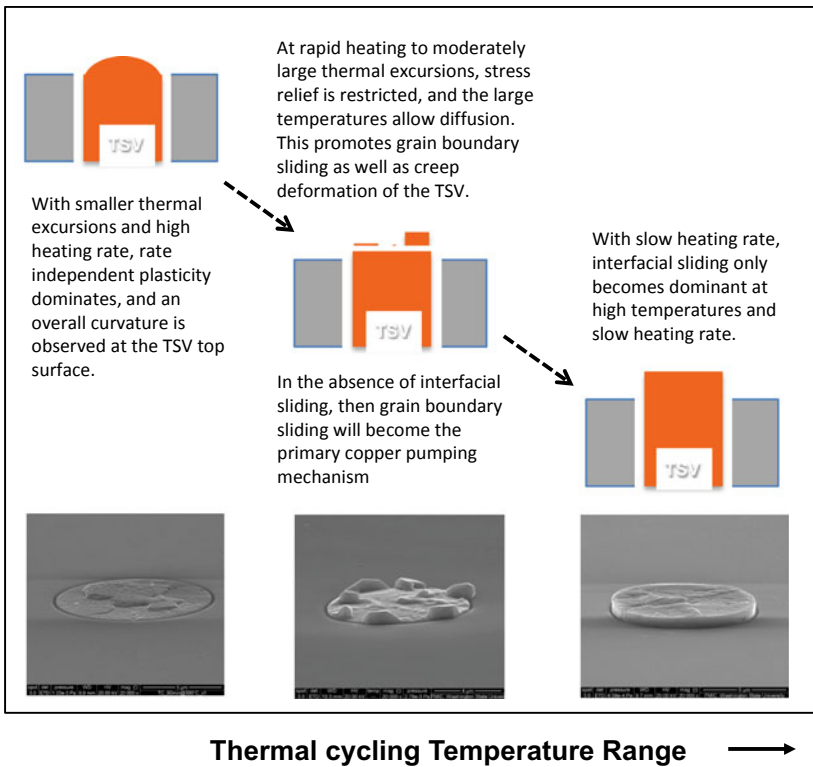


Fig. 4.23 Schematically shown TSV protrusion mechanisms correlated to heating rate and thermal cycling temperature range

temperature range, where there is sufficient thermal activation and time for diffusion, and the stresses in the TSV are high enough, grain boundary sliding is the dominant mechanism, leading to significant surface relief of the TSV-top surface. At high maximum temperature and slow heating rate, the stresses in the TSV are substantially lower (because of stress relief by dislocation or diffusional creep), and interfacial sliding dominates. This interplay between the stress state, heating rate and maximum temperature of the thermal excursion typically results in a superposition of all three of the effects shown in Fig. 4.23, although the effect of one or two of these mechanisms is predominant.

4.3.2 *Electromigration Related Effects*

Although electromigration (EM) is a significant reliability issue in metallic interconnects in electronics, particularly in BEOL structures, TSVs are generally less susceptible to EM induced failures. This is primarily due to their relatively large cross-sections, which reduces the current density. However, the combination of electric current and complicated stress states above and below the TSV, where it joins the BEOL or RDL structures, can cause substantial diffusional effects, and give rise to EM-related void growth. FEA of the effects of stress-gradient, potential gradient and temperature gradient on the atomic flux divergence (AFD), which correlates with diffusional flow and hence electromigration, has noted AFDs are typically high where the top and bottom metallizations meet the TSV [61]. A large proportion of the AFD is due to the stress gradient generated due to Joule heating, with relatively little due to the potential gradient. Still EM damage and void growth can occur. Generally, strategies to reduce stress gradients will reduce void growth.

EM experiments on devices with thin as well as thick metal layers at the top and bottom of TSVs generally show no void formation due to EM within the TSVs, irrespective of the current flow direction [62, 63]. However, voids form downstream of the direction of electron flow, at the intersection of TSV-end and the metal layer in the RDL. It has been hypothesized that these voids nucleate because migration of Cu atoms from the TSV to the void is prevented by the TiN barrier layer, but migration out of the void region can occur into the Cu lines at the end of the TSV. Thus, the layer of TiN, by being effective as a diffusion barrier, actually becomes the root cause behind EM void nucleation. In thin Cu lines, voids occupy the entire thickness of the line (between the TiN barrier and SiN capping layer). Current crowding at the location where the electron current exits the TSV is greater for the thicker lines, and therefore, thicker lines do not mitigate voiding. In thick lines, the voids are at the interface between TiN and the Cu-line. Experimental electromigration studies [64] have also shown voiding in backside Cu lines below the TSV downstream of the electron flow direction, but at the SiN-Cu interface, as opposed to at the TiN-Cu interface seen in Fig. 4.24. However, small voids present prior to EM experiments inside the TSV remained unaltered. Thus, even though the TSVs themselves are

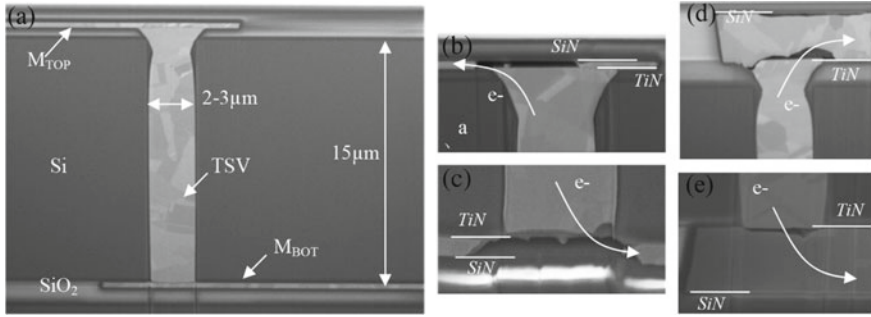


Fig. 4.24 (a) Chip showing a TSV with metal lines at top and bottom. Voids form due to EM at 300 °C at exits of electron flow at top and bottom for thin metal-lines (b) and (c) and thick metal lines (d) and (e) [62]

not susceptible to EM damage, the BEOL and RDL structures in the device can be significantly affected by EM.

A different type of complication is posed by interfacial sliding under electromigration conditions, as indicated in Sect. 4.3.1.3. As evident from Eq. 4.2, an applied electric current may enhance, or mitigate the kinetics of interfacial sliding due to the interfacial shear stress, depending on the direction of the applied field. Even when there is little or no shear stress at the interface, EM can drive interfacial sliding along the TSV-Si (actually, TSV-barrier layer) interface. Evidence of this is shown in Figs. 4.25 and 4.26, where the end of a TSV is seen to protrude in the direction of electron flow, and intrude opposite to electron flow for samples under EM with thermal cycling conditions, and at a constant temperature under a constant current. Under applied current, diffusional flow of Cu occurs along the interface in the direction of electron flow, and this can result in a time-dependent shift of the position of the Cu-filler relative to Si [52–54]. Since EM induced interfacial sliding is non-symmetric (i.e., it causes protrusion of the via downstream of the direction of electron

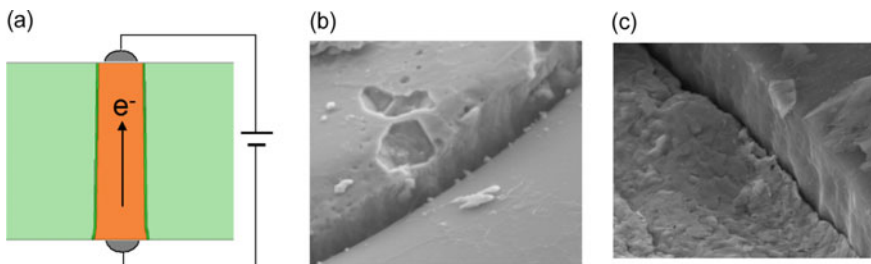


Fig. 4.25 (a) Schematic of experimental arrangement for electromigration cum thermal cycling (25–425 °C) experiments. (b) TSV edge showing protrusion due to 3 thermal cycles + EM due to a current density of $5.2 \times 10^4 \text{ A/cm}^2$, with upward electron flow through Cu. (c) The same TSV following a reverse current density of $-5.2 \times 10^4 \text{ A/cm}^2$, showing that the Cu now intrudes into Si [52, 53]

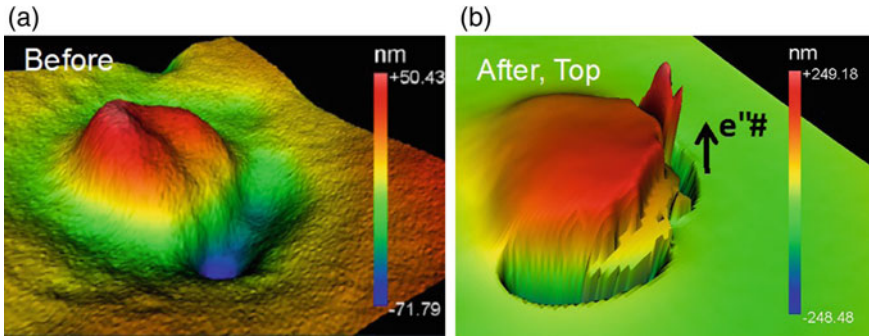


Fig. 4.26 Scanning white light interferometry (SWLI) images of the end of a TSV before and after EM experiments, showing protrusion in the direction of electron flow. A current was passed through Cu thin films deposited on the top and bottom of the chip through several TSVs simultaneously, for 62 h at 170 °C. The current density through each TSV was 5×10^5 A/cm² [54]

flow and intrusion at the opposite end), and unlike under thermal cycling conditions, it accrues continuously [52–54], it may pose a potentially serious reliability challenge, particularly as the current density through the vias increases with decreasing TSV diameter. It is noted that while this via-migration under EM conditions is noted in experiments conducted on samples with through-vias with no RDL layer, the presence of an RDL or BEOL dielectric can constrain such migration and therefore mitigate it. However, because of the low elastic modulus of the RDL/BEOL dielectric, the effect of any imposed constraint may be limited, and therefore, the effect of this phenomenon on the stability of the RDL or BEOL layer needs further study.

Recent studies of several TSVs in a Si interposer with metal layers on top of a TSV have shown two dominant damage mechanisms due to electromigration (EM) [65]. Generally, protrusion/intrusion of the TSV was suppressed due to the presence of the back end interconnect structure (BEIS) at the top, and the redistribution layer (RDL), copper bond-pad and the solder joint at the bottom. However, when subjected to extreme EM conditions (TSV current density of 1.5×10^5 A/cm² at 200 °C for 20 days), voids were observed in the metal-1 (M1) layer, where the electron current crowds following leaving the much larger cross-section TSV, and then leaves after fanning out again. Such a void is indicated with an arrow in Fig. 4.27a. These types of EM voids because of current crowding are consistent with routinely noted voids that form in high density interconnect structures at high current densities. A second type of damage that was noted under the extreme EM exposure was the concentration of Sn within the TSV, as shown in the Sn Ka x-ray map (from energy dispersive spectroscopy) in Fig. 4.27b. It is apparent that Sn has electromigrated in the direction of electron flow from the Sn-based solder ball, through the metallization below the TSV, along the TSV-Si interface, and into the TSV. Such alloying of Cu with elements from the solder under very high current densities can cause significant deterioration of the electrical properties of the device, as well as mechanical instability due to volume change due to alloying. As noted above, the experimental conditions in

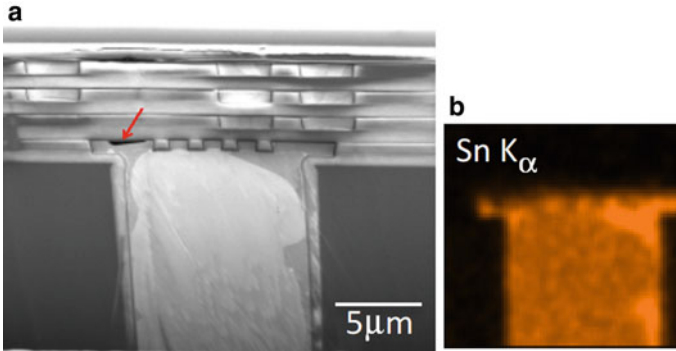


Fig. 4.27 (a) Focused ion beam (FIB) image of the cross-section of the region near the top of a TSV subjected to a current density of 1.5×10^5 A/cm² at 200 °C for 20 days. The electrons flow upwards through the TSV into the metal-1 (M1) layer, and turn 90° to leave the plane of the micrograph. (b) Sn K α x-ray map of the same TSV, showing Sn concentrations at the dark features of the ion image

these experiments were much more severe than those TSV-containing packages are subjected to, but suggest the types of damage to which 3D packages may be subjected with rising current densities and temperatures (ambient or due to Joule heating).

4.4 Towards Atomistically-Informed Reliability Modeling of TSVs

As discussed in Sects. 4.2.2.4 and 4.3.1.2, more robust modeling techniques are needed to complement the FEA and advanced experimental characterization in order to provide a complete picture of the microstructure and stress inside the TSVs. This section introduces two methods, i.e., the crystal plasticity FEA (CPFEA) and the phase field crystal (PFC) method, and discusses their capabilities for atomistically-informed reliability modeling of TSVs.

4.4.1 The CPFE Method

The challenge of managing mechanical stress is not new, and a number of simulators do exist and have a long track record of use in the electronics industry. Most of the proven simulators are based on FEA, or derivatives of that class of modeling technique. The established FEA stress simulators have typically been used for addressing the traditional chip-package interactions, and have therefore mostly modeled physical deformations, such as cracking, delaminating, or fracturing [66]. In this class of analyses Si dies and TSV fillers are typically modeled as monolithic bricks and

isotropic material models based on empirical equations are used, even though it has been known since 1934 that crystalline materials deform plastically by the slip of dislocations on discrete slip systems [67–69]. However, a physically based CPFEM method is relevant in order to address the polycrystalline nature of Cu TSVs and their complex deformation and stress relaxation mechanisms.

Early CPFEM models used phenomenological constitutive equations and considered dislocation slip as the only deformation mechanism [67]. In a phenomenological constitutive model, a critical resolved shear stress, T_c^α , is used as a state variable for each slip system α . The shear rate, $\dot{\gamma}_\alpha$, is formulated as a function of the resolved shear stress and the critical resolved shear stress:

$$\dot{\gamma}^\alpha = f(T^\alpha, T_c^\alpha) \quad (4.3)$$

The evolution of the material state is then formulated as a function of the total shear, γ , and the shear rate, $\dot{\gamma}$:

$$T_c = g(\gamma, \dot{\gamma}) \quad (4.4)$$

The first CPFEM simulations were performed in 1982 using a simplified setup of two symmetric slip systems to study the tensile behavior of a single crystal [70]. The technique was later extended to a polycrystalline scenario using a 2D setup with two or three slip systems [71, 72]. Simulations on a face-centered cubic (FCC) crystal with 12 slip systems was reported in 1991 [73]. Applying the aforementioned phenomenological constitutive laws to small-scale deformation, interface mechanics, and twinning and/or deformation-induced phase transformations are often found inadequate [65]. To address size effects, strain gradient theories [74] can be introduced into the CPFEM framework. As strain gradients can be associated with geometrically necessary dislocations (GNDs), new internal-variable constitutive formulations were developed to incorporate dislocation densities as physically-based state variables replacing the strain variables. This latter class of constitutive models also allows the flexibility to incorporate additional metallurgical mechanisms such as grain boundary mechanics or damage initiation into the model [67]. To deal with additional deformation mechanisms such as occurring in TWIP (twinning-induced plasticity) or TRIP (transformation-induced plasticity) steels, the CPFEM framework was further extended [75].

The result from a unidirectional compression on a copper single crystal using the CPFEM method is shown in Fig. 4.28 [76]. The simulation was implemented in the Düsseldorf Advanced Material Simulation Kit (DAMASK) framework [77]. Although the mechanical boundary conditions and the material are both different from the real Cu-TSV structures, the result highlights the usefulness of the CPFEM method in capturing atomistically-informed deformation and deformation induced crystallographic orientation evolution. The body centered cubic (BCC) tungsten single crystal subjected to uniaxial loading has also been recently studied using the DAMASK framework [78].

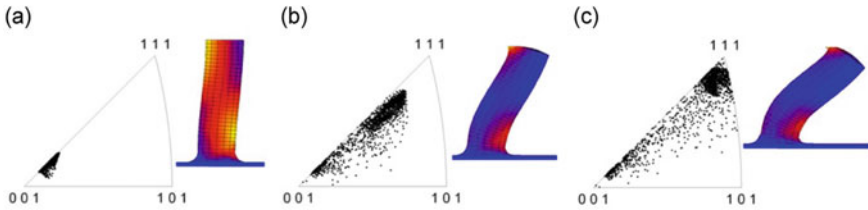


Fig. 4.28 Evolution of crystallographic orientation and geometry of a Cu single crystal pillar with a diameter-to-length ratio of 0.29 under compression with a strain (an engineering thickness reduction) of (a) 0.05, (b) 0.15 and (c) 0.25. Color coding represents accumulated plastic shear ranging from blue (low) to yellow (large). Starting single crystal orientation: $[1\ 1\ 12]$ compression axis (unstable) [76]

4.4.2 The PFC Method

The phase field (PF) methodology is an atomically diffuse interface method for modeling of complex microstructures in solidification, precipitation, and strain-induced phase transformations [79, 80]. The PF may be seen as describing the degree of crystallinity or atomic order/disorder in a phase [80]. More recently, a new class of PF models has been developed, called the PFC models, which describes the thermodynamics and dynamics of phase transformations through an atomically varying order parameter field that is loosely connected to the atomic density field [8, 81, 82]. PFC models naturally capture most of the salient physics of nucleation, polycrystalline solidification, grain boundaries [8, 83], and solidification in multi-component and multiphase systems [84, 85]. In addition, PFC models also capture, in the context of a single order parameter, elasticity and plasticity phenomena relevant to solid-state processes such as dislocation source creation, dislocation stability [86, 87], and creep [88]. The original PFC model was predominately used for the study of 2D triangular and 3D BCC crystal symmetries [8, 81]. Later models introduced multip peaked two-point correlation kernels in the nonlocal part of the free energy that allowed for a simple yet robust approach to simulate most of the common metallic crystal structures (2D square, BCC, FCC, HCP) in phase transformations [87, 88]. These so-called structural PFC (XPFC) models were later generalized to binary and multicomponent and multiphase alloys [85, 89].

Figure 4.29 illustrates a 2D PFC simulation of grain formation in TSVs with different geometries. To study the copper pumping phenomenon, mechanical loads have to be applied on such samples with corresponding grain structures. Since the PFC method does not model a solid-vacuum interface, traction boundary conditions in the PFC model using a penalty term are introduced. In deformation simulations, dislocation creation and annihilation are emergent characters of the PFC model. Therefore, applying the PFC model to TSV filler allows the investigation of the dislocation dynamics responsible for the metal extrusion or intrusion problem. The recorded dislocation dynamics can also be used to formulate dislocation-based constitutive laws for the CPFEM method. In addition, progress has been made to couple the

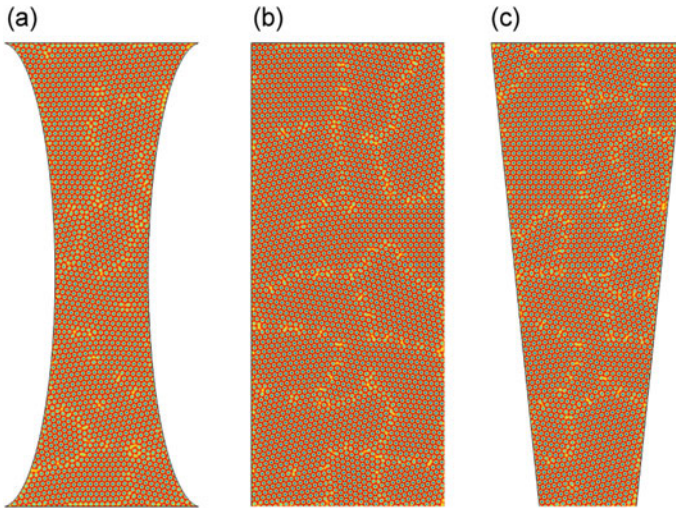


Fig. 4.29 Simulations on atomistic scale microstructural formation in (a) hourglass, (b) rectangle, and (c) trapezoid shaped TSVs using the phase field crystal model

atomic-scale PFC density field to order parameters that describe ferromagnetic and ferroelectric ordering [90]. As such, the PFC models can be used to study the role of external magnetic or electric fields on the evolution of atomic scale defect structures on diffusion time scales. This provides an opportunity to study electromigration related reliability issues of TSVs using the PFC models.

4.5 Summary

Some of the key reliability issues related to TSVs are discussed, starting with the origin and nature of stresses in TSVs, their effects on microstructure development and evolution, and their role on device performance and BEOL or RDL reliability. The main reliability complications are (i) void growth to relieve internal stress gradients during pre or post-CMP annealing, (ii) copper pumping during processing or service due to differential thermal expansion mismatch and associated inelastic deformation of the copper that may be accommodated by sliding at the interface, and associated distortion of the BEOL/RDL structure, (iii) piezoresistive effects that lead to device performance loss and require a keep-out zone adjacent to TSVs, and (iv) electromigration induced void growth downstream of the electron flow direction in the interconnect lines outside the TSV. These effects have been reviewed in the context of the associated physical mechanisms. Finally, two promising methods, i.e., the CPFEA and the PFC method, to enable atomistically-informed reliability modeling of TSVs are introduced.

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