

Chapter 15

Die and Package Level Thermal and Thermal/Moisture Stresses in 3-D Packaging: Modeling and Characterization



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List of symbols

A	Geometry factor for calculating thermal stress in multi-layered structure
$\bar{\epsilon}_T$	Average thermal strain
a	Via radius
σ_θ	Circumferential stress
ΔT_y	Critical thermal load for plastic yielding
C_{sat}	Saturated moisture concentration
α_{Cu}	CTE of copper
α_{Si}	CTE of silicon
D	Moisture diffusivity
d	Via diameter
E	Total volumetric strain
E	Young's Modulus
k_P	Factor for hydrostatic pressure gradient-driven diffusion
k_T	FACTOR for thermal gradient-driven diffusion

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$\Delta\omega_3$	Frequency shift of the longitudinal Raman mode
G and λ	Lame's elastic constants
η	Generalized Poisson's ratio
h_b	Bending axis
h_i	Top surface coordinate
h_m	Midpoint coordinate
H	Via depth
ε_c	Hygroscopic strain
σ_T	Mismatch thermal stress
ϕ	Normalized concentration or activity
p_{amb}	Ambient partial water vapor pressure
p_g	Saturated water vapor pressure
P	Hydrostatic pressure
ν	Poisson's ratio
$\dot{\phi}$	Porosity growth rate
P	Partial water vapor pressure
Q	Activation energy for moisture diffusivity
ΔH_r	Residual via extrusion
S	Solubility
T_{ref}	Stress-free temperature
γ_e	The rate of elastic extrusion
γ_p	The rate of plastic extrusion
D_T	Thermal diffusivity
ε_T	Thermal strain
T_m	Maximum temperature during thermal cycling
T_R	Room temperature
u_i	Displacement vector
ε_p	Vapor pressure-induced strain
W	Warpage
W	Wetness
X_i	Body force vector
ΔT	Thermal loading
κ_{app}	Applied external curvature
κ	Curvature
κ_{nat}	Natural bending-induced curvature
$\pi_{11}, \pi_{12}, \pi_{44}$	Piezoresistance coefficients
ρ_g	Density of saturated water vapor
σ_r	Radial stress
σ_{rz}	Shear stress in r - z plane
σ_z	Normal stress in z direction
β	Coefficient of hygroscopic swelling
ϕ	Porosity
ρ_a	Apparent moisture density

15.1 Introduction

3-D packaging with through-silicon vias (TSVs) is one of the key technologies implemented in semiconductor manufacturing in order to increase bandwidth, enhance performance, shrink form factor, and reduce power [1–3]. Due to the introduction of new features like TSV for providing short vertical interconnections, there exist unique reliability requirements for 3D technology [4, 5]. Compared to conventional 2D packages, particular attention must be given to the new failure mechanisms of TSV components and 3D chip stacks under various stress conditions [5–8].

Thermal stress in 3D package is generated due to the mismatch in coefficients of thermal expansion (CTEs) between dissimilar materials when there is temperature change. At die level, high thermal stress in TSV chips may cause many reliability issues, including extrusion of TSV, cracking of silicon chip, and unintentional carrier mobility change around TSVs. The issues in TSV chips will eventually affect the reliability of the whole 3D system. At package level, reliability issues caused by thermal stresses may include fatigue fracture of solder ball joints and other interconnects, the warping of dies, substrates and package, and the delamination and cracks initiated at the interface between dissimilar materials [8–12]. The warping or non-uniformity at package level can be especially critical because larger single die or multiple dies are often used in 3D structure. The overall warpage of a chip-substrate structure will affect the bonding process at board level [13].

In addition to thermal stress, particular attention is also given to moisture-induced stress. A typical 3D package will contain moisture-sensitive materials, i.e., polymeric materials at different levels, which can absorb a certain amount of moisture from the ambient. Excessive moisture absorption may increase the corrosion rate of the metal parts and aggravate the electro-chemical-migration [14, 15]. Moisture-induced stress, such as hygroscopic stress, may also cause leakage to bulk chips, metal delamination, cracking and extrusion in TSV chains [5], and the hygroscopic strain could be comparable or even higher than thermal strain [16–18]. More significantly, during reflow soldering or the highly accelerated temperature and humidity stress test (HAST), devastating material ruptures or interface delamination may take place. [19–27].

This chapter aims to provide fundamental theories, modeling and characterization methods for analyzing the effects of thermal and moisture-induced stresses in 3D packaging. First, the analysis and measurement of thermal stress in and around the TSVs are presented in Sect. 15.2. The results reveal the near-surface characteristics of thermal stress and the important role of Cu microstructure in controlling stress. Stress-induced reliability issues, including the keep-out zone and via extrusion, are discussed. In Sect. 15.3, thermal stress induced warpage at package level is studied. Analytical modeling of an idealized multi-layered structure is described first. Then several warpage control methods with experimental testing and numerical modeling are introduced. A new warpage control method is presented to achieve warpage-free flip-chip package. In Sect. 15.4, moisture-induced stress is calculated and coupled with thermal stress to form an integrated stress modeling. A theoretical framework based on damage micromechanics and effective stress concept is presented to achieve

stress integration, which is able to combine multiple field variables such as temperature, moisture concentration, vapor pressure, and void volume fraction. An example of integrated stress analysis is then performed based on the theory. Section 15.5 summarizes the findings of thermo-mechanical and moisture induced stresses in 3D packaging.

15.2 Thermal Stress and Its Effects on TSV Structures

15.2.1 Introduction

Due to the large thermal expansion mismatch between Cu TSVs and Si ($\alpha_{\text{Cu}} = 17 \text{ ppm}/^\circ\text{C}$, $\alpha_{\text{Si}} = 2.3 \text{ ppm}/^\circ\text{C}$), significant thermal stresses can be induced in and around TSVs to cause serious reliability issues [28–31]. To successfully implement TSVs in 3-D integration, it is essential to analyze and understand the characteristics of thermal stresses at die level, as well as their impact on TSV structures.

The confinement by the surrounding Si results in complex stress state in and around the TSV. The microstructure of Cu also plays an important role in controlling the stress of the TSV structure. To capture these unique characteristics, this section will first present stress analysis by both a semi-analytic method and numerical analysis, followed by stress measurement using two complimentary techniques. Finally, two reliability issues induced by stress, the device keep-out zone (KOZ) and via extrusion, will be discussed.

15.2.2 Characteristics of TSV Stress by Semi-analytic and Numerical Solutions

2-D plane-strain solution to the classical Lamé problem has been employed to analyze the thermal stresses of TSVs, but the 2D solution inherently could not capture the 3-D nature of the stress field near the wafer surface [32]. To overcome this limitation, a semi-analytic solution is derived for an isolated TSV embedded in silicon using a linear superposition method [33]. The stress contours calculated from the semi-analytic solution are plotted in Fig. 15.1. At the wafer surface ($z = 0$), the normal stress σ_z is zero as required by the traction-free boundary condition and is non-uniform away from the surface (Fig. 15.1a). At the wafer surface, the shear stress (σ_{rz}) has a singular concentration at the via/Si interface (Fig. 15.1b), and the radial stress (σ_r) and circumferential stress (σ_θ) are non-zero (Fig. 15.1c and Fig. 15.1d). Both the radial and shear stresses contribute to the driving force for interfacial delamination. Because the radial stress (σ_r) is tensile during cooling and compression during heating, the driving force for interfacial delamination under cooling is about twice of that under heating. Based on the semi-analytic solution, the steady-state energy release rate of

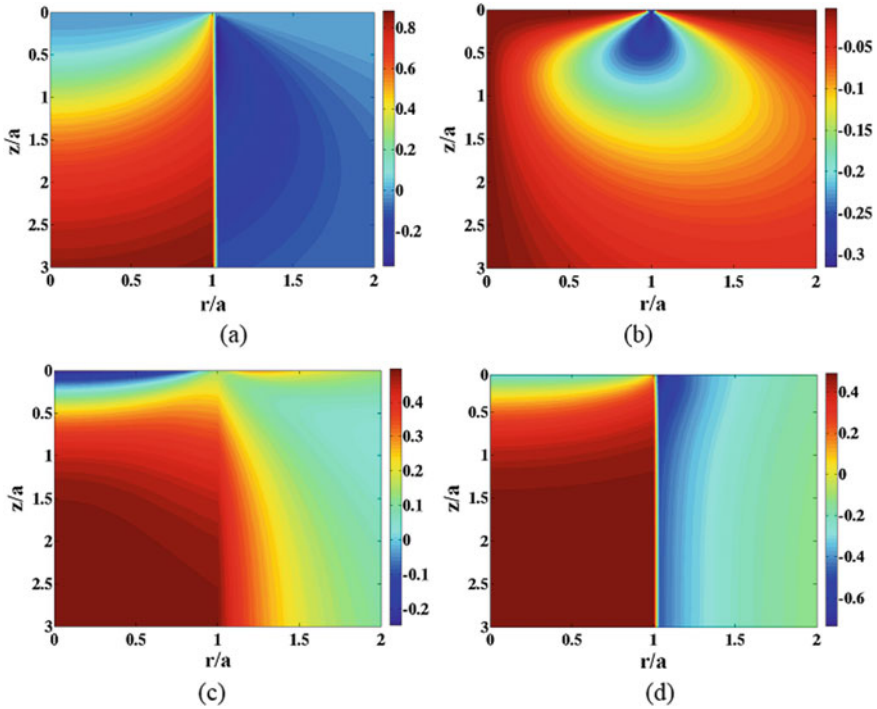


Fig. 15.1 Near-surface stress distributions predicted by the semi-analytical solution for a thermal load of ΔT . The stress magnitudes are normalized by $\sigma_T = -E\varepsilon_T/(1 - \nu)$, and the radial and depth coordinates (r and z) are normalized by the via radius $a = d/2$: (a) out-of plane stress (σ_z); (b) shear stress (σ_{rz}); (c) radial stress (σ_r); (d) circumferential stress (σ_θ) [33]

interfacial delamination is found to be linearly proportional to the via diameter, but to the square of the thermal mismatch strain, $\varepsilon_T = \Delta\alpha\Delta T$. This result suggests that decreasing the TSV diameter and the thermal load, or selecting via materials with smaller thermal expansion mismatch with Si are potential solutions to reduce the delamination driving force.

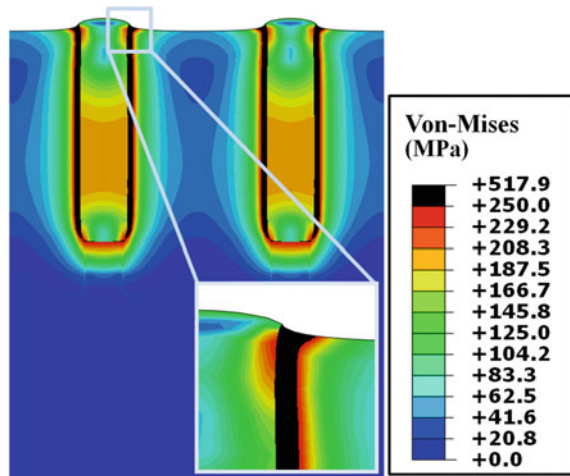
Finite element analysis (FEA) has been used to verify the semi-analytic solution and to further examine the thermal stress in the TSV. Three-dimensional (3D) FEA models are constructed for blind via structures. The via dimension is $10\ \mu\text{m} \times 55\ \mu\text{m}$ (diameter \times depth), and the Si thickness is $780\ \mu\text{m}$. There is an oxide barrier layer at the TSV/Si interface of $0.4\ \mu\text{m}$ thick, and the thin Ta barrier layer is neglected in the model. The material properties used in the model are listed in Table 15.1.

For a thermal load of $\Delta T = 200\ ^\circ\text{C}$, the von-Mises stress is plotted in Fig. 15.2 [34]. The von-Mises stress is much lower than the yield strength of Cu in most of the via, except for a small region near the via/Si interface at the top of the via. Since von-Mises stress is the effective shear stress driving plastic deformation, the FEA result suggests that the Cu via will be mostly elastic under temperature excursion, and plasticity will be localized near the junction between the via/Si interface and the

Table 15.1 Thermo-mechanical properties used in finite element analysis

Material	CTE (ppm/°C)	Young's Modulus (GPa)	Poisson's ratio
Cu	17	110	0.35
Si	2.3	130	0.28
Oxide	0.55	72	0.16

Fig. 15.2 Von-Mises stress for a thermal load $\Delta T = 200\text{ }^\circ\text{C}$. The via dimension is $10\text{ }\mu\text{m} \times 55\text{ }\mu\text{m}$ (diameter \times depth), and Si thickness is $780\text{ }\mu\text{m}$ thick [34]



wafer surface. The localized plasticity in TSVs can be attributed to the triaxial stress state in the TSV structure, which is distinctively different from the biaxial stress state of Cu thin film. As a result of the triaxial stress state, the effective shear stress causing plastic deformation is relatively low in TSV structures. This has important implications on TSV reliability which will be discussed in the rest of this section.

15.2.3 Measurement of Thermal Stress

Several experimental techniques have been developed to measure the stress behavior of TSV structures, including wafer curvature and micro-Raman spectroscopy [34–38]. While individual technique has its limitations, when combined and by correlating to the microstructure evolution and FEA, the results can provide basic understanding of the stress characteristics of the TSV structures.

The wafer curvature method utilizes an optical lever set-up to measure the bending curvature of the sample during thermal cycling. For a blind TSV structure illustrated in Fig. 15.3, this method is used to obtain the overall thermo-mechanical behavior of the TSV structure [35]. For TSV specimens going through single thermal cycles

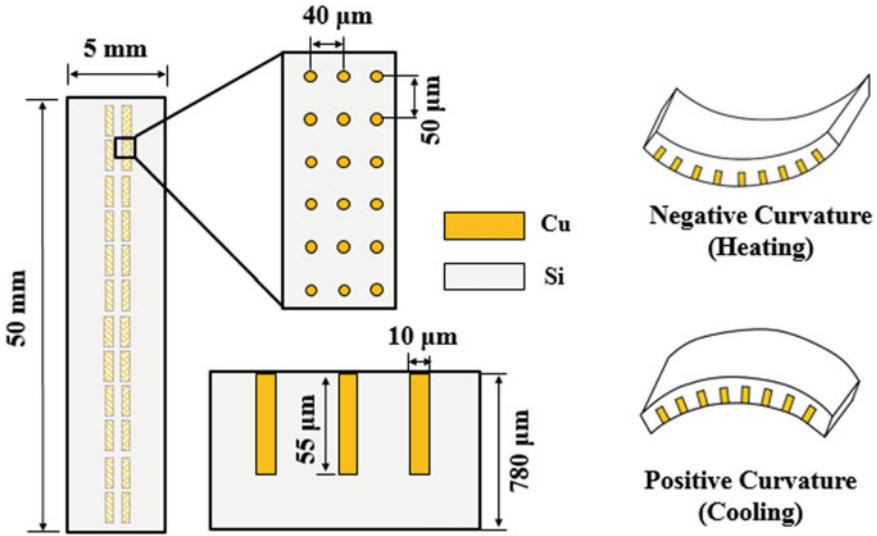


Fig. 15.3 Illustration of the TSV specimen for wafer curvature test. The specimen size is 5 mm × 50 mm × 780 μm (width × length × thickness) and contains periodic arrays of vias along the centerline of the specimen. The dimension of the TSV is 10 μm × 55 μm (diameter × depth), and the pitch distances are 50 and 40 μm in the longitudinal and transverse directions, respectively. The top surface of Si is covered with an oxide layer of 0.8 μm thick which was removed by mechanical polishing before measurement. The thickness of oxide barrier layer at the via/Si interface is about 0.4 μm. Adapted from ref [35]

to peak temperatures of 100, 200, 300 and 400 °C, the curvature change, $\Delta\kappa$, as a function of temperature, T , are plotted in Fig. 15.4a.

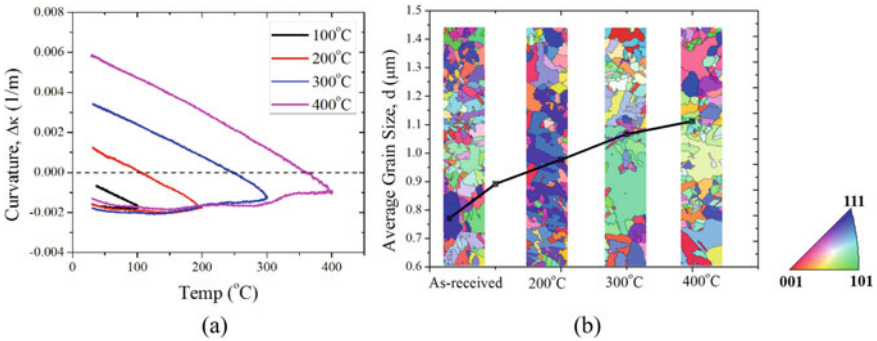


Fig. 15.4 (a) Curvature measurement of four TSV specimens subjected to single thermal cycling to 100, 200, 300, and 400 °C, respectively. (b) Grain growth in TSVs as shown by the crystal orientation maps and grain sizes (black line) obtained by electron backscatter diffraction (EBSD) after the TSVs have been thermal cycled to different temperatures. Adapted from ref [41]

Some distinct features of the curvature-temperature behavior of TSV structures as seen in Fig. 15.4 are: stress relaxation during heating; linear curvature-temperature relation during cooling; and absence of hysteresis loops. The stress relaxation observed in the heating portion of each test is correlated to Cu grain growth in the via, which is measured by electron backscatter diffraction (EBSD) (Fig. 15.4b). A decrease of additive elements (Cl^- , F^- , S^- , and CN^-) is found to accompany grain growth as obtained by time-of-flight secondary ion mass spectroscopy (TOF-SIMS) [39]. The linear cooling curvature observed in the experiment can be directly correlated to the triaxial stress state (as shown in Fig. 15.2) obtained by FEA, as the Cu via would remain mostly elastic with localized plasticity. This is in sharp contrast with electroplated Cu thin films which have bi-axial stress state and show hysteresis loops during thermal cycling [40]. The temperature at which the cooling curvature crosses zero gives the reference temperature at which the average stress in the TSVs is zero. With increased thermal cycling temperature, the amount of stress relaxation increases during heating. This leads to higher stress-free temperatures and accumulation of residual stress at room temperature after each thermal cycle.

Micro-Raman spectroscopy measures the near-surface stress in Si around the TSV and complements the measurement by wafer curvature method. TSV specimen as shown in Fig. 15.3 is used for the micro-Raman measurement [35]. Two specimens, referred to as A and B, are subjected to different thermal treatment and their stress-free temperatures are determined to be $T_{ref}^A = 100^\circ\text{C}$ and $T_{ref}^B = 300^\circ\text{C}$, from wafer curvature measurement. The micro-Raman measurement is performed using [001] backscattering configuration, and the signals are collected by scanning the laser across two neighboring vias along the [110] direction in each sample.

In the test configuration, longitudinal Raman frequency shift, $\Delta\omega_3$, is measured and can be correlated to the sum of the in-plane normal stresses, $\sigma_r + \sigma_\theta$, through Eq. (15.1) [42, 43]:

$$\sigma_r + \sigma_\theta (\text{MPa}) = -470\Delta\omega_3 (\text{cm}^{-1}) \quad (15.1)$$

As the measurement obtains only the sum of the two individual stress components in Si, FEA is used to delineate the stress components. The FEA model considers the anisotropic elastic properties of Si while treating Cu as linear elastic as deduced from the linear cooling curve in the wafer curvature measurement. The material properties in Table 15.1 are used in FEA. The thermal load is $\Delta T_A = -70^\circ\text{C}$ and $\Delta T_B = -270^\circ\text{C}$, as obtained from the reference temperatures. Since the Raman signal penetrates up to $0.2\ \mu\text{m}$ from the wafer surface, the stress components are extracted from $0.2\ \mu\text{m}$ below the wafer surface in the model [35]. The stress sums from both experimental measurement and FEA are plotted in Fig. 15.5 and show reasonable agreement. Away from the Cu/Si interface, the sum of the stresses first increases sharply, and then gradually decreases. Between the two adjacent vias, the stress depends on the pitch distance as a result of stress interaction. Because of the larger negative thermal load for specimen B ($|\Delta T_B| > |\Delta T_A|$), specimen B (Fig. 15.5b) shows a higher stress level in Si than specimen A (Fig. 15.5a). This establishes the correlation between the Raman measurement and wafer curvature measurement,

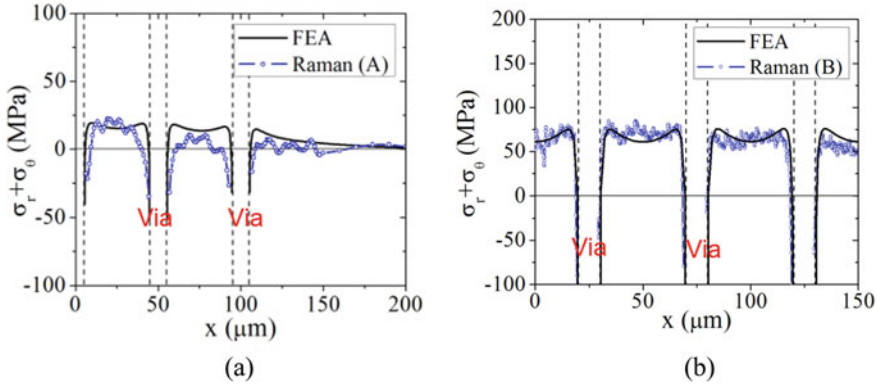


Fig. 15.5 Comparison of the near-surface stress distribution between Raman measurements and FEA: (a) Specimen A ($\Delta T_A = -70\text{ }^\circ\text{C}$); (b) Specimen B ($\Delta T_B = -270\text{ }^\circ\text{C}$)

which together show the dependence of residual stress on the thermal history of TSVs.

15.2.4 Effect of Thermal Stress on Carrier Mobility and Keep-Out Zone

The thermal stress in Si can degrade the performance of the MOSFET devices through the piezoresistivity effect [44]. This results in a keep-out zone (KOZ) around the TSV where the placement of active devices should be avoided [45–47]. For [001] Si with current flows in the [100] direction, the piezoresistance coefficients for n- and p-Type Si are listed in Table 15.2 [44].

With the piezoresistance coefficients, the carrier mobility change around the TSVs can be calculated from the thermal stress obtained in FEA and shown in Fig. 15.6 for an isolated via embedded in Si [47]. The via dimension is $10\text{ }\mu\text{m} \times 200\text{ }\mu\text{m}$ (diameter \times height), the Si thickness is $780\text{ }\mu\text{m}$, and the thermal load is $\Delta T = -250\text{ }^\circ\text{C}$. The dashed lines in the figures mark the boundaries of 5% change in mobility, which defines the KOZ. Since both the elastic properties and the piezoresistance of Si are anisotropic, the mobility change is highly directional and is very different for n- and p-type Si. For transistors with [100] channel, a sizable KOZ is developed in n-type silicon (Fig. 15.6a), but no KOZ exists in p-type Si. In contrast, for [110] channel, considerable KOZ exists for p-type silicon (Fig. 15.6b) while no KOZ exist in n-type

Table 15.2 Piezoresistance coefficients for n- and p-Type Si (in unit of 10^{-11} Pa^{-1})

	π_{11}	π_{12}	π_{44}
n-type Si	-102.2	53.7	-13.6
p-type Si	6.6	-1.1	138.1

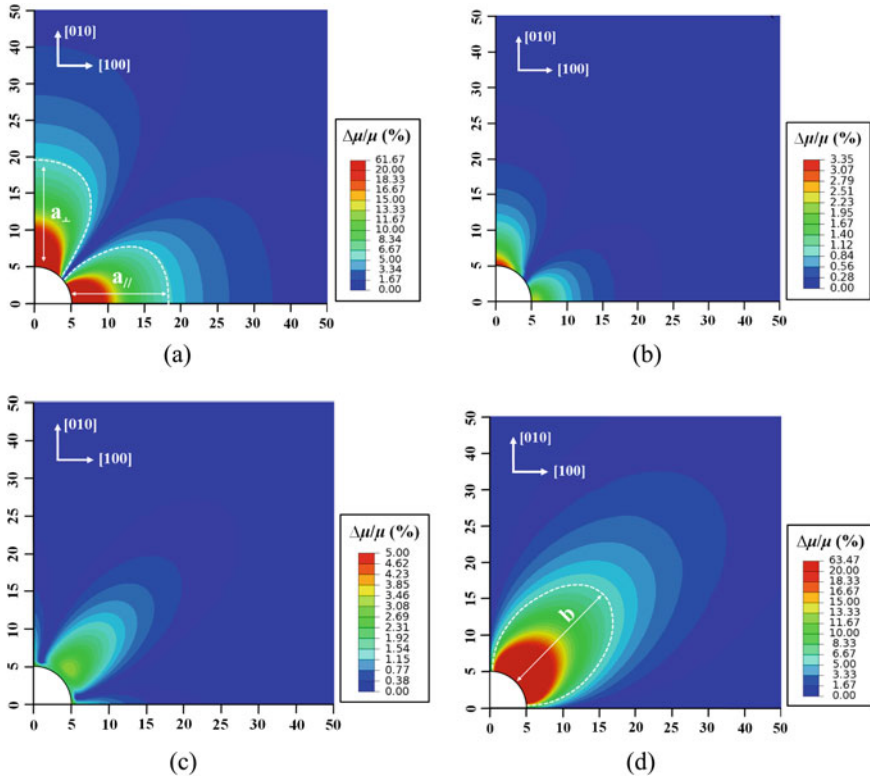


Fig. 15.6 Distribution of mobility changes in (a) n-type MOSFETS with the electric field and current density in [100] direction and (b) Mobility change for p-type MOSFET with [100] channel. (c) Mobility change for n-type MOSFET with current density in [110] direction. (d) p-type MOSFETS with the electric field and current density in [110] direction. The dashed lines indicate the 5% mobility change ($d = 10 \mu\text{m}$, $H = 200 \mu\text{m}$, and $\Delta T = -250 \text{ }^\circ\text{C}$). [40]

Si. Further analyses by FEA show that the KOZ increases monotonically with TSV diameter [47]. The plasticity of Cu can relax stress close to the via/Si interface to reduce the size of KOZ, but this effect is rather localized. When the TSVs are placed closer together, stress interaction between neighboring vias can increase the overall stresses in Si and thus the size of KOZ, but stress interaction is negligible when the ratio of via pitch to diameter is larger than 5.

15.2.5 Thermal Stress Induced via Extrusion

Via extrusion is the non-recoverable deformation of Cu near the top of the via after thermal cycles. Grain growth, plastic yielding by dislocation glide, and diffusional creep along grain boundaries and/or the via/liner interface are possible relaxation

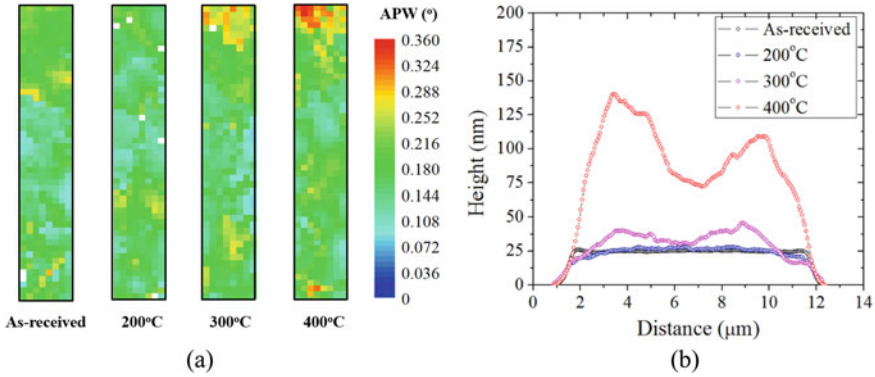


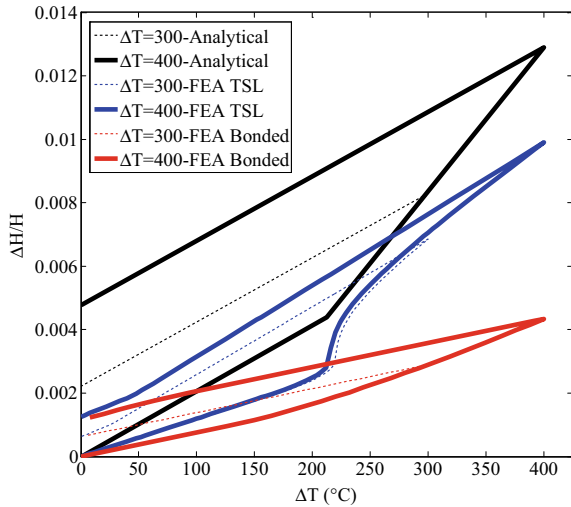
Fig. 15.7 (a) Average peak width (APW) of Cu for the as-received via and vias after thermal cycling to 200, 300, and 400 °C. Increased APW indicates increased plasticity in the Cu vias. (b) Via extrusion profiles obtained from AFM measurements [51]

processes responsible for via extrusion. A high-temperature post-plating annealing has been adopted in TSV fabrication to stabilize the grain structure to reduce via extrusion during subsequent thermal processing [28, 48, 49]. In general, grain growth could lower the yield strength of Cu due to the Hall-Petch effect, which in turn would cause more plastic deformation and Cu extrusion [50].

The local plasticity in Cu is observed experimentally by synchrotron x-ray micro-diffraction and correlated to the magnitude of via extrusion (Fig. 15.7) [51]. To elucidate the effects of Cu plasticity on via extrusion, a simple analytic model is formulated as follows. When the TSV is subjected to a thermal cycle from room temperature (T_R) to an elevated temperature T , the mismatch of thermal expansion between the Cu via and Si induces a compressive stress in Cu upon heating ($\Delta T = T - T_R$). Assuming perfect plasticity with a yield strength σ_y for the Cu via, plastic yielding of Cu is predicted when heating above a critical temperature, $\Delta T_y = \frac{\sigma_y}{\alpha_{Cu} - \alpha_{Si}} \left(\frac{1 - \nu_{Cu}}{E_{Cu}} + \frac{1 + \nu_{Si}}{E_{Si}} \right)$, which is proportional to the yield strength of Cu. Beyond the critical temperature ($\Delta T > \Delta T_y$), the Cu via deforms plastically, leading to more via extrusion at higher temperatures. The plastic extrusion does not vanish after cooling, resulting in a non-zero residual extrusion after a full thermal cycle: $\Delta H_r = H(\gamma_p - \gamma_e)(\Delta T_m - \Delta T_y)$, where H is the via height, $\gamma_e = 20.64 \text{ ppm}/^\circ\text{C}$ and $\gamma_p = 46.4 \text{ ppm}/^\circ\text{C}$ are the rate of extrusion as a function of temperature calculated from the thermo-mechanical properties in Table 15.1, and $\Delta T_m = T_m - T_R$ where T_m is the maximum temperature during thermal cycling [51]. This shows that the magnitude of the residual extrusion depends on the peak temperature during thermal cycling and the plastic yield strength of the Cu via. Increasing the yield strength of Cu would increase the yield temperature ΔT_y and thus decrease the residual extrusion for the same thermal load [50].

The effect of interfacial properties on via extrusion has been studied by numerical simulations using FEA models (Fig. 15.8) [50–52]. FEA shows that a perfectly bonded interface between the Cu via and Si reduces the residual extrusion at room

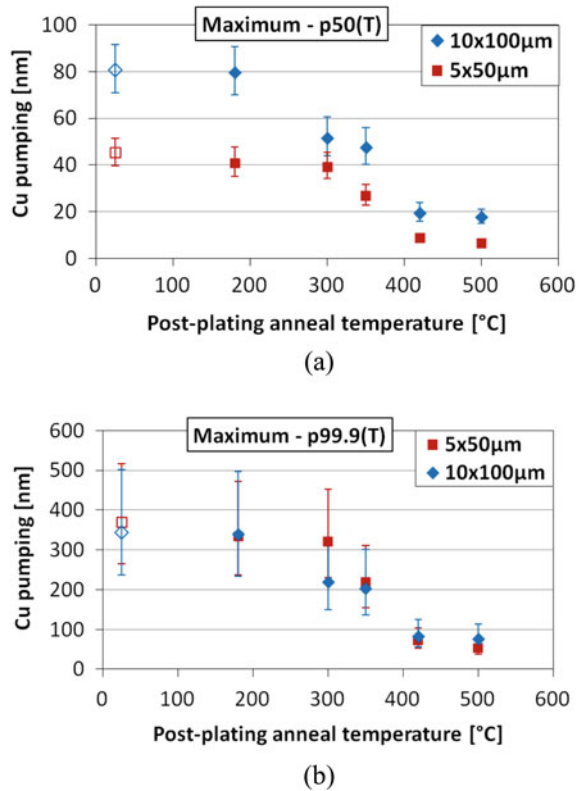
Fig. 15.8 Comparison of extrusion ratio, $\Delta H/H$, between analytical and FEA results assuming interfaces with perfect bonding and bilinear traction separation relationship. Assume zero initial residual stress [51]



temperature by about 3 times. Using a cohesive model for the via/Si interface, the via extrusion is found to be bound by two limits: the frictionless sliding in the analytical model as the upper bound and the perfectly bonded interface (no sliding) as the lower bound. This analysis implies that via extrusion can be suppressed by improving interfacial adhesion to resist sliding.

For a large ensemble of vias, via extrusion is found to follow a lognormal distribution [53, 54]. For two via sizes of $5 \times 50 \mu\text{m}$ and $10 \times 100 \mu\text{m}$ with different post-plating annealing temperatures, the average via extrusion at 50% is about half for the smaller TSVs (Fig. 15.9a), but the largest extrusions at 99.9% of the lognormal distribution is about the same for both sets of TSVs, independent of via size and anneal conditions (Fig. 15.9b). These results highlight the statistical nature of via extrusion, and indicated that the TSV reliability will not be improved by simply reducing via diameter, since 3DICs contain a large number of TSVs. Rather, the reliability is determined by the largest extrusions, i.e. the weakest link, in spite of their small percentage (about 0.1%). The statistical spread in via extrusion can be correlated to the grain size and orientation near the top of the vias and smaller extrusion is observed for vias with larger portion of twin boundaries [54]. It is therefore important to optimize the electroplating chemistry and annealing process to achieve grain structures with large portion of twin boundaries and large yield strength in order to minimize via extrusion. However, it is not clear how such grain structures could be so prevalent to completely eliminate the tail distribution of the largest extrusions.

Fig. 15.9 (a) Maximum average (50%) residual extrusion and (b) maximum tail distribution (99.9%) of residual extrusion for two sets of TSVs of $5 \times 50 \mu\text{m}$ and $10 \times 100 \mu\text{m}$ dimensions as a function of post-plating anneal temperature [53]



15.3 Thermal Stresses and the Warpage Control at Package Level

15.3.1 Introduction

Warpage by thermal stress is one of the most common but critical issues for electronic packaging [55–64], which could pose a great challenge in manufacture, application, and reliability testing of 3D packages, especially for the case when large, thin chip stacks are connected to organic laminates or substrates [8–10, 65]. Excessive warpage will give rise to difficulty in chip interconnecting and bonding to the substrate, usually leaving opens. The warping in chips can also cause compressive forces on molten solder balls, resulting in lateral expansion and unintentional bridging. Operations at board level is also affected by excessive package-level warpage. Examples include solder ball bridging or opening during surface mount process, and package failures during package functional test [60, 61].

To reduce thermal-stress induced warpage, traditional control methods, such as adding a stiffener ring or a lid, may not be efficient. These methods are typically

substrate-control methods, which could result in additional stress into the package. Therefore, it is necessary to develop more effective control methods based on deep understanding of warpage control mechanism [66].

To address the thermal stress induced reliability issues (e.g., excessive warpage and solder joint failures) at package level and provide potential solutions, this section will first introduce analytical theories for the calculation of thermal stress and warpage for multilayered structures under temperature loading. Then the warpage mechanism during the packaging process is demonstrated, followed by discussion on the effectiveness of traditional warpage control methods in Sect. 15.3.3. In Sect. 15.3.4, a new control approach is presented for achieving potential warpage-free package. Numerical modeling, as well as experimental testing, is performed to verify the new method. Different cases are studied and the results are discussed in details.

15.3.2 Thermal Stresses in a Multilayered Structure

As 3D chip stacks and other microelectronic devices can be conceived as multilayered structures, analytical modeling based on the existing theories may be adopted. The main advantage of analytical modeling is that one can perform quick calculation of thermal stress for any multilayered systems with regular geometry, especially for those including very thin layers.

There are several analytical methods available for calculating the thermal stress in laminated structures or multilayered composite used in electronic packaging. One theory introduced here is called the natural bending theory [67], which is based on the assumptions of linear elasticity and small deformation. The basic idea of the natural bending theory is illustrated in Fig. 15.10, where a two-layer system is used for simplicity. Due to different CTEs of layer 1 and layer 2 ($\alpha_2 < \alpha_1$), thermal mismatch is produced in the cooling process from high temperature (T_H) to room temperature (T_R). The theory first considers a stress-free case, so that each material will contract accordingly to their CTEs, resulting in mismatch in stress-free thermal strain ($\varepsilon_{T1}^0 = \alpha_1 \Delta T > \varepsilon_{T2}^0 = \alpha_2 \Delta T$). To accommodate the mismatch, layer 1 will be constrained and then bonded to layer 2. After the constraint is released and the stack will be bent. The process of natural bending theory can be used to explain how warpage is developed by thermal stress in dissimilar materials. Note that uniform temperature is considered in the theory.

Based on the natural bending theory, the warpage of a multilayered device can be resulted from both thermal loading and external applied curvature. The normal stress in x direction in each layer i of a composite can be expressed as a function of thermal strain and applied curvature, as [67]

$$\sigma_{xi} = \bar{E}_i [(\kappa_{nat} + \kappa_{app})(y - h_b) + \bar{\varepsilon}_T + v_i A - \eta_i \varepsilon_i^0] \quad (15.2)$$

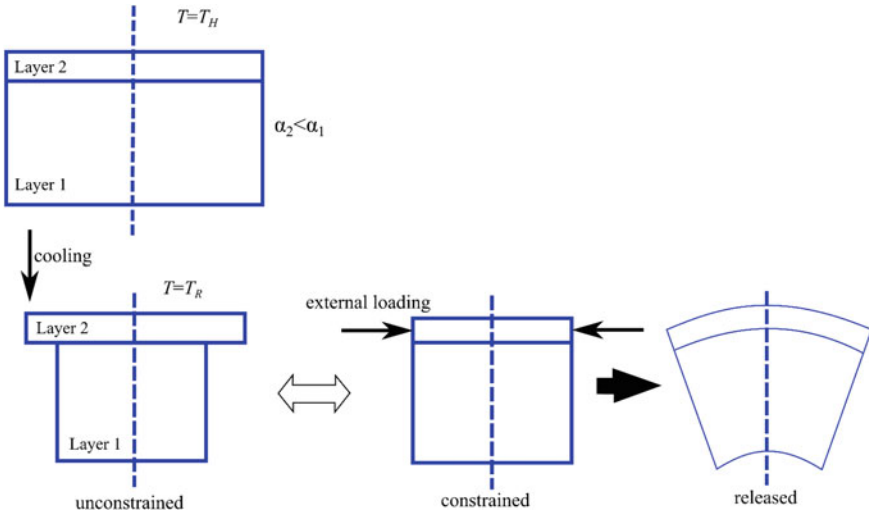


Fig. 15.10 Illustration of natural bending theory for warpage in a multilayered device [67]

where \bar{E}_i is elastic modulus based on geometry configuration; κ_{nat} the curvature caused by natural bending; κ_{app} is applied external curvature; y is the position in thickness direction; h_b is the bending axis; $\bar{\epsilon}_T$ is average thermal strain; ν_i is Poisson’s ratio; A is a geometry factor; η_i is generalized Poisson’s ratio; and ϵ_i^0 is the stress-free thermal strain. The expressions for h_b , $\bar{\epsilon}_T$, and κ_{nat} are given in Eqs. (15.3), (15.4), and (15.5), respectively:

$$h_b = \sum \bar{E}_i H_i h_{mi} / \sum \bar{E}_i h_i \tag{15.3}$$

$$\bar{\epsilon}_T = \sum \bar{E}_i H_i \epsilon_i^0 / \sum \bar{E}_i H_i \tag{15.4}$$

$$\kappa_{nat} = \frac{\sum \bar{E}_i H_i (h_{mi} - h_b) (\eta_i \epsilon_i^0 - \bar{\epsilon}_T - \nu_i A)}{\sum \bar{E}_i D_i [h_i^2 + H_i^2/3 - h_i H_i + h_b (h_b - 2h_{mi})]} \tag{15.5}$$

where h_{mi} and h_i are the coordinates of the midpoint and the top surface of each layer, respectively; and H_i is the thickness of each layer. The equations from natural bending theory can be used for different geometry configurations, such as uniaxial plain stress, uniaxial plain strain, and biaxial model, by choosing corresponding \bar{E}_i , geometry factor A , and η_i (see p. 48 in [67]). The theory provides a convenient tool for a rapid and easy modeling and monitoring the warpage of multilayer structures due to thermal stresses and applied external bending or curvature [67].

Another analytical method for calculating thermal stress and warpage in multilayered structure is the beam-type plate theory proposed by Wen and Barsaran [68], which was mainly developed to consider the stress behavior along the interfaces

between layers due to thermal loading. The analytical model follows Timoshenko’s bi-thermostat beam theory [69] (which was improved by Suhir [70] later), as well as the model proposed by Valisetty [71]. The model treats each layer of an N-layer laminated structure as a beam-type plate with orthotropic material properties. The thermal stress for isothermal loading can be obtained by solving the differential equations for the classical plate theory with beam-like behavior assumptions, and the displacements of each layer can be solved by the introduction of thermal strain terms into Valisetty model [71]. Despite the derived formulation is a little complicated, the model could yield very accurate results in a rapid manner.

15.3.3 Warpage Mechanism and Control Methods

In reality an IC package structure is much more complicated than a simplified multi-layered structure. In this section, a flip-chip package is adopted to demonstrate the development of warpage during different steps of packaging assembly. The structure, primarily comprising of a chip and a substrate, is shown in Fig. 15.11, which is considered as one of the fundamental forms that can be used to study the warpage mechanism.

As shown in Fig. 15.11, the chip having electrically conductive bumps on its active surface is flipped and attached on the top surface of the substrate. An underfill

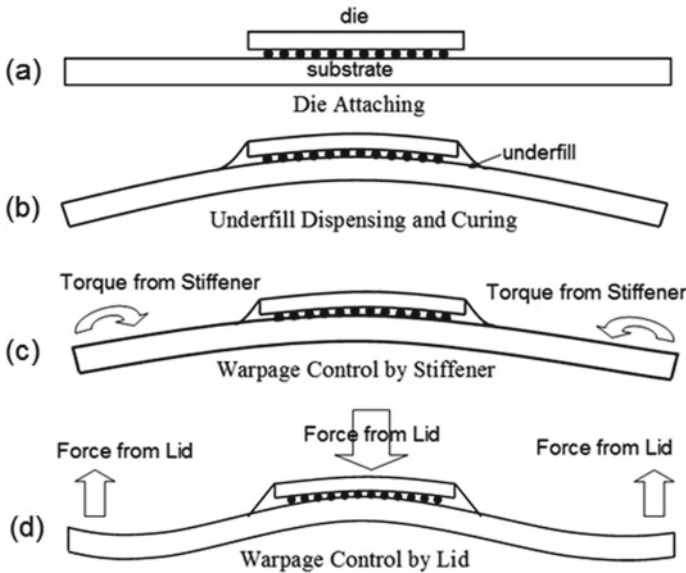


Fig. 15.11 Assembly processes of a flip-chip structure and mechanism of conventional ways for warpage control: (a) die attach, (b) underfill dispensing and curing, and (c), (d) stiffener or lid attach [66]

material is usually dispensed into the gap between the chip and the substrate through a capillary force to protect solder bumps. The degree of warpage will vary during the assembly process of the package. Figure 15.11 shows the basic steps for the assembly process, including: step (a) for die attach process; step (b) for underfill dispensing and curing process; and step (c) or (d) for stiffener/lid attachment process for warpage control. After the die attach step (a), the electrical connection between the die and substrate has been completed, and the warpage at this point is small due to the quick relaxation of the solder bump stress that is caused by the visco-plastic property of the solder material. At this stage, the mechanical connection between the die and substrate is still weak. In order to enhance the mechanical connection and to protect the solder bumps, the underfill is filled into the gap between the die and substrate. The underfill is usually cured at a high temperature, such as 165 °C. During underfill curing, the flip chip package is still very flat, i.e., the warpage at this point is very small due to the same reason as the visco-plastic property of the solder material. However, after the underfill is cured, the die and substrate will be strongly connected, and large warpage can be developed when cooling down to the room temperature or heating up to the reflow temperature. This can also be seen by the natural bending theory, and the reason for the warpage is due to the big CTE difference between the die and substrate. An example of downwards warpage after cooling down to room temperature (also called coplanarity issue) is shown in Fig. 15.11(b). JEDEC specification has defined 8 ml or 200 μm for large flip chip packages as the tolerance limit. However, for a 45 mm \times 45 mm size of flip chip package with a bare die, a warpage over 12 ml or 300 μm could exist.

To reduce the warpage, a stiffener ring or a lid is conventionally applied in the next processing step after underfill curing process [66, 72]. The mechanism of using a stiffener or lid to reduce the warpage is illustrated in Fig. 15.11c, d, where the stiffener or lid applies a force or torque at the edge of the substrate, forcing it to deform upwards. So, it is seen that the conventional ways using a stiffener or lid to reduce the warpage is a way to re-deform the substrate, or in other words, it is a substrate control method. As a result, the stress level in the flip chip package rises when the substrate is re-deformed by the stiffener or lid. For example, for the lip chip package with 45 mm \times 45 mm substrate size and 23 mm \times 23 mm die size, the warpage at room temperature is about 12, 8 and 5 ml for the package types of bare die, stiffener and lid, respectively. Though the lid method gives the lowest warpage, it causes highest stress in package, as compared to the bare die and stiffener packages.

Three main points about the warpage control by using stiffener or lid can be summarized as followings: (1) warpage has been developed after underfill dispensing and curing process. This means that warpage has been frozen in the package, (2) stiffener or lid attach process is done after underfill curing process, and (3) the conventional ways using stiffener or lid to control warpage is only to re-deform the substrate. Therefore, the above methods are substrate-control method, which will introduce additional stress into the package.

15.3.4 A Capped-Die Approach for Warpage Control

A capped-die approach is introduced here, which is illustrated in Fig. 15.12. The approach is based on die-control principle and is fundamentally different from substrate-control based approaches.

As shown in Fig. 15.12, there are four basic steps to assemble a capped-die package (after die-attach process): (a) dispensing underfill material between the die and the substrate; (b) dispensing adhesive material on the top of the die or the stacking dies in 3D; (c) covering the cap onto the die; and (d) concurrently curing the underfill and adhesive materials. Two key differences can be identified between the capped-die flip chip package design and the conventional flip chip packages using stiffener or lid. The first one is that the die cap mainly constrain the die, forming a capped-die, therefore it is a die control method. The second difference is that the underfill material between the die and the substrate is concurrently cured with the adhesive material between the die cap and die. As a result, the CTE between the capped die and the substrate may get matched. Therefore, the warpage after the underfill dispensing and curing process as showed in Fig. 15.11b may be avoided before it is frozen in the package if a die cap with a proper thickness is selected. The same base resin can give a good joint of both underfill and adhesive materials at the die edge region.

One potential failure mode of capped-die flip chip packages is the shear failure of cap edge, which is caused by a high stress around the die edge region when the die cap constrains the deformation of the die during temperature change (Fig. 15.13a). Based on this consideration, an improved die cap design can be used to lessen the risk of this failure mode (Fig. 15.13b). Besides that, using the adhesive material which has the same T_g as that of the underfill material may also help because both materials consistently become softer or harder when temperature passes T_g . It is preferred that both materials use the same resin as their base materials, and their fillers may be different. For example, for the thermal purpose, the fillers of the adhesive material

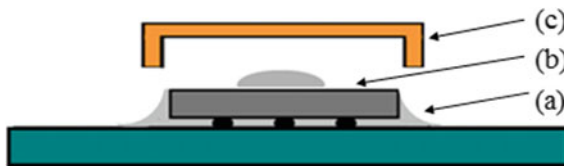


Fig. 15.12 Assembly process for capped-die flip chip package [66]



Fig. 15.13 (a) Potential failure modes for capped-die flip chip packages; (b) A capped-die flip chip package using an improved die cap design [66]

for bonding the die cap with the die may use high conductive fillers, such as silver flakes. Generally, the capped-die approach can be used to protect 3D chip stacks from large warpage, where a cap can be made to constrain the deformation of the stacking dies on a large organic substrate.

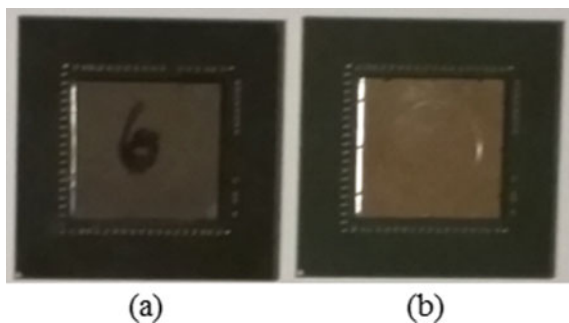
15.3.5 Warpage Characterization by Experimental Testing

Experimental testing by shadow moiré technique can be used to characterize the warpage deformation and evaluate the warpage control methods. Here we compare two different dies: one is a bare die and the other is a capped die, as shown in Fig. 15.14. The test vehicle is a flip chip package with 45 mm × 45 mm substrate size, 23 mm × 23 mm die size and 0.78 mm die thickness. The substrate of the flip chip package has eight metal layers and 0.8 mm core thickness. The CTE and Young's modulus of the core are 11.3 ppm/°C and 32GPa. In the test, the same underfill material is used as the adhesive material for bonding the die cap and the die. Two underfill materials, U6 and U2 are selected. The T_g of U6 and U2 are 95 and 135 °C, respectively.

Two different thickness, 0.2 and 0.4 mm, were tested. It was found that the warpage control using 0.2 mm thickness of die cap is only a little better than that by a stiffener ring, whereas much better warpage control is achieved by 0.4 mm thickness of die cap. In Fig. 15.15, the test data of warpage versus temperature are plotted for both bare dies and capped dies with 0.4 mm thickness. It is seen that when temperature changes, the capped-die package does not warp up and down, and the warpage curve is almost flat and at a warpage value of about 65 μm . This is an important feature that can enhance board-level reliability when mounting the package on a board and under thermal cycling. Also, this feature means that the stress variation inside the package during thermal cycling loading under component level is low, thus giving high component level reliability.

Another feature of the capped-die package is that the warpage is independent of underfill T_g , which is different from conventional flip chip package where higher

Fig. 15.14 Photos of test vehicles for verifying the capped-die concept: (a) bare die package structure, (b) capped-die package structure [66]



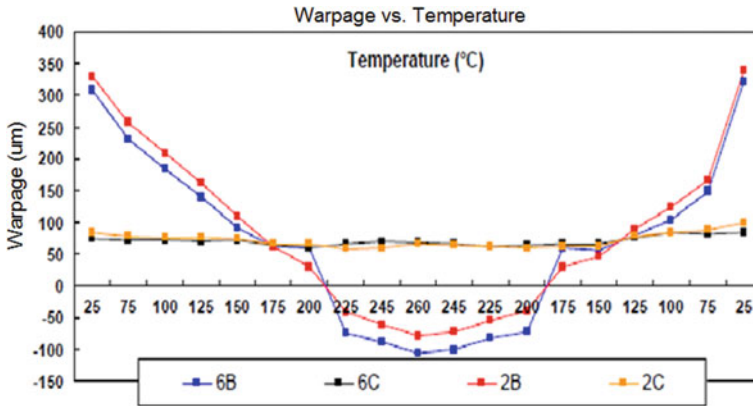


Fig. 15.15 Shadow Moiré data for bare die and capped-die flip chip packages, where the symbol 6B and 2B stand for bare die package structure using underfill material U6 and U2, and 6C and 2C stand for Capped-die package structure using underfill material U6 and U2 [66]

T_g of underfill causes higher warpage at room temperature. It is known that there are two issues for conventional flip chip package to use very high T_g of underfill material: one is higher warpage and the other is higher stress at die corner. The two issues may be avoided by using capped-die flip chip packages. So, for capped-die flip chip package, underfill materials with higher T_g than 120 °C may be applicable. As a result, the underfill material will not transition from hard to soft under application or test loading conditions, improving the reliability of bumps and low-k layers of the package.

It is also interesting to know why the capped-die package has stable warpage at a small value (about 65um). Actually, the small warpage is from the warpage of the flip chip package at curing temperature 165 °C. As can be seen in Fig. 15.15, the bare die package has similar warpage value around that temperature. The warpage value of the capped die package no longer varies with temperature because the CTE of capped die and substrate gets matched. Two factors may cause the small warpage value. One is the residual stress from solder bumps, and the other is the initial warpage of bare substrate due to unsymmetrical metal layers above and below the core.

According to the experimental testing, the capped die concept may give a promising package structure with the advantages of warpage-free control and low stress or high reliability in component as well as board levels for 3D packages. In order to determine the optimized thickness for the cap, FEA analysis can be performed with a parametric study. In the following section, FEM simulation is presented as a preliminary investigation for capped die package design.

15.3.6 Numerical Modeling for Optimizing Warpage Control Design

Numerical simulation is used here to verify the effectiveness of the warpage control method described above and also to optimize the cap design. FEM software ANSYS is utilized to carry out the thermo-mechanical simulation. Several cases are investigated and the results are given below.

(1) Comparison of different control methods

The same flip chip package used in the preceding test vehicle is used as an example for FEM simulation. The stress-free temperature is assumed as the curing temperature of 165 °C, at which the small warpage is not considered based on the test data. Four package structures are compared, including bare die, stiffener, lid and capped-die packages. The stiffener dimension is 0.6 mm thick and 7 mm wide, the lid dimension is 1.5 mm thick and 4 mm foot width, and the die cap is 0.4 mm thick.

The simulation results for the contour plot of the deformation of the four packages at room temperature are shown in Fig. 15.16, where W_{25C} stands for the warpage at room temperature which is defined as the difference between the substrate bottom center and the lowest point. It is seen from Fig. 15.16 that the capped-die package gives an ideal warpage control. Note that the simulation result shown in Fig. 15.16a for the room temperature warpage of the bare die package is in agreement with the test data showed in Fig. 15.15, validating the FEM model.

(2) Optimization of cap thickness to achieve warpage-free packages

There are several variables to be considered when designing a capped die package: the size of die cap, the gap size between the die edge and the cap, and the thickness of die cap. The size of a die cap usually follows the size of the corresponding die, being a little bigger than the die. For the gap size between the die edge and the side of the die cap, a proper value needs to be determined by experimental test for each case. It is suggested that the gap size should be in the range of 100–300 μm. The

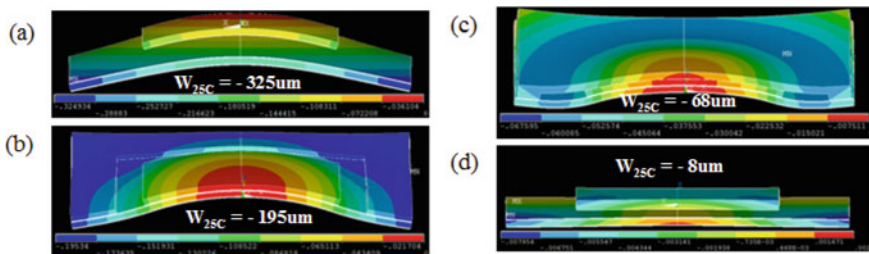


Fig. 15.16 FEM results of warpage for comparing various package structures: (a) bare die; (b) die with stiffener; (c) die with lid; (d) die with a cap [66]

smaller the gap is the stronger constraints that the die cap applies to the die, but the higher risk the failure between the die and the die cap becomes.

Die cap thickness is the third major design parameter, and a proper thickness may vary with different size of flip chip packages. For demonstration, a large size, a medium size and a small size of packages are considered in the FEA simulation. The large package is the same as the test vehicle, i.e., substrate size is 45 mm × 45 mm, die size and thickness are 23 mm × 23 mm and 0.78 mm. The substrate has eight metal layers and 0.8 mm thickness of core. The CTE and Young’s modulus of the core are 11.3 ppm/°C and 32GPa. For the medium sized package, its substrate size is 30 mm × 30 mm, die size and thickness are 17 mm × 17 mm and 0.3 mm. For the small package, its substrate size is 20 mm × 20 mm, die size and thickness are 10 mm × 10 mm and 0.1 mm. The substrate of the medium sized package has six metal layers and 0.4 mm thickness of core. The substrate of the small package has six metal layers and 0.15 mm thickness of core. The core materials of the medium and small packages are the same as the big package.

With trial and error method through multiple rounds of simulations, the proper die cap thicknesses for the three packages are determined as 0.4 mm, 0.3 mm and 0.25 mm, respectively. The simulation results of the contour plot of the deformation of the packages at room and high temperatures are showed in Fig. 15.17, where W_{25C} and W_{260C} stand for the warpage at 25 °C and 260 °C, respectively. It is seen that a warpage-free packaging for the different size of packages are theoretically achieved by a proper thickness of die cap. In practice, it is difficult to achieve such a

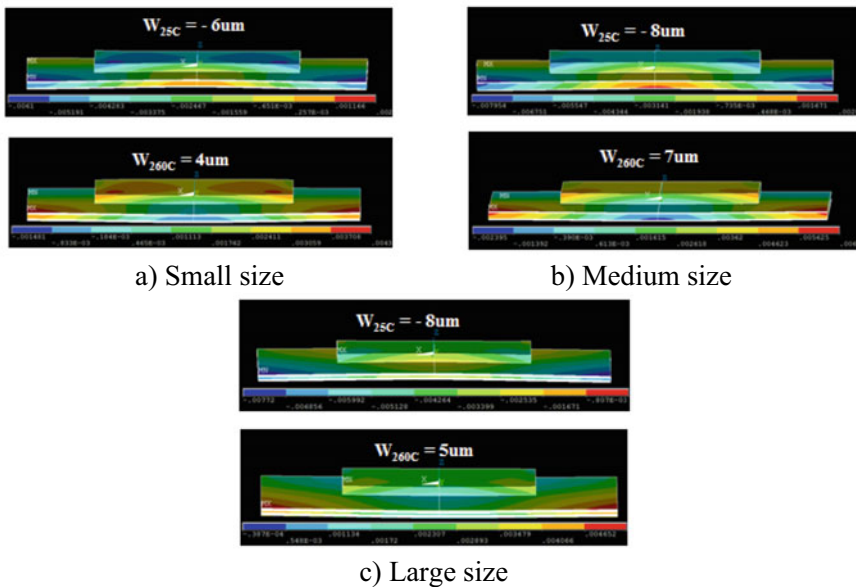


Fig. 15.17 Contour plot of the deformation of different sizes of package at room and high temperatures with optimized cap thickness [66]

small warpage because there is an initial warpage when curing the underfill material. However, it is ideal to achieve a flat warpage curve versus temperature, as shown by the test data in Fig. 15.15.

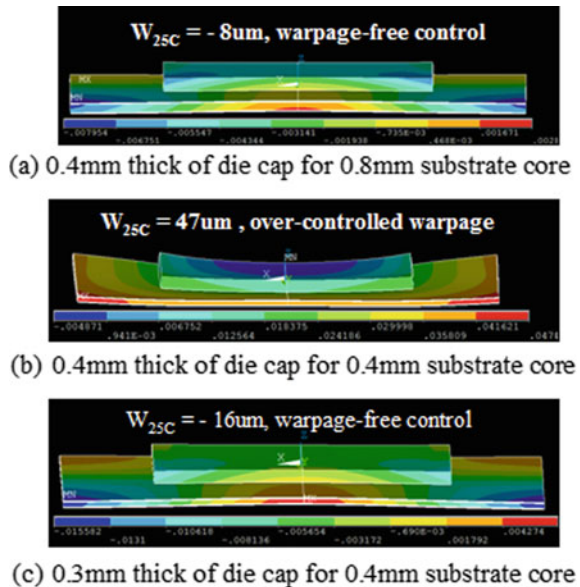
(3) Over-controlled warpage

In the preceding section for achieving warpage-free packaging, the die cap thickness is selected by trial and error method through multiple rounds of simulations for different package sizes. Here, an interesting phenomenon, called over-controlled warpage is shown for the capped-die method by selecting a thicker die cap. In the simulation example, the same large package is used, but a thinner substrate core of 0.4 mm thickness is considered. It has been seen that for 0.8 mm thickness of core, 0.4 mm thickness of die cap gives an ideal warpage control. By using the same 0.4 mm thickness of die cap for the package with the thinner core, the phenomenon of over-controlled warpage can be simulated, as shown in Fig. 15.18b. For the thin core, a thinner die cap, i.e., a 0.3 mm thickness of die cap is proper for an ideal warpage control, as shown in Fig. 15.18c. Note that the conventional stiffener and lid for warpage control never give the phenomenon of over-controlled warpage even though a very thick stiffener or lid is used.

(4) Warpage-free Control for Coreless Substrate

Compared to substrates with core, coreless substrates are desired for packaging application because it can shrink substrate size as well as improve the functional performance of flip chip package. However, flip chip packages using coreless substrates

Fig. 15.18 FEM results for proper die cap thickness versus substrate core thickness [66]



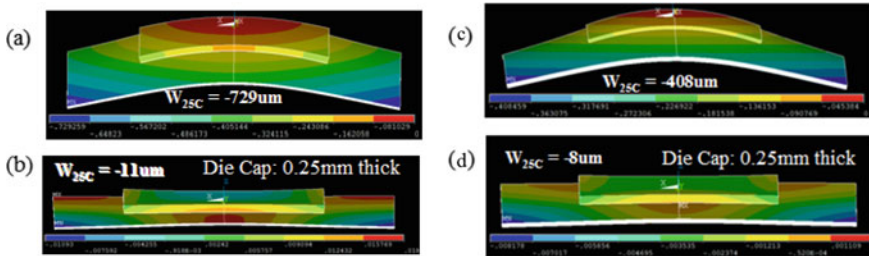


Fig. 15.19 Contour plot of the deformation of large package using 8 layers of coreless substrate (a), (b) and 6 layers of coreless substrate (c), (d) at room temperatures [66]

have very excessive warpage due to the low rigidity of coreless substrates. And it is not easy to control the large warpage using a stiffener or lid for big package size. It is known that coreless substrates exhibit a severe W-shape when its substrate warpage is controlled by stiffener or lid, limiting its applications.

FEM simulation is used to investigate the effect of capped die method for controlling the warpage of packages using coreless substrates. Two package sizes are simulated, and their dimensions and substrate metal layers are the same as the large and small packages done in the preceding section except the substrate type. For comparison, bare die packages are also simulated. Simulation results are shown in Fig. 15.19 for both the large and small flip chip packages. It is seen that the huge room temperature warpage is ideally controlled by a 0.25 mm thickness of die cap. One interesting thing is that for both large and small packages, the warpage-free control happens to be achieved by the same thickness of die cap. Note that the substrate has eight metal layers and die thickness is 0.78 mm in the large package (45 mm × 45 mm), and the substrate has six metal layers and die thickness is 0.1 mm in the small package (10 mm × 10 mm).

15.4 Integrated Stress Analysis for Combining Moisture and Thermal Effects

15.4.1 Introduction

In addition to reliability issues caused by thermal stress, many failures could also occur due to moisture-induced hygroscopic stress and vapor pressure at elevated temperature [14, 15, 25, 73–76]. The problem of moisture absorption and subsequent package failure at elevated temperature has become an important issue concerning the reliability of microelectronic devices. The adverse effects of moisture may include adhesion reduction, hygroscopic swelling, interface delamination and other material degradation problems [16–18, 25, 26, 77]. One extreme case is reflow soldering, in which temperature ramps up quickly to a peak temperature of 260 °C and the

encapsulated moisture in packaging material may evaporate to generate high internal vapor pressure, causing interface delamination and even pop-corning [14, 27, 77–79]. During the highly accelerated temperature and humidity stress test (HAST), moisture-induced stress also becomes very critical to cause package failures as high temperature, high humidity, and high atmospheric pressure are applied.

Due to the deleterious effects caused by moisture, extensive efforts have been made to investigate the moisture diffusion, desorption, and the ensuing mechanical stresses in encapsulated microelectronics devices [16, 26, 80–84]. More importantly, since moisture-induced stress is often accompanied with thermal stress (e.g., during reflow or HAST condition), it is necessary to perform integrated stress analysis to combine all these effects including thermal expansion, hygroscopic swelling, and internal vapor pressure development [17, 63, 77, 85].

To investigate the combined effects of thermal stress and moisture-induced stress, this section starts with the examination of moisture diffusion equation with varying temperature and relative humidity (RH) conditions in Sect. 15.4.2. Then the theory for incorporating moisture-induced stress is given in Sect. 15.4.3, where the concept of effective stress is introduced. The model for calculation of vapor pressure is described in Sect. 15.4.4, in which the void volume fraction and vapor pressure are introduced as two internal field variables. Section 15.4.5 then summarizes the complete set of governing equations including temperature, moisture, displacement, void volume fraction, and vapor pressure based on the literature [17]. Commercial finite element analysis software ANSYS is used to solve the equations. With a representative bi-material configuration, the solutions for moisture diffusion, vapor pressure, and integrated stress effects are presented in Sect. 15.4.6.

15.4.2 Moisture Diffusion

The transient moisture diffusion equation based on the Fick's law [86] is the most widely used in semiconductor engineering, which has a form as:

$$\frac{\partial C}{\partial t} = -\nabla \cdot (-D\nabla C) \quad (15.6)$$

where C is the local moisture concentration and D is the diffusivity (the rate of diffusion), and t is time. However due to dissimilar materials are used in 3D packaging, the moisture concentration C is discontinuous at the interface of different materials, creating numerical difficulty. As a result, a normalized concentration, or the activity of the diffusing material (denoted as ϕ here), is introduced [87]

$$\phi = C/S(T) \quad (15.7)$$

where S is the solubility of each material in a multilayered system at temperature T . When two dissimilar materials are joined at an interface, the normalized concentration is continuous across the interface between the two different materials. Substitute Eq. (15.7) into Eq. (15.6) and the transient moisture diffusion in terms of the normalized concentration becomes

$$S \frac{\partial \phi}{\partial t} + \phi \frac{\partial S}{\partial T} \frac{\partial T}{\partial t} = \nabla \cdot \left[D(S \nabla \phi + \phi \frac{\partial S}{\partial T} \nabla T) \right] \quad (15.8)$$

To describe non-Fickian behaviors, a general form of moisture diffusion constitutive model can be written as [88]

$$J = -SD(\nabla \phi + k_T \nabla T + k_P \nabla P) \quad (15.9)$$

where J is the total moisture flux, k_T and k_P are the factors for temperature gradient driven and hydrostatic pressure driven diffusion, respectively. Here the hydrostatic pressure P is defined as $-\sigma_{ii}/3$.

A comparison between Eqs. (15.8) and (15.9) yields

$$k_T = \frac{\phi}{S} \frac{\partial S}{\partial T} \quad (15.10)$$

which indicates that the normalized diffusion equation in (15.8) is actually a special case of the general moisture diffusion equation without considering the pressure-driven diffusion.

Another normalized variable, wetness w , was also proposed [24], which is:

$$w = C/C_{sat} \quad (15.11)$$

where C_{sat} is the saturated moisture concentration of each absorbent material for a given relative humidity and temperature. Since C_{sat} is not exactly a material property due to its dependence on the relative humidity, it is ambiguous to extend the above approach to a varying humidity condition, such as in a process from soaking to reflow, where relative humidity changes. Another general form for wetness can be used:

$$w = C/C_{sat}(RH_0, T) \quad (15.12)$$

where RH_0 is the reference relative humidity. Compared to Eq. (15.11), the wetness defined in Eq. (15.12) has an unambiguous definition and is continuous at the interface of dissimilar materials. For a varying relative humidity process, the denominator in Eq. (15.12) always refers to a 'reference' saturated moisture concentration at RH_0 and T , even though RH_0 may be different from the current relative humidity conditions. With Henry's law [86]:

$$C_{sat}(RH_0, T) = p_{amb}(RH_0)S(T) = p_g RH_0 S(T) \quad (15.13)$$

where p_{amb} and p_g are partial pressure at RH_0 and saturated vapor pressure of moisture at temperature T .

It has been observed that the saturated concentration is linearly proportional to the ambient relative humidity but not dependent on the temperature, as long as it is far away from the glass transition temperature [14, 80]. In this case, the $C_{sat}(RH_0)$, can be considered as a constant within the interested temperature range. Substituting Eq. (15.13) into Eqs. (15.12) and (15.6), we obtain

$$\frac{\partial w}{\partial t} = \nabla \cdot (D \nabla w) \quad (15.14)$$

which indicates that the thermal-moisture analogy holds true for a temperature-dependent moisture diffusion process when w in Eq. (15.12) is used. The Dirichlet boundary condition for Eq. (15.14) then becomes

$$w|_{bc} = RH_{bc}/RH_0 \quad (15.15)$$

where RH_{bc} is the relative humidity at the boundary.

Other methods like direct concentration approach (DCA), convection-diffusion models [78, 79], have also been developed, where normalization is not required. Particularly, the convection-diffusion model might be useful in the case of rapid heating where vapor flow is important. Details of these models can be referred to the literature [78, 79] and are not covered in this chapter.

15.4.3 Moisture-Induced Strain and Effective Stress Theory

Moisture-induced stress may include both hygroscopic stress and vapor pressure p . To characterize hygroscopic swelling, thermal-moisture analogy can be used:

$$\varepsilon_c = \beta C \quad (15.16)$$

where β is the coefficient of hygroscopic swelling, which is a material property that can be determined by experimental testing with TGA and TMA [14].

To consider vapor pressure induced strain, the effective stress concept is introduced by assuming polymeric material as porous media. As moisture is vaporized, the generated vapor pressure is exerted on the solid phase of the porous material. The coupling phenomena between vapor pressure and matrix material deformation can be described by the effective stress concept, as

$$\sigma_{ij} = \sigma'_{kk} - p\delta_{ij} \quad (15.17)$$

where σ_{ij} is the total stress tensor component, p is the partial water vapor pressure, and σ'_{ij} is the effective stress. Note the vapor pressure p in Eq. (15.17) has a different meaning from the pressure stress (which is denoted by capital P in Eq. (15.9)). Usually, the vapor pressure p in Eq. (15.17) has a positive value.

According to the definition of effective stress, the deformation of porous skeleton is governed by the effective stress only. Therefore, the constitutive model for linear, isotropic elastic material can be described by the effective stress as follows

$$\varepsilon_{ij} = \frac{1+\nu}{E}\sigma'_{ij} - \frac{\nu}{E}\sigma'_{kk}\delta_{ij} + (\alpha\Delta T + \beta C)\delta_{ij} \quad (15.18)$$

where E is Young's modulus, ν is Poisson's ratio, $\Delta T = T - T_o$ with T_o as the reference temperature. It can be seen that both thermal strain and hygroscopic strain are included. The effect of vapor pressure can be revealed by substituting Eq. (15.17) into Eq. (15.18), which leads to

$$\varepsilon_{ij} = \frac{1+\nu}{E}\sigma_{ij} - \frac{\nu}{E}\sigma_{kk}\delta_{ij} + (\alpha\Delta T + \beta C + \frac{1-2\nu}{E}p)\delta_{ij} \quad (15.19)$$

Equation (15.19) indicates that the vapor pressure contributes to the matrix deformation as an additional volumetric strain term. To summarize, the total volumetric strain can be written as

$$\varepsilon^{volu} = \varepsilon_T + \varepsilon_h + \varepsilon_p = \alpha\Delta T + \beta C + \frac{1-2\nu}{E}p \quad (15.20)$$

With Eqs. (15.20), (15.17) can be rewritten as

$$\sigma_{ij} = 2G\varepsilon_{ij} + \lambda\varepsilon_{kk}\delta_{ij} - \left(\frac{E}{1-2\nu}(\alpha\Delta T + \beta C) + p \right)\delta_{ij} \quad (15.21)$$

where G and λ are Lamé's elastic constants. Based on the constitutive law in Eq. (15.21), the deformation equilibrium now becomes [17]

$$G\nabla^2 u_i + (\lambda + G)e_{,i} - \left[\frac{E}{1-2\nu}(\alpha\Delta T + \beta C) + p \right]_{,i} + X_i = 0 \quad (15.22)$$

where u_i is the component of displacement vector, e is the total volumetric strain, X_i is the component of body force vector. Equations (15.21) or (15.22) implies that all applied loads: thermal expansion, hygroscopic swelling and vapor pressure, are in the forms of body loads. The resulting stress/deformation response caused by temperature excursion and moisture diffusion and evaporation can be obtained by solving the

force equilibrium equation with the above strain definitions and the governing equations of heat conduction and moisture diffusion. Since they are virtually independent of the stress state (if stress gradient-driven diffusion mechanism can be neglected), the temperature and moisture concentration fields can be determined, respectively, prior to a stress analysis, and then they can be incorporated into a subsequent stress analysis.

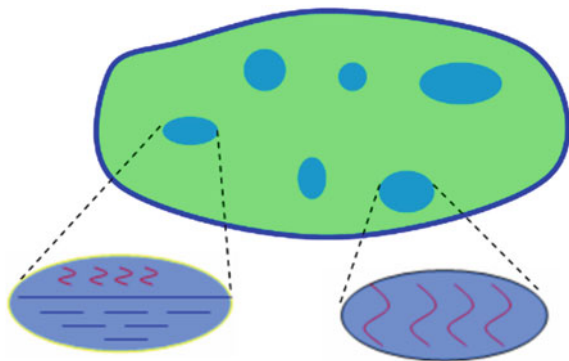
15.4.4 Vapor Pressure Modeling

To evaluate the total strain, vapor pressure must be determined first. Generally, vapor pressure is related to the local moisture concentration and free volume fraction as well (according to the porous media assumption). Although moisture diffusion is analyzed at a macroscopic level, the vapor pressure model should be considered at a microscopic level. Based on this principle, a micromechanics-based vapor pressure model has been proposed [89] and is well accepted in semiconductor packaging. Other vapor pressure models, such as those based on Henry's law [19, 20, 78, 79], do not consider the microscopic effect. Therefore, the micromechanics-based model is adopted and described in this chapter.

The micromechanics-based model considers a representative elementary volume (REV) as shown in Fig. 15.20. The RVE exists at any considered point in porous medium. All moisture absorbed is either in liquid water or vapor form. Moisture collects at the micro-/nano-pores, in free volumes, at the interfaces, and/or in micro/macro-voids. Unbound moisture will evaporate during the reflow process. The total moisture content in a REV is obtained from the local moisture concentration C at a macroscopic level. If the void volume fraction ϕ (or interstitial space fraction) is known, then the 'apparent' moisture density (ρ_a) in pores can be defined as [89]

$$\rho_a = C/\phi \quad (15.23)$$

Fig. 15.20 Representative elementary volume (REV) describing two distinct states of moisture in pores in polymer materials [89]



The calculation of vapor pressure starts with determining the state of moisture in the voids. If the voids contain only vapor and the vapor pressure reaches the saturation point, the density of saturated water vapor, ρ_g , can be expressed according to the ideal gas law:

$$\rho_g(T) = \frac{p_g(T)}{RM(\text{H}_2\text{O})T} \quad (15.24)$$

where $p_g(T)$ is the saturated vapor pressure at a given temperature; the gas constant $R = 8.314 \text{ J (mol K)}^{-1}$, and the water molecular mass $M(\text{H}_2\text{O}) = 18 \text{ g mol}^{-1}$. The vapor pressure is then evaluated by comparing ρ_a with ρ_g :

$$p(T) = \begin{cases} \frac{RT}{M(\text{H}_2\text{O})\phi} \cdot C, & \rho_a < \rho_g \\ P_{sat}(T), & \rho_a \geq \rho_g \end{cases} \quad (15.25)$$

Equation (15.25) provides a model to calculate vapor pressure. It indicates that vapor pressure is related to moisture diffusion (moisture concentration C), and temperature field (T), as well as the void volume fraction ϕ . The void volume fraction may be considered as a damage field variable. The growth of the void must follow the continuity equation, as follows [17, 90],

$$\dot{\phi} = (1 - \phi)\dot{u}_{i,j} \quad (15.26)$$

which is coupled with the continuum's deformation in Eq. (15.22).

15.4.5 Governing Equation for Integrated Stress Analysis

From the analysis in the previous sections, the basic field variables of the problem include: temperature T , normalized moisture concentration ϕ , displacement vector u_i , internal vapor pressure p , and void volume fraction ϕ . The vapor pressure p and void volume fraction ϕ can be considered as internal field variables. Void volume fraction ϕ is a damage parameter to describe the progression of damage in a system of interest. The governing equations for solving the problem are summarized as follows [17]:

$$\frac{\partial T}{\partial t} = D_T \nabla^2 T \quad (15.27)$$

$$S \frac{\partial \phi}{\partial t} + \phi \frac{\partial S}{\partial t} = \nabla \cdot [D(S \nabla \phi + \phi \nabla S)] \quad (15.28)$$

$$G\nabla^2 u_i + (\lambda + G)\varepsilon_{,i} - \left[\frac{E}{1 - 2\nu}(\alpha\Delta T + \beta C) + p \right]_{,i} + X_i = 0 \tag{15.29}$$

$$\dot{\phi} = (1 - \varphi)\dot{u}_{i,j} \tag{15.30}$$

where D_T is the thermal diffusivity. As normalized concentration is used, the equations can be solved for multi-material system such as 3D chip stacks. It is seen that an integrated stress modeling during reflow soldering requires five types of modeling, namely (1) moisture diffusion during moisture preconditioning and reflow, (2) thermal modeling, (3) hygro-mechanical modeling, (4) thermo-mechanical modeling, and (5) vapor pressure modeling.

15.4.6 Case Studies

To demonstrate the application of the integrated stress theory, a bi-material system is used to perform the analysis as shown in Fig. 15.21. The bi-material system can be viewed as the most fundamental structure in a 3D device. In the example, copper is chosen for material 1 and molding compound is chosen for material 2. The geometry and material properties are given in Tables 15.3, 15.4 and 15.5, respectively.

Fig. 15.21 A bi-material assembly for integrated stress analysis

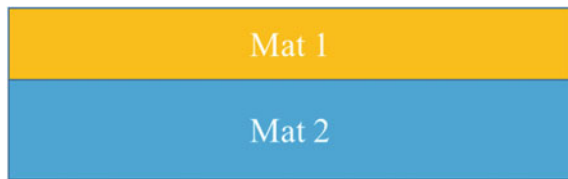


Table 15.3 Bi-material assembly geometry [17]

Geometry	Copper	Mold compound
Thickness (mm)	0.2	0.3
Length (mm)	2	2

Table 15.4 Temperature-dependent material properties for mold compound [17]

Temperature (°C)	CTE (ppm/°C)	E (GPa)
85	20	20.0
125	20	20.0
155	40	5.0
195	40	1.0
265	40	1.0

Table 15.5 Material properties of bi-material assembly [17]

	Copper	Mold compound
C_{sat} at 85°C/85%RH ($\mu\text{g}/\text{mm}^3$)	N/A	4.0
Diffusivity pre-factor D_o (mm^2/s)	N/A	5.0
Diffusivity activation energy Q (ev)	N/A	0.4
Initial void volume fraction	N/A	0.05
CTE (ppm/°C)	17	see Table 15.4
Young’s modulus (GPa)	130	see Table 15.4
Poisson’s ratio	0.34	0.3
Coefficient of hygroscopic swelling ($\text{mm}^3/\mu\text{g}$)	N/A	0.5×10^{-3}

The moisture diffusivity of molding compound is dependent on temperature, which can be described by the Arrhenius equation:

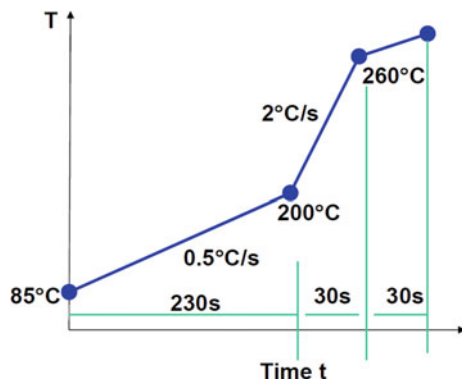
$$D = D_o e^{-\frac{Q}{RT}} \tag{15.31}$$

where D_o is a pre-factor, and Q is the activation energy (ev). Copper does not absorb moisture, therefore the diffusivity and saturated moisture concentration are assigned to very small (e.g. 10^{-6} lower) values. The values of D_o and Q are shown in Table 15.5.

The assembly initially experiences preconditioning at 85 °C/85%RH for 196 h, followed immediately by a reflow process. The time history of the reflow process is depicted by Fig. 15.23. According to the literature, the reflow temperature profile affects moisture distribution greatly [22] (Fig. 15.22).

Sequentially coupled moisture diffusion, vapor pressure, and integrated stress analysis is performed based on the governing equations described in Sect. 15.4.3.

Fig. 15.22 Reflow temperature profile used for the integrated stress analysis [17]



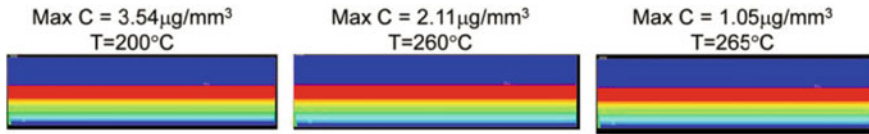


Fig. 15.23 Moisture contours at different temperatures [17]

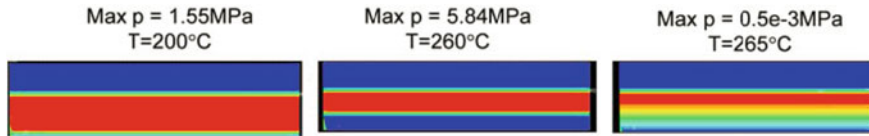


Fig. 15.24 Vapor pressure contours at different temperatures [17]

To solve the multi-field equations, we apply the thermal-moisture analogy and built-in user-defined swelling functions in ANSYS. The results are given and discussed in details below.

Figure 15.23 shows the absolute moisture concentration contour plots at three different temperatures during reflow. It can be seen that the maximum moisture concentration at copper/mold compound interface decreases significantly with the increase of reflow temperature.

Figure 15.24 gives the vapor pressure contour plots at the same three temperatures based on the micromechanics approach. It can be seen that the vapor pressure increases with the increase of temperature from 200 to 260 °C, despite of the decrease in the moisture concentration. However, with more moisture lost, vapor pressure starts to decrease even the temperature continues to rise to 265 °C. This indicates that there is insufficient residual moisture to keep the high vapor pressure as the desorption process goes on.

After the moisture concentration and vapor pressure fields are determined, they can be incorporated into a subsequent stress analysis using Eq. (15.22). Figure 15.25 shows the comparison of moisture distributions at 1 and 18 h in preconditioning under 85 °C/85%RH, and the corresponding deformed shapes of the assembly and the maximum von Mises stresses in mold compound. In the beginning of preconditioning, the assembly is in convex shape due to thermal mismatch from stress free temperature of 160–85 °C. Afterwards, mold compound swells with moisture absorption, and the assembly deforms from convex to concave shape. At the same time, stress level in mold compound increases significantly due to hygroscopic swelling.

To better demonstrate the importance of integrated stress analysis which consider the effects of hygroscopic swelling and vapor pressure, three types of stress analysis are compared: (1) Thermal load only. In this analysis, only thermal mismatch is considered at the reflow. Since this is a linear analysis, the stress state depends on the final temperature state only. (2) Combined thermal and hygroscopic swelling loads. At different times in the studied process (either in preconditioning or reflow stage),

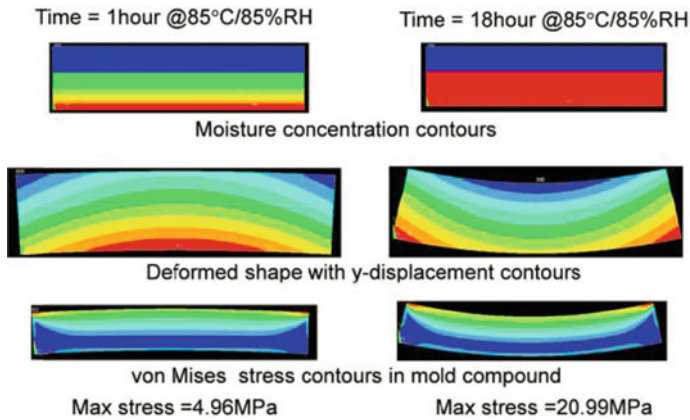


Fig. 15.25 Comparison of moisture concentration, deformation, and stress at different time in preconditioning process [17]

moisture distributions can be applied as body loads. The stress state depends on the temperature state and instantaneous moisture distributions. (3) Combined thermal, hygroscopic swelling and vapor pressure loads. In this case, Eq. (15.22) is used to apply a body load which comprises both hygroscopic swelling and vapor pressure.

Numerical results from the above three types of analysis are summarized in Tables 15.6, 15.7 and 15.8. Table 15.6 shows the maximum warpage, maximum von Mises stresses in copper and mold compound, respectively, at three different times during reflow: 200, 260, and 260 °C after 30 s hold. At 200 °C, hygroscopic

Table 15.6 Maximum warpage (W) and von Mises stresses (σ_e) in copper and mold compound at 200 °C [17]

	W (mm)	σ_e , MC (MPa)	σ_e , Cu (MPa)
Thermal stress only	0.4e - 3	2.4	8.7
Thermal + hygroscopic	0.7e - 3	4.9	17.3
Thermal + hygroscopic + vapor pressure effect	1.0e - 3	6.3	22.9

Table 15.7 Maximum warpage (w) and von Mises stresses (σ_e) in copper and mold compound at 260 °C [17]

	W (mm)	σ_e , MC (MPa)	σ_e , Cu (MPa)
Thermal stress only	1.3e - 3	6.0	21.9
Thermal + hygroscopic	1.5e - 3	7.2	27.5
Thermal + hygroscopic + vapor pressure effect	2.1e - 3	11.2	38.9

Table 15.8 Maximum warpage (w) and von Mises stresses (σ_e) in copper and mold compound at 260 °C after 6 s hold [17]

	W (mm)	σ_e , MC (MPa)	σ_e , Cu (MPa)
Thermal stress only	1.3e – 3	6.0	21.9
Thermal + hygroscopic	1.4e – 3	6.3	24.7
Thermal + hygroscopic + vapor pressure effect	1.4e – 3	6.3	24.7

swelling and vapor pressure induced stresses play significant roles in final stress state (Table 15.6). Results indicate that the effects of hygroscopic swelling and vapor pressure cannot be overlooked. Comparing Tables 15.7 and 15.8, it is apparent that the effects of hygroscopic swelling and vapor pressure fade when more moisture is lost at the same temperature 260 °C. The maximum stress state can be determined at a certain temperature with given reflow profile and the maximum stress may not occur at the peak reflow temperature since moisture continues to escape during temperature rise.

15.5 Summary

In this chapter, thermal/moisture-induced stresses and their effects on 3D packaging have been discussed. Techniques for thermal-mechanical and moisture modeling are introduced to characterize the stresses and the corresponding issues in 3-D packaging under both thermal and moisture loadings. Evaluation based on these modeling techniques can help to enhance the understanding of the failure mechanisms, provide guidance for package design, and improve the performance and reliability of 3D products.

In Sect. 15.2, the effects of die-level thermal stress on TSV structures are investigated. The thermal stress in TSV is induced by the CTE mismatch between Cu via and Si and has triaxial stress state due to the confinement of the Si substrate. To describe the distinct nature of near-surface stress in TSV structures, a semi-analytic 3-D solution has been developed for an isolated TSV embedded in the silicon wafer. As a numerical approach, finite element method has been used to analyze the thermal stresses in 3-D integrated structures and to evaluate stress-induced keep-out zone. Experimentally, wafer curvature method and micro-Raman spectroscopy are combined to measure the thermal stress in and around TSVs. The microstructure of Cu plays an important role in affecting the stress relaxation and residual stress after thermal cycling. The microstructure also has significant implications on via extrusion reliability, as grain growth, plasticity, and diffusional creep are underlying relaxation mechanisms causing via extrusion. It is important to optimize the processing conditions of TSVs, including the electroplating chemistry and annealing, to control the thermal stress and improve reliability of TSV structures.

In Sect. 15.3, the effects of thermal stress at package level of 3D packaging are discussed, with a focus on the reliability issue associated with warpage. Thermal-stress induced warpage in multilayered structures can be evaluated by analytical modeling. Two theories, the natural bending theory and the beam-like plate theory, are introduced. To identify the warpage mechanism during assemble process, a flip-chip package is studied, showing that warpage usually occurs after underfill is cured followed by a sudden temperature change. The convectional control methods, such as applying stiffer ring or a lid, are based on substrate control principle and thus may introduce additional stress into the package. On contrary, the capped-die approach, which is based on die control principle, is considered more efficient and is able to achieve warpage-free design in 3-D packaging. The key control mechanism of the capped-die approach is to reduce the mismatch of CTEs between the chip and substrate. The capped-die concept proves more effective than the conventional control methods through both experimental testing and numerical modeling. Ideally, it is possible to achieve warpage-free packaging in the full range of temperature variation with the approach. With warpage being controlled at a small and stable level, the corresponding reliability issues caused by thermal stress at package level can be effectively mitigated.

In Sect. 15.4, moisture-induced stresses, which includes both hygroscopic stress and vapor pressure, have been considered together with thermal stress in order to take account of the circumstance with both high temperature and high humidity (e.g., reflow process or HAST environment). To couple moisture and thermal effects, a damage micromechanics continuum theory is presented, which allows the coupling of moisture diffusion, heat conduction, matrix material deformation, as well as the growth of void volume fraction. The total strain is formulated as the combination of hygroscopic swelling, thermal expansion, and vapor-pressure induced strain. A new constitutive law is then established according to the effective stress concept. A complete set of governing equations are provided for integrated stress analysis, which can be solved by thermal-moisture analogy and built-in user-defined swelling functions in ANSYS. A bi-material assembly is used to illustrate the integrated analysis of moisture diffusion, vapor pressure evolution and stress determinations. The results show that the moisture- induced stresses play an important role in final stress state during reflow, as the moisture-induced deformation (which includes both hygroscopic swelling and vapor pressure induced strain) can be as significant as thermal expansion. It is concluded that the theory for integrated stress analysis can serve as a useful tool to analyze, understand, and improve the reliability of a 3-D IC package in circumstance like reflow soldering or HAST conditions where moisture-induced stress cannot be overlooked. With the normalized concentration used in diffusion equation, the theory can be applied to any 3D assembly that has many dissimilar materials. It is worth noting that there is still no consensus of vapor pressure model to be used in microelectronics packaging. However, the theoretical framework provided in this chapter does not depend on the vapor pressure model adopted.

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