Double Gate Tunnel FET Versus Double Gate MOSFET: Electrical Properties Comparison

Menka Yadav

Abstract In this manuscript, an investigation, with the help of extensive device TCAD Sentaurus simulations, is presented for comparative analysis to understand the effects of variations in gate and drain potential on the device electrical properties of such silicon double gate tunnel field effect transistor (DG TFET) as well as DG MOSFET. The study is mainly focused at electrical properties like electrical channel potential, electric channel field, electron density, electron quasi-fermi potential in channel, drain current, and threshold voltage calculation. From the TCAD simulated study, it is found that electrical properties in the channel region of DG TFET are quite different from DG MOSFET. It is observed that the central channel potential of DG TFET is not pinned to a fixed potential even after threshold voltage (as in case of DG MOSFET occurs), but it initially increases and later on decreases with increasing gate voltage. It is also observed that the threshold voltage extracted with maximum transconductance method or linear extrapolation (LE) and electron quasi-fermi potential of DG TFET are much higher than the DG MOSFET's one. It is also observed that just on-set of inversion is not sufficient condition for DG TFET threshold voltage. These differences are explained in this paper with proper physics reasoning.

Keywords BTBT · DG tunnel FET · Electric potential · Electron density · Electric field · Threshold voltage · Electron quasi-fermi potential · Drain current

1 Introduction

Nowadays, we are living the era of More-Moore and More than Moore, this is because of the continuous down scaling of the benchmarked device—metal–oxide–semiconductor field effect transistor (MOSFET) which inevitably leads to fundamental physical limits that can no longer be overcome by technology innovation alone. Limits for conventional MOSFETs are: subthreshold leakage which limits the subthreshold

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P. K. Mallick et al. (eds.), *Electronic Systems and Intelligent Computing*, Lecture Notes in Electrical Engineering 686, https://doi.org/10.1007/978-981-15-7031-5_75

swing (SS_{MOSFET}) to 60 mV/dec at room temperature and higher OFF state device current, I_{off}, at lower device dimensions. Hence, new device concepts are needed.

The tunnel FET, based on the interband tunneling effect, has recently been subject to a variety of both theoretical and experimental studies [1–4]. It is being demonstrated that the device has several superior properties as compared to the benchmarked MOSFET device.

TFETs have the possibility to overcome the drawbacks of MOSFET; therefore, they are widely studied in recent years [5, 6]. TFETs may have SS_{TFET} lesser than MOSFET at room temperature because SS_{TFET} is independent of temperature, therefore, TFETs can be a good option to operate at higher temperatures, without any compromise on reliability. TFETs works on band to band tunnelling (BTBT) principle; therefore, it could be scaled down without any degradation in its electrical properties [7]. For example, I_{off} and threshold voltage (V_{Th}) in MOSFET depend on the gate length scaling but in case of TFET, these properties do not change with further gate length scaling [8]. Because of its superior properties, TFETs can be used in lower power applications such as SRAMs.

In this manuscript, electrical properties of DG TFET like electric potential, electric field, electron density, electron quasi-fermi potential, etc., in channel region are comparatively studied with DG MOSFET. Threshold voltage for both devices using maximum transconductance method or linear extrapolation method (LE) is also presented, as explained in [9].

The organization of the paper is as follows: Sect. 2 describes the device structure and simulation setup, Sect. 3 describes simulation results and discussions and Sect. 4 concludes the work.

2 Device Structure and Simulation Setup

The DG TFET device structure under study is presented in Fig. 1. Here, a transverse cut AA' is taken. Cut AA' is used to explore the results at point A, which is termed as surface or Si-oxide interface and at the mid of the channel, i.e., at mid of cut AA', which is termed as the mid-channel point. The device parameters are listed in Table 1. For DG MOSFET also same device parameters are used, except phosphorus source doping is used.

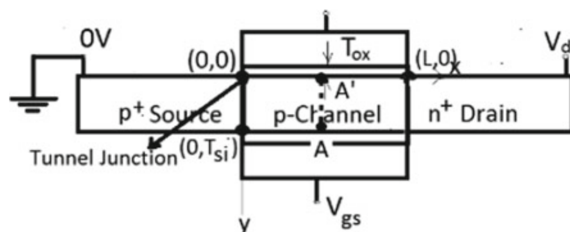

Fig. 1 Double gate tunnel FET device structure

Table 1 Double gate tunnel FET device parameters

	Parameter	Value
1.	Gate length, L_g	50 nm
2.	Source doping, *p*-type	10^{20}/Cm^2
3.	Channel doping-*p*-type	10^{17}/Cm^2
4.	Drain doping. *n*-type	5×10^{18}/Cm^2
5.	Gate oxide, HfO_2, ϵ_{ox}	22, ϵ_o
6.	Gate oxide thickness, T_{ox}	3 nm
7.	Silicon body thickness, T_{Si}	10 nm

Two-dimensional TCAD device simulations are done using TCAD device simulator Sentaurus [10]. To model BTBT, electric field dependent Kane's [11]- model is used for physics of the device. Since the source and drain regions are heavily doped and tunneling current is strongly dependent on band gap, band-gap narrowing model, *OldSlotboom*, is also included. High field saturation mobility model for electrons and holes is included. Shockley Reed Hall (SRH) model is used as carrier recombination model. Simulations are done for various gate voltage and drain voltages. The doping in the *n*-drain, *p*-source, and *p*-layer is kept constant at the optimum value and doping profiles used are abrupt. For *n*-type impurity, phosphorus, boron as a trivalent impurities are used and gate work function is set as 4.25 eV.

3 Simulation Results and Discussions

In this section, the simulated results for DG TFET at the surface, i.e., at point A and at the mid of the channel are presented and compared with DG MOSFET results. Electric properties at Silicon- HfO_2 interface of AA' cut, i.e., at point A are termed as surface electric properties and at mid of AA', i.e., center of the channel are termed as mid-channel properties.

3.1 Drain Current and Gate Threshold Voltage

Gate voltage, V_{gs} versus drain current, I_{ds} is shown in Fig. 2 for DG MOSFET and DG TFET. In Fig. 3, gate threshold voltage versus drain voltage is shown for both devices. We observed that DG TFET has higher threshold voltage than DG MOSFET. Here, the threshold voltage is extracted using maximum transconductance method, as given in [9], for MOSFETs. DG MOSFET has lower threshold voltage as compared to DG TFET because in DG MOSFET after on-set of inversion device becomes ON, while in case of TFET, on-set of inversion is not sufficient condition to make the device ON, as given in [12]. A saturation in the drain current is seen

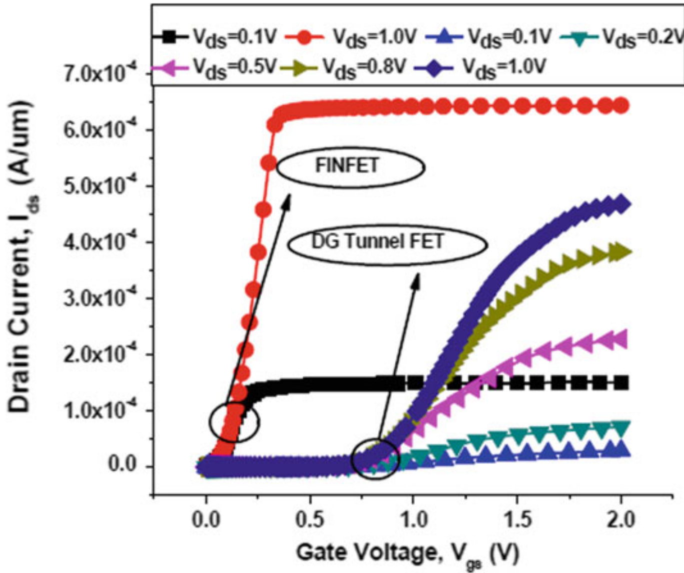

Fig. 2 Drain current versus applied gate voltage for DG TFET and DG MOSFET

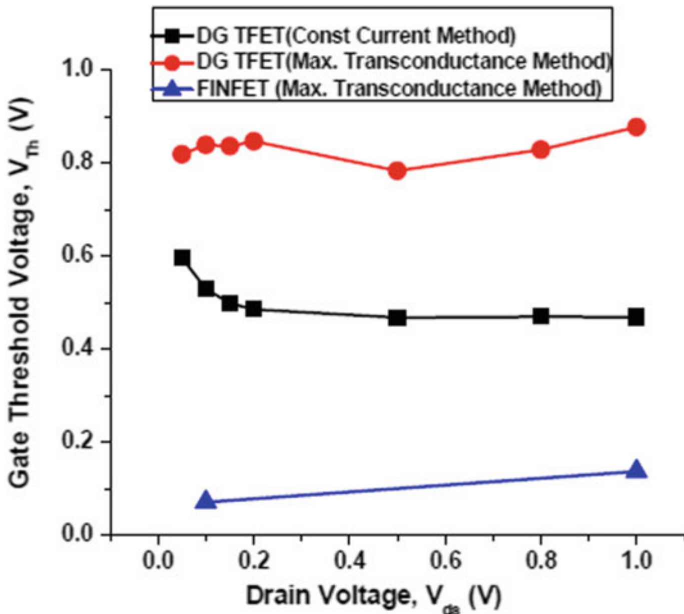

Fig. 3 Threshold voltage for DG TFET and DG MOSFET

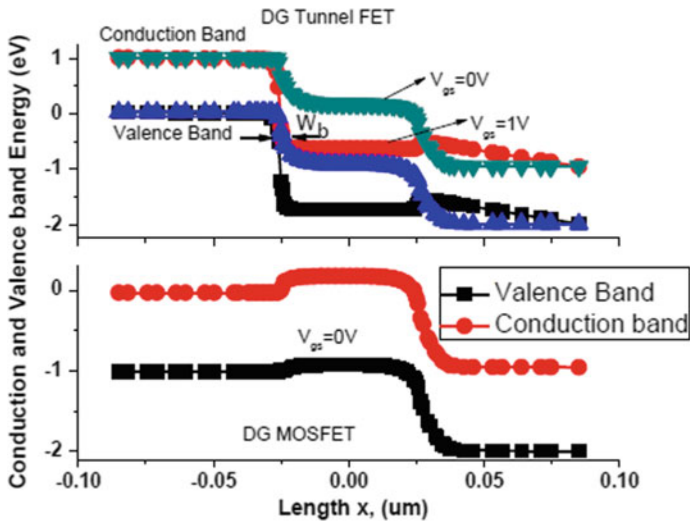

Fig. 4 Energy band diagrams for DG tunnel FET and DG MOSFET at V_{ds} =1.0 V

after a particular applied gate voltage, in DG MOSFET. This is because velocity saturation is obtained by electrons, hence the (drift) current starts to saturate. While in DG, TFET current is increasing with increase in applied gate voltage, V_{gs}, this is because after threshold voltage (which is higher than DG MOSFET), the band to band tunneling (BTBT) generation rate, G_{btbt}, increases at a rapid pace and this rate is also controlled by applied drain voltage, therefore, as we increase drain voltage the tunnel barrier width, w_b decreases, as shown in Fig. 4; hence, average electric field across the tunnel junction gets increased and we get

-larger current for larger drain voltages [13–15]. The tunneling generation rate is given in Eq. (1).

$$G_{btbt} = A\frac{E_{avg}^2}{\sqrt{E_g}}\mathrm{Exp}\left(BE_g^{3/2}/E_{avg}\right) \tag{1}$$

where

A 3.5×10^{21} $eV^{0.5}/cm\ s\ V^2$
B 22.6×10^6 $V/cm\text{-}eV^{3/2}$
E_g Silicon energy band gap
E_{avg} Average electric field along tunnel path

Here tunneling is occurring at source end denoted by circles in Fig. 1.

3.2 Electron Quasi-Fermi Potential

In Fig. 5, electron quasi-fermi potential (eQFP) versus drain voltage is shown for DG TFET. For DG MOSFET, eQFP although varies with applied drain voltage, V_{ds} its range is between 0 and 0.1 V even when V_{ds} is varied between 0 and 1.0 V. This is because the applied drain voltage sees a reversed biased *p*-*n* junction at the drain/channel junction, therefore, whole drain voltage is applied across this junction and channel eQFP remains zero always.

In case of DG TFET, *p*-*n* junction is formed at source/channel junction, therefore, the applied drain voltage can be seen at the junction and this sets channel eQFP equal to drain voltage, below threshold voltage as shown in Fig. 5. After gate threshold, there is enough tunneling current to make the device ON and hence the channel/drain region will act as a series connected resistance, since now channel is a resistive region so there will be a potential drop equal to the drain current times of the channel resistance. This will make the channel eQFP $\neq V_{ds}$; hence, there is a drop as seen at higher gate voltages, and this pattern is also followed at higher drain voltages with same physics.

But, in subthreshold regime, a hip hop change at higher drain voltages is seen. This is because for higher drain voltages, the whole channel *p*-type (since inversion is not set for lower gate voltages, as is clear from Fig. 6a) will work like a potential barrier, therefore, a fall in eQFP seen for higher drain voltages, which after onset of inversion follows the same physics as described in above paragraph.

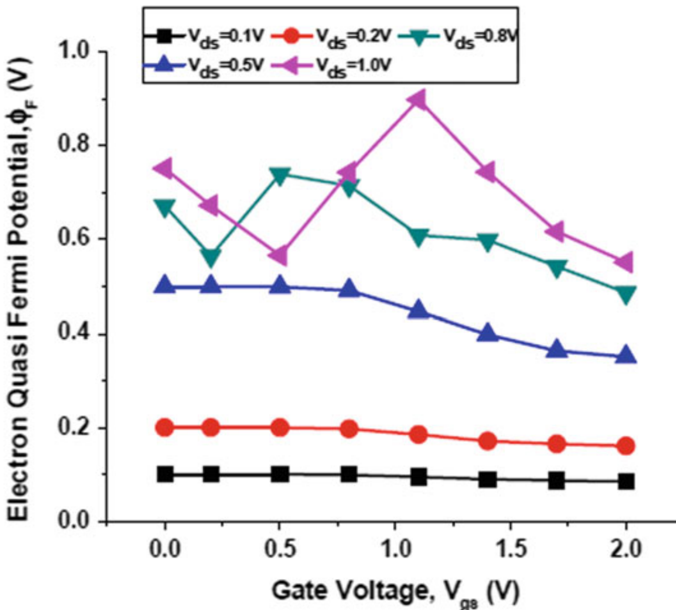

Fig. 5 Electron quasi-fermi potential at AA' cut for DG TFET

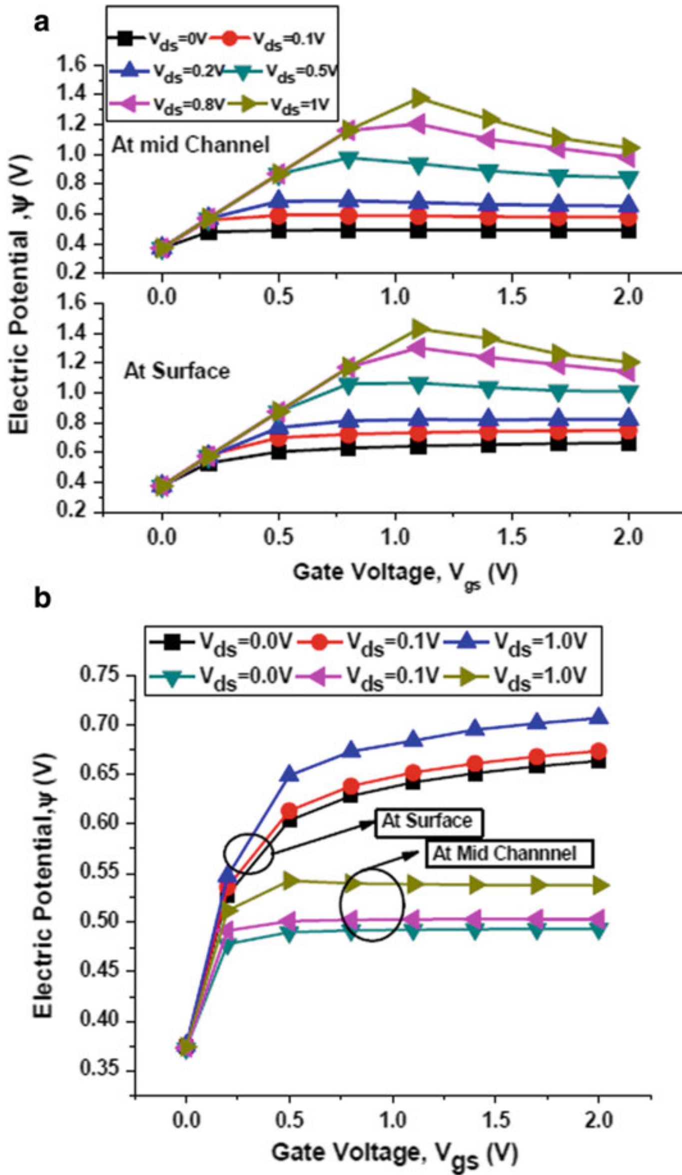

Fig. 6 Electric potential at surface and the mid-channel point for DG TFET and DG MOSFET. **a** Electric potential at surface and the mid-channel point for DG TFET. **b** Electric potential at surface and the mid-channel point for DG MOSFET

3.3 Electric Potential

Surface electric potentials and mid-channel potentials for 50 nm gate length DG TFET and DG MOSFET are shown in Fig. 6. For DG MOSFET, the surface potential always monotonically increases with increasing gate voltage, while mid-channel potential gets pinned to a fixed value for a fixed drain voltage, after threshold voltage as shown in Fig. 6b. It is also observe that the surface potential is always greater than mid-channel potential at any drain or gate voltage. This pattern of potential is also seen in literature [16, 17]. The shape of the pattern of potential will not change with the applied drain voltage, but for higher drain voltages, higher channel potentials are obtained. Since source/channel and drain/channel junctions in DG MOSFET are symmetric, therefore, there will be attraction of electrons from both source and drain regimes hence the symmetric pattern in the mid-channel and surface potential is found even if we change the drain voltage from 0.1 to 1 V.

In case of DG TFET as shown in Fig. 6a, surface potential and mid-channel potentials for lower V_{ds} (upto 200 mV) is seen constant, however, when we increase the drain voltage V_{ds} to 0.5 V and beyond this value, a monotonic decrease in -surface and mid-channel electric potentials is seen, this property of DG TFET is different from the potential pattern of DG MOSFET. At the same time, the surface potential is always greater than the mid-channel potential in DG TFET (i.e., the parabolic shape of the potential profile along AA' cut line). However, it is observed that the potential profiles for both DG TFET and DG MOSFET are parabolic in shape along AA' cut line, but still we are observing a different pattern in surface potentials and mid-channel potentials in both the devices. This is because a crossover point in potential is observed in case of DG TFET in oxide regime after gate voltage is further increased beyond threshold voltage as is clear from Fig. 6a.

It is also observed that surface potentials and mid-channel potentials for DG TFET are always much higher then surface and mid-channel potentials of DG MOSFET respectively. Potentials for DG TFET increase much more at higher applied drain voltages as compared to DG MOSFET, this happens because of sharper energy band bending in case of TFET, as shown in Fig. 3.2.

The possible reason for this decrease in both surface and mid-channel potential is the asymmetric device structure of TFET. Because of asymmetric device structure when the applied gate voltage is increased (below threshold voltage), since there is no tunneling from source to channel regime, therefore, the charge from drain/channel junction is attracted at surface (this is because of drain/channel tunneling at very low gate voltages or direct electrons are attracted from drain after inversion layer is formed), since there is no tunneling below threshold voltage, both surface and mid-channel potentials will increase monotonically as in case of DG MOSFET but after gate voltage goes beyond threshold voltage of the DG TFET device, the tunneling junction width at the source/channel junction gets lowered and more electrons will come to the channel, and these are related by Eq. (2) for both DG MOSFET and DG TFET. Since in DG MOSFET, there is zero eQFP hence surface potential increase, but in case of DG TFET eQFP is non zero and decreasing after threshold voltage (as

mention in Sect. 3.2), but electron density increases due to excess electrons generated from BTBT. This will decrease the channel potential as the gate voltage is increased.

In case of DG TFET, the nonzero eQFP will make its channel potential higher than the DG MOSFET's one.

3.4 Electric Field

In this subsection, total electric field ($E = (E_x^2 + E_y^2)^{0.5}$) versus applied gate voltage is presented for various drain voltages, V_{ds} for both devices. As shown in Fig. 7, surface electric field for DG MOSFET is almost independent of the applied drain voltage, while it decreases for DG TFET with applied drain voltage. While the mid-channel electric field increases with applied drain voltage in both the devices.

Because of symmetry in Double gate structures, the y-component of electric field will be zero at the mid channel and from x-component is more depending on the applied drain voltage. Hence, as the drain voltage increases, a corresponding increase in total electric field is solely due to E_x-component in both the devices. In DG TFETs, for lower gate voltages, the shape of the surface potentials as shown in [18] is not constant in the mid channel, due to sharp energy band bending in the device, as shown in Fig. 3.2, therefore higher mid-channel electric field is seen for lower gate voltages for DG TFETs. In case of surface electric field, a stronger E_y—component for lower drain voltages makes the total electric field higher. As the drain voltage is increased, it will make E_x stronger and E_y will become a bit weaker, since higher the drain voltage means, we need to apply higher gate voltage to make the surface potential constant, as shown in [12], therefore, the curves are shifted downwards for surface potential.

3.5 Electron Density

In this subsection, electron density for both devices is comparatively studied. Analytical expression for electron density in the channel is given by Eq. (2).

$$n(x, y) = \frac{n_{i,\mathrm{eff}}^2}{N_\mathrm{a}} e^{\left(\frac{\psi(x,y) - \phi_{\mathrm{Fn}}(x)}{V_\mathrm{T}}\right)} \tag{2}$$

where

$n(x, y)$ channel electron density/cm^3
$n_{\mathrm{i,eff}}$ effective intrinsic concentration of channel region per cm^3
N_a channel doping per cm^3
$\psi(x, y)$ channel potential at any point (x, y), V
$\varphi_{\mathrm{F,n}}(x)$ channel eQFP at x, V

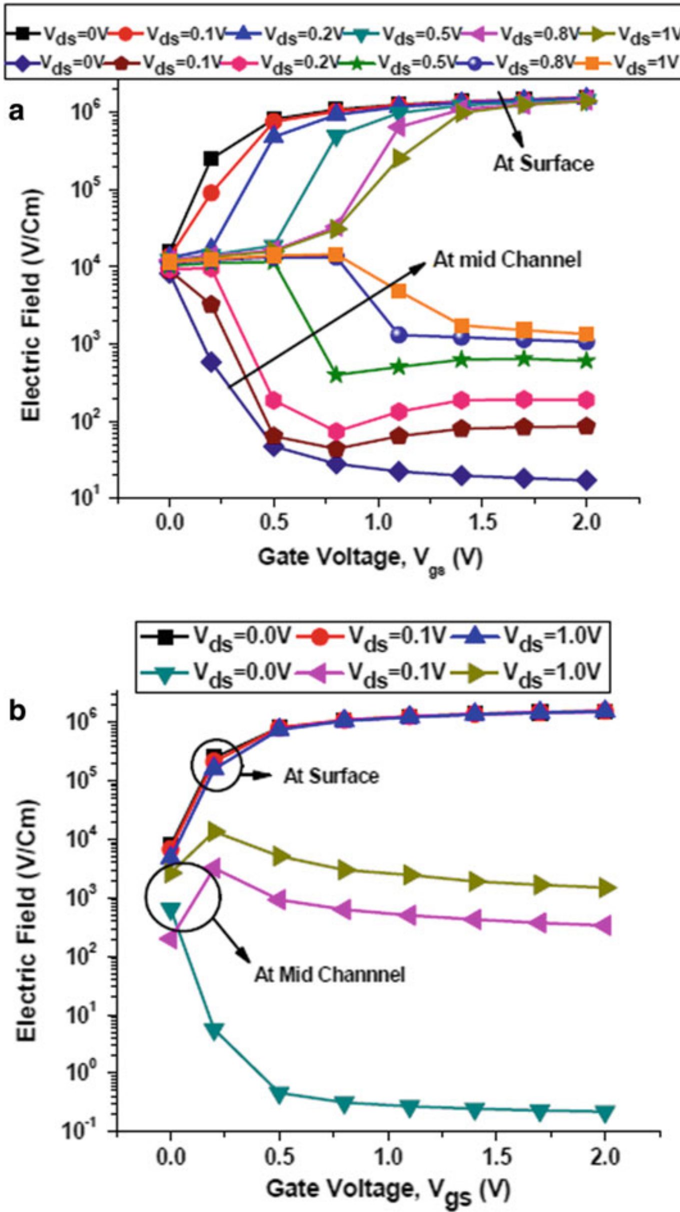

Fig. 7 Electric field at surface and the mid-channel point for DG TFET and DG MOSFET. **a** Electric field at surface and the mid-channel point for DG TFET. **b** Electric field at surface and the mid-channel point for DG MOSFET

V_T thermal voltage, V

It is clear from Fig. 8, DG MOSFET's electron densities are almost independent on applied drain voltage but DG TFET electron densities are strong function of drain voltages. This is because of higher quasi-fermi potentials seen in DG TFETs. As

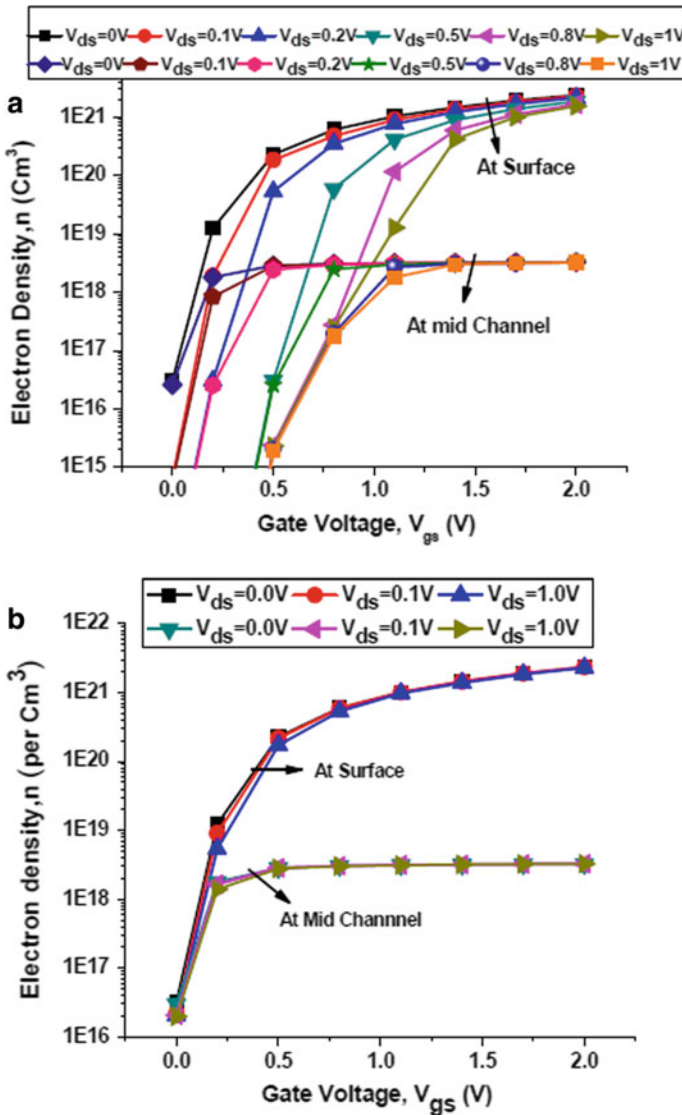

Fig. 8 Electron density at surface and the mid-channel point for DG TFET and DG MOSFET. **a** Electron density at surface and the mid-channel point for DG TFET. **b** Electron density at surface and the mid-channel point for DG MOSFET

shown in Sects. 3.2 and 3.3, an increase in drain voltage increases channel potentials and eQFP. But, we see, increase in channel potentials is lesser as compared to eQFP, hence from Eq. (2), electron density of DG TFET decreases with increasing drain voltages. As the applied gate voltage is increased, more electrons will be generated (due to BTBT) at the tunneling junction and will be attracted by vertical electric fields near the surface hence electron density will always increase with gate voltage, but mid-channel electron density will always be lesser than surface density.

4 Conclusion

Comparative study based on TCAD simulations for DG TFET and DG MOSFET devices with 50 nm gate length is carried out in this paper. It is found that although the channel (transverse) potential shape is parabolic in nature, its quality and quantity are different for both devices. In DG TFET, we found that the surface as well as mid-channel potential decreases after a particular gate voltage, which is different for different drain voltages. Unlike DG MOSFET, the mid-channel potential is not pinned to a fixed value after threshold voltage, but it decreases with increasing Vgs. Unlike DG MOSFET, a nonzero e—quasi-fermi potential is seen for DG TFET, which increases with applied drain voltage, but decreases at higher gate voltages. Gate threshold voltage for tunnel FETs is very high as compared to DG MOSFET and it is not depending on the on-set inversion charge theory. DG TFETs have very high I ON/I OFF, ratios, and steeper subthreshold swing. Electron density and electric field properties are also different for both the devices.

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