

# Resistive Random Access Memory Device Physics and Array Architectures



Victor Yiqian Zhuo, Zhixian Chen, and King Jien Chui

**Abstract** Resistive random-access memories (RRAM) has garnered much interest in recent decades as a strong candidate to replace conventional memories like NAND flash, SRAM and DRAM. In contrast to the electrical charge changes in flash memories to define memory states, RRAM devices rely on non-volatile, reversible resistance changes within the device, hence its name. Apart from its superior performance: low power, high speed, high endurance, its simple two-terminal metal-insulator-metal (MIM) structure allows for a more scalable design and simpler fabrication processes. However, the RRAM is not without its problems and challenges. The resistive switching property of RRAM is inherently stochastic, resulting in variations between memory states, which could result in bit errors if unaccounted for. Also, the two-terminal RRAM requires a select device to prevent wrong selection of devices in an array. This chapter focuses on the redox-RRAM, where resistance changes take place through redox reactions within the insulator layer of the MIM, and will describe the basic operating principles of RRAM as well as various RRAM architectures.

## 1 Broad Perspective on Nonvolatile Memory

Nonvolatile memory has become an indispensable part of our everyday lives, powering a wide gamut of applications, from massive data storage such as memory cards and solid state drives, to consumer electronics like mobile phones, digital cameras, and music players. Since its invention by Fujio Masuoka [1] and its commercialization by Intel Corporation in 1988 [2], flash memory is the most prominent nonvolatile memory technology that drives the proliferation of consumer electronics of increasing functionality and storage density. In less than three decades, flash memory has grown into a US\$20 Billion per year giant in the semiconductor industry

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V. Y. Zhuo (✉) · Z. Chen · K. J. Chui

Institute of Microelectronics (IME), Agency for Science, Technology and Research (A\*STAR), Singapore, Singapore

e-mail: [victor-zhuo@ime.a-star.edu.sg](mailto:victor-zhuo@ime.a-star.edu.sg)

[3]. Despite its dominance, the long-term scalability of flash memory is very uncertain due to inherent physical limits and device reliability [4].

Consequently, there is a need for a new nonvolatile memory that can keep up with the scalability and performance presented by future technology nodes. Many alternative memory technologies have emerged and are extensively studied and developed. Amongst them, the resistive random-access memory (RRAM), which retains information in the form of distinct resistance states [5], is widely regarded as the most promising for massive data storage.

Historically, the resistive switching phenomenon dates back more than two centuries and was first demonstrated on the electric arc by Sir Humphry Davy in 1802 [6]. In the 1960s, advances in thin film technology enabled very high electric fields in tri-layered structures which led to observable resistive switching behaviour in ultrathin metal/oxide/metal films [7, 8]. However, research efforts in these devices diminished after a decade of intensive study [8] due to the development of silicon integrated circuits. In 1971, Leon Chua hypothesized the existence of memristors, the fourth basic circuit element [9]. The recent intense surge of RRAM research activities was renewed in the late 1990s by Asamitsu et al. [10], Beck et al. [11], and Kozicki et al. [12] due to the declining progress of silicon technology. Then in 2008, Hewlett Packard Labs realized and termed analog switching RRAM devices as memristors [13], thereby validating the fourth basic circuit element hypothesized by Leon Chua.

In 2013, Panasonic produced the first commercialized embedded RRAM chip [14]. Subsequently, Toshiba and Sandisk announced a 32 Gb high-density RRAM chip [15]. In 2017, Taiwan Semiconductor Manufacturing Company (TSMC) announced the production of embedded RRAM chips in 2019 with their 22 nm technology process [16]. In addition, to achieve ultrahigh storage density, the two-terminal RRAM devices are implemented in a crosspoint array structure. In 2007, Samsung demonstrated the first three-dimensional (3D) RRAM crosspoint array [17]. Notably, a 3D XPoint memory technology was released in 2015 by Intel Corporation and Micron Technology Inc. Likewise, Crossbar Inc. also released 3D RRAM products with high scalability beyond the 10 nm node, as well as better read latency, energy efficiency and write performance than the current NAND flash memory products.

Other than data storage, RRAM technology can also be used in the development of human brain-like computing systems with very high energy efficiency, computing capability and density scalability. For instance, matrix-vector multiplication or dot product can be realized with RRAM crosspoint architecture [18, 19]. Functional neuromorphic chips using binary or analog RRAM devices has been successfully demonstrated [20–23] for online training.

Despite the advancements in RRAM technology, there is still insufficient breakthrough in the complete understanding of the RRAM physical switching mechanism [24–26]. The main area of contention on RRAM mechanisms revolves around its conductive filament (CF), especially on its composition and on how it connects and ruptures.

In this chapter, we will first review the proposed RRAM mechanisms, followed by the resistive switching materials. Thereafter, the RRAM crosspoint array architecture

will be discussed with respect to the selector device and the self-rectifying RRAM implementations. It will then end with a conclusion and future outlook.

## 2 RRAM Device and Operation

A typical RRAM device has a simple metal-insulator-metal (MIM) structure, whereby the sandwiched insulator is the active layer that stores the data. In general, a RRAM device is able to show two distinct resistance levels, namely the high resistance state (HRS) and the low resistance state (LRS), which represent the logic ‘0’ and logic ‘1’, respectively. More than two resistance levels can also be obtained via careful tuning of the programming voltage pulse width and amplitude, which leads to high data storage density.

The two basic RRAM operations are programming and erasing. The transition from HRS to LRS is known as the SET or programming operation. Conversely, the RESET or erasing operation denotes the transition from LRS to HRS. Usually, a pristine RRAM device will have an initial high resistance which requires an applied voltage that is higher than the SET voltage to activate the resistive switching capability. This event is called the electroforming or forming process.

The RRAM switching mode can either be unipolar or bipolar as illustrated in Fig. 1. For unipolar operation, the resistive switching is independent of the voltage polarity and only depends on the magnitude of the voltage and its duration. Nonpolar switching is used to describe a unipolar switching that occurs in both voltage polarities. Conversely, for bipolar operation, the voltage polarity is important as the SET and RESET operations occur in opposite voltage polarities. The switching mode usually depends on the device structure, especially in the asymmetry obtained via fabrication or electrical methods.

There are many ways to classify RRAM devices based on their active material, switching mechanism or the switching phenomena. Here, we will focus on the redox-RRAM and its two subcategories, anion and cation devices, to simplify the discussion on their mechanisms.

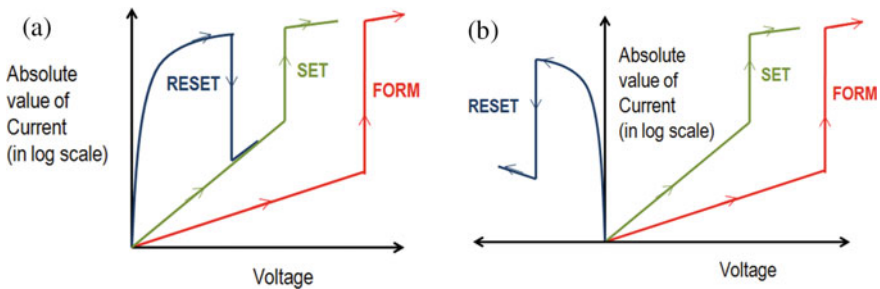


Fig. 1 Schematic of RRAM I-V curves showing two modes of operation a unipolar, and b bipolar

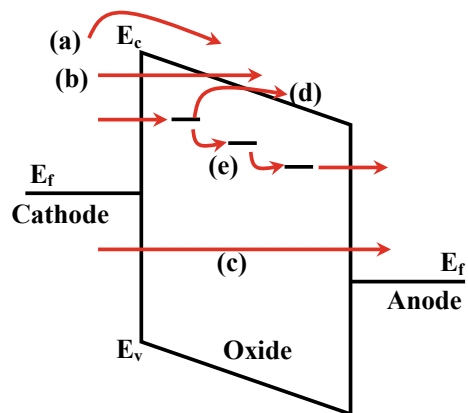
## 2.1 RRAM Conduction Mechanisms

In 2006, Szot et al. observed the CF inside insulating oxide using electron microscopy and proposed that the resistive switching was due to the reversible formation and rupture of the CF [27]. Ever since, the CF mechanism has been widely acknowledged. On the other hand, the non-filamentary switching phenomenon, also known as the interfacial switching mode, triggered by Schottky barrier changes at the dielectric-electrode interface, was also reported [5, 28, 29]. However, Schottky barrier changes are not exclusive to interfacial oxides and are also reported for filamentary switching oxides [5, 30–32]. The main difference between filamentary and interfacial switching modes is the dependence of the resistance to the device size, whereby for the former, the resistance is independent.

The CF within the dielectric is the localized conduction channel that is usually tens or hundreds of nanometers in diameter [33]. When the CF is formed between the electrodes, the RRAM device exhibits LRS. Conversely when the CF is ruptured, the device exhibits HRS. For cation RRAM devices, the resistive mechanisms are clear due to the ease at which the metal cations can be observed using microscopy techniques and thus verify the kinetic processes of the CF [34, 35]. As for anion RRAM, conduction depends on conductive channels created by oxygen vacancies, which is difficult to detect and to accurately fit with conventional current models. Though many attempts have been made to explain the conduction mechanism with Schottky emission, Poole-Frenkel emission, trap-assisted tunneling and other models, there is no single model that can accurately describe the conduction mechanism [31, 36].

In fact, there are many potential conduction mechanisms in RRAM as illustrated in Fig. 2. These conduction mechanisms can be grouped into two categories: (1) electrode-limited processes which consists of Schottky emission, Fowler-Nordheim tunneling, and direct tunneling as well as (2) bulk-limited processes, such as Poole-Frenkel emission, ohmic conduction, space-charge-limited conduction, hopping and trap assisted tunneling. For electrode-limited conduction mechanisms, the key factor

**Fig. 2** Band diagram illustration of the possible conduction mechanisms in RRAM: electrode-limited processes which consists of **a** Schottky emission, **b** Fowler-Nordheim tunneling, and **c** direct tunneling, as well as bulk-limited processes, such as **d** Poole-Frenkel emission, and **e** trap-to-trap hopping



is the barrier height at the electrode-oxide interface whereas for bulk-limited conduction mechanisms, the electrical properties of the oxide play a critical role. Typically, RRAM devices exhibit ohmic or hopping conduction at the LRS [31]. However, during HRS, the dominant conduction mechanisms vary even for similar MIM stacks [37, 38] or could depend on the applied voltage regime [31].

## 2.2 Anion Devices

### Switching Mechanisms

The active switching materials of anion RRAM devices include oxide dielectrics such as transition metal oxides, complex metal oxides, large bandgap dielectrics, as well as non-oxide dielectrics like chalcogenides and nitrides. In most metal oxides, the mobile species are widely believed to be the oxygen anions which is equivalent to the positively-charged oxygen vacancies. Hence, these RRAM devices are known as oxygen vacancy based RRAM (OxRRAM). Additionally, the anion migration leads to valence changes of the metal cations which leads to resistance change of the metal oxide and thus these devices are also termed as valence change memories (VCM) [5]. Since the resistance switching is caused by defects that modify electronic transport that is not limited to a specific electronic structure, almost all insulating oxides should show resistance switching behavior. In theory, the resistive switching phenomenon should also be observable in other insulating compounds like halides, borides, carbides and phosphides.

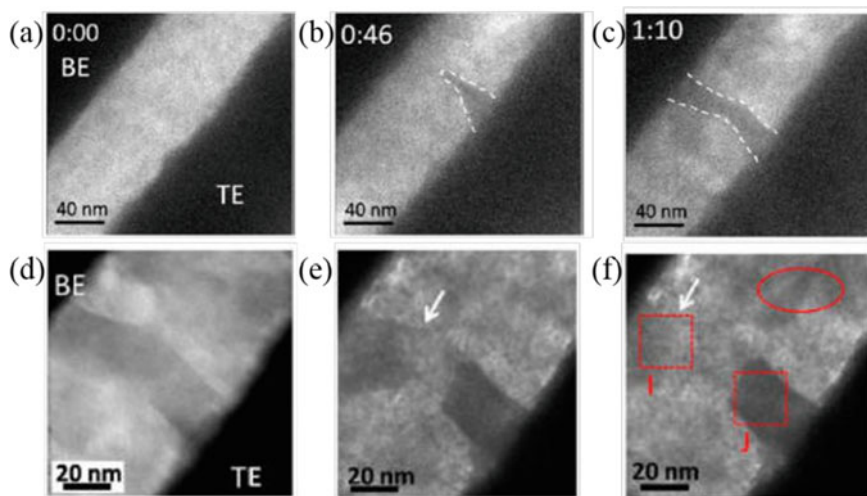
Since the earliest report of resistance switching in oxides by Hickmott in 1962 [7], oxides have been widely studied as anion-based switching materials, ranging from simple binary transition metal oxides, e.g.  $\text{TiO}_x$  [13, 32, 39],  $\text{TaO}_x$  [30, 40, 41],  $\text{HfO}_x$  [42–45],  $\text{ZrO}_x$  [46, 47], to rare-earth metal oxides, e.g.  $\text{CeO}_x$  [48],  $\text{EuO}_x$  [49], to perovskite-type complex oxides such as  $\text{SrTiO}_3$  and others [50–52]. In the even larger set of non-oxide switching materials, the resistive switching phenomenon has been shown in nitrides, e.g.  $\text{AlN}$  [53], selenides, e.g.  $\text{ZnSe}$  [54], tellurides, e.g.  $\text{ZnTe}$  [55], and polymers [56, 57].

Insulating oxides can be regarded as semiconductors with native dopants. They can be either n-type or p-type semiconductors if they are oxygen deficient or excessive, respectively. Under applied high electric field and/or Joule heating, the electrically and/or thermally driven motion of these native dopants leads to chemical changes which results in resistance change. As the mobility and concentration of oxygen vacancies or cation interstitials are adequately high in transition metal oxides [5, 58], they are widely acknowledged as the mobile species responsible for the resistance switching and this is supported by experimental evidence [27, 33, 59–61]. However, more direct evidence is needed to confirm the actual mobile species even though it is very difficult to detect and track the migration of oxygen vacancies in RRAM devices [62–68].

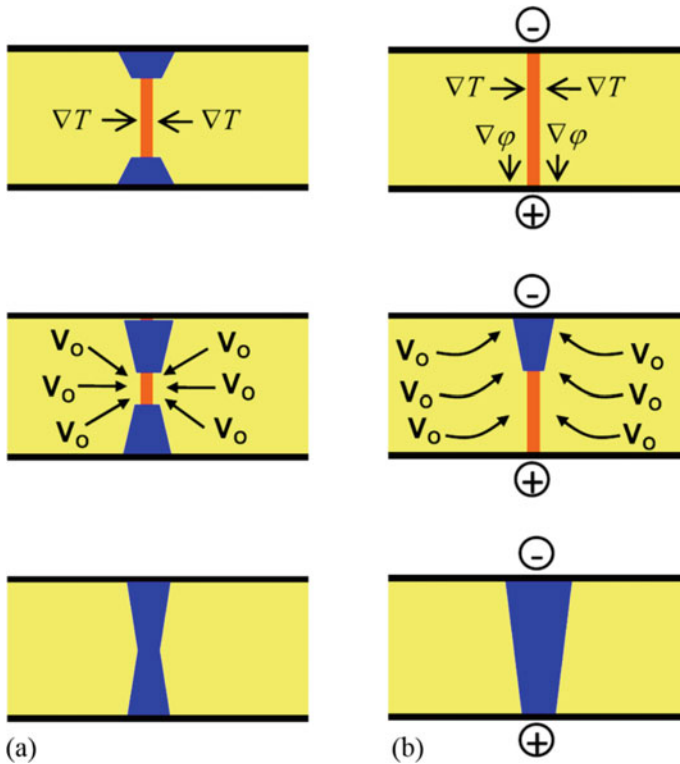
The CF in OxRRAM is usually created by an electroforming process where the pristine device is subjected to a higher than normal voltage or current to activate the resistive switching capability [69–71]. Once activated, OxRRAM typically show either unipolar or bipolar resistive switching and have different switching dynamics and dominant driving forces.

In order to clarify the switching dynamics on their unipolar Pt/ZnO/Pt RRAM device, Chen et al. traced the CF evolution using in situ transmission electron microscopy (TEM) [72]. As depicted in Fig. 3a–c, during the electroforming process via applied voltage sweep, a darker contrast near the top electrode (TE) indicated the growth of the CF which eventually formed into a complete CF with the thinnest area in the middle. During the RESET process shown in Fig. 3d–f, the CF ruptured in the middle due to Joule heating, which ended in the dissolution of the CF towards the bottom electrode (BE). This in situ observation of CF formation confirms the important role of thermal effects in the CF rupture process, which suggests that the resistive switching in unipolar OxRRAM systems is mainly dominated by thermochemical effects.

Other plausible mechanisms in unipolar OxRRAM systems such as thermophoresis and diffusion were also explored by Strukov et al. [73], where they proposed a resistive switching model based on radial Soret-Fick diffusion equations. This model was experimentally verified with pulse length dependent tests to observe the response of switching dynamics in OxRRAM systems to the temperature gradient induced by Joule heating. As illustrated in Fig. 4a, in the case of neutral oxygen vacancies, a symmetrical CF is formed similar to that in Fig. 3b. However, for positively charged oxygen vacancies, an asymmetric CF is formed due to drift



**Fig. 3** In situ TEM of a–c electroforming process and d–f RESET process taken from video in Pt/ZnO/Pt system. Reprinted (adapted) with permission from [72]. Copyright (2013) American Chemical Society



**Fig. 4** Side view schematics of unipolar SET switching in RRAM device with **a** neutral oxygen vacancies and **b** positively charged oxygen vacancies. Reprinted by permission from Springer Nature, Applied Physics A: Materials Science & Processing [73], Copyright (2012)

(Fig. 4b) and this is observed in TiO<sub>2</sub> OxRRAM by Kwon et al. [59] using in situ TEM. The electroforming process creates a radial temperature gradient due to Joule heating within the CF. The Soret force then attracts the vacancies towards the CF and since the vacancies are positively charged, they are attracted towards the negative electrode.

By considering both **thermophoresis** and the Fick diffusion of oxygen ions under the influence of Joule heating, the ion dynamics in OxRRAM can be described by the following Soret-Fick continuity Eq. (1) [73, 74]:

$$\frac{\partial \eta_v}{\partial t} = \nabla J_{Fick} + \nabla J_{Soret} \tag{1}$$

where  $\eta_v$  is the vacancy density,  $J_{Fick}$  and  $J_{Soret}$  are the fluxes induced by Fick diffusion and thermophoresis, respectively.

Unlike unipolar OxRRAM systems, it is the electric field effects that dominate in bipolar OxRRAM systems. One of more widely researched bipolar OxRRAM

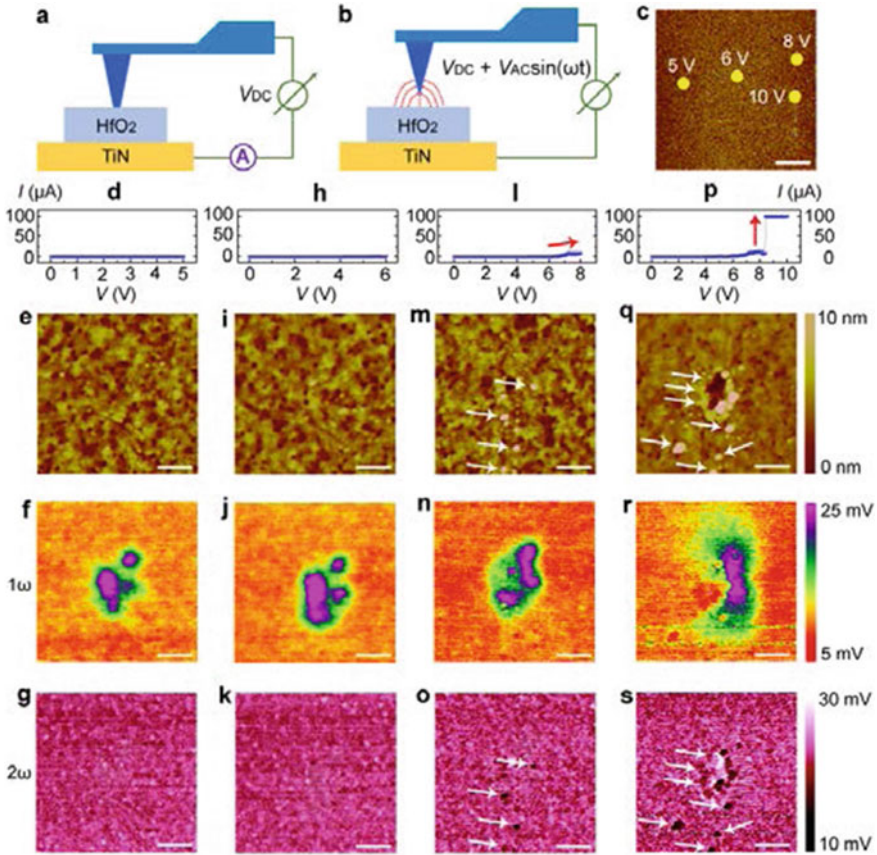
materials is  $\text{TiO}_2$ . Kwon et al. reported in situ studies on  $\text{TiO}_2$  RRAM devices where the CF was made of a conductive Ti-O phase, termed Magnéli phase, with a  $\text{Ti}_n\text{O}_{2n-1}$  stoichiometry [59]. Similar oxygen-deficient CF with Magnéli phase was reported in  $\text{WO}_3$  based RRAM systems by Tan et al. [75]. However, these observations rarely yielded any valid switching dynamics in bipolar OxRRAM systems that do not have stable intermediate phases such as  $\text{HfO}_2$  and  $\text{Ta}_2\text{O}_5$ . This could be due to sample surface contaminants and the reliance of TEM observations on just the ion mass attribute. To circumvent this, a new technique was developed by Yang et al. in 2017 to characterize the ion transport and CF growth dynamics in bipolar  $\text{TaO}_x$  and  $\text{HfO}_x$  based OxRRAM using electrostatic force microscopy (EFM) [76]. Specifically, EFM is sensitive to the ion charge accumulation, has sub-10 nm spatial resolution with no strict requirements on sample thickness nor vacuum level [77, 78]. By merging EFM with systematic atomic force (AFM) and conductive atomic force microscopy (C-AFM) characterizations [79], this approach is able to provide a clearer representation of the dynamic oxygen ion transport during the resistive switching of OxRRAM. As depicted in Fig. 5, this approach is able to detect the migration and accumulation of oxygen ions to the interface and the following redox reactions as well as oxygen gas formation, which led to oxygen-deficient CF and structural distortions in the memory film. The formation of these CF in  $\text{HfO}_2$  was directly identified using spherical-aberration ( $C_s$ )-corrected TEM and reversible ion migration was proposed to be responsible for the bipolar switching in  $\text{HfO}_2$  [76].

Although bipolar switching in OxRRAM tends to be due to ionic motion and electrochemical reactions caused by electric field effects, thermal effects still play a crucial role during the RESET process [80, 81]. Panda et al. combined two models, an analytical temperature model [82] and a filament dissolution model [83, 84] and found that the temperature varies in a parabolic path within the CF, and is highest at the middle of the CF and lowest at the electrodes [85], which is in agreement with hypothesis that Joule heating assists the RESET mechanism in OxRRAM devices.

### Material Selection Considerations

Since Joule heating is inevitable in the OxRRAM, it has a major influence on the material selection. In order for the OxRRAM to have stable and reliable resistive switching, both insulating and conductive phases are necessary. These two phases should not chemically react with each other to form a new phase, even at elevated temperatures caused by Joule heating. It should be a simple system with only two thermodynamically stable solid-state phases, one insulating phase and one relatively conductive phase for the conduction channel. Ideally, the conduction channel should have a high oxygen solubility to serve as a reliable oxygen reservoir to conserve the oxygen ions during repeated switching cycles [26].  $\text{TaO}_x$  and  $\text{HfO}_x$  are the prime candidates that fulfil these requirements, exhibiting switching endurance over  $10^{12}$  [86] and  $10^{10}$  cycles [87], respectively.





**Fig. 5** Schematics of the **a** conductive atomic force microscopy (C-AFM) and **b** electrostatic force microscopy (EFM) measurements performed on HfO<sub>2</sub>/TiN samples. **c** Topographic image showing locations where voltage sweeps with different amplitudes were performed. Electrical **d**, topographical **e**,  $1\omega$  (**f**), and  $2\omega$  **g** measurements on the region stimulated by voltage sweep up to 5 V during preceding C-AFM measurements. **h–k**, **l–o**, and **p–s** are the corresponding electrical and EFM results on the region stimulated by voltage sweep up to 6 V, 8 V, and 10 V during C-AFM measurements. Reprinted from [76] under a Creative Commons Attribution 4.0 International License. Full license terms at <http://creativecommons.org/licenses/by/4.0/>

### 2.3 Cation Devices

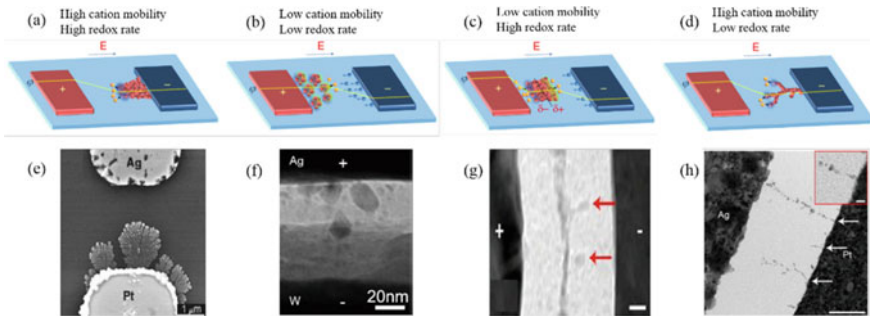
#### Switching Mechanisms

Cation-based RRAM devices are also known as metal ion based RRAM, electrochemical metallization memory, atomic switch or conductive bridge RRAM (CBRAM). First reported in the 1970s by Hirose et al. [88], and developed by Kozicki et al., in the late 1990s for data storage [89], the mobile species in CBRAM devices are metallic cations. Typically, the CBRAM MIM stack consists of a solid electrolyte

(SE) sandwiched between an electrochemically active electrode (AE) and an electrochemically inert electrode (CE). Candidates for the AE are limited to some metals that are mobile in the SE, and are usually Cu [90], Ag [91] or an alloy such as CuTe [35]. CE materials are less limited and include Pt, Ru, Ir, Au, W, Mo, Co, Cr, TiW, TaN or poly-Si [34]. Conventionally, the SE materials have been amorphous Si, C, doped organic semiconductors, iodides, methylsilsesquioxane, selenides, sulphides, tellurides, ternary chalcogenides, or even non-solid electrolytes like water and even vacuum gaps [92–95]. Recently, more and more metal oxides and nitrides have been used, including  $\text{Al}_2\text{O}_3$ ,  $\text{CuO}_x$ ,  $\text{HfO}_2$ ,  $\text{GdO}_2$ ,  $\text{MoO}_x$ ,  $\text{SiO}_2$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{TiO}_2$ ,  $\text{WO}_3$ ,  $\text{ZnO}$ ,  $\text{ZrO}_2$ , and  $\text{AlN}$  [96–98]. The transition from traditional electrolytes to the complementary metal-oxide-semiconductor (CMOS) compatible and inexpensive oxides have enhanced the retention and operation voltages of CBRAM, making them more suitable for certain applications such as switches in large-scale integrated circuits [96]. More details on the material systems available for CBRAM can be obtained from the comprehensive review by Valov et al. [34].

Switching mechanisms in CBRAM are similar to that in OxRRAM. Electroforming in CBRAM also causes structural alterations to the SE and creates nanoscale CFs to accommodate the electrochemically active metal ions for the subsequent resistive switching [35]. Most CBRAM devices exhibit bipolar switching where by the electric field is the dominant driving force. However, there are also reports of unipolar CBRAM, which suggests the possibility of Joule heating effects [99, 100]. Unlike OxRRAM, the switching mechanisms are better understood since the metal ions are more easily observed using microscopy techniques, thus the kinetic processes of the CF can be more easily verified [101]. Since ion migration and associated redox processes during resistive switching occur at the nanoscale, the TEM, specifically the in situ TEM, is currently one of the best techniques used to understand the dynamic processes of resistive switching as it can yield details on the chemical state, composition, morphology, size and trace the evolution of the CF growth/dissolution down to individual metal nanoclusters. As summarized by Yang et al. [102], there are mainly four different electrochemical metallization processes in CBRAM devices depending on the cation mobility and the redox reaction rate as shown in Fig. 6. The cation mobility influences the nucleation site of the CF and the direction of the CF growth whereas the redox reaction rate determines the ion supply which decides the CF morphology [102].

As schematically shown in Fig. 6a, when cation mobility and redox reaction rate are high in the SE, it leads to inverted cone-shaped CFs that initiate from the inert CF. This has been directly verified using in situ TEM for Ag/ $\text{H}_2\text{O}$ /Pt (see Fig. 6e) [101], Cu/ $\text{Al}_2\text{O}_3$ /Pt [103] and Cu/Cu-GeTe/Pt–Ir [104] devices. On the other hand, when both cation mobility and redox reaction rate are low, the cations traverse a short distance from the AE to attain critical nucleation conditions within the dielectric which leads to metal cluster formation. These metal clusters then form a CF that grows from the AE to the CE as shown schematically in Fig. 6b and has been reported in Ag/ $\text{SiO}_2$ /W (see Fig. 6f) [105], Ag/ $\text{ZrO}_2$ /Pt [106], Ag/a-Si/Pt [107], and TiN/ $\text{Al}_2\text{O}_3$ /Cu [108].



**Fig. 6** a–d Schematic diagrams of filament growth and e–h TEM images of corresponding exemplary filament for when a, e both cation mobility and redox reaction rate are high b, f both cation mobility and redox rate are low c, g low cation mobility and high redox reaction rate, and d, h high cation mobility and low redox reaction rate. Adapted by permission from Springer Nature Journal of Electroceramics [102], Copyright (2017)

If the SE layer facilitates low cation mobility and high redox reaction rate as shown in Fig. 6c, nucleation of the CFs occurs inside the SE analogous to the case when both cation mobility and redox reaction rate are low. The exception lies in the high reaction rate which causes persistent reduction of the metal cations at the sites of nucleation, resulting in the backward CF growth from the nucleation site to the AE. This has been observed using in situ TEM by Yang et al. for Ni CF growth in evaporated  $\text{SiO}_2$  thin films, as depicted in Fig. 6g [109]. For the last case shown in Fig. 6d where the cation mobility is high and redox reaction rate is low, CF nucleation occurs from the CE. The low redox reaction rate limits the ion supply such that ion reduction occurs at the edges of existing CFs, resulting in the formation of dendrite-like CFs towards the AE. This can be clearly observed in lateral  $\text{Ag/SiO}_2/\text{Pt}$  (see Fig. 6h) [107] and  $\text{Ag/Ag-PEO/Pt}$  devices [110].

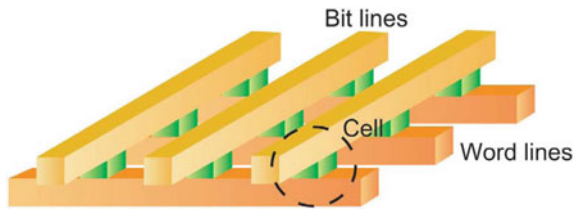
In general, the formation and dissolution of nanoscale CFs has been widely accepted as the resistive switching mechanism for CBRAM devices. However, other mechanisms such as phase transitions has also been reported for specific material systems. One such example is the  $\text{Ag/Ag}_2\text{S/W}$  device that was reported by Xu et al. using in situ TEM where the resistive switching was induced by a phase transition in the  $\text{Ag}_2\text{S}$  between the conductive argentite phase and the insulating acanthite phase [111]. Unlike conventional CBRAM devices, these  $\text{Ag/Ag}_2\text{S/W}$  devices have an abundance of Ag cations which allows intrinsic resistive switching in the SE without the need of cation injection from the electrodes.

Although there has been much progress in the understanding of the resistive switching mechanisms in both CBRAM and OxRRAM, more research is still needed to confirm the microscopic details, especially for the OxRRAM devices. Linking the structural changes in the memory layer to the device variation, degradation and performance would be significant and will pave the way to increased RRAM commercialization.

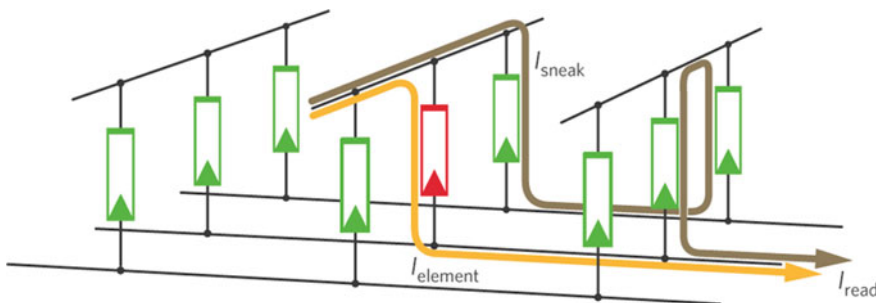
### 3 RRAM Crosspoint Array

RRAM's simple MIM structure allows the implementation of the highly dense crosspoint memory array. As illustrated in Fig. 7, a crosspoint array has parallel metal lines, known as word and bit lines, at the top and bottom planes, perpendicular to one another. At each crosspoint or intersection of these metal lines, a two terminal memory device is integrated. The word and bit lines are used to select a memory cell and write/read data, respectively [29]. Assuming that the width of both metal lines and spaces is equal to  $F$ , where  $F$  is the minimum technology feature size, the effective cell area will be  $4F^2$ , which is the smallest single layer or two-dimensional (2D) footprint [112].

However, it is not easy to directly use this passive resistive network since accessing a designated cell induces sneak path currents from adjacent memory cells. As depicted in Fig. 8, the sneak path problem occurs when the selected memory cell is at HRS (red) and all its adjacent cells are in LRS (green). During the read operation, the current flow through the selected memory cell should be low ( $I_{\text{element}}$ ). However, as the adjacent cells are all in LRS, significant sneak currents ( $I_{\text{sneak}}$ ) will flow through all the cells, thus contaminating the actual information of the target cell. Moreover, the leakage currents will also increase the power consumption. These problems worsen



**Fig. 7** Schematic diagram of a crosspoint memory array showing the word and bit lines. Reprinted from [29], Copyright (2008), with permission from Elsevier

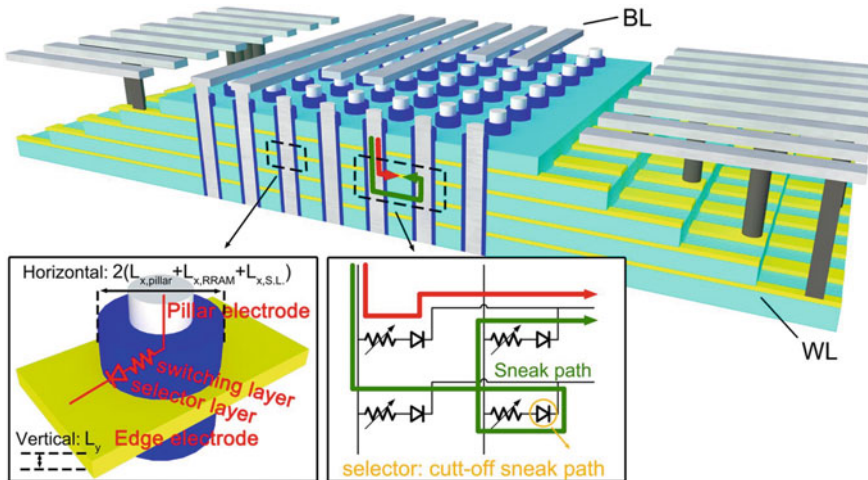


**Fig. 8** Illustration of the sneak path issue in a crosspoint memory array. Reprinted by permission from Springer Nature Materials [112], Copyright (2010)

with increasing array size due to more current leakage paths, causing memory performance degradation. To suppress this sneak path problem, a prevalent solution at the device level is to incorporate a selection device with each RRAM device such as a transistor or a nonlinear selector, to get a 1T1R or 1S1R configuration, respectively.

Another key requirement for crosspoint memory arrays is high scalability such that the storage capacity can meet the specifications driven by the growth of internet data, data centers and mobile computers. A seemingly straightforward solution is to decrease the individual cell size such as reducing the RRAM device diameter. However, this raises concerns regarding increased spatial and temporal variability in the RRAM devices contained in the crosspoint array. Also, the interconnect and peripheral circuit area should decrease with downscaling which will increase series resistance due to geometry scaling and increased surface scattering [113], resulting in operational problems at high operating currents. Several methods have been reported to reduce interconnect resistance such as using graphene and carbon nanotubes as interconnect materials [114].

In order to circumvent the problems in downscaling, unique three-dimensional (3D) array architectures have been proposed such as the horizontal stacked 3D and vertical 3D structures. By stacking multiple 2D layers of memory crosspoint (Fig. 7) into a 3D structure, the minimal feature size is further reduced to  $4F^2/n$ , where  $n$  is the number of stacked layers. Between these two 3D structures, the vertical configuration has higher processing yield and cost effectiveness since only one critical lithography etch step is needed after the sequential deposition of multiple stacks. As depicted in Fig. 9, the memory cells in a vertical 3D crosspoint architecture, are formed at the sidewalls between the horizontal electrode and the vertical pillar electrode [115].



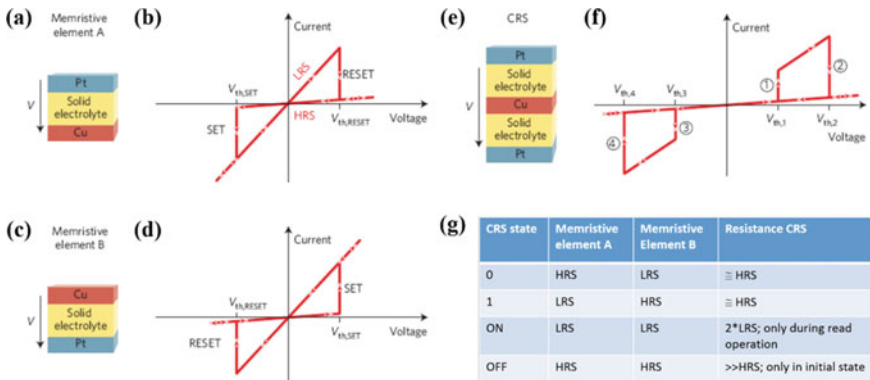
**Fig. 9** Vertical 3D RRAM crosspoint architecture. Reprinted from [115] under a Creative Commons Attribution 4.0 International License. Full license terms at <http://creativecommons.org/licenses/by/4.0/>

Instead of reducing the cell size, high density in a 3D array is achieved by increasing the number of stacked layers.

### 3.1 RRAM Design Without Selector Device

The key advantages of a crosspoint array with no selector devices are the simple fabrication process and high array density. However, it will require the RRAM device to be self-rectifying in order to overcome the sneak path current problem.

One of the several self-rectifying concepts is the complementary resistive switching (CRS) devices first reported by Linn et al. in [112]. As shown in Fig. 10e, the CRS device is made up of two bipolar Cu/SE/Pt devices connected back to back with a shared Cu electrode in the middle. LRS occurs when a Cu filament is created across the SE by a positive voltage applied to the Cu electrode whereas a negative voltage will induce HRS via dissolution of the Cu filament. This CRS device is able to derive a unique I-V characteristic and four CRS states as shown in Fig. 10e–g. At both logic states (0 and 1), the leakage current is suppressed since one of the two Cu/SE/Pt cells within the CRS device is in HRS. A key disadvantage of this concept is that the read ‘1’ operation is destructive; thus a write back process is required to revert the LRS (top cell)/LRS (bottom cell) to the original LRS/HRS state via an applied negative pulse. This increases the complexity of the peripheral circuitry and the power consumption [116]. Hitherto, the CRS phenomenon has been reported for several CBRAM devices [112, 117] as well as OxRRAM devices [86, 118, 119], using the anti-serial, back to back configuration. However, several challenges still



**Fig. 10** **a** Bipolar memristive element A with a Pt/solid electrolyte/Cu stack. **b** I-V behavior of memristive element A shows that transition between HRS and LRS can be performed by exceeding  $V_{th,RESET}$  and  $V_{th,SET}$ . **c** Bipolar memristive element A with a Cu/solid electrolyte/Pt stack. **d** I-V behavior of memristive element B. **e** Combining memristive elements A and B creates a CRS. **f** I-V behavior of a CRS. **g** All possible states of a CRS. Adapted by permission from Springer Nature Nature Materials [1124], Copyright (2010)

remain for practical CRS implementation such as the shared inner metal electrode and the inherent variability of each CBRAM in a CRS cell. It is also difficult to reduce the operation current in the CRS since the variability increases with the current reduction [120–122].

Another self-rectifying concept is to have a hybrid RRAM-selector cell such as the 3D double layer vertical structure demonstrated by Hou et al. [123–125]. By utilizing a Ta/TaO<sub>x</sub>/TiO<sub>x</sub>/Ti MIIM stack, stable bipolar resistive switching with over 10<sup>3</sup> self-rectifying ratio as well as superior endurance over 10<sup>10</sup> cycles for both top and bottom MIIM cells. Homogeneous interfacial switching mechanism was proposed to elucidate the bipolar resistive switching mode and self-rectification [124]. The key merit of this structure is the absence of the additional inner middle electrode that separates the RRAM from the selector which makes it very attractive for the high density vertical 3D crosspoint architecture.

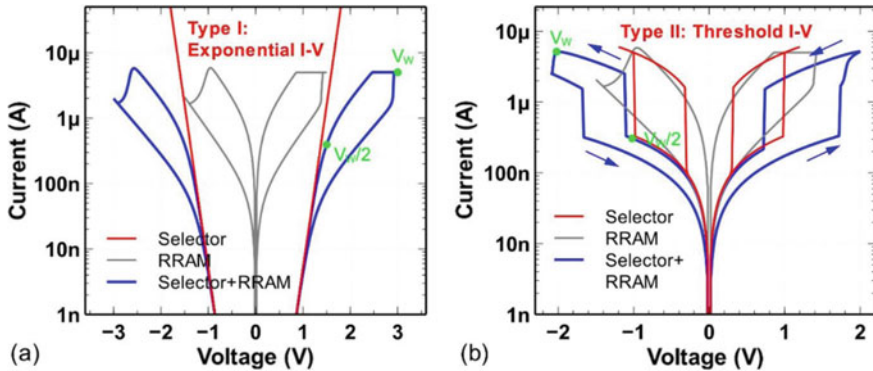
In 2017, Luo et al. demonstrated a bit cost scalable, 8-layer vertical 3D RRAM using a hybrid RRAM-selector cell [126]. With a TiN/HfO<sub>2</sub>/TaO<sub>x</sub>/Ti MIIM stack, the devices exhibited >100 non-linearity and high endurance (>10<sup>7</sup>). In addition, scalability down to 5 nm device size and 4 nm vertical pitch in a 3D RRAM array was also demonstrated [126]. Despite its high performance and scalability, the high LRS and HRS resistances in the GΩ range might require innovative circuit design.

### 3.2 RRAM Design with Selection Device

Since most RRAM devices operate in the bipolar switching mode, we will focus on two-terminal selection devices compatible with bipolar RRAM. Based on I-V characteristics, Yu et al. broadly categorized these selection devices into two groups: Type I (Exponential I-V selectors) and Type II (Threshold I-V selectors) [127]. Figure 11 shows the typical I-V characteristics of a bipolar RRAM device with Type I and Type II selectors. The two key selector performance metrics are (1) non-linearity, which is the current ratio between  $V_w$  and  $V_w/2$ , and (2) drive current density, which ideally has to be higher than 10 MA/cm<sup>2</sup> if the device scales below the 10 nm technology node. The selector non-linearity ensures limited sneak current from unselected memory devices during write and read operations. Other selector performance metrics such as speed, cycling endurance, variability should ideally be as good as or better than the memory cell that it is paired with. In addition, the selector material and fabrication process should also be CMOS compatible.

As seen in Fig. 11a, Type I selectors employ an exponential I-V curve to switch on the selector with a current increase of several orders of magnitude, resulting in high non-linearity. Reported Type I selectors usually involve engineering the oxide/electrode interface to form a Schottky barrier [128–130] or MIM structures with a tunnelling oxide barrier [131–134].

Ideally, Type II selectors are more preferred due to their sudden turn-on property with steep slope. Type II selectors usually show a hysteresis in their I-V characteristics as depicted in Fig. 11b, where they turn on above a threshold voltage and turns off



**Fig. 11** Typical I-V characteristics of a bipolar RRAM with **a** Type I Exponential I-V selector and **b** Type II Threshold I-V selector, respectively. Reprinted by permission from Springer Nature Journal of Computational Electronics [127], Copyright (2017)

below a hold voltage. Such threshold switching is exhibited in metal-insulator transition (MIT) Mott oxide materials such as  $\text{VO}_2$  [135–138] and  $\text{NbO}_2$  [139–141]. MIT is an electrically or thermoelectrically-triggered, rapid, reversible transition between a high resistive insulating oxide state and a low resistive metallic state. Son et al. have demonstrated fast switching speed ( $<20$  ns), large drive current density ( $>1$  MA/cm<sup>2</sup>) and a relatively small non-linearity ( $\sim 50$ ) in their  $\text{VO}_2$ -based MIT selector devices [135]. Interestingly, only the nano-scale devices exhibited MIT I-V characteristics while the micro-scale devices showed ohmic behaviour, as shown in the inset of Fig. 14. In addition to its small non-linearity, the transition temperature of  $\text{VO}_2$  is low at about 67 °C, which limits its practical applications since standard operating temperature is at 85 °C. Such limitations have led to new material considerations such as  $\text{NbO}_2$ , where higher non-linearity ( $\sim 10^4$ ) and higher drive current density ( $>30$  MA/cm<sup>2</sup>) has been demonstrated [139, 140]. This could be due to  $\text{NbO}_2$  having a larger insulating bandgap and higher transition temperature as compared to  $\text{VO}_2$  [142]. In addition, Park et al. developed a multi-layered  $\text{NiO}_y/\text{NbO}_x/\text{NiO}_y$  structure capable of suppressing the leakage current such that relatively higher non-linearity ( $>5400$ ), fast speed ( $<2$  ns) and drift-free performance is achieved [143].

Other than Mott materials, Type II threshold selectors based on chalcogenide materials have shown excellent selector performance. Several of these selectors are based on the ovonic threshold switching (OTS) phenomenon, which was first reported by Ovshinsky in 1968 [144]. OTS is an electronic transition between high and low resistance states via a region of negative differential resistance. Such OTS selection devices are different from chalcogenide-based memory devices, where the latter must be actively switched between states [144]. Most OTS selectors reported high non-linearity ( $>10^4$ ), which provides the full cell selectivity at read and write operations, and high on-state current ( $>30$  MA/cm<sup>2</sup>), which promotes scalability [145–147]. Several research groups have successfully demonstrated 1S1R integration using OTS selectors. In 2017, a joint project between IBM and Macronix demonstrated a 128 Gb



PCRAM crosspoint array using OTS selector that exhibited very low write (<300 ns) and read (<100 ns) latencies, good write high endurance (> $10^7$ ) and excellent thermal retention (> $10^4$  h at 85 °C) [148]. In terms of integration between OTS selector and RRAM, Lee et al. from Samsung reported in 2012, a 1S1R memory cell using a TaO<sub>x</sub>-based RRAM and a AsGeTeSiN-based OTS select device [149]. The nanoscale selector showed high selectivity ( $10^3$ ), endurance ( $10^8$ ) and on-state current density (>10MA/cm<sup>2</sup>).

Similarly, in 2017, Alayan et al. reported a 1S1R memory where HfO<sub>x</sub>-based RRAM was stacked with a GeSe OTS selector [150]. A stable and novel reading strategy was proposed and up to  $10^6$  read cycles have been achieved in their 1S1R memory cell.

In 2014, Jo et al. from Crossbar Inc. reported a Field Assisted Superlinear Threshold (FAST) Selector based on a superlinear threshold layer (SLT) whereby a conduction channel is created at the threshold electric field [151]. By themselves, these Type II threshold selectors exhibited excellent selector performance such as very high non-linearity (> $10^{10}$ ), large drive current density (>5 MA/cm<sup>2</sup>), high endurance (> $10^8$ ) and fast operation speeds (<50 ns). When the FAST selectors are integrated with low-current, forming-free RRAM cells in a 4 Mb 1S1R crosspoint array, the integrated 1S1R device demonstrated > $10^2$  memory on/off ratio and > $10^6$  non-linearity over  $10^5$  cycles [151].

Despite intense development of selector research in recent years, there is still no consensus on the best selector candidate as it must match the characteristics of the non-volatile memory device. Thus, the selector device still remains as a crucial challenge in the implementation of ultra-high density crosspoint memory architectures. Ultimately, a self-rectifying RRAM device would be ideal as it eliminates the requirement of an additional selector element.

## 4 Conclusions and Future Outlook

In the past decade, RRAM has seen much progress from single device up to 3D crosspoint array demonstrations. Nevertheless, challenges still persist such as detailed clarification of the resistive switching dynamics, the perfect matching of RRAM with selector or a reliable self-rectifying RRAM for true 3D vertical crosspoint implementation. Furthermore, new computing architectures are emerging, facilitated by the unique physical properties of RRAM and the perfect pairing between RRAM crosspoint arrays and the matrix-vector computation.

In the near future, RRAM technology is expected to have great potential in both data storage and computing. For instance, RRAM can be leveraged as a storage-class memory, which fills the gap between main memory and storage memory. In addition, the high-density, low-power and multi-level capabilities of RRAM has also motivated research into neuromorphic computing systems as a synaptic device, which would induce a paradigm shift in computing technology and a revolution in future electronic devices.

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