Design and Analysis of Low-Power SRAM

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Abstract The Static Random Access Memory (SRAM) is an integral part of memory architectures. With growing technology and scaling factor, static power consumption needs to be minimized. Therefore, an SRAM cell desires the new techniques and architecture, which can operate at very low sub-threshold voltage. In this paper, PN-based 10T SRAM cell (PPN10T) and transmission-based 8T (TG8T) have been analyzed and proposed a new 8T SRAM cell (P8T) to overwhelm the problems faced by conventional 6T SRAM (C6T) cell. The selection of W/L ratio and bit-line leakage problem has been significantly resolved for low-power SRAM design. Moreover, C6T, PPN10, TG8T cells and P10T has been compared for different performance parameters such as hold noise margin, read static noise margin (RSNM), write static noise margin (WSNM), read delay, write delay, $I_{\text{read}}/I_{\text{leak}}$ ratio, hold power dissipation and dynamic power dissipation.

Keywords SRAM · C6T · PPN10T · TG8T · P10T · Bit-line leakage · RSNM · WSNM

1 Introduction

Memory circuits are an integral part of any system design. In order to build a processor having the capability to process instructions at a very high rate, the processing unit requires significant SRAM cache memories. These cache memories take the primary part of a silicon area in the processor and consume more leakage power [1]. With

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the technology advances, static power consumption in CMOS devices required to be more attention, particularly for SRAMs because of leakage power is directly dependent on the amount of transistors present in the circuit. Previous study proofs that 70% of the total memory structure in a microprocessor-based designs are occupied by transistors, and it is going to be 80% in the future [2].

Hence, for stable and energy-efficient SRAM, low-power and minimum leakage component desired. The leakage currents flowing in the circuit are different so that from various places, power can be leaked [3]. Mainly Sub-threshold current, gate leakage current and junction leakage current are taken into consideration to calculate leakage power and the sub-threshold leakage current is the most relevant component among all [2, 4].

Numerous methods have been discussed earlier to minimize the power dissipation of an SRAM cell. In the drowsy mode method [5], one extra pMOS transistor can be connected between the voltage supply and the cell, therefore, cell will remained on the standby mode. Similarly, one nMOS transistor can be connected between the cell and the ground so that it can break the path connecting-cell to the ground. Subsequently, that sleep transistors will nearly eliminated the leakage power. In the voltage scaling method [6], static (leakage) power and supply voltage has a linear relation. Thus, leakage power can be reduced by operating the cells in standby mode at low supply voltage.

Consequently, when the cell is in the standby mode, it is connected to the smaller supply voltage compared to V_{DD}. The gated-V_{DD} (gated-GND) technique and dual-threshold voltage (dual-V_{t}) technique have been discussed in [5] to a decrease the leakage power. In these techniques, all the transistors of SRAM cells are at low-V_{t} transistors so that performance is maintained and the sleep transistors are used in either supply path or ground path with high-V_{t} transistors.

In addition to this, power dissipation during read and write operations in SRAM is a very essential due to leakage currents. In conventional SRAM, additional energy is lost during write operation as compared to the read operation. Because bit-line voltage swing during write operation is more and content stored in the cell can get tripped very easily during the read operation that leads to very low read stability [7]. Moreover, many design methods have been reported to improve the read and write-ability of the cell operating at low voltage supply. Sharifkhani and Sachdev [8] presented a technique in which, during the write operation, the write access transistors are controlled by a more abounded voltage supply. Schmitt trigger-based SRAM cell was proposed by Kulkarni et al. [9] that suggested to overcome the problem of read disturbance. PPN-based 10T SRAM cell (PPN10T) [10], transmission-based 8T (TG8T) has been recently reported [11], which describes the energy efficiency and variation tolerance of SRAM. Schmitt-trigger-based single-ended 11T SRAM cell was reported by Ahmad et al. [12]. In this case, two nMOS are connected in series in the cell of SRAM and transistors (read buffers) are connected; hence, it takes low power and gives good write and read static noise margin (SNM).

On the other hand in order to deal with disturbance problems through the read operation, Chang et al. [13] has been proposed novel circuit which contains two word lines and two access transistors. One of the word-line was used during read operation,

and the other was used in the write operation. This cell has a good read static noise margin. In addition, leakage and disturbance problems have been discussed briefly in [14, 15].

In this article detail analysis has been done for PPN-based 10T SRAM cell (PPN10T), transmission-based 8T (TG8T), conventional 6T SRAM (C6T) and projected a novel 10T SRAM cell (P10T) to tackle the problems faced by SRAM cells. The paper has been organized in the following order: in Sect. 2 transistor sizing and Bit-line leakage methods have been discussed. Section 3, explain about the proposed circuit, and performance of the circuit is analyzed in Sect. 4. Finally, in Sect. 5, conclusion of the work has been summarized.

2 Transistor Sizing and Bit-Line Leakage

SRAM cell design is sensitive to transistor sizing. The pull-up, pull-down, and access transistors sizes need to be appropriately selected to get the desired write and read operations.

The conventional 6T SRAM cell (to be called 'C6T' hereon) based on CMOS inverters is shown in Fig. 1. It consists of two back to back connected inverters and two access transistors N2 and N4. The access transistors are connected between inverters and bit-lines BL and BLB. The gates of N2 and N4 are connected to word line WL. The access transistors are turned on through the word line to enable writing and reading operation and turned off when the cell is in standby mode. The same ports are used for read and write operation.

Let us assume that the conventional 6T SRAM cells, '0' is stored at Q and '1' at Qbar ('Q'). For read operation, word-line (WL) and both bit-lines (BL and BLB) are held at '1'. Now, as Q is '0', then BL will discharge through pull-down transistor of 'N1'. For the flow of current, there must be some voltage difference between drain

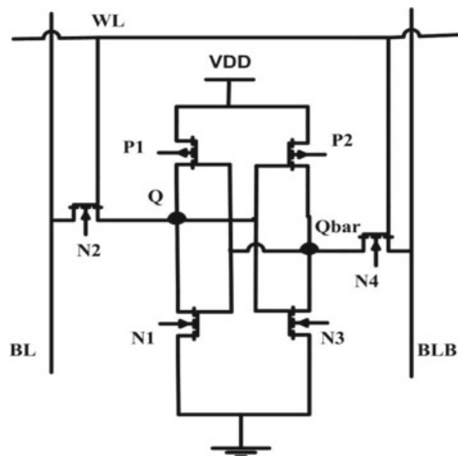

Fig. 1 Conventional 6T SRAM cell

and source of transistor of ‘N1’. Thus, the voltage at Q goes high by small amount for the time WL = 1. If it goes beyond this small amount, then input to right inverter (formed by P2 and N3) will become ‘1’ and ‘Q’ will be ‘0’. So, it will flip the data during the read operation. This is called the read disturbance problem. Thus, we should ensure that the voltage at Q should not increase too much. Thus current drive strength of ‘N1’ must be higher than that of ‘N2’ to make I_{read} to flow through series connection of ‘N1’ and ‘N2’. Drive strength of pull-down device and access device are given in Eqs. 1 and 2:

$$\beta_{\text{d}} = \mu \frac{W_{\text{d}}}{L_{\text{d}}} (V_{\text{cell}} - V_{\text{th,d}})^2 (V_{\text{ds,d}})^2 \quad (1)$$

$$\beta_{\text{a}} = \mu \frac{W_{\text{d}}}{L_{\text{a}}} (V_{\text{WL}} - V_{\text{th,a}})^2 (V_{\text{ds},a})^2 \quad (2)$$

To increase the drive strength, we cannot increase $V_{\text{ds,d}}$ in Eq. (1), as it is the voltage at point Q. So, to have drive strength of pull-down device should be higher than that of access device i.e.$\beta_{\text{d}} \gg \beta_{\text{a}}$.

So, to avoid data flipping (to have stable read), we can (i) increase W_{d} (ii) reduce the $V_{\text{th,d}}$ (iii) increase $V_{\text{th,a}}$ (iv) use cell voltage V_{cell} greater than V_{WL}. However, when we don’t want to go in handling voltages, we can make W_{d} higher than W_{a}. Also, increasing $V_{\text{th,a}}$ will help in reducing the bit-line leakage.

In Fig. 2, during the read operation in an SRAM cell, both the bit-lines are made high. If ‘0’ is stored in all an accessed cells of the particular column, and the threshold voltage of access transistors (connected to BL) is less, then sub-threshold leakage current I_{leak} will be flowing in each an accessed cell. As there are many cells in single column, then due to each I_{leak} the BL, so ‘BL’ get discharged and appear wrong output. Hence, this leakage current limits the number of cells present in one column. Consequently, increasing the threshold voltage of access transistors helps in avoiding I_{leak} and thereby increasing the number of cells present in a single column. However, increasing $V_{\text{th,a}}$ will reduce the current (as in Eq. 2) I_{read} which discharges the bit-line, and it takes a longer time to read thereby increasing read time. So, there is a trade-off between leakage reduction and write noise margin or read the time.

3 Proposed Circuit

In Fig. 3, the proposed SRAM cell (to be called P8T hereon) is shown. This circuit contained two extra transistors N5 and N6 which will provide a discharging path for a read current. In conventional SRAM cell (C6T), the read current (I_{read} or Ion) flows through access transistor N2 (N4) and pull-down transistor N1 (N3). As this flow path passes through the storage nodes, C6T suffers disturbance while the read operation. Moreover, in PPN10T cell, two pull-down transistors (N5 and N6) are connected in the circuit. This forms a discharging path for read current on both sides

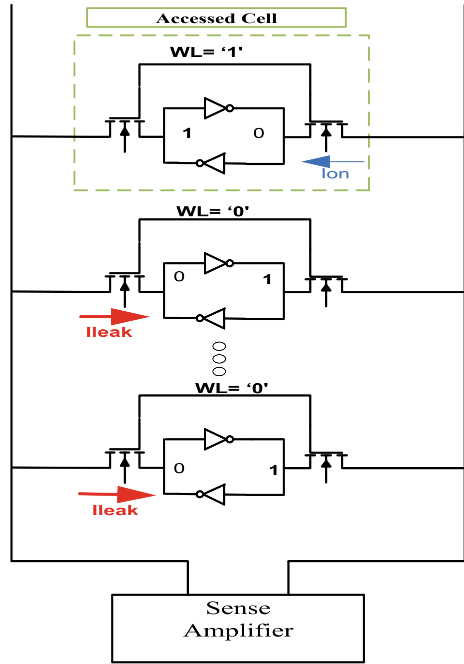

Fig. 2 Investigation of bit-line leakage problem

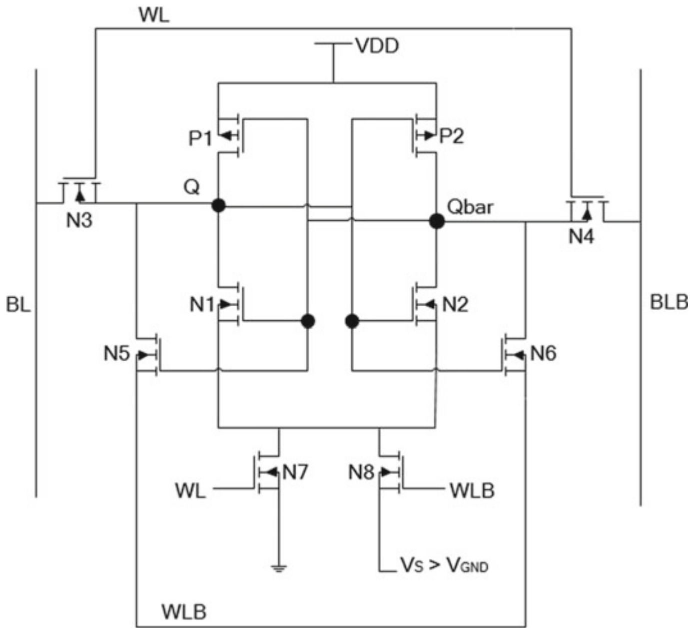

Fig. 3 Proposed SRAM cell (P10T)

of this SRAM cell, through one pull-down transistor (N5 or N6) and one access transistor (N3 or N4). Therefore, this discharging path for read current, PPN10T cell design does not suffer from disturbance. In addition to this, the pull-down transistors (N5 and N6) are connected to the pseudo storage nodes of WLB on each side of the cell. So, during a read operation, this WLB will be connected to ground, and thus the read current will flow from bit-line to ground through N5 or N6.

It is worth notice the fact that N-controlled SRAM design in which the data stored in the cell is reserved even when the cell is in the standby mode. This technique uses Dynamic Voltage Scaling (DVS) to reduce the leakage power in the cells. Due to this, the suggested design has a striking features of achieving tremendous leakage power savings. For this two-tail transistors in our proposed cell are connected. In this approach, usually a large row in the array of memory is partitioned into a number of smaller identical sub-blocks, and one pair of nMOS tail transistors controls each of these blocks.

In Fig. 4, N7 and N8 are shown and called tail transistors. Transistor N7 is controlled by WL, and it connects the cell to ground voltage. Transistor N8 is controlled by WLB, and it connects the cell to the voltage 'Vs' which is slightly higher than the ground voltage. When the cell is not in standby mode, i.e., when WL

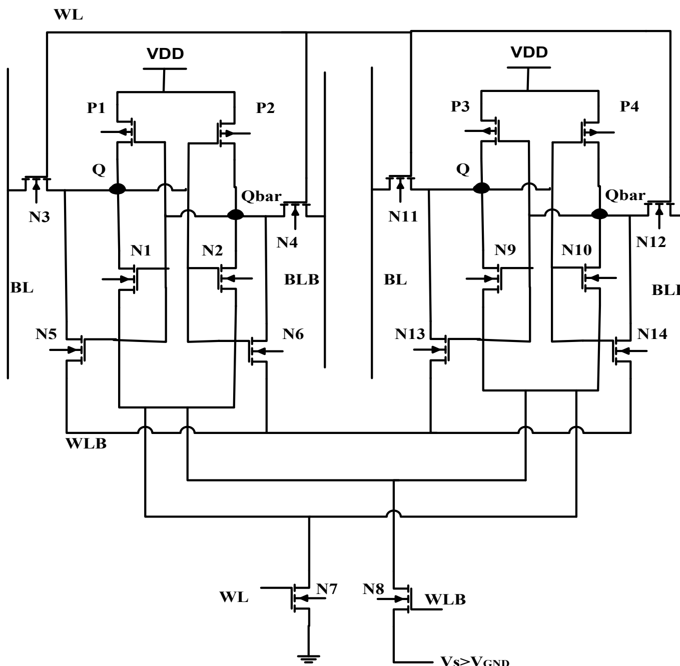

Fig. 4 Same tail transistor shared by two 10T SRAM cells from same row

is ‘1’, transistor N7 is ON and the cell is connected to ground thereby completing the path of VDD to ground. Also, when the cell is in standby mode, i.e., when WLB is ‘1’, transistor N8 is ON and the cell is connected to ‘Vs’ which is slightly higher than ground voltage thereby breaking the path of VDD to ground. These two-tail transistors are shared by more than one SRAM cell.

4 Performance Analysis

In this section, performance analysis have been done for proposed design, in terms of read access time, write access time, hold static noise margin, write static noise margin (WSNM), read static noise margin (WSNM), read-ability, write-ability, $I_{\text{read}}/I_{\text{leak}}$ ratio, static power dissipation, dynamic power dissipation and etc.

4.1 Read Access Time (T_{RA})

The TRA (read access time) is the time difference between the point when word line (WL) rises to 50% of its final state from its initial low state and the point when BL/BLB is discharged by 0.05 V from its initial high state [15]. During the read operation, there must be a difference of at least 0.05 V between the voltage levels of BL and BLB to avoid read error. As calculated, TRA for C6T is 0.5022 ns; for PPN10T it is 1.022 ns; for TG8T it is 1.44 ns, and for P10T it is 1.2857 ns.

4.2 Write Access Time (T_{WA})

The TWA (write access time), when writing ‘0’, is defined as the time difference between the point when WL reaches 50% of its final state (from its initial low state) and the point when ‘Q’ (Storing ‘1’ initially) falls to 10% of its initial high state. Similarly, TWA, when writing ‘1’ at ‘Q’ is defined as the time difference between the point when WL reaches 50% of its final state (from its initial low state) and the point when ‘Q’ (Storing ‘0’ initially) rises to 90% its initial low state. TWA for C6T is 0.38 ns; for PPN10T it is 0.9775 ns; for TG8T it is 0.4511 ns, and for P10T it is 0.4955 ns.

4.3 Hold Stability

Hold static noise margin (SNM) is helpful in determining the hold stability of SRAM cell, defined as that minimum value of noise voltage (DC) which will invert the data store in the cell when it occurs (develops). The noise margins are obtained using the butterfly curves. In the smaller wing, a largest fit table square is drawn, and a side length of that square gives the value of noise margins.

The side length of that square represents the SNM (hold SNM) of the cell. Figure 5 shows the 'butterfly curve' for cells of C6T, PPN10T, TG8T. From this figure, we can see that all squares have nearly equal sides, i.e., noise margins are nearly the same. The reason behind that is the internal latch structure is more or less the same in all three cells. As observed C6T, PPN10T and TG8T cells shows 275 mV, 296 mV, and 280 mV hold SNM respectively. Figure 6, shows 'butterfly curve' of P10T. As observed, P10T cell show 145 mV hold SNM. When static noise margin value is equal to or above 25% of supply voltage, the cell is considered to have good read stability.

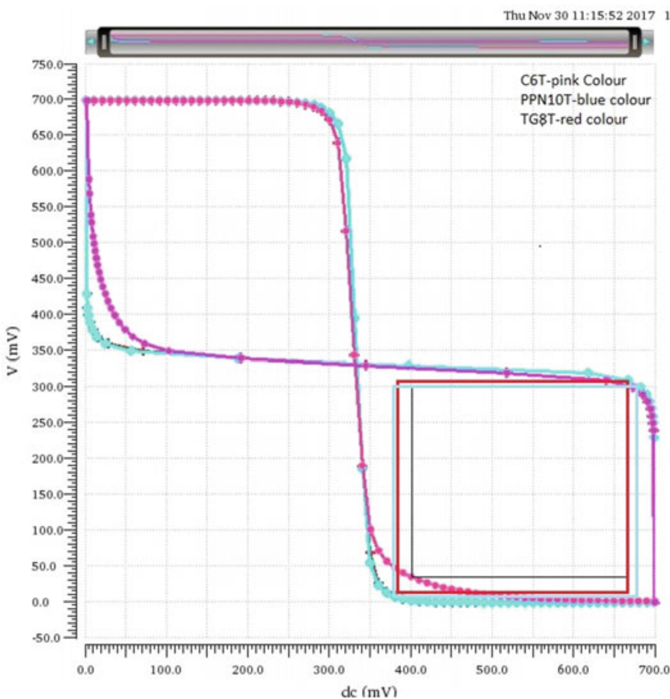

Fig. 5 Static noise margin (SNM) of C6T, PPN10T, TG8T at supply voltage of 0.7 V

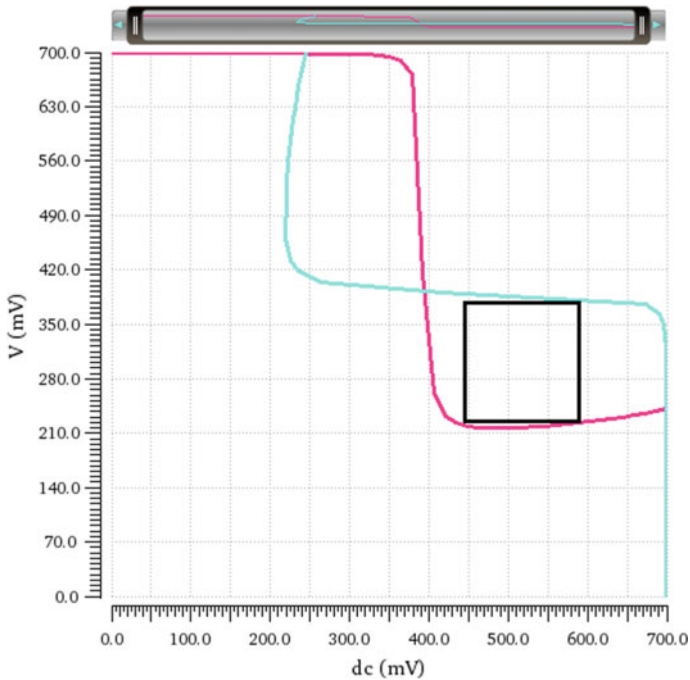

Fig. 6 Static noise margin (SNM) of P8T at supply voltage of 0.7 V

4.4 Write-Ability

Write static noise margin (WSNM) gives the write-ability of SRAM cell. Suppose a storage node is having a value '1', then the ability of SRAM cell to bring down this storage node from '1' to '0' is determined using the write-ability of the cell. If BL is successful in bringing the voltage at 'Q' (storing '1' initially) down to voltage level below the trip voltage of the other inverter with output 'Qbar' so that it content is tripped and '0' is stored in 'Q' and '1' that stored in 'Qbar'. The ratio of strength of pull-up transistor P1 (P2) to that of access transistor N2 (N4) determines the write-ability of SRAM cell. Figure 7, shows the 'butterfly curve' of the cells C6T, PPN10T, TG8T for determining WSNM. As observed, in C6T, PPN10T and TG8T

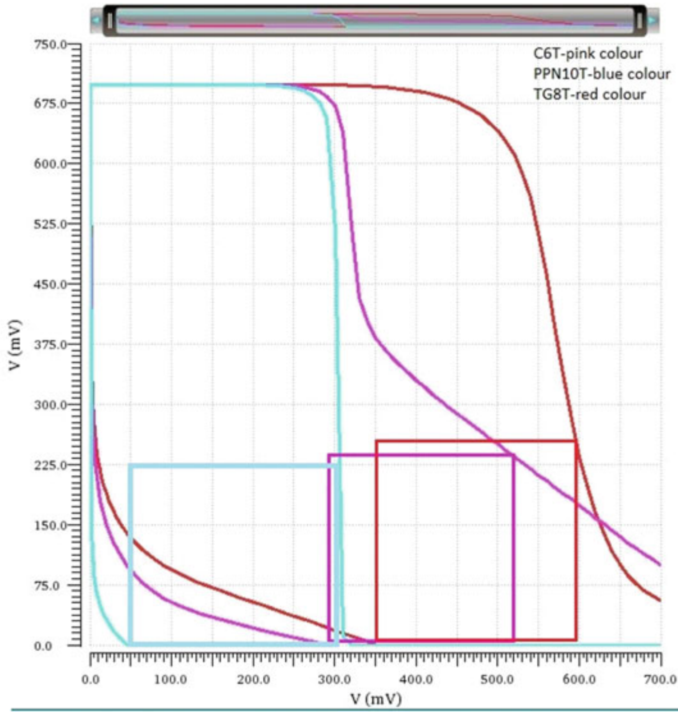

Fig. 7 Write static noise margin (WSNM) of C6T, PPN10T, TG8T at supply voltage of 0.7 V

cells show 224 mV, 168 mV, and 265 mV WSNM respectively. As observed in Fig. 8, P8T show 252 mV WSNM. The WSNM is highest for TG8T as it uses transmission gates instead of nMOS transistors for access transistors.

4.5 Read Stability

Read static noise margin (RSNM) is helpful in determining the read stability of an SRAM cell. Noise can easily affect the SRAM cell for the duration of the read operation because the voltage at '0' storing node rises by a small amount. The access transistor, size ratio control the rise in voltage level of storage node. If this ratio is small, then there will be high voltage at drain terminal of the pull-down transistor. Thus, there will be a high voltage difference between drain and source of pull-down transistor. This will require just a small noise voltage at the '0' storing node to invert the data stored in the cell. Therefore, read static noise margin is a critical

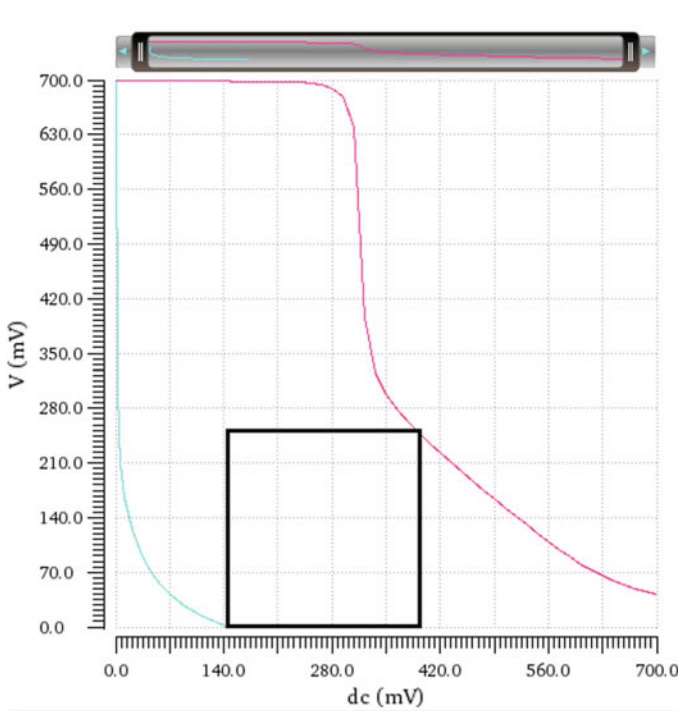

Fig. 8 Write static noise margin (WSNM) of P8T at supply voltage of 0.7 V

parameter in SRAM cell design. Figure 9 shows the 'butterfly curve' of the cells C6T, PPN10T, TG8T for determining RSNM. As observed in C6T, PPN10T and TG8T shows 105 mV, 290 mV, and 106 mV RSNM respectively. As observed in Fig. 10, P10T show 160 mV RSNM. As we can see, the RSNM is good for PPN10T and P8T cells as they use separate path for read current thereby avoiding the problem of the read disturbance.

4.6 I_{read}/I_{leak} *Ratio or* I_{on}/I_{off} *Ratio*

The on-current (I_{on}) is the current flowing into an accessed cell from the bit-line connected to it for the duration of the read operation while the off-current (I_{off}) is the current leaked to all the other an accessed cells of the same column. Usually, for reliable read operation, I_{on}/I_{off} ratio is 10 or above so that there is sufficient voltage swing between the bit-line and its complement at the time when sense amplifier starts

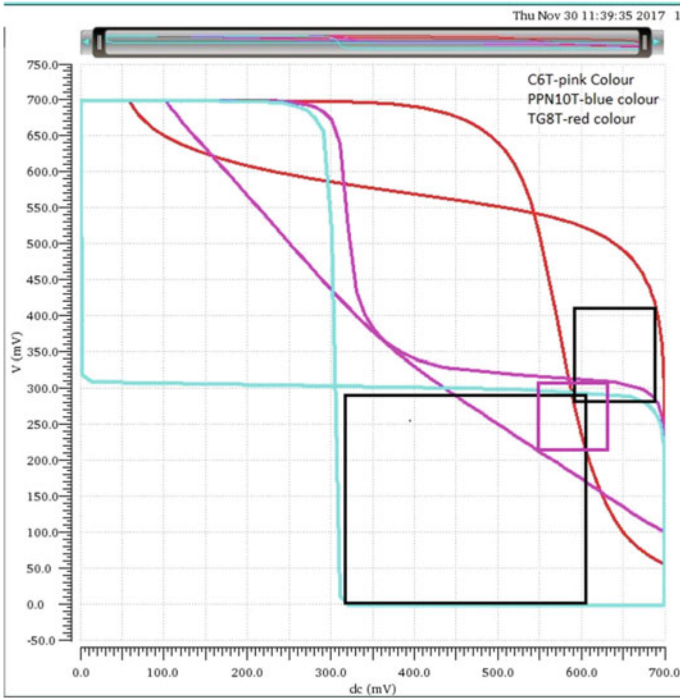

Fig. 9 Read static noise margin (RSNM) of C6T, PPN10T and TG8T at supply voltage of 0.7 V

its operation. Owing to the increased standby mode leakage current in transistors, particularly at very low voltages, this ratio has worsened. This bit-line leakage limits the bit-line length, thereby limiting the number of cells attached to a bit-line. Hence, a good I_{on}/I_{off} ratio is expected.

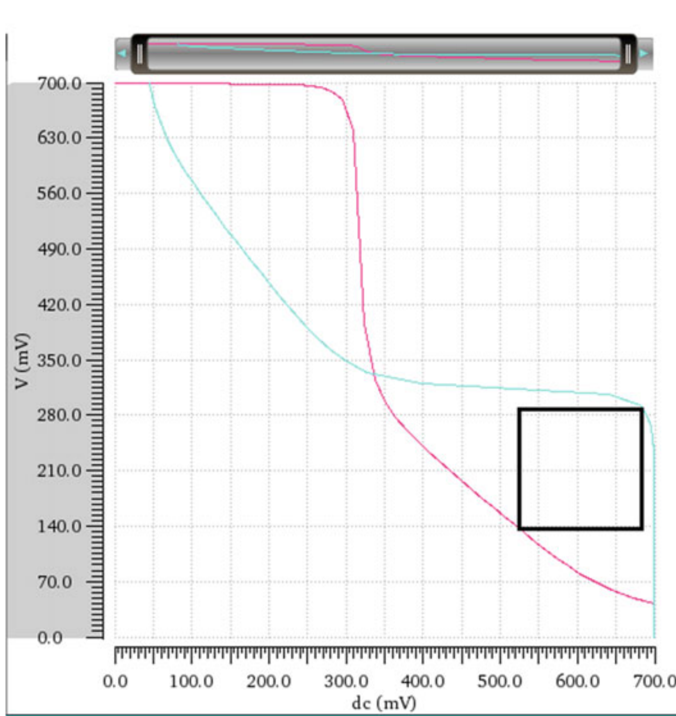

Fig. 10 Read static noise margin (RSNM) of P10T at supply voltage of 0.7 V

Table 1 gives the comparison of I_{read}/I_{leak} ratio of C6T, PPN10T, TG8T, and P8T at different supply voltages. The PPN10T and P10T show a good I_{read}/I_{leak} ratio among four circuits. Hence we can have a highest bit-line length in PPN10T and P10T, thereby allowing us to accommodate additional number of cells in a single column and increasing transistor density.

Table 2 gives the comparison of values of different performance parameters for C6T, PPN10T, TG8T, and P10T. The proposed SRAM cell has compact advantages in terms of hold, read and write SNM, delay and power dissipation over conventional 6T-SRAM, 10T-SRAM and TG8T-SRAM.

Table 1 I_{READ}/I_{LEAK} comparison

V_{dd} (V)	Conventional 6T SRAM (C6T SRAM)			PPN-based 10T SRAM cell (PPN10T SRAM)			Transmission gate-based 8T SRAM (TG8T SRAM)			Proposed 8T SRAM (P10T SRAM)		
	I_{read} (μA)	I_{leak} (nA)	I_{read}/I_{leak} (× 10^3)	I_{read} (μA)	I_{leak} (pA)	I_{read}/I_{leak}(× 10^3)	I_{read} (μA)	I_{leak} (pA)	I_{read}/I_{leak} (× 10^3)	I_{read} (μA)	I_{leak} (pA)	I_{read}/I_{leak} (× 10^3)
0.3	0.041	0.0128	3.2	0.0077	0.395	19	0.016	3.508	19	0.0071	0.3807	18.64
0.4	0.565	0.152	3.7	0.1054	0.577	182	0.169	4.356	38	0.082	0.563	145
0.5	4.132	0.239	17.28	0.797	0.797	1000	1.096	5.204	210	0.544	0.757	718
0.6	17.411	8.004	2.17	3.840	1.067	3598	5.210	6.056	860	2.7769	0.969	2865
0.7	42.814	373.02	0.11	13.226	1.401	9440	16.513	6.916	2387	9.059	1.2059	7512
0.8	86.958	0.0176	0.0049	32.297	1.815	17,790	35.070	7.792	4500	21.062	1.4735	14,293

Table 2 Comparison of four SRAM cells

Design specification	Conventional 6T SRAM (C6T SRAM)	PPN-Based 10T SRAM cell (PPN10TSRAM)	Transmission gate-based 8T SRAM (TG8T SRAM)	Proposed 10T SRAM (P10T SRAM)
Process technology (nm)	45	45	45	45
Hold SNM (@ 0.7 V) (mV)	275	296	280	145
Read SNM (@ 0.7 V) (mV)	105	290	106	160
Write SNM (@ 0.7 V) (mV)	224	168	265	252
Write access delay (T_{wa}) (ns)	0.380	0.9775	0.4511	0.4955
Read access delay (T_{ra}) (ns)	0.5022	1.0226	1.440	1.2857
Hold power dissipation (@ 0.7 V) (nW)	78.82	25.63	78.82	11.98
Dynamic power dissipation (@ 0.7 V) (μW)	2.669	2.314	1.766	0.9024

5 Conclusion

The conventional 6T SRAM cell faced many problems due to ever-increasing process variation and technology scaling. New cells with more transistors as discussed and proposed in order to overcome these problems. In this work, we have studied the overview of some previous techniques and proposed 10T SRAM cell and analyzed the circuits for different parameters like write access time (TWA), read access time(TRA), hold static noise margin, read SNM, write SNM, I_{read}/I_{leak} ratio, hold power dissipation. The performance analysis shows that in PPN10T to avoid the read disturbance problem and separate read path was used in PPN10T and hence proposed cell shows good RSNM that is necessary to make read operation successful. The projected cell gives better WSNM necessary to make write operation successful. Hold power dissipation and dynamic power dissipation is lowest in a proposed cell. The I_{read}/I_{leak} ratio of the suggested circuit is very good so that we can have a large number of SRAM cells in the single column of a memory array. Also, when we reduce leakage current to increase I_{read}/I_{leak} ratio, it gives overhead of increased read access time as seen in the case of all cells except conventional an SRAM cell. Moreover, due to the dynamic voltage scaling technique, the proposed circuit gives the lowest but enough hold SNM among four cells. Overall the proposed SRAM cell has many advantages over conventional SRAM cell, which overweight its few disadvantages.

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