Island Engineering of Single-Electron Transistor for Room Temperature Operation

Raj Shah, Rutu Parekh, and Rasika Dhavse

Abstract Single-electron transistors (SETs) have shown their competence to overpower MOSFETs as well as FinFETs in low power regime. However, research to exhibit room temperature operation and its demonstration for application in logic and memory circuits is still in infancy. A SET contains two ultra-thin tunnel barriers and a conductive island which work on the principle of Coulomb blockade (CB) and tunneling. Its dimensions must be planned properly to exhibit room temperature operation with CMOS compatibility. In this work, the island engineering technique is proposed for devising SET so as to observe both Coulomb blockade and quantum mechanical tunneling at room temperature. The island engineering is carried out for aluminum and copper island. The SET has been simulated in TCAD using the designed dimensions and its output as well as transfer characteristics have been plotted at room temperature. The analyses illustrate that out of all the SET devices, aluminum island SET with 4 nm tunnel barrier with 17 nm island length offers the desired CB and tunneling current in tens of nA range. To validate the results and ascertain the concept of CMOS compatible design, SET transfer and output characteristics have been simulated using Cadence Virtuoso using MIB model. The proposed technique of SET is also compared with the other SET optimization techniques.

Keywords Coulomb blockade · Island engineering · MIB model · Nano-electronics · Quantum mechanical tunneling · Single-electron transistor · TCAD

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1 Introduction

Owing to small size and low power consumption, single-electron transistors (SETs) are becoming an attractive alternative in the post-CMOS era of semiconductor technology [1–4]. They operate on the principles of Coulomb blockade and quantum mechanical tunneling (QMT), depicting the on and the off states of the device, respectively [5–7]. SETs have proved their potential to be a promising candidate for non-volatile memory as well as logic applications [2, 3, 8]. SET-MOS hybridization is also one huge field of interest for logic development. It is envisaged that SETs can outperform CMOS in nanometer regime with its virtues like ultra-low power consumption and scalability [2, 3, 9]. Since last two decades, many researchers have worked to overcome two fundamental issues of SETs, viz., (a) mass production and (b) room temperature operation. In recent years, with advent in time and technology, many CMOS-compatible processes are demonstrated for fabrication of SETs [2, 4, 10–12]. They include nanodamascene processes [4], patterning with reactive ion etching and electromigration, chemical mechanical polishing-based fabrication [10], self-assembly and self-alignment of quantum dots [11], even optical lithography of silicon nanowire [12]. Thus, prospects of integrating SETs in a CMOS process are bright. However, room temperature operation is still a matter of experimentation.

Coulomb blockade is inherently a low energy phenomenon [6, 7]. Hence, it cannot be detected at ambient temperatures easily. So, to observe the SET operation in true sense, the device needs to be engineered carefully. The material and dimensions of island play crucial role in tunneling of electron between source and drain. Hence, the effect of island on SET drain current along with CB and QMT must be observed. The structure of island should also be compatible with the CMOS fabrication processes. In this paper, we will present the rudiments of SET design followed by a detailed analytical approach. We will then simulate the device demonstrating thorough island engineering. Results show occurrence of both, the Coulomb blockade and the quantum mechanical tunneling in the optimized device. Finally, we will present validation of our device with MIB model [3].

2 SET Design Considerations

As shown in Fig. 1, a SET consists of two tunnel junctions on source and drain sides sandwiching a quantum dot. Every junction offers a barrier—popularly known as Coulomb blockade—to flow of electrons. These junctions or barriers ensure weak coupling of source and drain with the quantum island. An electron from source, after overcoming Coulomb blockade energy level, enters the island by the process of tunneling. Simultaneously, an electron leaves the island and tunnels to the drain, causing current to flow. Thus, to ensure the charge transfer, one needs to supply Coulomb energy to the island. This energy can be supplied by an external voltage source. It is given by [5–7],

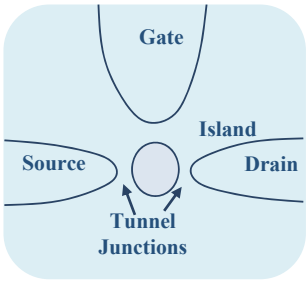


Fig. 1 Structural schematic of single-electron transistor

$$E_C = \frac{e^2}{2C_\sum} \tag{1}$$

where $C_\sum$ is the capacitance of the island given by $(2C_J + C_G)$, C_J being the tunneling junction capacitance. Correspondingly, Coulomb voltage is given by

$$V_{\mathrm{CB}} = \frac{e}{2C_\sum} \tag{2}$$

This capacitance is primarily governed by the device geometry and material parameters. With reduction in this capacitance, E_C increases, making the junction more opaque.

In addition to this capacitive coupling, the barrier offers tunnel resistance, which must be larger than the fundamental resistance $R_T \gg \frac{\hbar}{q^2}$, that is, approximately 25.8 KΩ [5–7]. It ensures localization of electron states to the island during blockade. R_T also controls the driving capability of the device. The device maximum operating frequency is $1/(R_T C)$ [9]. Conflict of speed and power can be addressed by fine tuning these two electrical parameters. This demands appropriate materials choice and fabrication of capacitors of the order of attofarads, which is possible in today's era.

For designing a rugged SET, Coulomb energy of the SET should be sufficiently higher than the ambient thermal energy. Table 1 illustrates capacitance and bias requirements with respect to thermal robustness. General trend dictates acceptable range as 20 $K_B T$.

It is evident from Table 1 that for room temperature operation of SETs, appropriate tunnel junction engineering and optimization is crucial so as to obtain: (a) very low total capacitance (aF), (b) high driving current (nA) and (c) very low thermionic current (during opaque state of the junction). A low-k dielectric like SiO_2 can offer a barrier less than 0.4 eV [13] aiding high level of transparency. But for junction opacity, high-k dielectric like TiO_2 which offers barrier greater than 1 eV is required. To resolve this conflict, Hajjam et al. proposed multi-dielectric stack to control the off current [13]. However, it involved realizing ultra-thin layers of various dielectric increasing design and process complexity. We propose that instead of tunnel

Table 1 Capacitance and bias requirements with respect to thermal robustness

C_G (aF)	C_Σ(aF)	E_C (eV)	$T = E_C/nK_B$ ($n = 1$) (K)	$T = E_C/nK_B$ ($n = 20$) (K)	$V_{CB} = e/2C_\Sigma$ (V)	$V_{BIAS} = e/2C_G$ (V)
0.023	0.115	1.39	16,000	800	0.695	3.47
0.046	0.138	1.15	13,000	650	0.575	1.73
0.14	0.232	0.68	7880	394	0.34	0.57
0.18	0.272	0.59	6840	342	0.295	0.44
0.023	0.093	1.72	19,900	9950	0.86	3.47
0.046	0.116	1.37	15,900	7950	0.685	1.73
0.14	0.21	0.76	8810	440	0.38	0.57
0.18	0.25	0.64	7420	371	0.32	0.44

engineering, one can opt for island engineering to achieve acceptable I_{ON} and I_{OFF} values. It is comparatively easy, simple to comprehend and process-friendly.

Figure 2a, b shows structure and MIB model of a single-gate SET [3]. Source, drain and gate are made up of n-polysilicon (phosphorus, 1e19 cm^{-3}), whereas the substrate is p-silicon (boron, 1e15 cm^{-3}). Tunneling junction capacitances on source as well as drain side are $C_{TD} = C_{TS} = C_J$, control gate capacitance is C_G, tunnel junction resistances are $R_{TD} = R_{TS} = R_T = 1$ MΩ. The total device capacitance is defined as $C_\Sigma = 2C_J + C_G$. SET design parameters compatible with BSIM predictive technology model (PTM) [14] and 22 nm node CMOS model operation at $T =$ 300 K are chosen. Consequently, supply voltage is chosen to be 0.8 V. For a robust reliable design of SET logic, which can operate with the least possible error at room temperature, the charging energy E_C must be as large as possible compared with the

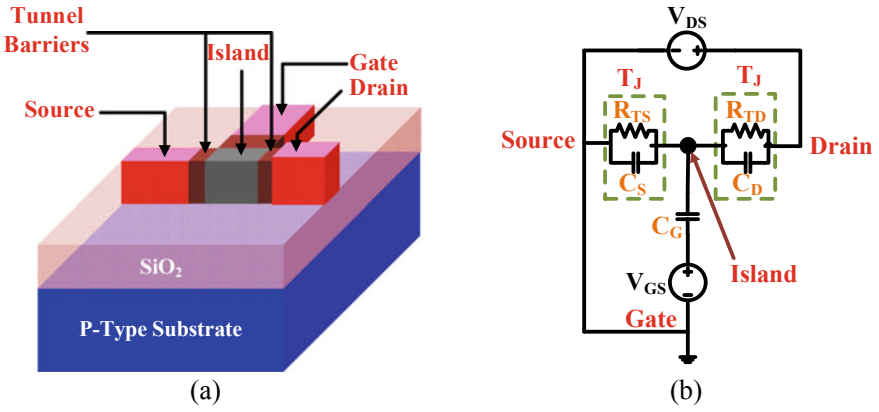


Fig. 2 **a** Single-gate SET structure, **b** equivalent MIB model where tunnel barriers are represented by parallel RC combinations ($R_{TS} \parallel C_{TS}$ and $R_{TD} \parallel C_{TD}$), gate dielectric as gate capacitance C_G, conductive island as black dot and two bias supplies, namely, V_{DS} and V_{GS} between drain—source and gatesource, respectively [3]

thermal energy. As such, Coulomb/charging energy $= e^2/C_\Sigma = 40\ K_BT = 1.036$ eV. This leads to a value of 0.155 aF for C_Σ. So, Coulomb blockade voltage $= e/2C_\Sigma = 0.51$ V. Control gate capacitance $= e/2V_{DD} = 0.045$ aF. Hence, junction/tunnel capacitance $= (C_\Sigma - C_G)/2 = 0.055$ aF. Background charge is neglected.

3 Island Engineering

Figure 3 shows top view of single-gate SET under consideration.

Table 2 illustrates SET electrical parameters and their possible mapping with its physical parameters. Our strategy is to play with island and junction dimensions while maintaining overall device dimension constant. The tunnel barrier engineering plays a vital role for this work to choose the tunnel barrier thickness [15]. We have experimented with aluminum and copper as island material, due to general good conductivity. In TCAD simulations, for global device, we used Philips Unified Mobility Model because it incorporates doping and temperature dependencies. For modeling tunneling near insulator for rapidly varying field, we used band-to-band and Schenk recombination models [16]. At material interfaces, we also used direct tunneling model as the barrier is trapezoidal [15, 16]. Junction width less than 3 nm did not result in satisfactory Coulomb blockade and greater than 4 nm did not show tunneling in the neighborhood of bias voltage. Under no influence of gate, devices

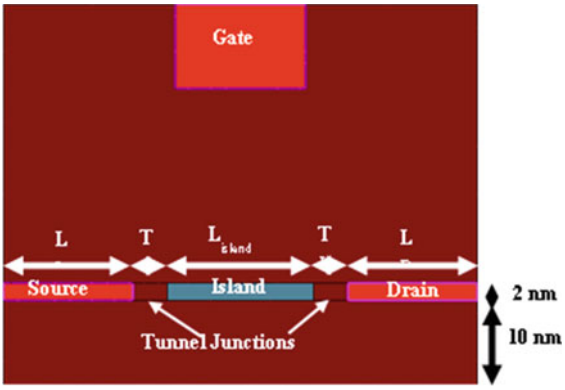


Fig. 3 Top view of single-gate SET

Table 2 Physical and electrical parameters of SET

Junction width	Physical parameters	Electrical parameters	Device name
$T_J = 4$ nm	$L_S = L_D = 15$ nm, $L_{island} = 17$ nm	$C_\Sigma = 0.11$ aF, $n = 27$	A
	$L_S = L_D = 30$ nm, $L_{island} = 32$ nm	$C_\Sigma = 0.18$ aF, $n = 17$	B
$T_J = 3$ nm	$L_S = L_D = 15$ nm, $L_{island} = 19$ nm	$C_\Sigma = 0.14$ aF, $n = 22$	C
	$L_S = L_D = 30$ nm, $L_{island} = 34$ nm	$C_\Sigma = 0.20$ aF, $n = 15$	D

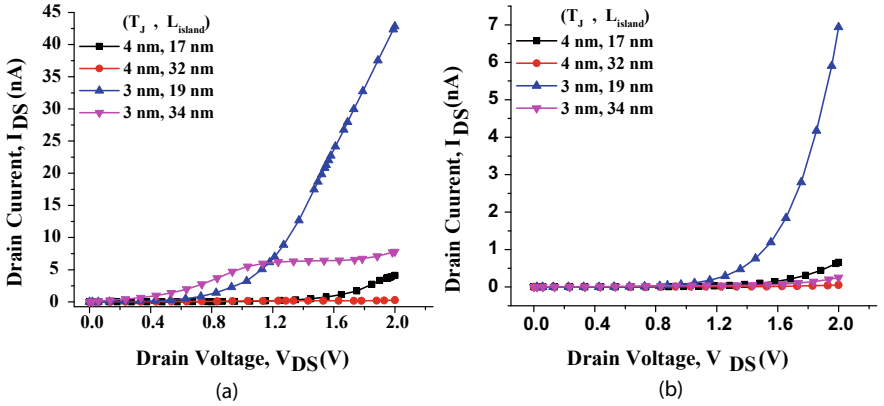


Fig. 4 V_D–I_D characteristics of single-electron devices for **a** aluminum island and **b** copper island for different island dimensions

exhibit blockade and tunneling as shown in Fig. 4a, b, for aluminum and copper island, respectively.

The devices clearly show the mechanisms of Coulomb blockade and quantum mechanical tunneling. In the limiting case of small structures, the structure resistivity becomes proportional to ρ0 * λ for any given fixed dimension [17], where ρ0 and λ are the bulk resistivity and mean free path for electron phonon scattering, respectively. Thus, the metal with the lowest product ρ0 * λ is expected to exhibit the highest conductivity. This product is 6.70e–16Ω m^2 for copper and 5.01e–16Ω m^2 for aluminum [17]. Hence, the current capacity of aluminum devices is higher than the copper devices. Coulomb voltage and SET capacitances extracted from above profiles for all the devices are listed in Table 3.

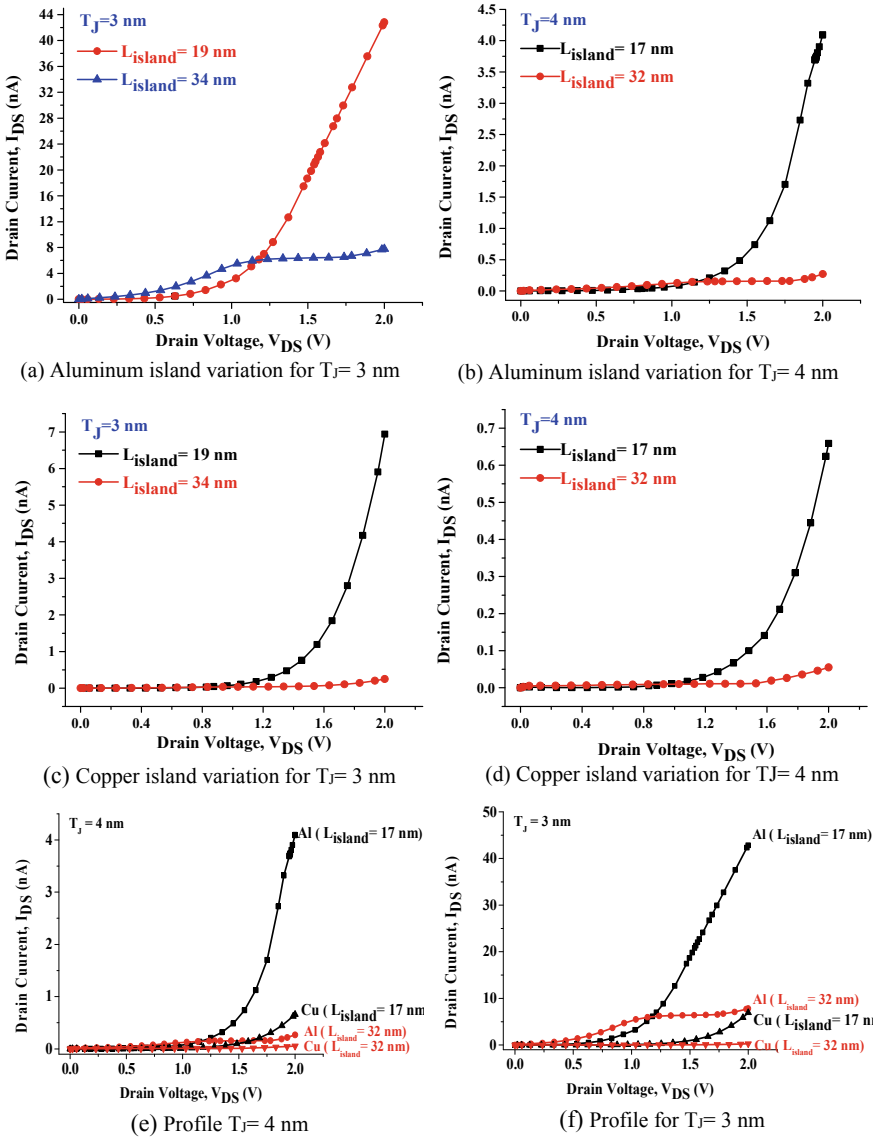
First observation here is that copper island devices offer better confinement than their aluminum counterparts. Small islands have higher Coulomb voltage. This is attributed to increased confinement and hence higher blockade. It is also observed that the extracted values have higher degree of matching as the device capacitance

Table 3 Derived and extracted parameters of SET

Device name	Analytical capacitances (aF)			Analytical V_{CB} (V)	Extracted V_{CB} (V)		Extracted total capacitance $C_{\sum}$(aF)	
	C_G	C_J	$C_{\sum} = 2C_J + C_G$	$e/C_{\sum}$	Aluminum Island	Copper Island	Aluminum Island	Copper Island
A	0.045	0.035	0.11	1.38	1.2	1.2	0.134	0.134
B	0.11	0.035	0.18	0.88	0.6	1.1	0.26	0.144
C	0.045	0.0468	0.14	1.14	0.7	1.25	0.22	0.13
D	0.10	0.0468	0.20	0.8	0.2	1.05	0.8	0.15

becomes smaller and smaller. Effect of island dimension and material can be seen in Fig. 5.

So, it is found that bigger island leads to higher Coulomb blockade and lower drain current.



(a) Aluminum island variation for T_J= 3 nm

(b) Aluminum island variation for T_J= 4 nm

(c) Copper island variation for T_J= 3 nm

(d) Copper island variation for TJ= 4 nm

(e) Profile T_J= 4 nm

(f) Profile for T_J= 3 nm

Fig. 5 I–V profiles for variation in materials and dimensions of island and junction

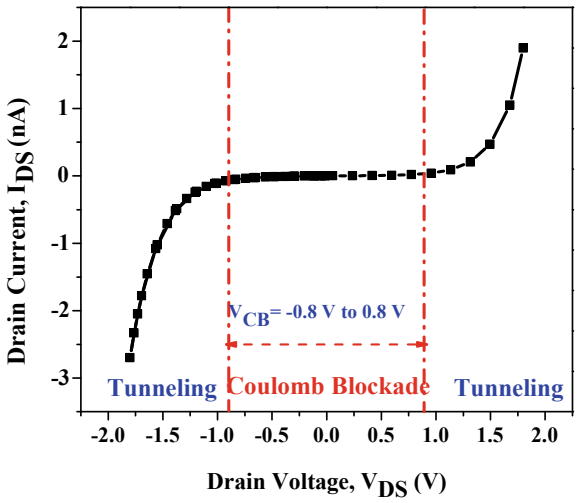


Fig. 6 Output characteristics of SET using TCAD

Finally, we settled for Device A with aluminum island ($C_G = 0.045$ aF, $C_J = 0.035$ aF) and simulated it for the bipolar I–V behavior. Result obtained is shown in Fig. 6.

4 Validation

Validation of our work was done by implementing SET in cadence with the help of MIB model. Parameters extracted from the TCAD simulations were used for implementing MIB model [3]. The model setup and various results are as shown in Fig. 7a–d.

Clear-cut manifestation of Coulomb blockade, tunneling and Coulomb oscillations indicate successful implementation of the designed device. Effect of gate voltage can be easily seen in both output as well as the transfer characteristics.

Comparison of our technique with other groups peer work is mentioned in Table 4.

5 Conclusion

Owing to modern technological inventions, it is possible to fabricate very small capacitive structures. Hence, SET has a potential to operate at room temperature in ultra-low power applications. Island engineering can be sought as simplest method for optimizing SET. The aluminum island device simulated here gives a stable room temperature operation with a current of the order of 10 nA and is compatible with

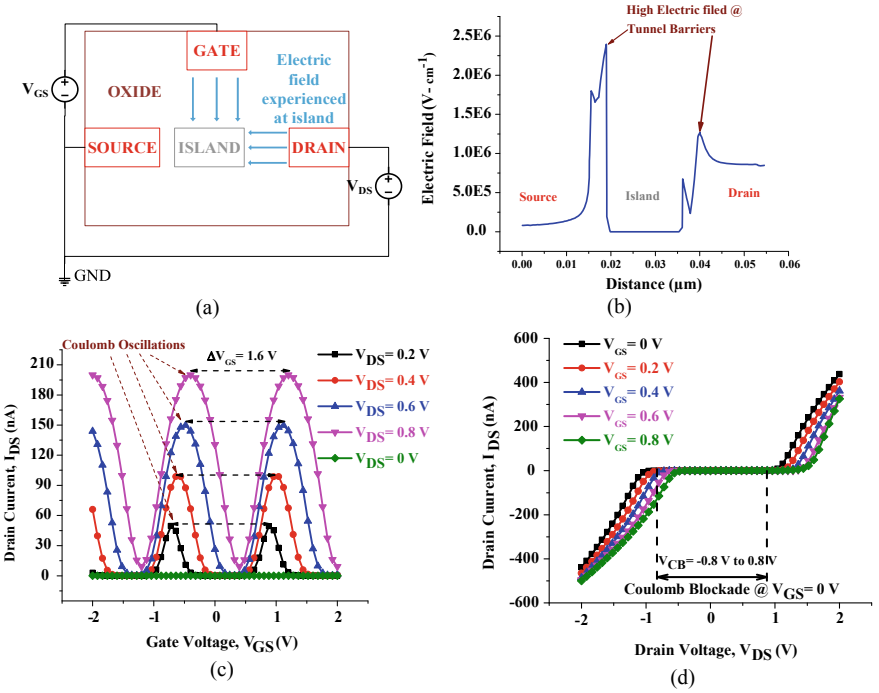


Fig. 7 **a** Electric field approaching at island, **b** simulated electric field of SET, **c** and **d** transfer and output characteristics of SET using MIB

Table 4 Comparison of proposed SET with other peer work with respect to various electrical and physical parameters

Reference	Technique	Pros	Cons
Dubuc [4, 18]	BEOL processing	CMOS BEOL process compatibility, high current drive	Required 3D integration, more back ground charge due to metallic structure
Joshi [10, 19]	Island material variation	Simple, CMOS fabrication processing	No room temperature operation
Hajjam [13]	Tunnel barrier optimization	Accurate	Time consuming, no CMOS technology compatibility
Proposed work	Island engineering (choosing proper island material and dimension)	Simple, accurate	Depends on resolution of nanoscale fabrication processes

BSIM predictive technology model (PTM) and 22 nm node CMOS model. The device can operate at a bias voltage of 0.8 V and can be used in logic as well as memory applications. The proposed technique is simple and easily realizable compared with the other techniques proposed.

References

1. Likharev K (1987) Single-electron transistors: electrostatic analogs of the dc squids. IEEE Trans Magn 23(2):1142. https://doi.org/10.1109/TMAG.1987.1065001
2. Uchida K, Matsuzawa K, Toriumi A (1999) A new design scheme for logic circuits with single electron transistors. Jpn J Appl Phys 38:4027–4032. https://doi.org/10.1143/jjap.38.4027
3. Mahapatra S, Vaish V, Wasshuber C, Banerjee K, Ionescu AM (2004) Analytical modeling of single electron transistor for hybrid cmos-set analog ic design. IEEE Trans Electron Devices 51(11):1772. https://doi.org/10.1109/TED.2004.837369
4. Dubuc C, Beauvais J, Drouin D (2008) A nanodamascene process for advanced single-electron transistor fabrication. IEEE Trans Nanotechnol 7(1):68–73. https://doi.org/10.1109/TNANO.2007.913430
5. Mahapatra S, Ionescu AM (2006) Hybrid CMOS single-electron-transistor device and circuit design. Artech House, Norwood, MA
6. Hanson GW (2008) Fundamentals of nanoelectronics. Pearson/Prentice Hall, Upper Saddle River, NJ
7. Hamaguchi C (2009) Basic semiconductor physics. Springer, Berlin, Heidelberg, Neckar
8. Durrani ZAK, Irvine AC, Ahmed H, Nakazato K (1999) A memory cell with single-electron and metal-oxide-semiconductor transistor integration. Appl Phys Lett 74:1293–1295. https://doi.org/10.1063/1.123528
9. Parekh R, Beaumont A, Beauvais J, Drouin D (2012) Simulation and design methodology for hybrid SET-CMOS integrated logic at 22-nm room-temperature operation. IEEE Trans Electron Devices 59(4):918–923. https://doi.org/10.1109/TED.2012.2183374
10. Joshi V, Orlov AO, Snider GL (2008) Silicon single-electron transistor with oxide tunnel barriers fabricated using chemical mechanical polishing. J Vac Sci Technol B Microelectron Nanometer Struct 26(6):2587–2591. https://doi.org/10.1116/1.297887
11. Ray V, Subramanian R, Bhadrachalam P, Ma L-C, Kim C-U, Koh SJ (2008) CMOS-compatible fabrication of room-temperature single-electron devices. Nat Nanotechnol 3(10):603–608. https://doi.org/10.1038/nnano.2008.267
12. Sun Y, Rusli, Singh N (2011) Room-temperature operation of silicon single-electron transistor fabricated using optical lithography. IEEE Trans Nanotechnol 10(1):96–98. https://doi.org/10.1109/TNANO.2010.2086475
13. Hajjam KGE, Bounouar MA, Baboux NA, Ecoffey S, Guilmain M, Puyoo E, Francis L, Souifi A, Drouin D, Calmon F (2015) Tunnel junction engineering for optimized metallic single-electron transistor. IEEE Trans Electron Devices 62(9):2998–3003. https://doi.org/10.1109/TED.2015.2452575
14. Predictive Technology Model (PTM). In: Predictive Technology Model (PTM). https://ptm.asu.edu/.
15. Shah R, Dhavse R (2018) Tunnel barrier optimization for room temperature operation of single electron transistors. In: Proceedings of the nanotech France 2018 international conference (nanotech France 2018), Sector, Paris, pp 37–40
16. Sentaurus Device User Guide.
17. Gall D (2016) Electron mean free path in elemental metals. J Appl Phys 119(8):085101. https://doi.org/10.1063/1.4942216

18. Beaumont A, Dubuc C, Beauvais J, Drouin D (2009) Room temperature single-electron transistor featuring gate-enhanced on-state current. IEEE Electron Device Lett 30:766–768. https://doi.org/10.1109/led.2009.2021493
19. Lee Y-C, Joshi V, Orlov AO, Snider GL (2010) Si single electron transistor fabricated by chemical mechanical polishing. J Vac Sci Technol B Nanotechnol Microelectron Mater Process Meas Phenom 28(6). https://doi.org/10.1116/1.3498748