A Fully Integrated Tunable Memristor Emulator Circuit

Vikash Kumar, Indrajit Pal, and Aminul Islam

Abstract This chapter introduces the design of a memristor emulator which can be used for fully integrated circuit applications. The design employs a single voltage differencing transconductance amplifier (VDTA) as the active building block for simulating emulator behavior. Further, the design also contains one active analog multiplier, one passive grounded resistor, and capacitor, respectively. The proposed emulator circuit is simulated on the 45 nm CMOS technology node making it both cost and power-efficient emulator circuit. All the analytical derivations mentioned in this research work have been verified by simulation results obtained using Virtuoso custom design platform of Cadence. The non-volatile nature of the proposed circuit has also been validated.

Keywords Voltage differencing transconductance amplifier · Memristor emulator · Voltage mode · Memductance · Hysteresis loop

1 Introduction

Memristor, which is the abbreviation of two words "Memory" and "Resistor," is a nonlinear two terminal element. Memristor theory is initially introduced by Leon Chua in 1971 [1]. Later in 2008, memristor fabrication was successfully carried out by Stanley Williams from the Hewlett-Packard Company using titanium oxide (TiO_2) [2]. Before the introduction of memristors, there were three basic passive

V. Kumar
Department of Electronics and Communication Engineering, Presidency University, Bengaluru, KA 560064, India
e-mail: vikashkumar@ieee.org

I. Pal · A. Islam (✉)
Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra, Ranchi, Jharkhand, India
e-mail: aminulislam@bitmesra.ac.in

I. Pal
e-mail: pal.indrajit99@gmail.com

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elements, i.e., resistor, capacitor, and inductor. As such, a linear resistor forms a relation between "voltage" and "current" and the two other fundamental elements capacitor and inductor form the relation between "voltage" and "charge" and "current" and "flux," respectively. Similarly, the two terminal passive element, memristor, forms the missing relation between "flux" and "charge." Memristor possesses memristance, which exhibits pinched hysteresis behavior. Memristance depends on the direction of current flow; i.e., when current is allowed to pass in one direction, the memristance increases whereas it decreases once the direction of current is changed. The memristor is a versatile element due to its non-volatile behavior and therefore is used in high-density memory circuits [3] and neuromorphic systems [4]. A memristor can also be employed in various analog and digital applications such as programmable sinusoidal oscillators [5], adaptive filters [6], chaotic circuits [7], logic gates [8], and digital multipliers [9].

Since the commercial viability of physical memristor is complex and expensive, researchers have focused their attention toward emulating the behavior of TiO_2 memristor as the reference model. Several research papers have been published on memristor emulator circuits which can be physically implemented [10–13]. Nevertheless, such emulators lack certain features such as use of more number of passive elements, electronic tunability, pinch hysteresis loop at reasonably lower frequencies, lower power dissipation, etc. This paper proposes a fully integrated memristor emulator circuit which employs the active element as voltage differencing transconductance amplifier (VDTA). The proposed circuit reports desirable memristor features such as tunability, lesser number of passive elements, and lower power consumption.

2 VDTA

The active block used for realizing the memristor emulator circuit is voltage differencing transconductance amplifier (VDTA) [14, 15]. Figures 1 and 2 show block diagram of VDTA and its CMOS technology realized schematic. Basically, the VDTA

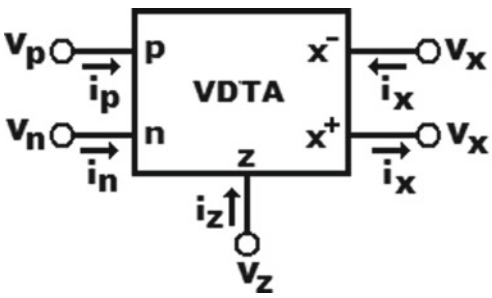

Fig. 1 Block diagram of VDTA

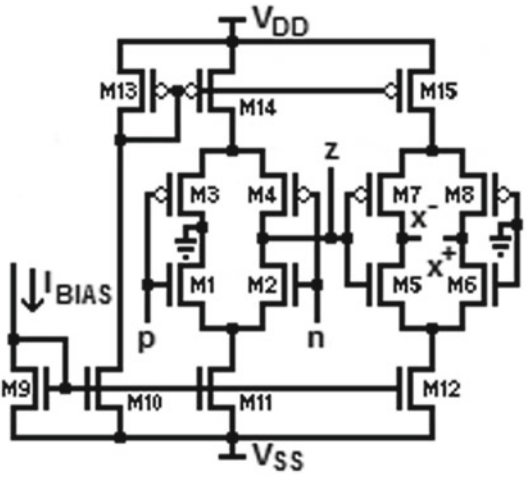

Fig. 2 Schematic of CMOS realized VDTA

consists of two operational transconductance amplifiers (OTAs) cascaded together as seen in Fig. 2.

The following matrix equation shows the current and voltage relations of VDTA's input–output terminals:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_{x-} \\ i_{x+} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ g_{\mathrm{mf}} & -g_{\mathrm{mf}} & 0 \\ 0 & 0 & g_{\mathrm{ms}} \\ 0 & 0 & -g_{\mathrm{ms}} \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix}. \tag{1}$$

Here, v_p, v_n, v_z, v_{x+}, v_{x-} and $i_{x+,}$ $i_{x-,}$ i_z are potential drops and currents at their respective VDTA ports. Current in p and n ports equals to zero due to very high impedance across them. g_{mf} and g_{ms} are effective transconductances of first and second OTAs, respectively, and are given as

$$g_{\mathrm{mf}} = \frac{g_{\mathrm{m1}} g_{\mathrm{m2}}}{g_{\mathrm{m1}} + g_{\mathrm{m2}}} + \frac{g_{\mathrm{m3}} g_{\mathrm{m4}}}{g_{\mathrm{m3}} + g_{\mathrm{m4}}}, \tag{2}$$

$$g_{\mathrm{ms}} = \frac{g_{\mathrm{m5}} g_{\mathrm{m6}}}{g_{\mathrm{m5}} + g_{\mathrm{m6}}} + \frac{g_{\mathrm{m7}} g_{\mathrm{m8}}}{g_{\mathrm{m7}} + g_{\mathrm{m8}}}. \tag{3}$$

where g_{m1}, $g_{\mathrm{m2,}}\ldots$, g_{m8} are individual transistor transconductances and can be calculated by using following relation

$$g_{\mathrm{mk}} = \sqrt{2\beta I_{\mathrm{DS}}}, \tag{4}$$

where

$$\beta = \frac{\mu_k C_{\text{ox}}}{2}\left(\frac{W}{L}\right). \tag{5}$$

Here, μ_k is mobility of kth transistor, C_{ox} is the ratio of oxide permittivity to its thickness, W and L are transistor dimensions, and I_{DS} is drain-to-source current.

3 Memristor Emulator Circuit

The presented memristor emulator circuit introduces the change in resistance by changing the value of applied voltage, v_{in}. The emulator circuit employs one VDTA as active element, two grounded passive elements, i.e., one resistor and one capacitor, an inverting/non-inverting buffer together with an analog multiplier. The configuration is shown in Fig. 3. The presented memristor emulator contains only active elements and grounded passive elements. Nonetheless, the earlier published emulator circuit comprises discrete multiplier circuits, which presents higher complexity, higher power, higher cost, etc. In this paper, the presented design consists of CMOS Gilbert cell-based analog voltage multiplier circuit which is fully integrated and consumes less power [16, 17].

Analyzing the circuit proposed Fig. 3 and using the current and voltage equations from [1], we obtain:

$$i_z = g_{\text{mF}}(v_p - v_n) = \mp g_{\text{mF}} v_{\text{fb}}, \tag{6}$$

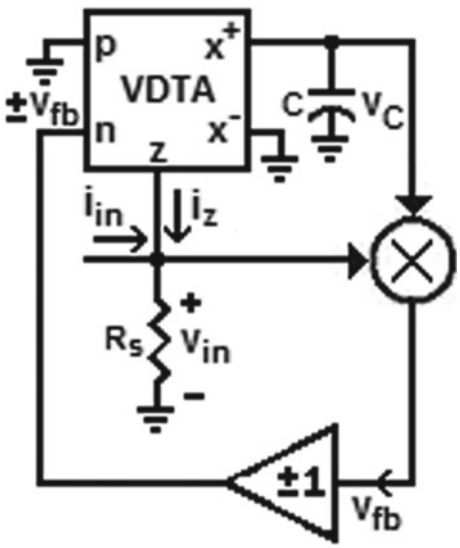

Fig. 3 Proposed VDTA-based memristor emulator

$$v_{\text{in}} = (i_{\text{in}} + i_z)R_{\text{s}} = (i_{\text{in}} \mp g_{\text{mF}} v_{\text{fb}})R_{\text{s}}. \tag{7}$$

Using (6) and (7), the current at the x^+ terminal is found to be:

$$i_{x^+} = g_{\text{mS}} v_z = g_{\text{mS}} v_{\text{in}} = g_{\text{mS}}(i_{\text{in}} \mp g_{\text{mF}} v_{\text{fb}})R_{\text{s}}. \tag{8}$$

The potential across capacitor *C,* i.e., v_{C}, is given by the integral of i_{x^+}. From (8), v_{C} is given as,

$$v_{\text{C}} = \frac{g_{\text{mS}}}{C} \int v_{\text{in}} \text{d}t. \tag{9}$$

The feedback voltage v_{fb} is obtained through CMOS Gilbert cell-based analog voltage multiplier circuit and is given by the multiplication of v_{C} and v_{in}, i.e.,

$$v_{\text{fb}} = v_{\text{C}} v_{\text{in}} = \frac{g_{\text{mS}} v_{\text{in}}}{C} \int v_{\text{in}} \text{d}t. \tag{10}$$

Putting (10) in (7), we get

$$i_{\text{in}} = v_{\text{in}} \left[\frac{1}{R_{\text{s}}} \pm \frac{g_{\text{mF}} g_{\text{mS}}}{C} \int v_{\text{in}} \text{d}t \right]. \tag{11}$$

Therefore, the memductance G_{M} is given by,

$$G_{\text{M}} = \frac{1}{R_{\text{s}}} \pm \frac{g_{\text{mF}} g_{\text{mS}}}{C} \int v_{\text{in}} \text{d}t. \tag{12}$$

From (12), the mathematical model of the presented memristor emulator shows incremental (+)/decremental (−) mode of operations.

4 Simulation Results

The presented emulator circuit has been implemented at CMOS 45-nm technology node using Virtuoso ADE of Cadence. $V_{\text{DD}} = -V_{\text{SS}}$; i.e., the power supply is considered as ±0.95 V. The passive component values are selected as $R_{\text{S}} = 1\ \text{K}\Omega$, $C = 10\ \text{nF}$. For a sinusoidal input signal (i_{in}) with amplitude of 50 μA, the behavior of characteristic frequency-dependent pinched hysteresis loop of the presented memristor emulator with variations in frequencies, i.e., at $f = 500$ Hz, $f = 1$ kHz, $f = 5$ kHz, and $f = 10$ kHz is shown in Fig. 4(a)–(d), respectively. The power dissipation of the emulator is calculated to be 3.956 mW.

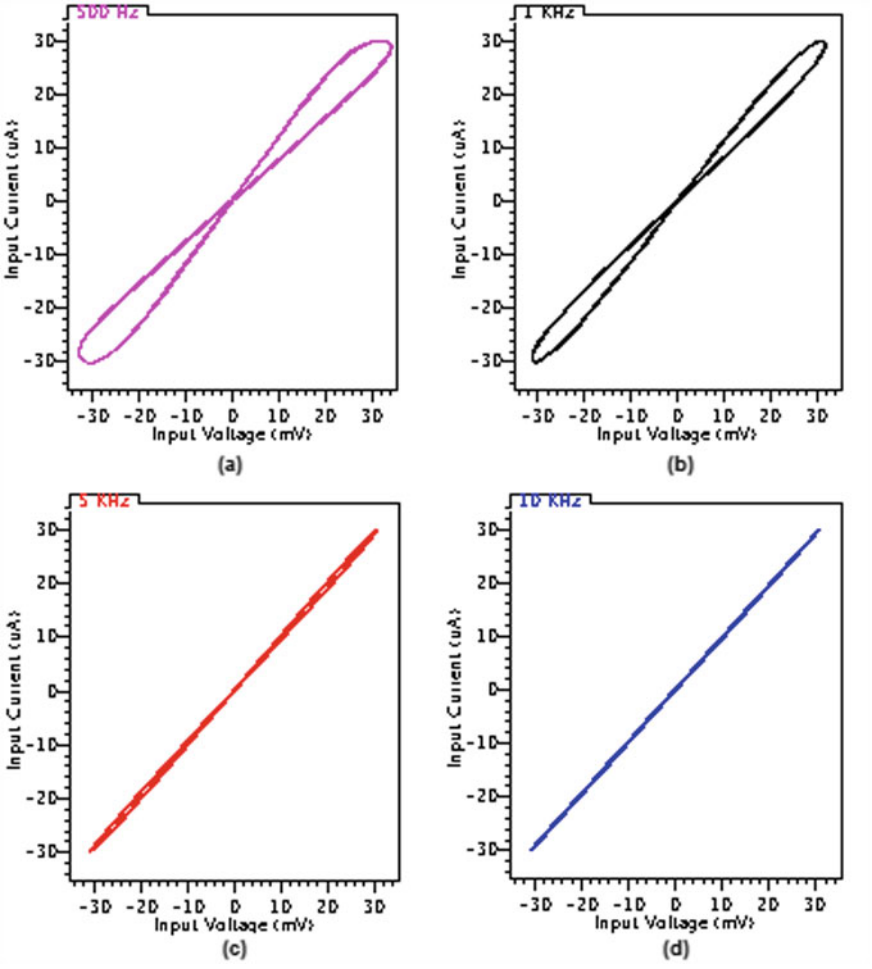

Fig. 4 Characteristic pinched hysteresis loop *I*–*V* plot of the presented memristor for sinusoidal input at amplitude 50 μA and frequency **a** 500 Hz **b** 1 kHz **c** 5 kHz and **d** 10 kHz

The controllability of bias current (I_{BIAS}) on the transconductance (g_{m}) is used for tuning the memductance presented by the presented memristor emulator. In accordance with (12), the memductance gradually increases/decreases with the increase in bias current. This tunable nature of the proposed memristor emulator circuit is advantageous for integrated circuit applications. Further, the change in memconductance when a train of pulse is applied across the presented memristor emulator circuits showing its incremental and decremental operations is shown in Fig. 5a–b, respectively.

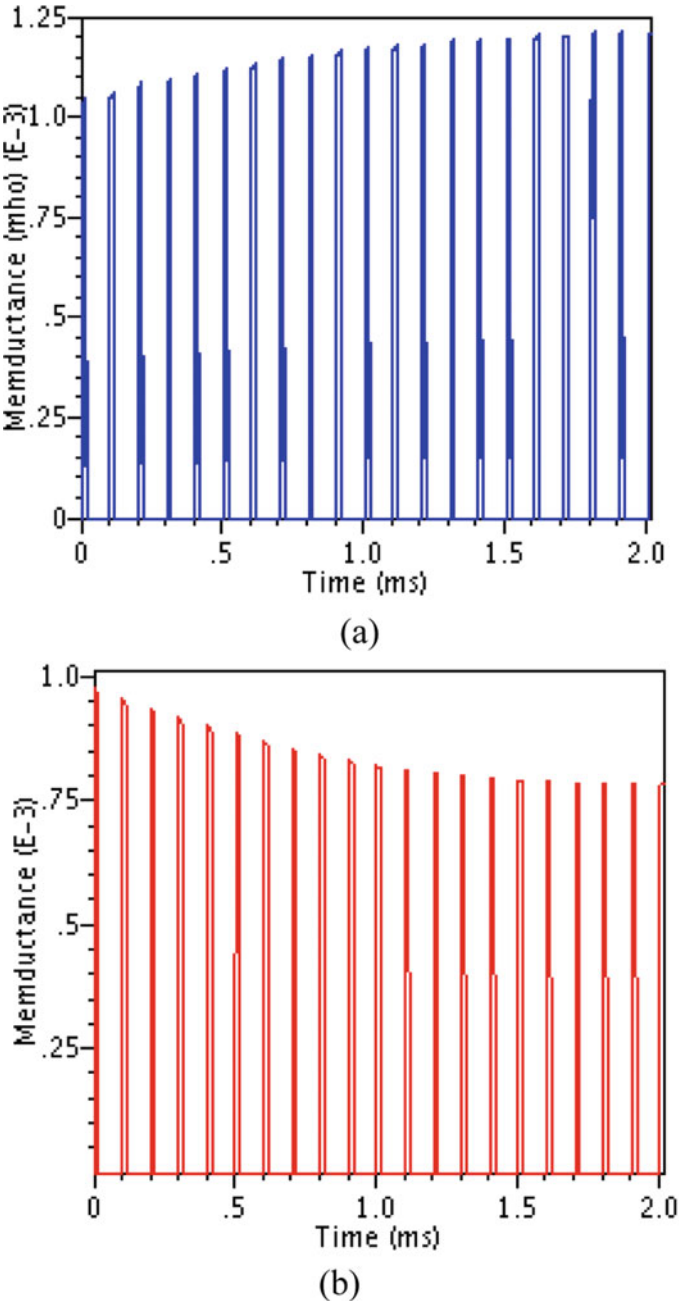

Fig. 5 Change in memconductance when a train of pulse is applied across the presented memristor emulator circuits **a** incremental **b** decremental memristor

5 Conclusion

A VDTA-based fully integrated grounded memristor emulator circuit is presented and designed using one VDTA, one four quadrant analog multiplier, two grounded passive elements, i.e., one capacitor, one resistor, and one inverting/non-inverting buffer. The presented emulator has simple circuit topology, fully integrated configuration, and low power consumption. The simulations presented here support the theoretical derivations, thereby making it a robust and versatile emulator. Further, the tunability via varying the bias current overcomes the process mismatches that occur during fabrication.

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