Lecture Notes in Electrical Engineering 664

Afzal Sikander · Dulal Acharjee · Chandan Kumar Chanda · Pranab Kumar Mondal · Piyush Verma *Editors*

Energy Systems, Drives and Automations

Proceedings of ESDA 2019

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Editors
Afzal Sikander
Department of Instrumentation
and Control Engineering
Dr. B. R. Ambedkar National
Institute of Technology
Jalandhar, Punjab, India

Chandan Kumar Chanda
Department of Electrical Engineering
Indian Institute of Engineering
Science and Technology, Shibpur
Howrah, West Bengal, India

Piyush Verma
International Energy Research Centre
Cork, Ireland

Dulal Acharjee
Applied Computer Technology
Kolkata, West Bengal, India

Pranab Kumar Mondal
Department of Mechanical Engineering
Indian Institute of Technology Guwahati
Guwahati, Assam, India

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Preface

This proceeding book is composed with most of the papers of '2nd International Conference on Energy Systems, Drives and Automations' held during 28 and 29 of December 2019 in Kolkata, India. As the theme of the conference is diverse, most of the papers are from electrical, mechanical, computer, electronics and biotechnology subjects with modern and latest concepts.

Many senior professors, scientists and their research scholars have contributed different chapters for this book, and some of them are—Prof. Jerzy Szymanski (Kazimierz Pulaski University of Technology and Humanities, Radom, Poland); Prof. Chandan Kumar Chanda (IIEST, Howrah, India); Prof. Pradip Kumar Sadhu (IIT (ISM) Dhanbad, India); Prof. Kamrul Alam Khan (Jagannath University, Dhaka, Bangladesh); Prof. Madan Mohan Tripathi (Delhi Technological University, India); Pranab Kumar Mondal (IIT Guwahati, Assam, India); Prof. Krishna Lal Baishnab and Prof. Koushik Guha (NIT Silchar, Assam); Prof. Aminul Islam (BIT Mesra, Jharkhand); Prof. Rajendra Prasad (IIT Roorkee); Prof. Dip Prakash Samajdar(IIIT Jabalpur, Madhya Pradesh); Prof. Navneet Gupta (BIT Pilani, Rajasthan); and many more.

About Edition In this book, about 68 chapters are included as research papers, tutorials, survey papers and report of science engineering projects of renewable energy, green bioenergy, solar cells and its applications in different projects, electrical appliances and its improvements, household electronics and applications, electrical drives, automation and control using software, power transmission through grids, network design for load balancing, high-speed compressor, operational amplifier design, etc., which are the main themes of maximum papers. Another group of papers are from medical instrumentations, signal processing and analysis using electroencephalogram (EEG), electrocardiogram (ECG), sequences of DNA analysis, etc., technology-based emotion control, habitat monitoring, etc.

About Papers Most of the papers are outcome of research work of Ph.D. students and their guides. There are many papers on low-powered circuits and devices such as memresistor, sensors, silicon gate, FET, MOSFET and high electron mobility-based transistors. Many papers are under microelectronics of nanotechnology-based, nanomaterials and its characteristics at different

compositions, carbon nanotubes, design and characteristic study of different diodes and transistors. Many papers are on antenna design and testing for generation of different bands of signals.

Group of papers are under neural network, tutorial, applications of feed forward and feedback technology, fuzzy systems, etc.

This book also includes some papers on habitat monitoring at drunk conditions of driver, unmanned vehicle control through wireless signal, application of pressure sensors in underground mines for monitoring probable damage, image processing, image and signal processing and coding, cryptocurrency and coding, etc.

All the editors have written chapters for this book and have given their valuable feedback and comments to improve the quality of this book. The editors are thankful to all the authors and especially to the research scholars and master degree students who have burnt their energy to compile this book. We thank all the editors, authors, experts and reviewers.

Jalandhar, India — Dr. Afzal Sikander
Kolkata, India — Prof. Dulal Acharjee
Howrah, India — Prof. Chandan Kumar Chanda
Guwahati, India — Dr. Pranab Kumar Mondal
Cork, Ireland — Dr. Piyush Verma

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About the Editors

Dr. Afzal Sikander is working as Assistant Professor with the Department of Instrumentation and Control Engineering, Dr. B. R. Ambedkar National Institute of Technology, Jalandhar, India. He has earned Ph.D. degree from the Department of Electrical Engineering, Indian Institute of Technology Roorkee, India with specialisation in Control Engineering. Dr. Afzal has over 10 years of teaching and research experience in the diverse field of Control Engineering. His areas of interest include Control Theory and Applications, Model Order Reduction, Machine Learning, Optimisation, Robotics and Renewable Energy. He is actively involved in various research projects funded by CSIR, ISRO, TEQIP, etc. He has published 48 research articles in reputed National/International journals and conferences including 17 research papers in SCI-indexed journals. He is a member of the Editorial Board and Guest Editor of numerous reputed Journals. He has organised three International conferences on recent trends in Electrical Engineering and Soft Computing in 2017 and 2018.

Prof. Dulal Acharjee is working as Director in Applied Computer Technology, Kolkata, India. Before, he worked as a Professor in the Department of CSE & IT of Purushottam Institute of Engineering and Technology, Rourkela, Odisha. He also worked as visiting Faculty in Maulana Abul Kalam Azad University of Technology, Kolkata. He received M.Tech. degree in Information Technology from Tezpur University. Before, he did M.Sc. in Applied Physics and Electronics from Dhaka University. He has long experience of working in Software training and development industry. His research interest is automated activity recognition system, sensor based applications, Microprocessor and Microcontroller based embedded systems etc. He has 80 numbers of publications, 15 in international journals, 2 book chapters and others in different National/International Conferences. He has delivered 16 invited talks in international conferences. He has organized about 20 international conferences as General Chair/Chairman in organising

committee. He is an editorial board member of international journal of 'Microsystem Technologies' of Springer-Nature, a SCI indexed journal. He is Guest Editor of many special Issues of this Journal.

Dr. Chandan Kumar Chanda is working as a Professor with the Department of Electrical Engineering, IIEST, Shibpur, India. He has earned Ph.D. degree from the Department of Electrical Engineering, B.E. College (DU), Shibpur, India with specialization in Power Systems. Dr. C. K. Chanda has over 30 years of teaching and research experience in the diverse field of Power Systems Engineering. His areas of interest include Smart Grid, Resiliency, Stability and Renewable Energy. He is actively involved in various research projects funded by Centrally Funded Organizations like DST, UGC. He has published 135 research articles in reputed National/International journals and conferences including 28 research papers in SCI-indexed journals. He is a member of the Editorial Board and Guest Editor of numerous reputed Journals. He has authored and co authored many books in reputed publishing houses.

Dr. Pranab Kumar Mondal is an Assistant Professor in the Department of Mechanical Engineering at Indian Institute of Technology Guwahati since May 2015. He received his undergraduate and postgraduate degree from Jadavpur University, Kolkata, and completed his Ph.D. from Indian Institute of Technology Kharagpur in 2015. His principal research interest, encompassing the broad area of Microfluidics, has covered various facets of micro scale multiphase transport, electro kinetics and micro scale transport of heat. He is currently working on stability analysis of flows with free-surfaces, capillary filling of bio-fluids. He has co-authored more than 65 referred journals conference publications.

Dr. Piyush Verma works as Senior Energy Policy Analyst at the International Energy Research Centre in Ireland where he leads the policy and regulatory innovation work. He works on the intersection of technology, policy, society, and the environment, and has significant experience researching, developing and implementing energy transition policies in India, Vanuatu, New Zealand and Ireland. He has been selected as World Energy Council's Global Future Energy Leader where he actively contributes to shape the policy agenda of frontier technologies. He also works as the Vice-Chair of Group of Experts on Energy Efficiency at the United Nations Economic Commission for Europe in Geneva. He is an Electrical Engineer, a postgraduate in Power Systems, and has a PhD in Energy Efficiency Technology and Policy from The University of Auckland, New Zealand. He has also completed a programme on 'Public Policy Challenges of the 21st Century' from the University of Virginia, USA.

Mitigation Methods of Ground Leakage Current Caused by Common-Mode in Voltage Frequency Drives

Jerzy Szymanski, Marta Zurek-Mortka, Pradip Kumar Sadhu, and Anik Goswami

Abstract Three-phase PWM (Pulse Width Modulation) inverters generate parasitic Differential-Mode Voltages (DMV) and Common-Mode Voltages (CMV). Parasitic voltages are a side inherent effect of using the PWM to shape the phase-to-phase inverter voltage. In this article, authors present a method for filtration of high-frequency harmonics of DM and CM voltages aimed at limiting the parasitic currents: DM voltage—phase-to-phase parasitic current and CM voltage—ground parasitic current. As the final result of the tests, almost complete elimination of leakage parasitic current form PE shock protection system was achieved. To build circuit which allows eliminate capacitance leakage current the earth protection system the two different kinds of double screened cables to supply inverter and motor were used.

Keywords Common-mode voltage · Differential-mode voltage · PWM modulation · Three-phase voltage inverter · Two-level PWM inverter · Screened cable

1 Introduction

Ground current of high-frequency disturbances is caused by the common-mode voltage of the inverter. The basic harmonic of this voltage has the frequency resulting

J. Szymanski (✉) · M. Zurek-Mortka
Faculty of Transport, Electrical Engineering and Computer Science, Kazmierz Pulaski University of Technology and Humanities, Radom, Poland
e-mail: j.szymanski@uthrad.pl

M. Zurek-Mortka
e-mail: m.zurek-mortka@uthrad.pl

P. K. Sadhu · A. Goswami
Department of Electrical Engineering, Indian Institute of Technology, Dhanbad, Dhanbad 826004, India
e-mail: pradip@iitism.ac.in

A. Goswami
e-mail: anik.goswami52@gmail.com

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from the switching frequency of the inverter semiconductor valves. In industrial applications, the capacitive ground leakage current forced by the CM voltage of the inverter flows to the transformer in the TN (ground-neutral) system through a grounded star connection of the secondary windings.

In IT (isolation-ground) system (or High Resistance Grounded network—HGR) of the industrial power supply system, the ground leakage current flows through the parasitic capacitances between the ground and the ungrounded star connection of the transformer secondary windings. In an industrial power system with an IT transformer network type, the CM voltage of the inverter, which is deposited on the parasitic capacitances between the ground and the ungrounded star connection of the transformer secondary windings causes high-frequency disturbances of voltages in transformer. In that case, the inverter CM voltage adds to the phase voltages of the transformer.

Two-level voltage PWM inverters are commonly used for supplying three-phase induction motors in industrial low voltage networks and also for traction motors in the DC and AC railway traction. Lack of effective methods for reducing the negative impact of parasitic CM and DM voltages is the cause for increased risk of fault to loads powered from a common transformer [1–4]. In addition, there is a risk of electric shock related to the leakage current caused by the CM voltage in inverters. During the operation of motors in a potentially explosive zone, the ground leakage current can cause sparking, provoking an explosion even if the motor's rotor speed is near zero.

The literature describes the cases of damage to converters due to leakage currents caused by the CM and DM voltages [2]. A variety of methods have been proposed in literature [4–8] to address the CM and DM noise problem and its related issues. The exact CM and DM equivalent circuits of PWM inverter in drive systems derived by taking the rectifier into account was presented in [9]. Besides, an improved LC filter using in transformer-less three-level photovoltaic inverter system for leakage current suppression was presented in [10]. The minimization of current harmonics in an alternating voltage grid is discussed in the literature [11, 12].

This paper is organized as follows: the first part is about the analytical description of CM and DM voltages of the inverter. The next part is about the studies on the CM and DM voltage of the inverter using simulation methods and verified then by the experimental results. In the final part of the article, a power supply system for the industrial drive voltage frequency converters (VFC) was proposed, in which high-frequency disturbance currents created as a result of CM and DM voltage were eliminated from drive system.

2 Analytical Description of Differential-Mode and Common-Mode Voltages of PWM Inverter

Voltage shaping in the PWM inverter has its side effects in the form of undesirable harmonics distortion of high orders, which are referred to as DM voltage—inter-phase voltage disturbance and CM voltage—defined as the sum of phase voltages divided by 3. CM voltage is, among other things, the cause of motor bearing currents [9, 13]. Based on the two-level PWM inverter model, analytical relationships describing these disturbances were derived. The inverter model is shown in Fig. 1.

The harmonic analysis of inverter voltages for sinusoidal PWM modulation enabling the determination of analytical equations describing CM voltage u_{CM} of PWM inverter is described. The expression of the inverter phase voltages is shown in Eq. (1) [2, 14]. The phase voltages are determined in relation to the neutral point G (Fig. 1), for individual phases of the inverter and can be expressed in the form of infinite harmonic series [15, 16].

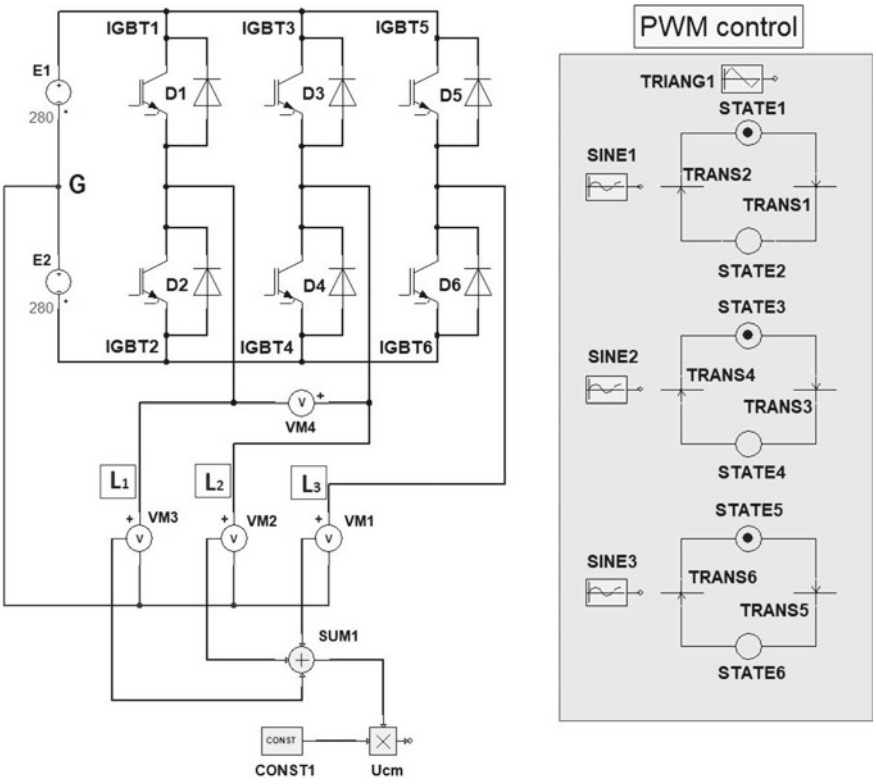

Fig. 1 Model of PWM inverter circuit: VM_1, VM_2, VM_3—phase voltage, VM_4—phase-to-phase voltage and u_{CM}—CM voltage

The inverter CM voltage u_{CM} as Fourier function takes the form [15, 16] (1):

$$u_{\mathrm{CM}} = \frac{2U_d}{3\pi} \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ n \neq 0}}^{\infty} \frac{1}{m} J_n\left(m\frac{\pi}{2}M\right) \sin\left((m+n)\frac{\pi}{2}\right) \left(1 + 2\cos\left(n\frac{2\pi}{3}\right)\right) \cos(m\omega_{\mathrm{c}}t + n\omega_0 t) \tag{1}$$

where

$J_n(x)$—Bessel function of the n-th order with the argument x,
M—PWM modulation factor,
M—index of row of harmonic carrier frequency f_{c},
N—index of row of harmonic frequency modulating of inverter f_0,
ω_0—frequency of the fundamental (modulating) harmonic,
ω_{c}—frequency of the carrier waveform (modulated) of PWM modulation.

Then, the inverter DM voltages for the individual pairs of the inverter voltage phases are described by Holmes and Lipo [15], Kempski [16] (2):

$$u_{\mathrm{DM}} = \frac{4U_d}{\sqrt{3}\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{m} J_m\left(m\frac{\pi}{2}M\right) \cdot \sin\left((m+n)\frac{\pi}{2}\right) \sin\left(n\frac{\pi}{3}\right) \cos(m\omega_{\mathrm{c}}t + n\omega_0 t) \tag{2}$$

To explain the formation of CM and DM voltage of PWM inverter, a model of three-phase two-level voltage inverter shown in Fig. 1 is used. There is an electrical scheme of a two-level three-phase inverter, which allows time and frequency analysis of inverter voltages for freely adopted PWM modulation parameters.

As a result of the simulation, the CM voltages for basic harmonic of phase voltage equal to 50 Hz were obtained, with two different modulation factors: $M = 0.9$ and $M = 0.1$ (Fig. 2).

The effective value of the CM voltage u_{CM} is determined with respect to half of the DC voltage supply of the inverter $1/2U_d$. For $M = 1$, the effective value of the inverter CM voltage is $1/4U_d$, and for M which is close to zero, it is $1/2U_d$.

A characteristic feature of the inverter CM voltage u_{CM} is the square shape with frequency f_{c} when the modulation factor M is close to zero (Fig. 2b), i.e. during the generation of basic harmonics of inverter phase-to-phase voltages with the effective values close to zero (Fig. 2d).

The inverter CM voltage u_{CM}, for M close to zero, is a rectangular waveform with the frequency f_{c} (Fig. 2c). This creates a danger for human electroshock due to the presence of high-frequency CM voltage with an effective value being 100% higher than when the inverter is operating with a modulation factor equal to $M = 1$ (Fig. 2a). With the occurrence of a rectangular waveform of inverter CM voltage at $M = 0$, its

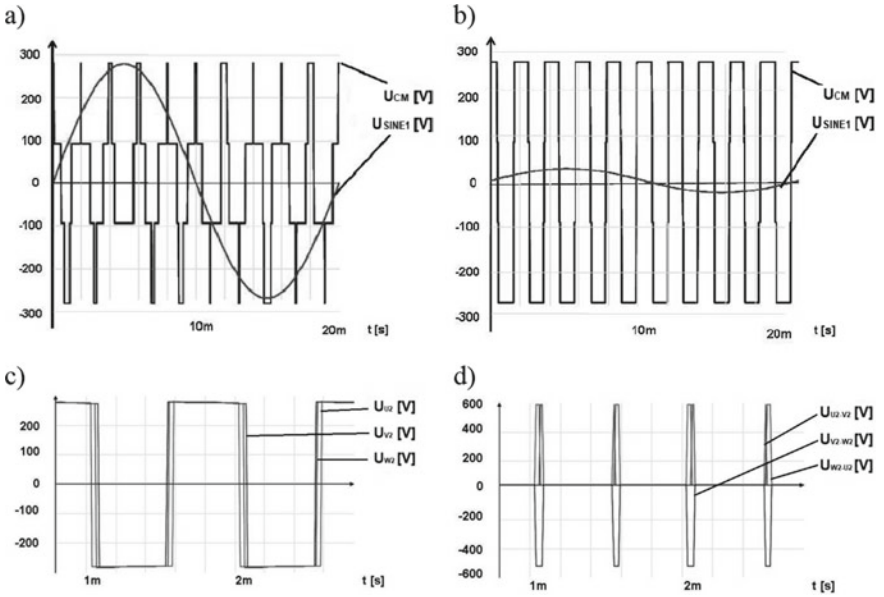

Fig. 2 The inverter CM voltage u_{CM} with sinusoidal modulation method of output voltages and inverter phase and phase-to-phase voltages ($f_{h1} = 50$ Hz, $f_c = 0.5$ kHz (TRIANG1): **a** the CM voltage u_{CM} and 1-harmonic of phase output voltage of the inverter at the modulation factor $M = 0.9$, **b** the CM voltage u_{CM} and 1-harmonic of phase output voltage of the inverter at the modulation factor $M = 0.1$, **c** inverter phase voltages for $M = 0.1$, **d** phase-to-phase voltages for $M = 0.1$

amplitude spectrum will consist only of the odd harmonics. The harmonics h_k have only odd rows: $k = 1, 3, 5, 7, 9 \ldots = 2n - 1$.

3 Simulation and Experimental Research of the Influence of CM Voltage on Ground Leakage Current

The scheme of power supply network with TN transformer configuration of inverter drives is shown in Fig. 3. It is a drive system model with a voltage frequency converter and a squirrel cage motor, where u_{CM} and parasitic current i_{CM} are pointed out. The motor is connected to the voltage inverter of the frequency converter with a three-phase screened motor cable. In the drive model shown in Fig. 3, the parasitic ground leakage current flows through the ground capacitance of the cable and motor, flowing into the inverter through two circuits: through the EMC ground filter of the intermediate circuit and through the transformer secondary windings working in TN power supply system. The capacitance of the intermediate circuit EMC filter has a small value, typically 0.22–0.35 μF, so a significant part of this current flows through the secondary windings of the transformer. Capacitive ground leakage current measured

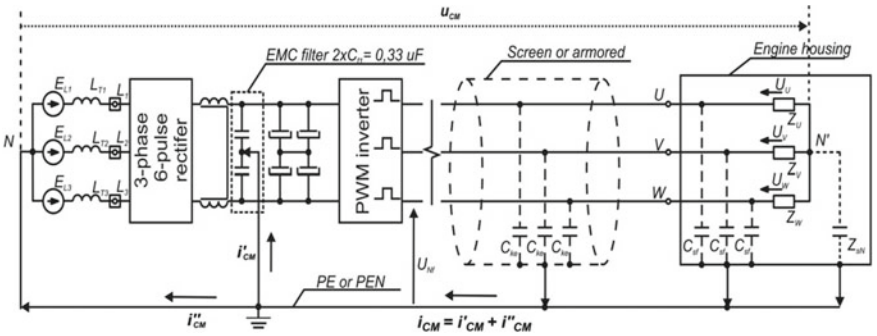

Fig. 3 The model of the drive system with the frequency converter and the parasitic ground capacitances of the screened cable and motor

in the protective PE conductor on the stretch between the transformer and the EMC filter of the drive frequency converter, caused by the inverter CM voltage u_{CM}, is shown in Fig. 3.

Figure 3 shows that despite the use of an EMC filter built in the drive frequency converter, a significant part of the ground leakage current (i''_{CM}) is flowing through the transformer secondary windings with the TN power network system causing undesirable deformations of the transformer voltages at the common point connection (PCC) of other loads. The inverter's switching frequency has a fundamental harmonic of the inverter CM voltage, e.g. 4 kHz. The parasitic CM voltage contains harmonics, which are placed around a multiple of the switching frequency (4 kHz) [17].

4 Methods of Limiting Parasitic Ground Leakage Currents Generated by Inverter

For high power drives with frequency converter, the authors propose supplying the drive from an IT network system (or High Resistance Grounded HRG network). The IT type system eliminates the galvanic shorting of the transformer windings with ground, and thus the ground current is limited and flows only through the parasitic ground capacitance on the secondary side of the transformer supplying the frequency converter. The ground leakage current from the transformer can be completely eliminated by using an external additional capacitive filter. It is possible to connect an additional circuit in which the ground leakage current flowing to the inverter is bypassing the transformer, Fig. 4a.

For the complete elimination of ground leakage currents from the PE (protective earth) wire and the transformer and to eliminate the DM voltage from the motor phase-to-phase voltages, the power supply system shown in Fig. 4b may be used.

The use of DM and CM filters together with an alternative ground leakage current circuit that bypasses the PE wire enables the use of unscreened motor cables without

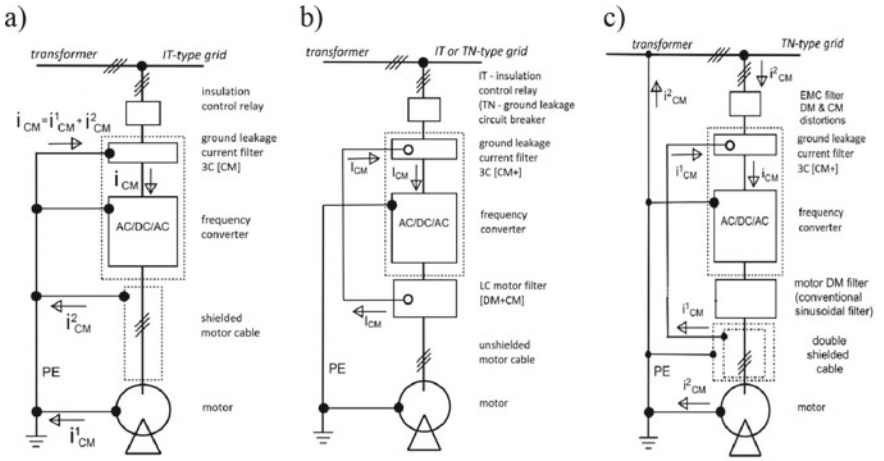

Fig. 4 Power system of the motor drive with frequency converter, where I_{CM} is the capacitive leakage current due to the CM voltage of the inverter: **a** with capacitive filter, **b** with patented DM + CM filter, **c** with double insulated screens motor cable [14]

length restrictions since in this case the motor phase voltages and phase-to-phase voltages are purely sinusoidal.

Figure 5a, b presents the results of experimental tests of ground leakage current measured in a PE wire using the motor power system solution according to Fig. 4a, b. Figure 5a indicates a significant effective value (0.5 A) of capacitive leakage current I_{CM} in PE wire using the motor power supply system according to Fig. 4a. Figure 5b proves the possibility of the complete elimination of capacitive leakage current I_{CM} from the PE wire using the power supply system according to Fig. 4b.

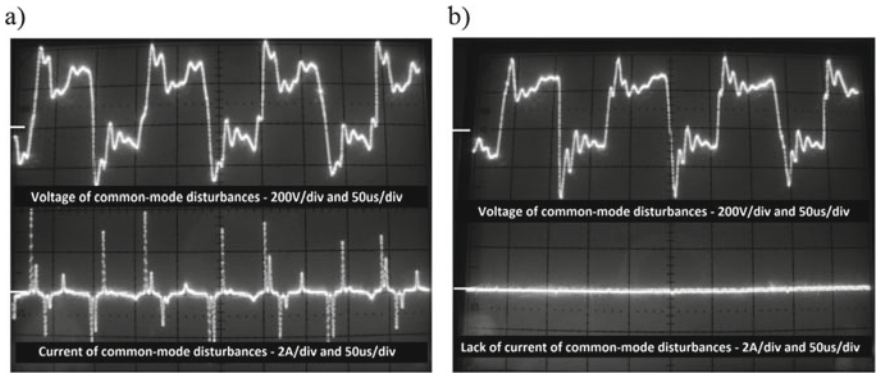

Fig. 5 The CM voltage u_{CM} of the frequency converter and ground leakage current I_{CM} in the PE wire: **a** using the CM filter (3C capacitive filter) in power system as presented on Fig. 4, **c** using a DM and CM filter of inverter disturbance voltages in power system as presented on Fig. 4b

Using double insulated screens power cables, it is possible to create a circuit for high-frequency grounding currents outside a PE wire in TN type network. Drive VFC power supply system with only motor leakage current in the PE wire is presented in Fig. 4c. Typically motor leakage current i^2_{CM} is much less than motor cable leakage current i^1_{CM}. Total leakage current i_{CM} is a sum of i^1_{CM} and i^2_{CM}. It is the right solution for a rather small power drive VFC, because for big power drives the cost and weight of the LC (DM) filters (sinusoidal filters) are high.

For a big power drive typically the motor LC filter is not used and in this situation, motor ground leakage current occurs in PE wire. A ground motor stray capacitance (between stator wires and grounded motor chassis) is usually much smaller than a ground stray capacitance of a screened motor cable and as a result current in PE wire depends mainly on cable ground stray capacitances, Fig. 4a.

Connection example with two double screened, insulated each other power cable, used in drive system is presented in Fig. 6b. Here one cable type is used to supply voltage frequency converter from transformer and the second type is used to feed a motor from frequency converter.

In IT (Insulated Terra) transformer configuration can be necessary to receive a bigger ground stray capacitance at input terminals of drive VFC against the motor cable ground stray capacitance—in this case, at the same cables length, it is possible using the different type of these cables. For example:

- as a cable feeding a drive VFC from transformer, 4 × 50 mm, a cable type TOPFLEX EMC–UV-2YSLCYK (producer Helukabel) with 320 nF/km stray capacitances between each wire and screen,

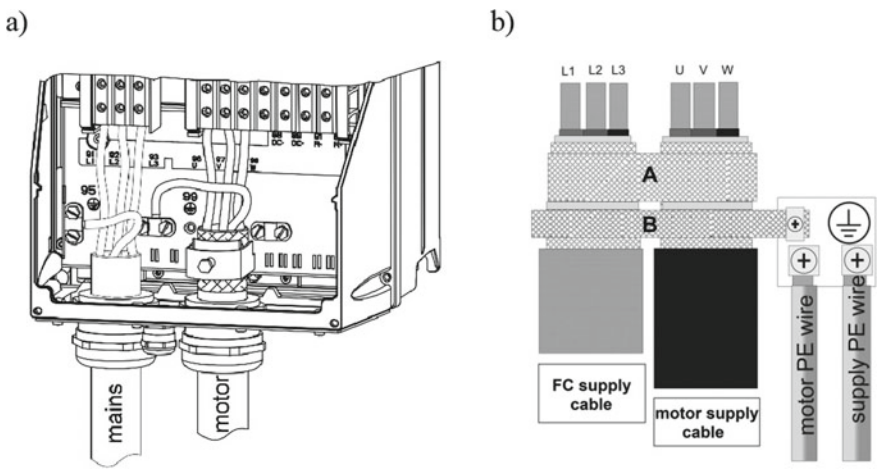

Fig. 6 Power cables screen connections at the drive VFC power terminals: **a** traditional connection with unscreened power supply cable and screened motor cable, **b** new concept of connection with two double, insulated each other screened cables: A—internal screens connected together but not to the PE system, B—external screens connected together and to PE system

- as a motor cable, (means cable between a VFI and motor), 3 × 50 mm + 3G10, a cable TOPFLEX EMC–UV-3PLUS 2YSLCY-J (producer Helukabel) with 32 nF/km stray capacitances between each wire and screen [18].

In this case of power cables application in the drive VFD system, a ground stray capacitance on the drive VFD inputs (works as current filter 3C[CM]) will be 10 times bigger than a ground stray capacitance on the motor terminals—screened motor cable, Fig. 4c.

5 Conclusion

In the absence of effective filtration of ground disturbance currents, which are caused by the PWM inverter CM voltage capacitive leakage currents causing high-frequency disturbances of phase and phase-to-phase voltages. The PWM inverters produce two types of voltage causing disturbances:

- differential-mode voltage (disturbance of phase-to-phase voltages),
- common-mode voltage (disturbance of the phase voltages causing the high-frequency flow of the capacitive leakage current, e.g. transformer).

The DM voltage does not present serious problems for the operation of motors because the content of higher harmonics at phase-to-phase voltages is greatly reduced through the improved PWM control strategies of the inverter for shaping phase-to-phase voltages or usage of sinusoidal LC filters. The steepness of voltage increase is also limited by the already implemented converter soft switching of transistors and does not exceed the voltage increase speed allowed by the 700 V/μs standards (e.g. IEC/EN61000-3-4). The insulation and production technology of motor are improved and there is no visible degradation as a result of rapid changes in the electromagnetic field around the insulation of the stator windings of the motor. The inverter CM voltage still causes negative effects in the drive system. The impact of this voltage is complex and depends on many factors, e.g. the motor power, the motor cable lengths, the types of motor cables: screened—unscreened, the supply system TN/IT, cable trays with motor cables, metal grounded or plastic ungrounded and many others.

With industry drives applications, the phase-to-phase disturbances (DM) and ground disturbances (CM) do not cause operational problems if these are filtered. There are, however, more complicated cases, for example when powering from one transformer in IT power system the multi-motor drive system, with individual high power drive VFC. In untypical cases, it is necessary to conduct a detailed analysis of the possibilities for limiting the negative impact of high-frequency ground disturbances caused by the inverters of VFC. The CM voltage, among others, may cause impermissible deformations of the transformer voltages both in TN and IT power system. Also the damage to the inverter power path, or disrupt data transmission in ICT systems, which are undesirable in control and visualization systems occurs.

Presented method of elimination of high-frequency leakage currents by usage of two kinds of double screened cables in VFC drive system is especially useful for big power drives in which application with standard DM and CM filters are too expensive or impossible to implement.

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Implementation of ANN-Based UPQC to Improve Power Quality of Hybrid Green Energy System

C. H. Siva Kumar and G. Mallesham

Abstract The rapid increase in the contribution of naturally replenished green energy sources to increase the generating capabilities of a modern power system poses a challenging task for engineers to maintain its power quality. The zest of the paper is to address the power quality issues that arose due to the presence of a wind energy system in a hybrid PEMFC and PMSG based wind energy system connected to a weak grid system. In this work, built a mathematical model of a hybrid renewable system consisting of a wind energy system with a permanent magnet synchronous generator, proton exchange membrane fuel cell system and estimated the carbon emission reductions. The work is further focuses on power quality issues aroused in a geographically weather-dependent wind variation impact. As these impacts limit the freedom of utilizing different power sources, it causes a variable voltage and output powers, especially in a weak grid system. To improve the power quality of hybrid weak grid systems modelled and simulated an ANN-based UPQC using MATLAB/Simulink. Simulation results are shown to verify the performance of the compensator to mitigate active power, reactive power fluctuations and voltage fluctuations due to the wind energy system and to mitigate symmetrical sags due to symmetrical loading conditions and swells due to unsymmetrical conditions.

Keywords Hybrid green energy system · Wind energy system · Proton exchange membrane fuel cell

1 Introduction

The annual rise in carbon dioxide around the world is about 1.3% [1]. This growth further increases across the globe as there is a rapid growth in all industrial sectors,

C. H. Siva Kumar (✉) · G. Mallesham
Department of Electrical Engineering, University College of Engineering, Osmania Universtiy, Hyderabad, Telangana 500007, India
e-mail: ch_siva_kumar@rediffmail.com

G. Mallesham
e-mail: drgm@osmania.ac.in

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power sectors, transport systems, etc., which further worsen weather conditions on the globe [2, 3]. Globally, many governments set new policies and their targets at sub-national level for decarbonization, with increasing private sector players in the generation of electrical energy results in growing the market for green renewable energy sources. As per the Renewables 2019 Global Status Report, during the last year, a total significant capacity of 2378 gigawatts (GW) of renewable power was added globally out of which around 28% is wind energy [4]. As the penetration levels of these green renewable energy systems increases to reduce the decolonization in one aspect, in another aspect, it increases the power quality issues in the modern power system. There is another emerging research field in electrical engineering is fuel cell systems. The benefits of using fuel cell-based charging stations are improving profit, fast installation of station, fast and smart charging, easy conversion of hydrogen, reliable, low-maintenance, quiet in operation, [5, 6], etc. The above two situations demand a combined operation of differently characterized green renewable energy resources like wind-fuel cell systems, wind-solar, wind-hydro systems, wind-geothermal, etc. A hybrid renewable energy system is a stand-alone electrical power source consisting of two or more electrical energy sources working together to meet the demand. Working together in a common grid as a hybrid grid, working under these situations is a challenging task for the working engineers to generate, coordinate and controlling of diversified characterized renewable energy systems in a grid, especially weak electrical grid system [7]. The above-mentioned problems come under the category of power quality problems of utility systems. These power quality problems cannot be handled by the utility system on its own. With the recent progress in power electronics devices and applications to electrical power systems for the benefit of end-users called custom power devices. Out of all custom power devices, UPQC has the best features of controlling power quality issues [8].

Many research works proposed different control approaches to extract distorted components like Akagi et al. [9] proposed instantaneous active and reactive power concept, Enhanced PLL based SRF control method [10], hybrid fuzzy back-propagation control scheme [11], a new SRF-based power angle control method [12], etc., for controlling of UPQC for a single power source and grid systems. The complete work of the paper is organized into different sections. The main part of the work is mathematical modelling of hybrid renewable systems: wind energy system with wind turbine and permanent magnet synchronous generator and fuel cell system, modelled a multilayer feedforward-type ANN-based UPQC in Sect. 2. In Sect. 3 discussed in detail about performance analysis of ANN-based UPQC in a weak grid network. Finally concluded the work in Sect. 4.

2 Carbon Emission Reduction Using HRES

The human activities that emit the greenhouse gases are transportation, generation of electricity, industrial, commercial residential and agricultural sectors. It is worth using a hybrid renewable energy system to reduce the percentage of carbon emissions

from the power sector as per Kyoto protocol to limit greenhouse gas emissions [13]. This work is one of the best solutions to reduce greenhouse gas emissions as it is using a hybrid renewable energy system for the production of electrical energy. A total of 21.61 MW of electrical power is produced using HRES which reduces the carbon emission by 21.19941 t [14].

3 Mathematical Modelling of Components Using MATLAB/Simulink

The most promising tool used by the engineers to solve effectively and safely is simulation. To understand the complete behavior of any systems using computer simulation studies needs a mathematical representation of the system. It needs the complete mathematical model-based description with the complete physical properties of a system to study and analyze. It reduces real-time cost, time of operation, flexibility to redesign the system, suggests required modifications and complete insights of any system to study and analyze. To carry this work, MATLAB/Simulink model-based design software is used. The following sub-sections describe the respective mathematical modelling of the components. In this section presented the mathematical modelling of wind turbine, permanent magnet synchronous generator is presented.

3.1 Modelling of Wind Turbine

A mathematical model gives the relationships between various variables. The mathematical expression for power output of a wind turbine (variable speed) and output torque is represented as

$$P_{\mathrm{m}} = \frac{1}{2}\rho A v_{\mathrm{w}}^3 C_{\mathrm{p}}(\lambda, \beta) \tag{1}$$

$$T_{\mathrm{t}} = \frac{1}{2}\rho \pi r^3 C_{\mathrm{p}} V_{\mathrm{d}}^2 \tag{2}$$

where ρ: air density (1.225 kg/m^3), A: swept area (m^2), υ_{w}: wind velocity (m/s) and C_{p}: power coefficient—0.59, V_{d}: disturbed wind speed. The overall output power of a wind turbine is (mechanically): 21.6e6 W and operated with a base wind speed by 14 m/s (fluctuating between 13 and 15 m/s).

3.2 Modelling of Permanent Magnet Synchronous Generator

The recent developments in synchronous generators: permanent magnet synchronous generators (PMSGs). PMSG is increasingly being used as variable speed turbines. As it reduces the cost of slip rings with high conversation efficiency, less maintenance, high reliability and reductions of weight of the nacelle. The dynamics of the machine referred [15–17].

The mathematical expression for torque is represented with the following notations: L_q and L_d are generator quadrature and direct axis inductances, R_s is the resistance, ω generator speed.

$$T_e = \frac{3}{2} p\left[\left(L_d - L_q\right) i_{sq} i_{sd} - \lambda_m i_{sq}\right] \tag{3}$$

3.3 Electrical Weak Grid System

One of the factors on which the manufacturers of wind tribunes depend tolerances on Short Circuit Ratio. It determines the stiffness of the gird. If the SCR below 2.5 is treated as a weak grid and on the other hand, it is considered as a strong grid its SCR value is greater than 20. A weak grid is sensitive to voltage fluctuations and to reactive power and a strong grid has the capability to maintain the reactive power variations due to voltage fluctuations. The *r*-value of the system considered is 5.5 [18].

3.4 Modelling of Proton Exchange Membrane Fuel Cell

The electrochemical technology of fuel cells has salient features like fuel flexibility, property of portability, noise-free operation, quick start-up, high power density and operates at relatively low temperatures. These features made a strong comeback of this technology for the generation of power in distributed power generation sectors. For the continuous operation of fuel cells, fuel is supplied continuously to anode and the corresponding reactant at cathode. Polymer membrane which conducts protons through it is used as an electrolyte. V-I characteristics of PEMFC are shown in Fig. 1 the following is the chemical reactions that take place in PEMFC [19, 20]:

$$\text{anode equation} : H_2 \rightarrow H^+ + 2e^- \tag{4}$$

$$\text{cathode equation} : 1/2\ O_2 + 2H + 2e^- \rightarrow H_2O \tag{5}$$

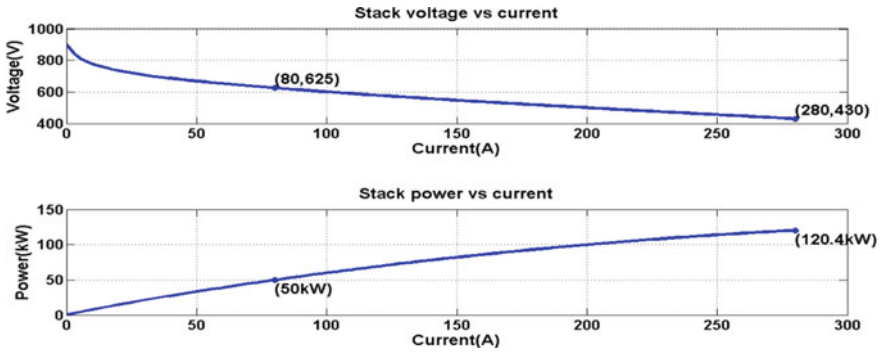

Fig. 1 V-I characteristics of PEMFC fuel cell

3.5 Modelling of ANN-Based UPQC

In the present scenario, power quality issue is one of the major issues in the electrical power distribution system to maintain the system parameters within the international standards like IEEE Standard 519-1992 (1992); IEEE Standard 1547-2003 (2003), etc. Custom power devices are the solutions to handle and control power quality issues at the distribution level. In this work a custom power device is called UPQC is modelled using the ANN control technique. A UPQC consists of three major parts: series: shunt and a common DC source: DC link [21]. Different power theories and techniques for UPQC have been used by the researchers are discussed in the introduction.

Combined intelligence of human intelligence, applications of machine processes and computer system: Artificial intelligence has become a part of design, analysis, processing, planning and controlling. With the introduction of these systems, reducing human errors fastens the best solutions to single and multiple objectives, solutions to non-linear systems, etc. have made a significant transformation in all fields of engineering and non-engineering sectors. In this work, a sub-area of Artificial intelligence: ANN technique is basically derived from the human nervous system: neurons in the brain. In this work an ANN-based UPQC (*p-q* theory) is built to improve the power quality of a hybrid green energy system with the following parameters: ANN: No. of layers hidden layers: 3, No. of epochs: 500, No. of inputs: 1 and outputs: 1 of the error voltage of PCC and DC link voltage. Training control scheme used is Gradient descent back-propagation with adaptive learning algorithm, which has the highest performance and quick convergence than back-propagation algorithms. The MATLAB/Simulink model of ANN shunt controller is shown in Fig. 2.

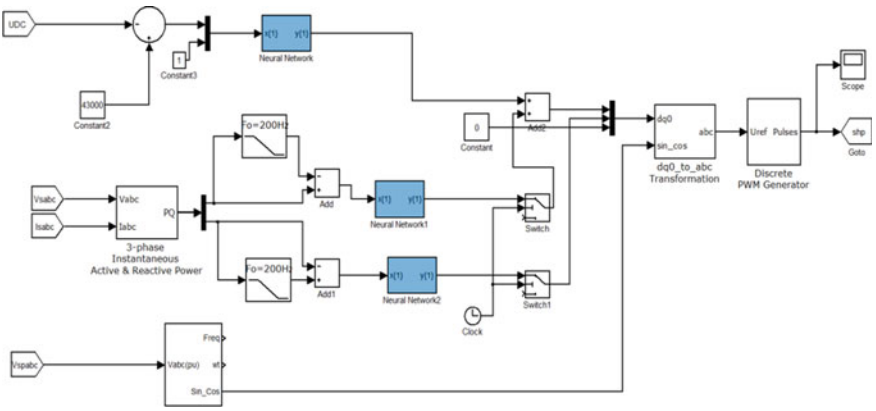

Fig. 2 ANN shunt controller block diagram

4 Performance and Analysis of ANN-Based UPQC

Built a hybrid network shown in Fig. 3 using MATLAB/Simulink to study the performance and analysis of ANN-based UPQC [22]. The network consists of a weak grid with a voltage level of 33 kV, a 21.6 MW PMSG based wind energy system, a 100-kW rated PEMFC. The notation i^{th} and j^{th} is used to represent the impedance Z between the nodes Z_{ij}. An ANN-based UPQC placed in the network at BB6. To study the performance of the built ANN-based UPQC the following case studies have been carried.

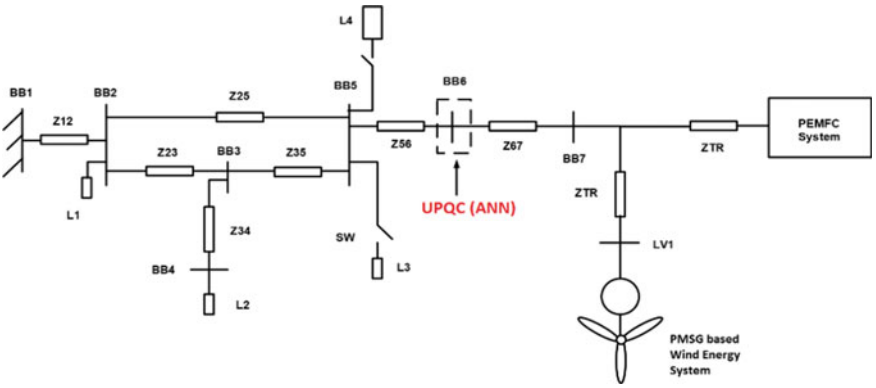

Fig. 3 Hybrid green energy system connected to weak grid

4.1 Simulation Case Study 1: Fluctuating Wind and Balanced Sags

The simulation is carried for a time period of 6 s with different balanced loading L_1: 15 MW + j 6.31 MVAr, L_2: 12 MW − j 2.4 MVAr, L_3: 9.2 MW + j 1.85 MVAr and L_4: 20 MW + j 15 MVAr, respectively, at 3.6, 4.2, 4.6 and 5.2 s, respectively. Figure 4a–c clearly demonstrates the active and reactive power fluctuations due to fluctuating wind and its impacts at grid, wind energy system and fuel cell system (without using UPQC). Figure 5a–c clearly demonstrates the active and reactive power fluctuations exits till 2.5 s so, then on-wards there are no active and reactive power fluctuations. These active power and reactive power fluctuations resulted due

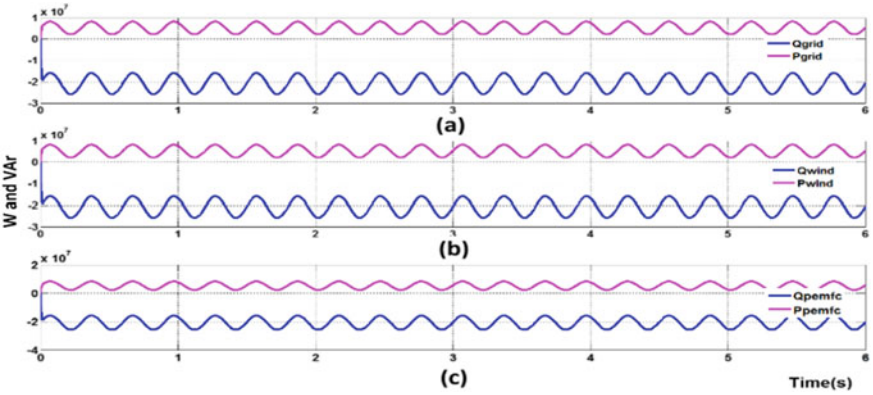

Fig. 4 Without UPQC: active and reactive powers: **a** P and Q at grid, **b** P and Q at PMSG based wind energy system, **c** P and Q at PEMFC

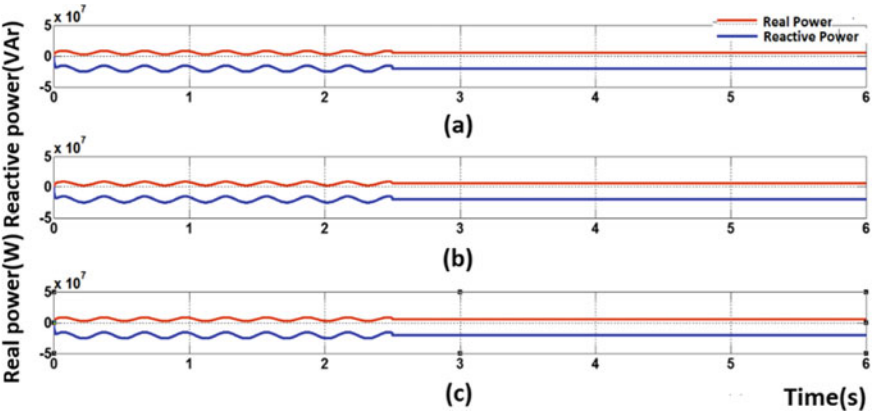

Fig. 5 With UPQC: active and reactive powers: **a** P and Q at grid, **b** P and Q at PMSG based wind energy system, **c** P and Q at PEMFC

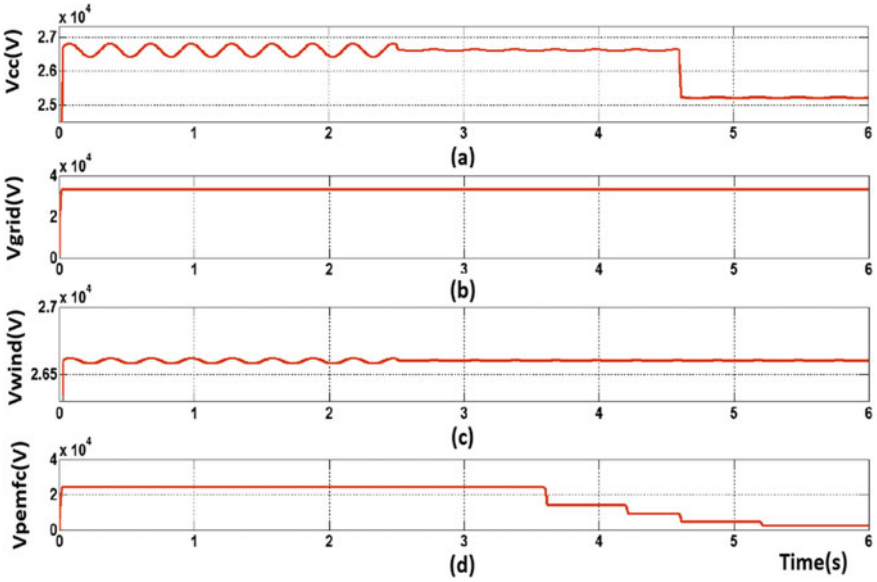

Fig. 6 Terminal voltages at: **a** point of common connection (PCC), **b** grid, **c** PMSG based wind energy system and **d** PEMFC system

to torque variations in wind turbine Eq. (2). At time 2.5 s both the series and shunt controllers of ANN-based UPQC is put into operation. The simulation results shown in Figs. 5 and 6 are the evidence of improvement of power quality using modelled an ANN-based UPQC. In Fig. 5a–c clearly demonstrated that after 2.5 s the controller put into operation results in nullyfying the power fluctuations in grid, wind and fuel cell systems. In Fig. 6a–d represented the terminal voltage at the point of common connection, grid, wind energy system and fuel cell system for the entire simulation period. As it is clearly demonstrated in Fig. 6c the voltage fluctuations are existing till 2.5 s, i.e. before the complete UPQC put into operation. And carried the analysis and it is found that these fluctuations are with IEC 61000-4-15.

4.2 Simulation Case Study 1: Unbalanced Swells Due to Unsymmetrical Conditions

Another important power quality aspect that generally the power system subjected to is: Voltage swell is quite opposite to sag: increasing the voltage more than one cycle and less than a few seconds. This power quality issue arises due to: sudden change in the reference of the ground, raise in un-faulted phases, large loads de-energization, insulation failure, damage to the very sensitive loads, etc. To analyze the compensator under these conditions built a system with different unsymmetrical conditions. This

case study is also carried for the simulation time period of 6 s. Initially loaded the system with balanced loads of 15 MW + j 6.31 and 12 MW − j 2.4 MVAr same that of the case 1. The following unsymmetrical conditions are created to analyze ANN-based UPQC. Faults are created on LV side of 630 kVA, 33 kV/690 V. 1. 4.6 to 4.8 s: 3-phase fault with R_f—0.001 Ω ground resistance: R_g 0.001 Ω 2. 5.2 to 5.4 s: L-L fault with 9 ohms resistance ground resistance: 0.001 Ω. 3. 5.6 to 5.8 s: L-G fault with ground resistance: 0.001 Ω.

Figure 7a–c results in different swell conditions on the secondary side of the transformer, the primary voltage is Fig. 7d maintained remains constant for all unsymmetrical conditions using ANN-based UPQC within IEEE 1159-1995 standards [23].

5 Conclusion

In this paper, the performance of an ANN-based custom power device UPQC carried for the proposed differently characterized hybrid green energy system with permanent magnet synchronous generator-based wind energy system and proton exchange membrane fuel cell system in a weak grid. The modelled compensator effectively handled both voltage and power fluctuations due to fluctuating wind effect of wind energy system without any difficulty by injecting appropriate voltage components and power quality issues due to symmetrical sag and unsymmetrical loading conditions within IEC 61000-4-15 and IEEE 1159-1995 international standards. These results will beneficial to researchers of hybrid renewable energy systems to improve the power quality issues.

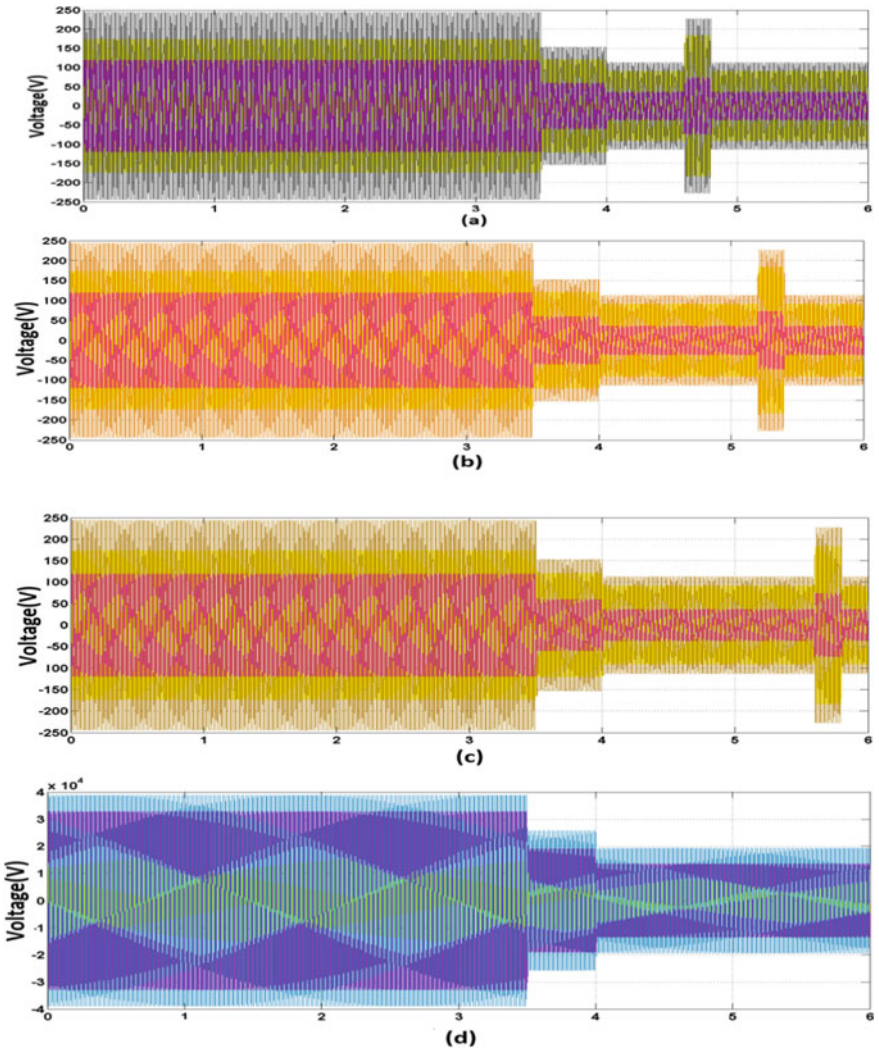

Fig. 7 Fault voltages on LV side of the transformer: **a** three-phase fault with fault resistance, **b** line to line fault with fault resistance, **c** L-G fault with fault resistance and **d** the HV side terminal voltage during the above three faults

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Thermal Energy Management Strategy of the Photovoltaic Cell Using Ferromagnetohydrodynamics

Sudip Shyam, Pranab K. Mondal, and Balkrishna Mehta

Abstract In the present investigation, a ferrofluid-based cooling method is suggested for the photovoltaic thermal (PVT) systems. Perturbing the ferrofluidic flow domain by an electromagnet can be an effective mechanism to alter the thermal flow characteristics. The temporal evolution of the ferrofluid flow domain under the influence of a constant and a time-varying magnetic field is observed by infrared thermography. The study has been conducted for three magnetic strength of $\overline{B} = 0G$, $\overline{B} = 700G$, and $\overline{B} = 1080G$, while the magnetic field frequencies are varied from 0.1 to 5 Hz. The primary objective of the investigation is to outline the mechanism of enhancement in heat transfer by exploring the role played by the various force fields, i.e., the interplay between the magnetic and the inertia force field. Also, the intricate interplay between the involved timescale, such as advective, diffusive, and magnetic perturbation timescales and its subsequent role on the thermal characteristics of the flow field, is explored in detail. Major inferences of the study are (a) on the application of external magnetic (constant and alternating) and heat transfer augments (b), and there exists a critical frequency (of the perturbing electromagnet) at which the augmentation is maximum; this frequency is a resultant outcome of the balance between the advective timescale and magnetic perturbation timescale. The inferences drawn from this investigation will have far-reaching implications in the purview of designing an effective thermal management in the photovoltaic systems.

Keywords IR thermography · Ferrofluid · Magnetic field

S. Shyam · P. K. Mondal (✉)
Microfluidics and Microscale Transport Processes Laboratory, Department of Mechanical Engineering, Indian Institute of Technology Guwahati, Guwahati, Assam 781039, India
e-mail: mail2pranab@gmail.com; pranabm@iitg.ac.in

S. Shyam
e-mail: sudipme2012@gmail.com

B. Mehta
Department of Mechanical Engineering, Indian Institute of Technology Bhilai, Raipur 492015, India
e-mail: krishnab@iitbhilai.ac.in

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1 Introduction

Solar energy is a renewable energy source that possesses an environment-friendly nature. The photovoltaic (PV) cell is a device that converts the falling sun's radiation into electrical energy by virtue of the photovoltaic effect [1, 2]. The overall efficiency of these photovoltaic cells depends on many factors, such as solar irradiation, tracking angle, and PV cell temperature. The efficiency of a solar cell is a strong function of the PV cell temperature. For every 1 °C increase in the cell's surface temperature, its efficiency decreases by 0.45% [3]. Owing to this particular fact, reducing the PV cell temperature has been an active area of research. Researchers have developed many active and passive techniques with which effective reduction in the surface temperature of the PVT system is possible [4–6]. Numerous researchers explored the role of nanofluid on the reduction of solar PV cell temperature [7–9].

Ferrofluid is a unique type of nanofluid. This particular fluid comprises magnetically active nanosized particles in a non-magnetic carrier medium [10, 11]. These nanoparticles are generally coated with a surfactant to avoid clustering. Under the influence of a magnet, the properties of ferrofluid get enhanced to a large extent [12]. These enhanced thermophysical properties ensure an augmented heat transfer in the flow domain [13–16]. Researchers have explored the implications of ferrofluid on a photovoltaic cell when disturbed by a magnetic field [17].

Even though most of the studies explored the implications of a static electromagnet on the ferrofluidic domain, a detailed experimental investigation of the consequence of a time-varying electromagnet on the cooling characteristics of a photovoltaic thermal system (PVT) is still lacking. Moreover, the measurement techniques adopted in such studies make the investigation quite narrow. When a magnetic field disturbs the flow domain, the evolution of the thermal flow field shows asymmetric characteristics, despite the existing geometrical symmetry. The temperature flow field and velocity flow field maintain symmetricity in an uninterrupted convective flow. However, perturbation by an electromagnet induces asymmetricity in the flow domain. Consequently, using a point measurement probe such as thermocouple in such a case may lead to erroneous results and may induce limitations to the investigation. Thus, in this investigation, an attempt is made to understand the implication of a magnetic field on the temporal evolution of the thermal flow field of ferrofluid flow in heated stainless steel (SS) capillary. Constant heat flux condition is provided to mimic the solar radiation falling in the photovoltaic cell, as can be seen from Fig. 1. The inferences drawn from this study could be extrapolated in designing an effective PVT cooling device. The ferrofluid flow field is perturbed by the static and alternating magnetic field. For the constant magnetic field study, three typical magnetic field strengths (B) are used, $\overline{B} = 0G$, $\overline{B} = 700G$ and $\overline{B} = 1080G$. A maximum heat transfer was found for $\overline{B} = 1080G$. Thus, in the alternating magnetic field case, electromagnet strength is maintained as $\overline{B} = 1080G$, and the frequency of electromagnet is tuned from 0.1 to 5.0 Hz. Infrared thermography measurement technique is adopted to record the temporal evolution of the thermal field.

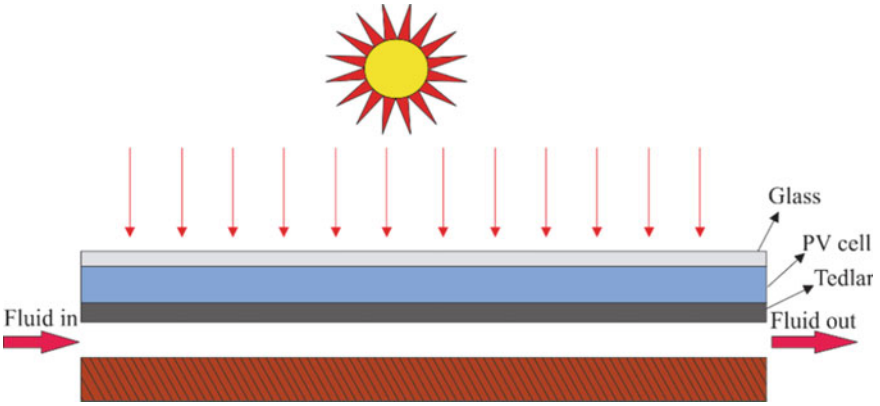

Fig. 1 Schematic of a photovoltaic cell along with its various components

2 Materials and Methods

The ferrofluid used is a water-based fluid having a 4.64% volume fraction of iron nanoparticles (V/V). The nanosized particles are coated with lauric acid to avoid clustering. The thermophysical properties of the fluids are highlighted in Table 1. Figure 2 illustrates the schematic of the developed experimental setup. The fabricated experimental setup consists of a test section, a DC power source for the heating mechanism, a syringe pump for driving the working fluid, an infrared camera for the acquisition

Table 1 Properties of ferrofluid and water

	Density (kg/m^3)	Specific heat (J/kg K)	Thermal conductivity (W/m K)	Viscosity (Pa S)
Water	995.2	4170	0.66	0.0091
Ferrofluid	1137.3	3420	0.71	0.00105

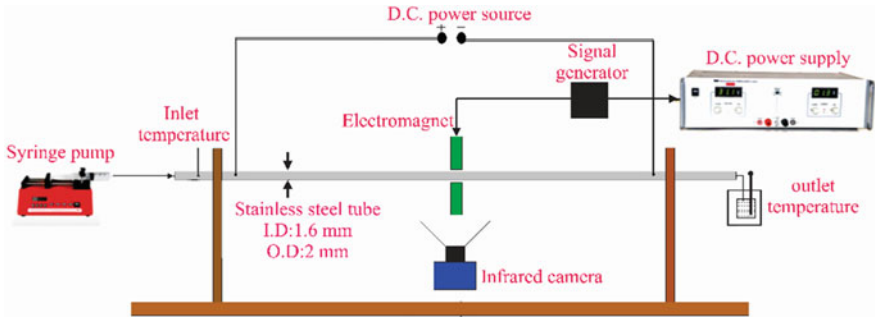

Fig. 2 Plot illustrates the schematic of the experimental setup

of IR thermograms, and two thermocouples for recording the inlet and outlet temperature. The test section consists of a SS capillary of inner diameter 1.6 mm, and a "C" shaped electromagnet, which stands on a PMMA platform. Uniform heat flux is maintained on the SS-tube surface, with the help of DC power source (make: Aplab). Power is delivered to the tube via copper electrodes, providing direct resistive heating. A heated length of 280 mm is maintained in the tube. Heat losses from the experimental setup are calculated following the conservation in energy principle, i.e., the difference between the energy supplied by the DC power source and the energy received by the working fluid. The heat losses were observed to be consistent and were around 2–3% for all the experiments.

The magnetic field is provided with the help of a C-shaped electromagnet, having a gap of around 5 mm in between the two poles. The SS capillary passes through this gap (the distance between the capillary surface and each individual pole is 1.5 mm). The electromagnet assembly is positioned on an internally threaded PMMA platform. For the alternating magnetic field case, the current is supplied to the electromagnet in a controlled manner by an in-house developed circuit. For measurement of the spatio-temporal evolution of the temperature flow field, an infrared camera (make: Flir A655Sc) is used. The infrared camera has a spectral bandwidth of 7.5–1.3 μm, with 16-bit digitization and a maximum FPS(frames per second) of 200 for the resolution of 640 × 120 pixels^2. Thin black tape ($K = 0.15$ W/m K) of emissivity, $\in = 0.98$, is used to coat the stainless steel tube for reliable IR readings. The spatial resolution of the IR camera is 15 μm in axial direction and 200 μm in the transverse direction. For the alternating magnetic field case, the IR camera acquisition rate is such that at least 40 images are captured at a particular time period of the magnetic field. The experiments are carried out in a dark room with a non-reflecting background to minimize the surrounding radiation.

3 Results and Discussion

3.1 Benchmarking of the Experiments

In the present investigations, infrared thermography is used for exploring the evolution of the temperature flow field of the ferrofluid flow domain. In Fig. 3, the benchmarking of our experimental results with the correlations of Churchill and Ozoe [18] is carried out. Churchill and Ozoe [18] proposed the following equations for hydrodynamically developed and thermally developing flow (for constant heat flux boundary conditions):

$$\frac{\mathrm{Nu}_{z,h} + 1}{5.364} = \left[1 + \left(\frac{220}{\pi} X^*\right)^{-10/9}\right]^{3/10} \tag{1}$$

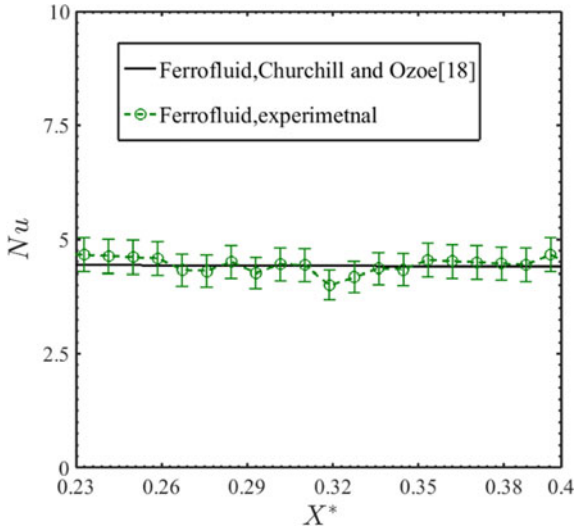

Fig. 3 Spatial evolution of Nu in the axial direction of the flow domain field in absence magnetic field

A good agreement can be observed in Fig. 3, between our experimental results and the correlation, as proposed by Churchill and Ozoe [18]. This agreement benchmarks our experimental results and justifies the reliability and accuracy of the IR thermography techniques adopted.

3.2 Distribution of Magnetic Field

In this section, we explore the spatial distribution of magnetic field flux inside the ferrofluid flow domain. As a result, the numerical simulations are conducted in the finite element platform of COMSOL Multiphysics®. Figure 4a depicts the computational domain of the simulated electromagnet. In Fig. 4b, we show the evolution of the magnetic flux and the magnetic force along the centerline of the flow field. The magnetic body force is calculated as

$$\overline{F} = (\overline{M}.\nabla)\overline{B} \tag{2}$$

where $\overline{M}$ is the magnetization and $\overline{B}$ is the magnetic flux density. The magnetization of the ferrofluid can be written as

$$\overline{M} = \chi \overline{H} \tag{3}$$

The magnetic flux density ($\overline{B}$) can be written as

$$\overline{B} = \mu_0(\overline{M} + \overline{H}) + \overline{B}_{\mathrm{R}} \tag{4}$$

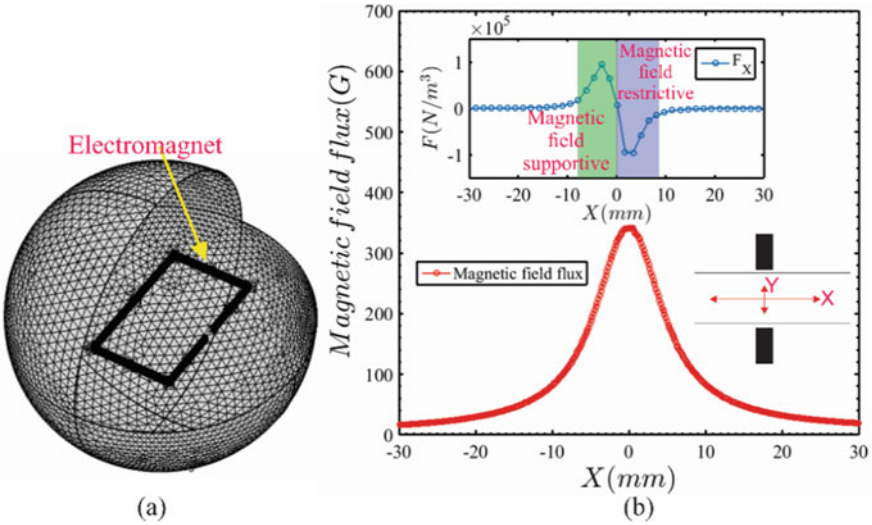

Fig. 4 **a** Plot depicts the meshing of the computation domain of the electromagnet. **b** The plot illustrates the distribution of the magnetic field along the centerline of the SS capillary. The inset depicts the changes in the magnetic force (F) along the centerline of the SS capillary

where $\overline{B}_R$ is the remnant flux density, μ_0 is the permeability of vacuum, χ is the susceptibility, and $\overline{H}$ is the magnetic field intensity. Using Eqs. (3) and (4) in Eq. (2), the magnetic body force (F) per unit volume can be written as:

$$F = \chi \nabla \left(\frac{B^2}{2\mu_0} \right) \tag{5}$$

Figure 4b illustrates the distribution of the magnetic flux density, $\overline{B}$ along the center of the flow field. It is clearly visible that, at $X = 0$, i.e., the center of the magnet, the flow domain realizes maximum magnetic force. The inset of Fig. 4b depicts the distribution of the magnetic force ($\overline{F}$) in the axial direction. It can be observed that the magnetic force exhibits a +ve and a −ve slope. Thus, it can be concurred that the role of magnetic force is both supportive and restrictive to the flow. At upstream of the magnet, the magnetic field supports the flow, while at downstream, it opposes the flow. This typical behavior of the magnetic field indicates that its sole intention is to retain the magnetic nanoparticle (MNP) aggregates in the magnetically active zone.

3.3 Effect of the Constant Magnetic Field

In Fig. 5, the impact of the magnetic field on the thermal characteristics of the

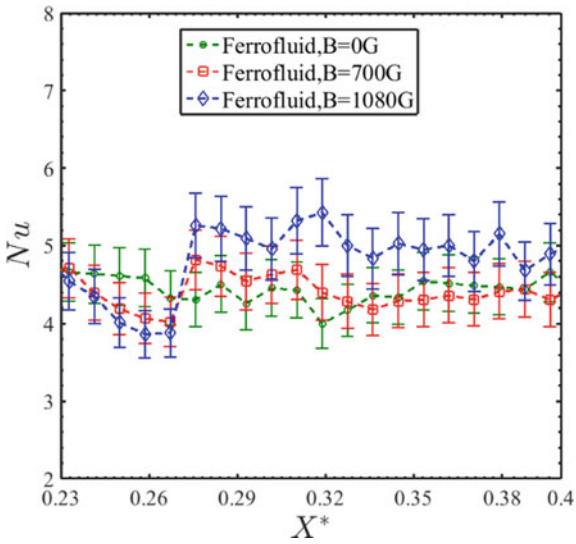

Fig. 5 Plot depicts the distribution of Nu is the axial direction for $\overline{B} = 0G$, $\overline{B} = 700G$ and $\overline{B} = 1080G$

ferrofluid flow is demonstrated. A close observation of Fig. 5 will show that under the influence of a magnetic field, augmentation in the heat transfer takes place in the flow domain. Also, the intensity of heat transfer augmentation is directly related to the applied strength of the magnetic field. This augmentation in the thermal behavior of the flow is possibly due to the fact that when the magnetic field is switched On, the magnetic nanoparticles (MNP) are attracted toward the magnet. These attracted MNPs get agglomerated in a chain-like cluster formation due to the dipole-dipole attraction [19]. As a consequence, hump-like structures (of MNPs) are formed at the walls near the vicinity of the magnetic poles. These structures disturb the bulk flow, in turn, enhances the momentum and thermal energy transport in the flow domain.

3.4 Effect of the Alternating Magnetic Field

It is quite evident from the preceding section that heat transfer is enhanced when a magnet perturbs the ferrofluid flow domain. In this section, the impact of a time-dependent magnetic field on the thermal flow characteristics is explored. The main motive behind using a time-dependent magnetic field is to ensure that the deposited ferrofluid aggregate at the magnetically active could be cleared off, such that fresh fluid could take its place. This spontaneous attraction of the magnetic particles and its subsequent clearing off to the bulk flow ensures that the boundary layer of the flow field is continuously disturbed, and thereby amplifying heat transfer. In Fig. 6, we show the variation of Nu for various magnetic field frequencies. It can be clearly observed that an initial increase in frequencies enhances the Nu. Then, after reaching its peak value, Nu decreases and ultimately attaining a constant value at higher

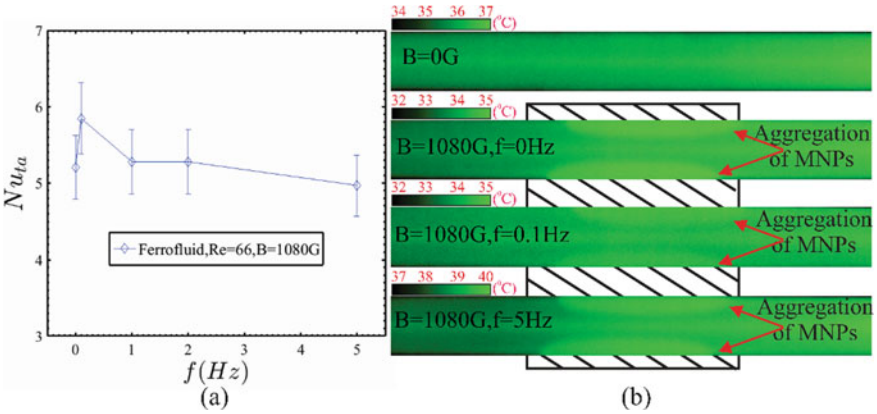

Fig. 6 **a** Plots depict the distribution of the time-averaged Nu for different electromagnet frequencies. **b** Thermogram represents the temperature flow field for the various magnetic field frequencies

frequencies. This typical behavior of the flow can only be understood once we explore the dynamics of the involved timescales, i.e., the advective timescale (L_C/U_{av}), the diffusive timescale $\left(L_C^2/\alpha\right)$, and the magnetic perturbation timescales $(1/f)$. The values of the various timescales involved are highlighted in Table 2.

From Table 2, we can clearly perceive that the diffusion timescale is larger than the other two timescales for all the cases. Thus, the flow dynamics are governed by the balance between the advective and perturbation timescales. At lower frequencies of the magnetic field, i.e., the case when $t_U < t_m$, the agglomerated aggregate could easily be cleared off during the OFF cycle (magnet in OFF state), thereby ensuring fresh ferrofluid aggregate takes its position and the redevelopment of the boundary layer of the flow field continues. While at high magnetic field frequencies, i.e., the case when $t_U > t_m$, the deposited aggregate could not be entirely dispensed from the flow domain. At very high frequencies, when $t_U \gg t_m$, the flow field behaves as if it is being perturbed by a constant magnet. As a result, the flow field attains almost a constant Nusselt number, and the redevelopment of the boundary layer is fully curtailed. Figure 6b depicts the temperature flow field captured by the IR camera. The hump-shaped cluster of MNPs is shown by the red marked arrows. As already explained at $f = 0.1$ Hz, a balance exists between the advective timescale and the perturbation timescale. As a result, the size of the hump of MNP's is minimum here.

Table 2 Values of the advective, diffusive, and perturbation timescale

Timescale	$f = 0.1$ Hz	$f = 1$ Hz	$f = 5$ Hz
Advective, $(t_U = L_C/U_{av})$	7.70	7.70	7.70
Diffusion, $\left(t_d = L_C^2/\alpha\right)$	14.1	14.1	14.1
Magnetic perturbation, $(t_m = 1/2f)$	5.0	0.50	0.10

However, at higher frequencies, i.e., at $f = 5$ Hz, the advective timescale is very high when compared to the perturbation timescale. Consequently, the thermal flow field resembles with the constant magnetic field case since the imbalance of the advective and perturbation timescale fully curtails the redevelopment of the boundary layer.

4 Conclusion

In the present investigation, the thermal characteristics of a magnetically perturbed heated ferrofluid flow domain are explored. The study is carried out to explore the suitability of ferrofluid as a means of lowering the temperature of a PVT system. The salient points from the present study can be enumerated as below:

- In the absence of a magnetic field, the ferrofluid behaves like its carrier fluid, and no augmentation in the thermophysical characteristics of the flow field is observed.
- Under the influence of a steady magnet, a 19% increase in heat transfer was observed when compared to the base case. The perturbation of the flow field by a constant magnet ensures the development of hump-like structures in the magnetically active zone. The hump-like structures mainly comprise of the MNPs, agglomerated in a chain-like fashion. These agglomerated MNPs disturb the bulk flow leading to augmentation of the thermal behavior of the flow field.
- On application of an alternating magnetic field, the augmentation process remains an interplay between the dominant timescales, mainly the advective and perturbation timescales. A critical frequency of $f = 0.1$ Hz is observed at which the advective timescale is balanced by the magnetic perturbation timescale. At this critical frequency, maximum enhancement in heat transfer is observed. The maximum enhancement of around 35% is observed when the electromagnet frequency is maintained at $f = 0.1$ Hz.

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ANN-Based Faster Indexing with Training-Error Compensation for MW Security Assessment of Power System

Shubhranshu Kumar Tiwary, Jagadish Pal, and Chandan Kumar Chanda

Abstract A simplified faster method for contingency analysis and screening is proposed for both on-line and off-line applications in electrical power networks. The suggested method uses the transmission line power flows to develop artificial neural network models which are then used for monitoring the transmission lines in real-time and provide binary output that signifies the state of the network. The outputs of the neural net are then used to calculate an index to determine the state of the whole power network grid. An additional term for the misclassification data has also been included to compensate for the errors in the classification of states, while using the neural networks. The proposed approach was applied to a test bus system and a state-owned utility. The results testify that the proposed method will provide faster results in shorter response time. The whole process of ANN-based security assessment is completed within 8 min.

Keywords Artificial neural networks · Load flow · Power system reliability · Power system security · Power system stability

1 Introduction

The rapid electrification of the rural areas and concurrent increase in the overall power consumption is leading to the electrical utilities operating with curtailed security margins every day. Some experienced people would say that a power network is constantly in a state of risk [1].

In this work, a new ANN-based method for real-time contingency analysis and ranking is proposed which takes a little under 8 min to provide the crucial information regarding the line loading severity. The time taken to arrive at acceptable results using ANN is nearly half of the time taken by traditional methods, which is very advantageous and relevant in the current deregulated power market scenario [2]. The proposed method uses the MW power flow on the lines based on historical records,

S. K. Tiwary (✉) · J. Pal · C. K. Chanda
Indian Institute of Engineering Science and Technology, Shibpur, Howrah 711103, WB, India
e-mail: mail_shubh2005@yahoo.co.in

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scheduling, and load forecasting, to develop simple neural net models to monitor transmission lines and provide binary outputs after reading the MW power flow on transmission lines. The binary outputs are then used to develop a new indexing method suggested in this work. This indexing may help as an ancillary service to help power system operators to execute crucial decisions.

This paper has five sections. Section 1 introduces the work. In Sect. 2, traditional MW security assessment method is revised, which is used here to verify the results. In Sect. 3, the ANN-based novel MW security assessment method is proposed and elaborated. In Sect. 4, two case studies are provided with comparison to the traditional methods. Section 5 concludes the paper with some insight into the work, followed by references.

2 Traditional MW Security Assessment

Traditional power system MW security assessment includes contingency analysis, ranking, selection, and evaluation as shown in Fig. 1.

To assess MW security of a power grid, contingency analysis is carried out as a routine activity in modern control centers. The double fold method of traditional process has the main drawback of consuming too much time for which 15 min is usually allotted, because of the complex calculations involved. In this work, Newton–Raphson load flow (NRLF) program has been used for the purpose of traditional security assessment process.

2.1 Contingency Analysis

The academic IEEE-14-bus network and the Damodar Valley Corporation's DVC-46 bus systems have been analyzed in this paper. In this work, for each line outage/contingency, a NRLF program is computed and the MW flows in other transmission lines are recorded. It may also be observed that the outage of some transmission lines has limited consequences on the power flow of remaining lines.

Fig. 1 Components of security assessment

2.2 Contingency Ranking

Transmission line flows are commonly restricted by thermal design limits, and sometimes outages may bring about limit violations in power (MW) flows. In such scenarios, system performance may be evaluated mathematically in terms of a dimensionless index which would reflect the severity of a contingency [3]. Performance index may be mathematically quantified using a function of line limits and line overloads in terms of the MW power flowing on a transmission line. The expression is as given in (1):

$$PI_{\mathrm{MW}} = \sum_{i=1}^{L} \frac{W_i}{2n} \left(\frac{P_i}{P_i^{\lim}} \right)^{2n} \tag{1}$$

where

P_i = The MW flow of line i.

$P_i^{\lim}$ = The MW capacity of line i.

i = The number of transmission lines in the system.

n = Stated exponent.

W_i = Real (non-negative) weighting co-efficient.

The $\mathrm{PI_{MW}}$ contains all line power flows normalized to their design limits. To obtain the absolute magnitude, the normalized line (power) flows are carried to an even power (by using $n = 1, 2, 3, \ldots$). $\mathrm{PI_{MW}}$ may have very small magnitude during the steady-state operation of power system, when the line active power flows are within the design limits, whereas $\mathrm{PI_{MW}}$ will have high magnitude during limit violation cases. The value generated using the above method is used for verification of ANN-based method proposed here.

3 Proposed ANN-Based MW Security Assessment Method

In this paper, a much simple ANN-based calculative approach is recommended, which can reduce the time consumption for contingency analysis and ranking by almost 50%. Instead of the 15 min time frame allotted for MW security method, the proposed ANN method takes a little less than 8 min.

As elaborated in [4], the ANN was applied to a stable power system as a tertiary application using the results of the power system load flow analysis. The method was robust but provided the results only in an off-line stable power network scenario, to identify the critical contingency. In the proposed method, a knowledge base concerning maximum and minimum stable power flow on a particular day in a

particular season in previous years is considered along with day ahead load forecast. Transmission line limits are also taken in to consideration. Based on these constraints, an acceptable secure state power flow range on each transmission lines is assumed. Taking the upper and lower limits of the above-mentioned range as the secure range of power flow and taking the power flow outside the aforementioned range as insecure, training data for the ANNs and their target classification are generated. The training data is minimal (only 300 datasets for each transmission line ANN) and is defined with clear delineation between the secure and insecure scenarios of the power network. The data can be minimized because every transmission line is designed and manufactured with a thermal limit which cannot be modified during the entire service life of the transmission line [5].

Thereafter, small supervised learning ANN with one input layer, one hidden layer, and one output layer is developed for each line. Small datasets are used for ANN training, keeping in mind the above-mentioned constraints, for rapid ANN development. The ANN's target output is assigned in the form of a binary set of 0's and 1's, where 0 means secure state of power flow on a line and 1 means insecure state of power flow. Generally, the best gradient for training was achieved at 26 epochs. Also, the training, validation, and testing accuracy was 100% because of the less quantity of training data and clear bordering between the two output classes.

In this way, an ANN is developed to monitor each line of a power network. Then, the outputs of all these ANNs are used to develop the proposed index, called as the Neural Net Index ($\mathrm{NI_{MW}}$) as shown below:

$$\mathrm{NI_{MW}} = \frac{1}{L}\sum_{i=1}^{L}(W_i Y_i + e_i) \tag{2}$$

where

Y_i = Output of the ANN monitoring line number *i*.

L = Total number of transmission lines on the network.

W_i = Real (non-negative) weighting co-efficient for line *i*.

e_i = Term for Erroneous Classification during Y_i training.

Since the ANN is trained to provide binary classifications of the states of the network, as explained previously, an error term is added to the results to compensate for the erroneous classification, if the accuracy during training is not 100%. This error term is usually significant when the error percentage during ANN training is large. The e_i term represents the cross-entropy loss for binary classifications and is determined using the equation provided below.

$$e_i = -(g \log q + (1 - g)\log(1 - q)) \tag{3}$$

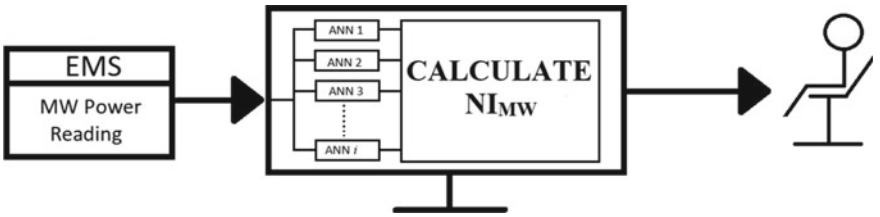

Fig. 2 NIMW process in real time

where g = binary indicator (either '0' or '1') if class marker 'x' is the correct classification for observation 'y'; q = predicted probability that observation 'y' is of class 'x'; log = natural logarithm.

In this method, the output of all the ANNs monitoring each line is summed up and divided by total number of transmission lines, during the event of any contingency. The weighting co-efficient signifies priority of any line, and its corresponding value may be changed depending on the preferences of the power system operator at dispatch center. The whole process of the ANN-based security assessment method can be explained with the help of Fig. 2.

The ANN model used in this work is a simple feed-forward neural network with error back-propagation. The developed ANN provides monitoring results almost instantly. Hence, the whole process of ANN development and obtaining monitoring results is completed within 8 min in real time, compared to the 15 min time frame using the traditional method. The results were verified using traditional method, to assess the computational performance, precision, time consumption, and physical significance. The analysis was performed on two networks shown in Figs. 3 and 4.

4 Case Studies and Application of NI_{MW} Method

The proposed method of the ANN-based security assessment was tested on a standard test bus system and a real-time utility grid of the Damodar Valley Corporation's, DVC-46 bus system. The results were verified using traditional method, to assess the computational performance, precision, time consumption, and physical significance. The analysis was performed on a laptop computer with an Intel Core-i7, 8th generation CPU with 6 cores, 8-GB of RAM (Random Access Memory), 128-GB Solid State Drive, and 1-TB of hard disk with a multi-thread processor.

4.1 Standard IEEE-14-Bus System Case

The academic test bus system network is shown in Fig. 3.

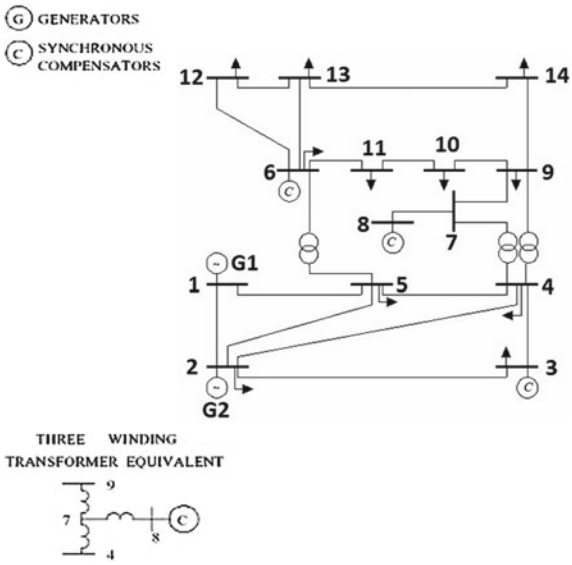

Fig. 3 IEEE-14-Bus test network

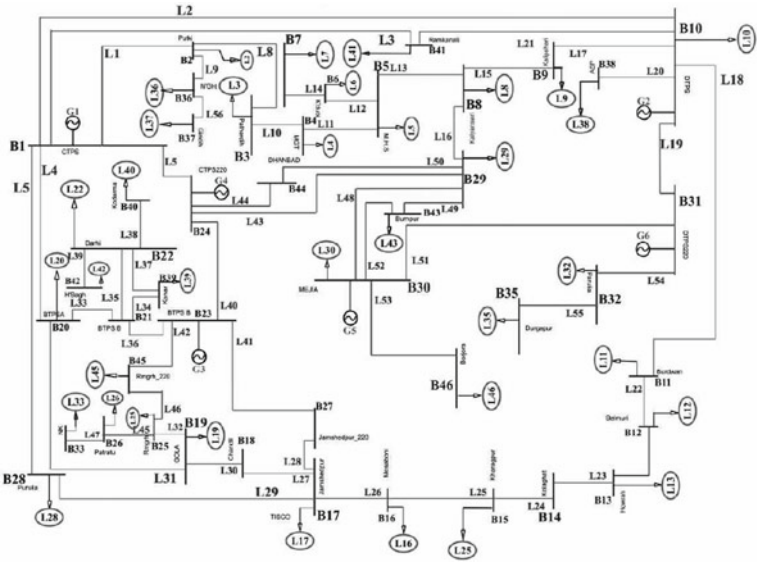

Fig. 4 DVC-46-bus network

The contingency analysis for the IEEE-14-bus academic network is performed as mentioned in Sect. 2. The performance index and ranking are calculated based on (1) and are given in Table 1.

Table 1 Ranking of the standard IEEE-14-bus system using traditional method

Rank	Line No.	PI_{MW}	Rank	Line No.	PI_{MW}
1.	17	9.874205	11.	5	1.071131
2.	16	3.787976	12.	9	1.069893
3.	3	2.878448	13.	8	1.067106
4.	15	2.828074	14.	1	1.061203
5.	14	2.621413	15.	13	1.051355
6.	12	2.257977	16.	6	0.936214
7.	4	2.171254	17.	11	0.935310
8.	18	1.136124	18.	2	0.914468
9.	20	1.085117	19.	7	0.129524
10.	19	1.081868	20.	10	0.00

Here, the higher the value of PI_{MW} the more critical is the line and the lower the value of PI_{MW} the more non-critical is the line. The time taken for calculating the PI_{MW} value for each contingency is recorded for comparison with the ANN-based indexing method. Then, the ANN-based contingency analysis method is performed. In this case, as mentioned previously, all lines are monitored by dedicated and specifically trained ANN. These ANNs provide binary outputs, where 0 means secure state of power flow and 1 means insecure state of power flow. When the power flowing on a line is within the prespecified secure range of power flow, the ANN classifies it as 0 otherwise 1. If in the event of contingency of any line, the power flow of any other line goes in to the insecure range, and its corresponding ANN acknowledges the state immediately. These ANN outputs are then used to comprehend mathematically the state of the power network immediately by using (2) as elaborated in Sect. 3. The outcome of the ANN-based line outage (contingency) analysis for the network of IEEE-14-bus system has been shown in Table 2.

Table 2 Ranking of the standard IEEE-14-bus system using NI_{MW} method

Rank	Line No.	NI_{MW}	Rank	Line No.	NI_{MW}
1.	17	0.90	11.	5	0.35
2.	16	0.85	12.	9	0.30
3.	3	0.80	13.	8	0.25
4.	15	0.75	14.	1	0.15
5.	14	0.70	15.	13	0.10
6.	12	0.60	16.	6	0.05
7.	4	0.55	17.	11	0.05
8.	18	0.50	18.	7	0.05
9.	20	0.45	19.	2	0.00
10.	19	0.40	20.	10	0.00

Table 3 Time taken to obtain results using NI_{MW} method

Knowledge base development (A)	Generating training data (all lines) (B)	Training and ANN development (C)	Identification of line outage and critical contingencies (D)	Total time $A + B + C + D$
142 s	122 s	110 s	16 s	390 s

As in Table 2, the ANN-based ranking of the lines is arranged in descending order. Here, the closer the value of NI_{MW} to 1 the more critical is the line and the closer the value of NI_{MW} to 0 the more non-critical is the line. The ANN based ranking is also almost exactly same as the traditional MW ranking and takes much less time to generate the results. The comparisons between time taken to attain the results are shown in Table 3.

From Table 3, it can be deduced that the whole process of ANN-based contingency analysis and ranking can be completed in little under 7 min for IEEE-14 bus network. And from the results of the ranking of the power network, it can also be seen that the ANN-based ranking correctly specifies 90% of all contingency cases, including critical ones. It may be noted here that the actual time taken for identifying line outages and detecting critical cases thereafter, which is the main aim of traditional security assessment procedure, is completed within 16 s.

And, mathematically, NI_{MW} range for each contingencies effect on the overall power network can be elaborated as below.

$0.80 \leq NI_{MW} \leq 1.0 \rightarrow$ Critical

$0.50 \leq NI_{MW} \leq 0.79 \rightarrow$ Alert

$0.00 \leq NI_{MW} \leq 0.50 \rightarrow$ Non-critical/No concern.

4.2 Real-World Damodar Valley Corporation's DVC-46 Bus Case

The DVC-46 bus system of the Damodar Valley Corporation grid network is as shown in Fig. 4. The DVC is a multi-purpose river valley project which operates with 4 hydel power plants and 10 thermal power plants and 36 substations. The contingency analysis for the DVC-46 bus grid network is performed as mentioned in Sect. 2. The performance index and ranking are calculated by using (1) and are tabulated in Table 4.

In this case as well, the time taken for calculating the PI_{MW} value for each contingency is recorded for comparison with the ANN-based indexing method. Then, the ANN-based indexing is performed, and as before, if in the event of contingency of any line, the power flow of any other line goes in to the insecure range, its corresponding ANN acknowledges the state immediately. These, ANN outputs can then be used to comprehend mathematically the state of the power network immediately,

Table 4 Ranking of the DVC-46-bus system using PI_{MW} Method

Rank	Line No.	PI_{MW}	Rank	Line No.	PI_{MW}
1.	12	69.78	29.	19	7.81
2.	18	65.24	30.	11	7.56
3.	45	63.84	31.	10	6.99
4.	3	63.02	32.	1	5.69
5.	41	59.14	33.	4	4.77
6.	8	48.23	34.	36	3.57
7.	27	45.62	35.	43	2.95
8.	9	43.32	36.	26	2.65
9.	48	42.59	37.	25	1.98
10.	51	41.98	38.	46	0.92
11.	30	41.02	39.	6	0.86
12.	31	40.25	40.	49	0.79
13.	32	39.85	41.	34	0.75
14.	53	37.67	42.	52	0.71
15.	21	32.51	43.	35	0.68
16.	50	30.15	44.	37	0.62
17.	40	28.21	45.	2	0.56
18.	16	10.69	46.	7	0.00
19.	15	10.42	47.	14	0.00
20.	29	10.08	48.	20	0.00
21.	44	9.75	49.	22	0.00
22.	17	9.55	50.	23	0.00
23.	5	9.30	51.	38	0.00
24.	24	9.01	52.	39	0.00
25.	33	8.82	53.	47	0.00
26.	13	8.50	54.	54	0.00
27.	42	8.21	55.	55	0.00
28.	28	8.07	56.	56	0.00

by using (2) elaborated in Sect. 3. The results of the ANN-based contingency analysis for the DVC-46 bus network are shown in Table 5.

As shown in Table 5, the ANN-based ranking of the lines is arranged in descending order. The individual ANN monitoring each line gives an output of 0 or 1 based on the state of the power flow at any given instant. The ANN-based ranking is also almost exactly same as the traditional MW ranking and takes much less time to generate the results. The time taken to attain the outcome for the DVC-46 bus grid network is shown in Table 6.

Table 5 Ranking of the DVC-46-bus system using NI_{MW} method

Rank	Line No.	NI_{MW}	Rank	Line No.	NI_{MW}
1.	12	0.96	29.	19	0.27
2.	18	0.95	30.	11	0.21
3.	45	0.91	31.	10	0.18
4.	3	0.87	32.	1	0.16
5.	41	0.85	33.	4	0.14
6.	8	0.84	34.	36	0.12
7.	27	0.82	35.	43	0.11
8.	9	0.80	36.	26	0.09
9.	48	0.78	37.	25	0.07
10.	51	0.77	38.	46	0.05
11.	30	0.71	39.	6	0.04
12.	31	0.69	40.	49	0.02
13.	32	0.68	41.	34	0.02
14.	53	0.66	42.	52	0.02
15.	21	0.63	43.	7	0.02
16.	50	0.61	44.	35	0.02
17.	40	0.59	45.	2	0.02
18.	16	0.57	46.	37	0.00
19.	15	0.55	47.	14	0.00
20.	29	0.54	48.	20	0.00
21.	44	0.50	49.	22	0.00
22.	17	0.45	50.	23	0.00
23.	5	0.43	51.	38	0.00
24.	24	0.41	52.	39	0.00
25.	33	0.38	53.	47	0.00
26.	13	0.36	54.	54	0.00
27.	42	0.34	55.	55	0.00
28.	28	0.32	56.	56	0.00

Table 6 Time taken to obtain results using NI_{MW} method for DVC system

Knowledge base development (A)	Generating training data (all lines) (B)	Training and ANN development (C)	Identification of Line outage and critical contingencies (D)	Total time $A + B + C +$ D
150 s	163.4 s	118.8 s	16 s	448.2 s

From Table 6, it has been observed that, even in the case of a utility grid of DVC-46 bus system, the whole process of ANN-based contingency analysis and ranking can be completed in a little under 7.5 min. And from the results of the ranking of the power network, it can also be seen that the ANN-based ranking correctly specifies 95% of all contingencies (even the critical ones) and correctly ranks them. It may be noted here that the actual time taken for identifying line outages and detecting critical cases, which is the main aim of traditional security assessment procedure, is also completed within 16 s using the novel proposed method.

5 Conclusion

The new concept of ANN-based indexing to be used in place of the traditional MW security assessment method was introduced, and an inclusive scheme for its development and application has been proposed in this paper.

The important inference of the assorted modules and methodologies proposed in this paper is:

1. a cross-entropy-binary loss function has been introduced for use in real time, to account for the misclassifications incurred during training.
2. simplicity for the real-time application and development of ANNs (as is evident from Tables 3 and 6).
3. the whole process of evaluation and selection of critical contingencies is completed in a little over 7 min (which is half (50%) of the 15 min time frame currently practiced in the power sector) which again proves the real-time applicability.
4. the output provided by the ANNs is binary in nature; hence, the calculation required for finding of the critical cases can also be quickly verified manually by the power system operators.
5. masking effects can also be compensated using the binary cross-entropy loss function
6. if the amount of training data for each ANN is equal, the time taken to provide correct results is also same

The process mentioned above may also be applied to large-scale power system, in a smart grid environment, for transient stability analysis and dynamic security assessment.

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Effect and Utilization of Leakage Inductance on the Performance of Multi-zone and Multi-load Half-Bridge Inverter Based Induction Heating System

Kallol Bhaumik, Avik Datta, and Pradip Kumar Sadhu

Abstract This research work aims to analyze the performance of multi-zone half-bridge inverter in terms of current gain including the effect of leakage inductance. Leakage inductance has been included in series with the load which is very similar to a transformer's leakage inductance. In general leakage, field is not desired. Utilization of leakage inductance is another aspect of this research work. Result shows that a higher value of current gain can be achieved with the help of leakage inductance. This means output current can be varied widely. Result also shows that beyond a particular value of leakage inductance current gain of the proposed inverter reduces due to weak flux linkage. Mutual induction effect has been neglected. Multi-load topology can be utilized to heat a number of objects at a time. The proposed circuit topology includes the multi-load as well as multi-zone heating and it has been simulated in PSIM environment.

Keywords Current gain · Leakage inductance · Multiple loads · Multi-zone inverter

1 Introduction

There are many applications [1] where the control of output current over a wide range is required. In the conventional half-bridge inverter current can be controlled [2–4] by varying the switching frequency. But variation of switching frequency results in complicated magnetic component design. Leakage inductance of the coil can be utilized to vary the inverter output widely. In this paper, current gain variation of a

K. Bhaumik (✉) · A. Datta · P. K. Sadhu
Electrical Engineering Department, Indian Institute of Technology (ISM) Dhanbad, Dhanbad 826004, India
e-mail: kallol_mid@yahoo.co.in

A. Datta
e-mail: avikdutta1985@gmail.com

P. K. Sadhu
e-mail: pradip@iitism.ac.in

A. Sikander et al. (eds.), *Energy Systems, Drives and Automations*, Lecture Notes in Electrical Engineering 664, https://doi.org/10.1007/978-981-15-5089-8_5

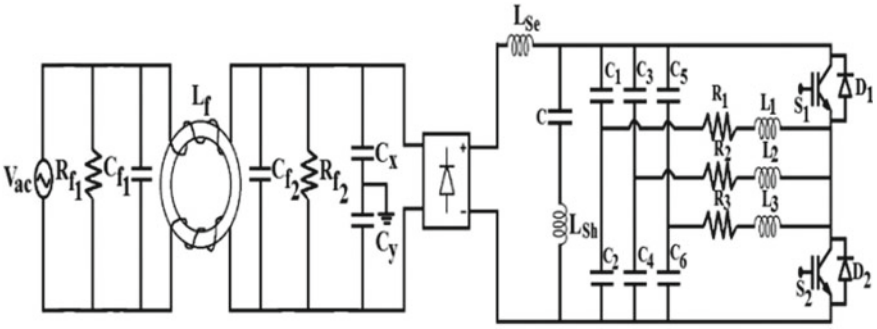


Fig. 1 Multi-zone and multiple-output induction heating system using half-bridge inverter

multi-zone multi-load half-bridge inverter-based induction heating system with the help of leakage inductance has been proposed.

This paper divided into two major parts. First part deals with the analysis of the proposed circuit followed by the effect of leakage inductance in current gain of the proposed circuit topology.

Analysis of Proposed Circuit: Proposed circuit provides three stages of operation. First stage of operation involves the ring filter followed by bridge rectifier. The output of the bridge rectifier is converted to the alternating quantity by a high-frequency half-bridge inverter. This stage is called inversion stage. In this circuit, IGBT is used as semiconductor switch.

Figure 1 presents the proposed multi-zone and multiple-output half-bridge inverter induction heating system. This assembly consists of one ring filter, a bridge rectifier and a multiple-output half-bridge inverter.

Different states of operation of the proposed circuit are shown below.

Figure 2a presents the charging phenomena of working coil when switch S_1 is turned on. Figure 2b shows the discharging phenomena of the working coil through freewheeling diode D_2. Figure 2c, d depicts the same charging and discharging phenomena when switch S_2 is turned on.

It is evident from Fig. 3a, b that induction heating can be found in series and shunt coils. Heating is available in different zones of the proposed inverter that means in series coil, shunt coil and three working coils when any one switch is turned on. This phenomenon is called multi-zone heating effect. Figure 3c depicts the output current waveforms for the load.

Inverter coils and load can be represented by an equivalent load impedance as shown in Fig. 4.

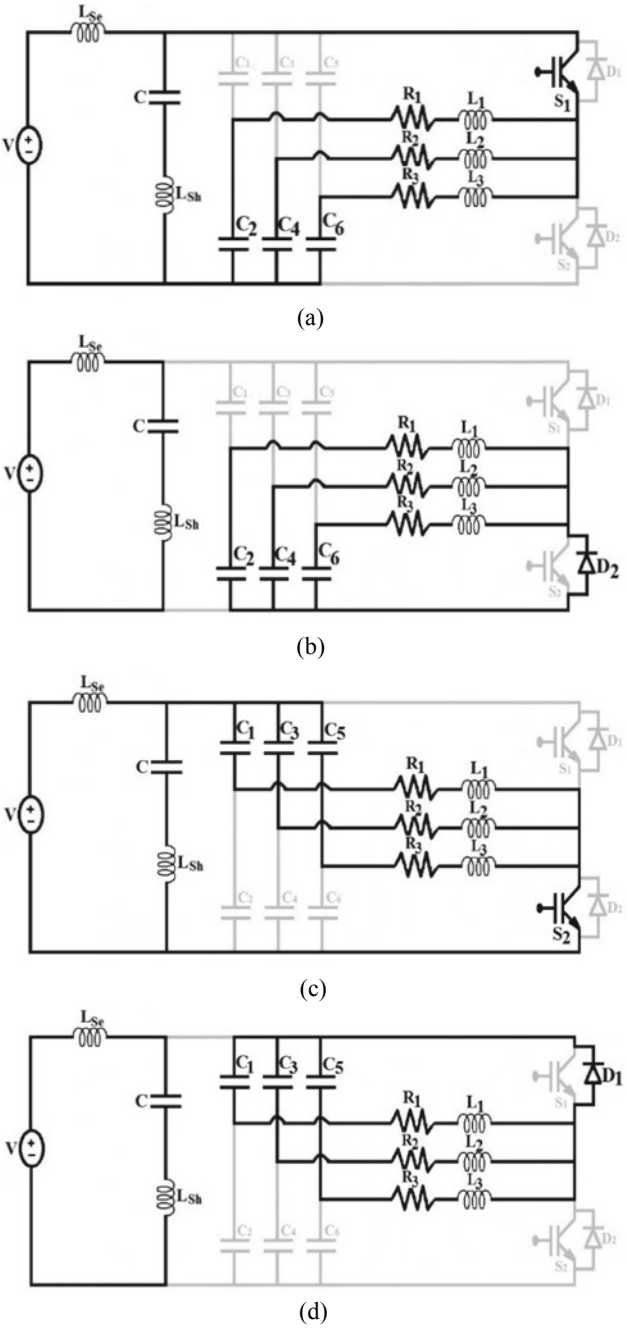
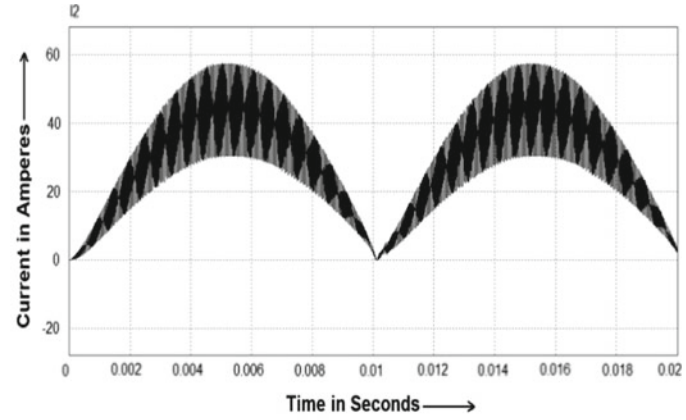
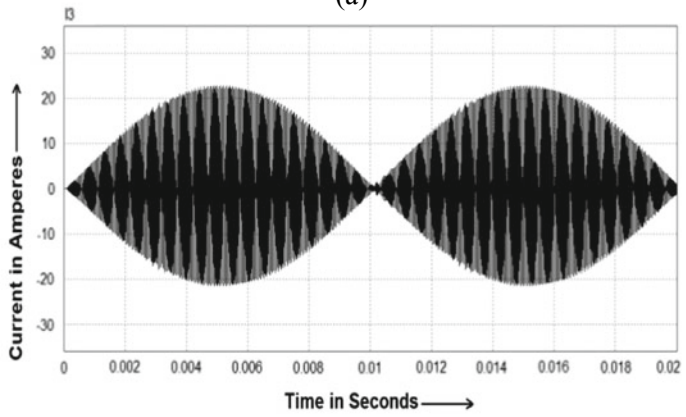


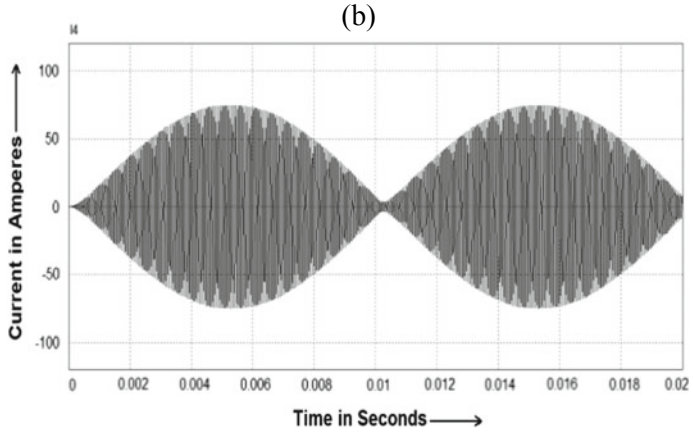
Fig. 2 Operating modes for under **a** upper switch S_1 is on, **b** upper switch S_1 is off, **c** lower switch S_2 is on and **d** lower switch S_2 is off



(a)



(b)



(c)

Fig. 3 Charging current waveform for **a** the coil Lse, **b** the coil Lsh and **c** coils *L*1, *L*2 and *L*3

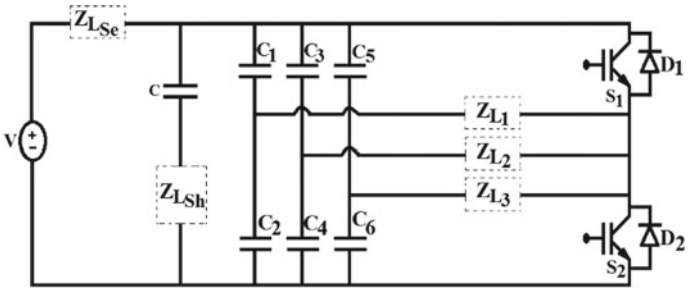


Fig. 4 Multi-coil induction heating system with the coils replaced by a single-phase transformer on load condition

2 Introduction to Leakage Inductance

The leakage inductance of multi-zone induction heater has already been calculated in [5, 6]. Leakage field of the solenoid has been shown in Fig. 5.

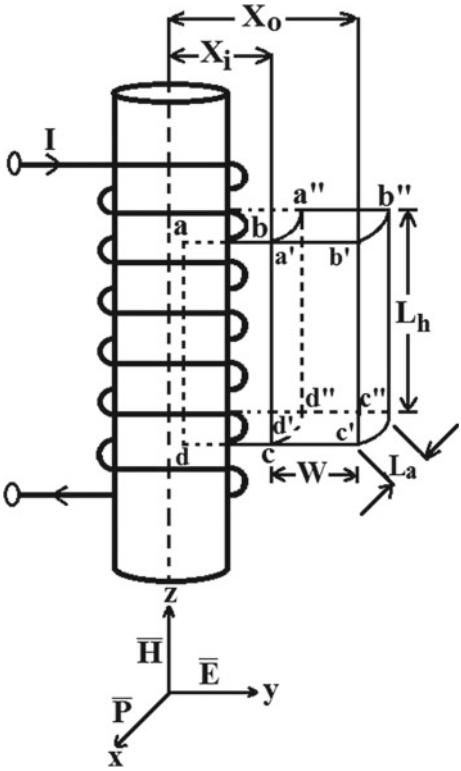


Fig. 5 Leakage field of solenoid

$$L_{lk} = \frac{1}{2}\mu_0 L_a \frac{N^2}{L_h} \frac{1}{\text{Sinh}^2(\gamma W)} \times \left[\frac{1}{4\gamma}\text{Sinh}(2\gamma W) + \frac{W}{2}\right] \quad (1)$$

Although Leakage inductance is not desirable, in some cases it plays a vital role [7–10]. Leakage inductance is equivalent to the series inductance. In this work leakage inductance is connected in series with the load impedance at the multi-load output side as shown in Fig. 6. One major drawback is that voltage regulation is affected in this process but current gain is improved. Equivalent circuit is shunt connected series RLC circuit as shown in Fig. 7. The effect of mutual inductance is neglected.

Figure 6 presents the proposed multi-zone multiple-output induction heating systems including leakage inductance.

Figure 7 presents the equivalent circuit of multiple-output load which is basically a parallel RLC circuit.

Frequency of resonant network

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (2)$$

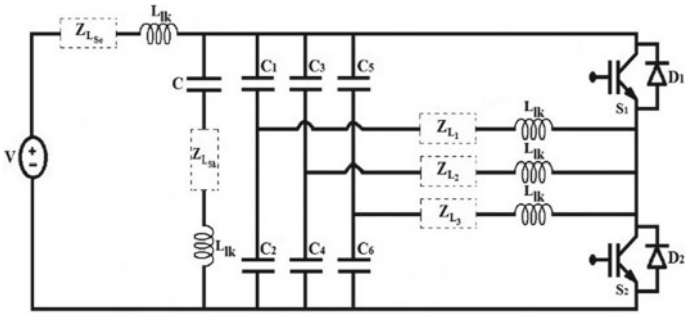


Fig. 6 Multi-coil induction heating system with the coils replaced by a single-phase transformer including leakage inductance on load condition

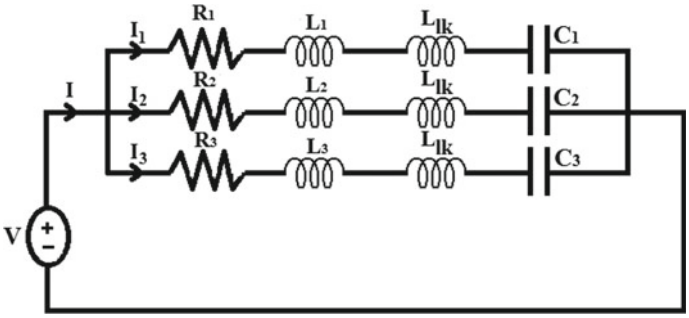


Fig. 7 Equivalent circuit of multiple-output

Table 1 Parameters of proposed inverter configuration

Item	Symbol	Value
Source voltage	V_{DC}	220 V
Resistance of each load	R	1 Ω
Inductance of each load	L	157 μH
Capacitance of each load	C	25.3 μF
Supply capacitance	C_s	0.4 μF
Switching frequency	f_{sw}	20 kHz

The ratio between the switching and resonant frequency is termed as normalized switching frequency and is given by

$$\omega_n = \frac{\omega}{\omega_0} \tag{3}$$

where ω is the switching frequency.

The circuit determines the magnitude of coupling and is given by

$$Q = \frac{R_L}{\omega_0 L} \tag{4}$$

The characteristic impedance of the circuit is given by

$$Z_n = \sqrt{\frac{L_{eq}}{C}} \tag{5}$$

where L_{eq} = Equivalent Inductance including leakage inductance.

Now the expression of current gain is

$$I_{gain} = \frac{I_0}{\left(\frac{V_d}{Z_n}\right)} = \frac{8}{\pi^2} \frac{1}{Q\left(1-\omega_n^2\right) + j\frac{8}{\pi^2}\omega_n} \tag{6}$$

Resonant capacitance can be calculated using the expression mentioned below.

$$C_r = \frac{1}{L_r\,(2\pi\, f_{s\omega})^2} \tag{7}$$

3 Simulation Results and Waveforms

In this work, 220 V is chosen as source voltage, 157 μH as coil inductance, 20 kHz as switching frequency as shown in Table 1 and value of resonance capacitance has been calculated using Eq. 1.

The value of current gain has been recorded for different values of leakage inductance. Table 2 presents a comparative study between the current gain with and without leakage inductance. At 0.0435 μH leakage inductance changes in current gain is not so much significant. Considerable changes in current gain occur from 10 μH leakage inductance.

Above results show that increment of leakage inductance results in increment of current gain. But after 100 μH of leakage inductance current gain falls abruptly and sharply. It happens due to weak flux linkages between working coil and load.

Figure 8 represents load current waveforms for the different leakage inductance. It shows the influence of leakage inductance on current gain. Presence of leakage inductance increases the value of current gain but at 100,0000 μH leakage inductance magnitude of current gain is very low shown in Fig. 8.

Though leakage inductance improves current gain, it has been observed that beyond a particular value of leakage inductance, current decreases and hence current gain decreases shown in Fig. 9. Increment of leakage inductance results in effective flux linkage reduction. Hence power transfer will be affected and load current will be decreased.

4 Conclusion

Leakage inductance of the induction heating coil is utilized in multi-zone multi-load induction heating system to improve the current gain. It has been observed that leakage inductance has a useful effect on the current gain but beyond a particular value current gain decreases. Current gain result has been compared with and without leakage inductance.

Table 2 Comparison of simulation results for different values of leakage inductance

Leakage inductance in micro-henry (μH)	Coil name	RMS value of output current in ampere (I_o)	RMS value of input current in ampere (I_{in})	Current gain
Solenoid under load impedance without leakage inductance	Z_{Lse}	27	26.8	1.007
	Z_{Lsh}	8.8	26.8	0.328
	Z_{L1}	30.9	26.8	1.153
	Z_{L2}	30.9	26.8	1.153
	Z_{L3}	30.9	26.8	1.153
Solenoid under load impedance including leakage inductance 0.0435 μH	Z_{Lse}	28.5	28.3	1.007
	Z_{Lsh}	8.9	28.3	0.314
	Z_{L1}	33.8	28.3	1.194
	Z_{L2}	33.8	28.3	1.194
	Z_{L3}	33.8	28.3	1.194
Solenoid under load impedance including leakage inductance 10 μH	Z_{Lse}	24.4	24.2	1.008
	Z_{Lsh}	8.4	24.2	0.347
	Z_{L1}	31.7	24.2	1.31
	Z_{L2}	31.7	24.2	1.31
	Z_{L3}	31.7	24.2	1.31
Solenoid under load impedance including leakage inductance 15 μH	Z_{Lse}	20.2	19.8	1.02
	Z_{Lsh}	8.2	19.8	0.414
	Z_{L1}	29.1	19.8	1.47
	Z_{L2}	29.1	19.8	1.47
	Z_{L3}	29.1	19.8	1.47
Solenoid under load impedance including leakage inductance 30 μH	Z_{Lse}	11.4	10.6	1.07
	Z_{Lsh}	7.3	10.6	0.688
	Z_{L1}	21.6	10.6	2.04
	Z_{L2}	21.6	10.6	2.04
	Z_{L3}	21.6	10.6	2.04
Solenoid under load impedance including leakage inductance 100 μH	Z_{Lse}	3.7	3.06	1.21
	Z_{Lsh}	4.6	3.06	1.5
	Z_{L1}	11.3	3.06	3.7
	Z_{L2}	11.3	3.06	3.7
	Z_{L3}	11.3	3.06	3.7
Solenoid under load impedance including leakage inductance 1,000,000 μH	Z_{Lse}	0.004	0.45	0.008
	Z_{Lsh}	0.02	0.45	0.045
	Z_{L1}	0.0014	0.45	0.003
	Z_{L2}	0.0014	0.45	0.003
	Z_{L3}	0.0014	0.45	0.003

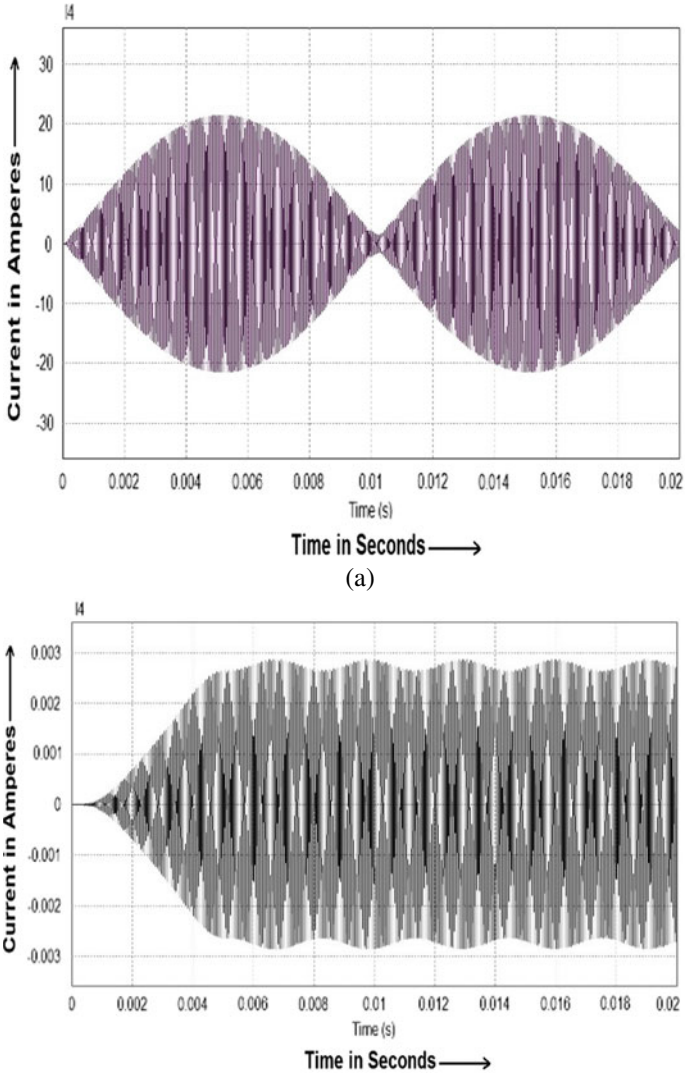


Fig. 8 Load current waveform for the coils ZL1, ZL2 and ZL3 including leakage inductances. **a** 100 μH and **b** 1,000,000 μH

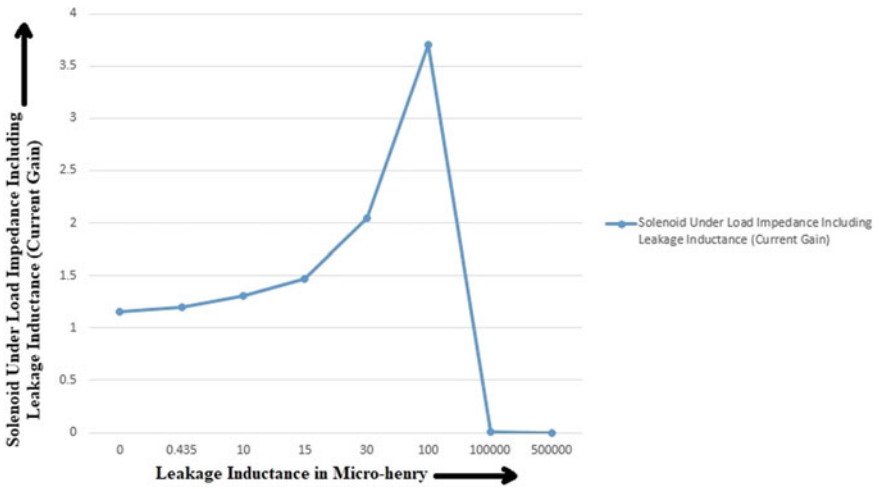


Fig. 9 Characteristic curve of leakage inductance versus current gain

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Static and CV Analysis of Gate Engineered GAA Silicon Nanowire MOSFET for High-Performance Applications

Neha Gupta, Ajay Kumar, and Rishu Chaujar

Abstract This paper discusses the performance analysis of Gate Electrode Work-function Engineered (GEWE) Silicon Nanowire (SiNW) MOSFET using device simulation software: ATLAS-3D in terms of static performance. The following performance metrics are studied: transconductance, conduction current density, potential, electron temperature and electric field. The effectiveness of GEWE-SiNW design was scrutinized by comparing it with conventional SiNW MOSFET. It is found that with the incorporation of GEWE scheme onto SiNW, it improves the conduction current density thus enhances the device current capability. In addition, device CV behaviour is also analyzed as a function of gate and drain bias voltage. This analysis is studied with an aim to optimize the gate length and oxide thickness for improved high-performance applications. It is perceived from the results that as gate length scales down to 10 nm and oxide thickness at 1.5 nm, both C_{gs} and C_{gd} reduce appreciably owing to low off current and high on current. Thus, GEWE-SiNW device paves the way for high switching performance applications.

Keywords Gate engineered · Silicon nanowire · Parasitic capacitance · RF FOMs

1 Introduction

Scaling of MOSFET to nano-regime dimensions is the utmost requirement for the semiconductor industry to achieve high speed, low power dissipation and higher density on a single chip [1, 2]. During scaling down of MOSFET dimensions, some

N. Gupta
ASH Department, Dr. Akhilesh Das Gupta Institute of Technology and Management (IPU), New Delhi, Delhi, India
e-mail: nehagupta@dtu.ac.in

A. Kumar (✉)
ECE Department, Jaypee Institute of Information Technology, Noida, India
e-mail: ajaykumar@dtu.ac.in

R. Chaujar
Department of Applied Physics, Delhi Technological University, Delhi, India
e-mail: chaujar.rishu@dtu.ac.in

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drawbacks arise known as Short Channel Effects (SCEs) such as drain induced barrier lowering (DIBL) [3], hot carrier effects (HCEs) [4, 5] due to high electric field at the drain end, punchthrough, threshold voltage roll-off, etc. [1, 6]. Another problem that arises due to scaling is that power supply is not scaled in proportion to device dimensions owing to which power dissipation increases and thus hampers the circuit performance in terms of noise, parasitic capacitances and delay requirements [4, 7]. To overcome this discrepancy, different device engineering schemes have been reported in literature, some of them are gate work function engineering [8, 9], gate stack engineering [10–12], gradient channel doping, etc. Moreover, novel device structures and novel channel materials also emerged as new ways to overcome the SCEs. Recently, Silicon nanowire (SiNW) MOSFET [13–15] looked like a possible solution due to ease of fabrication and outstanding properties of SiNW as it scales down to few nm ranges without compromise its characteristics. Latest study on device fabrication validated that GAA SiNW MOSFET owns superior electrical performances and good SCEs immunity [16, 17]. It was also shown that their cut-off frequency is considerably higher than planar Si MOSFET [18]. However, nanowire itself suffers from a shortcoming of gate leakage current due shrinkage of nanowire radius. Thus, to overcome this problem and to enhance the overall device performance of SiNW MOSFET, we have combined the gate electrode work function engineered (GEWE) scheme onto GAA SiNW. The gate electrode work function engineering scheme has already been applied onto many device structures like double-gate (DG) MOSFET [19], Recessed channel MOSFET [20, 21], junctionless MOSFET, surrounding gate MOSFET and found device overall improvement specifically in terms of increasing current capability and reduced SCEs. Moreover, we have already revealed in our previous work with the integration of gate engineering onto GAA SiNW, it improves device cut-off frequency and RF linearity [22, 23]. Therefore, this work examines the high performance of GAA gate engineered SiNW MOSFET in terms of static performance and its related parameters using ATLAS 3-D device simulator [24]. In addition, capacitance-voltage behaviour is also explored by taking the combined effect of gate length and oxide thickness.

2 Device Structure and Simulation Methodology

3D view of GAA SiNW and Gate engineered GAA SiNW MOSFET is shown in Fig. 1a, b, respectively. Gate metal is 15 nm long and consists of two metals $m1$ and $m2$ each as shown in Fig. 1b. The gate metal used at the source is Gold ($\Phi_{m1} = 4.8$ eV) and metal at the drain side is titanium ($\Phi_{m2} = 4.4$ eV). Since both the device consists of silicon nanowire; the radius of nanowire is 5 nm which remains same for both the devices unless stated otherwise. The oxide thickness (t_{ox}) is 1.5 nm. Whereas the source/drain regions are heavily doped with n-type impurities (5×10^{19} cm^{-3}) for both devices and channel is doped with p-type impurity of 1×10^{16} cm^{-3} so that abrupt junction is formed. In this analysis, we have incorporated the quantum model by invoking Bohm Quantum Potential Model in Silvaco [24, 25]. Table 1

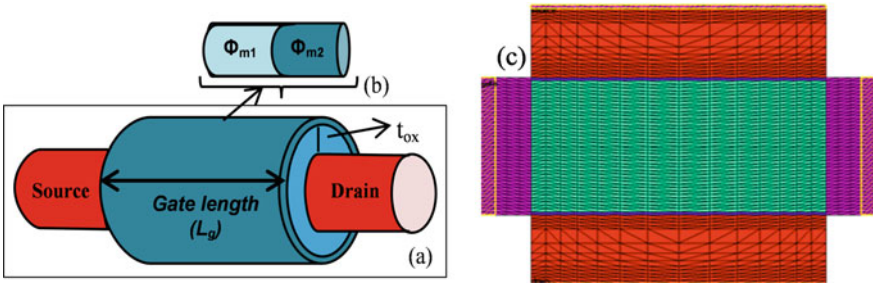

Fig. 1 **a** Schematic view of simulated cylindrical gate SiNW MOSFET, **b** structure of GEWE-SiNW MOSFET and **c** 2D structure showing mesh lines

Table 1 Simulation models

S. No.	Physical models	Description
1	Mobility models	Inversion layer Lombardi CVT mobility model, concentration-dependent mobility, high field saturation model and mobility degradation at interfaces are all included
2	Recombination model	Shockley read hall (SRH) recombination is included to incorporate minority recombination
3	Statistics	Boltzmann transport model. The use of Boltzmann statistics is normally justified in semiconductor device theory
4	Energy transport model	Hydrodynamic model is used as it includes all nonlocal effects and is more accurate than the drift-diffusion method. Drift-diffusion Model show shortcomings as channel length scale down to 50 nm.
5	Quantum mechanical model	Quantum mechanical model plays an important role in determining the performance of surrounding gate MOSFET. We take into account BQP quantum model

shows all the physical and transport models invoked during this analysis. Figure 2 illustrates the calibration graph of simulated SiNW MOSFET with the experimental results obtained by [26]. The result is well calibrated with the reference data, and thus validates the simulation models used in this process.

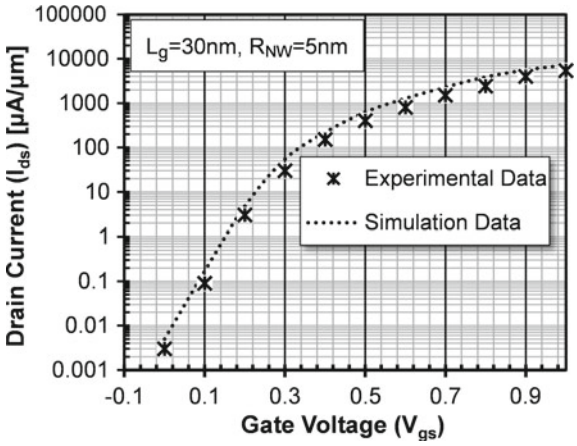

Fig. 2 Calibration of transfer characteristics of simulated GAA SiNW MOSFET with the experimental data of SiNW MOSFET

3 Results and Discussions

3.1 Static Analysis

In this paper, we compare GEWE-SiNW with SiNW MOSFETs in terms of static performance and demonstrated that the proposed device design possesses superior SCE immunity in comparison to conventional SiNW.

As it is evident from Fig. 3a that current driving capability (I_{ds}) and hence transconductance of the GEWE-SiNW increases appreciably compared to SiNW MOSFET. This is due to the incorporation of workfunction engineering which enhances the conduction current density along the source end in comparison to drain end as clearly shown in Fig. 3b. It is also evident from Fig. 3b that current density is more in channel

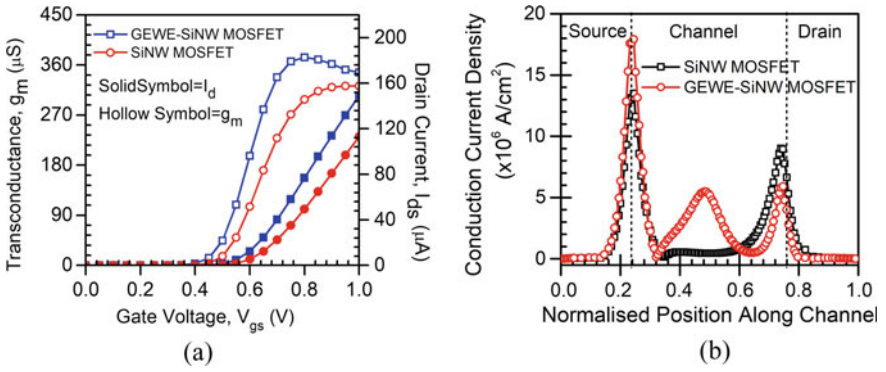

Fig. 3 **a** Drain and transconductance curve at $V_{ds} = 0.2$ V, and **b** conduction current density of SiNW and GEWE-SiNW MOSFETs at $V_{ds} = 0.2$ V and $V_{gs} = 1.0$ V

region which enhances the device efficiency too. Transconductance (g_m) of GEWE-SiNW is larger due to higher mobility of silicon nanowire compared to bulk silicon for the same inversion carrier density. Also, due to amalgamation of GEWE, it improves the conduction density and thus, results enhancement in transconductance.

Figure 4a, b demonstrates the 2D contour plot of surface potential for SiNW and GEWE-SiNW MOSFET at $V_{gs} = 1.0$ V and $V_{ds} = 0.2$ V. It is apparent from contour plots that there is a change in potential in a stepwise along the channel at the interface of M1 and M2 in GEWE-SiNW MOSFET as compared to SiNW. This is due to gate workfunction difference which results in a gradual step change of surface potential in GEWE-SiNW MOSFET as evident from Fig. 4b. This gradual step-change eventually results in suppression of SCEs due to screening of region under metal M1 from drain potential. On the contrary, SiNW shows continuous potential profile in channel region as shown in Fig. 4a.

Moreover, lateral electric field which is an important parameter and decides the short channel performance. It is observed from Fig. 5c that electric field peak is higher at drain end in SiNW as compared to GEWE-SiNW owing to GEWE scheme; it redistributes the field into channel region and thus decreases the field in drain region. This leads to reduced hot carriers in GEWE-SiNW. This same effect is observed

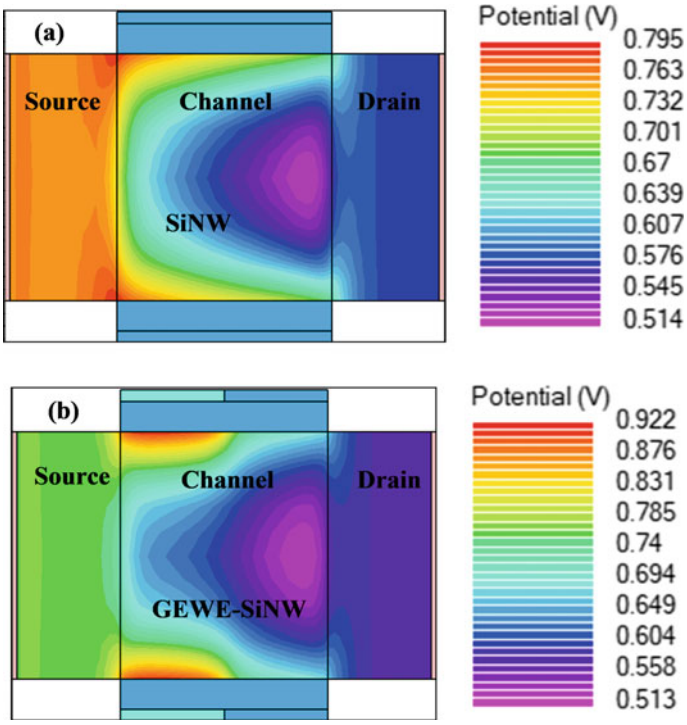

Fig. 4 Contour plot of surface potential distribution for **a** SiNW, and **b** GEWE-SiNW MOSFETs at $V_{ds} = 0.2$ V

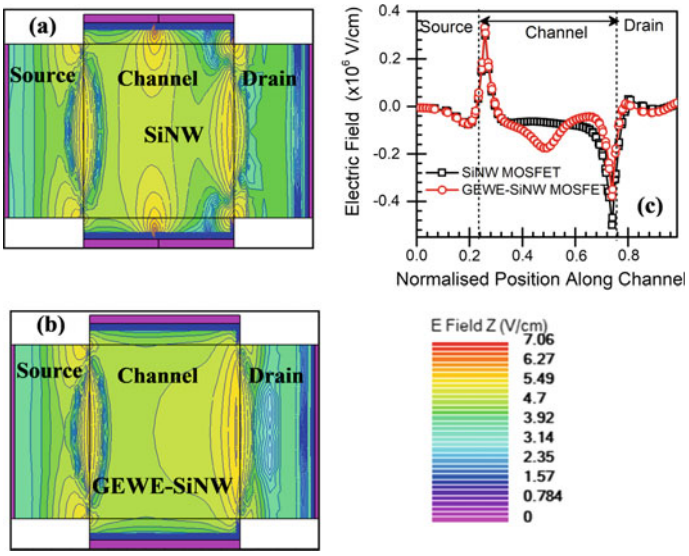

Fig. 5 **a**–**c** Contour plot of electric field distribution for **a** SiNW, and **b** GEWE-SiNW MOSFETs at $V_{ds} = 0.2$ V and $V_{gs} = 1.0$ V. **c** Electric Field along the normalized position of the channel for both devices at $V_{ds} = 0.2$ V

through 2D contour plot shown in Fig. 5a, b. Thus, GEWE-SiNW is more immune to SCEs such as HCEs.

Figure 6a, b shows the contours plots of carrier (electron) temperature along the channel for both SiNW and GEWE-SiNW MOSFET. It is clearly shown in plots that electron temperature is higher in SiNW at drain end due to high electric field at the drain end as seen above in Fig. 5c. On the other hand, due to the reallocation of electric field from drain to channel region therefore, electron temperature is appreciably reduced at drain end in GEWE-SiNW as observed in Fig. 6b. Therefore, this analysis appropriately justifies the effectiveness of GEWE scheme onto SiNW MOSFET and found that GEWE-SiNW is more immune to SCEs in comparison to SiNW.

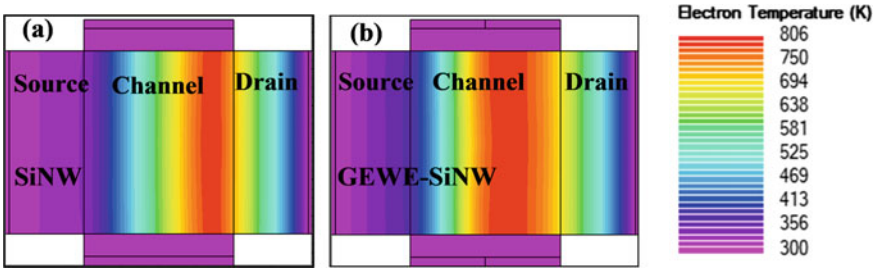

Fig. 6 **a**–**b** Contour plot of electron temperature for **a** SiNW, and **b** GEWE-SiNW MOSFETs at $V_{ds} = 0.2$ V, $V_{gs} = 1.0$ V

3.2 *Optimization of Oxide Thickness and Gate Length on Capacitances*

In order to investigate the capacitance-voltage performance of GEWE-SiNW MOSFET with the optimization of oxide thickness and gate length is performed simultaneously. Figure 7a reflects the gate to drain (C_{gd}) and gate to source (C_{gs}) capacitances with respect to gate voltage, however, Fig. 7b shows the C_{gd} and C_{gs} with respect to drain voltage for oxide thickness of 0.5, 1.5 and 2.5 nm at 10 nm gate length. The accumulation of charge increase with the gate voltage hence C_{gd} and C_{gs} increases and these capacitances are more prominent for lower oxide thickness (0.5 nm) and less for higher oxide thickness (2.5 nm) owing to the variation of distance (d) between charges ($C = \varepsilon_0 A/d$). When drain voltage increases (at constant gate voltage), gate to drain and gate to source capacitances are less prominent although these are slightly higher for lower oxide thickness (0.5 nm) and less for higher oxide thickness (2.5 nm) owing to the variation of distance.

Further, C_{gd} and C_{gs} are shown in Fig. 8a, b as a function of both gate and drain voltage, respectively are evaluated for oxide thickness of 0.5, 1.5 and 2.5 nm at 20 nm gate length. It is found that the values of capacitances are very less (in Atto farad) owing to GEWE architecture which reduces off current and improves on current. However, it is also observed that the capacitances are slightly higher for 20 nm gate length owing to the accumulation of more charge carriers in the channel. This kind of behaviour is also observed previously [27].

Furthermore, the gate to drain and gate to source capacitances with respect to gate voltage and drain voltage has been evaluated for the oxide thickness of 0.5, 1.5 and 2.5 nm at 30 nm (shown in Fig. 9a, b), and 40 nm gate length (shown in Fig. 10a, b). Again it is observed that GEWE-SiNW has very less drain and gate to source capacitances capacitance although the capacitance values are increases with the gate length and oxide thickness. Hence, it is optimized that the 10 nm gate length

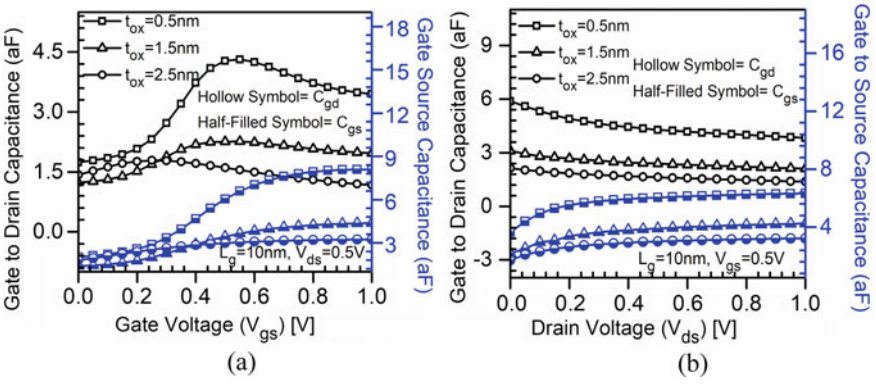

Fig. 7 **a** C_{gd} and C_{gs} with respect to gate voltage; **b** C_{gd} and C_{gs} with respect to drain voltage; at various oxide thicknesses for GEWE-SiNW MOSFET at 10 nm gate length

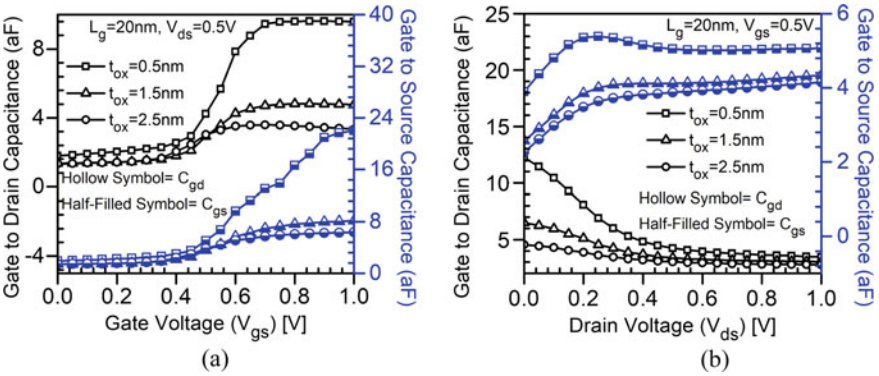

Fig. 8 **a** C_{gd} and C_{gs} with respect to gate voltage; **b** C_{gd} and C_{gs} with respect to drain voltage; at various oxide thicknesses for GEWE-SiNW MOSFET at 20 nm gate length

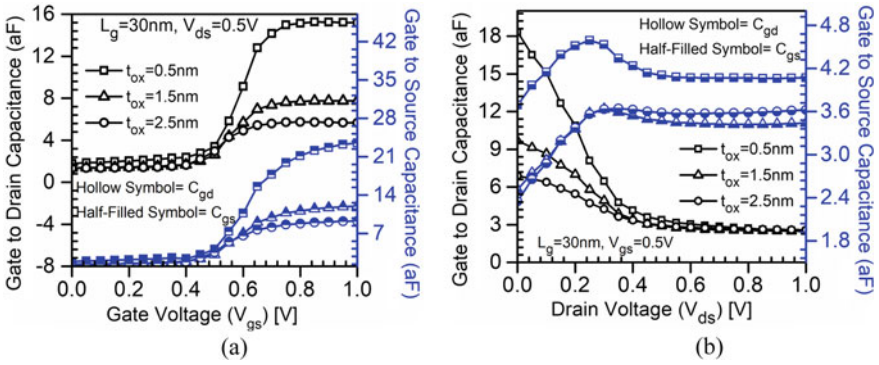

Fig. 9 **a** C_{gd} and C_{gs} with respect to gate voltage; **b** C_{gd} and C_{gs} with respect to drain voltage; at various oxide thicknesses for GEWE-SiNW MOSFET at 30 nm gate length

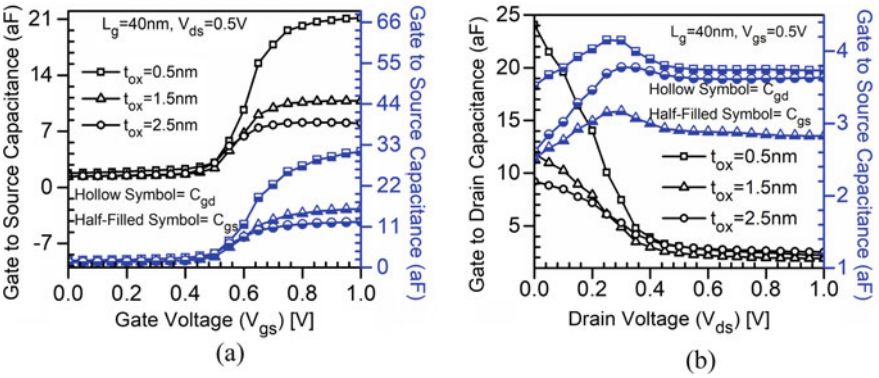

Fig. 10 **a** C_{gd} and C_{gs} with respect to gate voltage; **b** C_{gd} and C_{gs} with respect to drain voltage; at various oxide thicknesses for GEWE-SiNW MOSFET at 40 nm gate length

and 0.5 nm oxide thickness is more suitable in GEWE-SiNW architecture for higher switching performance applications.

4 Conclusions

Static performance of GEWE-SiNW is explored in this paper with an aim to analyze its high performance at room temperature (300 K). It is observed from the simulation results that with the amalgamation of GEWE scheme, current driving capability, and thus transconductance increase significantly due to high conduction current density at the source to channel end. Due to which its static performance also enhances in comparison to SiNW MOSFET. It is also found that in GEWE-SiNW, lateral electric field reduces appreciably at the drain end thus reduces hot carrier effects, and therefore it also impacts electron temperature. Electron temperature at drain end also reduces to 16% in comparison to SiNW. Thus, GEWE-SiNW is more immune to SCEs than SiNW. Furthermore, optimization of gate length and oxide thickness is also examined in terms of capacitance-voltage performance. Results reveal that parasitic capacitance improves noteworthy with gate length 10 nm and oxide thickness 1.5 nm in the inversion region. Thus, it justifies that scaling of dimensions leads to improvement in device performance, and thus find its application in high-performance applications.

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Prediction of Disease Using Machine Learning and Deep Learning

Ch. Aishwarya, K. Suvarchala, B. Aravind, G. Shashank, M. Anand, and N. V. Krishna Rao

Abstract Big data plays an important role in multiple industries, but it has a greater impact and is important to the rapidly growing healthcare industry. Big data plays a crucial role by providing a robust system wherein a better result in disease detection can be achieved. Initially, the predictions are made on the data available, but the lack of incomplete data leads to a reduction in the quality of accuracy. In addition to incomplete data the different characteristics of specific regional diseases, which vary with respect to the region can weaken the prediction more. In this paper, we compare machine learning algorithms and Convolutional neural networks (CNN) to show the increase in efficiency of predictions related to chronic disease outbreaks in communities. We implement and check the efficiency of the proposed models over real-life medical data. To avoid complications that arise due to missing data we use a latent factor model to reconstruct incomplete information. We perform predictions on a regional chronic disease lung infection. We propose a convolutional neural network-based multimodal disease prediction that performs predictions based on both structured as well as unstructured data.

Keywords Convolutional neural networks · Unstructured data · Disease prediction

1 Introduction

The most imperative industry in today's world is the health care industry and it is saturated with information, over 30 billion [1] healthcare transactions a year. Big data analytics in this industry has the potential to provide resolutions to common drawbacks such as inefficiencies in prediction and medication errors. Healthcare industry produces huge volumes of information such as zeta bytes of information taken from medical imaging, EHRs, medical devices and so much more that big data is able to aggregate, organize and manage to improve the entire healthcare industry

Ch. Aishwarya · K. Suvarchala (✉) · B. Aravind · G. Shashank · M. Anand · N. V. Krishna Rao
Department of CSE, Institute of Aeronautical Engineering, Dundigal, Hyderabad, Telangana, India
e-mail: kslrs11@gmail.com

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[2]. The three dimensions of Big data which are velocity, variety and volume are efficiently being utilized by healthcare industries.

The usage of convolutional neural networks for unstructured data has proven to provide good results. Furthermore, the differences in conditions, characteristics and regional climatic and living habit differences increase the complexity. The problem arises in the determination of main, unique characteristics of a disease in a specific region. And a question arises as to how can big data help simplify and provide a better model for more precise predictions.

To solve the above problems, we propose to make predictions based on input attained by the combination of both structured and unstructured data. Initially missing data is handled by reconstructing the missing information by latent factor model. Then after attaining the statistical data we use it to point out and filter the major chronic diseases in the specific region. The attainment of certain features from structured data is done by consultation of a set of experts from the healthcare industry. The unstructured data is handled and the features are automatically detected by using the CNN algorithm. So we propose a CNN based multimodal disease risk prediction. The predictions and results are obtained by the combination of both unstructured and structured data.

2 Literature Survey

This project is basically focused on predicting a particular disease before the occurrence of it. As we know prevention is better than cure, it is very much important to identify a particular disease and follow required guidelines before its intensity increases. So we have come up with an idea of predicting disease before the occurrence of it.

There is already a system existing on how to predict a disease, but it is focused on only datasets that are available in local healthcare communities (structured data). Proposed system mainly focuses on the big data that is widely used nowadays. It uses the multi-model CNN algorithm for a combination of unstructured data and structured data. This algorithmic model basically consists of three layers, i.e. the input layer, hidden layer (can be multiple) and the output layer.

In the input layer, we mainly give the required dataset (structured or unstructured), later in hidden layers, all the preprocessing is done, and finally in the output layer, the disease is predicted. Here, basically, the dataset collected is divided into training data and testing data. Later the algorithm is applied to the training dataset and a model is created, now when the model is ready, the testing data is used to test the model in possible ways.

Finally, when model is ready then it can be used with the real-time datasets. Usage of CNN for different formats of data helps us in attaining better accuracy.

3 Implementation Methodology

The data used in our project is structured and unstructured data and our project are based on classification, here basically for structured we use a dataset consisting of various attributes in form of rows and columns that are required for disease prediction. For unstructured we basically use an image of disease to be predicted.

The image collected should be of required pixels, the dataset considered is initially divided into testing and training dataset. Each of which consists of two categories of images, i.e. One consisting of images having pneumonia and other category is normal images of disease-free lungs. Here basically for structured data we use machine learning algorithms for the processing of the data and predicting the disease. We basically use a Jupyter notebook in this project and import necessary libraries like numpy, pandas, matplotlib, etc. Later, we follow steps of firstly importing dataset, later we try to understand the data by plotting histograms, correlation matrix, etc. We then perform data preprocessing which includes division of categorical variables into the category of numerical values by assigning each value to a particular category, out layer analysis, missing value analysis, removal of null values, etc. This helps us to clean the data, and finally the resultant obtained data is split into training and testing dataset.

Finally, we use the necessary required algorithm like K nearest neighbour, Random forest, Decision tree, etc. We use K nearest neighbour classifier for the predicting of the disease. We can use any algorithm for the same. But according to our research K nearest neighbour classifier gives us the best accuracy. By using any one of the algorithms, we can obtain the required result and plot the graph. This way we can basically predict the disease using machine learning for structured data. Coming to the unstructured data we use any kind of unstructured data like text, images, etc. We use neural networks in this prediction of unstructured data.

Neural networks are basically a term used in deep learning which is used to improve the efficiency of the output in comparison with various machine learning algorithms. Neural networks basically consist of various neurons. For neural networks we basically give input as a collection of features, each one is considered as a neuron. Each neuron is triggered with an activation function, ReLU (Rectified Linear Unit), or sigmoid function is commonly used activation functions.

All the neurons of all the pixels correspond to the first layer of the network and last layer corresponds to the output that is required. The activation value of each neuron in the final output layer consists of numeric values between 0 and 1 and this shows the level up to which the output is matched to the corresponding input. There can be any number of hidden layers and each layer consists of an arbitrary number of neurons. The activation values of these layers are affected by the activation values of the previous layers. As the number of layers increases the number of neurons decreases as after each layer, as the neurons are combined after each layer to get a better output and to ensure a better classification of the problem.

To identify a particular feature or edge at a particular part of the image, we use the activation values and corresponding weights of each neuron and calculate by using the below formula:

$$\sum_{i=1}^{n} w_i a_i$$

The above formula gives us the activation values but we need this value in the range of 0 and 1. So, we use a common function or activation function called the sigmoid function (y), i.e. also known as logistic curve.

$$y = 1/(1 + e^{(-x)}) \tag{1}$$

Here, y is the sigmoid function.

This is a mathematical function that gives us an S-shaped curve also known as logistic curve. This gives us a value near to zero for negative inputs and value near to 1 for positive inputs and suddenly increases if the input is zero.

$$y\left(\sum_{i=1}^{n} w_i a_i\right)$$

So, the activation curve of a particular neuron is a measure of how positive a relevant weighted sum is. Generally, weighted sum is measured with respect to zero and one. If we need to compare with a particular value we can subtract this value from the original formula and check if the weighted sum is greater than the required value generally called bias value. Each neuron in the next layer is connected to all the neurons in the previous layer and finding right weights and bias (b) values helps us in recognizing the particular output effectively.

$$y\left(\left(\sum_{i=1}^{n} w_i a_i\right) - b\right)$$

The above formula represents how the activation function of next layer neurons is calculated using previous layer neuron weights and activation values, we can also use the bias values if required.

General representation

$$a_1 = y(w_0 + b)$$

Thus, it's wrong to say that neuron is a number and is accurate to say that neuron is a function as each neuron in the next layer is made up of the values of functions of the previous layer.

Sigmoid is very difficult to use or operate at some points it is also a slow learner, so we come up with another activation function called ReLU(Rectified Linear Unit). The main objective of ReLU activation function is it takes the input from a neuron in the form of a digit and gives the output as a maximum of that integer and zero. When a neuron takes an input it automatically processes the input and finds the hidden features in it and finally generates the output. In order to train the above weights and bias values of neurons, we need a cost function, this cost function mainly defines the error in prediction of the accurate output. It basically defines how well they obtained output is matched with the required output. The value of cost function is low if the accuracy of prediction is high and vices versa. The cost function is calculated by adding up the squares of differences between the activation values and the values you want to obtain for each neuron, i.e. by using Mean Squared Error formula (MSE represented as x).

$$x = \left(\sum (\text{predicted value - actual value})^2\right) * \frac{1}{N}$$

where N is the number of observations.

The bias values define if a given function is active or inactive. The above cost function formula gives is non-convex and gives us multiple local minima values, in order to obtain a single value we need to use convex function. In order to minimize the cost function, we use gradient descent of the cost function. Gradient descent is a technique to minimize the weights (w) and bias values (b) which lead to the minimization of the cost function. The cost function of logistic regression is convex in nature and has one global minima so it is chosen over the mean squared error method which has multiple local minima.

The steps for gradient descent are as follows:

- Give initial values of w and b as zeros.
- Move towards steepest downhill direction.
- Repeat the above process until global minima are obtained.

Generally, for calculating the global minima of the gradient descent we use the slope of the input. If the input slope is low the shift towards right else shift towards left till the required minima are obtained.

The gradient of intercept $y(x)$ is calculated as

$$\mathrm{d}y/\mathrm{d}x(x) = 0$$

In general, it is calculated as:

$$y(x) = \frac{\mathrm{d}y}{\mathrm{d}x}$$

In case if we consider multivariable plane then, we consider the gradient [3] of the multivariable which gives us the direction of the steepest ascent, taking the

direction for negative value of the function decreases the function and for positive values, it increases the function. Repeat this again and again until the cost function is minimized. This cost function is basically average of all of the data and if we minimize it works well with all the data available. The algorithm which can be used to compute this gradient efficiently and is the heart of how neural network works is backpropagation algorithm [4]. The below is nonconvex cost function which may result in multiple local minima:

$$l(y_1, y) = \frac{1}{2}(y_1 - y)^2$$

So, we use the below gradient function to make it convex which may result in a single global minima:

$$l(y_1, y) = -(y \log y_1 + (1 - y) \log(1 - y_1))$$

The logistic regression cost function for entire training set can be considered as

$$J(w, b) = \frac{1}{m} \sum l(y_1, y)$$

Some of the results of the gradients of different combinations [5] of weights and biases may result in a huge change in cost function and some may lead to a lesser change of the cost function. So, making many changes in these combinations of weights and biases may lead to the establishment of a final output layer and with a minimum cost function but we cannot guarantee how well this model may work for different kinds of real-time input. So, we consider various models or algorithms like CNN, LSTM, RNN, etc. which would improve the quality of the designed neural network and give us a proper output. Basically, we can increase the accuracy [6] of obtaining the output by using backpropagation algorithm. This means that we can focus on the weights and biases of the previous layer neurons which have maximum effect on the activation value of the present layer neuron and we can try to adjust different combinations of weights and biases to ensure accuracy and decrease the possibility of errors. We consider this backpropagation process from second layer to the final layer and take the average of all the values which is considered as negative gradient.

This kind of shuffling [7] would take very long for a [8] larger training data. So, we divide this large training data into mini-batches and compute the gradient of these batches using backpropagation method. Each batch gives a significant computational speedup and very good approximations. If we plot the trajectory of network under the cost function we would observe a great steepness falling downhill [9] at a faster pace. This technique is called stochastic gradient descent.

4 Algorithm

Algorithms used for structured data we use different machine learning algorithms like KNN, decision tree, etc. CNN unimodal for unstructured data and CNN multi-modal for a combination of structured and unstructured data [10]. The process of obtaining predictions using the general, i.e. traditional risk models is done by machine learning algorithms, a supervised learning algorithm.

The data is divided into training and test data. The dataset taken consists of various attributes like sex, age, heartbeat rate, etc. To increase efficiency, we can classify the patients in test set as high-risk or low-risk. With the advancement in therapeutic information, obtaining the electronic wellbeing records is very advantageous. Information being available on such easy basis, opened up multiple easy methods to accumulate the wellbeing related information with the help of heterogeneous vehicular systems. Information related to patients such as test results, patient measurable data, or sickness history is generally recorded by the EHR.

This data will help us find some potential information and the answers driven by this information thus reducing the expenses of analyses. Qiu et al. also proposed an idea for the calculation for the optimal value to determine an optimal huge information sharing to help deal with entangle information collection.

One important application would be to recognize the patients with high-risk which will help reduce the medicinal cost as the high-risk patients generally need expensive human services.

Here, in CNN, i.e. in convolutional neural networks the input is taken and is converted and processed between layers as shown above process and after the processing through the different layers of neural network. The output obtained is taken as input for different algorithms like CNN, LSTM, RNN, etc. for further improvement in accuracy of prediction of the output. Generally, in CNN algorithm [11] if the text is taken as input the words of a text are represented as a vector can also be called as implanting natural language processing and the convolutional layer takes the first word and the last word from the vector and the weights and biases are adjusted in a better accurate manner to get a better activation value [12] through a proper activation function. There is a pool layer and a CNN classifier after a convolutional layer, the pool layer finds the words having a very crucial role, i.e. it finds the most important words and ignores the words that do not play a crucial role in classification, various features are identified after the processing of input from the pooling layer and convolutional layer and is given as input to the classifier for classification [13].

The above process is done in CNN unimodal and in CNN multi-modal uses both unstructured and structured data and is based on CNN unimodal, here we extract features separately for structured data and unstructured data and it follows the same process as CNN unimodal. This is divided into two parts, i.e. training the text and structured data and testing it separately [13].

The following diagram is a flow chart designed to show the algorithmic flow (Fig. 1) in traditional as well as in the modern method.

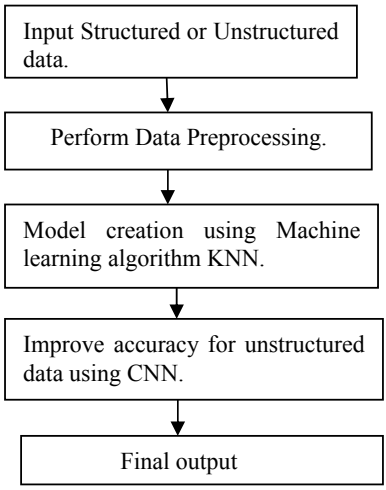

Fig. 1 Flow chart representing flow of machine learning and neural networks algorithms

5 Analysis of Performance and Results

Performance of different algorithms of machine learning compared with each other the KNN algorithm provides us the best accuracy. Coming to CNN, provides us better accuracy than machine learning models.

The CNN model created has a great variant in the prediction compared to normal machine learning algorithm. The performance is analyzed based on various factors like the running time, the amount of missing values, number of iterations, number of proper (Figs. 2 and 3).

Coming to CNN we are using VGG16 or VGG19 framework, which is a type of CNN. Here, we take x-ray of any disease as input and adjust the required pixels. We load the dataset as input consisting of images and divide it training and testing data. We later perform data preprocessing. Here we are using Keras framework with tensorflow as backend, Keras is an open-source framework used to improve the accuracy. We use RGB channel of images (image size path) and also consider the dimensions of RGB. We then ensure that all the layers are not trained and find the number of classes that are present in the trained dataset. We then flatten the between layers and finally create a last output layer to capture the prediction. Now, we compile by using the optimizer and accuracy and tell the model the cost and optimization method to use. Now upload the dataset, insert images and train data and run it. Finally, the classified output is obtained. Here in the output of CNN model 1 represents that the disease has occurred and 0 represents the disease is not occurred (Figs. 4 and 5).

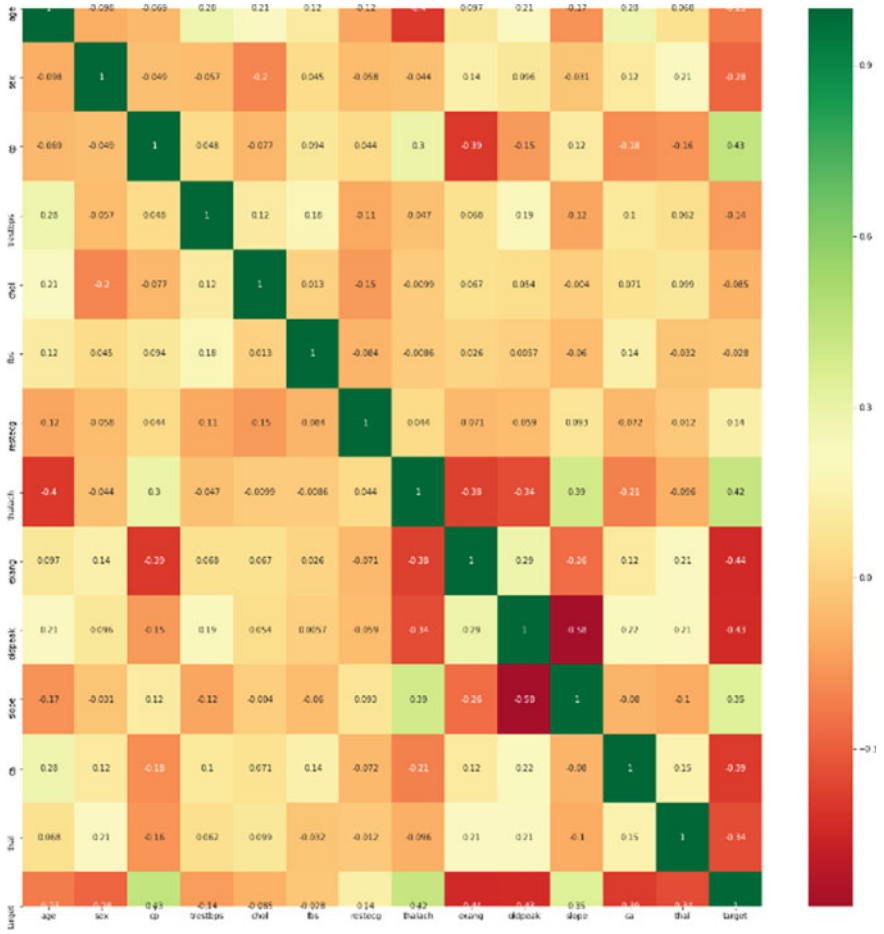

Fig. 2 Feature scaling output

6 Conclusion

Health sector is a very important sector these days and it is very important to predict the occurrence of a disease and cure it. All the existing systems work with either structured or unstructured data. So, we propose a machine learning and neural network-based multimodal disease risk prediction algorithm that uses a combination of both structured.

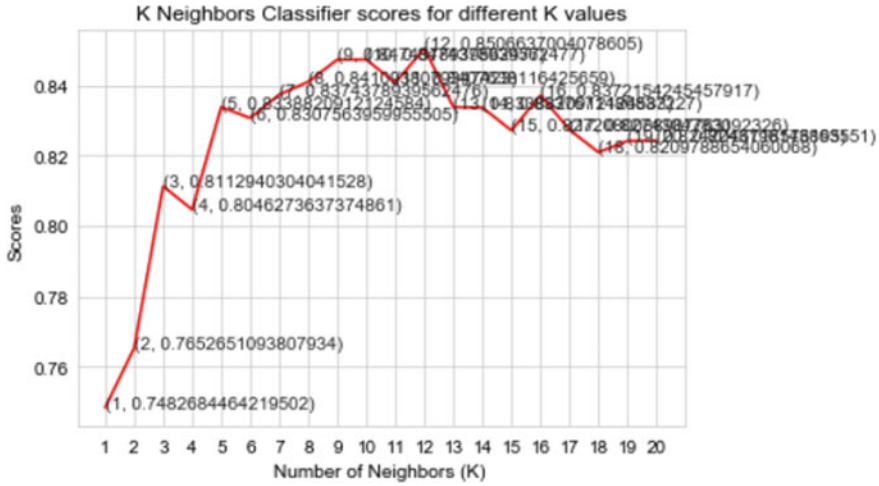

Fig. 3 KNN output graph plot

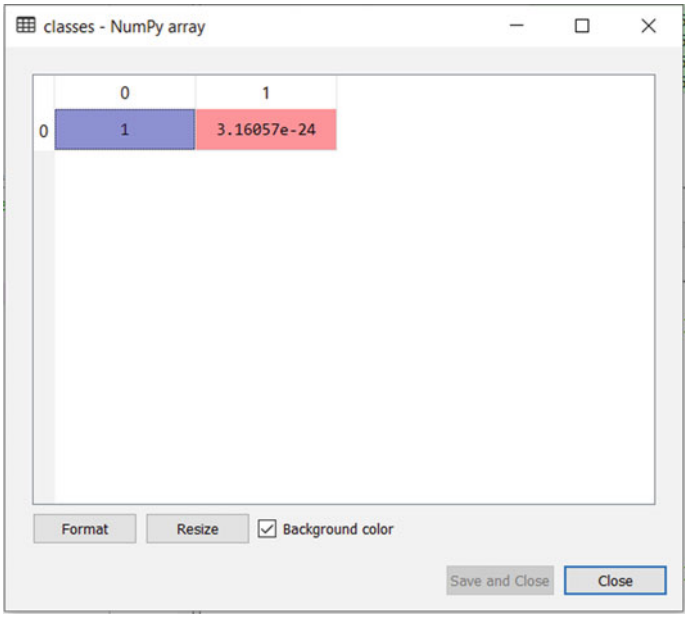

Fig. 4 CNN predicted output for classification (here the absence of disease is shown)

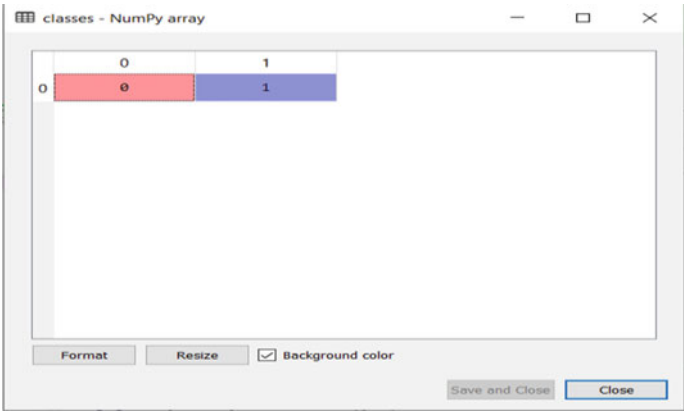

Fig. 5 CNN predicted output for classification (here the presence of the disease is shown)

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Effect of Source, Drain and Channel Spacing from Gate of HEMT

Shashank Kumar Dubey and Aminul Islam

Abstract This paper presents an AlGaN/GaN HEMT on 6H–SiC substrate. The impact of horizontal optimization of gate terminal with source-to-gate spacing and drain-to-gate spacing on DC and RF characteristic of the high-electron-mobility transistor (HEMT) and impact of vertical optimization of gate terminal with recessing have been represented in this paper. The 1.25×/1.32×/1.204× improvements in the drain current/transconductance/gate-source capacitance have been reported as the source-to-gate spacing varied from 1.833 to 0.633 μm. The 0.78× decrement in the ON-resistance of the device has been recorded as the drain-to-gate spacing varied from 3.327 to 1.327 μm. The recessing of the gate resulted in a 2.45× increment in the transconductance at the cost of severe decrement in the drain current as the recessing depth varied from 0 to 22 nm.

Keywords HEMT · Source-to-gate spacing · Drain-to-gate spacing · Recessed gate

1 Introduction

With the rise in demand for RF and microwave technology in the last couple of decades, the conventional semiconductors could not meet the demand due to various limitations in their high frequency and high-power applications. This has paved up the way for wide bandgap materials like GaN, SiC, etc. Among these, GaN-based heterostructure devices have shown great potential for the present and upcoming high power and microwave frequency application. This is because of its remarkable physical and electrical properties like high breakdown electric field, high saturation velocity and electron mobility. The breakdown field of GaN devices is about ten times

S. K. Dubey · A. Islam (✉)
Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra, Ranchi, Jharkhand, India
e-mail: aminulislam@bitmesra.ac.in

S. K. Dubey
e-mail: dubey.shashank1991@gmail.com

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higher than that of Si devices, observed as high as 3.3 MV/cm. Further, improvement in the breakdown voltage and high-temperature operation capability is achieved with the introduction of wider bandgap semiconductor material SiC. High electron mobility transistor (HEMT) is a field-effect transistor where a channel is formed by a junction formed by two different wide bandgap materials. In case of GaN HEMTs, GaN is the thick epitaxial layer over which resides the thin barrier layer, and a highly mobile two-Dimensional Electron Gas (2-DEG) is present at the heterointerface [1]. Due to their highly linear performance at high frequency, GaN-based HEMTs are widely utilized for high-power applications, RF applications like cellular telecommunications, imaging, RADAR and radio astronomy. Low noise amplifiers, oscillators and mixers are designed using GaN HEMTs attributing to their low noise and better high-frequency performance [2].

Due to technical advancements, HEMT devices have been used extensively for modelling of powerful devices because of its high-speed switching operations [1, 2]. These devices with high cut-off frequency are also widely used for power electronics applications such as power conditioning and microwave transceiver for communications [3]. The term high-electron mobility in HEMT signifies the higher mobility the electrons exhibit in the HEMT devices in comparison to that of other transistors, e.g. MOSFETs. The electrons from the heavily doped wide bandgap material diffuse into the undoped narrow-bandgap material and form a channel. Since, the channel is isolated from the area where the electron concentration is in bulk thus, HEMTs exhibit higher mobility. The AlGaN/GaN-based HEMT shows better performance than others on account of its existing material characteristics such as high-electron density, high breakdown voltage, large electric breakdown field (1.5×10^7 V/m, as compared to 2.5×10^5 V/m of GaAs), high-electron mobility (1000 $cm^2V^{-1}s^{-1}$), high-electron saturation velocity (1.5×10^7 cm/s) and large bandgap energy (3.42 eV, as compared to 1.4 eV of GaAs) [4–7]. The AlGaN/GaN HEMT has high spontaneous and piezoelectric polarization, which gives a two-dimensional electron gas (2-DEG) with electron density of about 10^{13} cm^{-2} for Al content in the range of 30–40% in barrier layer, without the need of the doping. Moreover, the GaN-based device gives 50× higher power capacity than the GaAs-based device [8].

HEMT devices find wide applications in the fields of imaging, radio astronomy, wireless communications, military (missile, RADAR seeker) applications, mobile communication and short-wavelength lasers and LEDs, radio detection and ranging (RADAR) [3, 4, 7]. HEMT-based devices are formed by combining hetero-materials (i.e. junction between two materials with different bandgaps and nearly equal lattice constants). When AlGaN and GaN materials are brought close to each other, a spontaneous polarization [9] occurs that leads to trapping of electrons in the narrow-bandgap material referred to as 2-DEG thereby forming a conducting channel [4]. Thus, AlGaN/GaN HEMT devices exhibit 2-DEG without doping. The key reason behind the formation of potential well (i.e. 2-DEG) at the interface is the mismatch of the lattice constants of AlGaN and GaN which eventually results in the piezoelectric polarization [10]. The potential well forms channel in which electrons flow. The HEMT is a three-terminal device namely source, drain and gate terminals. The electrons flow from the source to the drain. The source and drain terminals form

the ohmic contact whereas, the gate terminal forms the Schottky contact. The gate terminal is a terminal which controls the movement of carriers by varying the channel width.

The proper distances of source and drain with respect to gate are of great importance as they affect the performance of the device [11]. The source-to-gate spacing influences the drain current by varying the source resistance and impacts the transconductance while the threshold voltage remains almost the same. It also influences the gate-source capacitance and cut-off frequency of the HEMT device. The drain-to-gate spacing affects the breakdown voltage [12] which as a result impacts the ON-resistance. The recessing of gate is also an important technique to optimize the DC performance of a HEMT device.

The contribution of this work is as follows

- This paper studies impact of gate-to-source spacing to optimize the DC parameters such as drain-to-source current (I_D) and transconductance (g_m).
- It also examines effect of gate-to-drain spacing to optimize the ON-resistance of the device.
- It investigates the impact of gate recessing on the DC parameters such as drain-to-source current (I_D) and transconductance (g_m).

The entire work has been ordered as follows: Sect. 2 presents the structure of the proposed device. The simulation results are discussed in Sect. 3. The paper is finally concluded in Sect. 4.

2 Device Structure

The simulated device was modelled on a 6H-SiC substrate shown in Fig. 1. A 23-nm heavily doped and wide bandgap barrier layer of AlGaN was designed above the 2-μm channel layer of undoped and narrow-bandgap GaN. Since, there exists a lattice mismatch between GaN and 6H–SiC, a thin nucleation layer of AlN was designed. The fraction of Aluminium in the AlGaN barrier layer was 0.22. Moreover, a 3-nm GaN capping layer was designed on top of the AlGaN barrier layer to reduce the gate leakage current.

3 Simulation Results and Discussion

3.1 Effect of Source-to-Gate Spacing

Figure 2 illustrates the effect of source-to-gate spacing L_{SG} on the drain current of the device. The drain current has been observed to increase as the L_{SG} decreased. The increase in drain current with the decrease in L_{SG} occurs since [13]

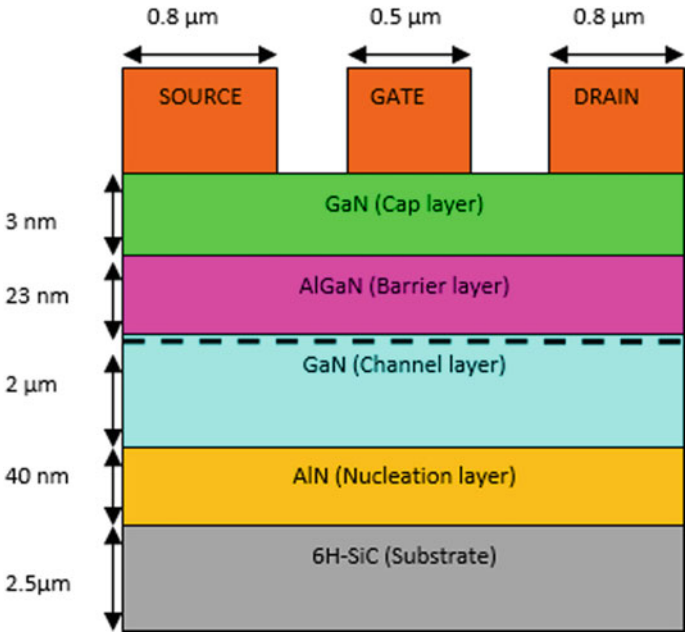

Fig. 1 The simulated proposed AlGaN/GaN HEMT on 6H-SiC

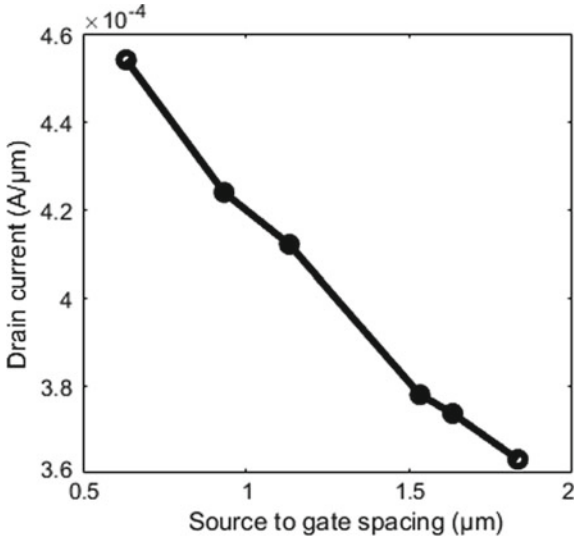

Fig. 2 Drain current versus source-to-gate distance

$$I_D = \frac{V_{DS}}{2R_C + R_S + R_D} \tag{1}$$

where V_{DS} is drain-to-source voltage, R_S is the source resistance, I_D is drain current, R_C is channel resistance and R_D is drain resistance. Thus, if R_S can be made smaller, the I_D can be made larger. The idea to decrease R_S is in accordance with the following relation given by

$$R_S = \frac{L_{SG}}{qn_0\mu_0} \tag{2}$$

where L_{SG} is source-to-gate spacing, n_0 is electron concentration, μ_0 is electron mobility. Thus, by decreasing the L_{SG}, we have improved the drain current of the HEMT device. The threshold voltage (V_t) is found to vary from −1.6 to −1.5 V as L_{SG} is decreased from 1.833 to 0.633 µm. Thus, analyzing a typical transfer characteristic curve, it is evident that higher currents obtained with downscaled L_{SG} where the V_t effectively remains the same lead to a high transconductance g_m. This effect can be seen in Fig. 3.

The increase in the gate-source capacitance C_{GS} with the reduction in L_{SG} occurs since as source and gate terminals are kept closer, the capacitance increases, and this is shown in Fig. 4. The cut-off frequency f_T remains almost the same as C_{GS} and g_m both increase with the reduction of L_{SG} as

$$f_T = \frac{g_m}{2\pi(C_{GS+}C_{GD})} \tag{3}$$

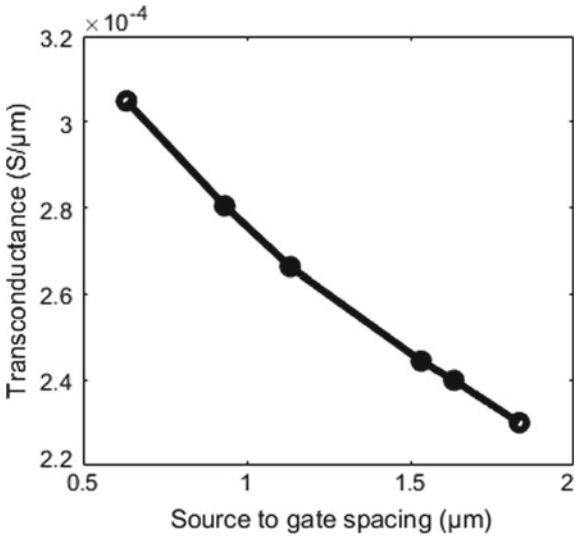

Fig. 3 Transconductance versus source-to-gate distance

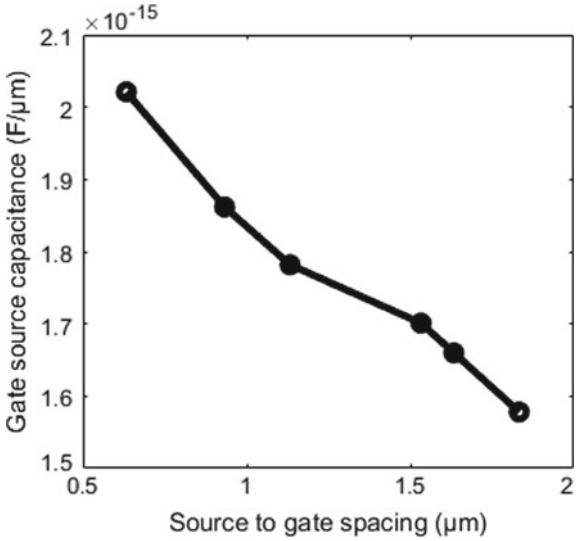

Fig. 4 Gate source capacitance versus source-to-gate distance

Therefore, the increase in g_m and C_{GS} compensate for any change in the f_T. This is shown in Fig. 5. As can be observed from Table 1, the I_D increases as L_{SG} decreases.

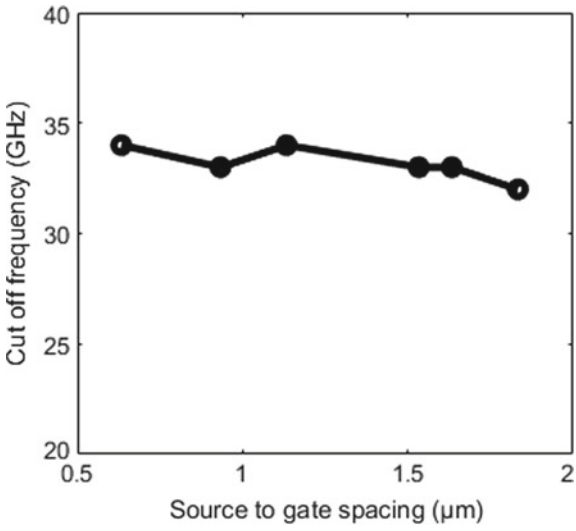

Fig. 5 Cut-off frequency versus source-to-gate distance

Table 1 Effect of L_{SG} on DC response

L_{SG} (μm)	I_D (A/μm)	$g_{m\,max}$ (S/μm)	$C_{gs\,max}$ (fF/μm)
1.833	0.00036312	0.00023	1.678
1.633	0.00037376	0.000239	1.6769
1.533	0.00037874	0.000244	1.711
1.133	0.00041195	0.000266	1.7818
0.933	0.00042379	0.00028	1.9618

3.2 *Effect of Drain-to-Gate Spacing*

Our investigation on variation of drain-to-gate spacing (L_{DG}) reveals that the drain current is mostly not affected. As the g_m and C_{GD} remain unaffected due to the variation in L_{DG} the f_T remains unchanged. The impact of L_{DG} variation on the RF performance of the device is reported in Fig. 6.

As can be visualized from the figure, the cut-off frequency remains almost unchanged even though the L_{DG} is downscaled from 3.327 to 1.327 μm. The effect of L_{DG} variation on the DC parameter such as ON-resistance of the device is reported in Fig. 7. As can be seen from Fig. 7, the ON-resistance increases as the L_{DG} increases. The increased L_{DG} increases the breakdown voltage [14]. The breakdown voltage V_{BR} impacts on ON-resistance R_{ON} of the device [15] as

$$R_{ON} = \frac{4V_{BR}^2}{\varepsilon_S \mu_n E_c^3}. \tag{4}$$

where V_{BR} is the breakdown voltage, E_c is the critical electric field, μ_n is the mobility of electrons and ε_S is the permittivity of the semiconductor.

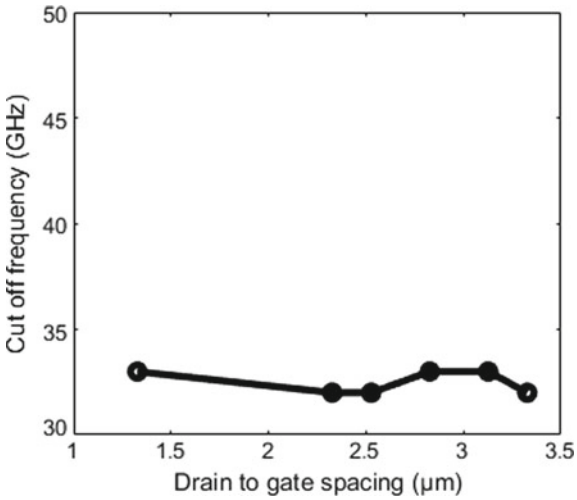

Fig. 6 Cut-off frequency versus Drain-to-gate distance (L_{GD})

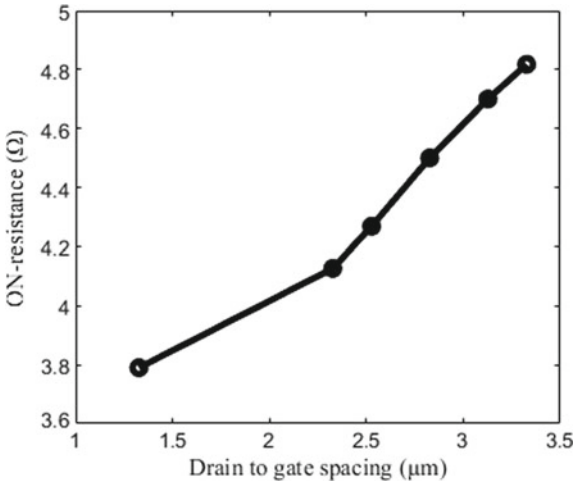

Fig. 7 ON-resistance versus Drain-to-gate distance (L_{GD})

3.3 Impact of Gate Recessing

The impact of position of the terminals in a direction parallel to channel has been discussed earlier in this paper. The position of a gate terminal in a direction perpendicular to the channel is also important as it changes the characteristics of the device. In this work, the gate to channel spacing is varied from 0 to 22 nm to observe its effect on transconductance, drain current and electron concentration in the channel. The results of this investigation are plotted in Figs. 8 and 9.

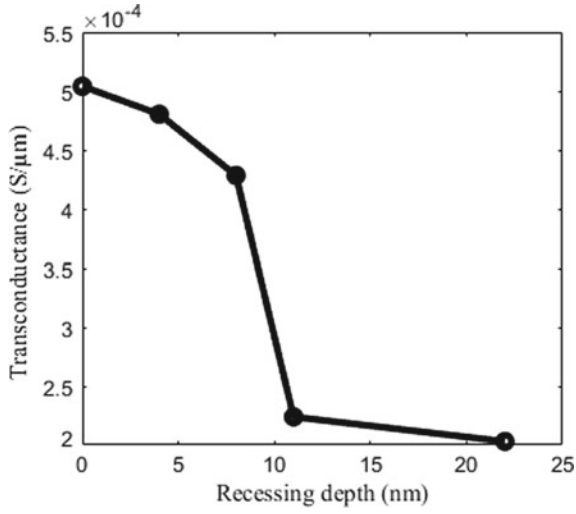

Fig. 8 Transconductance versus different recess depth

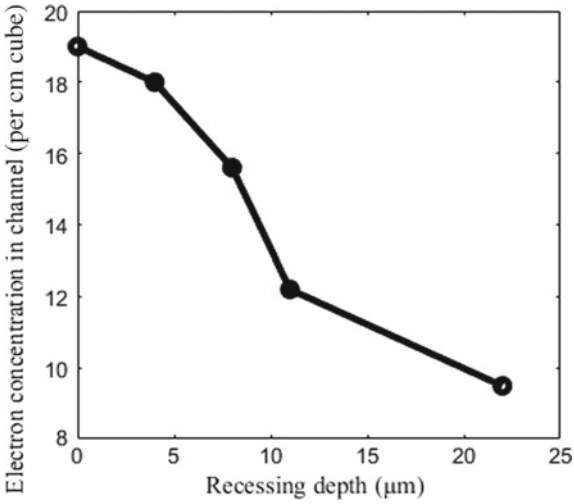

Fig. 9 Electron concentration in channel versus recessing depth

Figure 8 shows the transconductance versus recess depth curve. The transconductance increases as the recess depth increases. This is because the gate terminal has better control over the two-dimensional electron gas (2-DEG) as the gate to channel distance reduces. The same is modelled by [15]

$$g_{\mathrm{m}} = \frac{\varepsilon_0 \varepsilon_{\mathrm{r}} v_{\mathrm{eff}} W}{h} \tag{5}$$

where g_{m} is transconductance, v_{eff} is the effective velocity, W is the device width and h is the gate channel separation. The recessing of gate is done in order to achieve small h. The layer under the gate foot is cut and gate terminal is extended into it. This leads to a decrease in h those results in an increase of g_{m}. However, higher transconductance is obtained at the cost of lower drain current. This reduction is justified by the decreased electron concentration in the channel with deeper recessing of gate as shown in Fig. 9. Since the role of a gate terminal is to deplete the channel having the carriers, therefore, deeper recessing gives the gate a better control over the channel and increases the depletion.

4 Conclusion

This paper presents the impact of source-to-gate spacing and drain-to-gate spacing on DC and RF performance of the HEMT. The impact of recessed gate has also been reported. Thus, this work reports in brief about the source, drain and gate terminal designing of the HEMT.

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SFS/PI Approach for AGC of Two Area Interconnected Thermal Power System

Rita Saini, Girish Parmar, Rajeev Gupta, and Afzal Sikander

Abstract In this paper, stochastic fractal search (SFS) algorithm has been applied for optimal tuning of the parameters of two dissimilar PI controllers in automatic generation control (AGC) of interconnected thermal power systems with ITAE as objective function. The performance of the proposed SFS tuned PI controller for the same has also been compared with some popular techniques existing in the literature. From the simulation results, it has been found that the PI controllers optimized/tuned by the SFS produces less ITAE value, settling times, smooth dynamic response, less oscillations, and fast dynamic response when compared with some popular approaches in the literature for the same considered system and ITAE.

Keywords Automatic generation control (AGC) · Load frequency control (LFC) · Interconnected thermal power system · PI- controller · Stochastic fractal search (SFS)

1 Introduction

The necessity of an intelligent multi-area interconnected power system had been found in [1, 2] which controls the load deviations and system disturbances and provides enhanced power quality.

R. Saini (✉) · G. Parmar · R. Gupta
Department of Electronics Engineering, UTD, RTU, Kota, Rajasthan 324010, India
e-mail: ritasaini.ece@gmail.com

G. Parmar
e-mail: girish_parmar2002@yahoo.com

R. Gupta
e-mail: rajeev_eck@yahoo.com

A. Sikander
Department of Instrumentation & Control Engineering, Dr. B. R. Ambedkar National Institute of Technology, Jalandhar, Punjab, India
e-mail: afzals@nitj.ac.in

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Further, the power system is governed by a control mechanism known as "automatic generation control (AGC)", which is used to maintain a balance for generation and system load at low cost, control the interchanges of power and control frequency and tie-line power deviations, etc., [3–5].

. In each area of AGC for interconnected power systems, a controller is used to achieve the above objectives. The comparison for the performance of various controllers in AGC has already been given [6–10].

Numerous soft computing techniques have already been dealt in the literature for optimal tuning of controllers' parameters in AGC of power system such as; BFOA tuned PI with governor dead-band nonlinearity [11, 12], ICA-tuned PID [13], DE tuned PI [14], Classical frequency controllers tuned by DE for MAMS-PS [15], TLBO-tuned I and TLBO-tuned PID for MUMS-PS [16], Emotional Learning based controllers [17], Firefly Algorithm (FA) for controlling the frequency changes in interconnected AGC [18], Artificial Bee Colony (ABC) algorithm for AGC [19], GSA tuned PID & GSA tuned FOPID [20], and *h*GWO-PS based 2DOF-PID for AGC of two/three area interconnected thermal–thermal and hydro-thermal power system [21–23].

In the present work, SFS [24, 25] has been employed to optimize/tune the parameters of PI controller of dissimilar characteristics in AGC of interconnected non-reheat thermal power system. The optimization of PI controllers using SFS has been abbreviated as SFS/PI approach throughout the paper. The proposed approach produces far better results while comparing it with some available approaches in the literature.

2 Background Concepts

The background concepts behind the present work have been discussed as follows:

2.1 Mathematical Modeling of Two Area Interconnected Thermal Power System

In the present work, a block diagram of the aforesaid power system has been considered (see Fig. 1) [4, 6, 10, 16, 21–23]. The Details about theory and mathematical modeling of the proposed system can be found in the aforesaid literature [4, 6, 10, 16, 21–23].

2.2 Proportional-Integral PI Controller

The transfer function of PI controller (in Fig. 2) is given as

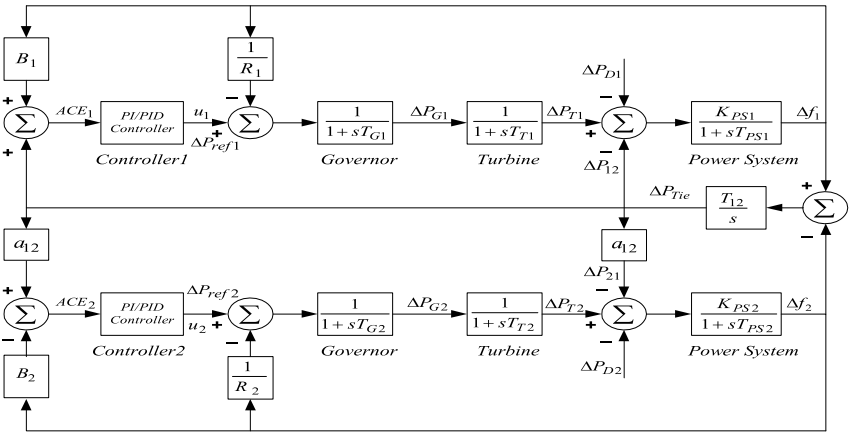

Fig. 1 Two area interconnected thermal power system

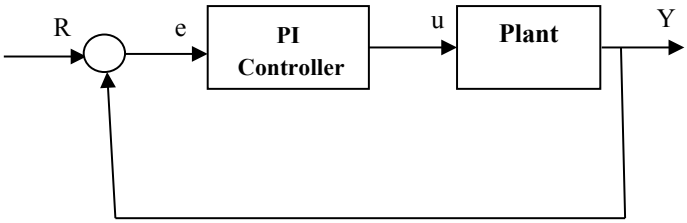

Fig. 2 PI- controller in closed-loop control system

$$T(s) = K_{\mathrm{P}} + \frac{K_{\mathrm{I}}}{s} \tag{1}$$

The block diagram of closed-loop control system with PID controller is shown in Fig. 2.

3 Objective Function and Constrained Optimization Problem

In the present work, the ITAE performance index has been used as an objective function, given by [21–23]:

$$F = \mathrm{ITAE} = \int_0^{t_{\mathrm{simulation}}} w_1 \cdot (|\Delta f_1| + |\Delta f_2| + |\Delta P_{\mathrm{Tieline}}|) \cdot t \cdot \mathrm{d}t \tag{2}$$

where $t_{\text{simulation}}$ is simulation time.

Minimize F

Subject to

$$K_{\text{P}_{\text{mn}}} \leq K_{\text{P}} \leq K_{\text{P}_{\text{mx}}}, K_{\text{I}_{\text{mn}}} \leq K_{\text{I}} \leq K_{\text{I}_{\text{mx}}} \tag{3}$$

where $K_{\text{P}_{\text{mn}}}$, $K_{\text{P}_{\text{mx}}}$ and $K_{\text{I}_{\text{mn}}}$,$K_{\text{I}_{\text{mx}}}$ are the minimum and maximum value of the controllers' parameters, which lie in the range $[-2, +2]$.

4 Stochastic Fractal Search Algorithm

SFS utilizes the property of diffusion present in random fractals to discover the search space. There are three main processes in SFS named initialization, diffusion and update and these steps of mathematical modeling for SFS can be found in [24, 25]. The optimization process of SFS has been stepwise explained in flow chart shown in Fig. 3. In order to simulate the SFS algorithm, the parameters are given in Table 1.

5 SFS for AGC of Two Area Interconnected Thermal Power System

For simulating the proposed SFS/PI approach for AGC of investigated power system in MATLAB/SIMULINK, area 1 is disturbed with step load perturbation (SLP) of 0.1 p.u. Number of "SA" (search agents) as 20 and number of iterations "I" as 50 are considered for simulation. The SFS is run 10 times among which the best final solution corresponding to the lowest ITAE value is selected as the proposed PI controllers' parameters (optimal parameters). The obtained parameters of PI controllers by SFS are given in Table 2.

ACE, Δf_1, Δf_2 and ΔP_{Tie} have been shown in Fig. 4 for SFS/PI approach which shows that the SFS/PI approach for the system under investigation produces better dynamic responses in terms of less settling times, fast and smooth response.

6 Results and Discussions

The comparison of optimal parameters, ITAE, system dynamic responses, and settling times of Δf_1, Δf_2 and ΔP_{Tie} are discussed below.

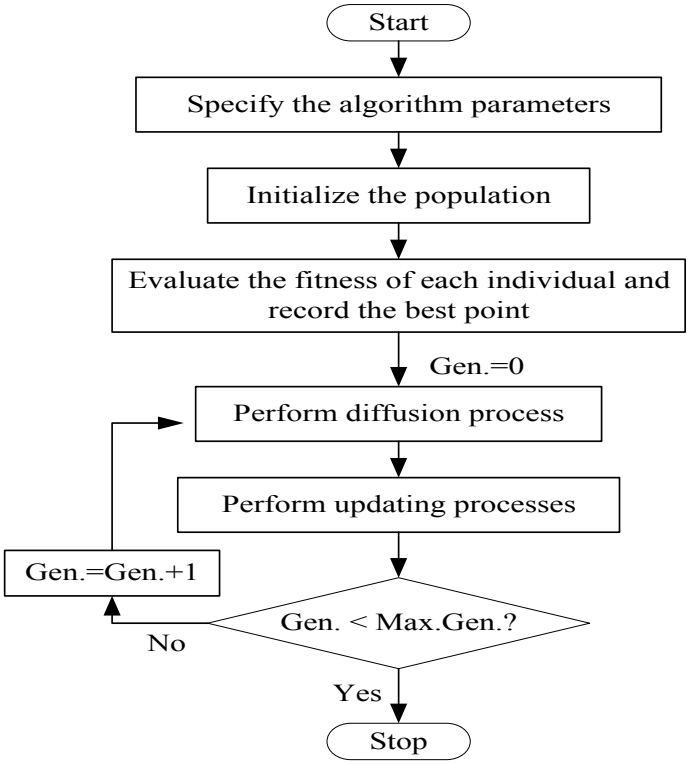

Fig. 3 Flow chart of SFS

Table 1 Parameter used for SFS algorithm [23]

Parameter	Value
Number of search agents (population)	30
S. diffusion	2
S. walk	0.75
Maximum iterations	30
Lower bounds	[0.001 0.001]
Upper bounds	[20 20]

Table 2 Obtained parameters of PI vontrollers by SFS

Controller/Area	K_P	K_I
PI/Area 1	1.2005	1.9611
PI/Area 2	1.0542	1.9611

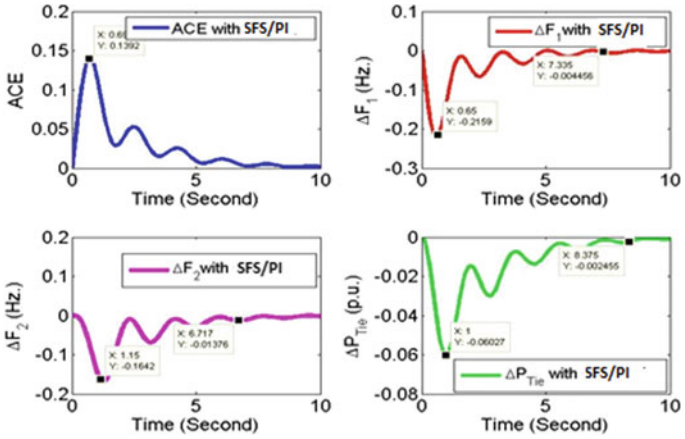

Fig. 4 ACE, Δf_1, Δf_2, and ΔP_{Tie} with SFS/PI approach

Table 3 Optimal parameters of PI/PID controllers obtained with various approaches

Algorithm/Controller	Optimal controllers' parameters
DE/PI [14]	$K_{\mathrm{P1}} = -0.3972$; $K_{\mathrm{I1}} = 0.4021$
PSO/PI [8]	$K_{\mathrm{P1}} = 0.4048$; $K_{\mathrm{I1}} = 0.4040$
PSO/PID [8]	$K_{\mathrm{P1}} = 0.4096$; $K_{\mathrm{I1}} = 0.4906$; $K_{\mathrm{D1}} = 0.4105$
SFS/PI (Proposed)	$K_{\mathrm{P1}} = 0.0125$; $K_{\mathrm{I1}} = 0.3765$

6.1 Comparison of Optimal Parameters

The optimal parameters of PI controllers by SFS for the aforesaid system have been given in Table 3 in which the optimal parameters obtained by other popular approaches are also mentioned for fare comparison.

6.2 Comparison of ITAE

A comparison of obtained ITAE value with different existing popular approaches has been given in Table 4. From which, it is said that SFS/PI approach produces the lowest value of ITAE (ITAE = 1.1763) in comparison to other existing approaches (see Fig. 5).

Table 4 Comparison of ITAE with other existing approaches

Algorithm/Controller	ITAE
Z-N/PI [11]	3.7566
GA/PI [11]	2.7473
BFOA/PI [11]	1.7975
DE/PI [14]	1.2553
PSO/PI [8]	1.2143
SFS/PI (Proposed)	1.1763

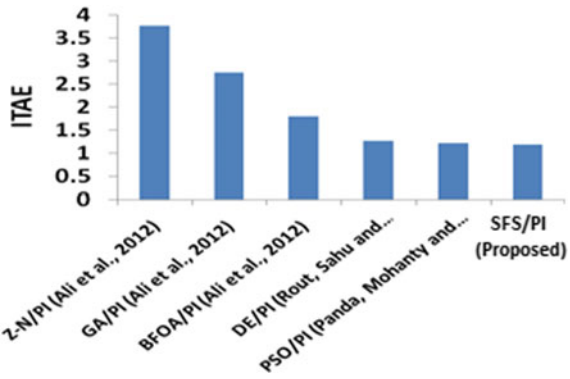

Fig. 5 Bar Chart comparison of ITAE

6.3 Comparison of System Dynamic Responses

The dynamic responses of the investigated system obtained by SFS/PI approach have been compared with some popular approaches in literature [11, 14] (Figs. 6, 7, 8 and 9). The simulation results demonstrate that SFS/PI approach exhibits better performance in terms of smoothness, number of oscillations and speed of response as compared to discussed approaches.

6.4 Comparison of Settling Times

The settling times of Δf_1, Δf_2 and ΔP_{Tie} for 2% tolerance band obtained by the proposed SFS/PI approach for the system under consideration have been given in Table 5 along with some popular approaches. In Table 4, it can be seen that less settling times have been obtained with SFS/PI approach among all other approaches. (see Fig. 10).

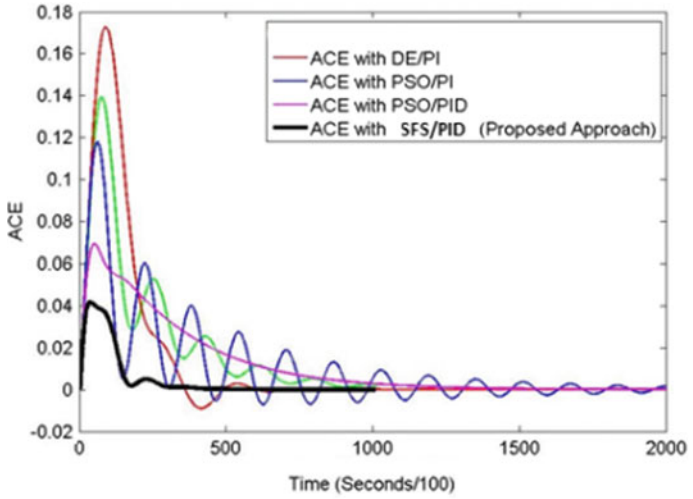

Fig. 6 Area control error (ACE)

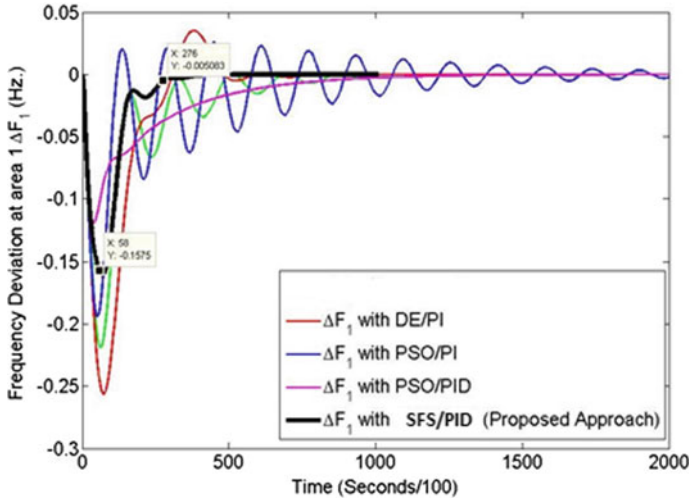

Fig. 7 Response of frequency deviation, ΔF_1 (Hz) at area 1

7 Conclusions

The application of SFS for optimal tuning of parameters of two PI controllers in AGC of standard two areas interconnected thermal power system has been dealt with ITAE as an objective function. For proving the proposed approach SFS/PI best, it has also been compared with some other approaches in the literature on the basis of ITAE,

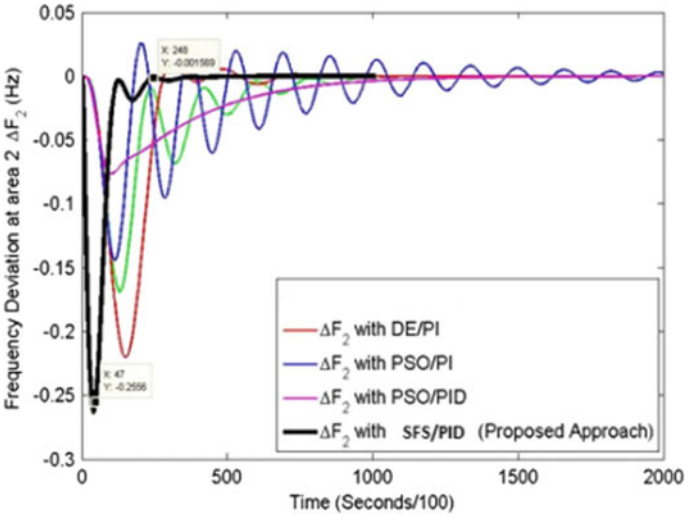

Fig. 8 Response of frequency deviation, ΔF_2 (Hz) at area 2

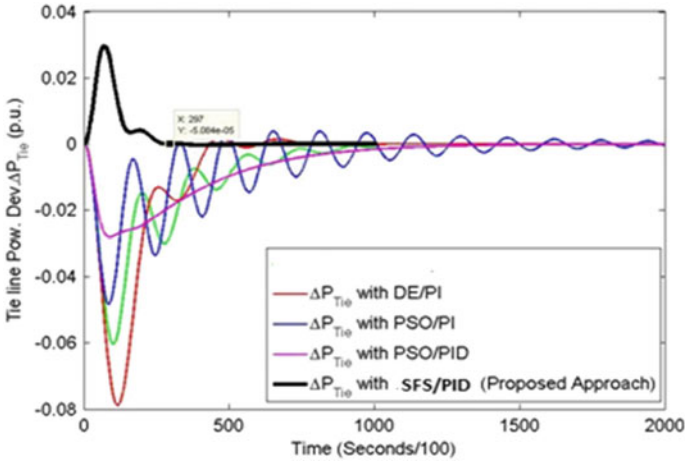

Fig. 9 Response of Tie-line power deviation, ΔP_{Tie} (p.u.)

Table 5 Comparison of settling times with other approaches

Algorithm/Controller	Settling times (2% tolerance band) T_s (s)		
	ΔF_1	ΔF_2	ΔP_{Tie}
DE/PI [14]	6.021	7.125	7.412
PSO/PI [8]	19.791	19.812	19.931
PSO/PID [8]	10.402	11.411	12.412
SFS/PI (Proposed approach)	2.719	2.452	3.142

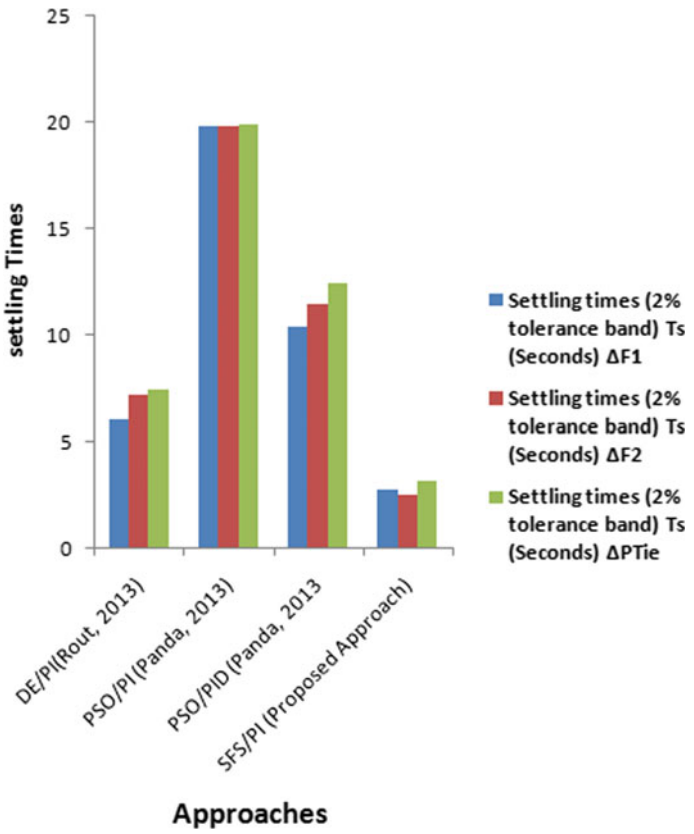

Fig. 10 Comparison of settling times of frequency and tie-line power deviations

settling times, and system dynamic responses. From the results obtained herein, it has been found that SFS/PI approach for the investigated system exhibits less ITAE, less settling times of Δf_1, Δf_2 and ΔP_{Tie}, fast response for Δf_1, Δf_2 and ΔP_{Tie} and smooth dynamic response of Δf_1, Δf_2 and ΔP_{Tie}.

Appendix

Simulation parameters of the two areas thermal power system [8, 11, 14, 19, 21–23]

P_{R}	2000 MW (rating)
P_{L}	1000 MW (nominal loading)
f	60 Hz
B_1 B_2	0.4253 p.u. MW/Hz
$R_1 = R_2$	2.401 Hz/p.u.

$T_{G1} = T_{G2}$	0.072 s
$T_{T1} = T_{T2}$	0.301 s
$K_{PS1} = K_{PS2}$	124 Hz/p.u. MW
$T_{PS1} = T_{PS2}$	2011s
T_{12}	0.5442 p.u

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Active Multifunctional Filter Design Using Carbon Nanotube Transistors

Vikash Kumar, Vidya Shree, D. Tejaswini, Shahid Afridi Qureshi, and Aminul Islam

Abstract A VDVTA-based MISO active multifunctional filter has been designed and analyzed using carbon nanotube field-effect transistor. The filter is capable of realizing multiple operations such as lowpass, highpass, bandpass, bandreject, and allpass filter functions. The circuit is configured to employ 3 input voltages and generate 1 output voltage. The proposed configuration provides capability of electronic controllability filter parameters, such as corner frequency (ω_c) and Q-factor via the external current of VDVTA. The presented work is realized in a 32-nm Standard CNFET Stanford model and is simulated using Hspice.

Keywords Carbon nanotube field-effect transistor · Voltage differencing voltage transconductance amplifier (VDVTA) · Biquad filter · Filter characteristics

1 Introduction

Filters are one of the most important and critical block in IC applications, for example radio applications, A/D and D/A convertor systems, etc. [1]. They are responsible for wide usage such like reducing noise, multiplexing, detecting signal, etc. Filters can

V. Kumar · V. Shree · D. Tejaswini · S. A. Qureshi
Department of Electronics and Communication Engineering, Presidency University, Bengaluru, Karnataka 560064, India
e-mail: vikashkumar@ieee.org

V. Shree
e-mail: vidyashreejogi345@gmail.com

D. Tejaswini
e-mail: tejaswini862@gmail.com

S. A. Qureshi
e-mail: princeafridi46@gmail.com

A. Islam (✉)
Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra, Ranchi, Jharkhand, India
e-mail: aminulislam@bitmesra.ac.in; dr.aminul.islam@ieee.org

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be categorized in two types: passive analog filters and active analog filters. While passive analog filters employ resistor, capacitor, inductor, and transformer and do not require any power supply, active analog filters comprise active elements besides passive elements and require power supply as well. Every kind of filter has its benefits and drawbacks. Active filters are preferred because of cost, less area on die, tunability, etc. Among active filters, multiple-input single-output (MISO) configuration is widely popular configuration for the synthesis and design of analog filters. In MISO, multiple-output filter operations are generated based on multiple combinations of inputs and selection of inputs can be done digitally by a microcontroller. Further, the use of active blocks such as OTA [2], CC [3], DVCC [4], OTRA [5], VD-DIBA [6], CDTA [7], etc., have given the flexibility to design multifunctional filters more conveniently. Nevertheless, each of the aforesaid active blocks carries few drawbacks such as (i) use of additional active blocks, (ii) employment of passive components, (iii) failure to simulate entire filter operations, and (iv) absence of electronic tunability. In order to reduce the above-listed drawbacks, several improvements have been executed. One of them is the new active element VDVTA (voltage differencing voltage transconductance amplifier) [8–10].

For this work, a MISO (3 inputs and 1 output) multifunctional filter has been implemented using one VDVTA, one active resistor, and 2 passive capacitors. The proposed circuit generates the primitive filter operations, specifically, lowpass, highpass, bandpass, bandreject, and allpass. Further, a new device carbon nanotube field-effect transistor (CNFET), which overcomes problems like short-channel effects, etc., of traditional MOSFETs, has been used to improve performance of multifunctional filter and provide robustness.

Organization of the paper is as follows: In Sect. 2, the concept of carbon nanotube field-effect transistor is discussed. Section 3 outlines voltage differencing voltage transconductance amplifier (VDVTA). In Sect. 4, the discussions on simulation results are presented. Lastly, conclusions are discussed in Sect. 5.

2 Carbon Nanotube FET (CNFET)

Due to intensive scaling of complementary metal-oxide semiconductor (CMOS) devices, several second-order effects such as DIBL effects, hot-carrier tunneling, surface scattering, GIDL effects, channel length modulation effects, leakage currents present momentous challenges for designing CMOS devices whose channel length is less than 45 nm. Such second-order effects and their challenges are anticipated by International Roadmap for Semiconductors (ITRS) [11]. Therefore, to avoid such design challenges and to preserve the saturating Moore's law, some novel devices are needed to be explored. Among all novel devices, carbon nanotube-based FETs (CNFETs) can be used to succeed the CMOS devices [12]. The benefits of CNFETs can be listed as:

- Re-adoptability of design infrastructure well established for CMOS.

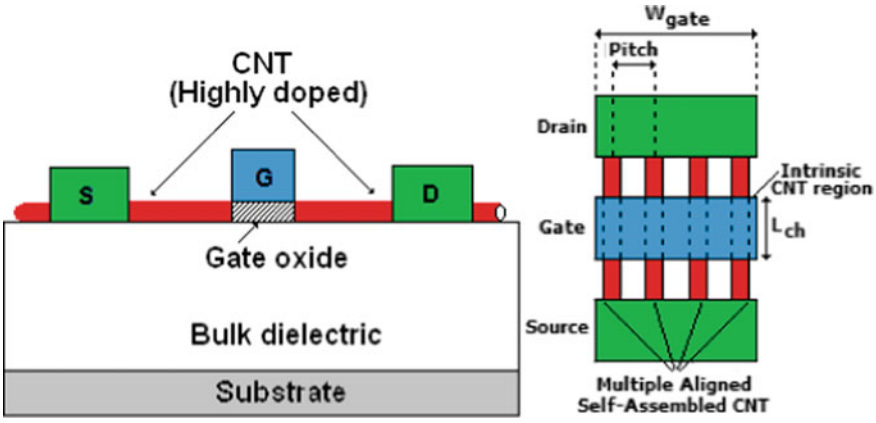

Fig. 1 **a** Cross-sectional diagram, **b** top section diagram of CNFET

- Analogous device structure to CMOS and almost similar principle of operation.
- Ballistic transportation of charge carriers [13].

The cross-sectional diagram and top-level diagram of a carbon nanotube-based FET (CNFET) is shown in Fig. 1a, b. Depending upon the angle through which a carbon nanotube is folded, it can work as either a conductor or a semiconductor depending on chirality integer vector (n_1, n_2). If $n_1 = n_2$ or $n_1 - n_2 = 3i$, then carbon nanotube works as a metal; otherwise, it works as a semiconductor. The characteristic parameters of a carbon nanotube are chirality vector (Ch), diameter (D_{CNT}), and threshold voltage (V_{th}) and are expressed as

$$\mathrm{Ch} = a\sqrt{n_1^2 + n_2^2 + n_1 n_2}, \tag{1}$$

$$D_{\mathrm{CNT}} = \frac{\mathrm{Ch}}{\pi}, \tag{2}$$

$$V_{\mathrm{th}} = E_{\mathrm{g}}/2q. \tag{3}$$

Here, E_{g} is energy band gap, q is electronic charge (1.6×10^{-19} C), and V_{π} is carbon π–π bond energy (3.033 eV).

3 Voltage Differencing Voltage Transconductance Amplifier (VDVTA)

VDVTA is a currently introduced, promising active element [14] which has wide range of applications such as in oscillators [15], filters [16, 17], etc. The block representation of VDVTA is shown in Fig. 2, and CNFET realization of VDVTA is shown in Fig. 3. VDVTA includes six high-impedance terminals ('p', 'n', 'z', 'x^-', 'x^+', 'v') and two stages. The first stage generates current output i_z from v_p and v_n. Similarly, second stage produces current i_{x^-} and i_{x^+} from v_z and v_v, respectively. The terminal associations are given by the equations below:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ g_{mx} & -g_{mx} & 0 \\ 0 & 0 & \pm g_{my} \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z - v_v \end{bmatrix} \tag{4}$$

where g_{mx} and g_{my} represent the transconductances of VDVTA.

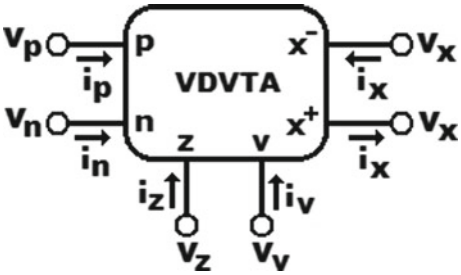

Fig. 2 Block representation of VDVTA

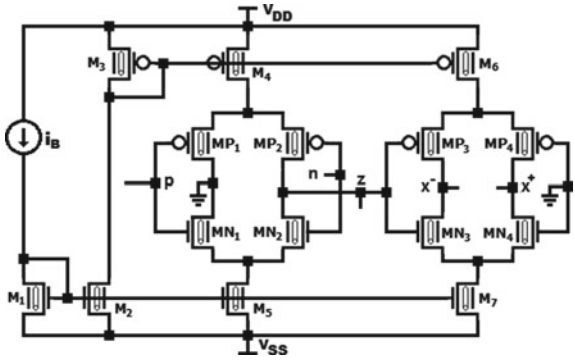

Fig. 3 Transistor-level representation of VDTA

4 Proposed Filter Circuit

The proposed circuit for the single VDVTA-based voltage-mode multifunctional filter configuration is depicted in Fig. 4. The circuit possesses three inputs (V_{i1}, V_{i2}, V_{i3}) and one output (V_{01}). Further, it also possesses one active resistor ($R_f = 1/G_f$) and two capacitors (C_f and C_g).

To implement the multifunctional transfer function, several arrangements of input voltages are changed in such a pattern that they achieve only one, i.e., either lowpass or highpass or bandpass or bandreject or allpass filter function at a time.

1. If $v_{i1}(s) = v_{LPF}(s)$ is the input voltage source and $v_{i2}(s) = v_{i3}(s)$ is grounded, it realizes a second-order lowpass filter (LPF) configuration. The analysis of the circuit given in Fig. 4 is presented as follows:

   Applying KCL at output node results in

$$i_x + v_{01}G_f + v_{01}sC_f = 0. \tag{5}$$

   Substituting the value of i_x from (4), we get

$$g_{my}(v_z - v_v) + v_{01}G_f + v_{01}sC_f = 0. \tag{6}$$

   From Fig. 4, v_z can be expressed as

$$v_z = \frac{i_z}{sC_g} = \frac{g_{mx}(v_p - v_n)}{sC_g} = \frac{g_{mx}(v_{01} - v_{LPF})}{sC_g}. \tag{7}$$

   Substituting for v_z from (7) in (6) results in

$$\frac{g_{mx}g_{my}}{sC_f}(v_{01} - v_{LPF}) - g_{my}v_{01} + v_{01}G_f + v_{01}sC_f = 0. \tag{8}$$

   Rearranging (8), the following expression is obtained

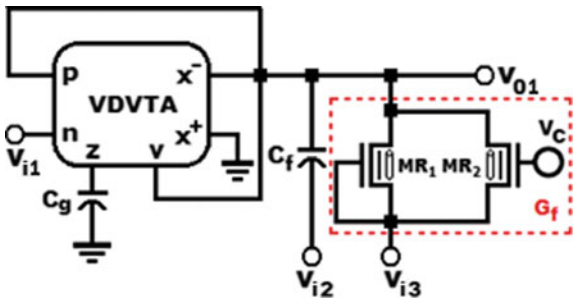

Fig. 4 Proposed memristor emulator

$$\frac{v_{01}(s)}{v_{\mathrm{LPF}}(s)} = \frac{g_{\mathrm{mx}}g_{\mathrm{my}}}{s^2C_{\mathrm{g}}C_{\mathrm{f}} + sC_{\mathrm{g}}\left(G_{\mathrm{f}} - g_{\mathrm{my}}\right) + g_{\mathrm{mx}}g_{\mathrm{my}}}. \tag{9}$$

A similar analysis can be followed for evaluating the transfer functions of remaining filter configurations. The input combination(s), realized filter configuration, and the corresponding transfer functions are mentioned as:

2. If $v_{\mathrm{i2}}(s) = v_{\mathrm{HPF}}(s)$ is the input voltage source and $v_{\mathrm{i1}}(s) = v_{\mathrm{i3}}(s)$ is grounded, then the configuration realizes a second-order highpass filter (HPF) configuration. The resultant transfer function is

$$\frac{v_{01}(s)}{v_{\mathrm{HPF}}(s)} = \frac{s^2C_{\mathrm{g}}C_{\mathrm{f}}}{s^2C_{\mathrm{g}}C_{\mathrm{f}} + sC_{\mathrm{g}}\left(G_{\mathrm{f}} - g_{\mathrm{my}}\right) + g_{\mathrm{mx}}g_{\mathrm{my}}}. \tag{10}$$

3. If $v_{\mathrm{i3}}(s) = v_{\mathrm{BPF}}(s)$ is the input voltage source and $v_{\mathrm{i1}}(s) = v_{\mathrm{i2}}(s)$ is grounded, then the configuration implements a second-order bandpass (BPF) filter configuration. The resultant transfer function is:

$$\frac{v_{01}(s)}{v_{\mathrm{BPF}}(s)} = \frac{sC_{\mathrm{g}}G_{\mathrm{f}}}{s^2C_{\mathrm{g}}C_{\mathrm{f}} + sC_{\mathrm{g}}\left(G_{\mathrm{f}} - g_{\mathrm{my}}\right) + g_{\mathrm{mx}}g_{\mathrm{my}}}. \tag{11}$$

4. If $v_{\mathrm{i1}}(s) = v_{\mathrm{i2}}(s) = v_{\mathrm{BRF}}(s)$ is the input voltage source and $v_3(s)$ is grounded, then the configuration realizes a second-order bandreject (BRF) filter configuration. The resultant transfer function is:

$$\frac{v_{01}(s)}{v_{\mathrm{BRF}}(s)} = \frac{s^2C_{\mathrm{f}}C_{\mathrm{g}} + g_{\mathrm{mx}}g_{\mathrm{my}}}{s^2C_{\mathrm{g}}C_{\mathrm{f}} + sC_{\mathrm{g}}(G_{\mathrm{f}} - g_{\mathrm{mx}}) + g_{\mathrm{mx}}g_{\mathrm{my}}}. \tag{12}$$

5. If $v_{\mathrm{i1}}(s) = v_{\mathrm{i2}}(s) = -v_{\mathrm{i3}}(s) = v_{\mathrm{APF}}(s)$ is the input voltage source, then the configuration realizes a second-order allpass (APF) filter configuration. The resultant transfer function is:

$$\frac{v_{01}(s)}{v_{\mathrm{APF}}(s)} = \frac{s^2C_{\mathrm{g}}C_{\mathrm{f}} - sC_{\mathrm{g}}G_{\mathrm{f}} + g_{\mathrm{mx}}g_{\mathrm{my}}}{s^2C_{\mathrm{g}}C_{\mathrm{f}} + sC_{\mathrm{g}}\left(G_{\mathrm{f}} - g_{\mathrm{my}}\right) + g_{\mathrm{mx}}g_{\mathrm{my}}}. \tag{13}$$

The net voltage at the output of multifunctional filter from (9)–(13) is expressed as:

$$v_{01}(s) = \frac{s^2C_{\mathrm{f}}C_{\mathrm{g}}v_{i2}(s) + sC_{\mathrm{g}}G_{\mathrm{f}}v_{\mathrm{i3}}(s) + g_{\mathrm{mx}}g_{\mathrm{my}}v_{\mathrm{i1}}(s)}{s^2C_{\mathrm{f}}C_{\mathrm{g}} + sC_{\mathrm{g}}\left(G_{\mathrm{f}} - g_{\mathrm{my}}\right) + g_{\mathrm{mx}}g_{\mathrm{my}}}. \tag{14}$$

From (14), the characteristics parameter such as cut-off frequency (ω_{c}), quality (Q) factor is evaluated to be:

$$\omega_{\mathrm{c}} = \sqrt{\frac{g_{\mathrm{mx}}g_{\mathrm{my}}}{C_{\mathrm{f}}C_{\mathrm{g}}}}, \tag{15}$$

$$Q = \frac{1}{(G_f - g_{my})}\sqrt{\frac{C_f}{C_g} g_{mx} g_{my}}. \tag{16}$$

From (15) and (16), it is observed that the corner frequency (ω_c) and Q-factor may be changed via changing the transconductances (g_{mx}, g_{my} or i_{bias}) and Q-factor can be individually changed by changing resistance (R_f) without disturbing corner frequency (ω_c).

5 Simulation Results

The presented multifunctional filter configuration has been implemented using CNFET. The findings presented here is the result of comprehensive simulation on SPICE using experimentally validated 32-nm CNFET model of Stanford University [18]. The supply voltage is taken as $V_{DD} = V_{SS} = \pm$ 0.8 V with bias current $i_B = 55$ μA. The filter gain characteristic for lowpass, highpass, bandpass filter, bandreject, and allpass filter configurations of proposed MISO multifunctional filter circuit is depicted in Fig. 5. The AC gain frequency responses of all the filter topologies, i.e., lowpass, highpass, bandpass, bandreject, and allpass filter functions are centered at the same cut-off frequency of 2 GHz. The transient response of the bandpass filter (BPF) configuration for a sinusoidal input peak-to-peak voltage of 2 mV and frequency of 2 GHz (shown in Fig. 6) is presented in Fig. 7. The sinusoidal output voltage waveform also has the same peak-to-peak voltage of 2 mV and frequency of 2 GHz, thereby validating the stable operation of the proposed circuit. Further, the proposed MISO multifunctional filter circuit draws a power of 88.6 μW from the supply voltage.

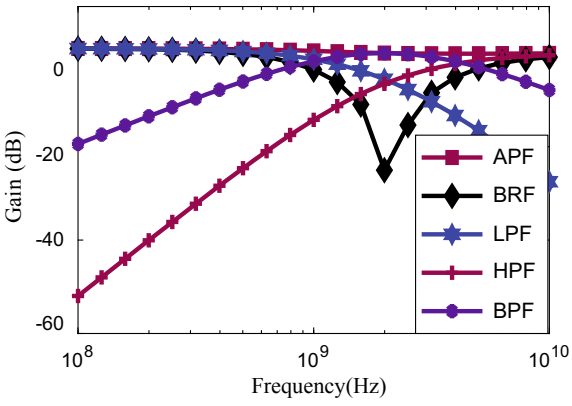

Fig. 5 Gain characteristic for all filter configurations

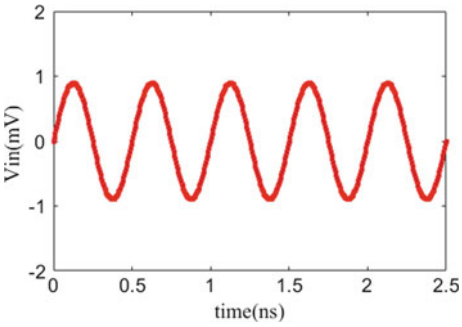

Fig. 6 Sinusoidal input of 2 GHz

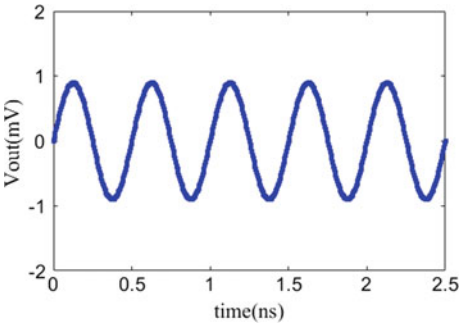

Fig. 7 Transient output at sinusoidal input of 2 GHz

6 Conclusion

The paper presents the design of electronic controllable MISO multifunctional active filter configuration using VDVTA and CNFET. The filter configuration employs a VDVTA, an active resistor, and 2 passive capacitors for implementing lowpass, high-pass, bandpass, bandreject, and allpass filter functions, respectively. The derivation of the mathematical expressions for transfer function, cut-off frequency (ω_c), and quality (Q) factor for all the filter configurations are provided. In order to confirm the theoretical analyses, simulation results are given.

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A Comprehensive Study of Time Moments and Markov Parameters in System Reduction

Arvind Kumar Prajapati, Afzal Sikander, and Rajendra Prasad

Abstract Time moments and Markov parameters play two important roles in the simplification of large-scale system. First role plays in the matching of steady-state responses of the full order and reduced order plants; for this, the matching of their initial few time moments are required. The matching of transient responses between the complete order and lower order systems is the second role of the time moments and Markov parameters. For the second role, the Markov parameters of the actual order and lower order plants must be matched. In this contribution, it is shown that the time moments are not only responsible for the matching of static responses but also for the matching of transient responses. For better understanding of the contribution of the time moments and Markov parameters, popular examples are taken from literature and in each examples, proposed concepts are explained. A new system diminution technique is also proposed which may be applicable when the Padé approximation methodology fails. The process of obtaining reduced plant by this method is based on matching of Markov parameters in place of time moments matching.

Keywords Reduced order modeling · Routh stability · Time moments and Markov parameters · Transfer function · Stability

1 Introduction

Model order diminution is concerned with the simplification of complexity of higher order systems; it transforms the higher order system into a lower order plant in

A. K. Prajapati (✉)
VIT-AP University, Amaravati, Andhra Pradesh, India
e-mail: arvindawr1990@gmail.com

A. Sikander
Department of Instrumentation and Control Engineering, Dr. B. R. Ambedkar National Institute of Technology, Jalandhar 144011, India
e-mail: afzals@nitj.ac.in

R. Prasad
Indian Institute of Technology Roorkee, Roorkee, Uttarakhand 247667, India
e-mail: rpdeefee@iitr.ac.in

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such way that the reduced order plant retains the essential features of the large-scale systems [1–6]. Several model order diminution technologies have been recommended for computing the reduced order plants [7–16]. In the frequency domain, Padé approximation methodology [7] and Routh stability technique [8] are the most frequently used methodologies for the system reduction. In [17, 18], it is recommended that the Padé approximation is the best method for the matching of initial few time moments of the complete order and simplified order models and the matching of the steady-state responses also. In some class of systems, the Padé approximation method does not ensure the preservation of stability of the full order plant in the reduced order system [19–23]. The Routh stability technique always promises the retention of the stability of the complete order plant in the reduced order plant. In this methodology, the first few Markov parameters of the actual order plant and reduced order plant are approximately the same and due to this, their transient responses are completely matched [17, 18]. But, the Routh stability method may provide the same simplified order plant for the different higher order plants and this non-uniqueness was described in [24]. In case of non-minimum phase large-scale systems, the Routh stability methodology fails to preserve the dominant roots of the actual plant in the reduced plant [25]. Several combined approaches have been recommended for the retention of fundamental properties of both the techniques in the lower order plants [26–31].

In the time domain, balanced realization is the standard method for the simplification of large-scale models. In 1981, Moore observed that the less controllable and less observable states have very less influence in the time response of the dynamic system [32]. In this technique, the simplified system is achieved by deleting the less controllable and less observable states of the balanced system (i.e., a system in which controllability and observability Gramians matrices are same). A dynamic system can be transformed into the balanced system by applying similarity transformation. In [33], the balanced realization method is simplified. In 2004, the balanced truncation methodology is extended for the simplification of large-scale linear time-varying models by Sandberg and Rantzer [34]. The balanced realization methodology is also extended for the model diminution of large-scale nonlinear systems directly by finding the incremental controllability and observability functions [35].

Mostly, the model order diminution techniques are related with the matching of initial few time moments [7, 36] or first few Markov parameters [37, 38] or both [39–41] of the reduced system to the corresponding terms of the original system. Therefore, the Markov parameters and time moments are important factor for the determination of the lower order plants. Hence, the impact of these parameters in reduced order modeling is important to explore. Generally, it is known that if the initial few Markov parameters of the simplified model and the full order plant are matched, then their transient responses will match thoroughly. Similarly, if the time moments of lower order plant and higher order system are matched, then their static responses will also be matched.

In this contribution, the few concepts concerned with the matching of initial few Markov parameters and initial few time moments of the simplified order model with full order system are proposed. It is also given that how many optimum number of

initial few Markov parameters and time moments are required for the determination of the reduced order systems. The rest of the contribution is arranged as: In Sect. 2, a new model order reduction method by the matching of Markov parameters is recommended. In Sect. 3, few concepts concerned with the matching of first few time moments and Markov parameters in the reduced order modeling are given. The numerical simulation results are given in Sect. 4. The conclusion of the contribution is discussed in Sect. 5.

2 Model Order Reduction by Markov Parameters Matching Method

Consider the nth order largescale asymptotically stable system:

$$G(s) = \frac{d_0 + d_1 s + d_2 s^2 + \cdots + d_{n-1} s^{n-1}}{d_0 + d_1 s + d_2 s^2 + \cdots + d_n s^n} \tag{1}$$

Taylor series expansion of $G(s)$ about $s = \infty$ is obtained as

$$\begin{aligned} G(s) &= M_{-1} s^{-1} + M_{-2} s^{-2} + \cdots + M_{-2r} s^{-2r} + \cdots \\ &= \sum_{i=1}^{\infty} M_{-i} s^{-i} \end{aligned} \tag{2}$$

where the parameters $\{M_{-i} : i = 1, \ldots, \infty\}$ are known as the Markov parameters [7, 42] and 'r' is the order of the simplified system. Similarly, $G(s)$ can also be expanded in the terms of its Taylor series expansion about $s = 0$; hence

$$\begin{aligned} G(s) &= C_0 + C_1 s + C_2 s^2 + \cdots + C_{2r} s^{2r} + \cdots \\ &= \sum_{i=1}^{\infty} C_i s^i \end{aligned} \tag{3}$$

where the parameters $\{C_i : i = 1, 2, \ldots, \infty\}$ are proportional to the system time moments [7]; in this paper, these are termed as time moments. In the proposed method, the lower order system $R_r(s)$ is chosen in such a way that maximum number of Markov parameters of the original system is retained in the reduced system. Let the reduced model $R_r(s)$ is given by

$$R_r(s) = \frac{a_0 + a_1 s + a_2 s^2 + \cdots + a_{r-1} s^{r-1}}{b_0 + b_1 s + b_2 s^2 + \cdots + b_{n-1} s^{n-1} + s^n} \tag{4}$$

For the matching of Markov parameters of reduced model to the large-scale systems, comparing (3) and (4), it gives

$$\begin{aligned} a_{r-1} &= M_{-1} \\ a_{r-2} &= M_{-1}b_{r-1} + M_{-2} \\ a_{r-3} &= M_{-1}b_{r-2} + M_{-2}b_{r-1} + M_{-3} \end{aligned} \tag{5}$$

$$0 = M_{-1}b_0 + M_{-2}b_1 + M_{-3}b_2 + \cdots + M_{-r-1}$$

$$0 = M_{-2}b_0 + M_{-3}b_1 + M_{-4}b_2 + \cdots + M_{-r-2}$$

$$0 = M_{-3}b_0 + M_{-4}b_1 + M_{-5}b_2 + \ldots + M_{-r-3}$$

In this equation, initial $2r$ Markov parameters of $R_r(s)$ and $R_r(s)$ are same. The last r equations are used to compute $b_i (i = 0, 1, \ldots, r-1)$ and initial r equations are used to compute $a_i (i = 0, 1, \ldots, r-1)$. In order to match the steady-state values of original and reduced system, a_0 is replaced by $a_{0\text{new}}$ and it is determined as

$$\frac{a_{0\text{new}}}{b_0} = K$$

where K is known as gain adjustment factor, which is defined by the steady-state value of the large-scale model

$$K = G(s)|_{s=0}$$

and rth order reduced model is

$$R_r(s) = \frac{a_{0\text{new}} + a_1 s + a_2 s^2 + \cdots + a_{r-1}s^{r-1}}{b_0 + b_1 s + b_2 s^2 + \cdots + b_{n-1}s^{n-1} + s^n} \tag{6}$$

This method is applicable when the Padé approximation method fails. Similar as Padé approximation methodology, this method also does not guarantee the stability of the lower order system.

3 Contribution of Markov Parameters and Time Moments in System Diminution

In model order diminution, the role of time moments and Markov parameters is of fundamental importance. On the basis of matching of time moments and Markov parameters of lower order plant with actual system, the contribution of these parameters is categorized as follows.

4 When Time Moments Are Matched

The Taylor series expansion of $R(s)$ about $s = 0$, is as

$$R_r(s) = c_0 + c_1 s + c_2 s^2 + \cdots + c_{2r} s^{2r} + \cdots = \sum_{i=1}^{\infty} c_i s^i \tag{7}$$

where $\{c_i : i = 1, 2, \ldots, \infty\}$ are the time moments of the lower order system. If the initial few time moments of the reduced model are matched with the initial few time moments of the large-scale system, then the following two cases are happened:

1. If the reduced model is unstable and $c_0 = C_0, c_1 = C_1, c_2 = C_2$ etc.

In this case, the time response of the reduced order system will not match with the time response of the large-scale plant because the reduced model is unstable. Hence, the necessary condition for the model order diminution is that the reduced order model must be stable otherwise that model order reduction methodology fails to simplify the particular large-scale system.

2. If the reduced order plant is stable and $c_0 = C_0, c_1 = C_1, c_2 = C_2$ etc.

If the first time moment of the reduced system is matched with the first time moment of the large-scale system, then their steady-state values are matched [17, 18]. The transient response of reduced order plant is matched with transient response of full order system and their proportionality of matching are depended upon the how many initial time moments of both systems are matched. As the number of matching of initial time moments is increased the proportionality of matching of transient responses of reduced model and original system is increased. Hence, by matching of first few time moments of the reduced model with the first few time moments of the original system, the transient as well as steady-state responses will be matched without matching of their Markov parameters.

4.1 When Time Moments and Markov Parameters Are Matched

In reduced order modeling, the matching of Markov parameters of the simplified order system with the large-scale plant guarantees the matching of their transient responses [17, 18]. If the initial few Markov parameters of the simplified system are only matched with the initial few Markov parameters of the higher order plant, it is not always possible that their performances will also be matched without matching of their steady-state values (i.e., first time moments). By matching of first time moment of the simplified order model with the first time moment of the original plant, the

matching of their time responses will improved by matching of more number of their Markov parameters.

5 Numerical Examples

Example 1 Consider a stable sixth-order large-scale system given in [7]

$$G(s) = \frac{(s+1013)(s+4.938)(s+0.7386)\left(s^2-4.233s+27.07\right)}{(s+1)^2(s+10)^2(s+100)^2} \tag{8}$$

$$= 0.1 - 0.0819s + 0.105548s^2 - 0.125999s^3 + 0.1461s^4 - 0.1633s^5 + \cdots \tag{9}$$

The second-order simplified system achieved by the Padé approximation method is

$$R_2(s) = \frac{-0.0980s - 0.4686}{s^2 - 4.8176s - 4.6856} \tag{10}$$

$$= 0.1 - 0.0819s + 0.105548s^2 - 0.125999s^3 + 0.1520s^4 - 0.1833s^5 + \cdots \tag{11}$$

From (9) and (11), it is clear that the initial four time moments of the original system are matched with the initial four time moments of the reduced model, but their time response will not match because of instability of reduced order system. Hence, it is compulsory that the obtained reduced model must be stable otherwise, irrespective of matching of time moments/Markov parameters, their responses will never match.

Example 2 Consider a fourth-order Cuk converter system in continuous mode given in [43–45]. This standard system has been taken to illustrate that without matching of Markov parameters, the transient responses of the reduced order and large-scale systems can be matched (Fig. 1).

$$G(s) = \frac{-814.8s^3 + 2.456 \times 10^7 s^2 - 1.232 \times 10^{12} s + 2.154 \times 10^{16}}{s^4 + 149.4s^3 + 4.922 \times 10^8 s^2 + 6.25 \times 10^{10} s^2 + 2.02 \times 10^{14}} \tag{12}$$

$$= 107 - 3.909 \times 10^{-2} s - 2.476 \times 10^{-4} s^2 + 1.718 \times 10^{-7} s^3 + 5.497 \times 10^{-10} s^4 - 6 \times 10^{-13} s^5 \tag{13}$$

$$= -814.8s^{-1} + 2.468 \times 10^7 s^{-2} - 8.346 \times 10^{11} s^{-3} + 9.567 \times 10^{15} s^{-4} + 4.08 \times 10^{20} s^{-5} + \cdots \tag{14}$$

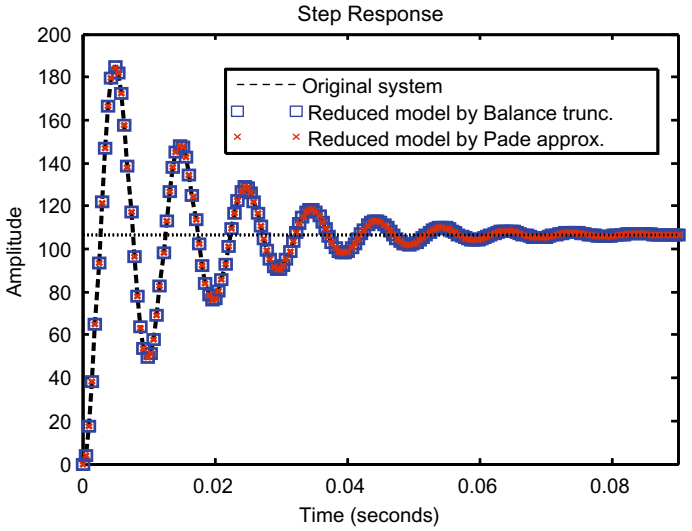

Fig. 1 Comparison of time responses of the large-scale system and its simplified system

Following are two stable reduced models of (11)

$$R_2(s) = \frac{-2524s + 4.382 \times 10^7}{s^2 + 127.1s + 4.108 \times 10^5} \tag{15}$$

$$= 107 - 3.915 \times 10^{-2}s - 2.476 \times 10^{-4}s^2 + 1.719 \times 10^{-7}s^3 + 5.494 \times 10^{-10}s^4 - 6 \times 10^{-13}s^5 \tag{16}$$

$$= -2524s^{-1} + 4.414 \times 10^7 s^{-2} - 4.573 \times 10^9 s^{-3} - 1.755 \times 10^{13}s^{-4} + 4.109 \times 10^{15}s^{-5} + \cdots \tag{17}$$

$$R_2(s) = \frac{-2511s + 4.378 \times 10^7}{s^2 + 127s + 4.106 \times 10^5} \tag{18}$$

$$= 107 - 3.909 \times 10^{-2}s - 2.476 \times 10^{-4}s^2 + 1.718 \times 10^{-7}s^3 + 5.499 \times 10^{-10}s^4 - 6 \times 10^{-13}s^5 \tag{19}$$

$$= -2511s^{-1} + 4.41 \times 10^7 s^{-2} - 4.5695 \times 10^9 s^{-3} - 1.753 \times 10^{13}s^{-4} + 4.102 \times 10^{15}s^{-5} + \cdots \tag{20}$$

The simplified order system in (15) is achieved by the balanced realization methodology and the simplified system in (18) is computed by the Padé approximation technique. From (13), (16), (19), it clear that the time moments of the simplified order plants are completely matched with the corresponding terms of original system but from (14), (17), (20), it is obvious that their Markov parameters are not matching but still their transient parts of are closely matched. It is due to the preservation of initial six time moments of the actual plant in the reduced plant. Hence, it is clear that without matching of Markov parameters, the time responses of the reduced order models are thoroughly matched with the complete order model. This condition is not only applicable with the simplified order plants which are obtained by the Padé approximation technique or by the balanced realization methodology but also applicable for the various other system diminution methods.

Example 3 Consider a standard non-minimum phase system described by the following tenth-order transfer function [46] as

$$G(s) = \frac{-6993.006(s-1)(s+4)(s+7.5)(s+12)(s+15)(s+25)}{(s+1\pm j2)(s+2)(s+7)(s+10)(s+10)(s+12.5)(s+18)(s+20)(s+30)} \tag{21}$$

$$= 0.999 - 1.8862s + 1.2657s^2 - 0.4597s^3 + 0.0906s^4 - 0.0233s^5 + 0.0305s^6 + \cdots \tag{22}$$

$$= -699s^{-1} - 3.59 \times 10^5 s^{-2} + 3.38 \times 10^7 s^{-3} - 1.90 \times 10^9 s^{-4} + 8.53 \times 10^{10} s^{-5} + \cdots \tag{23}$$

The second- and third-order reduced models determined by the Padé approximation method are given as

$$R_2(s) = \frac{-3.265s + 3.1174}{s^2 + 2.6236s + 3.1205} \tag{24}$$

$$= 0.9990 - 1.8867s + 1.2666s^2 - 0.4605s^3 - 0.0187s^4 + 0.1633s^5 - 0.1313s^6 + \cdots \tag{25}$$

$$= -3.2650s^{-1} + 11.6844s^{-2} - 20.4730s^{-3} + 17.2658s^{-4} + 18.5701s^{-5} + \cdots \tag{26}$$

$$R_2(s) = \frac{0.2763s^2 - 10.6154s + 10.3443}{s^3 + 3.984s^2 + 8.9049s + 10.3339} \tag{27}$$

$$= 0.999 - 1.8875s + 1.2673s^2 - 0.4608s^3 + 0.0911s^4 - 0.0235s^5 + 0.0297s^6 + \cdots \tag{28}$$

$$= 0.2763s^{-1} - 11.7208s^{-2} + 54.5651s^{-3} - 115.8709s^{-4} + 96.92s^{-5} + \cdots \quad (29)$$

The Markov parameters of second-order simplified model (24) and third-order reduced model (27) are different from the Markov parameters of the full order plant but their step responses are nearly matched as displayed in Fig. 2. The behavior of the second-order simplified plant is not completely matched with the performance of the full order plant because it retains only first four time moments of the complete order system. The behavior of third-order simplified system is closely matched with the performance of the full order model because it preserves initial six time moments of the actual plant. Hence, for the optimum matching of the performances, at least first four time moments of the higher order model should be preserved in the lower order system.

The steady-state responses of the simplified order systems are matched with the steady response of the higher order plant. The transient part of the third-order simplified plant is better matched with the transient part of the actual plant as compared to the transient part of second-order simplified plant. This is due to that the third-order simplified plant preserved extra fifth and sixth time moments of the original system. Hence, it may be concluded that the first time moment is utilized to match the steady-state value and the remaining other time moments are responsible for the improvement of matching of transient part in the order of 6th > 5th > 4th > 3rd > 2nd time moments.

Example 4 Consider a third-order transfer function given in [47]

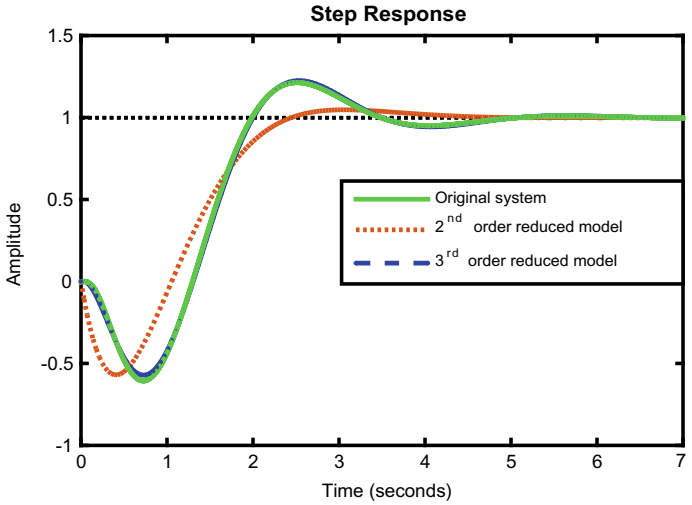

Fig. 2 Comparison of time responses of actual system and its reduced models computed by Padé approximation technique

$$G(s) = \frac{8s^2 + 6s + 2}{s^3 + 4s^2 + 5s + 2} \tag{30}$$

$$= 1 + 0.5s + 0.75s^2 - 3.375s^3 + 6.6875s^4 - 10.3438s^5 + \cdots \tag{31}$$

$$= 8s^{-1} - 26s^{-2} + 66s^{-3} - 150s^{-4} + 322s^{-5} - 670s^{-6} + \cdots \tag{32}$$

The second-order simplified plant determined by the Padé approximation technique is

$$R_2(s) = \frac{-1.7778s - 0.2222}{s^2 - 1.6667s - 0.2222} \tag{33}$$

$$= 1 + 0.4995s + 0.7527s^2 - 3.3988s^3 + 28.8858s^4 - 232.0044s^5 + \cdots \tag{34}$$

The second-order reduced systems obtained by various system diminution techniques are

$$R_2(s) = \frac{6s + 2}{4s^2 + 4.5s + 2} \tag{35}$$

$$= 1 + 0.75s - 3.687s^2 + 6.797s^3 - 7.918s^4 + 4.222s^5 + \cdots \tag{36}$$

$$= 1.5s^{-1} - 1.187s^{-2} + 0.586s^{-3} - 0.065s^{-4} - 0.219s^{-5} + 0.279s^{-6} + \cdots \tag{37}$$

$$R_2(s) = \frac{8s + 3.081}{s^2 + 3.486s + 3.081} \tag{38}$$

$$= 1 + 1.465s - 1.982s^2 + 1.767s^3 - 1.357s^4 + 0.962s^5 + \cdots \tag{39}$$

$$= 8s^{-1} - 24.81s^{-2} + 61.85s^{-3} - 139.195s^{-4} + 294.727s^{-5} - 598.678s^{-6} + \cdots \tag{40}$$

$$R_2(s) = \frac{1.0526s + 1}{0.132s^2 + 0.553s + 1} \tag{41}$$

$$= 1 + 0.5s - 0.4081s^2 - 0.1597s^3 - 0.0345s^4 - 0.002s^5 + \cdots \tag{42}$$

$$= 8s^{-1} - 26s^{-2} + 48.4s^{-3} - 5.6s^{-4} - 344.2s^{-5} + 1487.8s^{-6} + \cdots \tag{43}$$

$$R_2(s) = \frac{2.054s + 1}{0.2568s^2 + 0.9595s + 1} \tag{44}$$

$$= 1 + 1.095s - 1.307s^2 + 0.973s^3 - 0.598s^4 + 0.324s^5 + \cdots \tag{45}$$

$$= 8s^{-1} - 26s^{-2} + 66s^{-3} - 145.2609s^{-4} + 285.873s^{-5} - 502.469s^{-6} + \cdots \tag{46}$$

$$R_2(s) = \frac{1.5534s + 1}{0.1942s^2 + 0.756s + 1} \tag{47}$$

$$= 1 + 0.797s - 0.797s^2 + 0.448s^3 - 0.184s^4 + 0.052s^5 + \cdots \tag{48}$$

$$= 8s^{-1} - 26s^{-2} + 60s^{-3} - 99.65s^{-4} + 79.15s^{-5} + 205.026s^{-6} + \cdots \tag{49}$$

where the models (35) and (38) are determined by using Routh stability technique and the proposed methodology, respectively. The reduced order systems (41), (44), and (47) are given in [2] (Fig. 3).

In Fig. 4, the time responses of the higher order model and simplified order plants are displayed. The reduced system (35) gives a poor representation of the transient response because it preserves fully the first time moment and partially the second time moment. In concerned of overall time response, the lower order system (41) gives a significant perfection over (35). This is because, reduced model (41) fully preserves the first time moment and first two Markov parameters. The reduced order system (38) is an upgraded transient response over the simplified system (41). This is

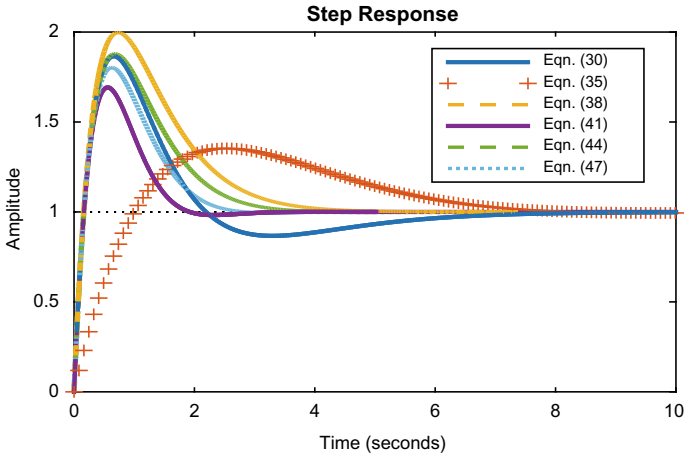

Fig. 3 Comparison of time responses of full and reduced order plants

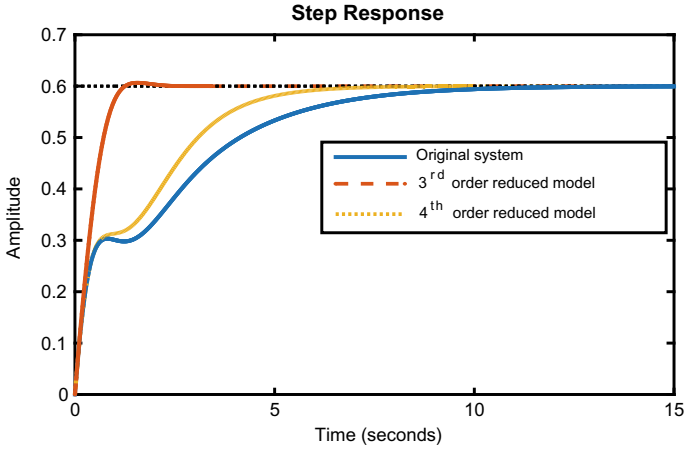

Fig. 4 Comparison of step responses of the large-scale system and its approximants

due to the retention of fully first Markov parameter, four Markov parameters partially, and fully the first time moment. But the lower order system (41) preserves partially the fifth Markov parameter, so it keeps five pivotal factors partially as the reduced system (38) but the behavior of (38) is little better than (41). Because, from transient point of view, the effectiveness of the Markov parameters is as 1st > 2nd > 3rd > 4th > 5th > 6th Markov parameter.

The models (44) and (47) are the best approximation of the original system (30) because both the lower order models preserve partially first five pivotal parameters of model order reduction. It is difficult to discriminate that which one is more optimum for the large-scale plant, but from transient point of view, (44) is better approximants because it completely preserves the first three Markov parameters compare to (47), which fully preserves first two Markov parameters.

Example 5 Consider a sixth-order stable model taken from [48]

$$G(s) = \frac{(s+6.049)(s+0.504 \pm j0.982)(s+0.972 \pm 0.527i)}{(s+0.5)(s+1)(s+2)(s+2 \pm j)(s+3)} \tag{50}$$

$$= 0.6 - 1.23s + 2.952s^2 - 6.438s^3 + 13.407s^4 - 27.39s^5 + \cdots \tag{51}$$

$$= 1s^{-1} - 1.5s^{-2} - 7s^{-3} + 71.2s^{-4} - 378.35s^{-5} + 1586.675s^{-6} + \cdots \tag{52}$$

All the approximants obtained by Padé approximation are unstable. The third-order and fourth-order simplified systems obtained by the proposed method are

$$R_2(s) = \frac{s^2 + 8.943s +}{s^3 + 10.443s^2 + 39.17s + 60.655} \tag{53}$$

$$= 0.6 - 0.24s + 0.068s^2 - 0.013s^3 + 0.0004s^4 + 0.0008s^5 + \cdots \quad (54)$$

$$= 1s^{-1} - 1.5s^{-2} + 12.8517s^{-3} - 136.194s^{-4} + 1009.3s^{-5} - 5981.7s^{-6} + \cdots \quad (55)$$

$$R_2(s) = \frac{s^3 + 6.959s^2 + 6.882s + 9.863}{s^4 + 8.459s^3 + 26.573s^2 + 36.231s + 16.439} \quad (56)$$

$$= 0.6 - 0.9033s + 1.4444s^2 - 1.9711s^3 + 2.4377s^4 - 2.8748s^5 + \cdots \quad (57)$$

$$= 1s^{-1} - 1.5s^{-2} - 7s^{-3} + 72.671s^{-4} - 390.925s^{-5} + 1654.1s^{-6} + \cdots \quad (58)$$

In this example, it is clear that both lower order plants keep first time moment fully but different number of Markov parameters, due to this there are significant differences in the matching of their time responses with response of original system. The third-order simplified system keeps first two Markov parameters completely so its starting part of transient response is matched and due to matching of first time moment, its steady state is also matched. In case of fourth-order simplified system, it retains first three fully and forth partially Markov parameters so that its starting part of transient is closed matched than the third-order simplified plant. The overall response of the fourth-order simplified system is better than the third-order simplified plant this is due to the difference of retained numbers of Markov parameters because both models preserve first time moment only. Hence, more number of Markov parameters of original and reduced model matches and then their responses will match more closely.

6 Conclusion

From the above discussion, it can be summarized that the matching of both time moments as well as Markov parameters in model order reduction is not necessary. The matching of any one parameter either time moments or Markov parameters is enough to match the responses of the reduced order plant with the original plant. The proportionality of matching of time responses of the reduced order plant with the original plants is dependent upon the number of matching of Markov parameters or time moments or both the parameters. Hence, the reduced order plant which preserves more number of Markov parameters or time moments or both, the time response of that simplified order system will match more closely with the response of the full order plant. The following few points related to the summary of this paper are enumerated as

1. In time moments matching concept, by retaining more number of time moments of the full order model in the simplified order plant, the response of the lower order system is compelled to match completely with the response of the complete order system.
2. In Markov parameters matching concept, by preserving the first time moment of the original plant, the response of simplified order system is enforced to match with the performance of the large-scale model by retaining large number of Markov parameters.
3. In matching of both the parameters, the response of the particular simplified order plant is better match with the response of the full order plant which retains more number of Markov parameters and time moments (pivotal parameters).
4. If the various lower order plants preserve equal number pivotal parameters, the responses of each simplified order plant will approximately be same and match with the response of the complete order system but from the transient points of view, the response of the particular lower order system will better match which retains more number of starting Markov parameters.

Thus, without retaining the Markov parameters of the large-scale system in the lower order system, the transient part of the lower order system will closely match with the transient part of the higher order plant. And, the time moments are responsible for the matching of the transient responses of the reduced and full order plants. By retaining the first time moment of the full order model in the lower order model, the response of the lower order systems is compelled to match more closely with the response of the higher order system by retaining more number of Markov parameters. The matching of time moments constructs the matching of responses of lower order systems to higher order systems from steady-state part toward the transient part. The matching of Markov parameters constructs the matching of responses from transient part toward steady-state part. By calculating the pivotal parameters of full order plant and lower order plant, the comparison of system reduction techniques can also be done without plotting of their time responses or computing their performance error indices.

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Computing Processes of Recurrent Neural Network at Different Layers

Dulal Acharjee and Jerzy Szymanski

Abstract For researchers, writing their own program to simulate the concept of model of design is mostly essential. Computing processes at different stages of Neural Network (NN) are discussed in this introductory tutorial. In NN, two types of computing are performed, Feed Forward and Feed Back processing. Sometimes, Feed Back computing is known as Recurrent Neural Network (RNN). Here, updating of weight values required for RNN is discussed in viewpoint of programming of simulation of any new model.

Keywords Neural network · Feed forward · Recurrent neural network

1 Introduction

Neural Network, NN, is a computing method that mimics the computational process of human brain. Human brain is a network of about 10^{11} Neurons. Neurons are the main unit of decision making of brain and are interconnected as mesh networks among themselves where data of communication are electric impulses or biochemicals moving from one cell to another. Each neuron is considered as computing process of computer having input and output. So, before starting a discussion on neural network, let us look at the basis of the concept of Neurons and its computing process [1].

What knowledge may be extracted from this Fig. 1? NN is invented by the logic of neural process. In Fig. 1, some general concepts are shown visually as input, output, and activation functions—these three terms are used in the computational process of NN. Conveying of data from one neuron to another is shown in this Fig. 1.

D. Acharjee (✉)
Applied Computer Technology, Kolkata, West Bengal, India
e-mail: dulalacharjee@gmail.com

J. Szymanski
Kazimierz Pulaski University of Technology and Humanities, Radom, Poland
e-mail: j.szymanski@uthrad.pl

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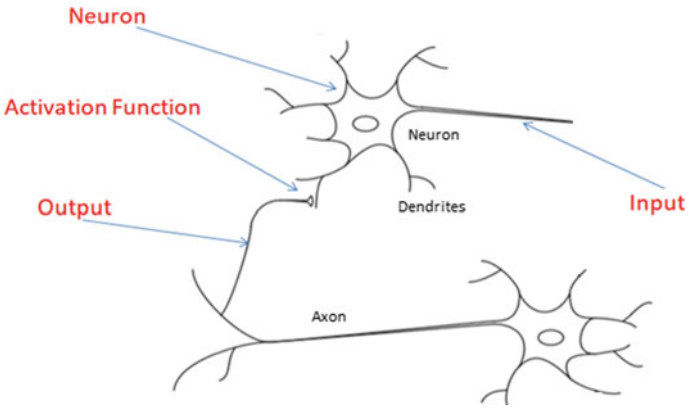

Fig. 1 Model of a neuron showing input/output concept

An incoming impulse can do two types of actions—either it excites a neuron to produce another impulse for neighbor neuron-this is known as firing a neuron, or, it will prevent firing the neuron which is known as an inhibitory effect.

Concept of neural process is simulated by computer's process. Computation of single neuron is shown in Fig. 2.

Here, $p =$ input; $w =$ weight value; It is an example of single input, weight, bias, and single output. $x =$ output of adder as $x = p * w + b$; and $a =$ output of activation function, $f()$. The reason for doing so many things is that there is a difference between "input value" and "expected value" and the aim is to minimize this difference to get the target output. Input value (p) is multiplied by a small weight value (w); then, that value is summed with a bias value (b); finally, output of summer is, $x = pw + b$; then, this value is given as input to activation function, $f(..)$, which is shown in Fig. 1 as: $x = f(pw + b)$. Activation function is also known as transfer function.

Activation function can be a nonlinear or linear function as some names are: Sigmoidal, hyperbolic tangent, Gaussian, Radial Basis Function (RBF); these are nonlinear functions. Examples of linear functions are hard limit, symmetric hard limit, saturating linear, etc.

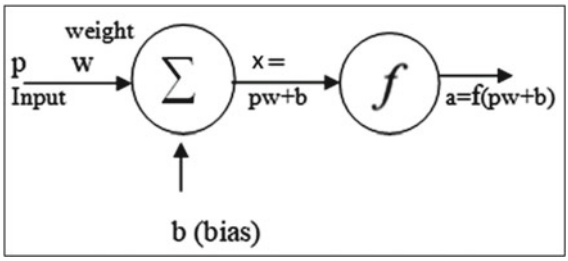

Fig. 2 A feed forward neural network

2 Recurrent Neural Network (RNN)

It is a network with feedback; a portion of output is connected as feedback to its input line. As general, RNN has a back directional connection from output to input line. In feed forward NN, the output is fixed for a fixed input for a particular activation function. But, in RNN, output is a function of time, as many times it will iterate—output will be changed.

A discrete-time RNN is shown below; it is like Hopfield NN where output is initiated from its input having associative memory. At the initial stage, $a(t) = p$, the input value. In this model, for next iterations, weight value is changed; bias is given once. Output $a(t)$ is updated with discrete-time increment of "1" as $t, t + 1, t + 2 \ldots$ etc. at each iteration, weight value is updated as [2, p. 66]:

$$w(t + 1) = w(t) \pm \Delta w \tag{1}$$

Using any function Δw can be computed. Generally, it is derivative of output with respect to weight value. In Fig. 3, a model of RNN is shown, where, output is a function of previous input as shown in Eq. (2) as [1, p. 49]:

$$a(t + 1) = f(w * a(t) + b) \tag{2}$$

2.1 Steps of Computations

In Fig. 3, a model of self-feedback processing is shown. It is like iterating a loop within a neuron or a process that changes its own value at each iterations. At initial stage, output is nothing but the input value, p; after that of—input is not involved in processing as shown below. Main point of observation is that in this case, both output and weight values are changed at each iterations.

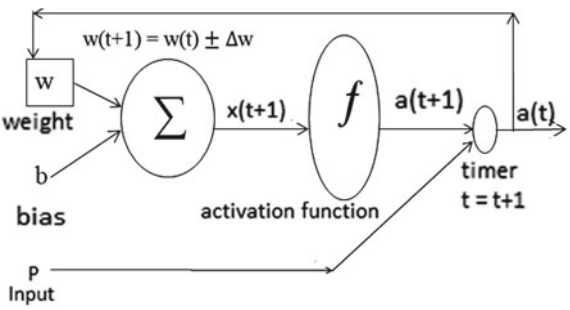

Fig. 3 Model of single layer-RNN or self-feedback

$t = 0$; $a(t) = p$; input value;
$t = 1$; $a(1) = f(a(0) * w(0) + b)$;
$t = 2$; $a(2) = f(a(1) * w(1) + b)$.

Where $w(1) = w(0) + \Delta w$.
So, the output at nth iteration when $t = n$ is

$$t = n : a(n) = f(a(n-1) * w(n-1) + b); \tag{3}$$

Equation (3) is the generalized equation of this model. It is also known as updating output value. Always, this output remains nearer to initial input value, p. In associative memory logic, values of weight, output, and time are stored within arrays that if required, previous values could be recalled for interest of analysis of the model [2, p. 98].

3 Updating Weight Value

Equations (1)–(3) show that Δw, a small portion of a value, is added or subtracted from the previous weight value. So, here, two questions arise,

1. What is that small value?
2. Will it be added or subtracted from previous weight value?

To get the answer of the first question, we shall calculate derivative of output, $a(t)$, with respect of weight value, $w(t)$ as, at any nth iteration, the generalized equation of computing weight value is:

$$\Delta w_n = \frac{\partial}{\partial w_{n-1}} a(n-1) \tag{4}$$

Or, we can say, it is the derived value of output in respect of weight value.

To get the answer to the second question, we need to know whether it is to find gradient descent point or gradient ascent point. For finding gradient descent value, it is required to subtract from previous weight value. And for finding maximum optimized value, Δw should be added with previous weight value as shown in above Eq. (1). So, in Eq. (1) it was used the operator sign plus or minus, $\pm$.

For accelerating or smoothing the progression of optimization curve, sometimes derived component is multiplied by learning rate which is discussed in the next section.

3.1 Learning Rate

Learning is a process to achieve the expected value. Within many steps, input value will reach nearer to the expected value, this process is known as learning about expected value. In how many steps or iterations, input value will reach to minimum or maximum optimized value is known as resolution. If it is less, then resolution gap will be more, and if it is more, i.e., by more number of steps expected output is achieved, the resolution becomes smaller in size. Let us describe with an example, say, input, $p = 2.6$, expected value, $y = 2.5$ in case of gradient descent method. Then, $2.5 - 2.6 = -0.1$ to be achieved within n (say 10) number of iterations. In this case, average increment $= -0.1/10 = -0.01$ which is known as learning rate (generally). Or in another way, if n numbers of times derivatives are performed on a function, then, average of these n number of values is known as learning rate (α, alpha). As shown in Eq. (5), multiplying the derivative accelerates or decelerates the growth rate. In that case, adjustable weight value becomes:

$$\Delta w_n = -\alpha \frac{\partial}{\partial w_{n-1}} a(n-1) \tag{5}$$

Here, as mentioned in Eq. (5), multiplying by learning rate (α, alpha) may be called another form of enforcement to output [3, p. 112].

4 Multiple Inputs and Single Output

In human brain, a neuron gets impulses or inputs from large number of neighbor neurons. So, in viewpoint of computer processing, for simulation of multiple inputs and multiple weight values, the diagram of a single neuron is as Fig. 4.

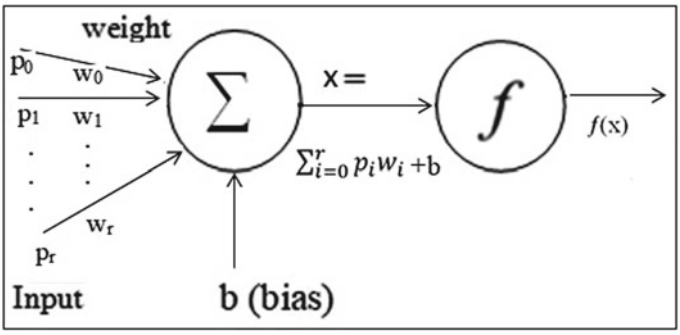

Fig. 4 Single neuron with multiple inputs

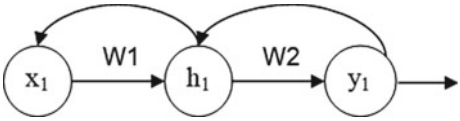

Fig. 5 Example of recurrent loops

In this case, there is a set of input vectors as $P = \{p_0, p_1, p_2 \ldots p_r\}$ and set of weight vectors as $W = \{w_0, w_1, w_2 \ldots w_r\}$. As shown in Fig. 4, weighted inputs are summed with bias value as

$$x = \sum_{i=0}^{r} p_i w_i + b \tag{6}$$

Activation functions, $f()$, takes x as input, and generates final output value as $a = f(x)$. It is noted that bias, b, is added once with weighted sum of input and weight value.

For simplicity, here in Fig. 4, input and weight lines are shown by the same line.

5 Computing with Hidden Neurons for RNN

In this section, parameters are assumed as x for input, h for hidden node, and y for output node.

5.1 One Input, One Hidden and One Output Neuron

Below, an example of a simple network of one input, one hidden and one output node is shown. Weight updating steps are shown in Fig. 5 as mentioned in Eqs. (7) and (8).

Updating Weight Values

According to previous recurrent formula, weight values at $(t + 1)$th time is:

$$w_2^{t+1} = w_2^t \pm \alpha \frac{\mathrm{d}E^t}{\mathrm{d}w_2^t} \tag{7}$$

and

$$w_1^{t+1} = w_1^t \pm \alpha \frac{\mathrm{d}E^t}{\mathrm{d}w_1^t} \tag{8}$$

where E^t = error value at time t.

Advantages of using iterative notations like t, $t+1$, $t+2$, etc. are that all weight values are stored within an array of weight, w. In any case, if previous weight values are required for checking, then we can look over the array data. It is known as associative memory which occupies lot of memory and power. But if, previous memories of weight values are not required, only a single variable can compute all operations, in that case, we can write as [2, p. 254]:

$$w2 = w2 \pm \alpha \frac{\mathrm{d}E}{\mathrm{d}w2} \tag{9}$$

In this case, left side, $w2$, of the equation is the updated weight value and $w2$ of right side of the equation is the immediate past weight value. As a proposal of computing steps, in the computer, right sides are computed first and then substituted within left parameter. Previous weight value $w2$ is lost and $w2$ is newly filled with a new value. So, another new parameter is not required to hold the right side's computed value.

Where E^t is known as error-index value at tth time; it is computed as using MSE (Mean of Square Errors) rule [4]:

$$E^t = \frac{1}{2}(\text{target} - \text{output}(y1, t))^2 \tag{10}$$

where $(y1, t)$ is the value of $y1$ at time t.

Output value of output layer is computed through activation function. Say, if activation function is Sigmoidal, then, output value of $y1$ is:

$$\text{output}(y1, t) = f(y1, t) = \frac{1}{1 + \mathrm{e}^{-y1,t}} \tag{11}$$

Putting this value in Eq. (10), we can compute the value of E^t. Then, putting this value of E^t, we can get updated weight value of $w1$ and $w2$ from Eqs. (7) and (8).

These updated weight values are used in next iterations or next loops for computations.

6 Computing with Two Input, Two Hidden and Two Output Neurons

Here, discussion will be given on a model of network as shown in Fig. 6 having two inputs, two hidden and two output neurons. Here, $h1$ and $h2$ form a hidden layer.

In Fig. 6, two input nodes make input layer; $h1$ and $h2$ nodes make hidden layer; $y1$ and $y2$ make output layer. In this model, each node has two inputs and a bias value. All input lines are connected with weight values as shown by w with a number. For

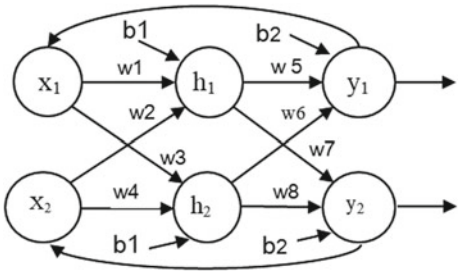

Fig. 6 A model of 2×3 nodes with hidden layer at the middle

simplicity of computation, both hidden nodes are biased by value, $b1$; and output nodes are biased by value, $b2$.

Feed Forward Computing

Here, for each of the hidden nodes, there are two inputs as shown in Fig. 6. In the same way, each output node has two inputs also. From Eq. (6), for multiple input values, the computations become:

$$h1 = x1 * w1 + x2 * w2 + b1 \tag{12}$$

$$h2 = x1 * w3 + x2 * w4 + b1$$

$$\text{Output of } h1 = O_{h1} = f(h1)$$

$$\text{Output of } h2 = O_{h2} = f(h2)$$

$$y1 = O_{h1} * w5 + O_{h2} * w6 + b2 \tag{13}$$

$$y2 = O_{h1} * w7 + O_{h2} * w8 + b2$$

$$\text{Output of } y1 = O_{y1} = f(y1)$$

$$\text{Output of } h2 = O_{y2} = f(y2)$$

Feed Back Computation

In Fig. 6, there are two output lines, and say, experimental outputs are O_{y1} and O_{y2}. In the supervised learning method, we should have two target values also in hand. At each iteration of computing, errors are computed and tried to achieve the nearest value to the target value. Say, these target values are T_1 and T_2. Our aim is to reach to optimized point of T_1 and T_2.

Now, from Fig. 6, let us compute error-index for weight value, $w5$, for adjusting weight value at the time of recurrent process:

$$\text{Say, error} = E = \frac{1}{2}(T1 - O_{y1})^2 + \frac{1}{2}(T2 - O_{y2})^2 \tag{14}$$

Generally, error-index is computed by differentiating error with respect to $w5$ and it is $\frac{dE}{dw5}$.

But, if we look at the equation of error formula, E, we see it is not differentiable with respect to $w5$, in computation of error—$w5$ is not related or dependent directly. So, we need to find out dependencies following chain rule [4].

Dependency sequences chart is like this:

Error < output of $y1$ < $y1$ < $w5$.

As shown in Fig. 6 for computing the values, error is directly related to "output of $y1$ or O_{y1}" which is directly related to $y1$ and finally, input value $y1$ is related to $w5$.

This chart shows that error is far away from $w5$ and if we find derivatives of error with respect to $w5$, we need to step three stages as shown in Eq. (15).

Following the chain rule, we can decompose and write it as a multiplication of three differential components as Eq. (15):

$$\frac{dE}{dw5} = \frac{dE}{dO_{y1}} * \frac{dO_{y1}}{dy1} * \frac{dy1}{dw5} \tag{15}$$

Therefore, final adjusted weight value is

$$w5 = w5 \pm \alpha \frac{dE}{dw5} \tag{16}$$

In Fig. 6 and from Eq. (15), it is shown that $\times 1$ and $\times 2$ have no direct role in weight updating of weight value, $w5$. As equations derived, similar equations should be formulated for updating weights of $w6$, $w7$, and $w8$.

Updating Weight Values

From Fig. 6, it is shown that $w1$ is one layer behind of output layer, so, it has no direct relation to produce output of $y1$ (say). Computing processes of updating $w1$ have many steps and discussed below:

We know from basic formula of weight updating that,

$$w1 = w1 \pm \alpha \frac{dE}{dw1}$$

Now, we have to compute error derivative in respect of $w1$, i.e., $\frac{dE}{dw1}$. Following the chain rule of dependencies, we can write

$$\frac{dE}{dw1} = \frac{dE}{dO_{h1}} * \frac{dO_{h1}}{dh1} * \frac{dh1}{dw1} \tag{17}$$

where, O_{h1} is the output of hidden node $h1$.

It is seen that E, is not directly related to output of $h1$, so, we have to compute derivative of total error, E, with respect to output of $h1$ and $h2$, as:

$$\frac{\mathrm{d}E}{\mathrm{d}O_{h1}} = \frac{\mathrm{d}E1}{\mathrm{d}O_{h1}} + \frac{\mathrm{d}E2}{\mathrm{d}O_{h2}} \tag{18}$$

where $E1$ and $E2$ are errors produced at node $y1$ and $y2$, respectively. Again two components of right-hand side of Eq. (18) to be decomposed with its dependent terms and those sections are avoided in this paper.

In this way, all independent components to be decomposed to dependent components for making derivatives, and finally, we can compute the value of $\frac{\mathrm{d}E}{\mathrm{d}w1}$ and we can adjust the value of $w1$ for next iteration which is the basic idea of RNN. In that way, other weights of this layer, $w2$, $w3$, and $w4$, can be formulated for updating. Then as shown in Fig. 6, next iteration can be computed using updated weight values as discussed above. For any model of RNN, here, basic processes of computations are formulated and explained with mathematical equations.

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The Mathematical Modeling Validation for Fault Location Technique in Parallel Transmission Lines

A. Naresh Kumar, G. Kranthi Kumar, V. A. Sankar Ponnapalli, and M. Chakravarthy

Abstract In this article, a novel technique based on an artificial neural network is proposed to locate the cross-country fault in an incomplete journey parallel transmission line. The proposed technique is employed using voltages and currents of single end of line to avoid the requirement of the communication channel. The discrete Fourier transforms is used to preprocess the signals. Levenberg–Marquardt method is selected for the training of artificial neural networks. The proposed technique is a negative effect by change in different attributes viz. fault types, fault inception angles, fault locations, and fault resistances. The comparison study of different techniques with artificial neural networks carried out and also validated with mathematical modeling. The key advantage of the technique is that it correctly estimates the locations of cross-country faults and also shunt faults, hence making it precise and reliable as compared to other techniques.

Keywords Artificial neural network · Cross-country faults · Multiple linear regression

1 Introduction

At present, complete journey parallel transmission line having the common tower, however, incomplete journey parallel transmission (IJPT) line on the same tower structure has been spawned in engineering because of different geographical environments and transmission requirements [1–3]. These transmission lines partially take the same tower construction. For instance, the outlet ends of the transmission line are set up on the common bus and the same tower, the central part is separated into

A. N. Kumar (✉) · G. K. Kumar
Institute of Aeronautical Engineering, Hyderabad, India
e-mail: ankamnaresh29@gmail.com

V. A. Sankar Ponnapalli
Sreyas Institute of Engineering and Technology, Hyderabad, India

M. Chakravarthy
Vasavi College of Engineering, Hyderabad, India

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two single circuit transmission lines, and the end parts are attached to two separate substations; the front and back parts of the line are separated into two single circuit transmission lines, and the central part is set up on the same tower, etc. The ends of two single circuit transmission lines are connected to different substations, respectively, so the lengths of two single circuit transmission lines are not equal. Therefore, the IJPT line cannot be completely regarded as two independent single circuit transmission lines or double circuit transmission line. Due to the special nature of the IJPT line, the traditional protection scheme and the six sequence fault components will no longer employ. Quick detection and accurate fault location of the faults in the transmission line play a vital role in improving the reliability of the power system. So it is essential to analyze the performance of protection schemes when the faults occur in the IJPT line.

Most of the research on double circuit transmission lines against shunt faults carried out in Refs. [4–7]. Different fault location methods [8, 9] for double circuit transmission lines have been developed based on the data of one terminal. Ref. [10] demonstrated artificial neural networks and constructs the location algorithm according to different fault types using the data of one terminal. The schemes [11, 12] require without knowing the fault classification to locate the faults. All these methodologies [4–12] do not take into consideration the cross-country faults. These faults are adversary to conventional technique performance. Moreover, a malfunction of distance relays may lead to three-phase trips of two circuits of line. The impact of misoperations can be predominantly serious under various conditions. Therefore, the location technique for cross-country faults has gained an increasing interest. In addition, very few studies on the location of cross-country faults have been published. Therefore, it is academically and practically meaningful to study for accurately location cross-country faults.

Cross-country faults may occur in different phases at more than one location of the incomplete journey parallel transmission line during thunderstorms. There have been several articles discussing cross-county faults in transmission line [13, 14]. The authors of [15] use the currents as the inputs to locate cross-country faults. However, these systems have addressed for complete journey parallel lines only. Fault location techniques for IJPT line have been described in [16, 17]. In this paper, a novel location technique for cross-country faults on IJPT line based on ANN is proposed. This work is a continuation of the previous investigation [17] and extends the application of fuzzy from shunt fault location in IJPT line. The main highlights and novelty of the paper are summarized as (1) Implementation of a location algorithm for IJPT line using single terminal current data only (2) Implementation of an ANN training for selection of best architecture, biases, and weights (3) Performance evaluation of the proposed technique for an extensive range of fault parameters. (4) The proposed technique is validated with mathematical modeling.

This paper is organized as follows. Section 2 describes the IJPT line configuration, designing, and simulation of cross-country faults. Section 3 is intended to explain the ANN algorithm for fault location. Section 4 presents the test results and performance evaluation. Finally, the conclusion is given in Sect. 5.

2 Incomplete Journey Parallel Transmission Line Under Study

A 400 kV IJPT line is developed in MATLAB/Simulink environment. The circuit topology of an IJPT line during cross-country fault condition is depicted in Fig. 1. At bus B_1, source S of IJPT line is connected which transfers power to R_1 at bus B_2 and R_2 and bus B_3. From the middle part, M of IJPTL is separated into two single circuit lines namely M-R_1 and M-R_2 which are connected to two different substations ER_1 and ER_2. Here S-M length is 100 km for both the circuits. At bus-2, substation of ER_1 of 210 MW is connected through a 100 km transmission line (M-R_1). Thereafter the power is transferred through 200 km transmission line (M-R_2) to ER_2 400 kV grid at bus-3. The current voltage signals of two circuits undergo changes during faults in any one circuit of the incomplete journey line. So these signals of both the circuits are taken as inputs of the supervised learning technique. The main job of faulty location is to find the distance of faults, thus it is considered that the length of the IJPT line is the output given by the supervised learning technique. Thus, the ANN input and the output matrixes A and B, respectively are

$$A = [\text{If1a, If1b, If1c, If2a, If2b, If2c, Vfa, Vfb, Vfc}]$$
$$B = [\text{L1a, L1b, L1c, L2a, L2b, L2c}]$$

where Vfa, Vfb, and Vfc are voltage signals measured from the source terminal, If1a, If1b, and If1c, are current signals of circuit 1, and If2a, If2b, and If2c, are of circuit 2 recorded at the source terminal. L1a, L1b, L1c, L2a, L2b, L2c are output locations. Current and voltages waveforms of IJTP line are shown in Figs. 2 and 3 respectively.

The MATLAB®7.01 software simulates cross-country fault in each phase of circuits. The current voltage signals of both the circuits are collected at source end of the transmission line with sampling frequency of 1.2 kHz. Further signals are processed by simple second-order Butter worth low-pass filter by a cut-off frequency of 480 Hz. The three-phase voltage and six-phase current signals has been estimated using Discrete Fourier Transform (DFT) tool of MATLAB2015® software. In order to train the ANN, the training and testing faults are simulated for various combinations of faulty conditions. The simulation of the training and testing faults is illustrated in Table 1.

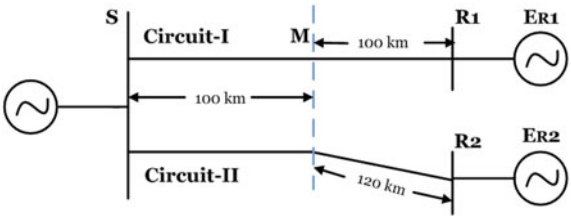

Fig. 1 The circuit topology of an IJPT line

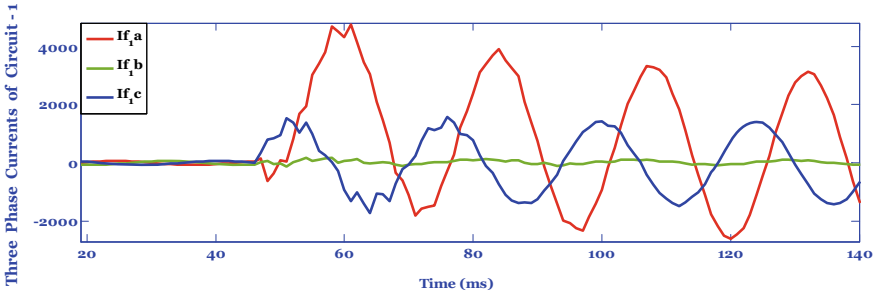

Fig. 2 Current waveform

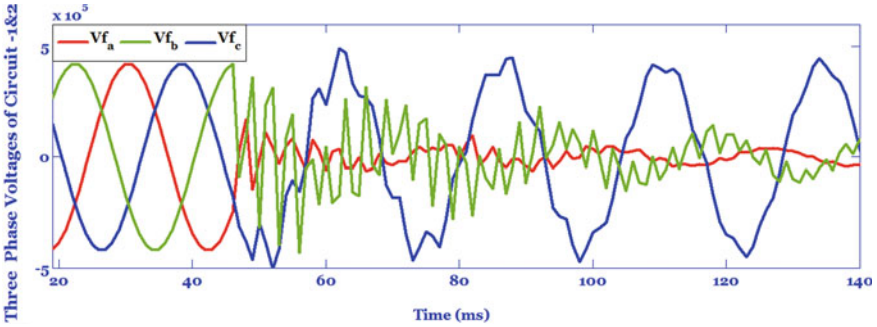

Fig. 3 Voltage waveform

Table 1 The generation of dataset

Fault parameters in IJPT line	Training data for ANN	Test data for ANN
Type of fault	(A1B1G, B1A1G), (C1B1G, B1C1G), (A1C1G, C1A1G), total no of cross-country faults = 6	(A1B1G, B1A1G), (C1B1G, B1C1G), (A1C1G, C1A1G), total no of cross-country faults = 6
Fault resistance (Ω)	0, 100	10–110 (in steps of 20 Ω)
Fault inception angle (°)	0, 90, and 270	0–360 (in steps of 50°)
Fault location (km)	Fault-1: (1–219) in steps of 21 km Fault-2: (1–219) location (1, 10, and 220) from fault-1 location Total no. of fault locations = 30	Fault-1: (1–219) in steps of 21 km Fault-2: (1–219) location (1, 10, and 220) from fault-1 location Total no. of fault locations = 30
Total no. fault cases	$6 \times 2 \times 3 \times 30 = 540$	$6 \times 2 \times 3 \times 30 = 540$

3 Proposed Technique

ANN has proved to be a powerful scheme for various aims including classification, fault detection, and estimation. Several ANNs are analyzed and trained to get a successful ANN architecture that satisfies the necessities of this research. The ANN model is determined according to the learning algorithm, hidden layers, activation function, and network architecture. Due to their capability of dealing successfully with nonlinearities and their benefits in real-time applications, it is convenient to develop ANN for locating faults. Basic architecture of ANN is shown in Fig. 4.

In this paper, ANN with a supervised learning technique is used. The normalized values of the six current and three voltages are as inputs of the ANN. Faulty location ANN model has six outputs for representing L1a, L1b, L1c, L2a, L2b, and L2c. The tangent sigmoid is used as a transfer function for both the hidden layers and the output layer. It is trained via Levenberg–Marquardt method with the set of mean square error of 10^{-5}. The mean square error is 9.99e−06 with 342 epochs in around 2 min computation time on a computer (i5, 2.4 GHz, 4 GB RAM). When the training and testing process is finished, MATLAB found 20 different valid ANN networks to operate. Among them, the ANN network with (9-18-18-6) architecture was chosen because it had the lowest errors. The ANN final architecture for faulty location has nine input neurons, two hidden layers each with eighteen neurons, and six neurons in output layer. Figure 5 shows the architecture of optimal ANN-based cross-country fault locator.

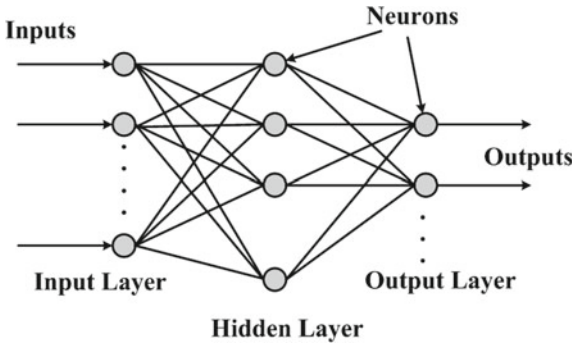

Fig. 4 Structure of ANN

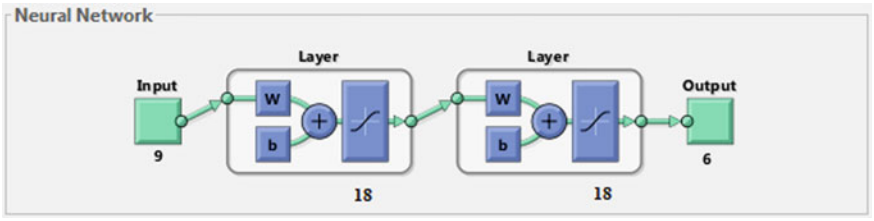

Fig. 5 The architecture of optimal ANN

Table 2 The performance of ANN for different inception angles

Fault inception angle (°)	L1a	L1b	L1c	L2a	L2b	L2c	Error rate for fault-1	Error rate for fault-2
10	29.10	200	78.08	220	220	220	0.050	0.040
50	28.88	200	78.15	220	220	220	0.060	0.075
100	29.23	200	77.96	220	220	220	0.115	0.020
150	29.14	200	77.80	220	220	220	0.070	0.100
200	29.02	200	78.06	220	220	220	0.010	0.030
250	28.73	200	78.28	220	220	220	0.135	0.140
300	29.25	200	78.31	220	220	220	0.125	0.155

4 Performance Evaluation

The reliability of the proposed protection technique under different fault scenarios has been evaluated in this section. Supervised learning based technique ANN for faulty location in IJPT line is checked with cross-country faults, fault inception angle, fault resistance, and fault location. The error rate is calculated using Eq. (1). Results of supervised learning technique are discussed hereunder.

$$\text{Error Rate } (\%) = \frac{\text{actual} - \text{Estimated } L}{\text{Line Lenth}} \times 100 \tag{1}$$

4.1 The Performance of ANN for Different Fault Inception Angles

The faults can take place with any fault inception angle at any time; therefore, to examine its effect on the suggested location framework, a variety fault inception angles of faults have been considered. In order to show the impact of fault inception, the fault in the fixed location with constant resistance at the various fault inceptions has been applied. Some of the test results of faulty location changing fault inceptions during cross-country faults are listed in Table 2. The error rate of the fault location in IJPT line remains satisfactory regardless of the variation in the inception angle.

4.2 The Performance of ANN for Different Fault Resistances

Normally, ground fault may occur with fault resistance. Small amount of fault current flowing in case of high resistance fault at source end in comparison with other fault situations and it cannot be located by the conventional technique. For this reason, it

Table 3 The performance of ANN for different resistances

Fault resistance (Ω)	L1a	L1b	L1c	L2a	L2b	L2c	Error rate for fault-1	Error rate for fault-2
10	200	200	200	192.19	220.82	220	0.086	0.081
30	200	200	200	192.03	221.18	220	0.013	0.081
50	200	200	200	191.94	221.35	220	0.027	0.159
70	200	200	200	192.09	221.26	220	0.040	0.118
90	200	200	200	192.17	221.04	220	0.077	0.018
110	200	200	200	191.80	221.02	220	0.090	0.009

is significant to investigate the impact of fault resistances on the proposed method. In order to show the influence of fault resistance, the fault of invariable location with fixed inception at various fault resistances have been employed. The error rate of each fault for various fault resistances is given in Table 3. As it is shown, the error rate of the fault location in IJPT line remains acceptable despite the change in the fault resistances.

4.3 The Performance of ANN for Different Fault Locations and Fault Types

The main purpose of the suggested technique that it is the application of cross-country faults. In order to study impact of fault type and fault location, the fault in the constant inception with invariable resistance at the various fault location and fault type has been used. The data set applied to test the performance of framework is presented in Table 4. According to the results of Table 4, it can be seen that the suggested framework for the cross-country faults in the IJPT line has an acceptable error rate. From experiment results, it can be noticed that the proposed technique is able to correctly locate all the cross-country faults.

4.4 Mathematical Modeling Validation

Mathematical modeling is developed for the locations of cross-country faults using multiple linear regressions (MLR). Regression technique has been used widely in many projects more than other prediction methods. MLR technique is function of additive and linear associations of the explanatory variables as a predictive study. It attempts to technique the connection between two or more explanatory variables and depended on variables by assumption a linear connection. The performance of MLR is validated to predict the location of cross-country faults from the same inputs and output variables taken for the ANN system. It is assumed that dependent variable L

Table 4 The performance of ANN for different locations and inceptions

Fault-1	Fault-2	L1a	L1b	L1c	L2a	L2b	L2c	Error rate for fault-1	Error rate for fault-2
A-phase fault in circuit-1 at 28 km	B-Phase fault in circuit-1 at 83 km	28.13	83.25	200	220	220	220	0.065	0.125
A-phase fault in circuit-1 at 132 km	C-Phase fault in circuit-1 at 167 km	131.98	200	167.24	220	220	220	0.001	0.012
B-phase fault in circuit-1 at 144 km	C-Phase fault in circuit-1 at 15 km	200	143.86	15.06	220	220	220	0.070	0.030
A-phase fault in circuit-2 at 65 km	B-Phase fault in circuit-2 at 126 km	200	200	200	64.95	125.76	220	0.022	0.109
A-phase fault in circuit-2 at 218 km	C-Phase fault in circuit-2 at 94 km	200	200	200	218.21	220	94.12	0.095	0.054
B-phase fault in circuit-2 at 19 km	C-Phase fault in circuit-2 at 206 km	200	200	200	220	19.30	206.16	0.136	0.072

is related by a linear combination of coefficients b to several independent variables F sample. MLR technique is written according to Eq. (2).

$$L_i = b_0 + b_1 F_1 + b_2 F_2 + b_n F_n \quad i = 1, 2 \ldots 6 \quad n = 1, 2 \ldots 9 \tag{2}$$

where L_i indicates the locations of cross-country faults output variables, b_0–b_n are the coefficients of regression, F_1–F_n is the currents voltage input variables.

$$\begin{bmatrix} N & \sum F_1 & \sum F_2 & \ldots & \ldots & \ldots & \sum F_9 \\ \sum F_1 & \sum F_1^2 & \sum F_1.F_2 & \sum F_1.F_3 & \ldots & \ldots & \sum F_1.F_9 \\ \sum F_2 & \sum F_2.F_1 & \sum F_2^2 & \ldots & \ldots & \ldots & \ldots \\ \ldots & \sum F_3.F_1 & \ldots & \ldots & \ldots & \ldots & \ldots \\ \ldots & \ldots & \ldots & \ldots & \ldots & \ldots & \ldots \\ \ldots & \ldots & \ldots & \ldots & \ldots & \ldots & \ldots \\ \ldots & \ldots & \ldots & \ldots & \ldots & \ldots & \ldots \\ \ldots & \ldots & \ldots & \ldots & \ldots & \ldots & \ldots \\ \ldots & \ldots & \ldots & \ldots & \ldots & \ldots & \sum F_8.F_9 \\ \sum F_9 & \ldots & \ldots & \ldots & \ldots & \sum F_9.F_8 & \sum F_9^2 \end{bmatrix}$$

$$L = \begin{bmatrix} \sum(F_1)L_1 & \sum(F_1)L_2 & \ldots\ldots\ldots & \sum(F_1)L_5 & \sum(F_1)L_6 \\ \sum(F_2)L_1 & \sum(F_2)L_2 & \ldots\ldots\ldots & \ldots & \sum(F_2)L_6 \\ \ldots & \ldots & \ldots\ldots & \ldots & \ldots \\ \ldots & \ldots & \ldots\ldots & \ldots & \ldots \\ \ldots & \ldots & \ldots\ldots & \ldots & \ldots \\ \sum(F_8)L_1 & \ldots & \ldots\ldots & \ldots & \sum(F_8)L_6 \\ \sum(F_9)L_1 & \sum(F_9)L_2 & \ldots\ldots & \sum(F_9)L_5 & \sum(F_9)L_6 \end{bmatrix}$$

$$F = b = \begin{bmatrix} b_0 \\ b_1 \\ \vdots \\ b_9 \end{bmatrix}$$

$$Fb = L$$

$$b = F^{-1}L$$

It can compute the regression coefficients of b matrix by solving the inverse of F matrix. The output of the mathematical modeling is validated the correct fault locations of cross-country faults in the IJPT line. Quantitative comparison of the proposed technique with other soft computing based techniques is given in Table 5.

Table 5 Comparison with other methods

References	Type of fault	Method used	Error rate (%)
Naresh Kumar and Chakravarthy [12]	Multi-location and transforming faults	Fuzzy	0.34
Naresh Kumar and Chakravarthy [10]	Simultaneous faults	ANN	0.41
Anamika et al. [9]	Short circuit faults	ANN	1.6
Naresh Kumar et al. [17]	Shunt faults	Fuzzy	0.32
Proposed framework	Cross-country faults	ANN	0.2

5 Conclusion

The cross-country faults in IJPT line cannot be located with traditional fault location techniques. To estimate the location of cross-country faults on IJPT line, an ANN-based technique is proposed. A sampling frequency of 1200 Hz is employed to measure the transient information and extract the data via Fourier transforms. The supervised network is tested with numerous fault cases to check the performance. The simulation results error rate in fault location is less than 0.2% for most of the fault cases. The proposed technique is found to be correct regardless of faulty type, fault resistance, faulty location, and fault inception angle. The proposed technique overcomes problems such as locating multi-location faults, requirement of both ends of transmission line information, and knowing the fault phase.

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Efficient FPGA Implementation of FIR Filter Using Distributed Arithmetic

Debarshi Datta and Himadri Sekhar Dutta

Abstract This paper briefs realization of pipeline based Finite Impulse Response (FIR) architecture using Distributed Arithmetic (DA) technique which is multiplier-less structure suitable in hardware implementation for area-time efficient design. The performance of the FIR architecture has been significantly increased by introducing carry-save accumulator unit (CSA). The conventional adder based shift accumulation unit for DA-based partial product coefficient computation is replaced by a CSA to reduce the critical path delay. The operating speed has been further improved by involving parallel dual-port random synchronous static access memory (DPSSRAM). The input bits are taken in parallel form, one word per interval. The modified architecture accelerates the FIR filter performance. The proposed DA FIR filter has been tested in Xilinx Virtex-5 (XC5VLX50T) Field Programmable Gate Array (FPGA) board. The implementation results show that the modified DA-based FIR filter with 8-bit input and 16-coefficients is 28.57% area and 50.14% speed efficient than other recent architecture.

Keywords Distributed arithmetic · DPSSRAM · FIR · FPGA

1 Introduction

Digital FIR filters are a vital role in signal processing applications such as communication systems, circuit designs, acoustic and many more [1]. It is a highly stable and linear in phase response. Other advantages include small size, high capacity and fast computing structure. In FIR architecture, as the numbers of taps are increased to achieve desire frequency response, automatically the complexity of the filter

D. Datta (✉)
Department of Electronics and Communication Engineering, Brainware Group of Institutions, Kolkata, India
e-mail: debarshidatta7@gmail.com

H. S. Dutta
Department of Electronics and Communication Engineering, Kalayani Government Engineering College, Nadia, India
e-mail: himadri.dutta@gmail.com

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increases. Hardware-based FIR filters provide high processing speed and provide good accuracy. In this context, the outstanding features of FPGAs such as high flexibility, short time to market, cost and performance make a suitable platform to implement digital FIR filter [2]. Several approaches have been made to improve the performance of the FIR filters. Distributed Arithmetic (DA) based FIR filters have achieved high performances in reconfigurable domain [3–6].

This technique decomposes the Multiplier Accumulator (MAC) operations into a series of LUT access and followed by shift accumulation operation [5]. It is a bit-serial method of computing the inner product of two vectors with a fixed number of cycles. All multiplications and additions are replaced by LUT. LUT is basically Static Random Access Memory (SRAM) based FPGA where all possible binary numbers are stored. For a large memory system partitioning LUT reduces the memory access time. So that, the speed of this system inevitably increases. DA methodology saves the hardware resources and reduces configuration time by using LUT instead of MAC units. DA-based FIR filters in FPGA provides high flexibility and cost-effective [7].

Pipeline and parallel processing technique can be involved in FIR filter to get high performance [8]. Pipeline operation which is basically inserting a register in each stage to reduce critical path delay. This technique improves the speed of the system. But at the same time, this leads to increase in hardware cost and latency. Latency is the time required to complete a single operation. In parallel processing, multiple outputs are obtained at every clock cycle. Applying both of these techniques in FIR filter to increase the throughput and low power consumption circuit.

High speed and low chip area FIR filters are of high demand in real-time applications. This paper addresses pipeline DA FIR filter mapped on FPGA. Multiplier-less DA-based FIR filter reduces the hardware resources and system latency [8]. The goal of this technique is to improve speed of the system and also reduce the number of slices that lead to optimum the area.

The remainder of this paper is divided as follows: The proposed DA-based FIR filter is described in Sect. 2. Simulation results relating to the FPGA implementation are presented and discussed in Sect. 3. Section 4 concludes the paper and scope for future work.

2 FIR Filter with Distributed Arithmetic (DA)

A Finite Impulse Response (FIR) filter, whose impulse function has finite duration, is consisted of multipliers, adders and delay blocks to generate output of the filter. Figure 1 shows the realization of N-order FIR filter.

Where Z^{-1} represents unit delay, $x[n]$, and $y[n]$ represent input and output sequence, respectively, in discrete domain. h[n] is for filter coefficient.

The mathematical expression for N-order FIR filter is given by [1] for $k = 0, 1, 2 \ldots N-1$

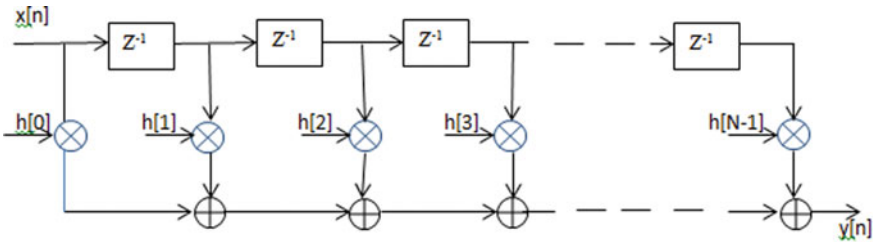

Fig. 1 Conventional FIR filter [1]

$$Y[n] = \sum_{K=0}^{N-1} h[k]x[n-k] \tag{1}$$

2.1 Distributed Arithmetic (DA)

Distributed arithmetic (DA) is a multiplier-less hardware efficient technique to store the pre-computed values into LUTs of FPGAs because multiplication requires large memory sized, and also it is a power-hungry operation. Basically, DA is bit-serial or fully parallel approach. The Eq. (1) can be simplified to remove time index (n), such as

$$y = \sum_{k=0}^{N-1} h_k x_k \tag{2}$$

Consider, For M word length, x_k can be represented in 2's complement and the expression is as follow:

$$x_k = -x_k^0 + \sum_{m=1}^{M-1} x_k^m 2^{-m} \tag{3}$$

where x_k^m represents the mth bit of x_k.The output y of word length M of the Eq. (2) can be rewritten as follows:

$$y = \sum_{K=0}^{N-1} h_k \left(-x_k^0 + \sum_{m=1}^{M-1} x_k^m 2^{-m} \right) \tag{4}$$

Or,

$$y = \sum_{K=0}^{N-1} h_k\left(-x_k^0\right) + \sum_{m=1}^{M-1} 2^{-m}\left[\sum_{k=0}^{N-1} h_k x_k^m\right] \tag{5}$$

2.2 Realization FIR Filter Using DA

The DA-based FIR filter involves LUT, shift registers and scaling accumulator. The coefficients are fixed values, the term $\sum_{k=0}^{N-1} h_k x_k^m$ from Eq. (5) have 2^N possible values; $h_1 x_1^m$, $h_2 x_2^m$, $h_3 x_3^m$ … $h_{N-1} x_{N-1}^m$. All of these values are pre-computed and store in LUT which is address by N-bits.

Consider, a FIR filter has $N = 4$, then the memory words are $16(2^4)$ which are store in LUT. Hence, the general expression is as follows:

$$\sum_{k=0}^{N-1} h_k x_k^m = h_0 x_0^m + h_1 x_1^m + h_2 x_2^m + h_3 x_3^m \tag{6}$$

The content of LUT is shown in Table 1 for 3rd order FIR filter.

The computation can be performed either serially or parallel hardware approach, shown in Fig. 2. The four-order FIR filter with DA method has required for a very

Table 1 24 Word of LUT data

Address				LUT contents (DATA)
0	0	0	0	0
0	0	0	1	h_0
0	0	1	0	h_1
0	0	1	1	$h_0 + h_1$
0	1	0	0	h_2
0	1	0	1	$h_0 + h_2$
0	1	1	0	$h_1 + h_2$
0	1	1	1	$h_0 + h_1 + h_2$
1	0	0	0	h_3
1	0	0	1	$h_0 + h_3$
1	0	1	0	$h_1 + h_3$
1	0	1	1	$h_0 + h_1 + h_3$
1	1	0	0	$h_2 + h_3$
1	1	0	1	$h_0 + h_2 + h_3$
1	1	1	0	$h_1 + h_2 + h_3$
1	1	1	1	$h_0 + h_1 + h_2 + h_3$

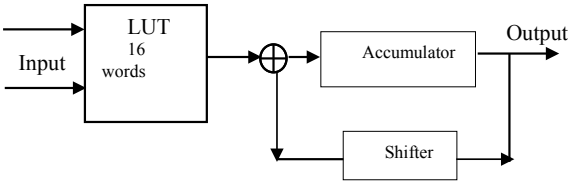

Fig. 2 LUT-based FIR filter [9]

small area, since only single LUT is used for implementing 2^4 memory locations. The inputs are collected from input registers at the input sample rate and coefficients (16) are stored in LUT.

The limitation of this method is only one sequence of bits are accessed at a time, after completion of the first sequence, the next sequence of bits are proceeds. This makes a high time consumption which diminishes the performance of the FIR filter design. To reduce the processing time, a modified DA FIR architecture has been proposed.

2.3 Proposed FIR Filter Using DA

The pipeline approach is used in FIR filter to achieve high speed and low power consumption [10]. Applying this technique incorporates DA topology in FIR filter which provides high efficient filter design, shown in Fig. 3. The parallel inputs are taken in each input sample rate and the pre-computed values which are obtained from coefficients of the FIR filter, are stored in Dual-Port Synchronous Static Random Access Memory (DPSSRAM) [11]. The size of DPSSRAM grows exponentially with an increase in filter order and makes a complexity. This problem can be alleviated by slicing DPSSRAM into the desired number. It reduces memory size and improves memory access time. Using this methodology, an area-time efficient FIR filter is realized.

The first sequence X_in 0 which are $x_0[0], x_0[1], x_0[2], \ldots, x_0[N-1]$ accessed by DPSSRAM. Simultaneously, the next sequence X_in 1 ($x_1[0], x_1[1], x_1[2], \ldots, x_1[N-1]$) are accessed by DPSSRAM. Hence, DPSSRAMs work in parallel and corresponding outputs are shifted and summed to get partial product results. To improve the operating speed, a carry-save accumulator (CSA) is used instead of conventional shift/add accumulation. This modified DA FIR filter improved throughput rate.

Figure 4 shows Dual-Port Synchronous Static Random Access Memory (DPSSRAM) where one port allows data is to be written and read, while the other port only allows data is to be read [11]. Though the dual-port circuit area is larger than single-port memory but due to fast memory access time, it is frequently used in high-speed system.

Dual-port memory has separate address decoders and data multiplexers for each access port.

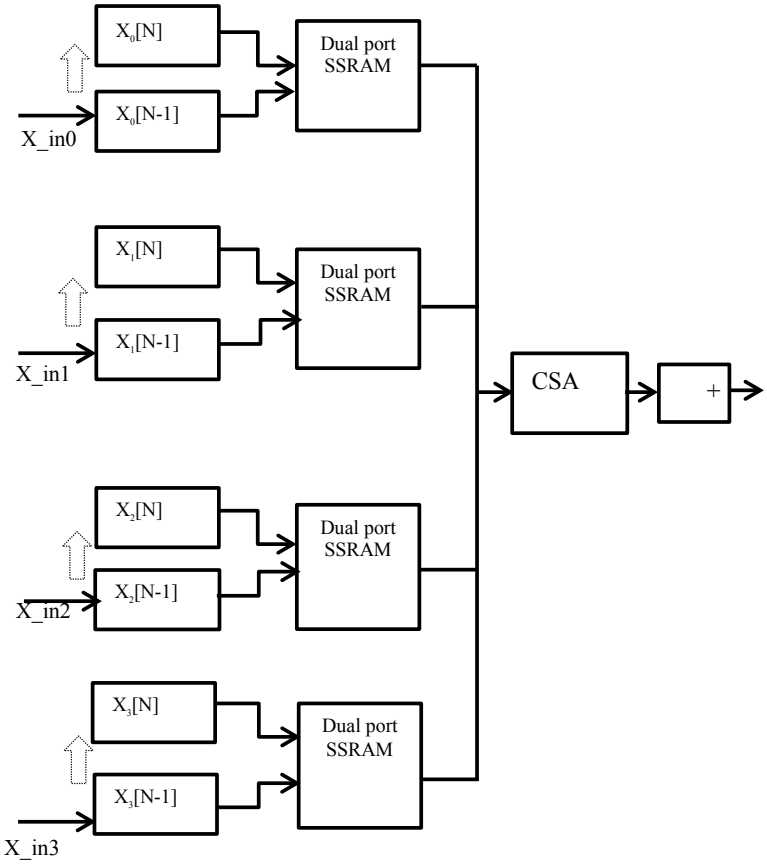

Fig. 3 Proposed pipelining DA FIR filter

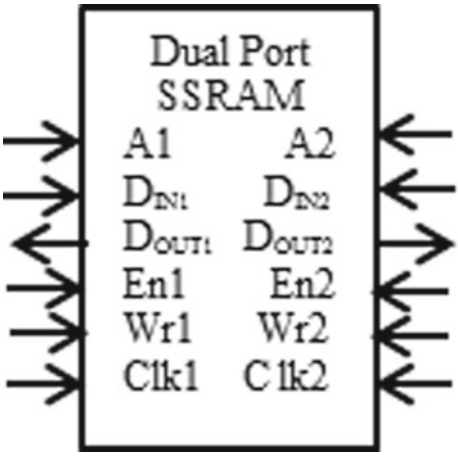

Fig. 4 Dual-port SSRAM [11]

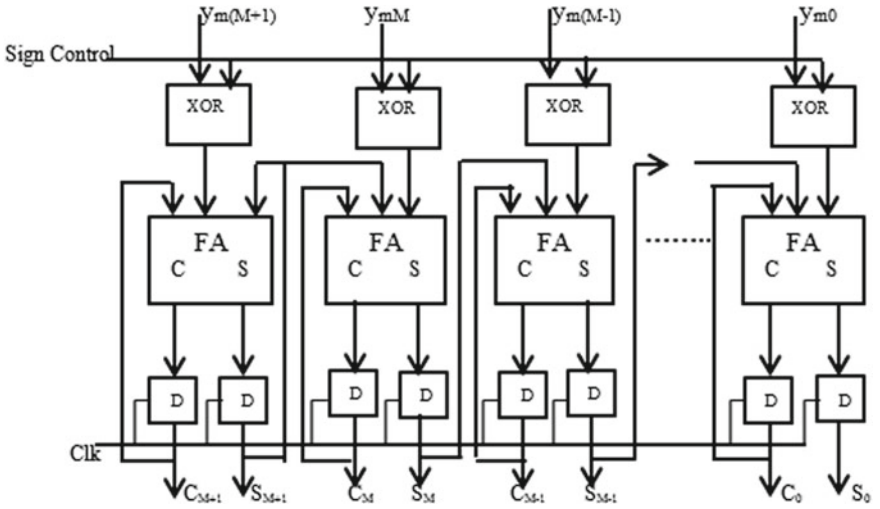

Fig. 5 Carry-save implementation of shift accumulation [11]

The critical path delay introduced in shift accumulation can optimize using carry-save accumulator (CSA), as shown in Fig. 5 [11].

Since, the vector h is set up one after another, the next in the least significant bit (LSB) fashion to the most significant bit (MSB) order to the CSA unit. Further, the negative (2's complement) of the DPSSRAM output needs to be accumulated in case of MSB address slices. Therefore, the DPSSRAM outputs of all the bits which are fed into XOR gates with a set sign control input only when the MSB slice acts as address. The output of XOR gates produces the 1's complement of the DPSSRAM output analogous to the MSB address slice without affecting the output for other bit slices. Finally, the sum and carry words which are obtained after clock cycles to be added by a final adder which is not shown here, i.e. (after the CSA unit) and the input carry of the final adder is required to be set to 1 on account for the 2's complement operation of the DPSSRAM output corresponding to the MSB slice.

3 Simulation Results

The pipelined DA-based FIR filter has been simulated using Xilinx ISE Design Suite 14.7 for synthesis and then synthesized bits are implemented on FPGA device. Here, Virtex-5 XC5VLX50T is the target device. This work is analyzed for 4-bit inputs 4-coefficients and 8-bit input with 16-coefficients DA FIR filters. In Fig. 6, this shows the simulation waveform of 4-bit input and 4-coefficients FIR architecture with DA method.

Table 2 shows hardware resource utilization and Table 3 represents the computation speed of various bit length proposed FIR architecture.

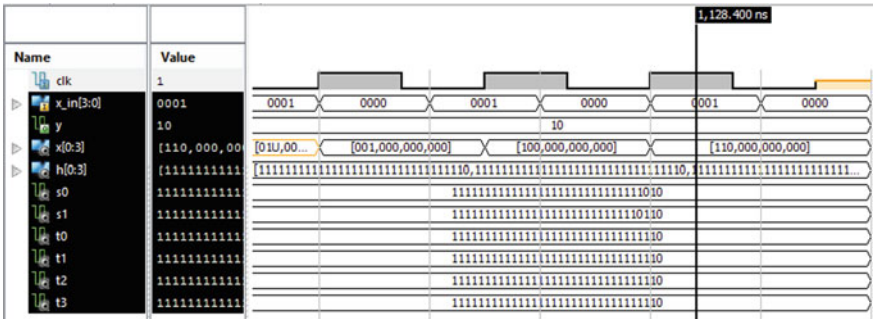

Fig. 6 Simulation waveform for 4-bit input and 4-coefficients FIR architecture with DA method

Table 2 Device utilization summary of proposed pipelined FIR filter using DA

Synthesis parameter	4-bit input and 4-coefficients	8-bit input and 16-coefficients
Number slice registers	19	98
Number of slice LUTs	27	94
Number used as flip-flops	19	98
Number of IOBs	12	25

Table 3 Measurement of computation speed for different orders of FIR architectures

Proposed FIR architecture	Max. Frequency in MHz (speed)
4-bit input and 4-coefficients	301.051
8-bit input 16-coefficients	136.632

Comparisons of proposed work with previous architectures are tabulated in Table 4. The proposed 8-bit input and 16-coefficients FIR filter is compared in terms of slices which indicate area and operating speed to the other DA FIR architectures. The proposed model reduces the slices because of decomposition of the DPSSRAM

Table 4 Performance report of proposed architecture with other existing architecture

Architecture for filter order 8	Number of slices (area)	Max. frequency in MHz (speed)
Meher et al. [3]	133	74.025
Yoo et al. [4]	146	70.552
Eshtawie et al. [5]	140	87.96
Meher et al. [6]	126	91
Proposed DA FIR 8-bit input 16-coefficients	98	136.632

and this makes enhance the operating frequency. Result analysis indicates that the proposed methodology is most area-speed efficient than other works. The proposed DA FIR filter saves up to 28.57% area and also improves the speed of nearly 50.14%.

4 Conclusion

This paper presents a prototype for implementing FIR filter using DA-based technique both in mathematical models and hardware architecture. In this method, the parallel DA FIR architecture consists of DPSSRAM and CSA to improve the operating speed. The pipeline architecture is more efficient than bit-serial approach and as a result, it is more accurate and provides high throughput. The goal of this algorithm in a filter is to provide maximum sample rate with optimum utilization of hardware resources. The proposed methodology optimizes critical path delay lead to significant improvement in operating speed. The simulation results are compared to the previous implementation. The synthesis report shows that the implementation of proposed DA FIR architecture utilizes less number of slices which replicate the effective area and also modification techniques leads to maximum frequency. The design implementation of DA FIR supports input sample frequency up to 136 MHz. Therefore, proposed DA FIR architecture has excellent performance on FPGA domain in terms of slices and operating frequency. Future work is to develop more input bits and coefficients of FIR filters architecture based on DA for area-delay-power efficient implementation on FPGA to meet the growing requirements of DSP applications.

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Voltage Cultivation from Fresh Leaves of Air Plant, Climbing Spinach, Mint, Spinach and Indian Pennywort for Practical Utilization

M. N. F. Rab, K. A. Khan, Salman Rahman Rasel, M. Hazrat Ali, Lovelu Hassan, M. Abu Salek, S. M. Zian Reza, and M. Ohiduzzaman

Abstract It has been designed and developed to study the voltage, current and power production from fresh leaves of five different vegetative as a comparative study. It has been collected fresh leaves from different vegetative and then it was embedded by two pairs electrodes Zn–Cu and Zn–Ag materials as positive and negative electrodes, respectively. The open-circuit voltage, short circuit current and maximum power have been measured by calibrated millimeters. It has been shown that it is possible to generate voltage, current and power from the fresh leaves of five different vegetative but PKL (Pathor Kuchi Leaf) is the best for electricity generation among them. It has not been done before yet this type of comparative study from five different fresh

M. N. F. Rab · K. A. Khan (✉)
Department of Physics, Jagannath University, Dhaka 1100, Bangladesh
e-mail: kakhan01@yahoo.com

M. N. F. Rab
e-mail: noorfazlerab@yahoo.com

S. R. Rasel
Local Government Engineering Department (LGED), Fulbaria, Mymensing, Bangladesh
e-mail: salman_rasel80@yahoo.com

M. Hazrat Ali
Department of Electrical and Electronics Engineering, European University of Bangladesh (EUB), Mirpur, Dhaka, Bangladesh
e-mail: ahazrat31@gmail.com

L. Hassan
Department of Physics, Jahangirnagar University, Savar, Dhaka, Bangladesh
e-mail: lovelu.iu.bd@gmail.com

M. Abu Salek
Department of Chemistry, Adamjee Cantonment College, Dhaka 1206, Bangladesh
e-mail: salek@acc.edu.bd

S. M. Zian Reza
Department of Physics, Uttara University, Dhaka, Bangladesh
e-mail: smzianreza@gmail.com

M. Ohiduzzaman
Department of Physics, Jashore University of Science and Technology, Jashore 7408, Bangladesh
e-mail: ohid@just.edu.bd

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leaves of vegetative. The studies had been conducted on PKL electrochemical cell using PKL extract. But in this research it has been used fresh leaves for electricity production. But no research has been conducted on rest of the fresh leaves of four types vegetative. Furthermore, it has also conducted a comparative study between the two pair electrodes Zn–Cu and Zn–Ag, respectively.

Keywords Zn–Cu and Zn–Ag electrodes · Air plant · Climbing spinach · Mint · Spinach · Electrochemical cell

1 Introduction

Electrical energy is a blessing to human beings. Our daily life is absolutely dependent on this energy. At present, there have many ways to produce electrical energy in the world [1–4]. But these conventional ways for producing electrical energy have many disadvantages such as limitation of sources, causes environment pollution, etc. For this reason, scientists are diverting their attention to non-conventional sources [5–7]. Renewable energy sources are non-conventional sources. In this study, we have found voltage from fresh leaves of different vegetative plants [8–10]. We have measured the voltage from leaves of Climbing Spinach, Air plant, Mint, Spinach and Indian Pennywort. We have observed that the voltage was stable until the leaves were fresh. When the leaves were getting dry, the voltage was dropping gradually. So we can come to a decision that fresh leaves of these vegetative plants may be a source of electrical energy. Before this study, the performances of electricity generation using the juice/sap of different vegetative and fruits have been studied [11–14]. The electricity generation from the living air plant has also been studied. But power generation from fresh air plant leaves was not studied yet. This work can play an important role in power generation in the near future.

2 Chemical Reactions

Electrode reaction can be represented as equations using different substrate in the following equations.

Acetate as substrate: Anode half-cell reaction:

$$CH_3COO^- + 4H_2O \rightarrow 2HCO^- + 9H^+ + 8e^- \quad (1)$$

Cathode half-cell reaction:

$$O_2 + 4H^+ + 4e^- \rightarrow 2H_2O \quad (2)$$

Total voltage generated from fresh leaves can be calculated from the Nernst potential of anode and cathode [15].

$$V_{\text{cell}} = V^{\text{o}}_{\text{cell}} - (RT/nF) \ln Q \tag{3}$$

where V_{cell} = cell potential (V), $V^{\text{o}}_{\text{cell}}$ = standard cell potential (V), R = universal gas constant (11 8.314 J mol^{-1} K^{-1}), T = Temperature (K), n = number of electrons involved in reaction, F = Faraday's constant = 96,500 C and Q = reaction quotient of the living PKL reaction.

Now, the Nernst potential of anode is described as:

$$V_{\text{anode}} = V^{\text{o}}_{\text{anode}} - (RT/nF) \ln\left(\left[\text{CH}_3\text{COO}^-\right]/[\text{HCO}_3]^2\left[\text{H}^+\right]^9\right) \tag{4}$$

where V_{anode} = anode Nernst potential (V), $V^{\text{o}}_{\text{anode}}$ = standard anode potential (V),

[CH COO^-] = acetate concentration (1 molL^-), [H_2O] = water concentration (1 molL^-), [H^+] = proton concentration (1 molL^-), [$HCO_3{}^-$] = bicarbonate concentration (1 molL^-). Hence, standard open cell potential of anode $V^{\text{o}}_{\text{cell}}$ is used which is typically −0.34 V versus standard copper electrode [16, 17]. Ideally, the reduction process in the cathode is, oxygen reduced in water Eq. (2), the Nernst potential can be determined as

$$V_{\text{anode}} = V^{\text{o}}_{\text{anode}} - (RT/nF)\left(\left[1/\text{pO}_2\left[\text{H}^+\right]^4\right)\right. \tag{5}$$

where V_{cathode} = cathode Nernst potential (V), $V^{\text{o}}{}_{\text{cathode}}$ = standard cathode potential (V), pO_2 = partial oxygen pressure (Pa), [H^+] = proton concentration (1 molL^-).

Ideally, we have the following equation:

$$V_{\text{cell}} = V_{\text{cathode}} - V_{\text{anode}} \tag{6}$$

It can be written as

$$V_{\text{cell}} = V_{\text{oc}} - R_{\text{in}} I, \tag{7}$$

where V_{oc} = open cell potential (V), R_{in} = internal resistance (Ω) and I = current density (A).

3 Methodology

Figures 1, 2, 3, 4 and 5 shows Air plants, Mint leaves, Spinach leaves, climbing spinach and Indian pennywort leaves, respectively collected from the agricultural

Fig. 1 Air plant

Fig. 2 Mint

field. The leaves are put between the two plates Zn and Cu firstly and then Zn and Ag as shown in Fig. 6. Using rubber and thread the plates are bound tightly [18]. Using calibrated multi-meter voltages are measured periodically. The collected data were tabulated shown in Tables 1 and 2, respectively, and then after it was graphically represented as shown in Figs. 7, 8, 9, 10, 11, 12, 13, 14 and 15.

Fig. 3 Spinach

Fig. 4 Climbing spinach

Fig. 5 Indian pennywort

Fig. 6 Experimental set up

4 Results and Discussion

4.1 The Variation of Voltage with the Variation of Time Duration of Different Fresh Leaves for Cu–Zn Pair Have Been Graphically Represented

It is shown (Fig. 7) that open-circuit voltage increases almost linearly with time up to 15 min. Then after it was almost the same up to 20 min. Then it increases again up to 25 min. Then after it decreases irregularly up to 65 min. It is shown that the obtained minimum voltage was 0.70 V and the maximum voltage is 0.76 V. Finally, it is 0.71 V after 65 min and then is almost stable. The maximum change in voltage variation for 65 min is 0.06 V and the minimum voltage variation is 0.01 V. Therefore, the % of voltage variation $(0.76 - 0.70)/0.70 \times 100\% = 8.57\%$.

It is seen (Fig. 8) that the voltage decreases about linearly up to 15 min. Then it increases linearly up to 20 min and approximately remains stable up to 65 min. The maximum voltage is 0.7 V and the minimum voltage is 0.4 V. Finally the approximate

Table 1 Table for comparative voltage study of different vegetative leaves using Cu–Zn pair

Date	Local time	Time duration (min)	Spinach	Air plant	Climbing spinach	Mint	Indian pennywort
04.05.19	12.20	0	0.701	0.681	0.604	0.774	0.429
	12.25	05	0.725	0.624	0.591	0.766	0.419
	12.30	10	0.740	0.572	0.588	0.765	0.465
	12.35	15	0.753	0.430	0.587	0.764	0.423
	12.40	20	0.753	0.593	0.552	0.764	0.404
	12.45	25	0.758	0.592	0.581	0.763	0.403
	12.50	30	0.736	0.610	0.576	0.765	0.425
	12.55	35	0.730	0.600	0.585	0.769	0.403
	01.00	40	0.729	0.604	0.584	0.773	0.413
	01.05	45	0.723	0.571	0.547	0.775	0.410
	01.10	50	0.718	0.578	0.565	0.774	0.422
	01.15	55	0.715	0.574	0.554	0.772	0.408
	01.20	60	0.712	0.604	0.550	0.771	0.404
	01.25	65	0.710	0.604	0.548	0.772	0.406

Table 2 Table for comparative voltage study of different vegetative leaves using Zn–Ag pair

Date	Local time	Time duration	Spinach	Air plant	Climbing spinach	Mint	Indian pennywort
04.05.19	2.25	0	0.591	0.540	0.588	0.555	0.00
	2.30	05	0.589	0.539	0.587	0.552	0.00
	2.35	10	0.586	0.537	0.583	0.553	0.00
	2.40	15	0.587	0.541	0.585	0.554	0.00
	2.45	20	0.588	0.538	0.582	0.550	0.00
	2.50	25	0.506	0.558	0.552	0.528	0.00
	2.55	30	0.518	0.547	0.550	0.531	0.00
	3.00	35	0.521	0.539	0.551	0.532	0.00

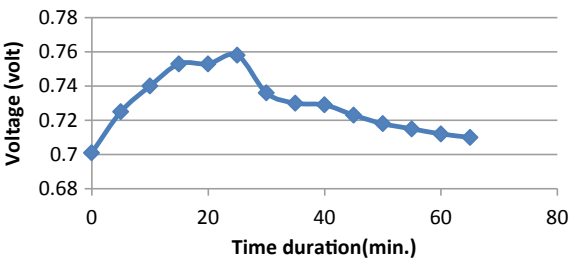

Fig. 7 Variation of voltage with the variation of time duration for Spinach

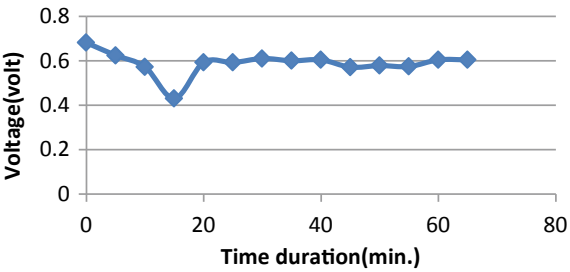

Fig. 8 Variation of voltage with the variation of time duration for air plant

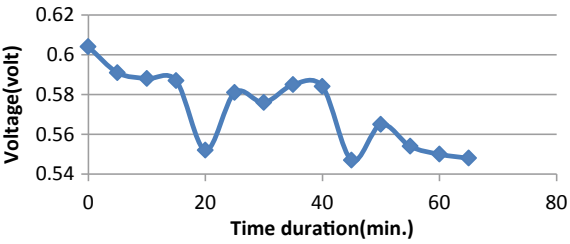

Fig. 9 Variation of voltage with the variation of time duration for climbing spinach

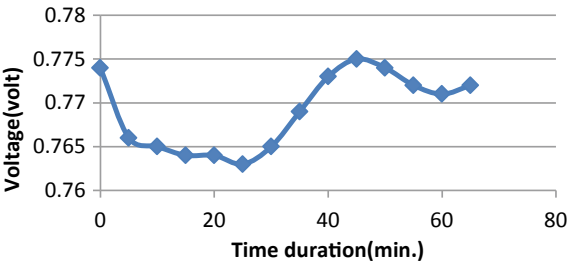

Fig. 10 Variation of voltage with the variation of time duration for mint

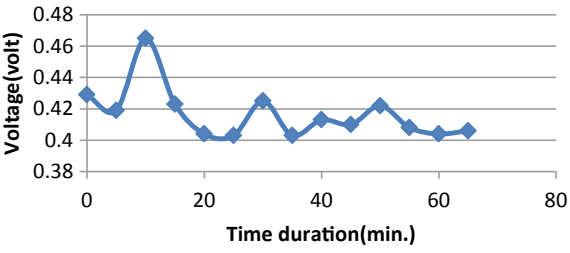

Fig. 11 Variation of voltage with the variation of time duration for Indian pennywort

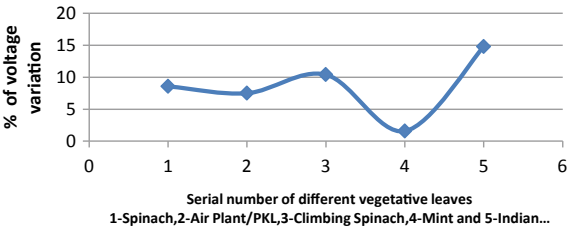

Fig. 12 Variation of % of voltage variation with the variation of the different vegetative leaves

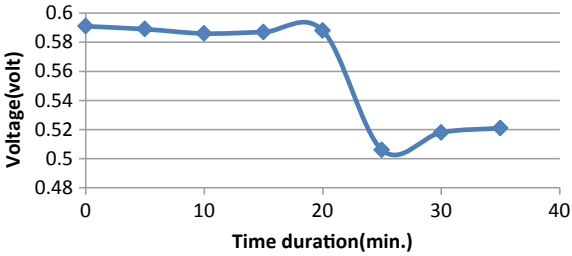

Fig. 13 Variation of voltage with the variation of time duration for spinach

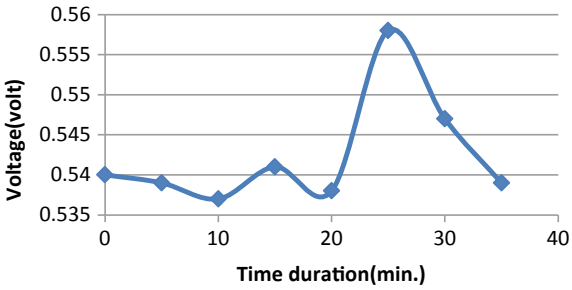

Fig. 14 Variation of voltage with the variation of time duration for air plant

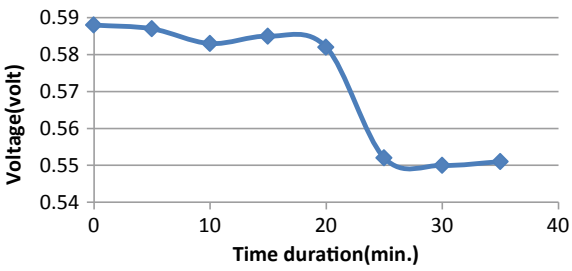

Fig. 15 Variation of voltage with the variation of time duration for climbing spinach

stable voltage was 0.6 V after 65 min. Therefore, the maximum voltage variation is 0.3 V and minimum variation is 0.1 V. The % voltage variation is $(0.7 - 0.4)/0.4 = 7.5\%$

It is seen (Fig. 9) that the voltage decreases about linearly up to 10 min. Then it remains stable up to 15 min then it decreases and increases irregularly up to 65 min. The maximum voltage is 0.605 V and the minimum voltage is 0.548 V. Therefore, the maximum voltage variation is 0.057 V. The % voltage variation is $(0.605 - 0.548)/0.548 = 10.40\%$.

It is seen (Fig. 10) that the voltage decreases up to 20 min exponentially and then it increases again up to 25 min almost linearly. Finally, it decreases up to 60 min. Then it increases again up to 65 min. The maximum voltage is 0.775 V and the minimum voltage is 0.763 V. Therefore, the maximum voltage variation is 0.012 V. The % voltage variation is $(0.775 - 0.763)/0.763 = 1.57\%$.

Table 3 Table for the % of voltage variation with different Zn/Cu fresh vegetative leaves electrochemical cells

Name of the different vegetative leaves	Serial no. of the different vegetative leaves	% of voltage variation
Spinach	1	8.57
Air Plant/PKL	2	7.5
Climbing spinach	3	10.40
Mint	4	1.57
Indian pennywort	5	14.81

It is seen (Fig. 11) that the voltage decreases about linearly up to 5 min. Then it increases linearly up to 10 min then it decreases and increases irregularly up to 65 min. The maximum voltage is 0.465 V and the minimum voltage is 0.405 V. Therefore, the maximum voltage variation is 0.065 V. The % voltage variation is $(0.465 - 0.405)/0.405 = 14.81\%$.

Table 3 shows the % of voltage variation with different Zn/Cu fresh vegetative leaves electrochemical cells. It is also shown that the maximum % of voltage variation is 14.81 for Indian Pennywort and the minimum % of voltage variation is 1.57 for Mint.

4.2 The Variation of Voltage with the Variation of Time Duration of Different Fresh Leaves for Zn–Ag Pair Has Been Graphically Represented

It is shown (Fig. 12) that the variation of % of voltage variation with the variation of the different vegetative leaves is not steady but always flexible. The maximum value was 14.81% and the minimum value was 1.57%.

It is seen (Fig. 13) that the voltage remains almost stable up to 20 min. Then it decreases up to 25 min. Then it increases about linearly up to 35 min. The maximum voltage is 0.590 V and the minimum voltage is 0.505 V. Therefore, the maximum voltage variation is 0.085 V. The % voltage variation is $(0.590 - 0.505)/0.505 = 16.83\%$.

It is seen (Fig. 14) that the voltage decreases about linearly up to 10 min. Then it increases and decreases irregularly up to 35 min. The maximum voltage is 0.558 V and the minimum voltage is 0.537 V. Therefore, the maximum voltage variation is 0.021 V. The % voltage variation is $(0.558 - 0.537)/0.537 = 3.91\%$.

It is seen (Fig. 15) that the voltage remains almost stable up to 20 min. Then it decreases up to 25 min. Then it remains almost stable up to 35 min. The maximum voltage is 0.588 V and the minimum voltage is 0.550 V. Therefore, the maximum voltage variation is 0.038 V. The % voltage variation is $(0.588 - 0.550)/0.550 = 6.90\%$.

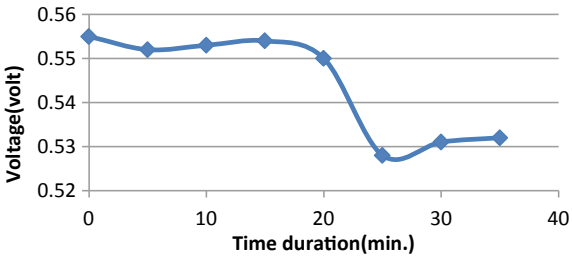

Fig. 16 Variation of voltage with the variation of time duration for mint

Table 4 Table for the % of voltage variation with different Zn/Ag fresh vegetative electrochemical cells

Name of the different vegetative	Serial number of the different vegetative	% of voltage variation
Spinach	1	16.83
Air plant/PKL	2	3.91
Climbing spinach	3	6.90
Mint	4	5.11

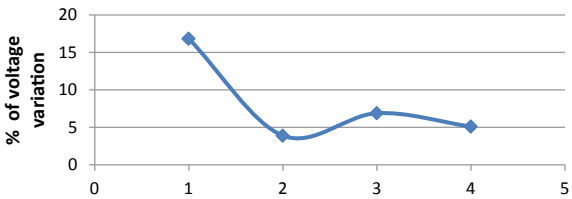

Fig. 17 Variation of % of voltage variation with the variation of different vegetative leaves

It is seen (Fig. 16) that the voltage decreases linearly up to 5 min. Then it increases up to 15 min. Then it decreases linearly up to 25 min and again increases about linearly. The maximum voltage is 0.56 V and the minimum voltage is 0.528 V. Therefore, the maximum voltage variation is 0.027 V. The % voltage variation is $(0.56 - 0.53)/0.59 = 5.11\%$.

Table 4 shows the % of voltage variation with different Zn/Ag fresh vegetative electrochemical cells. It is also shown that the maximum % of voltage variation is 16.83 for Indian Pennywort and the minimum % of voltage variation is 3.91 for Mint.

From Fig. 17, it is shown that the variation of % of voltage variation with the variation of the Different Vegetative is not steady but almost it is always flexible.

5 Conclusions

The fresh leaves are available in our country due to the development of agricultural research. Anybody can harness this electricity as a homemade product. Anyone can cultivate these vegetative leaves in the garden to get homemade electricity instead of

kerosene. This electricity can be used to power LED bulb. This is useful for remote areas of any country. This electricity is environmentally friendly and low-priced.

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Design of Green Energy Based Charge Controller for Domestic Uses

Sankha Subhra Mondal and Writuparna Banerjee

Abstract India is known for scarcity of energy where the gap between demand and supply is found to be almost 12% of the total demand of energy. As India is largely dependent on coal and other non-renewable resources, therefore this trend is quite notable. In India, only 7.7% of the total installed power capacity of 167,077 MW is provided by Renewable energy (RE) sources. The main component among the RE sources is the energy from the wind while the contribution of solar power currently is less than 0.1% (on-grid + off-grid) of the total installed capacity. The amount of solar power that was available at a specified place and time in India can be seen using the map data [1]. In this project, a green energy based charge controller is designed which is functional, reliable and economical as it is designed using compact and affordable components.

Keywords Solar photovoltaic cell (SPV) · Solar charge controller circuit · Load and lead-acid battery

1 Introduction

The generation of electricity from renewable resources is becoming essential due to the detrimental impact of electricity generation from fossil fuels. Solar power is easily available and therefore convenient for generation of electricity. Solar PV systems are cleaner, relatively noiseless, can be easily installed and integrated when compared to others [2]. These are the major advantages of PV. The sun shines in India about 6 h approximately. Moreover, out of 12 months, the sun shines in India for about 9 months. The solar photovoltaic modules (SPV) can be used for the generation of electricity from the sun. The SPV [3] is available in various output power to encounter

S. S. Mondal (✉) · W. Banerjee
Department of Electrical and Electronics Engineering, Swami Vivekananda Institute of Science and Technology, Dakshin Gobindapur, Kolkata, West Bengal, India
e-mail: sankhasubhramondal18@gmail.com

W. Banerjee
e-mail: writuparnabanerjee@gmail.com

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the load. However, the solar irradiation and the panel temperature determine the output power of a PV panel. To regulate the terminal voltage of the PV system at ideal values in various conditions of solar radiation DC/DC converter with a voltage feedback signal is generally used. To get a constant output voltage of 24–24.20 V within an input voltage range of 6–30 V, a buck-boost converter [4] is used to step down or step up a fluctuating input voltage. A feedback loop is used to generate a constant output voltage.

2 Charge Controller

A charge controller is an important part of power systems that act as a battery charger, where the power source can be hydro, PV, wind, fuel, or utility grid. Its objective is to properly feed the batteries and keep it safe for a long time. The working principle of a controller is quite simple. Charge controllers [5] block the flow of current in the reverse direction and prevent overcharging of battery [6].

Some controllers also prevent over discharge of battery, protect from electrical overload and display the status of battery and the power flow. In most controllers to control the unidirectional flow of current, transistors (semiconductor) are used which act as a valve to the flow of current. In some controllers, an electromagnetic coil called relay is used for opening and closing a mechanical switch. At night, the relay switches off to block the reverse current (Fig. 1).

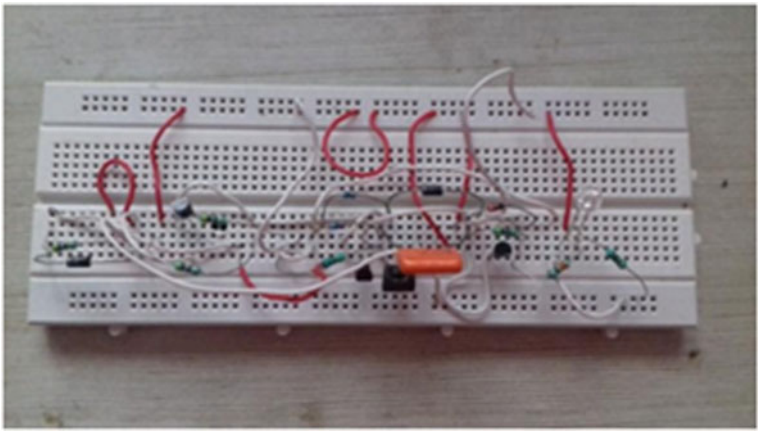

Fig. 1 Circuit representation on breadboard

3 Solar Cell

A solar cell system converts solar energy into electrical energy. The solar cell constitutes the building block of a solar panel [7]. Panels or modules are formed by grouping various cells. A solar cell is primarily a *p-n* junction. This is formed by doping two different layers of silicon with a small quantity of impurity atoms. A DC current is generated on exposing it to light. The generated current vs the solar irradiance follows a linear characteristic. The equivalent circuit diagram of an ideal solar cell is assumed to be a current source in parallel with a diode as shown in Fig. 2.

Junction current can be obtained from the below equation [8],

$$I_{\mathrm{D}} = I_{\mathrm{O}}\left[\exp^{(q(V+\mathrm{IR}s)/KT)} - 1\right] \tag{1}$$

where the solar cell output current:

$$I = I_{\mathrm{L}} - I_{\mathrm{D}} - I_{\mathrm{sh}} \tag{2}$$

$$I = I_{\mathrm{L}} - I_{\mathrm{O}}\left[\exp^{(q\,(V+\mathrm{IR}s)/KT)} - 1\right] - [(V + \mathrm{IR}_S)/R_{\mathrm{sh}}] \tag{3}$$

where

I = Solar cell current (A)
I_{L} = Light generated current (A) [Short circuit value assuming no series/shunt resistance]
I_{O} = The current at which the diode saturates (A)
Q = The charge of an electron (1.6×10^{-19} C)
K = Boltzmann constant (1.38×10^{-23} J/K)
T = Temperature of the cell in Kelvin (K)
V = Output voltage of the solar cell (V)
R_{S} = The series resistance of solar cell (Ω)
R_{Sh} = The shunt resistance of solar cell (Ω)

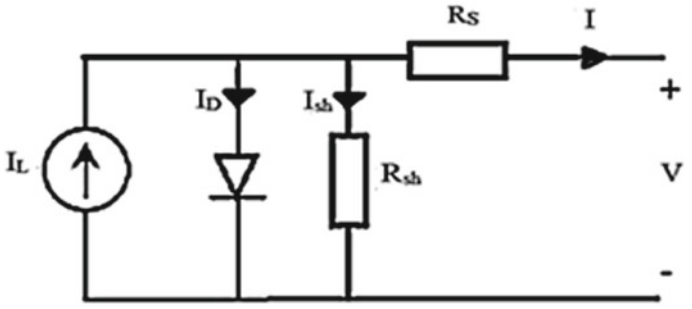

Fig. 2 Equivalent circuit diagram of a solar cell

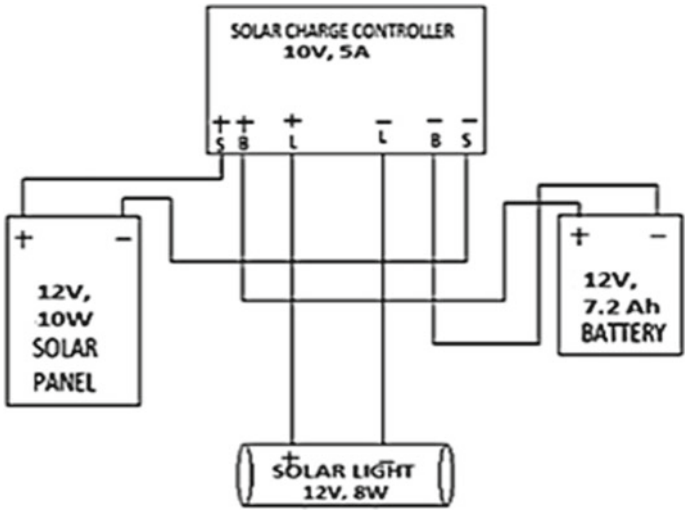

Fig. 3 Block diagram of the circuit

4 Block Diagram

Figure 3, shows the block diagram of the project. There are mainly four blocks such as solar panel, solar charge controller, a battery and a load. At day time solar panel works as a source and provides electricity to the load and the battery gets charged. At night, panel voltage is nearly zero, and battery discharges to keep the load current constant. By this process, it works efficiently.

5 Circuit Diagram

5.1 Solar Photovoltaic Effect

P-type and *n*-type semiconductors are used in making a photovoltaic cell. When two crystals are pushed together the electrons start diffusing from the *n*-side to the *p*-side where they recombine with the free holes. A net positive charge is left in the *n*-side and a net negative charge is left in the *p*-side due to the diffusion of free electrons and holes, respectively. An electric field and hence a potential barrier is created due to the charge separation. The potential difference thus formed stops any further diffusion of charge carriers. The potential at the contact causes the energy levels of *p*-side to be displaced upward and that of *n*-side to be displaced downward.

When solar electromagnetic radiation (photons) of energy greater than the bandgap energy E_g strikes the *p*-*n* junction, electrons in the valence band get excited

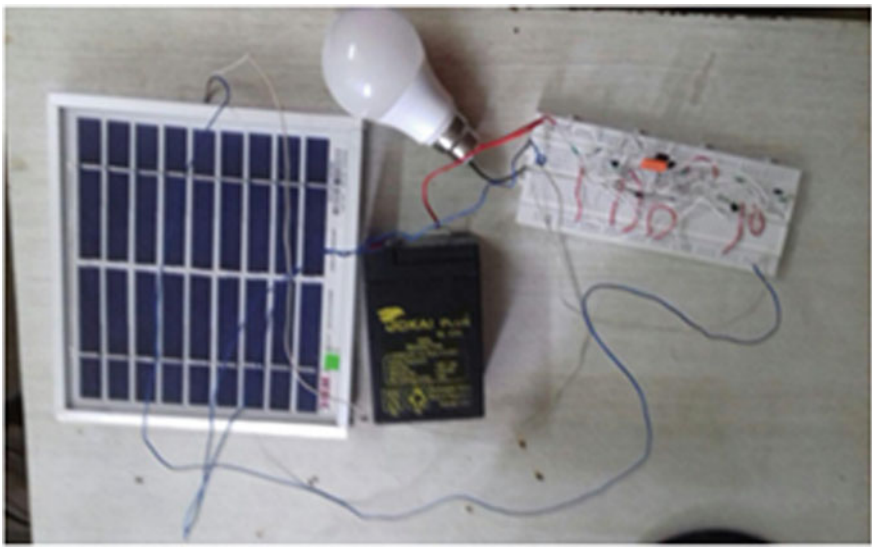

Fig. 4 Circuit diagram

and jump to the conduction band. As a result, electron-hole pairs are produced. The junction separates the pair by making the electrons cross the potential barrier and move to the n-side and the holes to the *p*-side. Thus, the potential difference across the junction gets reduced and a new equilibrium is reached. This potential difference across the junction is called the open-circuit voltage. Now if an external load is connected across the junction, the electrons are forced to cross the potential barrier and move through the external circuit. Thus, the current is delivered to the load. However, as the potential difference across the junction is now reduced, some of the charge carriers manage to cross the junction in the wrong direction. Thus, there is a leakage current at the junction and hence a reduction in load current delivered to the load.

6 Flow Chart of Voltage Stabilization Across the Load Using a Solar Charge Controller

Figure 5, depicts the flow chart of voltage stabilization across the load using a solar charge controller. As discussed earlier the main purpose of the solar charge controller is to maintain a constant voltage across the load even if the panel voltage fluctuates. When the solar irradiance from the sun strikes the panel then a voltage develops across the panel. This voltage fluctuates with the change in the intensity of sunlight at different instants. A fluctuating voltage may be dangerous for the load connected in the circuit. If the panel voltage is not stable then the solar charge controller is

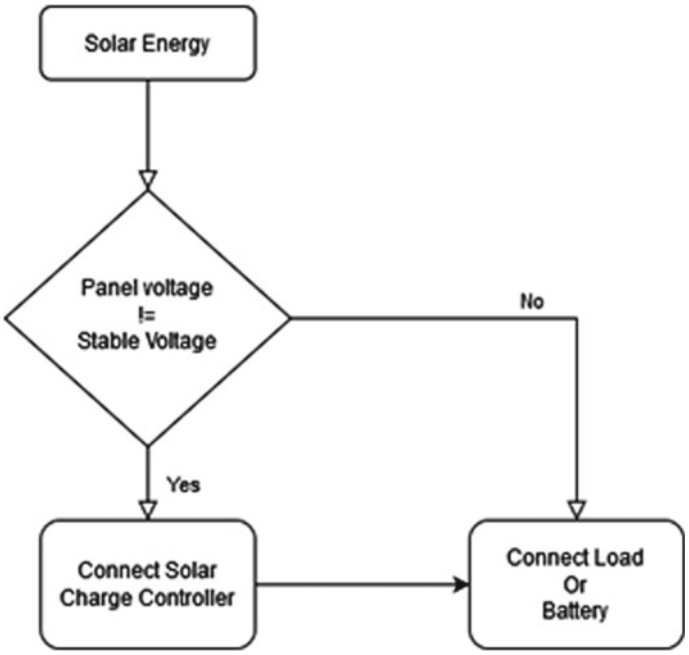

Fig. 5 Flow-chart of the operation

connected in the circuit to get a stable voltage across the load. If the voltage across the panel is stable then a load or battery is connected in the circuit to get a proper stable voltage across the output (load).

7 Result

7.1 During Day Time

The rating of solar panel is 12 V, 10 W as mentioned in the component specification of solar panel in Table 1. Here the voltage of panel under sunlight was found in the range of 11.58–11.87 V which is within 12 V rated voltage. At this voltage the battery charges. Without a proper charge controller, the load voltage fluctuates with the change in panel voltage. These fluctuating voltages can hamper the battery and load. But, in a proper functional and reliable charge controller, the load voltage remains constant even when the panel voltage fluctuates.

Hence the battery and load voltage can be controlled so that they are not hampered. It also can control the reverse current and the overcharging of the battery. So the solar

Table 1 Component specification

Name of the components	Quantity	Specifications
Led lamp	1	12 V, 8 W DC LED bulb
Solar panel	1	1. Photovoltaic cell: 10 W, 12 V. Nominal peak power: 10 W. Open-circuit voltage (V_{oc}): 12 V. Short circuit current (I_{sc}): 0.40 A voltage at Max. Power (V mp): 10.50 V. Current at Max. Power (Imp): 0.36 A irradiance: 100.0. Cell efficiency (%): 16.7 module efficiency (%): 10.9. Type: MULTI
Battery	1	12 V, 7.2 Ah, cycle use: 14.40–15.00 V, standby use: 13.50–13.80 V, maximum charging current: 1.50 A

charge controller circuit can be used for controlling all the voltages to protect the devices.

7.2 During Night Time

Here we are considering the voltage of panel at night is 0.1–0.2 V but not completely 0 V due to the street lights. At this voltage battery discharges to load. But here also for uncontrollable charge controller, the voltage across the load cannot be controlled. So the load can be hampered or may not work properly. But, in controllable charge controller, the voltage across the load can be controlled well and the load can work properly.

8 Result Analysis

Graphical analysis of the result which is mentioned in Table 2 has been shown. All the below graphs are the subset of the whole graphical analysis of the experiment.

Table 2 Test result

S. No.	Solar panel voltage (V)	Battery voltage (V)	Load voltage (V)	Load current (A)
1	11.39	11.87	11.87	0.673
2	10.54	11.89	11.89	0.6728
3	9.43	11.87	11.87	0.673
4	11.98	11.86	11.86	0.6722
5	11.90	11.87	11.87	0.6734
6	11.72	11.91	11.91	0.6717

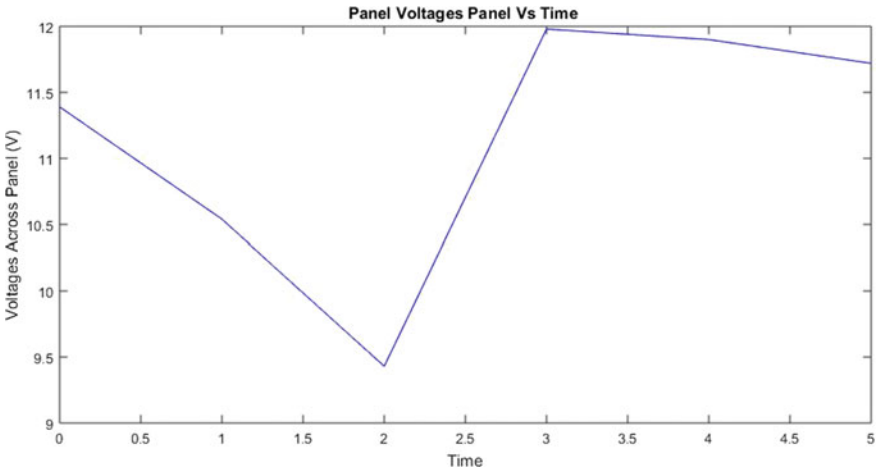

Fig. 6 Change in solar panel voltage

From the experimental table, we have got the values of voltages that appeared across the solar panel during the experimental time. The voltage was recorded at six different instants starting from the time instant 0 to 5. After plotting those values Fig. 6 was visualized. So the voltage across the panel is fluctuating in nature, which is not an ideal condition for charging the battery.

Load Voltage and voltage across the battery is the same as they are connected in parallel. Again, the voltage across the battery is the voltage across the charge controller as they are also connected in parallel. Figure 7 is the visualization of controller voltage with respect to time.

Figure 8 is the comparison of the above two cases (Figs. 5 and 6). Fluctuating voltage of the solar panel is stabilized after passing through the charge controller and it's providing a stale voltage which is an essential condition for battery charging. Hence, the controller is working properly.

Figure 9 is the load characteristics graph of the charge controller.

9 Cost Analysis

Solar power is much more economical when compared to conventional power supply. Solar energy is one of the non-conventional sources of energy, and it is more eco-friendly [6] than any other sources of energy out there now. For a system to be available for domestic use, it has to be cheap, compact and easily maintainable. The cost calculation of the solar photovoltaic system that has been installed in India has been calculated considering the life-time of the system as 15 years. In this project, a solar light of 8 W has been taken which is operated for 8 h a day from 4 PM to 12 AM.

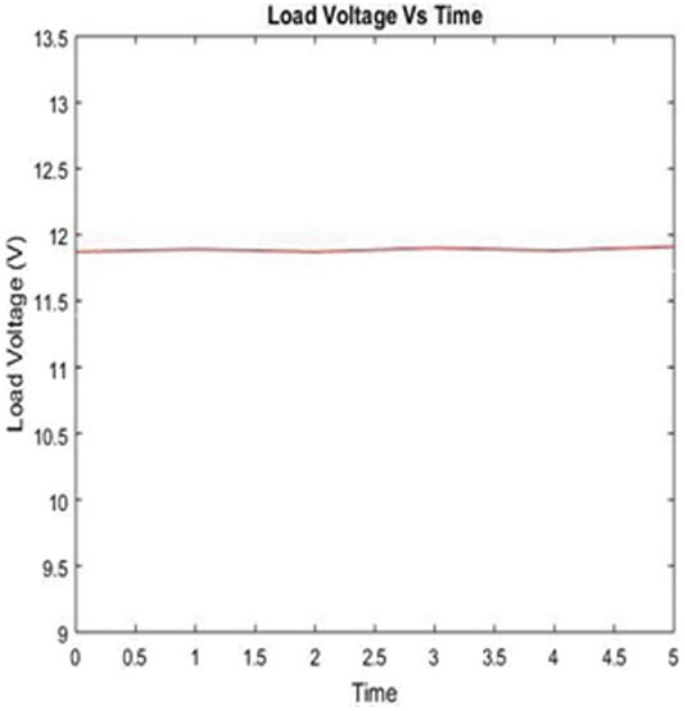

Fig. 7 Change in load voltage

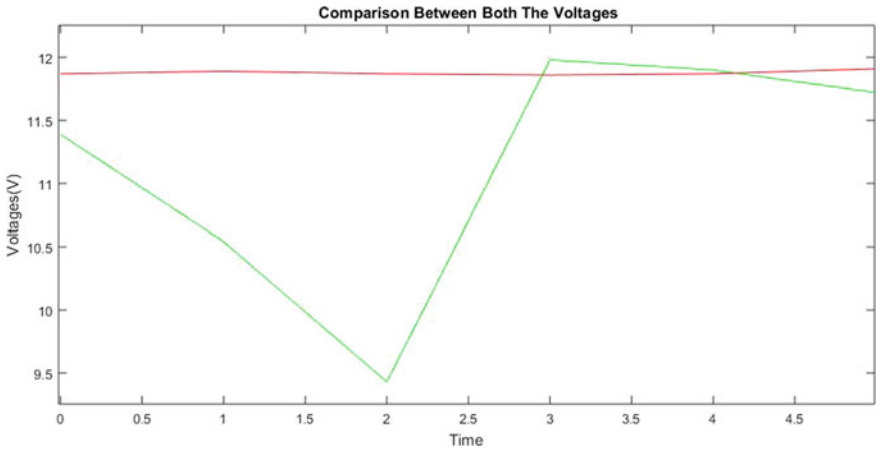

Fig. 8 Comparison between both the voltages

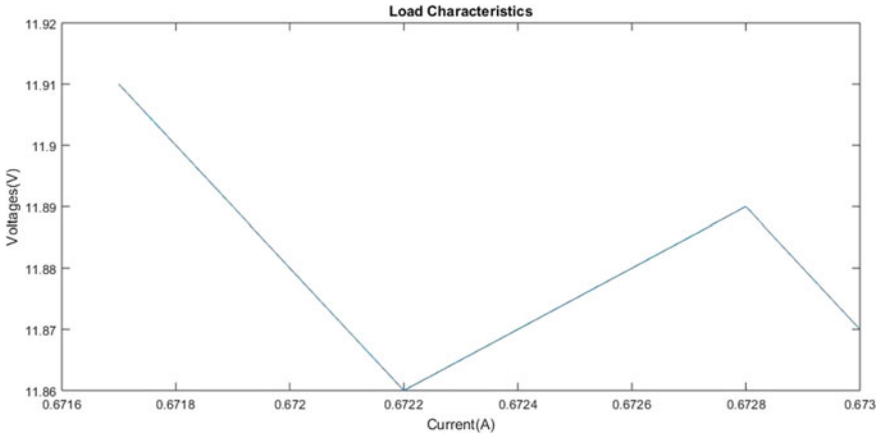

Fig. 9 Load characteristics

9.1 Conventional Power Supply

The amount of energy consumed by the solar light is 0.008 kW*h. Since we are testing our project in Kolkata, West Bengal under CESC, we have taken the tariff as Rs. 12/unit or kW*h as an aggregate to our load specification [9]. So, the amount to be paid for a 0.008 kW load to operate for 1 h per day is (0.008 × 12) = Rs. 0.096 kW*h. If the load operates for 8 h then the cost will be (Rs. 0.096 * 8) = Rs. 0.768 (Table 3).

However, for Non-Conventional Power Supply (Solar), the major cost for the consumers is the initial investment of this project.

Solar PV Panel = Rs. 300/,
Battery = Rs. 800/,
Charge controller = Rs. 450/.
Miscellaneous Cost = Rs. 100\
So, Initial investment is Rs. (300 + 800 + 450 + 100) = Rs. 1650.

The solar panel sold in India comes with a manufacturing warranty for a minimum of 15 years. The battery comes with a warranty of 4 years. By going through personal observation and market research, it can be concluded that a battery generally needs to be replaced about every 6 years. In a span of 15 years, the battery needs to be replaced about 2 times. So initially a consumer may find it hard to pay that much amount of money but in the long run, it is the cheaper and the best option. The total maintenance cost in a span of 15 years is (Rs. 800 × 2) + (Rs. 450 × 2)/- = Rs. 2500/-.

Now, according to cost data visualization (Fig. 10), The blue bars of the graph indicate the initial and maintenance cost of solar power supply. The green bars indicate the cost of energy generated by the Solar supply in terms of the tariff rate of

Table 3 Cost of energy consumption of LED bulb

Time period	Cost (avg. of Rs. 12/kW*h)
1 day	0.768
1 year or 365 days	280.32
2 years	560.64
3 years	840.96
4 years	1121.28
5 years	1401.60
6 years	1681.92
7 years	1962.24
8 years	2242.56
9 years	2522.88
10 years	2803.20
11 years	3083.52
12 years	3363.84
13 years	3644.16
14 years	3924.48
15 years	4204.80

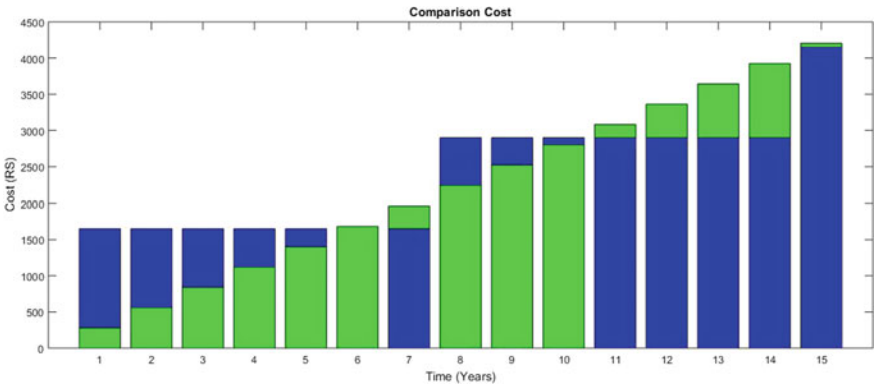

Fig. 10 Cost analysis with the help of data visualization

Conventional Power supply. Each and every year the green bar is increasing but the maintenance of the solar power system is required after a minimum of 6 years.

Hence, the growth of the blue bars are comparatively slower than the green bars.

Initial cost and maintenance cost within a span of 6 years has been calculated and from the graph (Fig. 11), it can be concluded that solar power will be more economical as compared to Domestic Power supply. On implementing the solar panel on a larger scale, the net profit will increase. Estimated economic benefits should encourage consumers to switch to solar power.

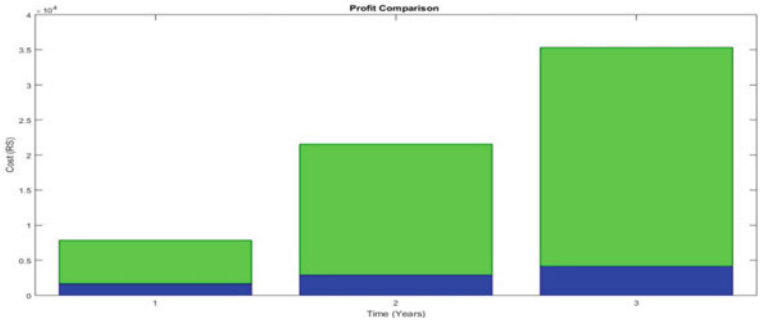

Fig. 11 Profit analysis with the help of data visualization

10 Conclusion

Our project's focus is to use the solar photovoltaic (SPV) technology to meet the demand of the domestic, household and small scale industries for operating small loads. In this project, a working model has been designed which can be implemented on a larger scale. The hardware is also being made, which has been tested under particular conditions.

The project on which the experiment has been conducted is very much viable for the operation of 1 kW loads to be used for operating a small load or LED bulb.

Acknowledgements This document is prepared on the basis of utilization of renewable energy sources in a cost-effective manner.

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Resonant Tunneling Diodes: Working and Applications

Revathi Bhukya, Gorla Hampika, and Manisha Guduri

Abstract This paper will cover the basic working of tunnel diode, its V-I characteristics curve, principal function of RTD, the Double Barrier Quantum well (DBQW) structure, and applications. This will enable the reader to get a fair idea about what tunnel diodes exactly are and understand the importance and scope of their applications.

Keywords Tunneling · Negative resistance · Quantum well · Double barrier

1 Introduction

A **diode** is a two-terminal device that allows flow of current mainly in one direction. Hence, it can be used as a switch. The most common type of diode is the P-N junction diode, which is a crystal of semiconductor connected to two electrical terminals, a P-N junction [1–5].[1] "Cat's whisker diodes" was the name given to the first semiconductor diodes and they were made using crystals like galena.[2]

There are many other types of diodes that are used today, and one of them is tunnel diode.

It is created by changing the doping concentration from 1 part in 108 (that of a normal P-N junction diode) to 1 part in 103. This changes the width of the depletion layer from 5 microns to less than 100Å. This thickness is very small compared to the wavelength of visible light. For such potential energy barriers which are very thin, the electrons do not surmount the junction, but rather penetrate through it. This quantum mechanical response is called tunneling [6].

The resonant tunneling diode (RTD) has gained a lot of interest as a result of the pioneering work done by Esaki and Tsu who laid the ground for its far-ranging

[1] https://www.sciencedirect.com/topics/physics-and-astronomy/quantum-wells.

[2] https://circuitglobe.com/tunnel-diode.html.

R. Bhukya · G. Hampika (✉) · M. Guduri
Department of Electronics and Communication Engineering, Institute of Aeronautical Engineering, Hyderabad, Telangana 500043, India
e-mail: hampika.g@iare.ac.in

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applications in very high-speed circuits and devices. It has been extensively studied due to its significance in the field of nanoelectronics.

It is a semiconductor device whose conduction depends on quantum mechanical effects. The principle effects are tunneling of electrons through thin barrier materials and quantization of electrons in the quantum well [7].

2 Tunnel Diode

In a tunnel diode, the doping concentration is high in both p and n regions due to which the fermi level on *p*-side goes below the valence band and fermi level on *n*-side goes above the conduction band which results in small width of depletion region (100Å).

When forward bias is increased, the difference between fermi levels decreases and width of depletion region decreases as well. This results in a phenomenon in which carriers punch through and forward tunneling current increases (Fig. 1b).

Maximum electrons tunnel from filled states which are present in *n*-type to empty states in *p*-type (Fig. 1c) which leads to peak current (point A in Fig. 2).

After attaining maximum current, if forward bias is increased, tunneling current decreases.

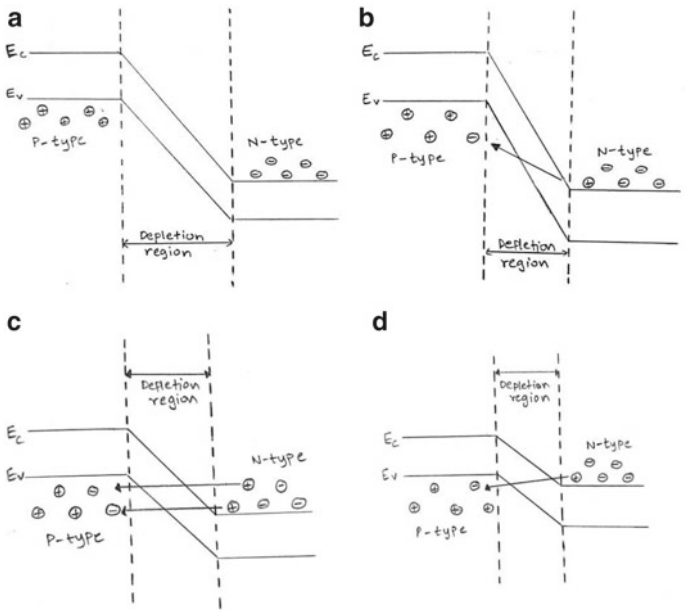

Fig. 1 Energy band diagram of RTD **a** Zero biased condition. **b** Small forward voltage condition. **c** Moderate forward voltage condition. **d** High forward voltage condition

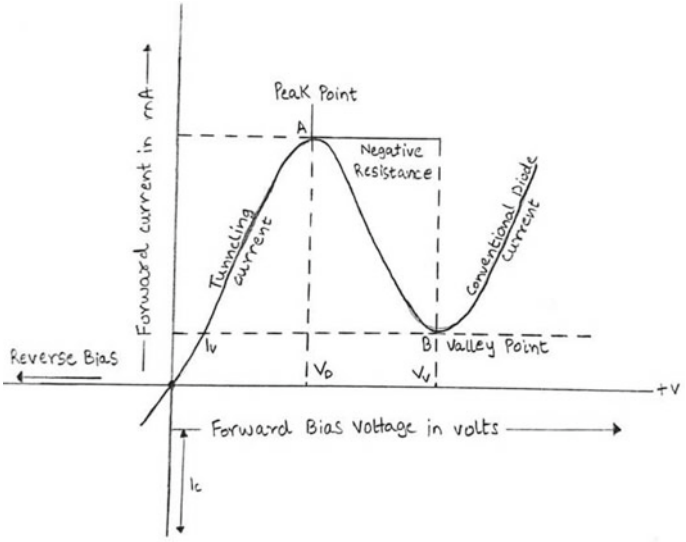

Fig. 2 Characteristics of tunnel diode

Since there are now no filled states in *n*-type at the same energy level as empty states in *p*-type, the tunneling current drops to valley point (point *B* in Fig. 2) as electrons cannot tunnel through the barrier.

After this, on increasing forward bias the applied potential will overcome the barrier potential and current will flow through the tunnel diode like it does in a normal diode and will show similar I-V characteristics [8].

3 Functionality of RTD

The RTD is a semiconductor device in which the quantum mechanical effects determine the conduction. The principal effects involved are:

- Tunneling of electrons through thin barrier materials.
- The quantization of electron energies in a quantum well structure.

Before we go any further, it is essential for us to first understand quantum wells. Quantum wells [9] are essentially heterostructures in which one semiconductor layer is positioned between two layers of different semiconductor material. The materials should be chosen carefully so that an energy dip (or well) is created, which confines the electron in the middle layer. This happens when the energy of the electron which is available for conduction in the middle layer is lower than those in the outer layers. Hence, materials that allow this must be considered.

The basic structure of RTD [10] consists of potential barrier structures and a quantum well of finite thickness and height. The AlxGa1-xAs/GaAs RTD is made of a double barrier heterostructure which contains a quantum well (made of GaAs) and two potential barrier structures (made of AlGaAs).

The twin barrier structure is interfaced between two binding regions for GaAs which operate as sources of electrons.

When a voltage is applied to the RTD, the current flows between the two outside electrodes and resonant tunneling occurs when the energy of the incoming electrons matches the energy levels produced in the well. This resonant amplification of the conductivity is a very fast process that results in a differential negative resistance in the characteristics of the current-voltage.

In the effective mass approximation, the standard equation for current is given by:

$$J = \frac{em \times kT}{2\pi^2\hbar^3} \int_0^\infty dET(E, V).\ln\left[\frac{1 + e^{\frac{Ep-E}{kT}}}{1 + e^{\frac{E_r - E - eV}{kT}}}\right]$$

$$T(E, V) = \frac{\left(\frac{\Gamma}{2}\right)^2}{\left[E - \left(E_r - \frac{eV}{2}\right)\right]^2 + \left(\frac{\Gamma}{2}\right)^2}$$

where,

E Energy observed from the emitter conduction band edge
E_r Resonant level energy with respect to the centre of bottom of the well
Γ Resonance width.

4 Double Barrier Quantum Well (DBQW) Structure

DBQW is the basic RTD device configuration (of nanometre range).

- Region IV is a quantum well with small bandgap semiconductor. (e.g., GaAs)
- Regions III and V represent quantum barriers with large bandgap semiconductor. (e.g., AlGaAs)
- I, II, VI, and VII regions are contacts which are heavily doped and made from small bandgap semiconductors.

The Double Barrier Quantum Well Structure shown in Fig. 3 [1] is concerned with electron energy versus length under bias. This is important as we want to study the mechanism of electron transport which includes its behavior under the influence of bias voltages under a certain energy band structure.

Here, it is observed that electron wavelength is comparable to the DBQW's characteristic dimensions. Hence, the electron's wave nature results in quantum phenomena like tunneling, interference, energy quantization, etc. Consequently, we

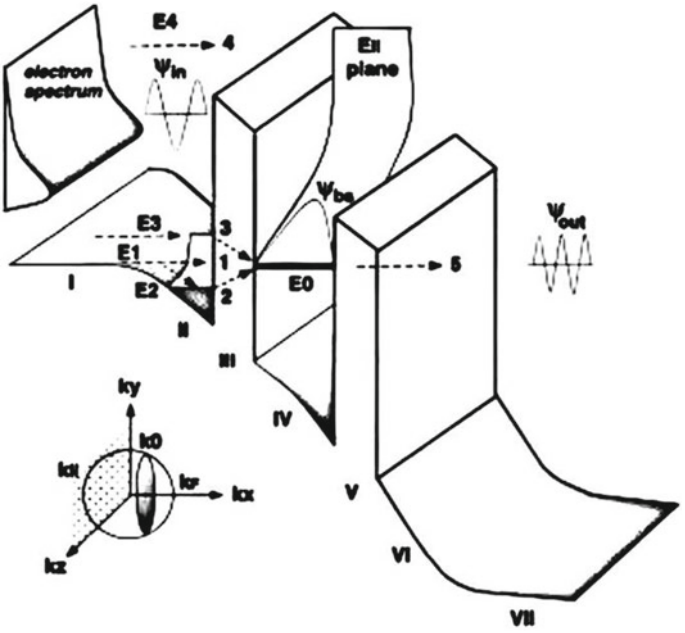

Fig. 3 Double barrier quantum well structure

detect resonant tunneling in DBQW structure which forms the basis for the working of RTD.

5 Applications

Research on RTDs has been going on for almost 20 years, the main reason being their compatibility with many traditional technologies such as metal oxide field-effect transistors (MOSFETs) and high electron mobility transistors (HEMTs) [11]. The low-power, high-speed advantages can now be enforced with digital circuit applications.

RTDs are used in a circuit which is named MOBILE (monostable-bistable transistor logic element). A MOBILE RTD is applicable where a large sampling rate is necessary such as high-resolution imaging and communication systems. A regular CMOS flip flop cannot meet the ultra-high speeds of RTD devices.

It has also been observed that using Schottky collector RTDs a 650 GHz oscillator has been achieved. RTD also finds applications in many other devices like frequency dividers and analog-to-digital converters.

6 Conclusion

To support future ultrahigh-speed applications conventional transistor technology will not be enough. Resonant tunneling diode is a possible solution to this problem. These high-speed, low-power, and small devices are very significant as we continue to move down to the atomic scale where major problems include parasitic effects and heat. But, in order to reach its maximum functionality, better and advanced manufacturing methods are required for RTDs [12].

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Gray World Based Fuzzy C-Means Satellite Image Segmentation

Nitin Sharma, Rajni Sharma, and Kanchan Sharma

Abstract Satellite image segmentation is used to partition an image into subregions and recognize the multiple objects of the same class as a single entity. This paper proposes a novel gray world based Fuzzy C-Means (GBFCM) a clustering-based satellite image segmentation technique. To achieve the objective of an increase in the spatial information, contrast, local detail present in the satellite image and to reduce the computation time, the gamma correction method is introduced in the proposed approach. The most basic attribute of the image cluster is its reduction of intensity from a cluster centre which improves by modification of gamma values. To measure the effectiveness of the proposed cluster-based segmentation approach, Signal-to-Noise Ratio (SNR), Mean Square Error (MSE), Mean Absolute Error (MAE), Peak Signal-to-Noise Ratio (PSNR) is considered and compared with the recent schemes. The results confirm that the proposed approach efficiently enhanced the resolution of the satellite image in comparison to the state-of-the-art resolution algorithms namely OTSU, Thresholding, K-means, and is found to outperform in all the methods.

Keywords Gray world · Fuzzy C-means · K-means · Segmentation · Resolution · Satellite images

1 Introduction

Satellite images consist of multispectral information and are being used in number of areas like climate-related studies, agriculture, landscape, geology, fishery, etc. [1].

N. Sharma (✉)
Department of ECE, Maharaja Agrasen Institute of Technology (GGSIPU), Delhi, India
e-mail: nitinsharma@mait.ac.in

R. Sharma
School of Computing, Galgotia University, Greater Noida, India
e-mail: rajnisharma.hp@gmail.com

K. Sharma
Department of ECE, Indira Gandhi Delhi Technical University for Women, Delhi, India
e-mail: sharma_kanchan@yahoo.com

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Satellite image enhancement is of profound interest in the current scenario due to which researchers are continuously working to improve the quality of the captured image. These images are captured from high altitude in space which usually involves conditions beyond human control. Moreover, these images are poorly illuminated and have a very low spatial resolution. Due to this, too many objects (or regions) remain unrecognized. These regions, therefore, are required to be enhanced in such a way that it retains the spatial information and the appropriate greyness. To provide a definite class in the desired region with certainty for a satellite image is always a typical task. This task is achieved by using Fuzzy based method that handles the problem by associating certainty factors with class labels.

Generally, the homogeneous region present in the satellite images contains valuable information required to detect the texture and pattern of different shades present in the low-resolution satellite images. These objects are determined on the basis of gray shades by using the clustering approach [2–4]. The main challenge behind the satellite images is to extract the actual information present in the captured image by the camera. Therefore, the clustering approach is able to distinguish various regions captured in the low-resolution satellite image used for further analysis. The clustering approach segments the image according to the pixel gray value similarity. The main goal of using satellite image segmentation is to classify pixels into homogeneous regions based on specific characteristics of the image. The homogeneous groups are performed in two ways, either by a supervised approach to learning or by unsupervised approach to learning. Supervised learning approach considers the standard data set which is used to train the system and thereafter the learned system is tested, hence the clustering using this method is referred to as supervised clustering [5, 6]. In the other method, data set is not used to train the system, hence this clustering approach is called unsupervised clustering [7, 8]. The unsupervised clustering is more popular than supervised clustering. The algorithms like k-mean, Fuzzy C-Means (FCM) are examples of an unsupervised algorithm [9, 10]. K-means clustering procedure has a simple and easy way to classify a given dataset into a number of apriori-fixed clusters (assuming k clusters). FCM clustering allows two or more clusters to belong to one piece of data [11]. The FCM-based clustering method; a popular choice for segmentation has been investigated in the works of [12, 13]. The purpose of segmentation in the proposed approach is to enhance the low-resolution image by using a spatial domain technique [15–19].

The proposed approach GBFCM is different from the existing clustering segmentation algorithms. GBFCM makes cluster formation so that pixels belonging to the same cluster are more correlated than pixels belonging to other clusters. The proposed technique involves the gamma correction method which enables fast computation and gets better detail in the satellite image. The paper is organized as follows. In Sect. 2, we present the basic concepts of the clustering approach for image analysis. The general context that justifies the FCM method and modifies the FCM-based approach in satellite image segmentation is explained in Sect. 3. The performance metric used is discussed in Sect. 4. Simulation results obtained in reference to the application of proposed GBFCM to satellite images are given in Sect. 5. Finally, Sect. 6 concludes the paper.

2 K-Means Clustering

Data vectors are placed in a fixed number of clusters in K-Means algorithms. Initially, the fixed cluster centroids are randomly allocated. The centroid size is the same as the data vector size or length. The cluster assignment to each pixel is carried out on the basis of nearness or closeness given by the computation of Euclidean distance measurement. When all the pixels are mapped or get assigned cluster, the re-computation of the mean of each cluster is carried out. This process is repeated until no significant changes are observed for each cluster mean or for some fixed number of iterations [7].

This clustering technique was identified as one of the most efficient image segmentation methods. A number of hybrid algorithms using K-means with other optimization techniques have been presented in the literature which improves the segmentation of the image to a much-optimized scale.

Algorithm 1 K-Means Algorithm

1. Randomly initialize the K cluster centres.
2. Compute the Euclidean distance for each pixel and pixel map to a cluster with the minimum distance to its cluster centre.
3. Obtain the mean pixel values in each cluster and formed new cluster centres.
4. Repeat the above two steps until the convergence occurs.

3 Proposed Gray-Scale-Based Fuzzy C-Means (GBFCM)

FCM algorithm usually improves the ruggedness of regions. This is also due to the conformity of the clustering and less complexity of the method; its applications in different areas of image analysis. Therefore, the pixels are clustered to display the pixels of the same cluster as a region [11].

To develop a new FCM-based algorithm with less computational cost, a gamma correction based method is introduced. Its basic criterion is required to minimize the objective function given by,

$$J_m = \sum_{i=1}^{N} \sum_{j=1}^{C} u_{ij}^{m} |x_i^{\gamma} - c_j|^2 \tag{1}$$

where m is any real number greater than 1. u_{ij} is the membership degree of x_i in the cluster j. x_i is the i^{th} d—dimensional measured data, γ is the power operator (or gamma) values lies between 0 and 1, c_j is the d—dimension centre of the cluster.

The proposed GBFCM method is described in the flowchart shown in Fig. 1. First, we initialize the cluster centres and read the input image as gray values. Thereafter

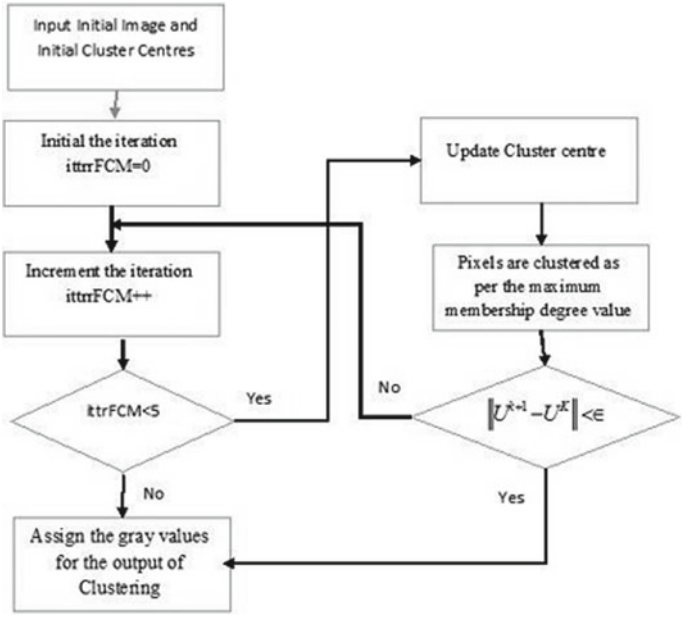

Fig. 1 Flowchart of proposed GBFCM method

the obtained gray values are clustered into five different clusters in five number of iterations based on the degree of membership function values that minimizes the given objective function at the optimal value of gamma (γ) as given in Eq. 1.

These five regions carried significant information in under or overexposure conditions. The pixels having exposure in terms of gray shades shows the hierarchal position of objects present, in the satellite image. The proposed GBFCM-based method shows pixels in terms of different grayscale values.

Algorithm 2 FCM Algorithm

1. Initialize matrix $U = [u^{ij}]$ randomly, i.e. say $U(0)$
2. In kth step: compute the centres vectors $c(k) = [c_j]$ with $U(k)$

$$c_j = \frac{\sum_{i=1}^{N} u_{ij}^{m} * x_i^{\gamma}}{\sum_{i=1}^{N} u_{ij}^{m}} \tag{2}$$

3. After computation of centre vectors, update the value of U_k and U_{k+1}

$$U_{ij} = \frac{1}{\sum_{k=1}^{c} \left(\left\| \frac{x_i^{\gamma} - c_j}{x_i^{\gamma} - c_k} \right\| \right)^{\frac{2}{m-1}}} \tag{3}$$

4. Check whether $\left\| U^{k+1} - U^{k} \right\| < \in$ If it is True then
5. STOP; otherwise continue and return to step 2.

Therefore, the different hierarchal regions are easily detectable. It also detects the changes observed with time by using the same captured image.

By introducing gamma correction to an objective function shows better performance for image segmentation of satellite images. These five centres increase or decrease the intensity values according to the gamma value. Finally, we assign the fixed five different gray values to each cluster obtained. These clusters segment the image as per the pixel similarity. These five homogenous regions detect the information in different shades. The proposed method modifies objective function by using the gamma values instead of the slower distance computation that reduces the pixels within local spatial neighbours and their clustering centres, which leads to low computational complexity. Therefore, in this paper, we introduce GBFCM-based method used in segmentation and address the problems associated with conventional thresholding based methods. Here, gamma correction reduces the shadowing effect that is favourable to satellite image segmentation.

4 Performance Metric

The four quantitative parameters are used in performance evaluation of the proposed technique and compared with the available existing technique are as follows.

4.1 Measurement of Signal-to-Noise Ratio (SNR)

The Signal-to-Noise ratio (SNR) is one of the most important statistical parameters for image or signal quality measurement. It is the ratio of signal power to noise power. It is mathematically represented as

$$\text{SNR (in dB)} = 10 \log_{10} \left[\frac{P_{\text{signal}}}{P_{\text{noise}}} \right] \tag{4}$$

where P_{signal} is the mean or expected value of the signal and P_{noise} is the variance of noise. When a value of SNR ratio higher than 1 (0 dB) then the power of the signal is higher in comparison to the power of the noise, this ensures lower distortion and less noise-induced interference.

4.2 Measurement of Mean Square Error (MSE)

Mean Square Error (MSE) is characterized as the error square expectation. This error is perhaps the difference between quantity of desire $f(i, j)$ and quantity estimated $F(i, j)$ for each pixel of the image [14].

$$\text{MSE} = \sum_{i=1}^{M} \sum_{j=1}^{N} |f(i, j) - F(i, j)|^2 / M \times N \tag{5}$$

The MSE is a way of selecting the best estimator. Ideal value of Mean Square Error is equal to zero.

4.3 Measurement of Peak Signal-to-Noise Ratio (PSNR)

Peak Signal-to-Noise Ratio (PSNR) is expressed as a ratio of the maximum signal power value to the noise power value that affects its representation's fidelity. Generally, it was in decibel (dB) terms. It is widely used in compression algorithms as a statistical measure of image reconstruction overall quality [15]. It is expressed mathematically by using the mean squared error (MSE) which is defined as a noisy approximation of another for two different $M \times N$ monochrome images are given by:

$$\text{PSNR} = 10 \log_{10} \left(\frac{\text{MAX}^2}{\text{MSE}} \right) \tag{6}$$

Here, MAX is the maximum pixel intensity value which is equal to 255 for an 8-bit image.

4.4 Measurement of Mean Absolute Error (MAE)

Mean Absolute Error (MAE) is the absolute difference between the reference image and test image [15]. It is given as

$$\text{MAE} = \frac{\sum_{i=1}^{M} \sum_{j=1}^{N} \left| \hat{X}(i, j) - X(i, j) \right|}{M \times N} \tag{7}$$

5 Simulation Results and Discussions

This section discusses the tools used for the simulation. It also describes the result obtained by the different classical and proposed method of image segmentation in detail.

5.1 Methodology Used

By using MATLAB 7.1 on Intel 64 bit processor I3, the proposed method was successfully simulated. Around 120 images have been tested and some of them (three) are presented here. We consider the discussed four performance metrics Mean Squared Error (MSE), Signal-to-Noise Ratio (SNR), Peak Signal-to-Noise Ratio (PSNR) and Mean Absolute Error (MAE). These metrics are evaluated for three different satellite images and tabulated in Table 1. It clearly shows from the result obtained that the proposed GBFCM method is better among the other methods. Figures 2a, 3a and 4a show the Low contrast satellite image from NASA's Earth Observatory. Figures 2b, 3b and 4b show the resulting image obtained by applying Otsu's method on the low contrast satellite image. Figures 2c, 3c and 4c show the K-mean clustering-based satellite images. Figures 2d, 3d and 4d show the resulted Fuzzy C-means based enhanced and segmented satellite images.

Figures 2d, 3d and 4d depict a much better performance in comparison to Otsu's and other threshold methods conventionally used for image segmentation. These images show more detail as compared to the other methods. Figure 2d shows that the brightness is more in the high-intensity region as compared to the other methods.

Table 1 Performance metrics—SNR, PSNR, MSE AND MAE values for GBFCM, OTSU, thresholding, and K-means clustering methods

	Methods	SNR	PSNR	MSE	MAE
Figure 2	Proposed method	56.69	15.0755	2020.78	35.10
	OTSU method	48.20	6.58508	14,274.85	110.43
	Thresholding	48.23	6.61214	14,186.18	109.92
	K-means clustering	48.37	6.75625	13,723.198	108.17
Figure 3	Proposed method	52.44	14.3043	2413.50	38.71
	OTSU method	48.22	10.0812	6382.04	68.35
	Thresholding	48.24	10.1002	6354.13	68.12
	K-means clustering	48.44	10.3036	6063.40	66.35
Figure 4	Proposed method	55.61	6.58793	14,265.50	91.517
	OTSU method	52.47	3.44290	29,429.94	142.92
	Thresholding	52.47	3.447052	29,401.88	142.82
	K-means clustering	52.55	3.5223	28,896.72	141.15

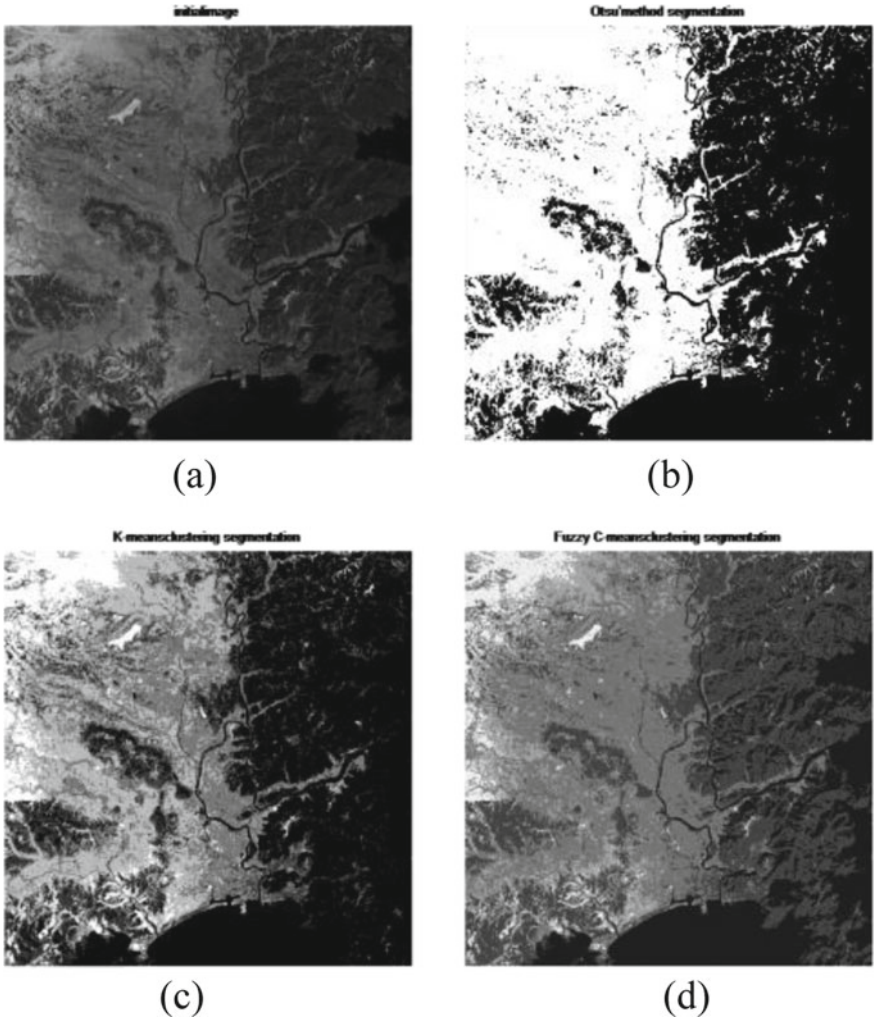

Fig. 2 **a** Low contrast satellite image from NASA's Earth Observatory. **b** OTSU method based satellite image. **c** K-means clustering-based satellite image. **d** Proposed GBFCM-based enhanced satellite image

In other methods, the intensity value gets increased in the low-intensity region. The signal-to-noise ratio achieved is 56.69 dB which is comparable with the threshold method, Otsu's, k-mean clustering as 48.20 dB, 48.23 dB, 48.37 dB, respectively. When we applied the same proposed method on the other two test images it showed that the resulting image obtained is more likely suitable than the other three techniques. Figures 3d and 4d show more information in terms of gray shades. Table 1 depicts that the signal-to-noise ratio has values 52.44 dB, 55.61 dB which is higher than the other techniques. Similarly, we have shown for other two test images that

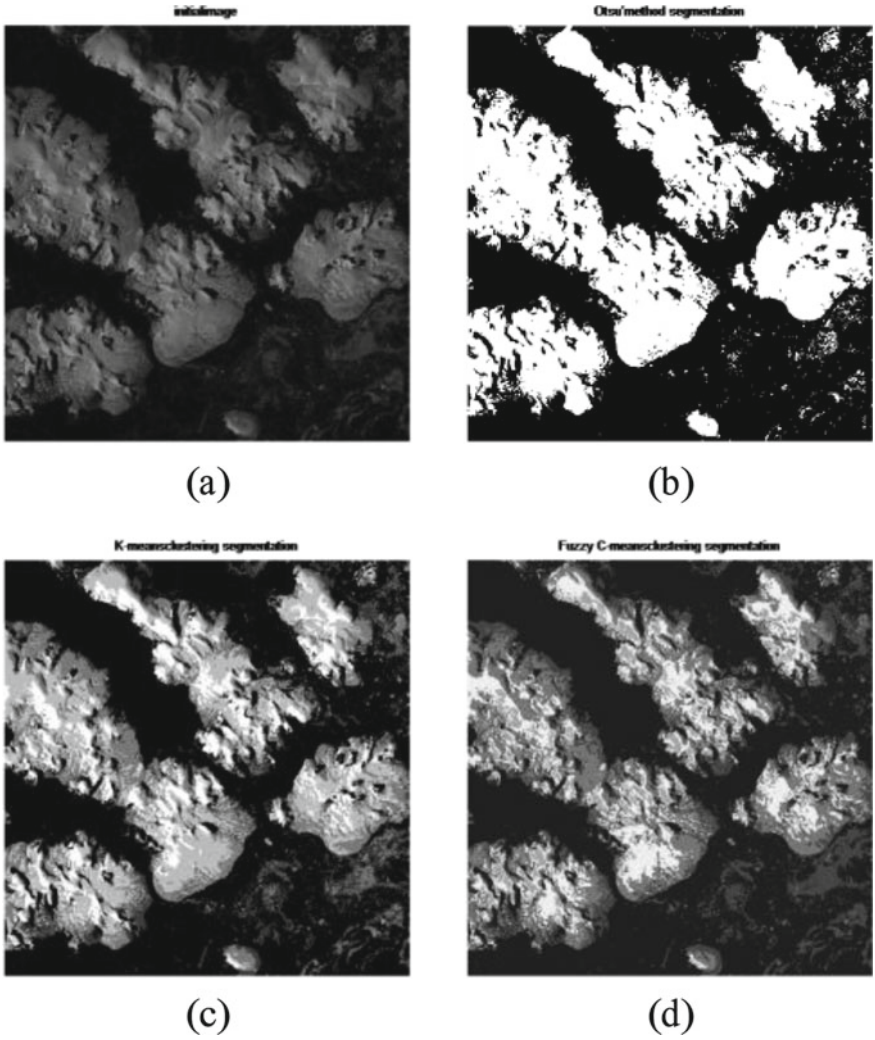

Fig. 3 **a** Low contrast satellite image from NASA's Earth Observatory. **b** OTSU method based satellite image. **c** K-means clustering-based satellite image. **d** Proposed GBFCM-based enhanced satellite image

the proposed method performs well as compared to the other three techniques. In Fig. 4d, we have shown that the image obtained from the proposed method is brighter than the other methods even though it has more details and brighter than the other. The proposed method shows that the contrast and intensity increases by maintaining the original information in the image but other methods fail to maintain the original information as seen in the test images.

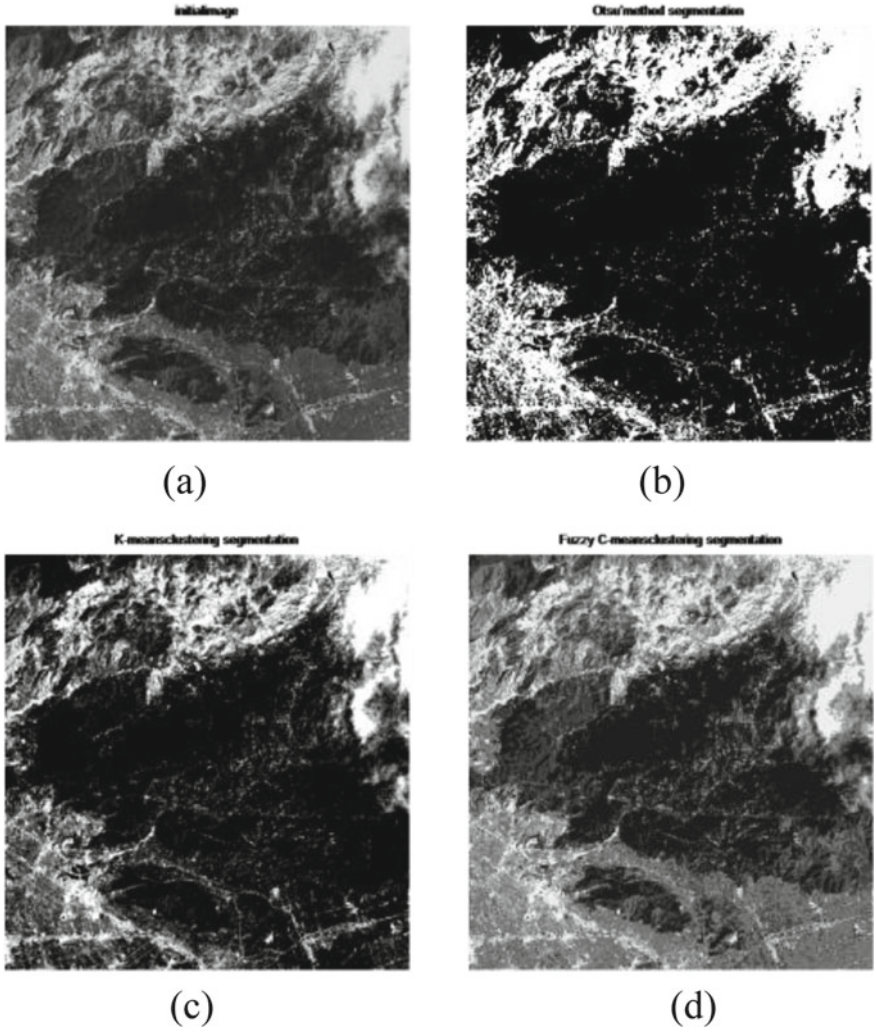

Fig. 4 **a** Low contrast satellite image from NASA's Earth Observatory. **b** OTSU method based satellite image. **c** K-means clustering-based satellite image. **d** Proposed GBFCM-based enhanced satellite image

6 Conclusions

There are many fuzzy clustering algorithms, but the algorithm used most often in satellite image segmentation is the FCM algorithm because of the fact that ambiguity can be handled and much more information can be given compared to K-means. Also for noise-free images, the FCM algorithm works well. This work is also useful for the

classification of the images. The proposed GBFCM uses gamma correction which is faster in distance computation and more detailed information can be achieved.

The proposed algorithm confirms its statistical approaches effectiveness by comparing the results attained with the existing SNR approach and gaining higher values for PSNR, whereas, MSE and MAE are lower, which signifies that the image achieves more fine details as compared to the other methods. It can, therefore, be proved that the performance of the proposed algorithm is much better than that of the existing approach.

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Built-in Reliability Investigation of Gate-Drain Underlapped PNIN-GAA-TFET for Improved Linearity and Reduced Intermodulation Distortion

Rahul Pandey, Jaya Madan, Rajnish Sharma, Minaxi Dassi, and Rishu Chaujar

Abstract This work investigates the built-in reliability of four different TFET candidates by assessing the linearity performance and harmonic distortion (HD). The Gate-Drain Underlapped, n+pocket, cylindrical GAA-TFET (GDU-PNIN-GAA-TFET), a result of the amalgamation of two highly successful engineering schemes and a potential transistor candidate as a result of analog performance improvements in other respects, forms the primary device whose linearity/HD parameters are analyzed through industry-standard linear performance metric like V_{IP2}, V_{IP3}, IIP3, ZCP and P1dB, HD2 and HD3, respectively. In order to gauge the progressive improvement of the GDU-PNIN-GAA-TFET, the simulation results for the intermediate engineered devices (GDU-GAA-TFET, PNIN-GAA-TFET) are compared with those of the conventional TFET. A remarkable improvement in the performance of GDU-PNIN-GAA-TFET is observed. This indicates the possibility of operation of the GDU-PNIN-GAA-TFET as a reliable device for future low-power, high-frequency wireless applications that are peeping over the horizon.

Keywords Double gate · Gate-drain underlapping (GDU) · Harmonic distortion (HD) · Linearity · n+source pocket · Tunnel FET

R. Pandey (✉) · J. Madan · R. Sharma
VLSI Centre of Excellence, Chitkara University Institute of Engineering and Technology, Chitkara University, Punjab, India
e-mail: rahul.pandey@chitkara.edu.in

J. Madan
e-mail: jaya.madan@chitkara.edu.in

R. Sharma
e-mail: rajnish.sharma@chitkarauniversity.edu.in

M. Dassi
Chitkara University School of Engineering and Technology, Chitkara University, Himachal Pradesh, India
e-mail: minaxi.dassi@chitkarauniversity.edu.in

R. Chaujar
Department of Applied Physics, Delhi Technological University, Delhi, India
e-mail: chaujar.rishu@dtu.ac.in

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1 Introduction

The concept of quantum mechanical tunneling implemented as an operating principle has replaced the concept of thermionic emission altogether in field-effect transistors and the same has been authenticated by Appenzeller in 2004, with the fabrication of first carbon nanotube TFET [1]. Since then TFET has proven to be an excellent candidate to replace MOSFET, but the popularity that MOSFET gained in the electronics industry within a decade of its inception, TFET has yet to achieve [2]. This is due to the fact that MOSFET has been the basic building block that led to the advancements in the CMOS technology resulting in IC revolution. The industrial sluggishness in the embrace of TFETs can in part be attributed to the fact that we are not as keenly in search of a modern transistor candidate for microelectronic applications today as we were when the MOSFET was first fabricated. However, to meet the large demand of the miniaturized devices in future, low-power devices that are as efficient as the MOSFET will be required.

To ensure the reliable operation of any CMOS device for wireless applications, minimization of intermodulation and high-order harmonics is understood to be essential [3]. The primary effort of this work is to improve upon the linearity and distortion parameters of conventional TFETs, while preserving their superior analog performance so as to make them more suitable for use in engineering systems. For designing a portable system using power amplifiers it is generally advantageous to maintain the linearity at transistor level. TFETs were conceptualized to be gated p-i-n devices that could be seamlessly integrated with MOSFETs using extant VLSI fabrication infrastructure [4].

Since conduction in TFET is due to quantum mechanical Band-to-Band Tunneling (BTBT) in which the majority carrier electrons tunnel the potential barrier at the source-channel interface and these tunneling electrons constitute the majority current in TFET as compared to the electrons that are thermally generated in MOSFETs [5, 6]. This carrier injection mechanism attributes some desirable features to TFETs like achieving subthreshold swing less than 60 mV/decade, which is the limit imposed on MOSFETs due to Fermi-Dirac statistics and low OFF-state current. Thus, making it applicable for high speed and low-power applications [7, 8].

Further, TFET design and functionality have undergone tremendous change with the incorporation of engineering schemes, such as Gate-Drain Underlapping (GDU) (to tackle ambipolarity) and source pocket implantation (enhancing ON-state current). Their amalgamation has been considered in this work [9–11]. Today, with attempts to increasingly technologize our living spaces and urban environments (with IoT and smart cities, for instance) and simultaneously decrease power consumption, a necessity has arisen for low-power electronic components that demonstrate highly linear behaviors at wireless frequencies. This necessity can be fulfilled by TFETs adapted for highly linear operation [3]. Thus, in this work, the linearity of TFETs with GDU scheme and source pocket incorporation (i.e., GDU-PNIN-GAA-TFET) has been analyzed using signal performance metrics such as V_{IP2}, V_{IP3}, Input Intercept Point 3 (IIP3) and zero crossover point. These performance metrics indicate that

there is a substantial improvement in the linear performance of a TFET with both GDU scheme and p-n-i-n structure making it suitable for high-frequency engineering applications that simultaneously require low-power dissipation.

2 Device Design Parameters and Simulations

The 3-D and cut plane view of cylindrical GAA-TFET with underlapped gate near drain and n+pocket engineering is shown in Fig. 1a–b respectively. The radius/channel length of the device is 10 nm/50 nm with a gate oxide (SiO_2) thickness of 2 nm. For optimum device performance as shown in our previous work [11, 12]: (i) the gate metal workfunction is set to $\Phi_M = 4.3$ eV for maximum I_{ON}/I_{OFF}, (ii) the gate is underlapped on drain by 15 nm, and (iii) the n+pocket width/doping is 4 nm/4 $\times$ 10^{19}cm^{-3}, respectively. Further, the p+source and n+drain doping are 1 $\times$ 10^{20}cm^{-3} and 5 $\times$ 10^{18}cm^{-3}, respectively. All simulations are performed using commercial Silvaco ATLAS TCAD [13]. The simulation setup is calibrated with the

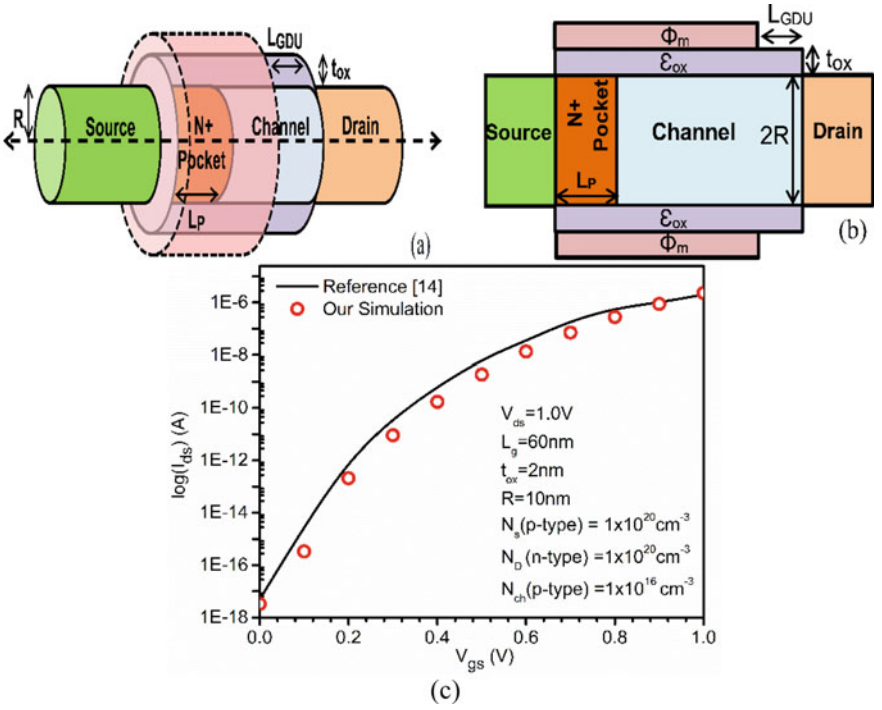

Fig. 1 **a** 3-D view of cylindrical GAA-TFET with N+source pocket and gate drain underlapping. **b** Cut plane view of GDU-PNIN-GAA-TFET. **c** Calibration of transfer characteristics with experimentally reported work [14]

experimentally reported work [14]. The calibration is done by varying the tunneling mass of electron and hole for non-local band-to band tunneling model (n-BTBT). The tunneling mass of electrons and holes are tuned in such a manner that the drain current of the simulated device (designed similar to the experimental device) is matched with the transfer characteristics of the experimentally reported device.

The transfer characteristics are well-matched with reported experimental data by setting me.tunnel and mh.tunnel at 0.22 m_o and 0.52 m_o, respectively from their respective default values as shown in Fig. 1c. Further, the n-BTBT model is used in conjunction with Shockley- Read-Hall (SRH) recombination, bandgap narrowing (BGN), and concentration and field-dependent mobility models (CONMOB) for simulating the ON-state current (I_{ON}) in an optimal manner. The carrier distribution was modeled by Fermi-Dirac statistics. Further, Newton and Gummel methods were used for numerical simulation. The devices under consideration (DUCs) in this work are GDU-PNIN- GAA-TFET and their conventional counterparts, i.e., GDU-GAA-TFET, PNIN-GAA-TFET, and GAA-TFET.

3 Results and Discussions

The transfer characteristics of the engineered devices, i.e., PNIN and GDU architectured GAA-TFET are depicted in Fig. 2. A considerable improvement in drive current from an order of 10^{-8}A to 10^{-5}A can be seen with implantation of n+pocket in the channel. This improvement in drive current is a consequence of sharper band bending at the source side due to the implantation of n+pocket. This band bending is localized at the interface of source and n+pocket and after tunneling through the source/pocket interface, the electrons flow as a result of the conventional drift-diffusion mechanism.

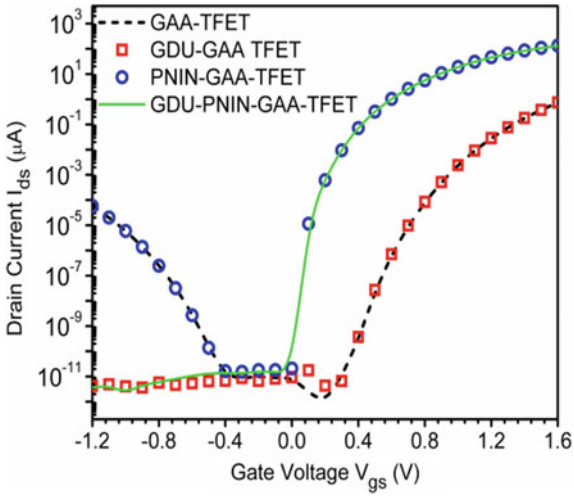

Fig. 2 Drain current (I_{ds}) w.r.t. gate voltage (V_{gs}) of all the DUCs at constant V_{ds} = 1.0 V

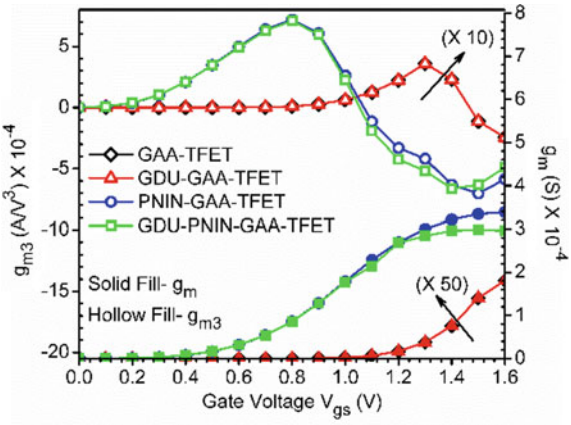

Fig. 3 Transconductance (g_m) and g_{m3} for all the DUCs at constant drain voltage $V_{ds} = 1.0$ V

Device biasing at a V_{gs} corresponding to the peak of g_m curve ensures highest gain. In Fig. 3, it can be seen that the PNIN engineered devices demonstrate very high g_m. If the device is biased at the optimized V_{gs}, i.e., the zero crossover of g_{m3}, the nonlinear behavior of the g_{m3} can be minimized. Thus, for a small signal, Harmonic Distortion (HD) caused by g_{m3} can be diminished by simply biasing the device at the Zero Crossover point (ZCP) of g_{m3}. The ZCP is the V_{gs} at which g_{m3} falls to zero. The curves of Fig. 3 for g_{m3} are shifted towards lower V_{gs} for PNIN-GAA-TFET and GDU-PNIN-GAA-TFET. By implication, lower V_{gs} will be needed to bias these devices for cancellation of the HD caused by g_{m3}.

V_{IP2}/V_{IP3} signifies improved linearity and low distortion operation and is evaluated as (see Eq. 1) and (see Eq. 2), according to literature [15].

$$V_{IP2} = 4\frac{g_{m1}}{g_{m2}} \tag{1}$$

$$V_{IP3} = \sqrt{24\frac{g_{m1}}{g_{m3}}} \tag{2}$$

Figure 4a clearly depicts appreciably high singularity peaks of V_{IP2} and V_{IP3} with implantation of the n+pocket. Further, peaks are acquired at lower V_{gs} as compared to their conventional counterparts. This translates to preservation of linearity at lower V_{gs} with n+pocket. Another important linearity parameter of a device is IIP3 (i.e., third order intercept input power). It is input power at which first and third harmonic powers are equal and is assessed by (see Eq. 3) [15] IIP3 should be maximized for high linearity operation. It can be seen in Fig. 4b that considerably higher IIP3 is obtained after the implantation of n+source pocket in a conventional TFET. This improved IIP3 is attributed to the abrupt band bending caused by n+pocket, which significantly enhancing e$^-$BTBT rate, and concomitantly g_m.

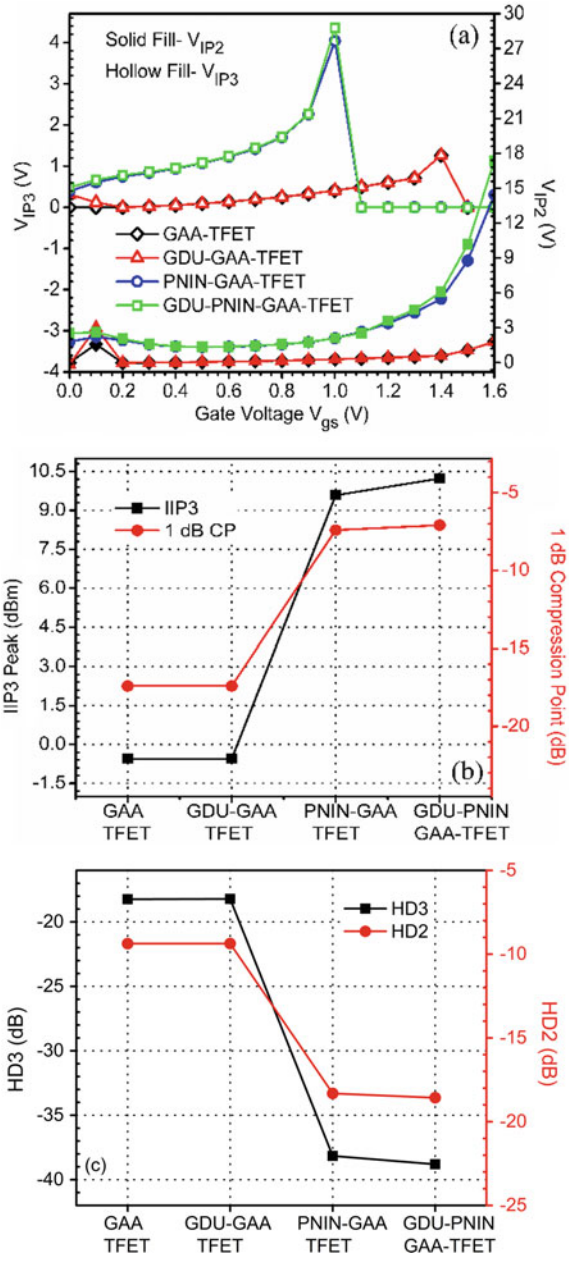

Fig. 4 **a** V_{IP2}/V_{IP3} w.r.t. V_{gs} **b** IIP3/P1-dB **c** HD2/HD3 for all DUC at $V_{gs} = V_{ds} =$ 1.0 V

$$\text{IIP3} = \frac{2}{3} \times \frac{g_{m1}}{g_{m3} \times R_s} \tag{3}$$

An important performance parameter of an amplifier circuit is its 1 dB compression point (P1dB). It represents the maximum input power that can be handled by amplifier circuit while delivering constant gain. Beyond this input power, the gain of amplifier circuit decreases. P1dB is assessed by (see Eq. 4).

$$1dB \text{ Compression Point} = 0.22\sqrt{\frac{g_{m1}}{g_{m3}}} \tag{4}$$

Figure 4c depicts the P1dB for all DUC. The higher P1dB of PNIN-GAA-TFET and GDU-PNIN-GAA-TFET signify that implantation of an n+pocket in TFET may render it feasible for Low Noise Application (LNA). This higher P1dB with n+pocket is due to reduced distortion and higher g_m as a result of steeper band bending in ON-state of the device. To meet the demands of next-generation wireless communication technology, low distortion devices are imperative. HD FOMs, i.e., third order HD (HD3) evaluated by (see Eq. 5) and (see Eq. 6) is shown in Fig. 4c [16]. Lower values of HD2/HD3 are generally understood to be desirable for LNA and HF applications.

$$\text{HD2} = 0.5V_a\left(\frac{dg_{m1}}{dV_{gs}}\right)/(2g_{m1}) \tag{5}$$

$$\text{HD3} = 0.25V_a^2\left(\frac{d^2g_{m1}}{dV_{gs}^2}\right)/6g_{m1} \tag{6}$$

where V_a(=50 mV) is the amplitude of the AC signal. The reduction in HD2/HD3 of PNIN-GAA-TFET and GDU-PNIN-GAA-TFET leads to an improvement in the device linearity and minimizes HD. Further, to ensure minimum signal distortion another important parameter, i.e., the third order intermodulation distortion, IMD3 is evaluated. It is the extrapolated intermodulation power at which the first and third order intermodulation harmonic powers are equal and is evaluated by (7) [17]:

$$\text{IMD3} = \left[\frac{9}{2}(\text{V}_{\text{IP3}})^3 g_{m3}\right]^2 . R_s \tag{7}$$

For improved device performance or reduced signal distortion, IMD3 should be minimum. Figure 5 shows that IMD3 reduces appreciably with the implantation of n+pocket, i.e., for PNIN-GAA-TFET and GDU-PNIN-GAA-TFFET in comparison with their conventional counterparts. This reduced IMD3 with n+pocket reduces the signal distortions and thereby makes PNIN-GAA-TFET a promising contender for the wireless communications system.

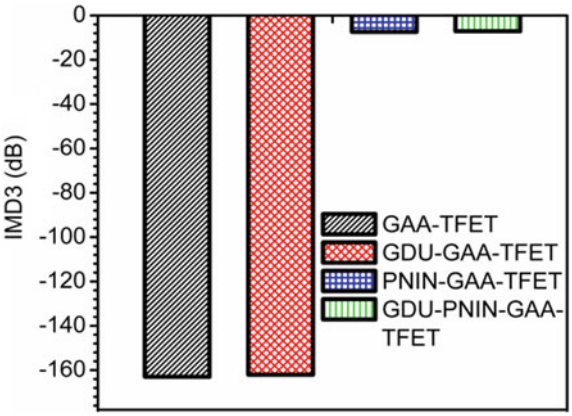

Fig. 5 IMD3 for all DUC at $V_{gs} = V_{ds} = 1.0$ V

4 Conclusion

This work shows the superiority of GDU-PNIN-GAA-TFET for HF, low-power applications through an analysis of linearity and HD FOM such as V_{IP2}, V_{IP3}, IIP3, ZCP and P1dB, HD2 and HD3. The results herein show a significant reduction in distortion parameters with the integration of N+source pocket along with superior drain current. The well-understood benefit that accrues to the device by implantation of this pocket compounds the effect of gate-drain underlapping to result in a robust device with reduced ambipolarity. This work also sheds light on the fact that implantation of the n+pocket leads to improved linearity of the device. Further, the GDU-PNIN-GAA-TFET preserves the linearity improvement of the PNIN-GAA-TFET while also tackling the persistent problem of ambipolarity in TFETs. Therefore, the resultant device, i.e., GDU-PNIN-GAA-TFET, is a competent candidate for the upcoming wireless era in which hitherto commonplace devices may not be able to fulfill the world's low-power, HF applications.

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Efficiency Enhancement of Solar Panel Using Photodiode

Mohammed Asim, Mohd Suhail Khan, Javed Ahmad, Taufique Umar, and Ahmed Riyaz

Abstract Solar energy is becoming a very fast and important means of renewable sources of energy. The output of solar panels varies with movement of the sun. In order to track maximum power, maximum power point trackers are used to track maximum power from the solar panel. With the solar tracking, more energy generation is possible, since the solar panel can maintain a perpendicular profile to the rays of the sun. Hence, increasing the overall efficiency of the solar panel.

Keywords Solar cell · DC motor · LDR

1 Introduction

Solar energy is the form of energy that has been received from the sun in heat and light form and that is used over a range of ever-evolving technologies such as solar cells. Majority of the world's current electricity is supplied generated from fossil fuels such as coal, oil and natural gas, because of the depletion of fossil fuel, increase in their cost, environmental pollution, etc. solar PV is much in demand. Important advantage of solar energy is that its production causes no pollution, modularity and flexibility [1–3]. Solar energy is one of the important sources of renewable energy

M. Asim · M. S. Khan · T. Umar
Department of Electrical Engineering, Integral University, Lucknow, India
e-mail: asimamu@gmail.com

M. S. Khan
e-mail: mohdsuhail1991@yahoo.com

T. Umar
e-mail: taufiqueumr30@gmail.com

J. Ahmad
University Teknologi, Malaysia (UTM), Skudai, Malaysia
e-mail: ahmad.1995@graduate.utm.my

A. Riyaz (✉)
Department of Electrical Engineering, BGSB University, Rajouri, India
e-mail: ahmedriyaz@bgsbu.ac.in

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and the technologies of solar cell are broadly classified as active and passive solar technologies depend upon how they absorb and distribute solar energy. Active solar technologies deal with the used of PV systems, concentrated solar PV system and many more Whereas, passive solar technologies the window, walls, floor which are made to collect, store and distribute energy in the form of heat in the winter season and rejects the heat in the summer season [4–6]. The difference between the active and passive systems is that in passive systems it does not require the use of the electrical and mechanical drive. The sun can be similar to a black body of 5760 K with a solar irradiance of 1370 W/m^2 at one astronomical unit distance. Incoming solar radiation at the upper atmosphere of the earth are about 174,000 terawatts (TW) out of which 30% is reflected back to space and rest of them is absorbed by land and oceans. Solar power is the conversion of sunlight into electricity, either directly using photovoltaic (PV), or indirectly using concentrated solar power. The international energy agency in 2014 projected that by 2050, about 16–11% of electrical power will be contributed from the solar photovoltaic and concentrated solar power. Initially, the photovoltaic solely used as a source of electricity for small- and medium-sized applications, calculated power from a single solar cell to remotely located homes that are powered by an off-grid rooftop PV system. As there is a decrease in the cost of electricity obtained from solar, the number of grid-connected solar PV systems has grown into the millions and the utility-scale of solar power stations with hundreds of megawatt are being built. Solar PV is rapidly becoming an inexpensive, low-carbon technology to harness renewable energy from the sun. The largest power station of solar photovoltaic in the world is about 850 MW which is in china. In this paper, model with one solar panel, two LDRs, one microcontroller and two DC motors are used. The setup of this model is such that solar panel is facing the sun. The solar panel is placed on a wooden board; one of the DC motors is placed behind the wooden board which moves the panel in vertical direction and the other DC motor rotates the panel along the horizontal axis.

In this paper, model with one solar panel, two LDRs, one microcontroller and two DC motors are used. The setup of this model is such that solar panel is facing the sun. The solar panel is placed on a wooden board; one of the DC motors is placed behind the wooden board which moves the panel in vertical direction and the other DC motor rotates the panel along the horizontal axis. When sun moves away from the solar panel, some of the rays fall on the photodiode which is connected to the DC motor, and hence it will power the DC motor. Due to which the motor will rotate the panel towards the direction of the sun until the panel casts a shadow on the photodiode, and the photodiode stops receiving the sunlight. The microcontroller used in the setup is known as Arduino Uno R3 microprocessor. The code in Adruino Web Editor is written in C++ language. The program code helps in comparing the resistance of the two LDR's precisely. The hardware model of our proposed work is shown in Fig. 5, the output reading of voltage, current and power with and without tracking mechanism is shown in Table 1. Comparison of output power with and without tracking mechanism is shown in Table 2.

Table 1 Reading of the setup

Without tracking mechanism				With tracking mechanism		
Time	Output voltage	Output current	Output power	Output voltage	Output current	Output power
9 a.m.	4.92	0.06	0.295	6.12	0.09	0.558
10 am	5.36	0.07	0.376	6.43	0.10	0.643
11 a.m.	5.42	0.07	0.379	6.53	0.12	0.783
12 noon	4.76	0.06	0.285	6.21	0.08	0.496
1 p.m.	4.98	0.06	0.298	6.62	0.13	0.860
2 p.m.	5.67	0.07	0.396	6.47	0.09	0.582
3 p.m.	5.84	0.08	0.468	6.35	0.10	0.635

Table 2 Comparison of output power with tracking mechanism

Time	Output power without tracking mechanism (W)	Output power with tracking mechanism (W)	Increase in output power (w)
9 a.m.	0.295	0.558	0.263
10 a.m.	0.376	0.643	0.267
11 a.m.	0.379	0.783	0.404
12 noon	0.285	0.496	0.211
1 p.m.	0.298	0.860	0.562
2 p.m.	0.396	0.582	0.186
3 p.m.	0.468	0.635	0.167

2 Literature Review

Our solar panel design deals with the problem of a solar panel not facing towards the sun. As we all know that solar panels are static devices, hence they cannot change their positions according to the continuously changing position of the sun with respect to the solar panel. In order to tackle this problem, three types of solar models are designed.

2.1 Solar Panel with a Single Photo Diode and a DC Motor

Figure 1 shows the model of a solar panel with a single photodiode and a DC motor. The solar panel is placed on a wooden board. The DC motor has been placed behind the wooden board, with a photodiode mounted on it. When the sun moves away from the solar panel, some of the rays fall upon the photodiode, which is connected to the DC motor, and hence it will power the motor. The motor would rotate the panel towards the direction of the sun until the panel casts a shadow on the photodiode,

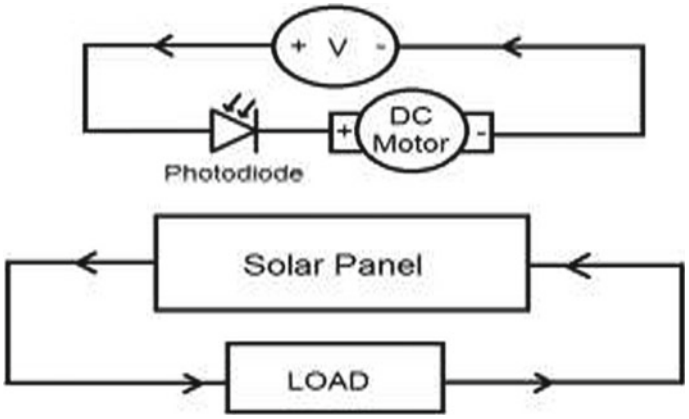

Fig. 1 A circuit diagrams to represent the setup of the proposed model

and the photodiode stops receiving the sunlight [7–9]. A voltage source is present to power the DC motor. Now, the voltage source present is such that it is not sufficient to power the motor. The motor would only move when the photodiode is conducting as well. This is done to prevent the DC motor from working when the photodiode is not conducting, otherwise the motor would run independently, without the use of photodiode. The solar panel would provide an output of around 1 W. The motor's speed is around 10 rpm. The torque of the motor is dependent upon the minimum torque required to rotate the panel. The biggest disadvantage of this model is that the solar panel does not face the sun completely since the shadow on the photodiode is cast before the panel would face the sun completely. Another disadvantage is that after the sunset, the panel needs to be manually rotated to the position where it would be facing the sun during sunrise. Hence we have come up with two other models.

2.2 Solar Panel with Two Extra-Solar Cells and DC Motor

We have installed two more solar cells in addition to our main one. These are placed at either edge of the main solar panel, making an angle of 90° with the main solar panel. The function of these solar cells is to supply power to our DC motor present behind the main solar cell, which would rotate the solar panel, when powered. The basic idea behind this setup is that whenever the sun shifts away and the solar panel is not able to receive maximum sunlight, the solar panel placed at 90° with the main panel (let's call it panel B) would receive the sunlight unable to reach the main solar panel. As a result, it will power the motor, which would rotate anti-clockwise. Now since our main solar panel is connected to the motor, it will also rotate in the direction of motor, and will also rotate anti-clockwise, and will continue its rotation, unless the motor stops working. This can only happen when solar panel B is unable to receive

sunlight. As a result, the main solar panel will again receive maximum sunlight as it was receiving while facing the sun. This process will continue until the time of sunset [10, 11]. Now at the time of next sunrise, the panel must face the direction of the sun. In order to achieve this, we have installed solar panel A, whose function is the same as solar panel B that is to track maximum sunlight at the time of sunrise. But the main difference is that the polarity of the motor has been reversed in this case. As a result, solar panel A will rotate the main panel clockwise, while solar panel B will rotate the panel anti-clockwise. In this manner, we are able to create a solar panel that would be able to rotate according to the change in position of the sun with respect to the panel. The main solar panel is of 1 W. The added two extra-solar panels give the same output each. Any obstruction in the path of sunlight and the entire setup (main solar panel, solar panels A, solar panel B, DC motor) is prohibited as it will interrupt the proper functioning of the setup. This setup has two solar panels to track the sunlight more effectively as compared to the previous model. But the disadvantage of this model is that it is bulky and occupies more space. Second, the extra-solar panels would cost more.

2.3 Solar Panel Two LDR and a Microcontroller

Figure 2 shows an alternative to the previous model, we designed another model, which follows the same principle of detecting the maximum sunlight, but unlike the previous model, we have not used additional two solar panels to track the maximum sunlight. Instead, in this model, we have used two light-dependent resistors. A Light-Dependent Resistor has a high resistance in the dark and low resistance in the light. Two LDR's are used which are placed on the top of the panel as shown in Fig. 3. Tracking of the system is done by using microcontroller.

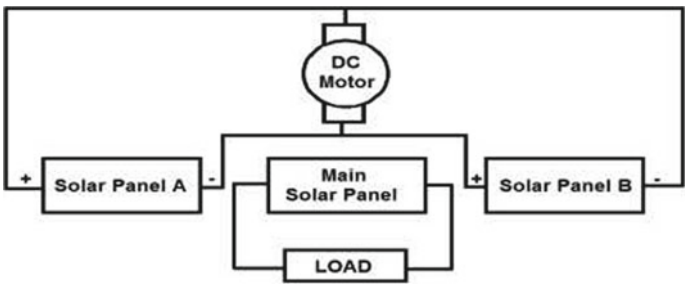

Fig. 2 A circuit diagram to represent the working of the second proposed model

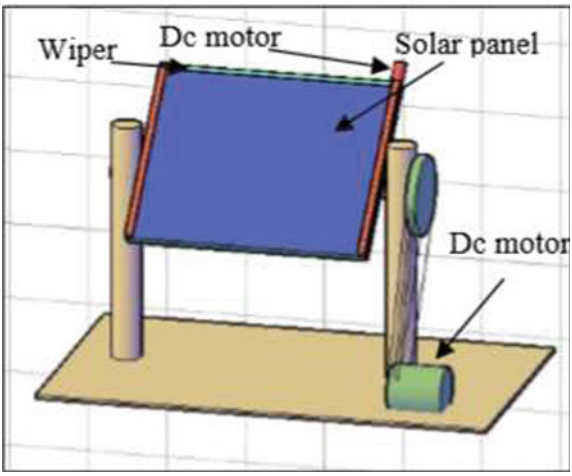

Fig. 3 A circuit diagram to represent the working of the third proposed model

3 Proposed Model

By considering the pros and cons of three proposed model the most beneficial and effective model is to use solar panel with two LDRs, one microcontroller and one DC motor to track the maximum sunlight shown in Fig. 4. In this proposed model two LDR (light-dependent resistors) are used, the LDR changes the value of resistance according to the light falling on it. The resistance value of this LDR is very high, sometimes it is greater than 10 MΩ, when the light falls on this LDR the resistance of these LDR drops drastically. This LDR has a very large value of resistance in the night time and a low resistance value in the day time. In our proposed work, we use two LDR which are placed on the top of the solar panel as shown in Fig. 4. The proposed model consists of two DC motors, one rotating the panel along the vertical axis (present below the wooden table on which the solar panel is mounted on), and the other DC motor rotating the panel along the horizontal axis. The entire circuitry is driven by a 9 V battery. The solar panel is first rotated along the vertical axis by the DC motor mounted below the wooden table. This motor rotates the panel along the direction of the LDR receiving more illumination (and thus having lower resistance), that is, in a clockwise direction or counter-clockwise direction.

4 Control Strategy

System which automatically tracks the light of the sun is done by using the microcontroller (P89V51RD2) through which the given requirement can easily be achieved at low cost. Controlling of DC motor that is mounted to make the panel to track the sun by receiving information from the LDR is done by using microcontroller. The

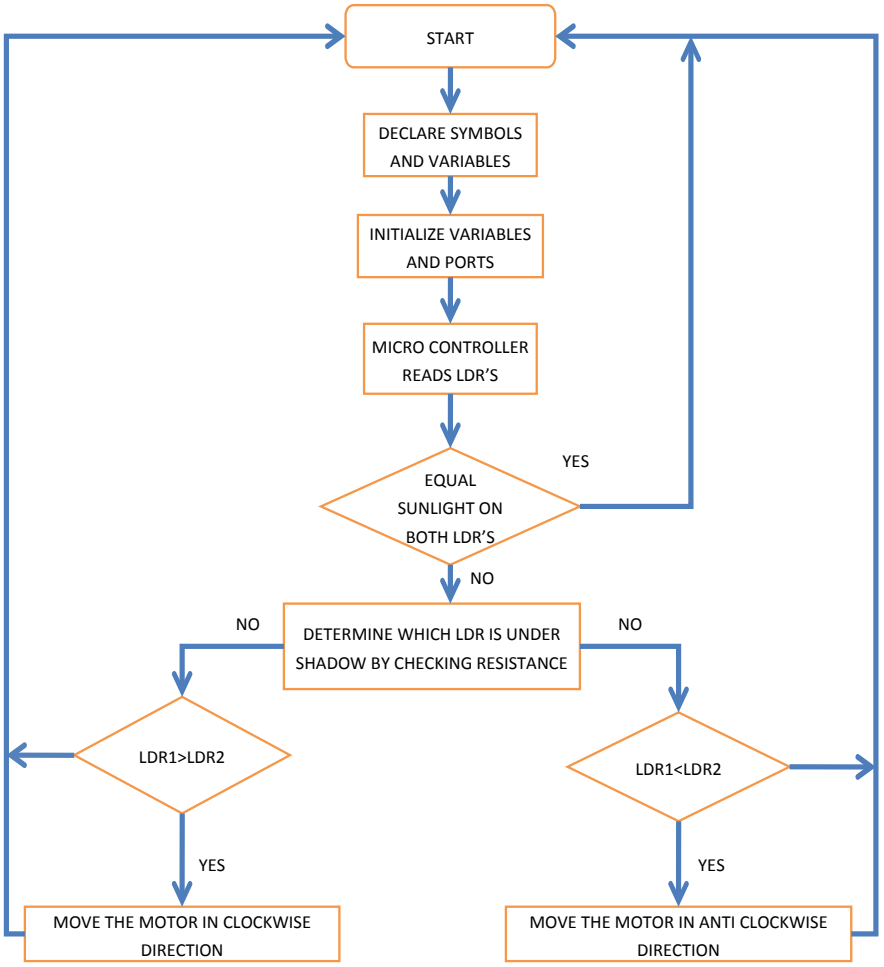

Fig. 4 An arrangement of solar panel with a microcontroller, LDRs and DC motor

algorithm for sun tracking is very easy to understand, it works by using the microcontroller, compares the intensity of light falling onto the LDRs. When the light of the sun falls on these LDR's, the resistance values of these LDR's are checked and a motor whose rating is 10 rpm is connected to the panel which rotates in the direction where the resistance value of LDR is less, till the value of resistance on the both of LDRs are equal. As we can see clearly, the basic working of this model is similar to the previous one, except that in this model, we have used two LDR's instead of two solar panels. As a result, the model becomes less bulky and lighter. In addition to this, the solar panel has more space to move. Another difference is that the previous model was rotating along the vertical axis, while this model is rotating along the horizontal axis.

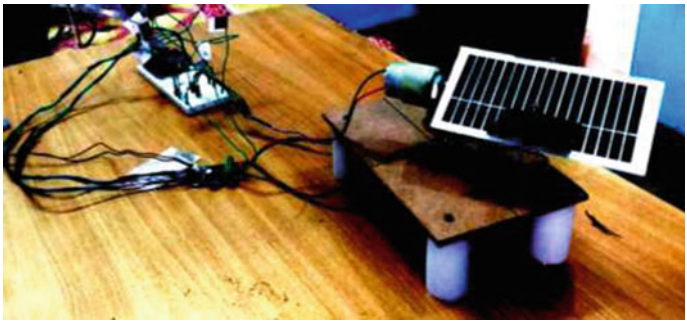

Fig. 5 A photographic representation of the constructed model, using 80 W lamp as a source

5 Experimental Setup

Considering the pros and cons of the three proposed models, the model with one solar panel, two LDRs, one microcontroller and one DC motor turns out to be the most beneficial as well as an effective model. Hence, a model, similar to the proposed model with two LDRs, one microcontroller and one DC motor has been constructed. The constructed model consists of two DC motors, one rotating the panel along the vertical axis (present below the wooden table on which the solar panel is placed on), and the other DC motor rotating the panel along the horizontal axis. The entire circuitry is driven by a 9 V battery. The solar panel is first rotated along the vertical axis by the DC motor mounted below the wooden table. This motor rotates the panel along the direction of the LDR receiving more illumination (and thus having lower resistance), that is, in clockwise direction or counter-clockwise direction (Fig. 5).

6 Analysis and Output Results

We can clearly see that the output power obtained in every case is more in the solar panel with tracking mechanism compared to the setup without tracking mechanism. It follows that the overall efficiency of the solar panel system is improved when the tracking mechanism is installed in the same solar panel efficiency is given by the ratio of output power to the input power. Now in order to find out the increase in efficiency, we simply divide the output power of the solar panel with the tracking mechanism to the output power of the solar panel without tracking mechanism.

So, it is clear from the above calculations that there is a considerable increase in the output power of the solar panel with tracking mechanism as compared to the setup without tracking mechanism. Thus, since the output power is the same because the time is the same during the comparison of solar panels with and without tracking mechanism, the increase in output power indicates an increase in efficiency.

7 Conclusion

Designing and implementation of the system is done which tracks the solar energy received from the sun. The required program was written that specified various actions required for the apparatus to work as a result of which the tracking mechanism of the system was achieved. The designing of the system is done on a dual-axis tracking as it is known that the dual-axis tracking mechanism is more efficient in tracking the sun as compared to single-axis tracking. Dual-axis tracks are more suitable in regions where there is a frequent occurrence of partial shading of the solar panel due to obstructing of insolation received by the panel, like tall buildings, etc., or due to cloud formation. The projected was implemented with a minimum investment in equipment were used without affecting the efficiency or the working of the overall system.

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Performance of Solar Cell Under Changing Atmospheric Condition

Saloni Sinha, Piyush Agarwal, Nitin Kumar Gupta, Mohammed Asim, and Ahmed Riyaz

Abstract Solar panel or solar photovoltaic array helps in maximum utilization of energy during daytime that is from sunrise to sunshade. However, shading on solar panels can have a huge impact on the performance of solar photovoltaic panels. This shading has severed effects on the output of solar cells. But most of the time a common misconception occurs that the partial shading does not make any impact on the output of solar panels. But solar photovoltaic panels are highly susceptible to changing atmospheric conditions and the shades falling on it. Solar insolation, the surrounding temperature, array configuration and shading on solar panels affect the performance of the solar photovoltaic array. Basically, the solar photovoltaic panel consists of several cells that are connected to each other in a series circuit. Because of this series connection, the performance of the solar panel is significantly reduced even if the smallest section of the solar panel is shaded. Due to any of the factors such as passing of the clouds, neighbouring buildings, towers, trees and the presence of the telephones poles which can exert its complete or partial shadow on the solar panels, performance of solar array can be affected. It can be investigated that the *P-V* characteristic curve varies under different atmospheric conditions and changing number of shaded modules of the solar photovoltaic string. Overheating of shaded cells is the major effect caused by partial shading of the photovoltaic module. It leads to the reduction of energy of the entire solar module. Here we are studying

S. Sinha · P. Agarwal · N. K. Gupta
AKTU, Lucknow, India
e-mail: salonisinha21095@gmail.com

P. Agarwal
e-mail: piyush.agarwal@iilmcet.ac.in

N. K. Gupta
e-mail: guptanitinmiet@gmail.com

M. Asim
Department of Electrical Engineering, Integral University, Lucknow, India
e-mail: asimamu@gmail.com

A. Riyaz (✉)
Department of Electrical Engineering, BGSB University, Rajouri, India
e-mail: ahmedriyaz@bgsbu.ac.in

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the harmful effects and variations caused by partial shading on the overall solar photovoltaic module's performance. PSPICE and MATLAB are types of simulation models to test the performance of PV module and to present the result.

Keywords Photovoltaic · Solar energy · Maximum power point tracking (MPPT) · P-V characteristics · Array configuration · Partial shading

1 Introduction

Energy extracted from natural resources like sunlight, wind, tide, rain and geothermal heat is basically renewable energy or nonconventional energy and this renewable energy is naturally available in environments. Shortage of availability of fossil fuel and natural gases has provided a renewed impetus to the growth and development of clean and renewable energy sources. All across the globe a mechanism called "Clean development mechanism (CDM)" is being adopted by various organizations. There is another factor in the world apart from the rapidly decreasing reverse of fossil fuels is the pollution associated with their combustion. In contrastto it, renewable energy sources are known to be much cleaner and produce energy without the harmful effect of pollution, unlike conventional energy resources. With the increasing demand for nonconventional energy sources, several power-generating units and stations such as power plants and stand-alone systems use the photovoltaic installation for the generation as well as the distribution of the power for the various purposes. While in series-connected photovoltaic module, if the solar cells are not fully illuminated the overall performance is adversely affected. As a result of this, the output characteristics of solar module get more complicated because of the non-uniform power capturing. There are few cells under shaded condition but in spite of this there should be the same current flowing in all the cells of series array is required. But by the rule, the shaded cells produced the less photon current. The shaded cells acting like a load and start draining the power which is normally generated by cells that are fully illuminated as the cells under shade may get reversed biased. This reversed biased system creates a hotspot problem and it may irreversibly damage the complete system if proper protection is not provided. From the past many years some researcher has worked on studies about the various characteristics of the solar PV module and also about those factors which can effects their output characteristics.

We can consider the theories and outcomes of some of these researchers. Walker has proposed a model on the basic of MATLAB to properly simulate the features of solar photovoltaic module and to study the effects of variation in temperature, load variation in insolation on the output power of the module. Though, the effect of shading on the PV characteristics is not considered by this model.

2 Overview of Different Types of Solar Photovoltaic Module Array (SPVA) Configuration

There are various types of solar photovoltaic array (SPVF) configurations shown in Fig. 1. Basically, the different configuration indicated the various types of connection of the solar photovoltaic cells either it is series or in parallel connection [1–3]. The way in which all photovoltaic modules are connected to each other is called the different combinations of the solar photovoltaic array configuration. There are different types of array configurations like series combination, parallel combination, series-parallel combination (SP), total cross-tied combination (TCT), bridge-linked combination (BL), and honey-comb combination (HC) configurations.

Series and parallel combination configurations are common as well as widely used configurations. But the output current and voltage value obtained is very low in such a configuration. In series-parallel (SP) configuration initially, solar module is series connected to obtain the desired amount of voltage, and finally all the modules which have a connection in form of series are again connected in parallel. TCT configuration is obtained from SP configuration and finally a tie established to the junction across the row. Equal voltages obtained across the ties, sum of current across the various ties remains equal and the obtained power is in the series-parallel configuration.

During BL configuration bridge rectifier configuration is used to connect all the modules. As we know the four diodes constitute a bridge in a rectifier. Thus, here in the same form, four modules are connected together to form a bridge configuration. Pair of modules in bridge forms series connection and other pair are connected in parallel while ties are present in between the bridge. The calculation of current and voltage will be obtained as accurate by adding voltage in series connection and current in parallel connection. There is also one another configuration obtained by adding some modifications in the BL configuration called HC configuration. The HC configuration has the combination of advantages of both TCT and BL configuration.

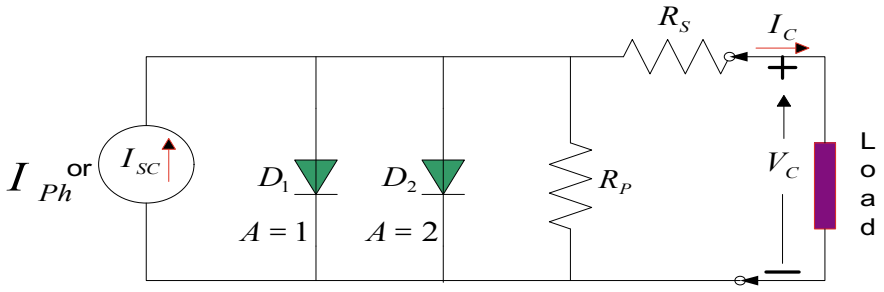

Fig. 1 Solar photovoltaic circuit diagram

3 Performance Characteristics of Solar Photovoltaic System Under Different Atmospheric Condition

P-V characteristics of solar PV cells shown in Fig. 2 demonstrate the different amount of electrical power obtained by the photovoltaic module at different voltages.

Multiple photovoltaic modules are connected in series to form a string so that the required amount of voltage and power output can be obtained. During uniform irradiance condition the solar photovoltaic strings exhibit the same *P-V* characteristic as shown in Fig. 2 that have only one peak and this peak shows the maximum power point of the string (MPP) as is known as the global peak. But if partial shading of any objects falls on the solar photovoltaic string and the irradiance will become non-uniform the *P-V* characteristics of this solar string exhibit a different curve having more the one peak point in it due to presence of bypass diode as shown in Fig. 3. In such a condition the point associated with the highest peak denoted as the global peak while all other peaks called the local peak points.

V-I characteristics of solar photovoltaic system vary with different atmospheric conditions and with different numbers of module under shaded conditions. Figures 4 and 5 shows the *V-I* characteristics with uniform and non-uniform solar irradiance, respectively.

Nowadays at various power-generated industries, the solar photovoltaic array install on the roof of building itself, thus in such a case it will become more difficult to ignore the effects of shades as the shade of building will definitely fall on to the solar panel throughout the day and in every season. Thus, these shadows decrease the level of overall power generated by the solar cells. Now to solve this problem and to obtain the desired amount of electrical power a large number of solar modules will be required but it led to the higher cost of the installation and because of the higher

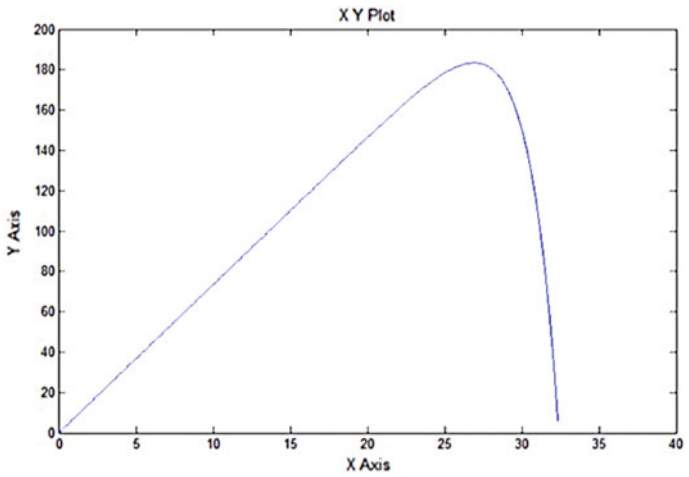

Fig. 2 *P-V* characteristics of solar array with uniform irradiance

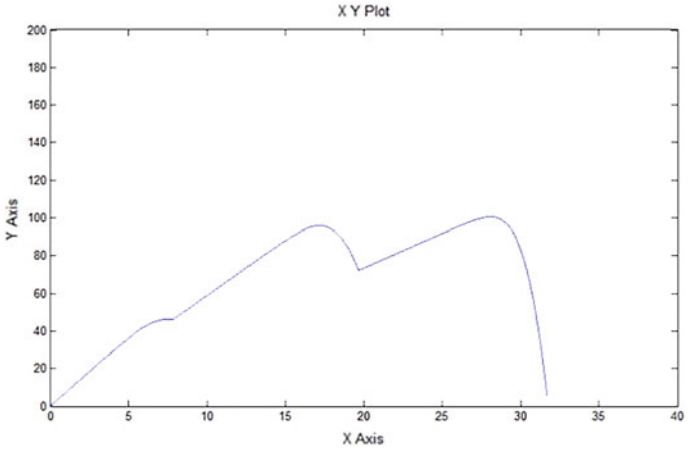

Fig. 3 *P-V* characteristics of solar array with non-uniform irradiance (shading effect)

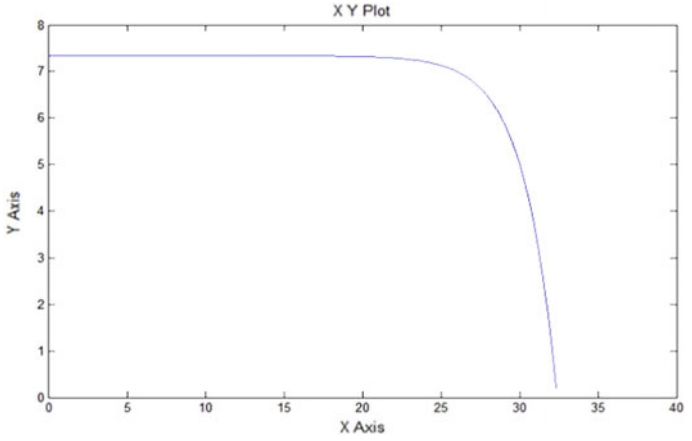

Fig. 4 *V-I* characteristics of solar array with uniform irradiance

installation cost solar photovoltaic module will become useless as compared to initial situation. This is the reason why the impact of partial shading has been discussed in recent years. The study of partial shading involves the various time-consuming and cost-effective procedure and became very complex such as it required appropriate whether condition, field testing is very costly as well as time-consuming [4–6]. One the other hand the numbers of shaded and illuminated cells are keeping on changing during the whole experiments. Thus, to obtain the accurate and appropriate result it is better and more convenient that the study would be carried out on some simulation model with the help of a computer.

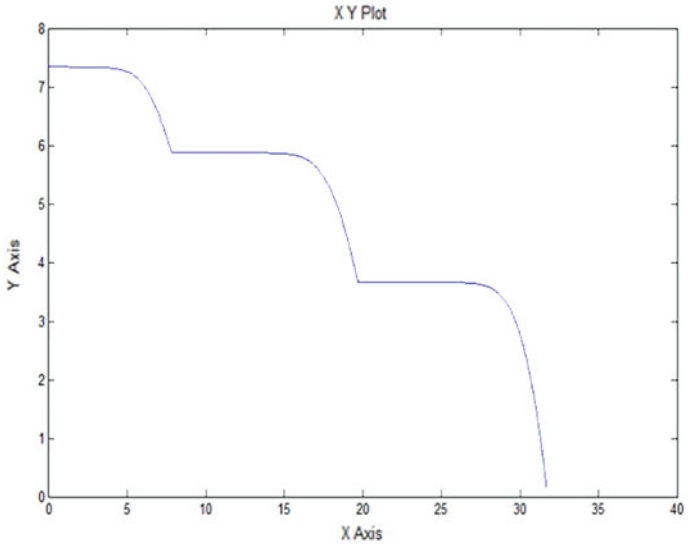

Fig. 5 *V-I* characteristics of solar array with non-uniform irradiance (shading effect)

4 PSpice Equivalent Circuit for Solar Photovoltaic Module

A PSPICE model is well designed to study the solar PV module having 36 cells series connection. By varying the quantity of cells in this PV module we can observe the variation in the output power and efficiency of the module and the stresses on the various shaded cells due to different illumination levels.

The circuit diagram shown in Fig. 1 is used for simulation model using PSPICE software. This is a one diode circuit for solar cell configuration. There are two diodes, a current source, a parallel and a series resistance. Photocurrent IP generated by the current source varies with proportionality to the density of the solar radiation incident on the panel surface and the surrounding temperature.

Through load I current is flowing which is given by the following equation.

$$I = I_L - I_o\left\{\exp\left(\frac{V + IR_{\text{se}}}{V_t}\right) - 1\right\} - \frac{(V + IR_{\text{se}})}{R_{\text{sh}}} \tag{1}$$

The above circuit is showing the PSPICE simulation software. Electronics load creates the practical characteristics which are valid for the PSPICE software. If the energy of photon of light incident on the surface of the photovoltaic cells is greater than the bandgap energy then the flow of emitted electron creates current [7–9]. However, there is a big difference between photovoltaic cell and the photodiode, in photodiode the light falls on the *p*-channel of the semiconductor junction and current or voltage signals generated due to that light but a photovoltaic cell is always forward biased. Usually a number of PV modules arranged in both the series and

Table 1 Technical specification of the solar cell and solar module used

S.No.	Parameters	Single cell	Module
1	Rated power (W)	1.03	37.08
2	Voltage at maximum power (V_{mp}) (V)	0.46	16.56
3	Current at maximum power (I_{mp}) (A)	2.25	2.25
4	Open circuit voltage (V_{oc}) (V)	0.56	21.24
5	Short circuit current (I_{sc}) (A)	2.55	2.55

parallel combination to meet the requirements. PV modules of commercial sizes generally range from 60 to 170 W is available. Series combinations are required to increase the voltage of module whereas the parallel combinations are required to increase the current in the array [8, 9].

For PSPICE software the following parameters like shunt and series resistance (Rse and Rsh), diode reverse saturation current (Io), diode ideality factor (n), should match to that of the PSPICE model. We can take an example of Solkar Model 3712/0507 having 36 cells connect to each other in series. The solar photovoltaic module under the study has various specifications which are provided in Table 1.

Here we can say all 36 cells have same characteristics for the accuracy of result few parameters like temperature difference between the shaded and un-shaded cells and the reverse breakdown strength of the shaded cells can be neglected. For any given value of F i.e. the ratio of absorbed photon current generated by shaded cells and that of fully illuminated cells, the value of R_{se} and R_{sh}, i.e. series and shunt resistance is assumed to be the same. These assumptions will not affect the conclusion obtained.

Most of the time the shaded cells get reversed biased and the problem becomes more serious as well as dangerous. Let us consider an example when the two group of cells one is fully illuminated and the second that has shading illumination are connected in series. The photon absorption current under fully illuminated cells and the shaded cells are I_{Li} and I_{Si}, respectively. Since, there are only few cells which have shading illumination thus the value of I_{Li} is higher than that of the I_{Si}. If the total output current of the module, i.e. I is less than $I_{Li}(I < I_{Li})$ the junction diode D_s is in forward biased and the chance of risk due to shaded illuminated cells are totally eliminated. But if the value of total output current of the module is greater than that of $I_{Li}(I > I_{Li})$ then the diode will be in reverse biased and the diode current $I_{Ds} = I_{Li} - I$ flow in the reversed direction through the diode. Thus, the reversed biased diode D_s provides very high resistance which is enough to consume the power generated by the photovoltaic module and will eventually reduce the load current I.

5 Technologies Used to Minimize the Effects of Partial Shading

Since it's difficult to avoid the effect partial shading of photovoltaic array in the new trends because of the neighbouring buildings and trees surrounded the solar PV module everyday throughout the season. It leads to the importance of the study of the partial shading to obtain the desired sufficient output from the solar photovoltaic module. Now the question arises how can we minimize the effect of shading and obtain the desired output power even during the shaded conditions. Shortly, to get the superior performance in partial shaded condition. Since solar panel depends on the direct energy of the sun to produce power, but in many installations, some environmental factors can partially shade panel which directly or indirectly reduced the final amount of energy produced due to solar PV module.

All the solar panels are not the same, one of the technologies behind the sun power panel is Maxeon *cell technology* in which the cell is made up of Maxeon solar cells, which looks very similar but fundamentally different from the cells used in the conventional solar panels. They are made up of thick plated copper on a solid copper foundation allowing them to handle more power as well as to make them practically immune from the breaking and corrosion because the solar panels work in open area directly in contact with atmosphere and they can lose power due to atmospheric factors. Sun power Maxeon solar cells also perform differently when they are shaded, diode protection is built into each cell allowing the continuous power to be generated even in the shaded cells as compared to the conventional solar cells where a non-negligible amount of power is lost due to shaded cells. Even if the one cell is shaded the panel loses approx. 33% of the total power because there is no built-in protection in the conventional solar panels. Researchers have proved it experimentally too by taking the examples of few shading conditions for Maxeon cell and for conventional solar cells, for example, pipes, tree and shading leaves on the solar panel. As the sun moves across the sky the shadow swipes across the solar panel and the energy generated by each system is measured throughout the day. The total energy generated by each system is compared by the energy generated by the same system without shade to determine the impact of shading. The conclusion occurs that in the conventional solar panel there is a wide variation in the amount of energy generated due to shade as compared to the solar panel made up of Maxeon cells. These independent tests confirm that the sun power panels produce the most energy even in the challenging real-world condition. Sun power Maxeon technology insures that you will have an eco-friendly, low-cost energy protection.

Supercapacitors are used to reduce the effects of partial shading on the PV solar system. If we consider a solar panel having two solar modules connected in series with each other it will draw some current and voltage while they are not in shade. But if there is some partial shading occurs the current flowing through the solar panel is reduced adversely and hence the power generated by solar panel will also be reduced. To reduce the harmful effect of the shading on the PV solar system researcher used some capacitor known as supercapacitor. The shaded cells acting like the resister and

Fig. 6 Super capacitor technology to reduce the partial shading affects

consumed most of the generated power due to the rest of the illuminated solar cells thus the overall efficiency of the solar cell will be reduced as compared to the fully illuminated solar cells. The supercapacitor as shown in Fig. 3 when connected in parallel with each solar string and all the solar string is connected in series under the shaded condition all the supercapacitor will take over the resistance of each shaded solar panel and all the power will pass right through this supercapacitor to the load on which the output is desirable (Fig. 6).

6 Conclusion

The study of partial shading on the solar photovoltaic module is observed as well as concluded that there is a measurable amount of wastage of power and loss due to various types of shade fall on the surface of solar panel. Due to non-uniform illumination of the solar modules connected in series there is a risk of generation of hot spot and it may cause the system failure at an irreversible basis. Most of the power generated by the fully illuminated cells is waste due to shaded illuminated cells as these cells worked as a reversed biased and acted as the load that can able to consume maximum amount of generated power. To eliminate the power consumption on the shaded cells one should take the proper care while connected in series and make sure that the same current is flowing through the fully illuminated as well as shaded cells even under different patterns of shadings. These small cares lead to better protection of the solar photovoltaic array and also helps in the generation of a desirable amount of energy even during the shading period.

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Application of Convolutional Neural Network and Machine Learning Techniques in Brain Tumour Detection

Abhishek Das and Raka Ganguli

Abstract In the field of machine learning, deep learning has been more prominent in recent years. It is an effective machine learning tool and has wide applications. In this paper, we propose a method of applying deep learning architecture to classify brain tumours using magnetic resonance imaging (MRI) images and measure its performance. The underlying architecture for complex features is convolutional neural network, and for low-level features, we have integrated machine learning techniques, namely grey-level co-occurrence matrix and histogram of oriented gradients.

Keywords Machine learning · Brain tumour · Deep learning · Convolutional neural network · Optimization · Edge detection · Texture analysis · Feature extraction

1 Introduction

1.1 Human Brain and Brain Tumour

Brain is the coordinating centre for sensation as well as intellectual, emotional and nervous activity. A brain tumour arises when there is uncontrolled mitosis forming an abnormal group of cells inside or around the brain which can potentially disrupt the normal functionality of the brain [1]. There are various techniques used by researchers to detect brain tumours. In recent years, machine learning (ML) models have become quite prominent in image classification. More importantly, deep learning (DL) models are effective in representing complex image features [2]. Convolutional neural network is one such DL architecture that can efficiently process

A. Das
Institute of Engineering and Management, 700091 Kolkata, India
e-mail: madhurima39@gmail.com

R. Ganguli (✉)
Sudhir Chandra Sur Degree Engineering College, 700074 Kolkata, India
e-mail: raka.ganguli@gmail.com

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Fig. 1 3 different types of brain tumour

an image using hidden layers. Such ML and DL techniques have been widely implemented in the medical field to detect anomalies in the human body, thus revealing what is not visible under traditional image processing methods or to the naked eye.

1.2 Types of Tumours

Meningioma Tumour A meningioma is a tumour that forms on membranes surrounding the brain and spinal cord. Such tumours have low rate of growth and are mostly benign.

Glioma Tumour Glioma is a type of tumour that occurs in the brain and spinal cord. It forms in the gluey supportive cells also known as glial cells. The glial cell surrounds nerve cells and supports their functionality. Glioma tumours disrupt said functionality. Such tumours can be potentially fatal depending on the location and rate of growth.

Pituitary Tumour Pituitary tumours are abnormal growths that develop in the pituitary glands. Some of these tumours affect hormone secretion. Hormones regulate body functions and hence require optimum regulation. Pituitary tumours disrupt this regulation. Most of these tumours are benign (Fig. 1).

1.3 Deep Learning

Deep learning is a subset of machine learning based on learning multiple levels of representations whereby a hierarchy of features is described. The higher levels are defined from the lower levels. Unlike traditional neural networks, DL structure

includes hidden layers between input and output layers. With increased depth of the neural network, the extracted features become more complex, thus presenting a plethora of features related to the input image which are not captured through traditional image processing methods.

2 Convolutional Neural Network

2.1 What Is CNN?

Convolutional neural network (CNN) is a DL architecture used commonly in image recognition. In this technique, the input is assigned certain learnable parameters (weights and biases) and is transformed through a series of hidden layers to produce an accurate output feature map. Figure 2 illustrates a fully connected neural network with hidden layers. Convolutional neural networks are efficient in identifying complex features of the input image. The input image is converted into a 3D matrix of pixels in the input layer before fed into the CNN architecture. The CNN architecture has 3 layers. The first two layers, i.e. convolution and pooling, perform feature extraction. The input matrix multiplied with its respective weight and added with the bias is passed through an activation function in the convolution layer. The activation function is required for the sake of nonlinearity in the output function. At multiple layers, the output of the previous layer is fed as the input of the next layer. The pooling layers down-sample the feature maps. Finally, the third layer, a fully connected layer maps the extracted features into the final output.

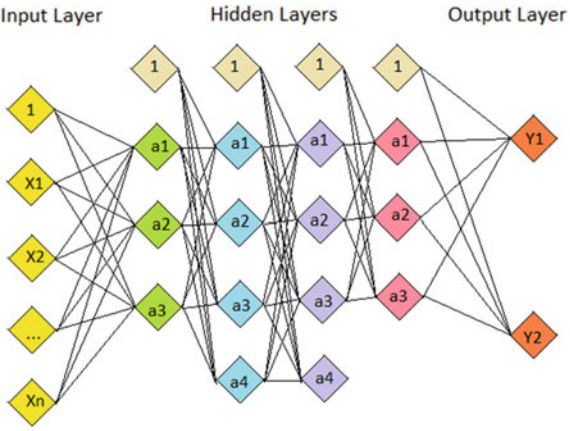

Fig. 2 A basic neural network with hidden layers

2.2 Optimization in CNN

Optimization is a crucial part in CNN where the cost function is minimized by updating the kernel weights using gradient descent and back-propagation algorithms [3]. For the output layer, the cost is basically the difference between the actual/predicted output activation and the desired output, i.e. the ground truth. It is dependent on the weights and biases for the last layer as well as the activations of the previous layer.

$$A_j^L = \sigma\left(\sum_k w_{jk}^L A_k^{L-1} + b_j^L\right) \tag{1}$$

Here, summation is done is over all neurons k in the $(L-1)$th layer. This expression can be rewritten in matrix form by defining a weight matrix w^L for each layer L. The entries of the weight matrix w^L are simply the weights connecting to the Lth layer of neurons. Simply put, the entry in the jth row and kth column can be denoted by w_{jk}^L. Similarly, for each layer L, a *bias vector* b^L can be defined. The components of the bias vector are just the values b_j^L, one component for each neuron in the Lth layer. Lastly, the activation vector A^L is defined. The components of A^L matrix are the activations A_j^L. σ stands for sigmoid function which is the activation function in this case. The equation in matrix form thus becomes

$$A^L = \sigma\left(w^L A^{L-1} + b^L\right) \tag{2}$$

Back-propagation Back-propagation has four steps, viz. the forward pass, the cost function calculation C, the backward pass, and the updation of the kernel weights and biases. The objective of back-propagation is to compute the partial derivatives $\partial C/\partial w$ and $\partial C/\partial b$ of the cost function C with respect to any weight w or bias b in the network. Here, C is the cost function which in this case has the form

$$C = \left(A^L - y\right)^2 \tag{3}$$

Differentiating w.r.t. w^L, we get

$$\begin{aligned}\frac{\partial \mathrm{C}}{\partial \mathrm{w}^{\mathrm{L}}} &= \frac{\partial \mathrm{C}}{\partial \mathrm{A}^{\mathrm{L}}} \times \frac{\partial \mathrm{A}^{\mathrm{L}}}{\partial \mathrm{z}^{\mathrm{L}}} \times \frac{\partial \mathrm{z}^{\mathrm{L}}}{\partial \mathrm{w}^{\mathrm{L}}} \\ &= 2\left(\mathrm{A}^{\mathrm{L}} - \mathrm{y}\right)\sigma'\left(\mathrm{z}^{\mathrm{L}}\right)\left(\mathrm{A}^{\mathrm{L}-1}\right)\end{aligned} \tag{4}$$

$$\frac{\partial C}{\partial A^L} = \frac{\partial C}{\partial z^{L+1}} \times \frac{\partial z^{L+1}}{\partial A^L} \tag{5}$$

If $\partial C/\partial z^L$ is considered as the error signal for layer L, then in order to calculate it, the error signal for the $(L + 1)$th layer has to be calculated first. Thus, it is calculated recursively layer by layer and this method is called back-propagation. Similarly, the derivative of the cost with respect to the bias is the error signal itself.

$$\frac{\partial C}{\partial b^L} = \frac{\partial C}{\partial z^L} \times \frac{\partial z^L}{\partial b^L} \tag{6}$$

Gradient Descent The weights are updated using gradient descent after the error signal of each neuron is calculated. The gradient of the cost function is calculated iteratively. After each iteration, a step is taken proportional to the negative of the gradient and the weight (w); i.e., the learnable parameter is updated. The purpose is to converge towards the minimum where the optimal weight lies. Mathematically, the gradient is defined as follows.

$$w = w - \eta \frac{\partial C}{\partial w} \tag{7}$$

Here, w stands for each learnable parameter, i.e. the kernel weight, η stands for a learning rate, and C stands for the cost function. The learning rate is basically the step size. The higher the step size the quicker the chances are to reach the minimum; however, there is a risk of overshooting the minima in an attempt to cover greater area in each step. Hence, despite the process being relatively more time-consuming, a low step size is preferred where it is possible to gradually move along the negative slope and reach closer to the minima, thus obtaining greater accuracy. This is the gradient descent technique.

Feature Extraction Using CNN The CNN architecture can be trained using data and ground truth labels and then tested on patient images. Preprocessing techniques are applied to the raw data to remove the distortions and noise. Removal of the noise enhances the overall quality of the image. The unwanted characteristics are suppressed, and the important features are described by augmenting the data set before it is fed to the CNN. The input is then convolved using kernels to produce feature maps. The convolution neural network consists of input layer, convolution layer, activation layer, pooling layer, and fully connected layer [4–7]. The activation function is used to introduce nonlinearity. The activation layer consists of the activation function. A commonly used activation function is the sigmoid function. Another such activation function is the rectified linear unit (ReLU). The pooling layer downsamples the feature maps and creates a summarized version of the features excluding the elements that are not required. Thus, computation is reduced. Pooling techniques like max pooling or average pooling can be applied to filter the feature map and reduce its spatial size. The fully connected layer in the end takes the output of the preceding layer as its input and produces an N-dimensional vector as output. N represents the number of available options that can be chosen from while giving the final output

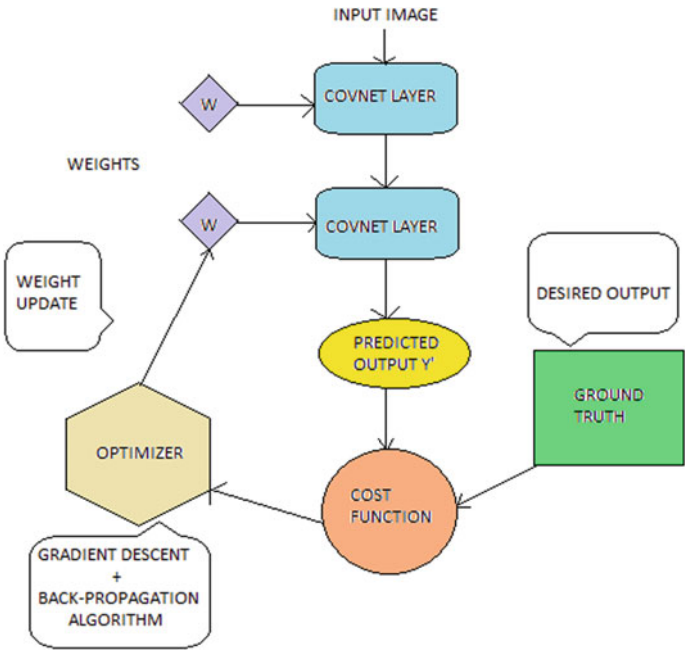

Fig. 3 Block diagram of the CNN classifier proposed for tumour detection

result. The cost function calculation is important to improve accuracy by updating the kernel weights using gradient descent and back-propagation algorithms. The cost can be minimized, thus optimizing the functionality of the CNN. Finally, the CNN is ready for test data and the output can be compared with the ground truth to demonstrate how accurate the CNN architecture is; Fig. 3 illustrates the block diagram for the methodology used to classify brain tumours using CNN [8].

3 Histogram of Oriented Gradients

3.1 Edge Detection Using HOG

HOG technique [9] uses the gradients (direction and magnitude) arranged in histograms over a particular domain, thus defining a feature. Gradients, mathematically defined as the derivatives, are useful because the magnitude of gradients is large around the edges and corners which are the regions of abrupt change and hence contain significant information about the object shape. HOG is an effective edge detection technique.

Calculating the Gradient Vector In order to calculate the HOG, the first step is to determine the vertical and horizontal gradients which can be done by filtering the input image using the following kernels

For gradient along the X-axis, the kernel used is $[-1, 0, +1]$
For gradient along the Y-axis, the kernel used is $[-1, 0, +1]^T$

For a function $f(x, y)$, the gradient is given by g_x and g_y, for the X- and Y-axis, respectively. This gradient is basically the change in pixel size between two adjacent cells of the image. The gradients are vectors and have a direction. For a particular cell, there are two mutually perpendicular gradients along X- and Y-axis. The resultant gradient is calculated by vector addition. The magnitude is given by

$$g = \sqrt{g_x^2 + g_y^2} \tag{8}$$

The direction of the gradient vector is given by

$$\theta = \tan^{-1} \frac{g_y}{g_x} \tag{9}$$

The magnitude of the gradient fires wherever there is an abrupt change in intensity. At every pixel, the gradient has a magnitude and direction. The gradient vectors are mapped for each pixel on the image patch.

Steps to Obtain the HOG The image is divided into 8×8 cells, and the gradient is computed (magnitude and direction) for each cell in the image patch. For each 8×8 patch, there are 64 such gradient vectors. A histogram is created for the generated gradient vectors in the form of an array of angular bins. Each bin represents the gradient direction over a range of 20°. So over the range 0–180°, there are in total 9 bins. The values are thus down-sampled from 64 to 9. This histogram is known as the feature vector of size 9, also represented as a 9×1 matrix. Figure 4 illustrates the block diagram of an 8×8 cell where the colour in each cell represents the range which the angle of the gradient vector falls under. The colour is hence representative of the angular bin. Figure 5 represents the histogram that has been generated by taking the angular bins as the class and the number of gradient vectors in each angular bin as the corresponding frequency.

Normalization Image gradients are sensitive to contrast and illumination. Multiplying or dividing the pixel values by a common factor automatically changes the gradient by the same factor. In order to remove such variations, the histogram needs to be normalized. This is done over a 16×16 block consisting of 4 histograms of size 9×1 that are concatenated to form a 36×1 element vector.

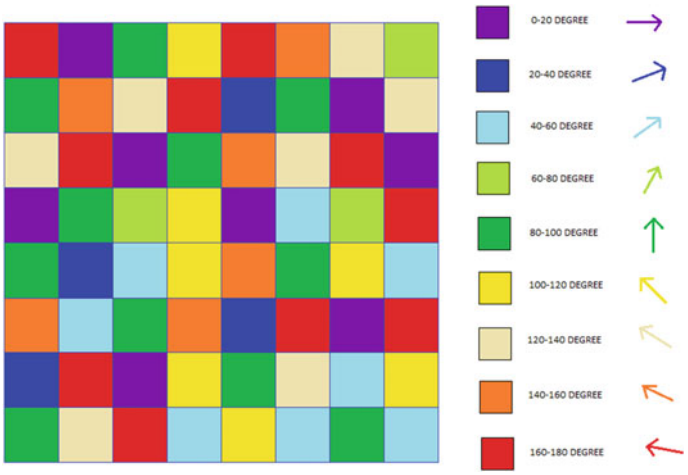

Fig. 4 An 8 × 8 image patch consisting of 64 cells and their respective angular bin

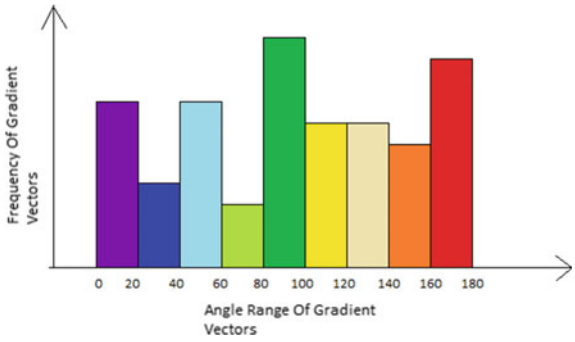

Fig. 5 Histogram generated from the gradient vectors and their angular bins

4 Grey-Level Co-occurrence Matrix

4.1 Texture Analysis Using GLCM

GLCM is a well-known statistical method of examining texture that takes into account the spatial relationship of pixels [10]. A co-occurrence matrix over an image is described by the distribution of relative frequencies of grayscale tones between adjacent pixels at a given offset. These relative frequencies are also known as co-occurrence values. For an image I of size N × M, the co-occurrence matrix P can be defined as

$$P(i,j) = \sum_{x=1}^{N} \sum_{y=1}^{M} 1, \quad \text{if } I(x,y) = i \ \& \ I(x+\Delta x, y+\Delta y) = j \qquad (10)$$

$$P(i, j) = \sum_{x=1}^{N} \sum_{y=1}^{M} 0, \quad \text{otherwise} \tag{11}$$

Here, i and j are pixel values, and x and y are the spatial positions in the image I. The offset $(\Delta x, \Delta y)$ describes the distance between the concerned pixel and its adjacent pixel. $I(x, y)$ indicates the pixel value at the pixel (x, y). The means and variances are calculated for P_x and P_y. The co-occurrence matrix is useful in statistically calculating features like contrast, shade, correlation, entropy, etc. The underlying concept is to convert the image into grayscale to represent the intensity carried by each pixel. The contrast ranges from black to white with different shades of grey in between, thus creating a monochrome where only the information of the intensity can be obtained. The relative intensity and its frequency of occurrence between adjacent pixels is what presents an idea of the overall texture of the image.

5 Discussion

This method is yet to be applied practically. The technique is novel in the sense it integrates various architectures to bring out a comparison between the different feature maps extracted due to the different techniques, i.e. HOG, GLCM, and CNN. The algorithm can be implemented in Keras Python library. We are currently working on potential modifications that can be theoretically applied to optimize the performance. Machine learning and deep learning techniques can efficiently describe an image in its minute detail. The objective is to detect several features that potentially cause tumour in brain which are often masked by the traditional image processing techniques.

6 Conclusion

In this theoretical paper, a method of tumour detection based on deep learning architecture has been proposed. The texture-based features can be extracted using grey level co-occurrence matrix (GLCM). For classification purpose and edge detection, histogram of oriented gradient can be implemented. Integrating HOG and GLCM techniques, a combination of shape-, margin-, and texture-based features can be segmented. The more complex features can be extracted using CNN. The aim is to transform the input data into a set of features, and this is called feature extraction. The CNN can be trained by updating the learnable parameters. This concept can be implemented in various medical fields, replacing the traditional methods. CNN architectures are flexible and their applications are ever increasing, even beyond the field of medical science. The level of accuracy can be improved through various optimization techniques, thus making the CNN architecture evolve.

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Upshot of Blockchain Technology: A Study

Adusumilli Taraka Venkata Satya Sai Rohit, B. Padmaja, Y. Mohana Roopa, and E. Krishna Rao Patro

Abstract The blockchain technology is at a stage where its threshold capabilities have not yet been recognized. Various technologies emerge as the technological era progresses but one technology that is at its core roots and has the potential to disrupt many industries is blockchain. This technology has the potential to create an unimaginable difference in our lives. The blockchain technology is the answer and various questions can be framed across it. It has the potential to change the way the centralized systems work and can lead to an unimaginable futuristic technological advancement.

Keywords Blockchain · Centralization · Ethereum · Peer-to-peer · Consensus · Node

1 Introduction

The blockchain technology has been the backend technology behind the much famous bitcoin cryptocurrency. While in the recent decade, the actual advantages and use cases of this blockchain technology came into foresight. This technology is an answer to many questions and problems we are facing in this world of the internet. The internet was a revolution and it solved the major problem we couldn't even imagine. It has grown into a massive network of authorities and gave rise to emerging tech giants like Google, Facebook, Amazon and many other e-commerce and centralized

A. T. V. S. S. Rohit (✉) · B. Padmaja · Y. Mohana Roopa · E. Krishna Rao Patro
Department of Computer Science and Engineering, Institute of Aeronautical Engineering, Hyderabad, Telangana, India
e-mail: arohit5636@gmail.com

B. Padmaja
e-mail: b.padmaja@gmail.com

Y. Mohana Roopa
e-mail: ymohanaroopa@gmail.com

E. Krishna Rao Patro
e-mail: patrosir@gmail.com

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sectors. The security of blockchain is well balanced by cryptographic functions. Therefore, the issues of security of blockchain are minimum. But the internet did not solve two major problems which were supposed to be solved by it, they are trust and intermediation problem. Blockchain was initially the technology that is behind the bitcoin cryptocurrency. Later it was observed that this can be used more than just offering cryptocurrency services. It can solve the problem of trust and intermediation. Blockchain is a combination of a collection of various distributed ledgers called nodes that record various transactions and data flow in them. This decentralized platform is the forefront of disrupting many industries out there and has a humongous scope of emerging into a new technological revolution in the coming by years. This decentralized platform can solve many issues and can preserve the trust, assets and values of users with themselves, unlike the centralized sectors which impeccably use our data and turning it into their business model. Its decentralization helps in the depletion of centralized and intermediate bodies and authorities. Its principles of consensus also promise to provide security. It is deeply encrypted using secure hash algorithms and consensus algorithms [1]. It can allow us to create value, trust and truth with clever use of distributed ledger, cryptography and computation. This ultimately leads to a new possibility of a new decentralized world where users of the third-party can be empowered without beholden to third-party power brokers. In this paper, the impacts of blockchain technology, its basic revenue generation models and its collaboration impacts with different sectors are discussed. In Sect. 2. related work is discussed followed by Sect. 3 that discusses the working methodology of blockchain technology. In Sect. 4, the impact of blockchain technology in various sectors is highlighted. Section 5 discusses the future scope and implications of this technology. Finally, in Sect. 6 conclusion and applications of blockchain technology are discussed.

2 Related Work

Blockchain is still in its initial stages. Many sectors are still predicting the future. According to Jesse et al. [2], even though blockchain appears to be a suitable solution for ongoing transactions using cryptocurrencies, it has still some technical challenges and limitations that need to be studied and addressed. High integrity of transactions and security, as well as privacy of nodes, is needed to prevent attacks and attempts to disturb transactions in blockchain. In addition, confirming transactions in the blockchain requires computational power [2]. Victoria L Lemieux further addresses transactional, financial and medical record-keeping using blockchain technology which is even in its initial stages of the development. He believed and proposed that this technology can change the future of these sectors [3]. Roman Beck et al. further illustrated that as it is used today, it is a tamper-resistant database of transactions consisting across a large number of nodes [4]. So, his study with similar to the above-mentioned works dives into various sectors with which blockchain can integrate and produce some progressive results and statistics for that particular application.

3 Working Methodology

3.1 Emergence of Blockchain Technology

It all started with the emergence of bitcoin a decentralized cryptocurrency introduced by Satoshi Nakamoto in his whitepaper in 2009. Even though bitcoin was announced in 2009, various technologies that support it have already been invented or were in existence since 1991 itself and various researchers contributed to those technologies. Stuart Haber and W. Scott worked on cryptographically securing of information. But these measures had a lot of complications. In 1993, proof of work algorithm was introduced to countermeasure the implications and paying a way for secure consensus of information. After bitcoin which is a peer-to-peer electronic cash system was introduced later the true power of the underlying technology blockchain is recognized. In 2014, Ethereum blockchain was created which supports not only currency transfers but also a new virtual compilation of smart contracts, a new way of decentralized supercomputing across the network which has great possibilities to enter and change the functioning of many industries and sectors [5]. It was 2015 when bitcoin finally emerged as a successful cryptocurrency holding a major share. During 2016–2017, the blockchain emerged as a futuristic technology. Today we can visualize the near decentralized future and the designs of the applications towards meeting that goal [2].

3.2 Introduction to Blockchain Technology

Blockchain is a collection of various peers typically called as nodes in a decentralized manner [6]. It is the latest form of database and virtual computing system but in a decentralized manner. It is very much secure as it uses the best underlying technologies of consensus, cryptography and hashing. But this is not just a computing phenomenon. Decentralized applications are going to enable a decentralization trend at the societal, legal, governance and business levels because everything is being decentralized. So, let's get ready to understand blockchain concepts. The information on the blockchain can be cryptographically secured. This distributed network of nodes has greater potential and has a wide range of applications in dealing with storage, traversal and state changes. The nodes have various components such as previous hash number, a record of transactions and nonce which is just an additional value that is changed constantly to match up the hashing values. The transactions are recorded in a block and these blocks are added to the chain of blocks. But the blocks can't be simply added to the chain. For a block to be added it should be verified valid first. This task is done by a special set of nodes or peers called miners. They use huge computing power to reach a consensus state. Finally, after verifying that the block is a valid one they add it to the copy of the network and broadcasts it. Various miners compete to add the block but only those get a chance who solves a computational

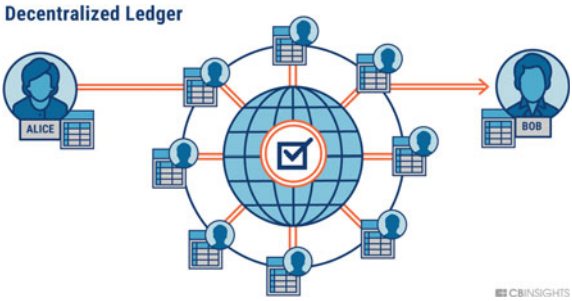

Fig. 1 A simple model of blockchain technology

problem according to various consensus algorithms. Blockchain now is in its early stages like the internet in the 1990s. The true potential unlocks as the years pass on and research goes on. Many major sectors, private and public companies have already started researching how blockchain can advance their business models and so on. IBM's 'HyperLedger' project is one of the biggest consortia of companies dedicated to the development of blockchains to meet the needs of individual sectors [7]. Ethereum is one of the most famous public blockchains which has the great additional functionality of not just dealing with cryptocurrency trade but also it acts as a virtual computer which executes simple logics known as smart contracts on the distributed network of nodes which allows the data to flow in a desired way and change to the desired state. As one can see how this technology can help the way things work in our centralized, trustless based world of the internet era [4] (Fig. 1).

3.3 Consensus and Types of Blockchains

The consensus is a phenomenon where the addition of a new block that is the set of transactions or data flow is verified by specific methodologies probably by using various consensus algorithms available like proof of work or proof of stake [8]. Consensus protects the privacy and user rights and its main contribution is its trust. The main consensus is achieved which is the main purpose of blockchain which is built upon the layers of trust and security. The main consensus algorithms include proof of work, proof of stake and proof of authority [9]. The various types of blockchains are available to cater to various business and application related goals. There are public blockchains, private blockchains and consortium or shared blockchains. The bitcoin and Ethereum blockchains are examples of public blockchains [10]. In a public blockchain, anyone can download the software and create a node while consortium blockchain allows only certain users to be nodes. Technically speaking both private and consortium blockchains are permission oriented blockchains since they both require permission to access them. However, the main difference between blockchain network and the traditional database-oriented network is that the blockchain has built-in benefits of cryptographic auditability and

Fig. 2 Working of smart contract on Ethereum blockchain

more immutability whereas in databases, the data can be added, removed and modified and is not necessarily traceable. Even blockchains can interact with each other known as blockchain interoperability which supports the concept of the futuristic revolution of web 3.o (Fig. 2).

4 Impact of Centralized Monetary Sectors

4.1 Problems of the Internet in the Centralized Sectors

Blockchain was early similar to the internet in the 1990s. It is not a use case of the internet but a fundamental core technology which has its unimaginable use cases. The internet was supposed to solve two major problems prevailing at those times and to make efficient the systematic flow. The two problems are trust and intermediation. The trust problems are not at all solved whereas intermediation has risen to heaps and bounds to a large extent. These intermediate companies are trying to offer us services but they are the ones who take greater advantage of profits and revenue generation models whereas clients and service providers are not capable of gaining much in this scenario. The biggest e-commerce service providers act as intermediaries between B2B models and B2C models. Social media platforms like Face book and Google offer free services but without any concern steal our data and make huge revenue generation models with them. Here the trust is completely lost and the matter of privacy is not at all present and is completely vanished. Next comes trust. In this centralized world, trust has completely lost its importance and meaning. Institutions have used centralized authority to obtain power and create a monopoly for themselves. Wherever we see, there is a lot of fake news, fake profiles, fake invoices,

fake offers, fake incentives. Everything is being polluted in a centralized space. Of course, it has solved a lot of never imaginable problems and paved the way to a global technological revolution, every time there is a need for a new technological revolution and blockchain is one among them. Blockchain which is a decentralized platform offers the core values of trust, security and privacy with its integrated cryptography algorithms and hash functions along with the consensus [11]. It has the potential to solve the problems which were not able to be solved by the internet and its centralized authorities and companies. One of the imaginable impacts of blockchain can be on the government. Now, individuals can have full control over their data, assets and reputation. A blockchain between government and its tender undertaken companies can ensure the successful completion of the project without any scams and issues as it is completely decentralized and various nodes can monitor the flow. It's impossible to modify the data flow or the status of the workflow thereby assuring the security and strong trust issues.

4.2 Implication of Blockchain on Traditional Business

The current business market uses large databases to store various kinds of data and server end applications. They are deployed at the central server and offer various services acting as intermediaries. But centralized platforms are under one's control and monetary models are owned by one. Furthermore, it can present the problems of trust and security issues as discussed. Therefore, many businesses are now looking towards blockchain technology to overcome challenges they are currently faced with centralized databases. The blockchain network is transparent and verifiable. It also improves the accuracy, efficiency and transaction speed, minimizing disputes and the need for intermediaries. Many use cases are being effective in terms of fleet management and supply chain management and tracking which is laying a perfect foundation for business-oriented operations. The ownership of medical records is being stored on a blockchain [3]. Another field that blockchain can disrupt is the music industry. Music ownership and distribution where music creators are directly benefited. Blockchain also plays a major role in a machine to machine communication in IoT which promises an interesting future ahead [12]. Finally the integration of blockchain technology with other emerging technologies such as Internet of things, artificial intelligence promises a great future. Artificial intelligence can majorly be benefited by this because the true and trusted data sets are available due to the core values offered by the blockchain technology.

However, blockchain is not the solution to every possible problem and business out there. The various factors one needs to consider before deploying this technology are:

- Are there multiple interactions between many entities?
- Does the business rely on intermediaries?
- Is there any trust issue in the business model?

- Are there any assets or data that need provenance in tracking?
- What part of the business can be automated and put into a smart contract?

4.3 Tokenized Ownership, Ico and Revenue Model of Deploying Blockchain

This technology uses tokenized ownership as its business model [13]. That is the creator of a decentralized application can initially create some tokens and raise funds to develop the project furthermore. The tokens are required by the entities to view the content or to deploy a smart contract using ether which is the cryptocurrency of Ethereum blockchain. The value of tokens can keep on increasing as the product or project develops. Another way of increasing the revenue or offer services is initial coin offerings (ICO). It is similar to the general public shares offered by a company in the business world. Though cryptocurrency is banned in several countries, other forms of revenue generation models can be invented. Blockchain makes things transparent, democratic, decentralized, efficient and secure.

5 Future Scope and Implications

5.1 Applications of Blockchain Technology

Everything in this world is built from scratch. The future belongs to those who build it. Therefore, this technology is in its beginning stages and yet to be built-in the nearby future. Various advantages are offered by this wonderful technology.

- **Banking and Payments**: To facilitate the banking functionalities in a decentralized way.
- **Cyber Security**: To ensure trust and privacy [14].
- **Supply chain management**: To ensure that the supply goes on smoothly with perfectly recorded transactions [15].
- **Networking and IoT**: To connect various devices and record data flow [16].
- **Insurance**: This technology can change the way insurance policies can function without any middlemen securing trust [17].
- **Private transport and Cab sharing**: Blockchain can be used to create decentralized peer-to-peer ride sharing apps allowing both driver and customers to set terms privately without any third-party customers [18].
- **Cloud storage**: Data is stored on multiple computers or servers with mixed layers of security and trust [19].
- **Charity**: One of the biggest applications which can be beneficial to large people in charity. This ensures trust and no middlemen can steal or loot the money thereby reducing scams.

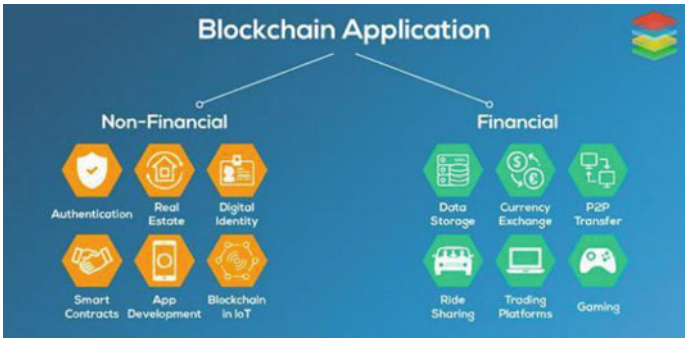

Fig. 3 Working of smart contract on Ethereum blockchain

- **Voting**: Voting is another sector in which we can apply this technology. It ensures secure voting and permanent record of it. Therefore, no chance for electronic fraud or vote-rigging [20].
- **Government**: The main factor required is a trust which can be ensured. It can even allow local governments to work effectively and bridges a perfect way among various government bodies from central to the state level. It allows collaboration of untrustful parties in a business to ensure the perfect execution of project tenders, business goals and stake holdings.
- **Healthcare**: Use to store medical records of various patients [21].
- **Energy Management**: Management of energy in an efficient way to facilitate low energy areas [22].
- **Online music**: Blockchain startups are coming up with ways for musicians to get paid directly from their fans.
- **Retail**: Connecting buyers and sellers. In this case, trust comes from smart contract system.

  Crowdfunding: Trust is created using smart contracts [23] (Fig. 3).

5.2 Drawbacks of Blockchain Technology

As with every technology, blockchain has some drawbacks. Blockchain is a complex technology consisting of complex topics that include consensus, chains, nodes and miners. All these things create confusion initially when you start working on it. Public blockchains like bitcoin processing speed are too low when compared to other centralized operators. Even the wastage of resources is another major problem. The data is not permanent, if you own more than 51% of nodes then you can tamper with the blockchain which is not usually possible with public blockchains but there's a chance with private blockchains [24]. The blockchain is at an evolving stage. Though

there are some lags and drawbacks there is a huge possibility for its development in the coming future.

5.3 Current State of Blokchain Technology

Blockchain is in its initial stages. Many industries, private organizations, public organizations have already started investing and research of blockchain. Many wonderful startups are being created. The Hyperledger is another biggest world project which is a consortium of various major companies. It is working on how to apply blockchains to solve their application related problem and change the way their business function. Another biggest advantage is the future development of web 3.o. The problem with the internet is that we are looking for products or applications but instead, you are becoming a product who gets a good market value and sold to different financial institutions to get monetized. This web 3.o is being built using blockchain protocols. So, it's time to dive in and believe decentralized future ahead.

6 Conclusion

This technology has been observed in many ways in which it can disrupt many industries with its true potential of decentralization, cryptography measures and consensus techniques. Though blockchain is in its initial stages, it has a larger future prospective and can emerge as a truly decentralized technology that supports the vision of web 3.o. This technology can be applied to various use cases and some emerging outcomes in various fields of medical, business, government, private or public market places can be obtained. The industries will be hugely benefited by using this technology. Now as we waited for the outcomes of the internet in the past when it was released in the 1990s, now it's time to wait and see how this technology will evolve and can cope up with different other fields out there in the massive world of everlasting technology. Therefore, we have seen the different aspects and have dive into many of its ongoing and futuristic applications in various fields. So, let's believe that the decentralized future is going to play a key role in many aspects and this technology answers it.

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Indium Phosphide Based Dual Gate High Electron Mobility Transistor

Shashank Kumar Dubey and Aminul Islam

Abstract In this paper, the performance of cubic InP/$In_yGa_{1-y}As$ DG MOS-HEMTs, has been discerned by studying the gate geometries' effects on the breakdown voltage, subthreshold slope and maximum cut-off frequency owing to varying doping concentrations. After a meticulous simulation, the breakdown voltage was found out to be 1417 V. The proposed InP/InGaAs based HEMT exhibits subthreshold slope of 63.9 mV/decade. The unity gain frequency (f_t) is found to be 113 GHz and is constant for 1 V < V_{ds} < 2.5 V, while maximum frequency f_{max} = 216 GHz for V_{ds} = 7 V. To explore the reliability of the device under high gate and drain bias conditions, a profound study has been carried out.

Keywords InP/InGaAs · HEMT · Breakdown voltage · Subthreshold slope · Cut-off frequency (f_t) · Maximum frequency (f_{max}) · Transconductance

1 Introduction

HEMT has wide applications in high-speed low noise amplifiers, high-frequency and power electronics applications, and high bit rate communication [1]. HEMT exhibits excellent performance characteristics that can operate in the high-frequency range. In order to improve the range of operating frequency, a double-gate HEMT (DGHEMT) is designed with two gates on either side, thus improvising amount of current flow. Compared to single gate HEMT, a DGHEMT exhibits good pinch-off behavior and high transconductance. Due to its excellent microwave and noise performance, DGHEMT is used in low noise microwave amplifier design [2]. InP/InGaAs HEMT provides excellent performance in microwave frequency ranges and manifests a cut-off frequency of around 100 GHz [3]. The low noise figures, high mobility

S. K. Dubey (✉) · A. Islam
Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra, Ranchi, Jharkhand, India
e-mail: dubey.shashank1991@gmail.com

A. Islam
e-mail: aminulislam@bitmesra.ac.in

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(greater than 10,000 cm^2/V-s), high electron density (because of high band offset $\Delta E_c = 0.52$ eV and $\Delta E_g = 0.71$ eV) and good thermal conductivity, InP/InGaAs DGHEMT are used in low noise amplifiers [4, 5]. Double-gate HEMT (DGHEMT) has set an epitome to reduce the short channel effects in the compound semiconductor devices. The increase in double current density, controlled gate, and transconductance intensifies the device performances in terms of cut-off frequency, maximum frequency oscillation, and drain induced barrier lowering.

The channel conductivity determines the efficient performance of DGHEMT, but the high doping concentration leads to ionized impurities scattering which results in low mobility [6]. An alternate way to increase carrier concentration in a channel is by using group III-V materials with a large bandgap difference [1]. A heterostructure is formed with doped wider bandgap material (InP) and undoped lower bandgap material (InGaAs). Electron from the doped InP ($E_g = 1.35$ eV) falls and gets trapped in the quantum well-formed in InGaAs ($E_g = 0.75$ eV) layer [3]. The channel formed in the InGaAs layer does not have impurity scattering due to the electrons donated by the InP layer.

2 Device Structure

The schematic diagram of DGHEMT is shown in Fig. 1 along with the device dimensions and materials used in various layers. DGHEMT incorporates two identical gate

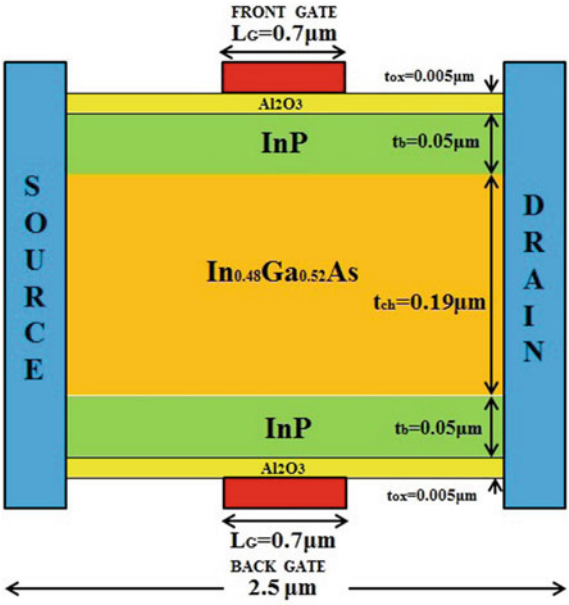

Fig. 1 Schematic diagram of the proposed device

geometries of length 0.7 μm, one at the top and other at the bottom. It is followed by an Al_2O_3 layer of thickness 0.005 μm on both sides [4]. The InP layer has thickness of 0.05 μm with concentration of 1×10^{18} atom/cm^3. The epitaxial structure is symmetric on both sides of the InGaAs layer (channel layer) having thickness of 0.19 μm with a doping concentration of 1×10^{14} atom/cm^3. The source and drain contact incorporate parasitic elements like metallization resistances and pad capacitances, whose value can be derived from the available result [4]. With an effort to model accurate device physics, the density gradient based model in a device simulator named ATLAS has been used. The DGHEMT channel confinement has been simulated with proper device dimensions and materials at various layers. It consists of symmetrically placed double heterostructures [7] implying the dimensions and doping densities of upper and lower layers.

The order of statements in the code begins with specifications of structure, which includes- meshing (forming grids), regions, and electrodes in addition to doping distribution which is specific to different layers in the structure of DGHEMT [8]. The grid has been defined such that it covers the requisite physical simulation domain. It is important to specify a good grid as it is a crucial issue for the simulation of devices. Finer meshing provides higher accuracy in simulation results at the cost of longer simulation time. Generalization is not used as it varies according to technology used for resolving critical areas like the heterojunctions and transport phenomena [9]. Hence allocation of fine grid critical areas (channel and heterointerfaces) with a coarser grid is assigned to DGHEMT structure. Once specifications of mesh are done, material type is also given to the structure of InP/InGaAs DGHEMT structure as shown in Fig. 1. Further, the values for basic parameters such as bandgap, electron mobility, saturation velocities, etc. for the channel material, are specified.

After having specified the regions, proposed materials, and the doping profile contact electrodes such as the source, the drain, Gate1 (Front Gate), and Gate 2 (Back Gate) are defined in the simulation code. In the final step, the quantum moments model has been applied to model the quantum mechanical effects glaring in the nano-dimensional channel of DGHEMT. Also, the statements defining solution specifications are specified to calculate the characteristics of devices by stepping the biases on electrodes from the initial equilibrium condition to obtain the solutions. DGHEMT structure provides an equal control of gate and hence exhibiting high transconductance property in addition to good pinch-off characteristics [10–12]. After exhaustive simulation, it was observed that the layer structure utilized in the geometry for device formation resulted to lower parasitic resistances owing to cutback in sheet resistance and higher 2DEG (two-dimensional electron gas) density in the channel. To ensure device reliability complete analysis of device potential the characteristics- subthreshold slope, breakdown voltage, and frequency analysis are taken into consideration and a detailed study has been presented in this paper.

3 Device Model

We used InP instead of AlGaN because of some advantages. The advantages of InP over AlGaN are as follows:

- In off-state, lower ionization rate of carriers at a given electric field results in higher breakdown voltage.
- No mechanical constraints are observed in the epitaxial structures since $In_{0.48}Ga_{0.52}N$ and InP are lattice-matched.

The sub-threshold slope of the InGaAs/InP based HEMT is given by

$$S = \frac{kT}{q}(1+\eta)\ln 10 \tag{1}$$

where η is a non-ideality factor related to trap density. The proposed structure shows the subthreshold in accordance with [13] . The value of η is calculated for the observed value of subthreshold slope (S) and is found to be 0.1072 for the proposed InP/InGaAs structure.

Subthreshold characteristics and the subthreshold leakage current are highly correlated. Lower value of subthreshold leakage results in higher value of ON/OFF current ratio and steeper subthreshold slope [9, 10]. We have used Al_2O_3 between InP and gate. The gate leakage of the proposed structure comes out to be of the order of 10^{-13} and the ON/OFF ratio is about 10^{10}. Keeping the short channel effects in consideration, model equations for current can be written as follows:

$$I_{\mathrm{ds}} = k(V_{\mathrm{ds}})k_n'\frac{W}{L}\left[(V_{\mathrm{gs}}-V_t)V_{\mathrm{DSAT}} - \frac{V_{\mathrm{ds}}^2}{2}\right] \quad \text{when } V_{\mathrm{DSAT}} < V_{\mathrm{gs}} - V_t \tag{2}$$

$$I_{\mathrm{ds}} = k(V_{\mathrm{DSAT}})k_n'\frac{W}{L}\left[(V_{\mathrm{gs}}-V_t)V_{\mathrm{DSAT}} - \frac{V_{\mathrm{DSAT}}^2}{2}\right] \quad \text{when } V_{\mathrm{ds}} \geq V_{\mathrm{DSAT}} \geq V_{\mathrm{gs}} - V_t \tag{3}$$

where k_n' is a proportionality constant which gives the measure of the mobility and $k(V)$ which is measure of degree of velocity saturation, expressed as

$$k(V) = \left(1 + \frac{V}{E_C L}\right)^{-1} \tag{4}$$

where E_c represents the critical electrical field at which drift velocity of the carrier saturates. Our proposed model has been verified with the simulation results.

4 Simulation Results and Discussion

Extensive simulations were carried out to verify our results using Silvaco Atlas [16]. Improved results were obtained by adjusting the value of saturation velocity and the parameters for transverse and lateral fields given in the Yamaguchi model. HEMT with InP/InGaAs instead of AlGaN/GaN exhibits better breakdown voltage and performance. The breakdown voltage of the AlGaN/AlN/GaN HEMT and AlInN/AlN/GaN MOSHEMT proposed by authors in [14, 15] were found out to be 780 and 1162 V. The proposed design showed breakdown voltage of 1417 V due to use of Si_3N_4 as passivation layer as shown in Fig. 2. The subthreshold slope of the proposed model is shown in Fig. 3. Exponential dependence of I_{ds} on V_{gs} for the proposed device is shown in Fig. 4. Proposed InP/InGaAs exhibited sub-threshold slope of 63.9 mV/decade. Low power dissipation and high performance in digital circuits and systems correspond to lower value of the subthreshold slope.

Current in the device depends mainly on two factors, mobility and carrier concentration. With the decrease in scattering the depth of the quantum well increases resulting in an increase of mobility of the charge carriers. Enhancement in mobility is achieved with the presence of an undoped InGaAs spacer layer. The transconductance

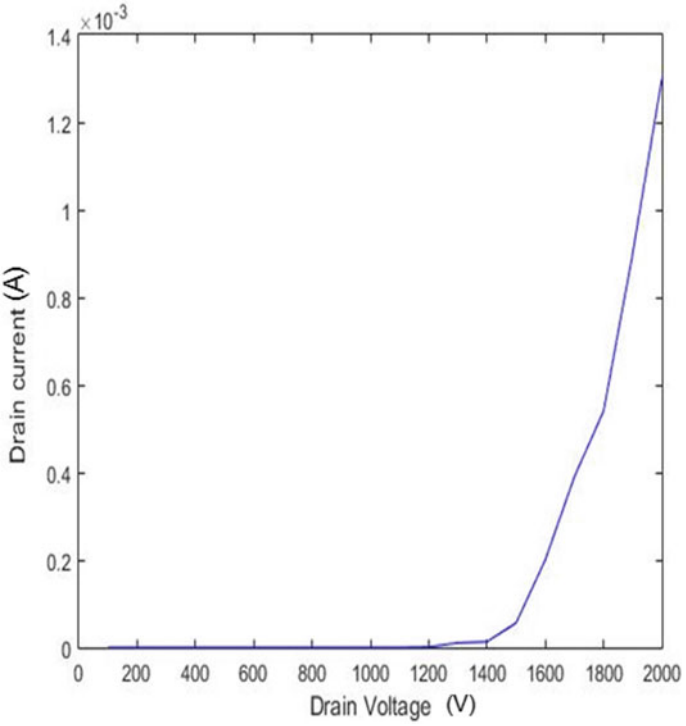

Fig. 2 Breakdown voltage characteristics of the proposed HEMT device

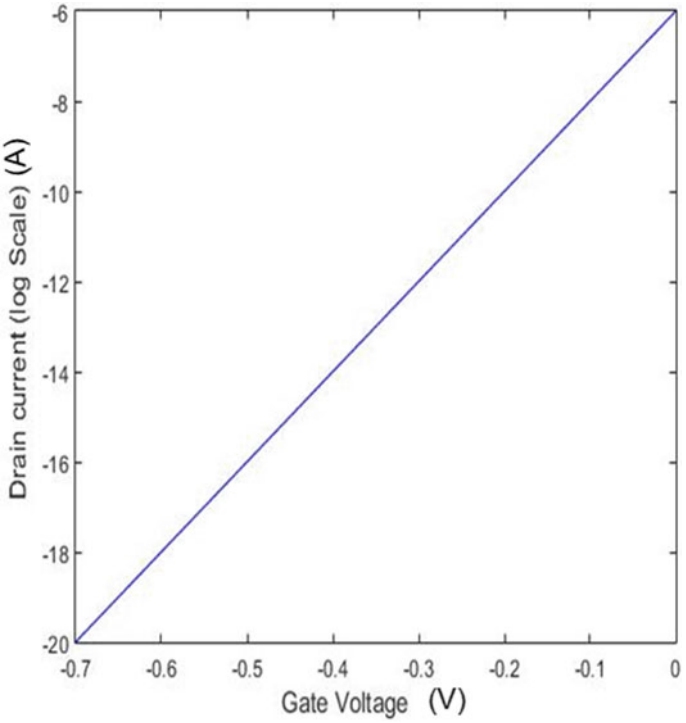

Fig. 3 Subthreshold characteristics of the proposed device

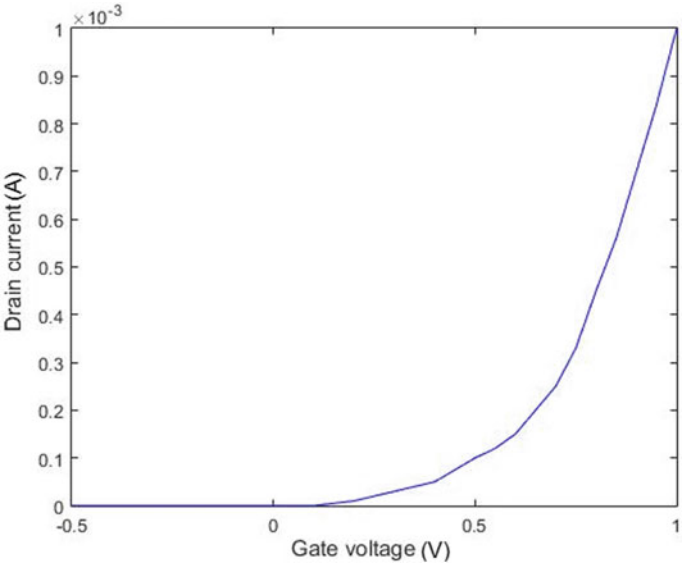

Fig. 4 $I_{ds} - V_{gs}$ characteristics of the proposed HEMT device

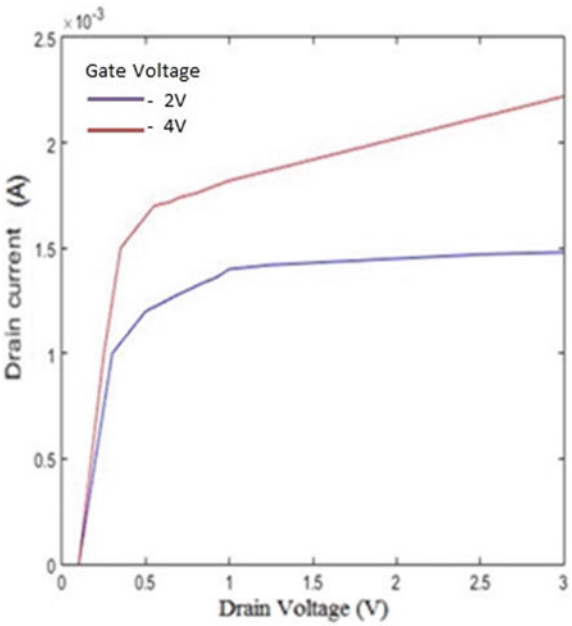

Fig. 5 $I_{ds} - V_{ds}$ characteristics of the proposed HEMT structure

curve for this device was found to be steep resulting in greater switching efficiency. We got an excellent ON/OFF current ratio of 10^{10}. The maximum transconductance of 193 mS/mm was achieved. In comparison to the transconductance of AlGaN/GaN structures, HEMTs with AlInN as barrier layer have a wider peak and gradual drop. Figure 5 shows ID-VD (output) characteristics of the presented device structure.

The relation between f_{max} and f_t can be expressed as

$$f_{max} = \frac{f_t}{\sqrt{\frac{4(R_{GS}+R_G+R_S)}{R_S} + \frac{2C_{GD}}{C_{GS}}\left\{\frac{C_{GD}}{C_{GS}} + gm(R_{GS}+R_s\right\}}} \tag{5}$$

Current gain and unilateral power gain as a function of frequency for the proposed device is plotted in Figs. 6 and 7. The unity gain frequency (f_t) is found to be 113 GHz and is constant for 1 V < V_{ds} < 2.5 V, while f_{max} = 216 GHz for V_{ds} = 7 V.

5 Conclusion

This paper successfully examines InP/InGaAs based HEMT structure, which offers improved performance compared to AlGaN/GaN-based HEMT. The sub-threshold slope is found to be closer to the ideal value and ON/OFF current ratio is found to be quite high. The observed breakdown voltage is high due to the use of Si_3N_4

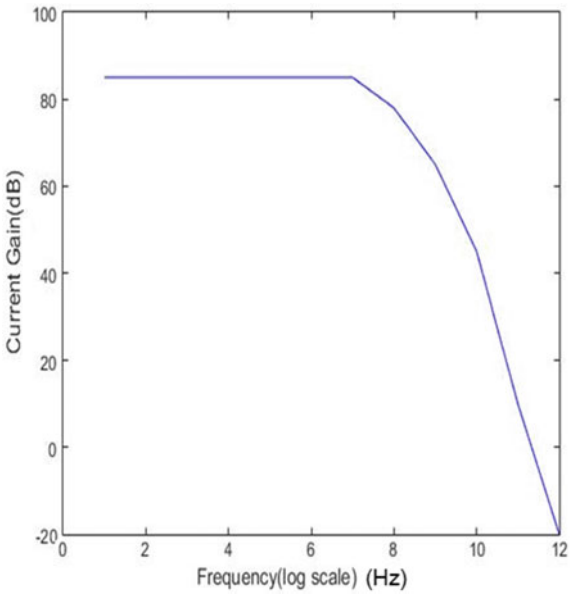

Fig. 6 Plot for cut-off frequency for the proposed HEMT structure

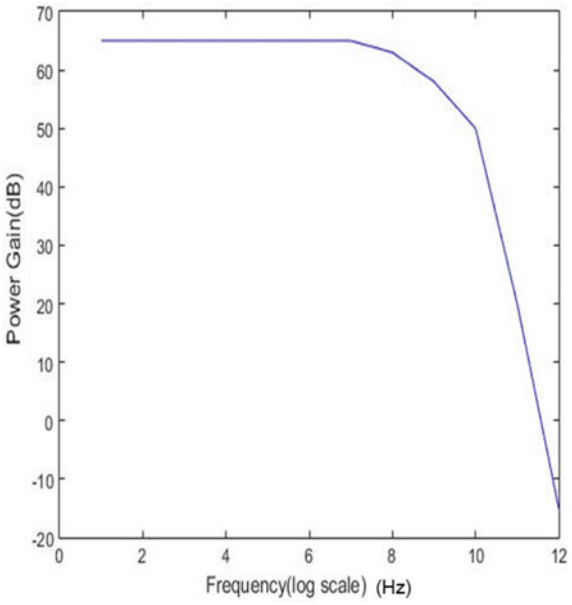

Fig. 7 Plot for maximum frequency for the proposed HEMT structure

passivation. Our findings prove it to be very encouraging device for high-frequency and high-power applications.

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Separation of Diffuse and Specular Reflection Components from Real-World Color Images Captured Under Flash Imaging Conditions

Nygel Thomas, Mayaluri Zefree Lazarus, and Supratim Gupta

Abstract Image processing applications like endoscopy, flash photography are prone to specularity reflection because of the usage of flash illumination during image acquisition. The formation of specularity reflection paralyzes the performance accuracy of many state-of-the-art feature detection algorithms. Specularity removal in the case of real-world imaging conditions is further challenging when the source of illumination is unavailable. Literature suggests that chromaticity based reflection removal algorithms circumvent the illumination source dependency by transforming the pixels into the chromaticity-intensity plane and solving a fine-grained, least-squares problem of the dichromatic model. In this paper, we extend the existing chromaticity based removal approach to Hue-Saturation-Value color domain and explore its suitability in specularity removal under flash imaging conditions. Experimentation on MIT intrinsic database demonstrates that our approach achieves desirable reflection separation results with minimum execution time compared to the state of the art.

Keywords Reflection · Saturation · Dichromatic reflection model · Color space

1 Introduction

Specularity problem is one of the most challenging hindrances in applications like biomedical, computer vision, and digital photography. With the advent of smartphones, people can capture images in low illumination conditions by using mobile flash as a source of illumination [1–3]. Low illumination condition photography

N. Thomas · S. Gupta
National Institute of Technology Rourkela, Rourkela, Odisha 769008, India
e-mail: nygel93@gmail.com

S. Gupta
e-mail: sgupta.iitkgp@gmail.com

M. Zefree Lazarus (✉)
C. V. Raman Global University, Bhubaneswar, Odisha 752054, India
e-mail: zefree.lazarus@gmail.com

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needs skill/expertise in capturing images, as the captured image can be flawed by the specularities formed due to the flash. Similarly, in the case of medical applications like endoscopy wherein a small camera with an attached flash is invasively navigated through the body of a patient—capturing video of the intended body organ for medical examination—suffers from information loss due to specularity effect. The specular problem resurfaces in many other image processing applications involving flash photography [4].

Variation in illumination level, relative positioning of ambient light source and the camera—resulting in specular reflections—which paralyze the performance accuracy of many existing state-of-the-art feature detection algorithms [5–7]. Therefore, mitigation of the specularity problem is a relevant and important challenge.

1.1 Specularity Problem

Image formation of an object is governed by three processes:

- Illumination of the object by a light source.
- Reflection of light by the object.
- Detection of the reflected light.

Generally, illumination sources have a uniformly distributed spectrum in all wavelengths of the visible region. Depending on the nature of the object, it absorbs a few wavelengths and reflects back its complementary colors—thereby providing a specific color. In literature, there are quite a few reflection models that define the image formation. Lambertian reflection model is one such fundamental reflection model [5]. In this model, the light reflected by the material is assumed to be isotropic, i.e. independent of the viewing direction. The materials which show this property are called matte materials. These matte materials do not show glare or mirror-like behavior called specularity. Many computer vision algorithms assume Lambertian surfaces and neglect the effect of specularity as outliers. In real-world images, these assumptions do not hold good because most of the objects photographed are not matte materials and therefore result in specularities. Due to this, the extent to which the Lambertian reflection model-based algorithms can be utilized is limited. A more realistic model that considers both highlights and anisotropic reflection is the Dichromatic Reflection Model (DRM) proposed by Shaufer [8].

Based on DRM, removing specularities from images can be coined as a problem of extraction of corrupted pixels from an image and converting it into a meaningful representation. Intrinsic image decomposition, a branch of image processing deals with such information retrieval application algorithms. An exhaustive survey on the available literature is provided in Artusi et al. [5]. Most of the available algorithms have high time complexity and therefore the adaptability of these algorithms for real-time applications is limited.

1.2 Contribution of This Work

In this manuscript, we explore the DRM approaches and check the usability of the available state-of-the-art intrinsic decomposition methodologies in the context of specularity removal in real-time images. By extending the chromaticity based reflection removal approach proposed in Shen et al. [13] to Hue-Saturation-Value (HSV) color space we propose a simple yet practical way of suppressing the spectacle problem.

The paper is organized as follows: Sect. 2 describes the Dichromatic reflection model—its assumptions, advantages, and limitations; Sect. 3 describes the chromaticity based reflection removal algorithm; Sect. 4 provides the proposed extension of the method discussed in Sect. 3; Sect. 5 the experimentation, simulation results, and observations are reported. The concluding remarks are given in Sect. 6.

2 Dichromatic Reflection Model

Dichromatic Reflection Model (DRM) is a mathematical model that describes the reflection of light from a non-uniform surface. It focuses on the color aspect of reflection of light from a nonhomogeneous material illuminated by a uniform single source of light. Based on these assumptions, the model proposes that the total reflected light from a surface of uniform color is the weighted linear combination of the light reflected from the surface or interface of reflection which is called specular reflection and the complementary color reflected from the lattice of the material called diffuse reflection. The reflection from the surface will have mirror-like or specular features and the body component has diffusive properties that contribute mainly to the glow less color or matte of an object. These specular and diffusive components can be classified into:

- A univariable function of the wavelength of the illuminating source and gives the relative spectral power distribution.
- A multivariable function the geometrical properties which give the geometrical scale factor.

The total radiance of reflected light from a surface,

$$L(\lambda, i, e, v) = L_i(\lambda, i, e, v) + L_b(\lambda, i, e, v) \tag{1}$$

By using the dichromatic mathematical model, we can further divide the body and surface into variable separable equations which depend on the geometry of the surface as well as the wavelength of the illuminant light. They are mutually independent. Thus, the Eq. 1 can be further modified as,

$$L(\lambda, i, e, v) = m_i(i, e, v)c_i(\lambda) + m_b(i, e, v)c_b(\lambda) \tag{2}$$

where m_i and m_b are the scale factors which change from point to point depending upon the geometry and C_i and C_b are the spectral power density over a range of wavelengths which do not depend on geometry. By using the linearity property as well as the variable separability of the body and surface reflection components, Shaufer [8] proposed that the pixels of a dichromatic surface will be confined to a parallelogram when plotted in RGB space.

The DRM provides a basic mathematical model but does not provide an effective way of isolating the specular pixels. This aspect was further extended by Klinker et al. [9] by plotting the color histogram of all the pixels. The histogram forms a T-shaped distribution with highlight and matte component clustering into two side lobes of the T-shaped structure. But this approach is limited to dielectric objects as well as objects with uniform diffuse colors. Tan et al. [10] extended the DRM approach and proposed a chromaticity based approach that separates the reflection components from a single image by mapping the pixels in a particular color space to maximum chromaticity-pixel intensity space.

2.1 Extension of DRM to Pixels in a Color Space

As the DRM models color in terms of its reflection, it is obvious to extend the concept of dichromatic reflection to the popular color spaces. Moreover, when this model is fitted into a particular color space, the possibility of separation of its reflection components also has a pivotal role. This subsection gives the extension of DRM to the most used color space, viz. RGB space.

The spectral power density is the energy received on a surface per unit area per unit wavelength for a particular illumination. Using the spectral projections, the pixel values of the color images can be computed from the Spectral Power Distribution (SPD) of the measured light. For a color camera, the color value of every pixel is given by the color matrix with the corresponding RGB components viz. r_x, g_x and b_x for a pixel. Color value matrix for an SPD $X(\lambda)$ and a camera sensitivity for R, G and B, $r(\lambda)$, $g(\lambda)$ and $b(\lambda)$, respectively is given by

$$C_x = \begin{bmatrix} r_x \\ g_x \\ b_x \end{bmatrix} \tag{3}$$

where $r_x = \int x(\lambda) r(\lambda)$, $g_x = \int x(\lambda) g(\lambda)$, $b_x = \int x(\lambda) b(\lambda)$ respectively.

2.2 The Linearity of the Model

The model which is obtained by combining the properties of a dichromatic color model and RGB color space is found to have linearity property. If $X(\lambda)$ and $Y(\lambda)$ are two different SPDs, the resultant color value matrix which arecombined in ratios a and b, respectively, is obtained by

$$C_{(aX+bY)} = aC_X + bC_Y \tag{4}$$

After applying the linearity property to the spectral projections we have

$$C_L = m_i c_i + m_b c_b \tag{5}$$

C_L is given by the linear combination of all the SPDs which contribute to the illumination of a particular surface contributing to the corresponding pixel value. The pixel values line on the surface of a plane on a parallelogram in color space [10]. Due to the linearity property, the pixel values are confined to a two-dimensional plane rather than a three-dimensional space.

3 Separation Using Chromaticity

In order to separate the diffuse and specular components of a single color image, the chromaticity of pixels can be used as a parameter [13]. They can be obtained using the intensity of every pixel form the corresponding RGB vectors of every pixel. The chromaticity based approach transforms the pixels in a particular color space to a two-dimensional plane which is spanned by the maximum chromaticity and intensity values of every pixel.

The chromaticity for a pixel can be defined as:

$$\beta(\boldsymbol{p}) = \frac{I(\boldsymbol{p})}{I_r(\boldsymbol{p}) + I_g(\boldsymbol{p}) + I_b(\boldsymbol{p})} \tag{6}$$

where $I(\boldsymbol{p})$ is the intensity of the pth pixel and $I_r(\boldsymbol{p})$, $I_g(\boldsymbol{p})$, $I_b(\boldsymbol{p})$ are its corresponding RGB values. β is a vector with R, G and B components such that $\beta = (\beta_r, \beta_g, \beta_b)$. The chromaticity factors can be separately found out for the diffusive as well as specular components using Eq. (6).

In order to separate the two reflection components from a color image, its corresponding RGB color space is mapped to an intensity-maximum chromaticity space. Maximum chromaticity is a scalar which is defined by:

$$\beta_{\max} = \frac{\max\left(I_r(\boldsymbol{p}) + I_g(\boldsymbol{p}) + I_b(\boldsymbol{p})\right)}{I_r(\boldsymbol{p}) + I_g(\boldsymbol{p}) + I_b(\boldsymbol{p})} \tag{7}$$

4 Proposed Methodology

Color models specify a coordinate system of color space where each and every point in that space represents a unique color [11]. The chromaticity approach in [13] is defined in RGB color space, so in this manuscript, we extended the approach to Hue-Saturation-Value (HSV) color model to analyze whether the transformation enhances or diminishes the separation of reflection components.

4.1 HSV Color Model

Hue-Saturation-Value is one of the widely used color space in many image processing applications. In the HSV color model, color is represented as a combination of hue, saturation, and value which is modeled geometrically as a cone or cylinder. Hue is the color portion of the color model expressed as a number from 0° to 360°. Saturation is the amount of gray in the color, from 0 to 100%. Value works in conjunction with saturation and describes the brightness or intensity of the color, from 0 to 100%, where 0 is completely black, and 100 is the brightest and reveals the most color. The advantage of the HSV color model is the independency of hue and value/brightness channels. Hue channel exclusively contains information about the color of pixel whereas the value channel has information regarding the intensity of the reflected light from the object. Saturation channel is found to give information about both colors as well as brightness.

4.2 The Effect of Specularity on Pixels in RGB, HSV Color Spaces

Since DRM assumes illuminant light to be white (contains wavelength of all frequencies with uniform energy density), in RGB space for an 8-bit pixel, specularity is represented by the channel values (255, 255, 255). Histogram analysis on MIT intrinsic image database [19], reveals to us the fact that the presence of specularities results in a right shift of intensities in all three channels (R, G, and B). In HSV color space specularity does not have any significant impact on the hue channel [12]. From Fig. 1, we can notice that the value of hue changes insignificantly with different levels of illumination brightness. There is a right shift in the brightness value (V) channel. In saturation channel, we find an inverse relationship between the S channel values and the specularities causing the S channel values to shift left.

Based on this observation, we propose to extend the maximum chromaticity based approach proposed in Shen et al. [13] to HSV color space. Removal of specularity from images is generalized as a two-step problem.

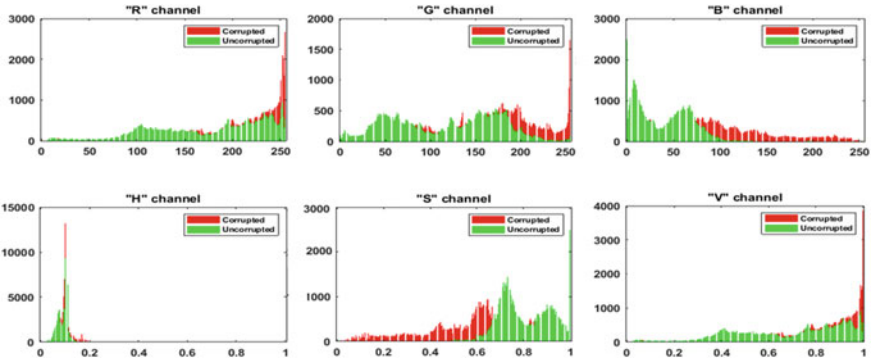

Fig. 1 Effect of specularities in RGB, HSV color spaces. In the figure, each subplot contains the histogram of corrupted and uncorrupted images taken from MIT intrinsic database [19]

- Identifying the location of the diffuse and specular pixels from the original image which is degraded by specularity effect.
- Modifying the pixels which are corrupted by specularity.

The proposed extension of the maximum chromaticity based approach is given in Fig. 2.

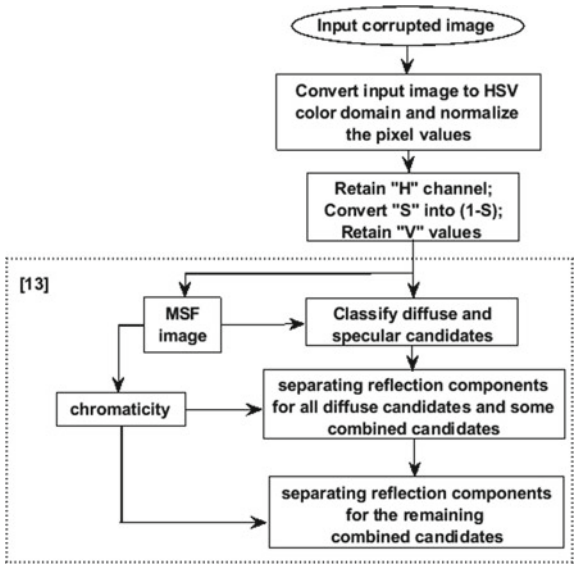

Fig. 2 Flowchart of the proposed method

5 Experimentation

To compare the performance of the existing and the proposed extension of [13], we have considered the single image based intrinsic image decomposition methodologies proposed in [13–18]. Real-world images from MIT intrinsic image database [19] were used for experimentation. The dataset contains 120 images of various illumination conditions captured with and without flash. The images with flash were given as the input image and the images captured under no-flash are considered as the ground-truth for qualitative analysis. PSNR, SSIM, and EKI were the parameters used for comparison. Sample images of the experimental output image are given in Fig. 3.

5.1 Simulation Results: Visual Similarity Measure

For qualitative measurement of the visual similarity between the ground-truth image and the output rendered image, the authors considered four metrics, namely, Peak Signal to Noise Ratio (PSNR), Structural Similarity (SSIM) index [20], Edge Keeping Index (EKI), and time taken for the execution. Mean Square Error (MSE) represents the cumulative squared error between the reconstructed and the input image, whereas

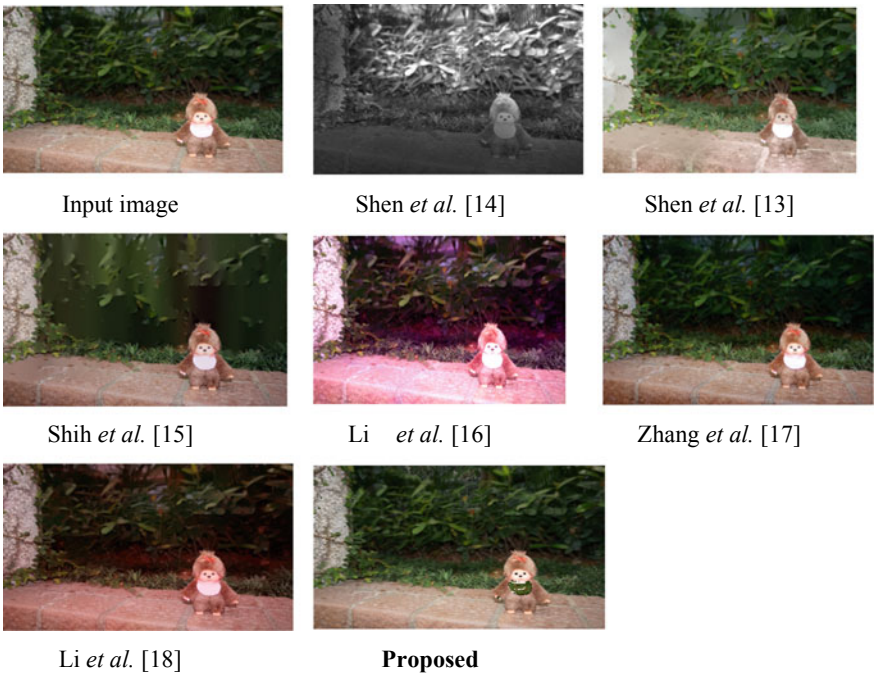

Fig. 3 Sample output image of the state-of-the-art algorithms [13–18] and the proposed approach

Table 1 Visual similarity measure values of the proposed and state-of-the-art algorithms. Database: MIT intrinsic database [10]

	PSNR (in dB)	SSIM	EKI	Time (in sec)
Shen et al. [14]	57.16	0.55	0.45	5.10
Shen et al. [13]	62.68	0.71	0.80	0.37
Shih et al. [15]	53.81	0.43	0.13	3.70
Li et al. [16]	64.40	0.78	0.73	1.09
Zhang et al. [17]	64.76	0.78	0.77	9.17
Li et al. [18]	63.45	0.75	0.81	0.41
Proposed	66.23	0.80	0.84	0.26

PSNR (in dB) represents a measure of the peak error. SSIM is used to quantify the amount of visual and structural information retained in the output rendered image. SSIM index measure varies between 0 and 1, where 0 corresponds to structurally completely uncorrelated images, and 1 corresponds to similar images. On the other hand, edge preservation capability and discrepancy in edge location between output and the ground-truth image is determined using EKI. EKI values vary between 0 and 1. A higher value of EKI index indicates that most of the edges in the input image are retained in the output rendered image. Experimental results are presented in Table 1.

From the results, it is evident that the proposed approach enhances the performance of [13] and the results are slightly better than many of the compared state-of-the-art methods. The major advantage of the proposed preprocessing step of conversion into HSV color space are:

- HSV color space is less sensitive to noise.
- As hue values do not change much because of specularity, the processing of identifying and separating reflection components is mostly confined to (1-S) and V channels only.

Due to the above-mentioned advantages, the proposed preprocessing approach provides better visual similarity measures in comparison with the existing approaches. Also, as most of the processing is confined to two channels, the proposed approach takes lesser time than [13].

5.2 Implementation Details

All the experiments were conducted on a PC with Intel (R) Core (TM) i7—3770 CPU and 8:00 GB RAM. The algorithms were implemented in MATLAB R2017a without any GPU acceleration.

6 Conclusions

The specularity removal of images is a relevant but challenging task. Most of the available literature on specularity removal has been tested on synthetic images only. In this manuscript, we implemented a few state-of-the-art intrinsic image decomposition methods for single image based specularity removal application. We have extended Shen et al. [13]—a chromaticity based reflection removal algorithm into HSV color domain. Experimental analysis on MIT intrinsic images [19] reveals that the proposed extension of [13] has better performance and minimum time complexity than the existing approaches.

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Solar Medical Sterilizer Using Pressure Cooker for Rural Off-Grid Areas

K. A. Khan, Salman Rahman Rasel, S. M. Zian Reza, M. A. Saime, Nazmul Alam, M. Abu Salek, and Mehedi Hasan

Abstract To design and develop a prototype, solar medical steam sterilizer for use in remote areas around the world. A paraboloidal dish-type concentrator was used as a collector and a pressure cooker was used as a receiver/absorber. The concentrator and receiver (C–R) system was used as a medical sterilizer. To increase the reflectance of the concentrator, aluminum foil was used as cover to reflect the solar radiation on to the bottom of the pressure cooker. The bottom of the pressure cooker was coated by normal black body. The pressure cooker gained temperature and pressure. A thermocouple was used to measure the temperature, and pressure gauze was used to measure the pressure, respectively. The solar beam radiation was measured by pyrheliometer. The required temperature was 121 °C, and the pressure was 1.05 kg/cm^2 which were obtained, and those were measured by thermocouple and pressure gauze, respectively. When the obtained temperature 121 °C and pressure 1.05 kg/cm^2 was kept for

K. A. Khan (✉) · N. Alam
Department of Physics, Jagannath University, Dhaka 1100, Bangladesh
e-mail: kakhan01@yahoo.com

N. Alam
e-mail: nazmulalam.shovo@gmail.com

S. R. Rasel
Local Government Engineering Department (LGED), Fulbaria, Mymensingh, Bangladesh
e-mail: salman_rasel80@yahoo.com

S. M. Zian Reza
Department of Physics, Uttara University, Dhaka, Bangladesh
e-mail: smzianreza@gmail.com

M. A. Saime
Chief Instructor (Technology) Computer, Dinajpur Polytechnic Institute, Dinajpur, Bangladesh
e-mail: abu.saime@gmail.com

M. Abu Salek
Department of Chemistry, Adamjee Cantonment College, Dhaka 1206, Bangladesh
e-mail: salek@acc.edu.bd

M. Hasan
Department of Electrical and Electronics Engineering, City University, Dhaka, Bangladesh
e-mail: mehedi.physics@gmail.com

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15 min mixed with medical instruments and water, and then it was tested at ICDDRB and BCSIR at Dhaka, Bangladesh and shown that these medical instruments were sterilized properly. The cost of the whole system was around 90 USD. It has been used as a paraboloidal dish-type concentrator, a pressure cooker, and medical instruments mixed with water which makes a solar steam medical sterilizer.

Keywords Solar thermal conversion · Sterilization · Parabolic dish-type concentrator · Pressure cooker · Aluminum foil · Thermocouple

1 Introduction

It is needed to sterilize the apparatus of test tube, needle, syringe, caser, cotton, etc., as a mandatory for the betterment of the patient [1–3]. For this reason, autoclave is used in the hospital which is run by grid electricity [4–7]. The electricity crisis is high in Bangladesh. There are a lot of areas in Bangladesh where there is no grid electricity till today. As a result, it is not possible to set up the health center at the remote areas of Bangladesh [8–11]. To keep it in mind, it has been developed the solar medical sterilizer. It is operated by solar thermal system. It is not needed any fossil fuel to operate this new and innovative technology [12–15]. This technology can be used at the off-grid areas of Bangladesh. Furthermore, it can be used in the space research center also. It is found that this solar sterilizer can kill the germs of test tube, needle, syringe, caser, cotton, etc., at 1.05 kg/cm2 pressure and 121 degree celsius (°C) temperature [16–19].

2 Objectives

i. To design and develop an innovative solar medical sterilizer.
ii. To use the solar thermal technology for medical equipment and disposal of hospital waste for steam sterilization at the off-grid areas across the globe.

3 Methodology

The components of the instrument are parabolic concentrator, aluminum foil, pressure cooker, thermocouple, digital thermometer, pressure gauge, fillary nut, Benzu bolt, copper pipe, socket, rubber, plastic pipe, etc. This solar medical sterilizer has mainly two components.

3.1 A Is Parabolic Dish-Type Solar Concentrator

Figure 1 shows the design details of solar medical sterilizer. Figure 1a shows the design of a solar medical sterilizer. Figure 1b shows the backside of the concentrator, and Fig. 1c shows the tracking system of the sterilizer system.

Figure 1 shows that B is the base stand, C is absorber, and d is the chamber.

Figure 2a shows the solar medical sterilizer for practical demonstration for the students. Figure 2b shows an experimental setup for R&D purposes. The size of the medical sterilizer is given: aperture diameter of the dish, $D = 1.8$ m, aperture area $= 2.76$ m^2, depth of the dish, $d = 0.27$ m, focal length of the dish $= D^2/16d = 0.78$ m. The concentrator focuses the radiation to the absorber/pressure cooker (C). The pressure cooker acts as an autoclave. The absorber was coated by normal black coating. Then the absorber absorbs the more heat. The water was put into the absorber and that absorber transfer the heat to the absorber. The obtained stagnation temperature was around 150 °C. The thermal and optical efficiency test was also studied before using it as a sterilizer.

(a). Design **(b) .**Back side **(c).**Tracking device

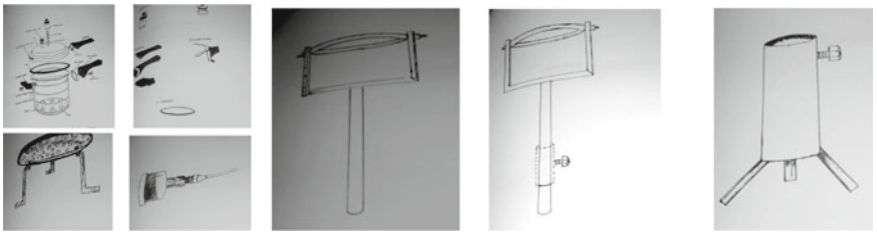
Fig. 1 Design of an experimental setup of a prototype solar medical sterilizer

(a). Sterilizer for practical demonstration **(b).** Experimental set-up for practical use

Fig. 2 An experimental setup of a prototype solar medical sterilizer

(a) Design of a P.C **(b)** P.C. with a Chamber **(c)** Medical instruments

Fig. 3 Design of an experimental setup of an absorber of a prototype solar medical sterilizer



(a) : Different parts **(b) :**Frame **(c) :**Inclined Adjuster **(d) :** Base

Fig. 4 Different parts of the medical sterilizer

3.2 Absorber (Pressure Cooker)

Figure 3 shows the pressure cooker details which act as an autoclave. Figure 3a shows the design of a pressure cooker, and Fig. 3b shows the pressure cooker with a chamber where the medical instruments have been set up.

Figure 4 shows the different parts of the pressure cooker (PC). Figure 4a shows four parts including the chamber. Figure 4b shows the frame of the pressure cooker, Fig. 4c shows the inclined adjuster of the frame, and Fig. 4d shows the base of the solar medical sterilizer. Figure 3 shows a pressure cooker, which acts as an autoclave. The medical instruments (Fig. 4) have been used as a load. There is a thermocouple (E), and a pressure gauge (F) is shown in Fig. 3. The required obtained temperature and pressure were measured by a thermocouple (E) and a pressure gauge (F), respectively.

4 Results and Discussion

The paraboloidal dish-type sterilizer took above 1 h for sterilization with 300 ml of water and 1.5 kg load. The test of the effectiveness of the sterilizers, culture in test tubes was kept along with medical items in all the models during experiments (Table 1).

Table 1 Data for measurement of sterilization period of a prototype solar medical steam sterilizer

No. of observation	Local time (h)	Time duration (min)	Insolation (w/m^2)	Temperature (°C)	Pressure (kg/cm^2)	Load (kg)	Quantity of water (ml)
1	11.00	00	600	50	0.5	1.5	300
2	11.20	20	610	65	0.6	1.5	300
3	11.40	40	618	80	0.8	1.5	300
4	12.00	60	630	90	1.0	1.5	300
5	12.20	80	642	110	1.3	1.5	300
6	12.40	100	650	130	1.4	1.5	300
7	13.00	120	663	142	1.5	1.5	300
8	13.20	140	700	150	1.6	1.5	300

Figure 5 shows that the change of insolation/beam radiation with the change local time (*h*). Here insolation means the beam/direct radiation. It is mentioned that the diffuse radiation does need to work in this paraboloidal dish-type sterilizer.

It is found (Fig. 6), the variation of insolation/beam radiation with time duration (min). Here insolation means the beam/direct radiation. It is mentioned that the diffuse radiation does need to work in this paraboloidal medical sterilizer.

It is found (Fig. 7) that the variation of temperature (°C) with local time (h). Here temperature increases with local time. It is also shown that after operation it needs around 1 h upto sterilization temperature (121 °C).

Figure 8 shows that the change of temperature (°C) with the change of time (min). Here temperature increases with time duration. It is also shown that after operation it needs around 1 h upto sterilization temperature (121 °C).

Fig. 5 Variation of insolation/beam radiation with local time (h)

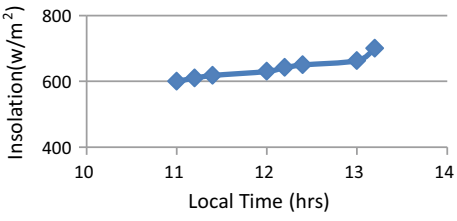


Fig. 6 Variation of insolation/beam radiation with time durations (min)

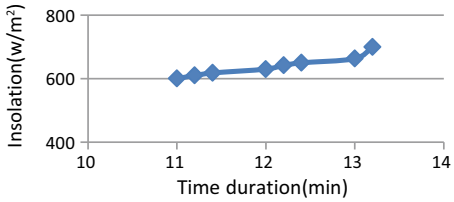


Fig. 7 Change of temperature (°C) with the change of time duration (h)

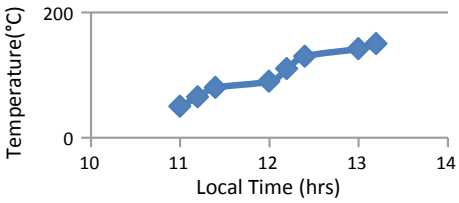


Fig. 8 Variation of temperature (°C) with time duration (min)

Figure 9 shows that the change of temperature (°C) with the change of insolation (w/m^2). Here temperature increases with time insolations/beam radiation. It is also shown that after operation, it needs around 1 h upto sterilization temperature (121 °C).

It is found from Fig. 10 that the change of pressure (kg/m^2) with the change of local time (h). Here pressure increases with time local times. It is also shown that after operation it needs around 1 h upto sterilization pressure (1.05 kg/cm^2).

It is found (Fig. 11) that the variation of pressure (kg/m^2) with the variation of time duration (min). Here pressure increases with the change of time duration. It has been found that after operation, it needs around 1 h upto sterilization pressure (1.05 kg/cm^2).

It is found (Fig. 12) that the variation of pressure (kg/m^2) with the variation of insolation (w/m^2). Here pressure increases with the variation of insolation/beam

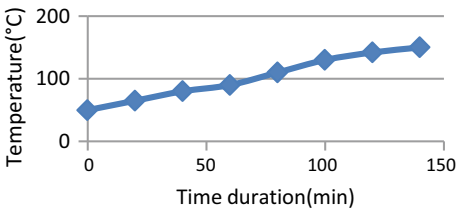


Fig. 9 Variation of temperature (°C) with insolation/beam radiation (w/m^2)

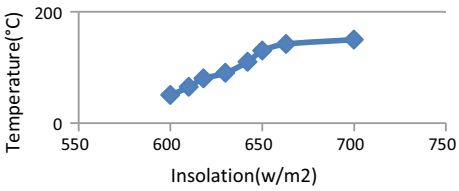


Fig. 10 Variation of pressure (kg/cm^2) with Local time (h)

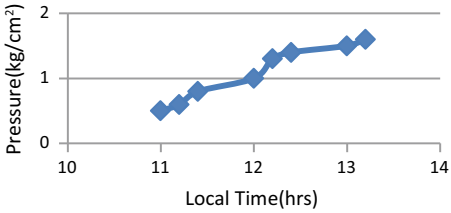


Fig. 11 Variation of pressure (kg/cm^2) with time duration (min)

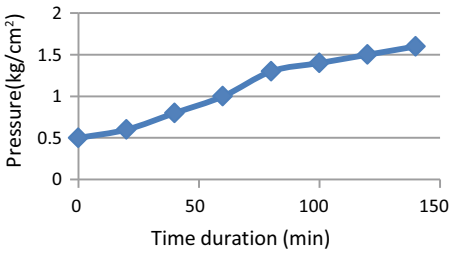


Fig. 12 Variation of pressure (kg/cm^2) with insolation (w/m^2)

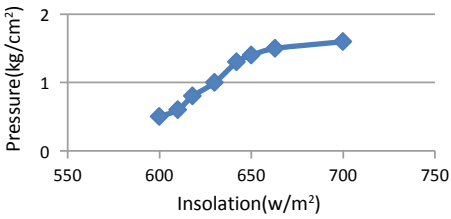


Fig. 13 Variation of pressure (kg/cm^2) with temperature (°C)

radiation. It is also shown that after operation, it needs around 1 h upto sterilization pressure (1.05 kg/cm^2).

It is found (Fig. 13) that the variation of pressure (kg/m^2) with the variation of temperature (°C). Here pressure increases with the variation of temperature. It is also shown that after operation, it needs around 1 h upto sterilization pressure (1.05 kg/cm^2).

5 Prototype Solar Medical Sterilizer (Without Pressure Cooker) by Fresnel Reflecting Solar Fresnel Reflecting Concentrating Collector

It consists of 32 mirror strips (Fig. 14) of equal width and separated by equal distance. The reflectance of each mirror strip is around 0.7.

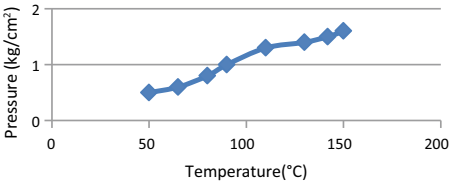


Fig. 14 Experimental setup of a solar medical sterilizer by Fresnel reflecting concentrator

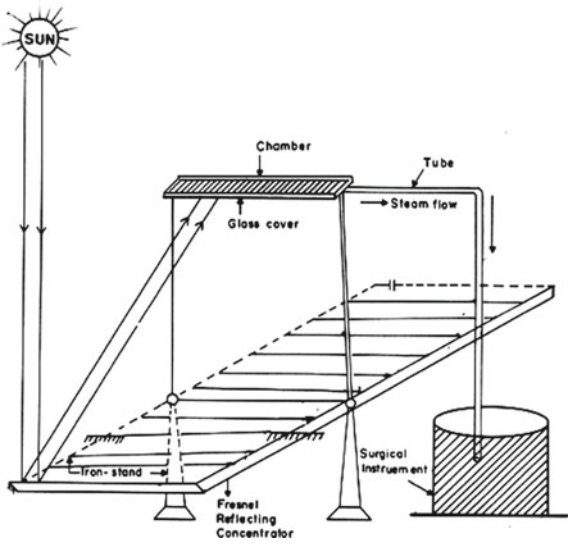


Fig. 15 Used medical instruments

A small amount of water, less than 50 c.c., is added to the chamber to make up for steam. The chamber is then loaded (Fig. 15) shows vessel can hold many syringes or a range of surgical instruments.

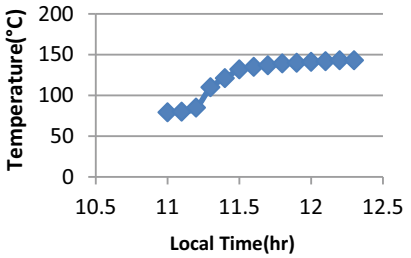
6 Experimental Observations and Discussions

The sterilizer with 1.5 kg load and 300 ml water attains the required temperatures of 152 °C in about 50 min and completes the process in 65 min (Fig. 16; Table 2).

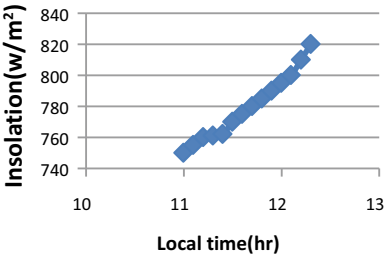
Figure 16 shows the chamber temperature versus time for suns on one sunny day. It has been found that the change of insolation with the change of time for absorber. The condition of the loads was 1.5 kg load and quantity of water taken 250 ml. From Fig. 16a, b, it is shown that the sterilization period is around 65 min (Table 3).

The condition of the absorber was 1 kg load, and quantity of water was 200 ml. It is shown that the sterilization period was around 52 min (Fig. 17; Table 4).

Figure 18a shows the variation of temperature and pressure versus time with load. The load condition was 1.5 kg load and quantity of water taken 250 ml. Figure 18a



(a). Variation of temperature with time.



(b). Variation of insolation with time.

Fig. 16 Variation of temperature and insolation with time

Table 2 Data collection for temperature and insolation

Local time (h)	Time duration (min)	Temperature (°C)	Insolation (w/m^2)
11.00	00	79	750
11.10	10	80	755
11.20	20	85	760
11.30	30	110	761
11.40	40	121	762
11.50	50	132	770
11.60	60	135	775
11.70	70	137	780
11.80	80	139	785
11.90	90	140	790
12.00	100	141	795
12.10	110	142	800
12.20	120	143	810
12.30	130	143	820

shows the variation of temperature with the change of time. It has been found from Fig. 18b about the required pressure for around 2 h by the pressure cooker (PC).

7 Conclusion

The sterilizer was found to work satisfactorily. Microbiological test showed that this model was capable of sterilizing surgical instruments. From the study and actual field operation, it is concluded that the operation of this solar medical sterilizer is simple and required tracking after every 15 min. It can save 30 kg of fuel woods every day.

Table 3 Data collection for temperature and insolation

Local time (h)	Time duration (min)	Temperature (°C)	Insolation (w/m^2)
11.00	00	77	650
11.10	10	81	655
11.20	20	84	660
11.30	30	109	661
11.40	40	118	662
11.50	50	131	670
11.60	60	134	675
11.70	70	136	680
11.80	80	138	685
11.90	90	139	690
12.00	100	140	695
12.10	110	141	700
12.20	120	141	701
12.30	130	141	702

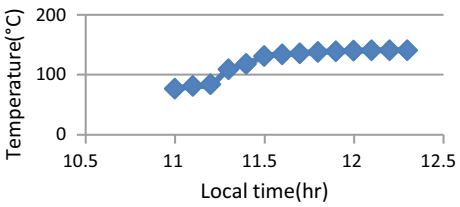
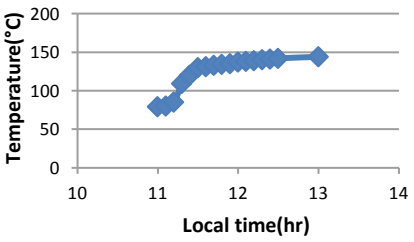


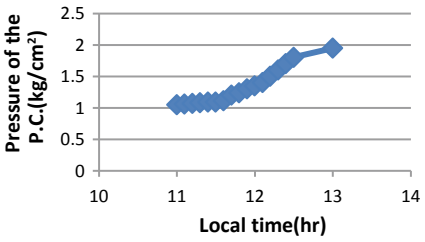
Fig. 17 Variation of temperature with time

Table 4 Data collection for temperature and pressure

Local time (h)	Time duration (min)	Temperature (°C)	Pressure of the PC (kg/cm^2)
11.00	00	79	1.05
11.10	10	80	1.06
11.20	20	85	1.07
11.30	30	109	1.08
11.40	40	120	1.09
11.50	50	130	1.09
11.60	60	131	1.11
11.70	70	133	1.20
11.80	80	134	1.24
11.90	90	135	1.30
12.00	100	137	1.35
12.10	110	138	1.40
12.20	120	139	1.50
12.30	130	140	1.60
12.40	140	141	1.70
12.50	150	142	1.80
13.00	160	144	1.95



(a): variation of temperature with time



(b): variation of the absorber pressure with time

Fig. 18 Variation of temperature and pressure of the absorber with time

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Performance Analysis of (13,0) and (17,0) Carbon Nanotube Field Effect Transistors (CNFETs)

Nishant Gupta, Ankita Dixit, and Navneet Gupta

Abstract This paper explains the comparative analysis of the performance of (13,0) and (17,0) carbon nanotube field-effect transistors (CNFETs). The comparison is done by studying the output and transfer characteristics of CNFETs. Modeling of the total capacitance of cylindrical CNFETs for the two types of chirality (13,0) and (17,0) has also been reported in the paper. It has been observed that (13,0) carbon nanotube has lesser propagation delay, however, but the drain current is higher for (17,0) for the given parameters. This shows that the switching application is better in case of (13,0) for the given parameters.

Keywords Carbon nanotube · Switching · On-current · Chirality

1 Introduction

According to Moore's law, in any of the circuits, the dimensions of the devices have decreased by the factor two in every two years. But it has been observed that after attaining a certain limit on the device size, factors like electron tunneling, power dissipation short-channel effects, associated leakage currents, and the changes caused in the device structures and doping, predominate and hence making us to look for other materials which could replace the current technology successfully. And one of such replacement in traditional MOSFET channel structure is the use of single-walled carbon nanotube (SWCNT) or an array of carbon nanotubes as a path between source and the drain [1].

In the carbon nanotube field-effect transistor (CNFET) technology, the single-wall carbon nanotube (SWCNT) is usually used as a path between source and drain for

N. Gupta (✉) · A. Dixit · N. Gupta
Birla Institute of Technology and Science, Pilani, Pilani-Campus, Rajasthan, India
e-mail: guptanishant113@gmail.com

A. Dixit
e-mail: ankitadixit.199@gmail.com

N. Gupta
e-mail: ngupta@pilani.bits-pilani.ac.in

A. Sikander et al. (eds.), *Energy Systems, Drives and Automations*, Lecture Notes in Electrical Engineering 664, https://doi.org/10.1007/978-981-15-5089-8_27

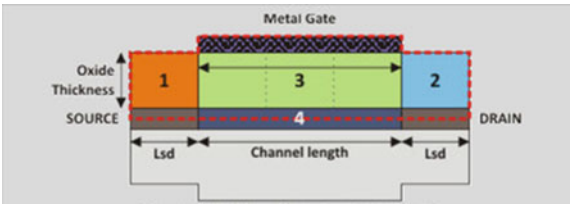

Fig. 1 Schematic view of cylindrical CNFET considered for simulation

the current. Both p and n channel transistors can be formed using carbon nanotubes. CNFETs and MOSFETs have very similar physical structures, and their current–voltage characteristics are very promising and similar. This makes us to conclude that CNFET is a promising candidate for replacing MOSFETs [2].

SWCNTs are synthesized by laser ablation which helps in the fabrication of CNFETs. These SWCNTs are deposited from solution onto oxidized Si wafers which are placed pre-patterned with platinum and gold electrodes [3]. All the initially made CNFETs were the hole conductors whose reason was unclear, but the predictions say, that it must be due to the doping by adsorption of oxygen from the atmosphere or due to contact doping. Now, for making the transistor as donor conductor it was doped by thermal annealing in a vacuum and by using an alkali gas [4]. This method involves the transfer of charge from within the nanotube, which seems very similar to doping performed in case of conventional semiconductor devices.

The manufacturing of both *p*-type and n-type CNFETs enabled mankind to make its first carbon nanotube CMOS circuits. Derycke et al. are credited for demonstrating the first simple CMOS logic gates, which also included an inverter fabricated using a single carbon nanotube. After that, more complex carbon nanotube-based circuits have been built [5–9]. Figure 1 shows the schematic view of CNFET considered for this study.

Cylindrical CNFETs are the further improvement on the top gated device geometry. Here, the whole body curvature of the nanotube is gated, instead of covering just a small part of it. This reduces the leakage current and improves the device switching ratio and hence enhancing the device's electrical performance. Fabrication of these types involves wrapping carbon nanotubes in gate dielectric and gate contact with the help of atomic layer deposition. Finally, these nanotubes are then deposited on an insulating substrate, due to which some part of its wrappings gets etched off, making its ends to expose. The gate, drain, and source contacts are then deposited on the metallic gate wrappings and at the ends of the nanotubes [10].

For the simulation of devices, we consider ballistic transport for semiconducting carbon nanotubes, for which we require Schrodinger and Poisson's equation with other quantum effects to be taken into consideration [10]. Ballistic transport in the carbon nanotubes applies when its channel length is smaller in comparison with electron mean free path length hence, CNFETs with channel lengths less than 50 nm are generally best-suited for the ballistic operation. According to the ballistic theory, a gate voltage is required for controlling the energy barrier for the current flow,

while the source and the drain voltages are used for controlling their Fermi level, respectively [10].

1.1 Gate Capacitance

The total gate capacitance is a simple series addition of the capacitance of insulator layer C_{ins} and capacitance of inversion layer C_{inv} [11]. As shown in Fig. 2 in which the first sub-band of the electron is occupied, the C_{inv} can be given as a series combination of centroid capacitance C_{cent} and quantum capacitance C_Q. C_Q is defined by the properties of material its channel is made of. The term quantum capacitance was coined by Luryi [12]. As the charge inside the quantum well increases, Fermi level of the semiconductor moves up and above the conduction band, because density of state is finite in any of the semiconductor quantum well. This type of movement of the Fermi level gives rise to quantum capacitance, which originates from the intervention of E_F into the E_C.

The C_{cent} is given as the average of electron channel from the insulator interface [13]. The C_{ins} has the inverse relationship with its thickness. The C_{ins} is smaller in its value than compared with C_{inv} in case of strong inversion, and thus, the gate capacitance tends to C_{ins}. As the thickness of insulator approaches, the nanometer range, which is more apt for us, the insulator capacitance C_{ins} and C_{inv} becomes finite, which means that C_{cent} and C_Q start to influence the total capacitance at gate [14]. When C_{cent} is ignored and all the charges are supposed to be present inside the semiconductor layer, then the charge induced in the channel is supposed to give $\frac{Q_S^2}{2C_{ins}} + \frac{Q_S^2}{2C_Q}$ amount of energy to the MOS, where the total electron charge in the channel is represented by Q_S [14]. The first term in the above expression describes the electrical field energy in the oxide layer and the second term gives the energy in the semiconductor layer [14]. Usually, C_{ins} is smaller in comparison with C_Q, so the second term in the above expression is neglected. But as the size of the device

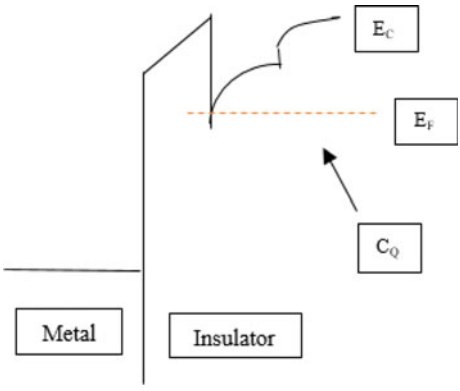

Fig. 2 Conduction band diagram in strong inversion

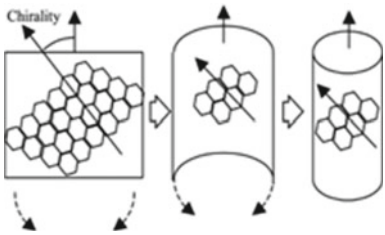

Fig. 3 Schematic representation for the formation of a carbon nanotube using graphene [15]

reaches the range of few nanometers, C_{ins} becomes comparable or even bigger in value than C_{Q}, and hence, C_{Q} should be precisely used in the devices which work at this scale, to determine the total gate capacitance [14].

1.2 Device Parameters

SWCNT can behave like a semiconductor or as a conductor, depending upon the atomic arrangement in the tube as shown in Fig. 3.

Direction of chirality is represented by the integral pair (n, m). We can easily find out that if the given carbon nanotube is semiconducting or metallic in nature by seeing its indexes (n, m). The nanotube is metallic if its indexes are given as, $n = m$ or $n - m = 3i$, where 'i' is an integer, else, the tube acts as a semiconductor [15]. The diameter of the nanotube could be calculated from the following formula:

$$\frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + mn} \tag{1}$$

where $a_0 = 0.142$ nm is the atomic distance between two carbon atoms. (13,0) CNT has the diameter equal to 1.0177 nm, and (17,0) has a diameter equal to 1.3309 nm. Current–voltage characteristics of the CNFET are similar to MOSFET. The threshold voltage is defined as the voltage required to switch on the transistor. Intrinsic carbon nanotube's threshold voltage can be approximated to be first-order inverse function of the diameter. CNFETs has four terminals (Source, Drain, Gate, and Body), just the same as our traditional silicon-based transistors as shown in Fig. 4, Since we are trying to achieve a low series resistance in the ON-state, hence we can place a lightly doped semiconducting nanotube under the gate for making the channel, and heavily doped carbon nanotube segments between the source/drain and the gate. Slowly, the gate potential is increased with the help of external means, and the device gets electrostatically turned ON or OFF. Although carbon nanotubes act as the best replacement for silicon due to its idiosyncratic possessions like stiffness, tenacity, and strength, still it is not being able to be produced in large quantity due to the lack of relevant technologies and higher cost of its production. A particular reference current at a fixed V_{gs} voltage gives a threshold voltage which can easily be controlled by varying the diameter of the carbon nanotube. For the fabrication of SWCNTs with the

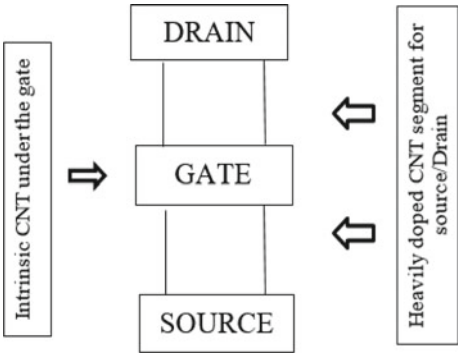

Fig. 4 Schematic diagram of a carbon nanotube transistor [15]

required chirality structure has been given in. CNFETs can easily be used for making a near-ballistic channel transport for the electron; hence, they are more appealing to us.

Also, the high dielectric gate insulator can easily be applied and the device physics of CNFETs is relatively easier to execute. Till date, most of the work which has been performed on CNFETs is on their DC properties, but the research is still going, on its AC parameters which are technologically more relevant to us. Theoretically, it is having been shown that a short nanotube operating in the ballistic region and having a limit on quantum capacitance should be able to provide gain in the range of terahertz.

Terms like current density, device switching speed, propagation delay, switching energy, operating temperature, and cost are evaluated for comparing the performances of CNFET-based logic circuits and CMOS logic circuits [14].

2 Results and Discussions

In this work, the simulation of the cylindrical carbon nanotube FET is done with the help of nanohub simulator (Fig. 5) which is an online environment for the simulation of nano-devices such as CNFETs, Si-Nanowire FETs and many types of conventional field-effect transistors like *pn* junction, Si-MOSFET, DG-MOSFET, etc. The nanohub was created by the NSF-funded Network for Computational Nanotechnology and provides a very good resource for nanoscience and technology-related kinds of stuffs. In the following Table 1, the parameters considered for simulation are listed.

Figures 6, 7, and 8 show the I_{ds} versus V_{gs}; I_{ds} versus $V_{ds;}$ and Capacitance versus V_{gs} for the (13,0) chirality CNFET.

Figure 6 plot is obtained by varying V_{gs} in the steps of 0.1 V from 0 to 0.7 V and keeping V_{ds} as constant at 0.4 V.

Figure 7 plot is obtained by varying V_{ds} in the steps of 0.1 V from 0.1 to 0.7 V and keeping V_{gs} at a constant bias of 0.4 V.

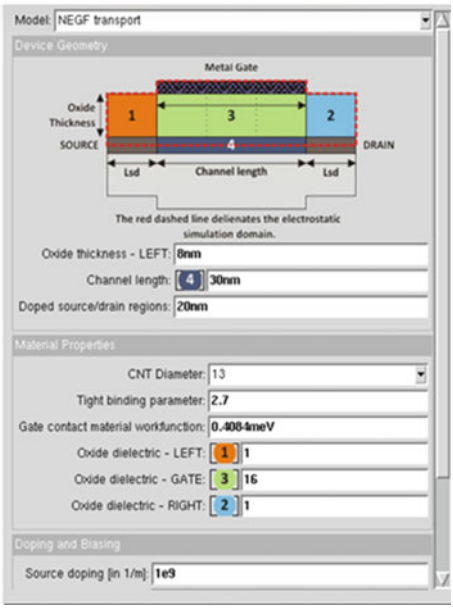

Fig. 5 Simulation tool environment

Table 1 Parameters considered for simulating (13,0) and (17,0) cylindrical CNFETs

Parameters	Values
Channel length	30 nm
Oxide thickness	8 nm
Doped source/drain region	20 nm
Tight binding parameter	2.7
Gate contact material work function	0.4084 meV
Left oxide dielectric	1
Gate oxide dielectric	16
Right oxide dielectric	1
Source doping	10^9 m^{-1}
Drain doping	10^9 m^{-1}
Channel doping	0

Figure 8 plot is obtained by varying V_{gs} values in the step of 0.1 V from 0 to 0.7 V while keeping V_{ds} at the constant bias of 0.4 V.

Figures 9, 10, and 11 show I_{ds} versus V_{gs}; I_{ds} versus $V_{ds;}$ and Capacitance versus V_{gs} for the (17,0) chirality CNFET.

Figure 9 plot is obtained by varying V_{gs} value in the step of 0.1 V from 0.1 to 0.7 V, keeping V_{ds} at a constant bias of 0.4 V.

Figure 10 plot is obtained by varying V_{ds} value in the step of 0.1 V from 0.1 to 0.7 V, keeping V_{gs} at a constant bias of 0.4 V.

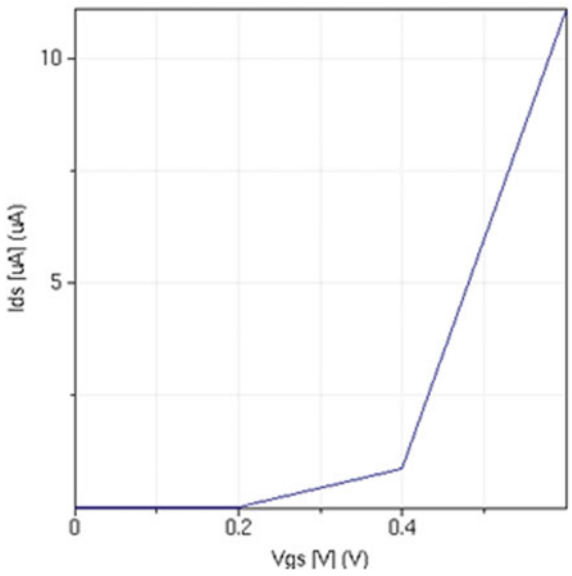

Fig. 6 I_{ds} versus V_{gs} plot for (13,0) CNFET

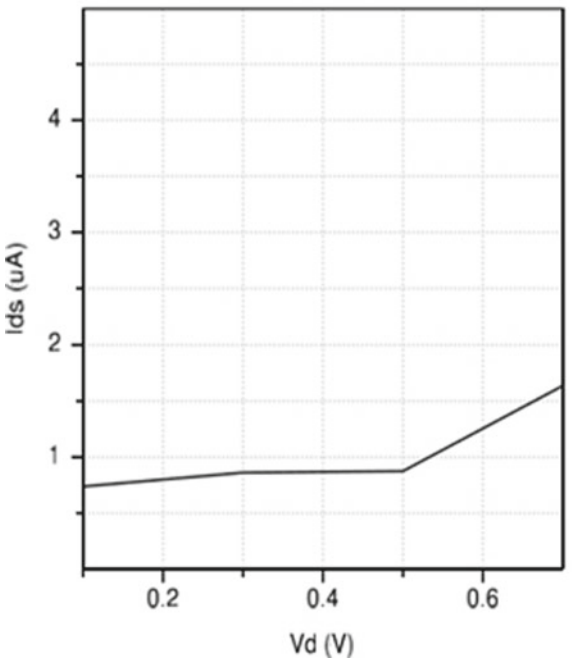

Fig. 7 I_{ds} versus V_{ds} plot for (13,0) CNFET

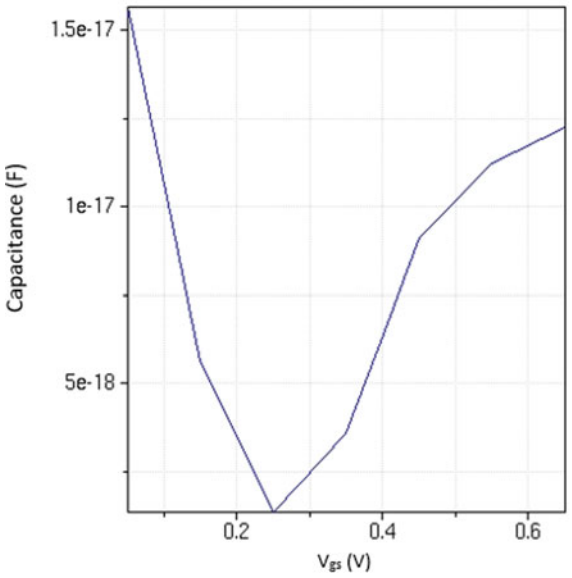

Fig. 8 Capacitance versus V_{gs} plot for (13,0) CNFET

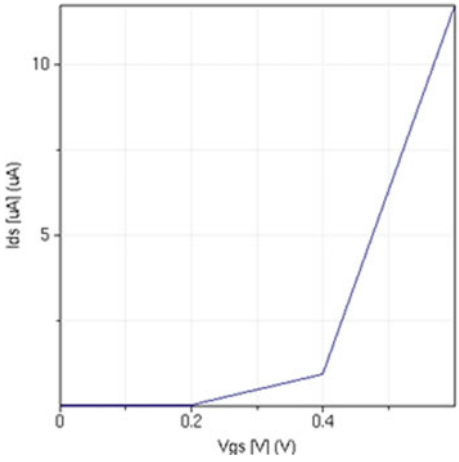

Fig. 9 I_{ds} versus V_{gs} plot for (17,0) CNFET

Figure 11 capacitance versus V_{gs} Plot for (17,0) CNFET plot is obtained by varying V_{gs} value in the step of 0.1 V from 0.1 to 0.7 V, keeping V_{ds} at a constant bias of 0.4 V.

The I_{ds} versus V_{gs} characteristic for the cylindrical CNFET is shown in Figs. 6 and 9 for both the chirality; (13,0) and (17,0). It can be inferred from these curves that (17,0) have higher drain current I_{ds} than (13,0) till 0.32 V and then (13,0) has higher drain current till 0.45 V, after which they both have the approximately same value of current for constant V_{ds}.

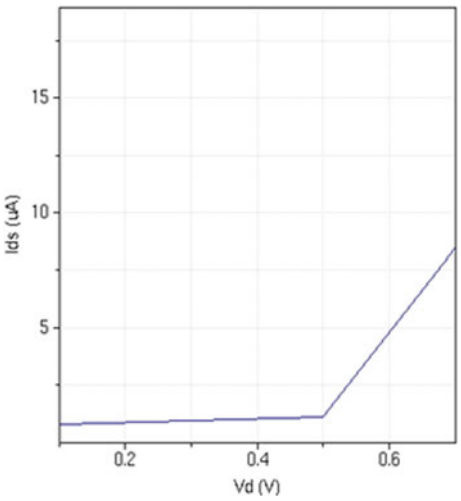

Fig. 10 I_{ds} versus V_{ds} plot for (17,0) CNFET

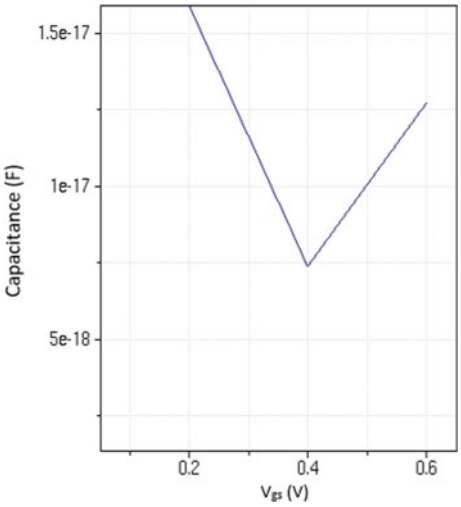

Fig. 11 Capacitance versus V_{gs} plot for (17,0) CNFET

From the graphs of Figs. 7 and 10 plotted at the gate voltage of 0.4 V show drain current of 1.25 uA at 0.6 V of V_{ds} in case of (13,0) carbon nanotube. On the other hand, (17,0) chirality carbon nanotube, at gate voltage of 0.4 V, has Ids equal to 5 uA at V_{ds} of 0.6 V. And similarly, for other values of V_{ds}, we got the larger value of drain current for (17,0) chirality CNFET.

In this paper, we have also studied the effect of carbon nanotube diameter on total gate capacitance at different gate voltages for single-walled CNFET devices. From Figs. 8 and 11, it is clear that in deep nanometer regime, CNFET devices are advantageous over MOSFETs due to their lesser quantum capacitance (which is an

important factor in the calculation of total gate capacitance) and hence improved threshold voltages, propagation delays and reduced leakage of current. On the other hand, in case of MOSFETs, the value of quantum capacitance goes on increasing which leads to increased propagation delay and hence performance degradation [14]. From the simulations performed above, we got the graph of total gate capacitance which also contains the factor of quantum capacitance. Now, on comparing the capacitive values of the (13,0) and (17,0) chirality CNTFETs, the minimum value of 1.37987×10^{-18} F is achieved in the case of (13,0) at the gate voltage of 0.25 V and (17,0) has its minimum capacitance of 7.40927×10^{-18} F at the gate voltage of 0.4 V; also on seeing the overall graph, we could infer that (13,0) is having a lesser gate capacitance (and hence quantum capacitive value) at most of the values of V_{gs}, which makes (13,0) more reliable and faster with minimized propagation delay.

3 Conclusion

In this paper, we have compared (13,0) and (17,0) CNFET in terms of their output and transfer characteristic and also the capacitance of CNFET due to their chirality. It was observed that drain current is high for (17,0); however, for (13,0) gate capacitance is lower. Therefore, we can infer from the results that (13,0) is better for switching applications as compared to (17,0). Hence, we conclude that (13,0) CNFET is more reliable and faster as compared to (17,0) CNFET.

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Enhanced Electrical and Mechanical Characteristics Monitored by Various Software for Lithium-Ion Battery Tests

Snigdha Sharma, Amrish K. Panwar, and M. M. Tripathi

Abstract This paper represents a battery test bench for testing of lithium-ion coin cell ($LiMn_2O_4$) batteries for electrical and mechanical characterization where mechanical tests are performed using Multiphysics software and electrical characteristics are tested using hardware circuits. A hardware test bench has been developed to analyze various electrical tests for evaluating coin cell battery performance during a discharge cycle. These electrical tests have been performed on the data acquisition software to obtain real-time data and display the battery-related information such as voltage and load curves. Further, a battery test like an external short circuit test has been performed and also for improving battery characterization, the capacitor bank has been connected parallelly with the battery bank. Also, simulation has been performed for mechanical characterization of lithium-ion ($LiMn_2O_4$) coin cell battery such as thermal modeling test at various temperature ranges (26–124 °C) that has been simulated using Multiphysics software, where cell temperature has been analyzed on the various range. Also, various tests during simulation have been performed and analyzed during a drive cycle. The state of charge has been triggered for both negative and positive electrodes.

Keywords Data acquisition software · Multiphysics software · Electrical test · Mechanical test · Lithium-ion battery bank · Capacitor bank

S. Sharma · M. M. Tripathi (✉)
Department of Electrical Engineering, Delhi Technological University, New Delhi, India
e-mail: mmmtripathi@gmail.com

S. Sharma
e-mail: sharma.snigdha93@gmail.com

S. Sharma · A. K. Panwar
Department of Applied Physics, Delhi Technological University, New Delhi, India
e-mail: panwaramar@gmail.com

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1 Introduction

In recent years, society's status creates a lot of problems in the environment such as the greenhouse effect, pollution, and many more. For making environment eco-friendly and pollution-free, we focused on renewable energy or eco-friendly devices such as electric vehicles, rechargeable batteries, and many more [1]. Nowadays, the most attractive and commercialize rechargeable batteries are lithium-ion batteries. This battery has gained a lot of attention in various sectors due to its miscellaneous advantage in the energy storage area [2]. In today's world, the batteries are not only growing in the field of portable electronics but it also step-in toward the field of the automobile sector, electricity sector for energy storage, communication sector, and many others [3]. Hence, battery technology usage increases rapidly in various fields for different types of applications for future prospects [3]. Moreover, rechargeable lithium-ion batteries have a lot of advantages such as high capacity, high energy density, high power density, long cyclability, low memory effect, and the least environmental effect but these are also complicated while using experimentally. So, to make these batteries more reliable and safe, the battery test has been evaluated to determine the battery characteristics [4, 5].

This paper evaluates the lithium-ion battery and performed several tests on it to examine the mechanical and electrical characterization techniques. In this, mechanical characterization has been analyzed on Multiphysics software in which experimental data is used for designing the theoretical model and optimized the battery simulation results during the drive cycle on various loads [6]. This simulation model includes various inputs in terms of model parameters, physical data, thermal and electrical properties, etc. Hence, various tests are performed after simulated the battery model such as thermal temperature range test, coin cell polarization test, and cell potential and load test at different C-rate [7]. Therefore, battery characterization with the help of computational techniques has been proposed through Multiphysics software [8].

Further, the hardware prototype was designed to evaluate the lithium-ion coin cell. This coin cell was fabricated in a research laboratory and used to develop a battery bank. In this coin cell, the cathode was made up of $LiMn_2O_4$ material and this material was synthesized in the laboratory. However, this coin cell was used to develop a battery bank for a hardware prototype. This hardware was interfaced with software through NI-6001 DAQ card [9] and results were optimized with the help of data acquisition software [10]. The main focus of this experiment is to optimize the electrical characteristics such as battery voltage and current during discharge condition and also perform battery external short circuit tests.

2 Model Geometry and Formulation

2.1 Battery Model Formulation

Simulation analysis has been optimized on (1D) one-dimensional model geometry for better results [11]. In this study, the optimization of mechanical characterization for lithium-ion coin cells has been evaluated. The main focus during this simulation is the temperature of the coin cell, cell potential during various load cycle, and penetration tests on the cell. These all three components are monitored and act as a control unit for the model. This simulation model also explains the state of charge (SOC) of the cell and represents the charging and discharging curves. Firstly, the lithium-ion coin cell model was designed on Multiphysics software [12]. In this model, the cell contains five components for simulation which are followed as a current collector (CC) for both sides, separator, positive electrode, and negative electrode.

Initially, aluminum CC was connected with the positive electrode and the lithium manganese oxide ($LiMn_2O_4$) was used as a positive electrode. Further, separator (microporous polypropylene sheet Celgard 2400) was used to separate the positive and negative electrode and liquid electrolyte ($LiPF_6$ with the EC: DMC-1:1) was filled between both these layers for the movement of ions during oxidation and reduction process. Finally, the negative electrode was used as a carbon, and copper CC was attached to a negative electrode.

During this model formulation, the mechanical characterization of the cell has been optimized. Coin cell battery was taken for heat transfer and heat flows only in one direction for the solid interface. There were two conditions for optimizing the temperature variance across the cell, i.e., thermal insulation and convective heat flux condition.

Initially, the 1D model of coin cell battery has been designed and different parameters are set according to the battery conditions. Table 1 represents the various material parameters for the evaluation of thermal properties. Similarly, boundary conditions were set for the battery such as thermal insulation was set in the leftmost boundary of the battery and also at the center of the battery. Hence, the heat flux condition shows the heating surface of the battery which was set on the rightmost boundary. After heating conditions, air cooling through a heat transfer coefficient 10 W/(m^2 K) was applied to the boundaries of the battery. Finally, drive cycle data has been imported in the model that provides information regarding C-rate versus time at various intervals from 20C to 1C and 1C is equal to 12 A.

Table 1 1D battery model parameters for thermal properties

Parameters	$LiMn_2O_4$	Carbon	$LiPF_6$	Aluminum CC	Copper CC
Young's modulus (Pa)	$4.9*e^8$	$4.2*e^8$	–	$110*e^9$	$70*e^9$
Density (kg/m^3)	3600	2240	940	8960	2700
Heat capacity (J/kg k)	2500	884	1046	385	900

2.2 Model Parameters

The lithium-ion coin cell model has certain other more parameters for simulation which had taken from experimental results such as electrode thickness, the total thickness of the cell, and many more. There are some operational parameters for coin cell which explained in Table 2. Therefore, these parameters may change according to the requirement of the simulation model.

There are many known parameters such as positive and negative electrode transfer coefficients and the electrolyte charge transfer coefficient that are taken from the literature and others are optimized according to the simulation analysis. In Sect. 3, the experimental setup will be illustrated from the battery model.

3 Overview of Experiment

For electrical characterization, a simple hardware prototype has been designed with the help of simple electronic components. A lithium-ion coin cell has been connected with a circuit for optimizing the discharge curves with the help of data acquisition software [13].

3.1 Materials and Equipment

For optimizing the electrical characteristics, the following equipment was used to develop a hardware circuit such as a battery bank of six coin cell that is connected in series and parallel, multiple resistance of various range 0–500 Ω, DC motor used a variable load, capacitor bank connected parallelly, multiple switches, wires, PCB, and other monitoring instruments [11].

3.2 Experiment Setup

A hardware prototype was used for three electrical tests in which different types of discharge curves have been optimized. In Fig. 1, three different circuit diagrams were demonstrating for electrical characterization. Firstly, a short circuit test was performed and Fig. 1a demonstrates the circuit diagram in which switch SW1 is closed for measuring the battery potential and current across the terminal with the help of NI DAQ card.

Secondly, a switch is closed and DC motor was connected across it as load and the potential and current of the battery bank were monitored as shown in Fig. 1b. In this circuit, a capacitor bank was not connected across the battery bank. Lastly, a

Table 2 Measured parameters for battery simulation

Parameter	Units	Value	Description
Cell voltage	V	3.8	Cell potential
Length	m	$1.42*e^{-4}$	Cell total thickness
epsl_separator	–	0.4	Porosity
$Temp_{initial}$	K	328	Initial temperature
$Temp_{final}$	K	395	Final temperature
Max electrode SOC	SOC_{max}	0.79	Operational SOC
Min electrode SOC	SOC_{min}	0.02	Operational SOC
Q-Battery	A*h	12	Capacity
N-layers	–	25	No. of cell layers
kT-battery	L_batt/(L_pos/kT_pos+L_neg/kT_neg+L_pos_cc/kT_pos_cc+L_neg_cc/kT_neg_cc+L_sep/kT_sep)	0.87451 W/(m K)	Thermal conductivity
Rho_battery	(rho_pos*L_pos+rho_neg*L_neg+rho_pos_cc*L_pos_cc+rho_neg_cc*L_neg_cc+rho_sep*L_sep)/L_batt	2189.3 kg/m^3	Density
Cp-battery	(Cp_pos*L_pos+Cp_neg*L_neg+Cp_pos_cc*L_pos_cc+Cp_neg_cc*L_neg_cc+Cp_sep*L_sep)/L_batt	1391.8 J/(kg K)	Heat capacity
C-rate	–	1	C-rate factor

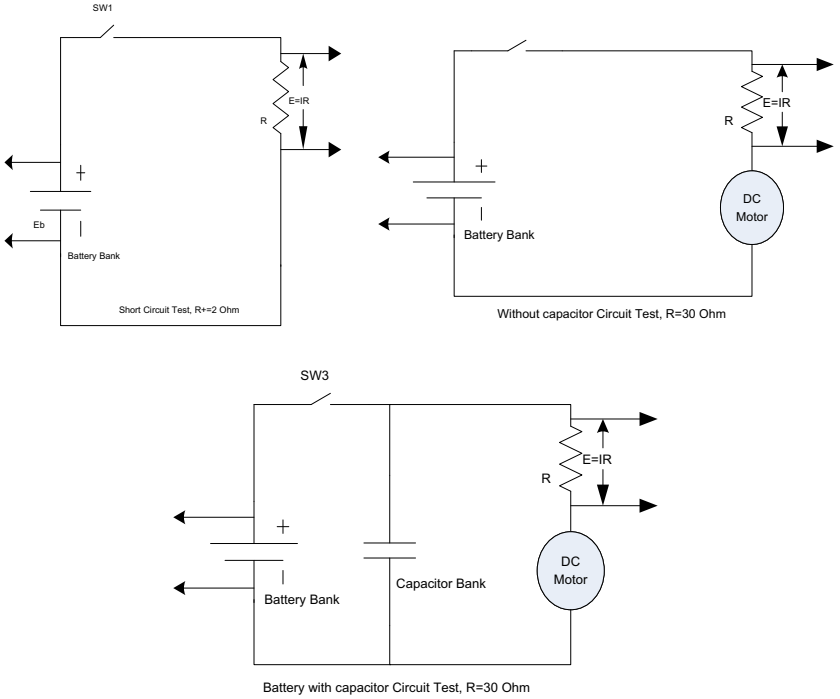

Fig. 1 Circuit for hardware design. **a** circuit for short circuit test. **b** Circuit design for battery without capacitor bank. **c** Circuit for the hybrid combination of battery and capacitor bank

hybrid combination of both capacitor bank, as well as battery bank, was connected across the load and then voltage and current discharge curves were measured as shown in Fig. 1c. In this hardware, when the battery supply is ON and the voltage starts flowing across the variable resistor terminal, then two terminals of NI DAQ card were connected and read the data across it [14]. Further, this DAQ card makes a connection with the PC for analyzing data with software [15].

This is a real-time simulation software in which hardware and software are interfaced with one another [16]. There are many in-built functions in this software that help for analyzing data such as communication links, electronic functions, mathematical functions, and many more [17]. There are two panels in the software, i.e., front panel that helps for interfacing between hardware and software whereas other is VI panel that helps for modification in the virtual instrument. Figure 2 represents the VI panel of the software in which the program has been developed for analyzing the data of the hardware prototype.

Now, a hardware setup was developed with a 2032-coin cell of $LiMn_2O_4$ material as well as a capacitor bank. Figure 3 demonstrates the hardware prototype for electrical testing and discharge curves were obtained on the front panel.

Moreover, in this study, both the hardware and simulation setup were developed for optimizing the battery characteristics [18].

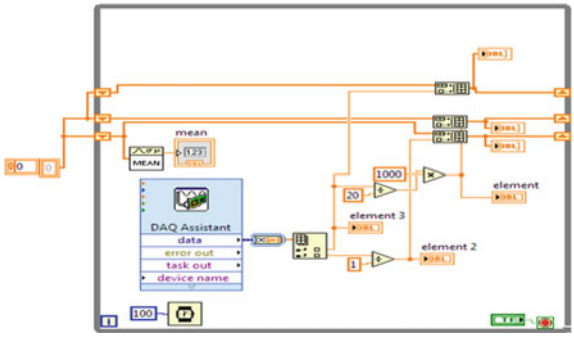

Fig. 2 VI front panel program for hardware prototype

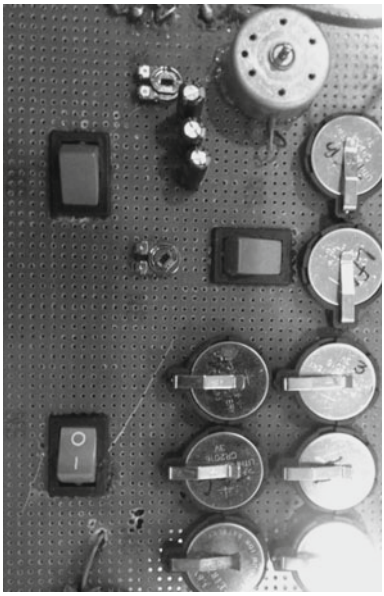

Fig. 3 Hardware prototype for electrical testing

4 Result and Discussions

For battery characterization, the following mechanical and electrical tests have been carried out on the simulated model as well as on the hardware model. Initially, simulated results were optimized on the software at different boundary conditions and then experimental results were evaluated. Hence, all results were briefly explained.

4.1 Mechanical Characterization

In this simulation, a lithium-ion coin cell has been formulated through the software and for thermal analysis, a heat source generator was connected with a separator to raise the temperature of the cell. Using homogenized properties, a convective heat flux boundary condition was set for analyzing the temperature difference across the cell. The temperature across the cell increases gradually, and the heat flows across the separator in one direction only. Figure 4 represents the surface temperature after the 1500 s, in which the temperature was uniformly distributed over the surface of the cell and heat was accumulated for a long time across the cell.

After the 3D simulation view of the coin cell, the plot has been plotted at various interval timing and analyzes the temperature change across the cell. Figure 5

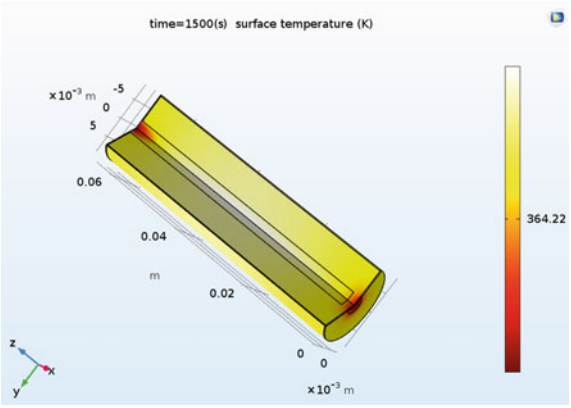

Fig. 4 Temperature distribution on the surface of the cell

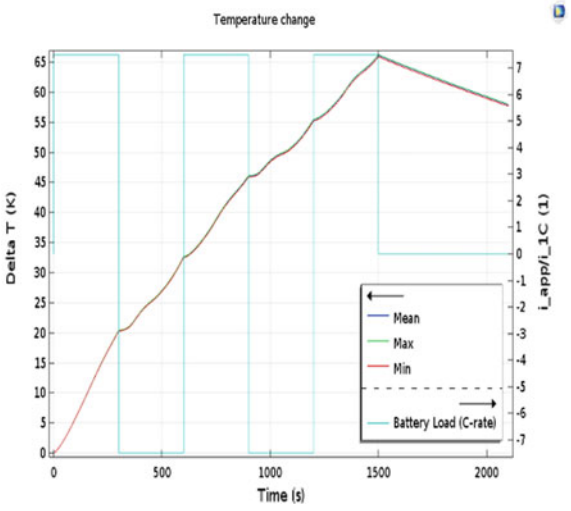

Fig. 5 Temperature plot at various range

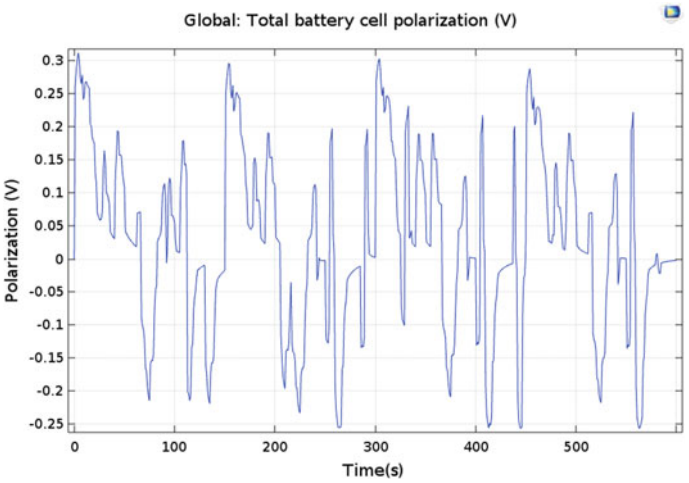

Fig. 6 Mechanical polarization test for cell

represents the plot of temperature in which mean, the maximum, and minimum temperature were analyzed.

It shows that there was no variation in the temperature and no hot spot was shown across the boundary of the cell. Also, the temperature across the battery was going on increasing during the drive cycle. In the temperature plot, the battery load at various C-rates was constant which shows stability in the coin cell. Figure 6 represents the mechanical polarization test of the cell, which shows the internal resistance as well as the life cycle of the cell. If polarization across the cell was large, then it may lead to the small life cycle as well more heat generation across the cell so it should always be minimum. In this result, polarization voltage was very small about 0.3 V which would be considered as a negligible internal resistance across the cell and its cycle represents the cell life which was stable during the drive cycle and less heat generation also.

During all this mechanical characterization, the cell was at the operating condition. Hence, simulated electrical graphs were plotted to obtain the data during simulation such as cell current, potential, and load at various C-rates. Figure 7 represents the cell potential at limiting range 4.2 and 4 V during charging and discharging operation.

Furthermore, the cell was observed at various C-rates and it shows good cyclability during this operation. However, Fig. 8 represents the state of charge of both positive and negative electrodes and in this plot, a positive electrode shows a 65% state of charge and the negative electrode attains 14–29% state of charge.

Hence, these results show a good state of charge during its operation and also represent less strain on the cell which causes good stability on the cell during its operation.

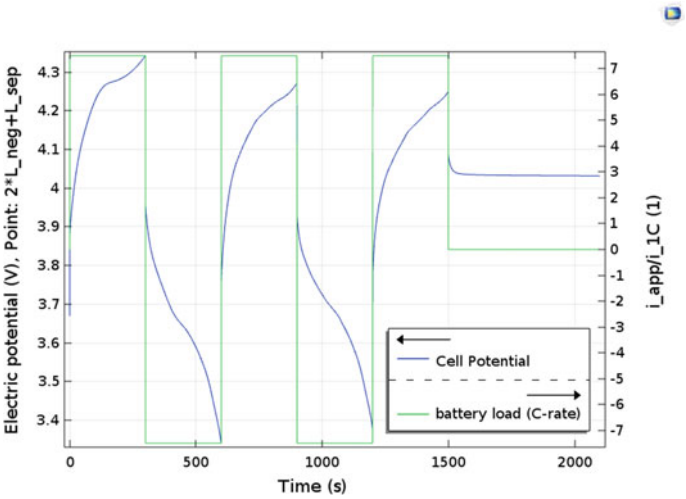

Fig. 7 Cell current, load, and potential during a drive cycle

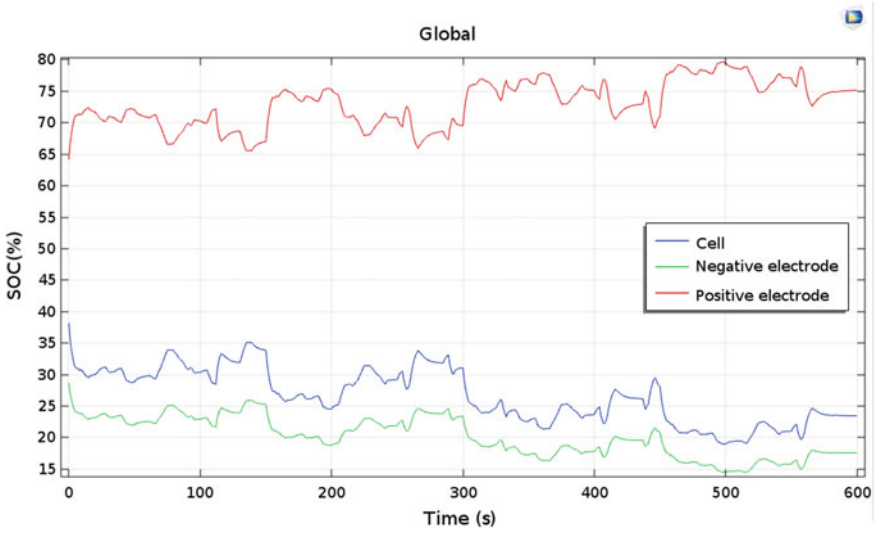

Fig. 8 State of charge (SOC) plots

4.2 Electrical Characterization

During this characterization, a hardware prototype was connected through the NI DAQ card and interfaced with data acquisition software for obtaining real-time data.

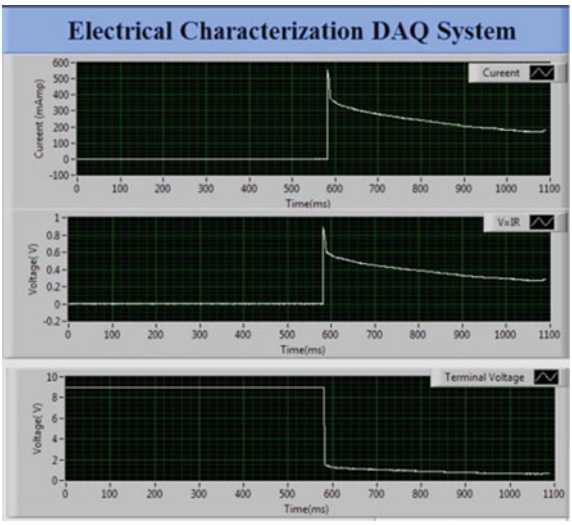

Fig. 9 Short circuit test

5 Short Circuit Test

In this test, an electrical circuit has been connected to evaluate the battery bank characteristics.

This test helps to know the high discharge current as well as also helps to understand the sweeping potential across the circuit. Figure 9 represents the short circuit test characteristics across the hardware prototype. During this test, there is a sudden rise in the current of 515 mA takes place and similarly, there is an increment in voltage drop, i.e., 0.85 V across the resistor of 1.5 Ω in the circuit. Hence, there would be a sudden rise in current due to short circuit tests across the battery bank which would help to know the high discharge current across the circuit.

6 Test with Load and Without Capacitor Bank

In this test, the battery bank has been connected directly to the load (motor) for obtaining the discharge characteristics of the battery. Figure 10 represents the discharge curve of the battery bank in which the capacitor bank is not connected in the circuit. Hence, the maximum current in this situation occurs at 79 mA but after a certain time, the current value starts decreasing till 19 mA.

There is a lot of fluctuation in the waveform, which represents a lot of noise in the circuit. Hence, to overcome this fluctuation in the circuit, a capacitor bank has been connected parallelly in the circuit.

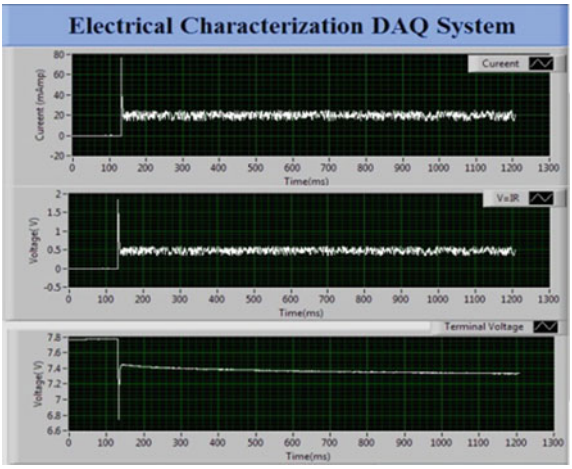

Fig. 10 Test with load and without capacitor bank

7 Test with Capacitor Bank

During this test, the capacitor bank is connected parallelly in the circuit through load and battery banks. Figure 11 represents the discharge characteristics of the battery bank which was connected parallelly with a capacitor bank and DC load.

In this characterization, a sudden increase in current of 150 mA across the resistor has been observed and also fluctuation in the waveform was minimized in the circuit. Hence, it represents a high accelerating current in the circuit.

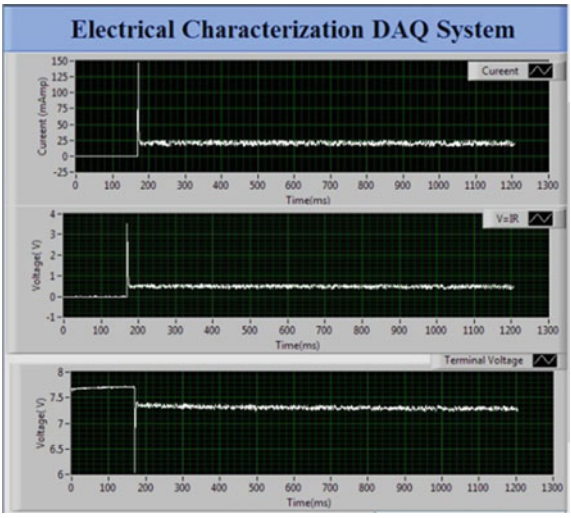

Fig. 11 Test with capacitor bank

8 Conclusion

In this paper, mechanical and electrical characterizations were successfully performed and optimized using the Multiphysics software and hardware prototype with data acquisition software. For the mechanical characterization of li-ion battery, theoretical results were obtained and evaluated which shows better heat management and good polarization capability in the battery. Whereas in electrical characterization, experimental results were carried out with the help of a hardware prototype. The hardware testing results were monitored and evaluated on the software. These electrical results show good electrical behavior and high accelerating current in the hybrid combination circuit.

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Design of Drunk and Drive Detection Device

Gorla Hampika, Vodela Rohit, P. Abhishek, and Guduri Manisha

Abstract Nowadays almost every road accident and deaths caused by road accidents are due to driving after consumption of alcohol. These major accidents and deaths can be controllable by checking vehicles using alcohol detectors by policemen. But this approach is unable to solve the issue of road accidents because police cannot check each and every vehicle. Alas, regardless of remarkable progress, liquor impaired riding remains an extreme country-wide trouble that dangerously impacts many victims per annum. In order to solve this issue, this research article designs an alcohol detection system using Raspberry Pi.

Keywords Raspberry Pi · CCTV · MQ3 sensor · LCD · GSM · GPS · DC motor · Buzzer

1 Introduction

Nowadays, many accidents are going on as a result of the liquor utilization of the driver or the individual who is driving the vehicle. Alcoholic drivers are in a precarious state thus, impulsive decisions are made on the expressway which imperils the lives of road users, the driver comprehensive [1]. The fundamental reason behind this venture is "Drunken driving location". The monstrosity of this risk rises above race or limit. However, strict checking of drunken drivers is a test to the police officers and road safety officers. This restricted capability of regulation implementation operators undermines each and every manual exertion went for controlling drink-riding. There may be consequently the requirement for a programmed liquor area method that can work without the task of life. Consequently, drunken driving is a primary reason for accidents in almost all countries in every unmarked location in the path of the arena [2]. Government must uphold legal guidelines to introduce such features to manipulate all vehicle firms to preinstall such accessories while generating the vehicle itself. Avenue protection is constructing as the most important social problem

G. Hampika (✉) · V. Rohit · P. Abhishek · G. Manisha
Department of Electronics and Communication Engineering, Institute of Aeronautical Engineering, Hyderabad, Telangana 500043, India
e-mail: hampika.g@iare.ac.in

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on this planet over peculiarly in India. Consuming and using is as of now an actual emerge downside, which is often going to rise as one of the vital big troubles in the close to destiny.

The Nigerian Bureau of records printed 11, 363 avenue accidents in 2016. Despite the truth that the file expressed velocity violation because the principal purpose for these accidents, it might probably securely be gathered that almost all of the cases would have been in view that of driver's unstable situation prompted by drivers getting alcoholic before they drive. The investigation performed by using the arena wellbeing institution in 2008 demonstrates that about half 60% of auto crashes are recognized with beverage driving. Our prototype approach coordinates the accompanying apparatus parts in the constitution: A LCD, GSM, GPS, MQ-3, Buzzer, DC Motor and 2- LED's are integrated to a processor of pi3. The process actualized by us goes for reducing the avenue accidents quickly seeing that of drunken driving. The proposed process was once structured and simulated utilizing Proteus VSM simulator. The program code to be burnt into the Arduino board used to be written in Arduino IDE sketch.

2 State of Art

Some of the researchers have been done research on alcohol detection. Some of the authors proposed methodologies as mentioned, in this paper [1] author describes alcohol detection for vehicle by using AT89S51 microcontroller and MQ-3 sensor for alcohol detection as the main component. To alert the person we use Buzzer as an alerting device.

In this paper, [3] author aims to reduce the serial episodes of drunken driver accidents, he proposed IR sensors to absorb IR rays released by Ethanol and relay circuit to control the fuel supply.

In this paper, [4] author implemented Aurduino UNO, alcohol sensor, alcohol detection for drunken driving and GPS is also equipped for the identification of drunken driver location.

In this paper [5] author proposed a drunken driving detection device with Aurduino ATMEGA 328 microcontroller with alcohol sensor to detect blood alcohol content and GSM module with sim slot, GPS for tracking the location.

In this paper [2], author implemented AT89S51 with alcohol sensor for drunken driving detection devices, which avoids drunken driving road accidents.

3 Proposed Device

This system acquires advancement to the current innovation the vehicles and furthermore improves the security highlights, consequently demonstrating to be a strong development in the core organization. Our proposed work contains extraordinary

models that makeup process: power provides unit, the MQ3 detection unit, CC digital cam, the system locking unit, start-up approach, monitoring, alarm unit and an indication as (see Fig. 1). The block diagram illustration of the method has proven underneath (see Fig. 1).

The hardware equipment assembled in this system are Power Supply, Raspberry Pi, Camera Module, GSM, GPS, Motor Driver, DC Motor, LCD, Buzzer and Led's which interfaces with a software. The software tool used is Embedded Linux.

The system distinguishes the presence of liquor and security of ignition of the Car and swiftly locks the motor of the auto. Inside the equal time at SMS alongside, the area of the automobile is sent to three pre-chosen contacts. As a result, the technique lessens the theft and quantum of street accidents, fatalities because of alcoholic utilizing in the future [6]. A viable association is given to build up the wise process for car swap will reveal uncommon parameters of the car within the core of consistent time interval and may ship this advantage to the base unit. The proposed strategy would whole the abilities to speak with the base station by the use of GSM and manipulate one in every of style parameters. The whole manipulate procedure has the improvement of little quantity and high reliability. The future extent of this system is to control the accidents and giving priceless details concerning the unintended automobile, hence diminishing the cost of accidents taking situation seeing that of drunken driving [3].

This manner furthermore integral to look at the security from robbery, ignition, gasoline stage of the automobile, Rain detection and a few protection indications with the aid of way of using outdoor males and females by the usage of unwanted touching while parking the automobile [7]. A liquid crystal show display is probably equipped within the vehicle to transport approximately as an indicator to the reason

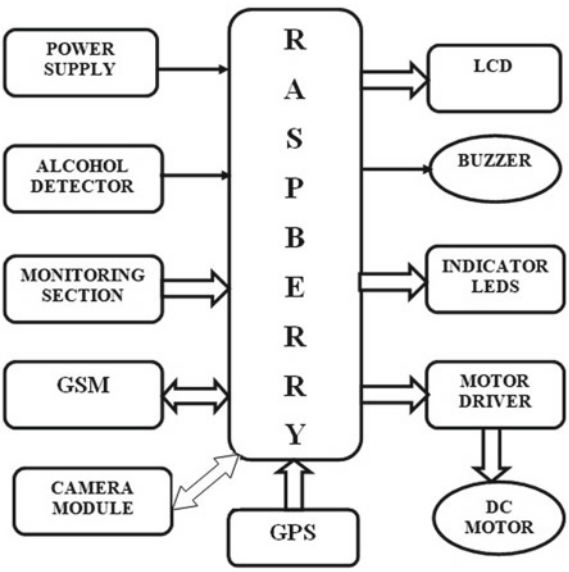

Fig. 1 Architecture of drunk and drive detection device

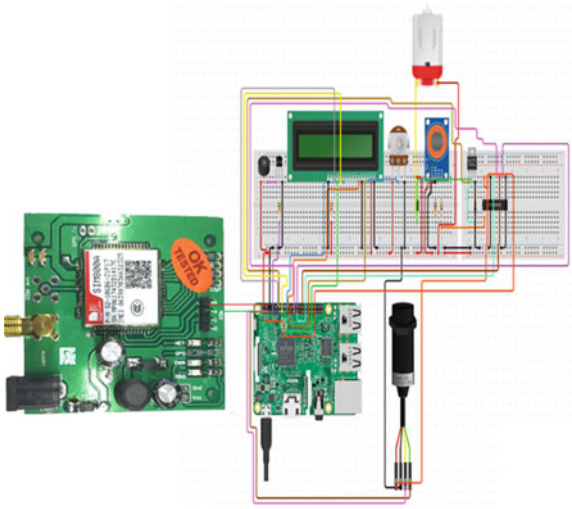

Fig. 2 PCB of drunk and drive detection device

pressure in conjunction with all people inside the car. DC motor is utilized in the auto motor to expose the concept of motor locking system. The Raspberry Pi 3B version microcontroller (see Fig. 3). The organizational set up of Raspberry Pi can be applied to continue shopping for output from alcohol sensor and digital camera module. Additionally, the strategy checks out up to now as viable, then the sensor likely instantaneous the processor in regards to an appropriate voltage [8]. Due to this reality, the technique will thus discontinue the engine and it ships a message to the users. The Linux operating system which is the ecosystem for writing laptop applications is utilized to write down the code, gather, create hex record and load to the controller [4]. The simulation setup for the proposed procedure has been proven (see Figs. 2 and 3).

Fig. 3 Raspberry Pi3 model B board

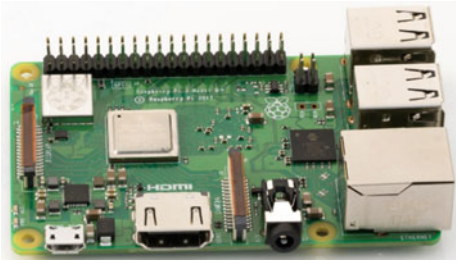

Fig. 4 Raspberry Pi3 model B board

4 Components Specifications

In this section, this research paper discusses the entire hardware of the drunken driver detection device (seen Fig. 2).

4.1 Raspberry Pi Micro Controller

In this device, we have used the Raspberry Pi3 model B microcontroller (seen Fig. 4). The Pi is a series of small board computers advanced within the UK by using the Raspberry Pi foundation. Several generations of Raspberry Pi's had been released. All models feature a Broadcom So, C with incorporated PI-well matched CPU and on-chip GPU (see Fig. 4).

4.2 Monitoring Unit

Sensors are the devices that convert physical quantity into electrical signals. The list of types of sensors used in this system are explained below.

Rain sensor—used to identify the rain present outside the vehicle
Fuel sensor—used to monitor fuel levels in the tank of the vehicle.

Vibration sensor—used to detect the unwanted human being touch when park the vehicle.

Alcohol Sensor—used to detect the alcohol content from driving a person's breath when a person wants to drive after drinking alcohol.

Buzzer
Buzzer is a device that generates beep sound. It requires 5v DC and also interfaced with a BC547 transistor for amplifying the low current into sufficient amplification. The device which is used in this project for alerting when driver alcohol percentage exceeds the threshold limit.

LCD
Liquid Crystal Display, another way it is called LCD, is used to display all alphabets, Greek letters, special characters and mathematical symbols. The most used character-based LCD displays are developed by Hitachi's with HD44780 controller. The available LCDs in the market are 1 line, 2 line and 4 lines.

GSM Module
Global System for Mobile Communication (GSM) is one of the most widely used in wireless sensor technology for communication systems with low cost. It communicates Arduino with 9600 baud rate and supports full-duplex communication. This technology works based on the AT commands. The user or authorized person gets SMS when alcohol sensors detect alcohol content more than limit.

GPS
Global Positioning System (GPS), is used to finding the location it doesn't require any telephonic or internet. This module is compatible with TTL logic and easily communicates with Arduino microcontroller. Whenever a sensor activates the GPS system finding the location parameters and sends those to Arduino microcontroller.

DC Motor
A motor is an electrical device that converts electrical energy into mechanical energy. The DC motor is an electric DC motor that is used to show the idea of motor blocking. Here in this work, the DC motor will connect with the L293d motor controller to the microcontroller, when the alcohol is distinguished, the DC motor stops at another to demonstrate that the alcohol is recognized, the Buzzer will be alert and will continue to function when do not identify alcohol.

Camera Module
A webcam is a digital video, digital camera that feeds or streams its snapshot in actual time to or through a computer to a PC community. The time interval "webcam" (a clipped compound) can also be utilized in its fashioned think of a video dig cam connected to the internet regularly for an indefinite time, as opposed to for a distinctive session, usually delivering a view for all and sundry who visits its web page over the web. Webcams ordinarily comprise a lens, a snapshot sensor, support electronics and might also encompass one or even two microphones for sound.

5 Related Work

The alcohol sensor is used to detect either the person consumed alcohol or not. Drunk driving detection through Iris recognition using Gabor filter which focused on three functions, firstly taking a sample of facial image, this image encodes into a format that is convenient for calculations, finally a signal will control the vehicle through the microcontroller which is connected to the ignition system of vehicle.

$$\frac{\text{Face}_{\text{pre}} - \text{Face}_{\text{post}}}{\text{Face}_{\text{post}}} * 100$$

Even we are having multiple sensors, we need some specific approaches for particular persons, some of the factors are considered as follows:

- Alcohol percentage
- Facial recognition.

As know from experimental research alcohol inflects the emotions of a human. The nature of alcohol on the facial expression of emotion might be high. We have some electronic databases such as PubMed, PsycInfo and Web of Science for our required samples. Choosing samples from databases with some predefined algorithm.

5.1 General Work Flow

In this article referred to, the driving person FACE DETECTION AND RECOGNITION based on alcohol consumption. This article predominantly points to recognizing algorithms such as PCA (main component analysis), MPCA (Multi-linear Principal Component Analysis) and LDA (Linear Discriminant Analysis) under which we recognize an unknown image by comparing it with the recognized testing images previously preserved in the database (see Fig. 5).

The most fundamental detail required is the alcohol content using a wide range of sensors this can also be easily spotted. Depending on the alcohol level the raw data from the alcohol sensor is passed and thresholded. Another parameter discussed in the model is the eye blink rate. Sensors are available for this function such as for alcohol content. Facial recognition, in connection with machine-learning techniques.

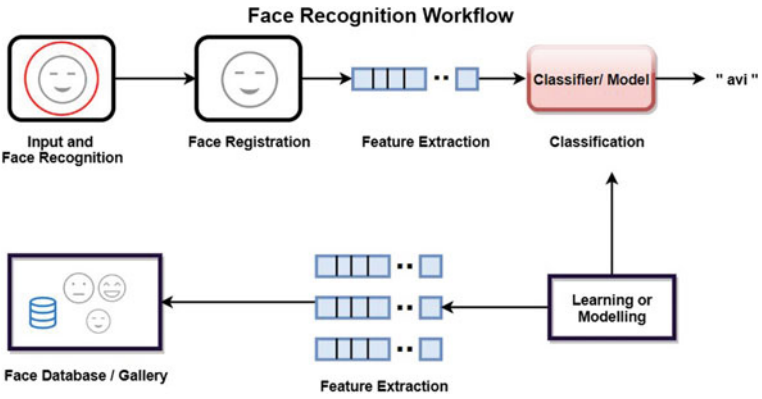

Fig. 5 Work flow of proposed system

Drunk driving detection using neural networks wants to take advantage of a camera to record face images [4]. The images are recorded most often when the engine starts turning on, and also when driving to reduce detection cheating. A fully connected, three-layered neural network system is used to detect whether or not a person is drunken. Neural network is trained to use the back-propagation method by issuing before and before facial photographs (see Fig. 6).

When the drunken drivers enter into the vehicle the alcohol sensor automatically detects and send it to the microcontroller then controller lock the ignition, then the Buzzer will be alert and SMS will be sent to authorized person or some public department. The status of the LCD at alcohol detection (see Figs. 8 and 9).

After alcohol detection, the authorized person has got the SMS from the system (see Fig. 7).

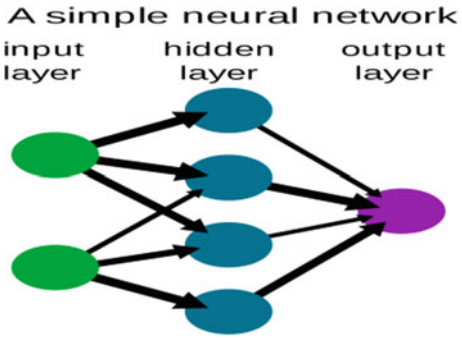

Fig. 6 Neural network

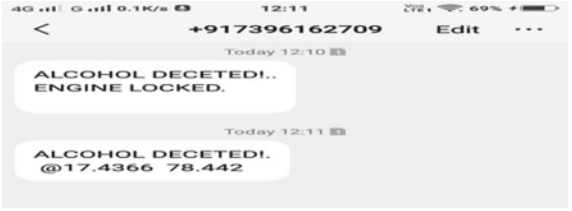

Fig. 7 Message at mobile

Fig. 8 System implementation

Fig. 9 Status of LCD when alcohol detection

6 Results

The LCD display of the system when power is on (See Fig. 8).

Whenever the driver wants to start the engine the camera module at vehicle automatically captures the face of the driver, then sends it to the microcontroller. If the image is authorized then ignition lock has been enabled then engine started.

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An Architectural Overview of Unmanned Aerial Vehicle with 5G Technology

Vodela Rohit, Gorla Hampika, Abhishek Tenneti, and Manisha Guduri

Abstract In the current era, communication has become an essential part of life for basic needs in a man's life and hence this is driving us to see much advancement in those lines. Those advancements are predicted in 5G technology. It is evident from the researchers that, soon 5G is becoming an applicable area in day to day communications. In this paper, a brief discussion on 5G technology and its application in unmanned aerial vehicles (UAVs) is done. A cost-effective UAV architecture with 5G implementation is proposed in this paper. The challenges in this architecture are also discussed. A rural area application with 5G—UAV architecture is also implemented in this research paper.

Keywords 5G network · Architecture · Drone · Low cost · Connectivity

1 Introduction

The 5G communication is expected to be launched very soon and various trial runs and controlled tests are being performed to implement this technology. Once deployed, it has a many advantages which will make it strong over the existing technologies. Theoretically, it is expected to be 100 times faster than the present technology and with the help of this technology, communication speeds up to approximately 50 megabits per second to more than 2 gigabit per second at the beginning. Well, this is the bright side but there are still some hurdles which this technology has to overcome such and one of them is the architecture or the current methodology to deploy this technology of communication. So, we are going to use the miniature drones or UAVs to solve this issue of bulky and stationary mobile towers which are very hard and time taking to install and they are also of very high cost compared to the UAVs we are opting to this method in the rural areas to overcome certain issues. A radio network based on UAVs, in fact, introduces several advantages, including: i) the possibility to cover where the users are located, ii) a general decrease of the installation costs,

V. Rohit · G. Hampika (✉) · A. Tenneti · M. Guduri
Department of Electronics and Communication Engineering, Institute of Aeronautical Engineering, Hyderabad, Telangana 500043, India
e-mail: hampika.g@iare.ac.in

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thanks to the fact that multiple UAVs can share the same ground site to recharge themselves and to exchange data with the core of the network, and iii) the adoption of short-distance Line-of-sight (LOS) communication channels between the users and the UAV covering them [1].

To solve this problem, in this article, we learn the design of a low-cost 5G architecture, where the 5G base stations (BSs) are on board of unmanned aerial vehicles (UAVs). The role of UAVs to provide radio connectivity is accepting considerable notice from the research community (see, e.g., [2–5]) Using this method, we are going to show an effective and a cheaper architecture of the 5G network.

In the near future, 5G is the ruling technology and provides a vast wide area connectivity [6]. There is no surprise that 5G technology becomes easily accessible in urban and developed areas. The scenario is quite different when it comes to rural and under-developed areas, because of less number of users (demand and supply rule) and accessibility issues. 4G is an efficient technology but it has its own limitations which the 5G is going to overcome as greater speeds can be achieved and the number of users can be increased and latency is reduced, bandwidth provided is greater than 4G and it also consumes very low power. 5G frequency ranges from 600 MHz to 6 GHz [7].

We focus on the main problem which is to provide the 5G network in the rural areas with low cost and greater efficiency. Due to high density in urban areas, the cost of establishment of 5G base band networks is easier compared to rural areas. This problem in rural areas can be overcome by opting drone-based architecture which we are going to propose. Wireless communication by leveraging the use of unmanned aerial vehicles (UAVs) has attracted increasing interest recently [7].

2 UAV—Architectural Overview

We review the UAV-based 5G architecture, based on the reference architecture of [8, 7]. Here, we are going to form an effective and reliable architecture using the UAV which means that we are going to place our base stations on these UAVs and let them hover a particular area which is enough to cover a whole village within a square kilometer; we require not one but a decent number of drones here to form a network. While the drones are hovering overhead, they are in sync with the ground station, i.e., the stationary base station which provides the link to users and the network. All the UAVs are fixed to hover at a constant height and are synchronously flying; their job is to provide an area where the communication can take place and to maintain radio connectivity.

To provide 5G connectivity, a maximum distance restriction between the UAV covering the area and the site where it is connected through a radio link must be guaranteed. This is an essential condition for maintaining radio connectivity between the low-level features that fly in the UAV and resolve the power issue and they will not even have any obstacles as they fly at a decent amount of height in the sky which makes it easier to expose the solar panels to the sunlight. Each drone covers a territory

and a group of these can cover a very large area very easily. These sites where the drones will be hovering need to be planned and placed during the planning phase of the architecture; we have to make sure that one of the UAVs covers the sufficient amount of area and we also must make sure that they are in the proper range from the control base station and as these are not stationary; these base stations are portable and can hover or fly from place to place if required which is one of the biggest advantages of using the UAV-based architecture. High-level ones are placed at the ground sites [7]. These UAVs need to be recharged in order to operate and fly; so, to solve that issue, we are going to use a renewable source which is the sun and is available for a good time for the UAVs to charge and operate and also to store the power for operating during the night time. So, we use the solar panels on these UAVs and drones too. Energy-efficient operation, on the other hand, aims to reduce unnecessary energy consumption by the UAVs. As the main energy usage of UAVs in wireless applications is to support either aircraft propulsion or wireless communications, energy-efficient operation schemes can be broadly classified into two categories. The first one is energy-efficient mobility, for which the movement of the UAVs should be carefully controlled by taking into account the energy consumption associated with every maneuver [9].

3 Proposed Architecture

We considered a rural area near Dundigal which is situated at the outskirts of Hyderabad city where the reception of cellular networks with the regular architecture is very low and we plan to set up our architecture in this particular area in order to do that we need to hover the UAVs over the area as they cover up the desired territory and fly there in a fixed position as they form a cluster and are controlled by a control station on the land. The UAVs contain an on-board Base station which helps in the uplink and downlink for the users and all these UAVs are in range with the control station and the users who seek for the communication must be under these UAVs. These UAVs are spread such that they cover the whole desired area and we must take care that no UAVs are overlapped or interfered with each other as we set up these UAVs at a fixed point now it is up to the control station to control these UAVs and to make sure are all synchronized and are in the ideal position now when the UAVs are set we need to focus on the control station which consist of the basic control station circuitry which is fixed at point which is suitable and in range with all the UAVs order to function. Today, especially in remote locations, a number of BSs already operate with no connection to the power grid. The most common solution to power off-grid base stations consists in installing a Diesel power generator, which requires large amounts of fuel, which is expensive in itself, but becomes extraordinarily costly when transport is problematic (helicopters are necessary when locations are really remote), and when fuel thefts occur [10]. This issue can be resolved by using solar power as the primary source of energy for the establishment.

We also consider the main factor for the UAVs to remain stable in the air, and for that, they need a good supply of energy from the battery so it will be a little difficult and inefficient for the UAVs to come back on the ground and charge for a while so to avoid that, we also propose a method which will keep the UAVs in the air and also charge at the same time and that is by placing a solar power-based circuit onboard which will charge the battery mid air without any interruption for the formation of UAVs so eventually after serving their time in the air they return back to the charge point.

So in order to establish the perfect communication for the users, the UAVs can be set as shown in Fig. 1. We plan on setting up them over the village in that manner, and the control station somewhere in the middle and that is how the UAVs are able to provide the connectivity to the users they need to be in sync with the other UAVs. In Fig. 1, we show a basic architecture which is required to set the network with decent efficiency and minimal cost. The basic architecture can be seen in Fig. 2 and there we can see the basic architecture of the network.

We discussed earlier about the cost of the installation of the sites and other circuitry with the information about the cost estimation is mentioned in the following table as

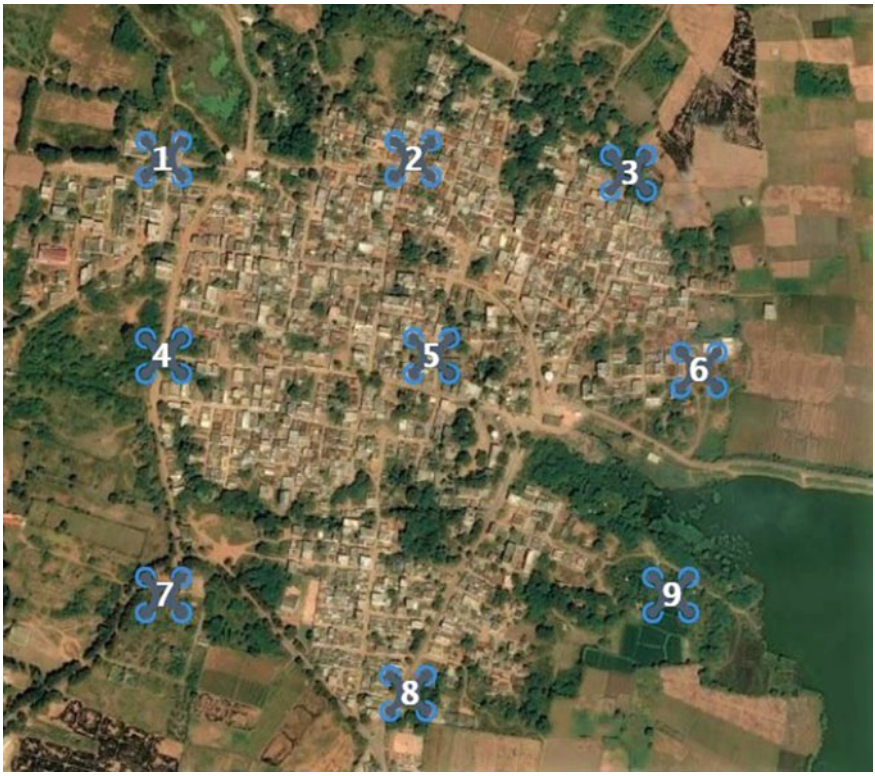

Fig. 1 Arrangement of the UAVS over the village to form a cluster

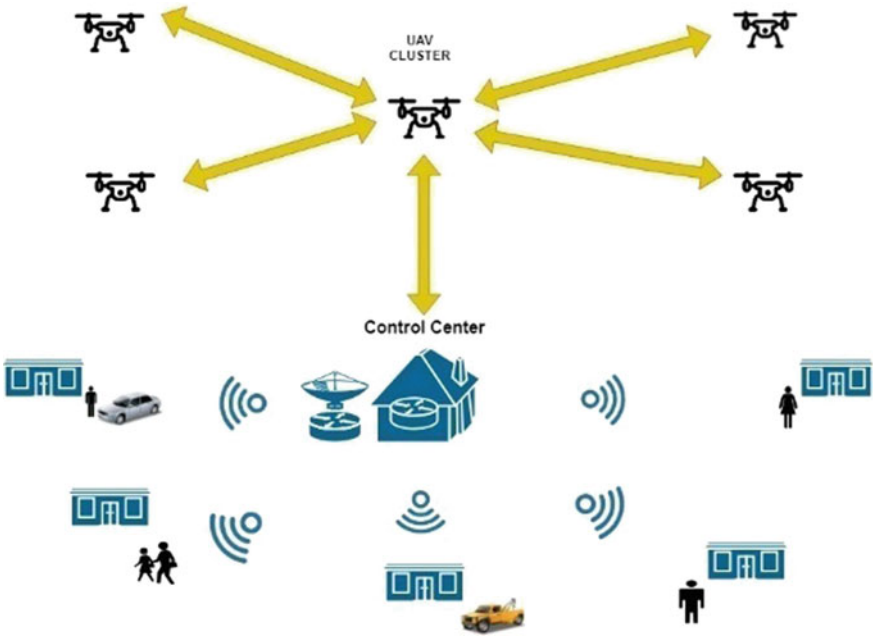

Fig. 2 Graphical representation of UAV-based architecture

Table 1 Cost estimation

Type	Traditional architecture cost	Uav's cost
Close range	30–40 lakhs	10–20 lakhs
Long range	90–150 lakhs	50–80 lakhs

shown in Table 1. The below table shows us the difference in the cost for installing a traditional tower-based architecture and the UAV-based architecture. This simply says that, our proposed UAV architecture is cost effective as well as efficient when compared to traditional architecture. This proposed architecture is implementable in rural areas where the signal strength is poor. This proposed UAV architecture efficiently utilizes 5G technology to overcome existing issues and improvise the communication range.

It is also observed that, the proposed UAV architecture is quite simple when compared to traditional architecture.

4 Conclusion

This research paper concludes by proposing UAV architecture with 5G technology. The proposed UAV architecture is proved to be cost effective with high efficiency. It is also seen that, the proposed UAV architecture is applicable in remote areas.

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Interstellar Space Travel Using Nuclear Propulsion

Abhishek Tenneti, Gorla Hampika, Vodela Rohit, and Manisha Guduri

Abstract This paper discusses Nuclear Fuels for Propulsion which then opens up an entirely new branch and application of nuclear fuels that improves conventional fuels used for interstellar space travel, which has future scope in aerospace.

Keywords NTP (Nuclear thermal propulsion) · NEP (Nuclear electrical propulsion)

1 Introduction

Nuclear Propulsion is the process of using nuclear fuel as a propellant to provide a thrust for the rocket.

Generally, the propellants used for rockets during space travel/lunar travel are Liquid Hydrogen and Liquid Oxygen. Though it seems to be a better fuel, there exist many drawbacks which became more prominent in recent days like storage, maintenance and efficiency. The equipment required to store these fuels are very costly and are highly sensitive to change in temperature and pressure and also g value ($g = 9.8$ m/s^2). If there exists a small leak in the storage tanks, the chances of the rocket to reach/complete mission will be very low and in fact, the rocket will not even cross the earth's atmosphere and might eventually explode up in the initial stages.

Apart from these problems, the thrust produced by these conventional fuels is very low, in the order of 1–4 g. The U.S Government officially began to work on the interstellar space travel using nuclear fuel, which was led by Dr. Ted Taylor of General Dynamics and physicist Freeman Dyson in the year 1958 at Princeton [1].

The project was named Project ORION which was an idea to create an interstellar spacecraft that could travel to the nearest galaxy, Alpha Centauri within 30 years. The main engine of the rocket will be a nuclear reactor comprising of control rods,

A. Tenneti · G. Hampika (✉) · V. Rohit · M. Guduri
Department of Electronics and Communication Engineering, Institute of Aeronautical Engineering, Hyderabad, Telangana 500043, India
e-mail: hampika.g@iare.ac.in

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moderators, etc, which will help control the nuclear reaction and prevent it from an uncontrollable chain reaction.

The nuclear reaction, when initiated will produce a heat that is then directed to Liquid Hydrogen propellant will produce thrust in the magnitude of 1000 g, which can be controllable by limiting the flow of propellant. The remaining heat will be directed to water sinks which convert the heat to steam which is then passed through various filters that remove various noble gases and various other byproducts obtained in the reaction.

The energy produced will be used to run many operations on the ship including life support system, detection and removal of CO_2 gases produced during respiration, Artificial Gravity maintenance and many more systems. The general time required to reach a celestial body near us, like Mars is nearly 850–900 days which is very long and may have side-effects on the crew like micro-gravity, cosmic radiation and many more [2].

Using nuclear fuel, the travel time will be significantly reduced by 500 days, i.e. the total time will be nearly 300 days [1]. In any given duration, the time taken to return home will also be 300 days and there will not be any fuel wastage to course-correct in special/extreme cases. The crew needn't limit their exploration to outer orbit only, which enables in further expedition and research.

2 Classification of Output Power

The output power of the nuclear reactor is generally classified into two types which are as follows:

2.1 Nuclear Thermal Propulsion

The heat produced from the nuclear reaction will be used to propel the rocket in the desired direction.

2.2 Nuclear Electric Propulsion

The energy produced from the nuclear reactor is converted to steam, and then it is used to move the turbines which produce electric energy, which in turn is used to propel the rocket.

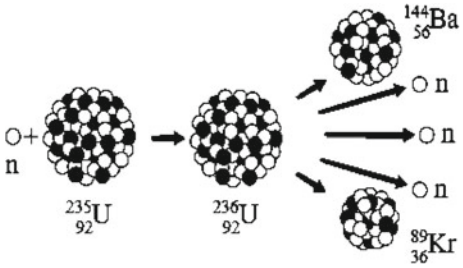

Fig. 1 Nuclear fission reaction of U-235 nucleus

Table 1 $I_{SP}/T/W$ ratio of different reactors [3]

Type	I_{sp}	T/W
Chemical (H_2/O_2)	400–500 s	50–75
NTR-solid core	500–1000 s	1–20
NTR-gas core	1000–6000 s	1–10
NEP-ion thruster	2000–10000 s	$\ll 1$
NEP-hall thruster	1000–5000 s	$\ll 1$
NEP-MEP thruster	1000–8000 s	$\ll 1$

3 Basic Process Occurring in the Nuclear Reactor

From (Fig. 1), it is evident that a large amount of energy (Nearly 190 Mev) is being released from the reaction occurred, thereby giving our system the thrust it needs for take-off.

The characteristics of the energy parameters released and utilized are as follows:

Heat Energy = 0.023 Mev/nucleon (0.558 W/g Pu-238)

Natural Decay Rate = 87.7-year Half-life used terrestrially over 70 years.

Heat Energy = 0.851 Mev/nucleon.

The fission of 1 kg of Uranium-235 yields as much energy as 2.70,000 kg of Coal.

Thrust directly related to thermal power of reactor: 100,000 N ≈ 450 MW (Th) at 900 s.

Specific Impulse is directly related to exhaust temperature which will be 830 ~ 1000 s (2300–3100 K).

Specific Impulse improvement over chemical rockets due to lower molecular weight of propellant (exhaust stream of O_2/H_2 engine actually runs hotter than NTP) (Table 1).

4 Components of NERVA Reactor Engine

N.E.R.V.A (Nuclear Engine for Rocket Vehicle Application) is the engine which we are using to power our rocket for Interstellar Travels [5].

Fig. 2 KIWI test reactors

It is basically a nuclear reactor consisting of all the essential equipment like Control Rods, Moderators, Coolants and other stuff as shown in Fig. 2.

There were many models of prototypes build, out of which only a few were successful, after many simulations.

5 Successful Test Attempts

Previous reactor is modified and is the final design after a series of design analysis tests.

In order to make the engine feasible for the proposed application, the scientists of the United States were finding and developing prototypes which were an approximation of actual engine. The testing sequence was called KIWI tests [5].

The various test reactors being designed are given.

On September of 1964, the eight of the NERVA reactor tests were successfully completed making it the only reactor to be built for space-crafts to explore deep space missions conducted by N.A.S.A.

6 Total NTP Exhaust System

In this module, different components are like engine containment, Nuclear Thermal engine, water cooling module, heat exchanger, water tank, post-test module, etc. In Fig. 3, example of some modules are shown below: Nuclear thermal engine is shielded by strong shields. As NTP produces heavy heat, it needs multi-stage cooling system.

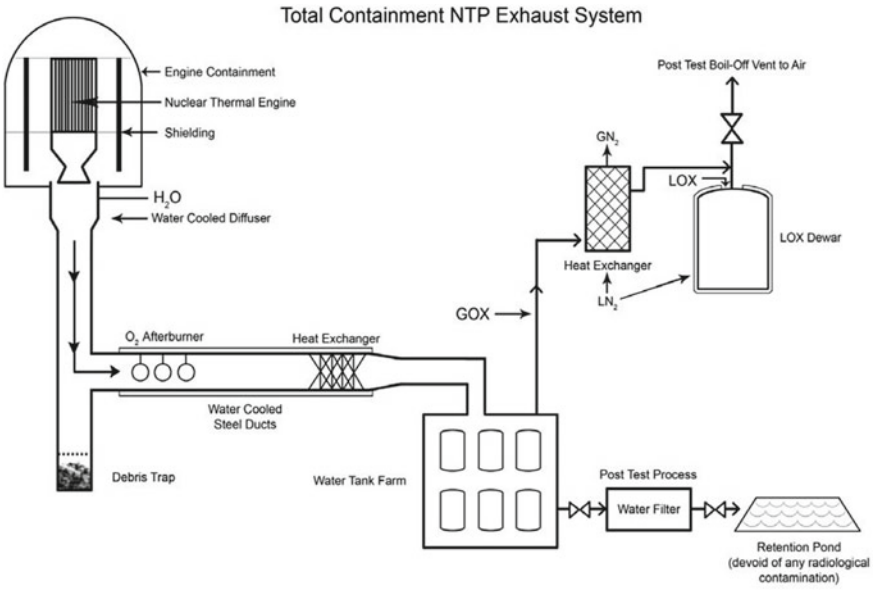

Fig. 3 Some components of containment NTP exhaust system

7 Working

The hydrogen exhaust from the engine flows through a water-cooled diffuser that transitions the flow from supersonic to subsonic to enable stable burning with injected LO_2 which also reduces the heat of the exhaust [4].

Byproducts include steam, excess O_2 and in minor amount, a small fraction of noble gases (e.g. xenon and krypton). Water spray and heat exchanger will be used to dissipate the heat from steam/O_2/noble gas mixture to lower the temperature and steam condensation.

Water tank farm collects H_2O and any radioactive particulates of high-risk factor present inflow. Drainage/Residuals are filtered post-test.

Heat exchanger cools the residual gases to very low temperatures (freezes and collects noble gases) and condenses O_2. LOX Dewar stores LO_2, will be drained during post-test via boil-off.

8 Different Types of NTP Rockets

1. Solid Core Nuclear Rocket

   See Fig. 4.

2. Liquid Core Nuclear Rocket

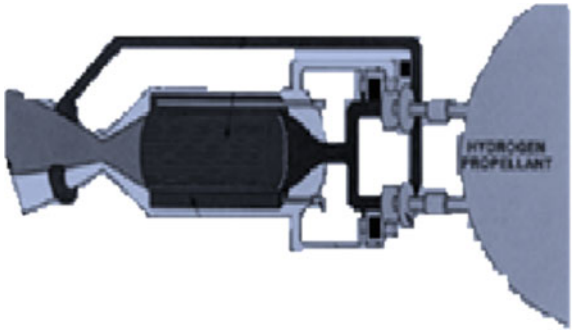

Fig. 4 Solid core nuclear rocket

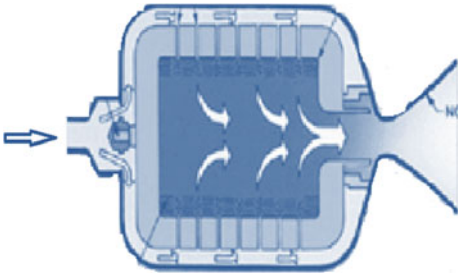

Fig. 5 Liquid core nuclear rocket

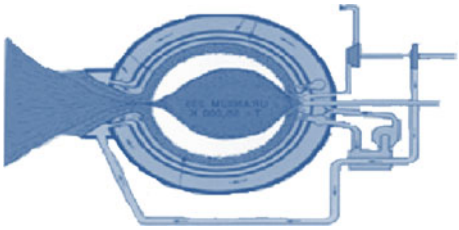

Fig. 6 Open cycle gas core nuclear rocket

See Fig. 5.

3. Open Cycle Gas Core Nuclear Rocket

   See Fig. 6.

4. Closed Cycle Gas Core Nuclear Rocket.

   See Fig. 7.

9 Data Sheet of Power Output for Various Fuels

Un-alloyed U reduces mass, but adds low/modest risk in fuel performance and is different than KRUSTY fuel.

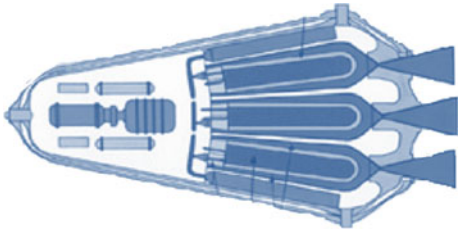

Fig. 7 Closed cycle gas core nuclear rocket

Table 2 Comparing the I_{sp} and T/W of chemical propulsion to multiple nuclear systems [3]

Parameter	Chemical(H_2/O_2)	NTR-solid core
Payload mass	100 tonnes	100 tonnes
Travel time	1 year	1 year
Mission delta-V	7.7 km/s	7.7 km/s
I_{sp}	500 s	1000 s
Mass ratio	*4.806*	*2.192*
Structural mass	*25 tonnes (c = 0.05)*	*15 tonnes (c = 0.10)*
Propellant mass	*475 tonnes*	*137 tonnes*
Total initial mass in LEO	*600 tonnes*	*252 tonnes*
Payload fraction	*0.167*	*0.397*

The U2rh mass shown is extremely optimistic-neutronically ideal [entire core in single can] and H_2 is 10x less than previous estimates; more importantly, development time/cost/risk will be substantially higher (Tables 2 and 3).

Where,

C-1 = Fuel Weight, C-II = BeO (Beryllium Oxide), C-III = Reactor Component Weight, C-IV = Neutron Shield Weight, C-V = Gamma Shield Weight, C-VI = Power Converter Weight, C-VII = Heat Rejection Weight.

Table 3 Explaining the weight table of 10 KWe kilo power MARS ISRU demo [3]

Fuel type	C-1 (kg)	C-II (kg)	C-III (kg)	C-IV (kg)	C-V (kg)	C-VI (kg)	C-VII (kg)
U7Mo-HEU	20	100	40	400	20	390	310
U7Mo-LEU	390	300	200	580	20	390	300
U-LEU	300	300	190	550	20	390	300
U2rh-LEU	100	300	180	500	200	410	400

10 Why Nuclear Fuels for Propulsion

The fuel allocation for various tasks will be efficient without requiring any additional fuel when compared to other fuels.

The crew will be protected by cosmic radiation and micro-gravity effects.

The energy provided will be highly pure and needn't be converted/filtered for usage.

The main advantage is that we won't be requiring Highly Enriched Uranium, but we can also use Low Enriched Uranium, which also provides a nearly equal amount of thrust.

11 Conclusion

Nuclear fission will lead us to an era of marvelous scientific advancement which might even open doors to a new division of science unexplored by us and might provide solutions to many of our crises.

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IoT-Based Real-Time Application of Tilt Sensor for the Pre-warning of Slope Failure—A Laboratory Test

Guntha Karthik, Gopal Sharma, and Singam Jayanthu

Abstract A slope failure is an occurrence in which a slope collapses suddenly due to internally damaged self-retainability because of geological disturbance in the earth's crust. Because of this, the people who are working on the slopes are failing to escape before identifying failure. Though it is not achievable to stop the slope failures by this integrated design, this design can give the pre-warning for slope failures. The project aims to capture the slope movements through the accelerometer sensor. The captured readings from the sensor are transferred to the server through the integrated system, which consists of sensors, microcontroller (Arduino), and Wi-Fi module (ESP-01 module), which works as a communication medium and it was used to integrate the device to the Internet. The received data from the installed integrated system are continuously plotted in an open-source Internet of things (IoT) service provider displayed through the ThingSpeak software.

Keywords Slope failures · Wi-Fi module · Accelerometer sensor · Arduino · ThingSpeak software

1 Introduction

Due to the geographical conditions and the changes occurring in the climatic conditions like the heavy rainfall and the earthquakes, the landslides or slope failures occur [1]. The movement of the slopes can be either upward or downward direction. There are specific causes of these slope failures. The steeper slope is the primary cause of the instability of slopes [2]. The natural tendency of the steep slopes is to move the materials downwards [3]. The excess amount of water in the slopes is hazardous, and it leads to the instability of the slopes. Loss of vegetation at the slopes is also the

G. Karthik (✉) · G. Sharma
Stanley College of Engineering and Technology for Women, Hyderabad, India
e-mail: gunthakarthik@rocketmail.com

S. Jayanthu
Department of Mining, National Institute of Technology Rourkela, Rourkela, Odisha 769008, India

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cause. As the vegetation is more, the strength of the slope increases. Human-made things are also one of the reasons for the slope failures. The building of the roads, blasting the humans' leads, made that to the slope failures. So, an effective monitoring system [4, 5] is required to detect the slope failures in advance and to alert the people and also reduce the loss of human life. The main concern of the research work is to make a slope failure monitoring system by taking readings with the minimum required components and with high efficiency. The analysis of accidents in open-pit mines has revealed that slope failure and dump failures have upward trends in recent times [6]. List of few examples of fatal accidents involving slope and dump failures from 2000 to 2017 are mentioned in Table 1.

Table 1 Few examples of fatal accidents involving slope and dump failures in Indian OC mines [10]

L. No	Date	Name of mine	Incidence	Fatalities/damages
1	24.06.2000	Kawadi OC mine of M/s Western Coalfields Limited (WCL)	Slope failure of 31 m high OB benches	10 workers
2	09.12.2006	Tollen Iron Ore Mine, M/s Kunda R Gharse in Goa	Failure of slope 30 m to 46 m high dump	06 workers
3	17.12.2008	Jayant OC Project of M/s Northern Coalfields Limited (NCL)	Failure of dragline dump	05 workers 01 shovel buried
4	04.06.2009	Sasti OC Mine of M/s WCL	Dragline OB dumps of 73 m height failed and slided down the pit	02 workers 02 excavators buried
5	25.02.2010	Hansa Minerals and exports Granite Mine	Granite mass slided along an inclined joint plane and failed from height varying from 10 to 55 m	14 workers
6	22.06.2014	Amlai OC Mine, M/s South Eastern Coalfields Limited (SECL)	Dump failure due to sudden development of cracks in the embankment and unstable ground conditions	2 workers 1 dumper 1 dozer 1 crane
7	29.12.2016	Rajmahal OCP of M/s Eastern Coalfields Ltd (ECL)	Dump failure due to the development of cracks and unstable ground conditions	25 workers 12 tippers 6 excavators and 1 dozer
8	1.12.2017	JunaKunada OC Mine, Majri Area, WCL	Slope failure due to the development of cracks and unstable ground conditions	3 excavators 8 dumpers 1 dozer 1 service van

2 Methodology

The methodology of the integrated system in the form of the flowchart is shown in Fig. 1. Generally, in India, there is a problem of slope failures in the hilly areas and opencast mines [7]. To provide some amount of solution to this problem, we designed a system in which we measure the elevation values by using the accelerometer sensor. The recorded values are sent to the cloud using the ESP01 Wi-Fi module, and the

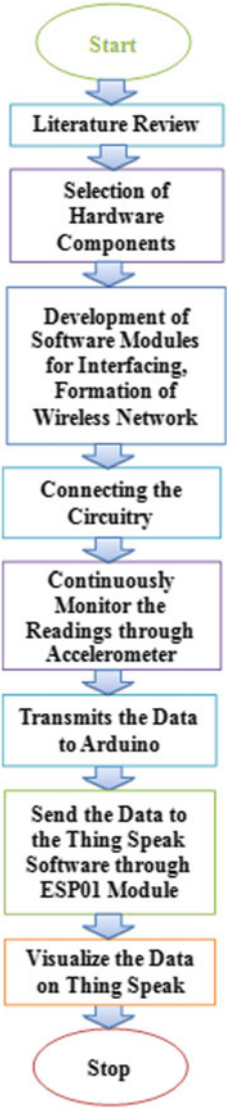

Fig. 1 Flow diagram of the integrated work

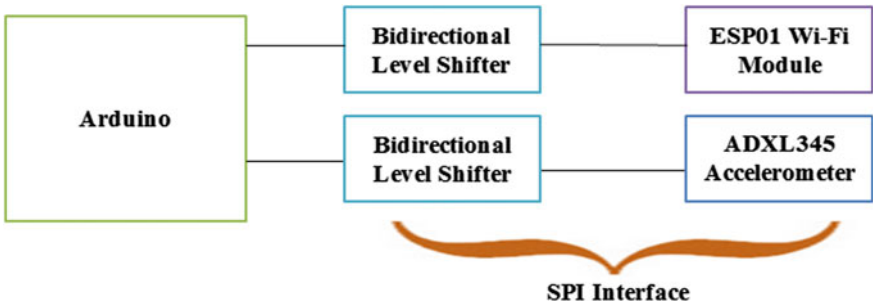

Fig. 2 Block diagram of smart tilt meter

data was displayed in the ThingSpeak software. The block diagram for the smart tilt meter is shown in Fig. 2.

3 Hardware Design

The hardware design consists of tri-axial accelerometer, Arduino microcontroller, logic level convertor, and Wi-Fi module. In the design, the microcontroller was interfaced and programmed with sensor and communication modules to monitor the ground movements. The hardware programming was done using embedded C language and simulated and transferred using Arduino IDE software. Figure 4 shows the hardware connections of the integrated system.

3.1 Tri-Axial Accelerometer (ADXL 345)

ADXL345 is a small, thin, low power, high resolution of 13-bit, and measurement at up to ±16 g. ADXL345 has a digital interface supply voltage. It has the ground pins, reserved pins, and interrupt pins. ADXL345 is accessible through either an SPI or I2C digital interface [8]. ADXL345 is accessible for mobile device applications. It measures the static acceleration and dynamic acceleration components of gravity in tilt sensing applications resulting from motion or shock [9]. As shown in Fig. 3, the accelerometer sensor identifies the vibrations from its surroundings.

3.2 Arduino

Arduino UNO microcontroller is an electronic platform that has an open-source hardware and software interface. The operation of the Arduino microcontroller is as

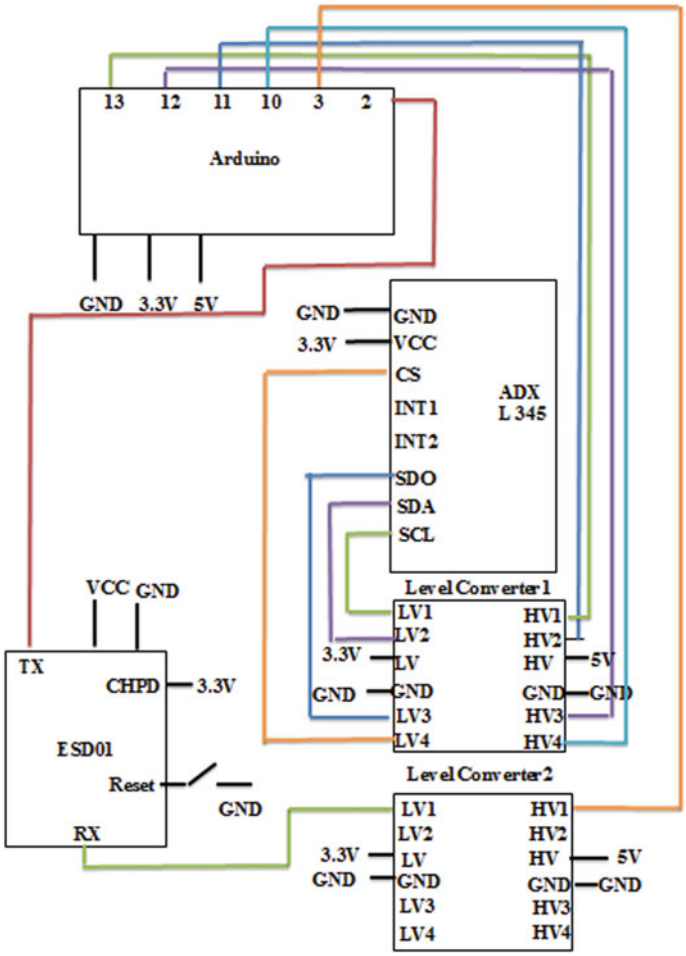

Fig. 3 Connection diagram of integrated system

simple as transferring the instruction into it and acquiring the required output. The main features of Arduino microcontrollers are available at low cost, its flexibility, and open-source IDE for the users. The Arduino acts as the communication and processing medium between the tilt sensor and the RF module that transfers the data that was given by the tilt sensor, as shown in Fig. 3.

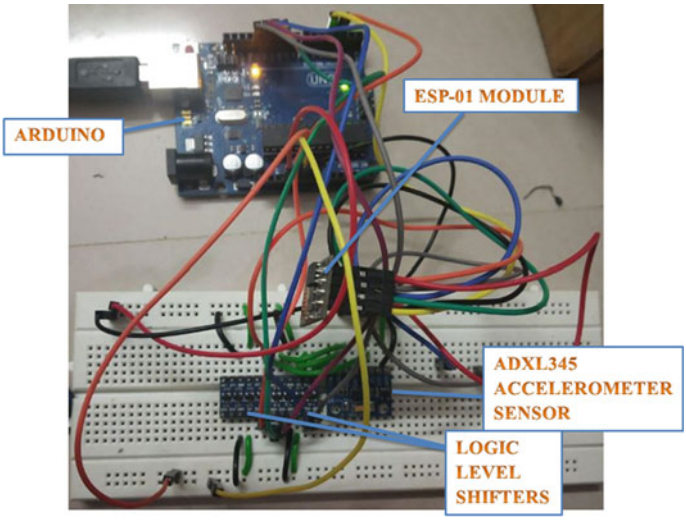

Fig. 4 Hardware connections of an integrated system

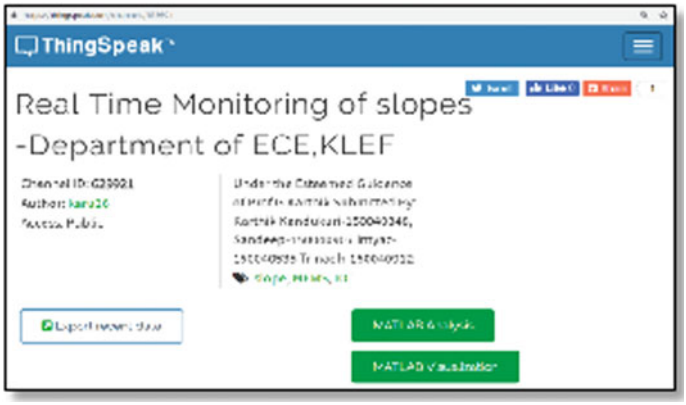

Fig. 5 Developed GUI through in ThingSpeak software

3.3 Logic Level Converter

The logic level converter is also called the level shifter or the level translator, which is a small circuit that converts the 5 V signals to 3.3 V signals and also converts vice versa. The level converter has the capability of converting four pins on the high side to 4 pins on the low side. Of the two sides, each side contains two inputs and two outputs. Apart from its flexibility to use logic level converter does not work with an analog input. The board needs to be powered up from the two voltage sources, i.e., high voltage and low voltage. High voltage is connected to 'HV' pin, and the low

voltage is connected to 'LV' pin (high voltage means around 5 V, and low voltage means about 3.3 V).

3.4 Wi-Fi Module

The Wi-Fi module (ESP-01) allows the access of microcontroller to the Wi-Fi network. In the integrated work, this module has the capability of integrating all the components of the system since it has a system on a chip (SOC). This module does not need a separate microcontroller to manipulate the inputs and outputs because ESP-01 itself acts as a small microcontroller. It is possible to have up to 9 general purpose input/output (GPIOs) depending upon the version of ESP8266. By using these GPIOs, we can able to give microcontroller Internet access like the Wi-Fi shield to the Arduino. By using these GPIOs, we can also be able to program the ESP8266 as a microcontroller with Wi-Fi enabled.

4 Software Module

ThingSpeak is a cloud platform that provides various services, particularly for building IoT applications. ThingSpeak is used to visualize the collected data from the host as charts, graphs, and it also can create plugins, apps to collaborate with external Web services, APIs. There are eight fields in ThingSpeak platform for storing data of any type. In the integrated work, these fields are used to store the data from the sensor module. In the included work, there are three location fields in which we store the latitude, longitude, and elevation, from the tilt sensor. It also consists of one status field, which a short message to describe the data stored in the channel. We integrate any Internet-connected device with ThingSpeak. In the integrated work, we are sending the sensor data from the host microcontroller and Wi-Fi bridge (Fig. 4).

5 Results and Analysis

The laboratory test was conducted in the communication system laboratory of K L University by giving manual tilting inputs to the sensor. The output graphs are observed and were developed GUI during the test, as shown in Fig. 6. Results can be accessed at any time by using the following link: https://thingspeak.com/channels/629921. The accelerometer sensor has calculated the three axes (roll, pitch, yaw) of the elevation for the slope change. If the elevation is very minute, there is no change in the readings and axis values of the accelerometer. If the precision is more (e.g., more than one degree), there is a change in readings and axis values. The reading is displayed visually by using the software known as ThingSpeak, as shown in Fig. 6,

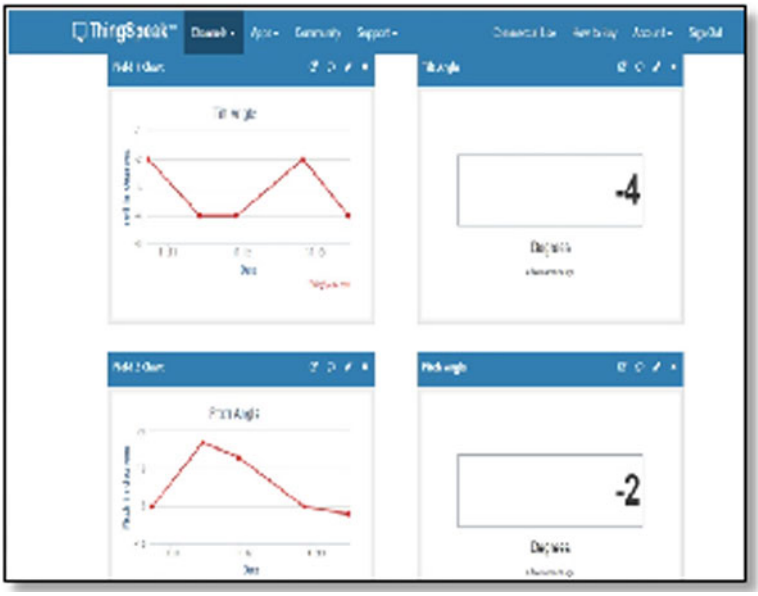

Fig. 6 Representation of real-time data from accelerometer in ThingSpeak software

in which, along with the readings, the plots of the tilt angle and the pitch angle are also displayed, and the data is saved in the cloud. The working of the system is as follows: The system continuously monitors the readings. The values recorded in the accelerometer sensor were sent to the ThingSpeak software through the ESP01 Wi-Fi module. The visualization of data can be accessed in ThingSpeak software (Fig. 5).

6 Conclusion

Real-time monitoring of terrain surface is one of the challenging research areas. Hence, the paper discusses the development of a system that the readings and the system plot about the elevation of the particular objects, which is useful for landslide detection. This system uses the accelerometer sensor that senses the movement of the object, an ESP01, which is a Wi-Fi module used to send the recorded data to the cloud, and the ThingSpeak software, which is used to visualize the data in the form of graphs and values. The integrated system is useful for landslide detection and monitoring. The further up-gradation of the system can be done by installing the integrated system in two or three landslide-prone areas.

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Optimizing the Random Offset Voltage in Two Stage Amplifier Considering Noise-Power Trade-off Using HWPSO Algorithm

N. M. Laskar, Koushik Guha, K. L. Baishnab, P. K. Paul, and K. Srinivasa Rao

Abstract In this paper, the new Hybrid Whale Particle Swarm Optimization (HWPSO) algorithm is employed in minimizing the random offset voltage in a two stage Operational Amplifiers. Random offset voltage arises in due to transistor mismatch and imposes a restriction on the precision of specifications such as Gain, CMRR etc. obtained using the amplifier. This is more significant in case of low frequency applications such as in Neural or Biomedical. In order to minimize random offset an inherent tradeoff with the circuit area has to be met. Additionally, one of the prime requirements for these low frequency amplifiers is the need of low power as well as low noise. A specialized design approach is used as design constraint in this work to achieve a striking balance between these two design specifications i.e. Noise and Power while minimizing the random offset. Simulations are performed and comparative analysis illustrated that the HWPSO algorithm outperforms other state of art algorithms by giving a minimum random offset voltage of 1.638 mV with a circuit area of 3.51×10^{-9} m^2. An optimal input noise of 28.24 nV/$\sqrt{}$Hz and power of 3.12 mW is obtained. Validation of HWPSO results have been done by performing simulations in Cadence Virtuoso, which are found to be in close agreement with the algorithmic results.

N. M. Laskar · K. Guha (✉) · K. L. Baishnab · P. K. Paul
Department of Electronics and Communication Engineering, National Institute of Technology Silchar, Silchar, Assam 788010, India
e-mail: koushikguha2009@gmail.com

N. M. Laskar
e-mail: naushad.0015@gmail.com

K. L. Baishnab
e-mail: klbaishnab@gmail.com

P. K. Paul
e-mail: pkp059@gmail.com

K. Srinivasa Rao
Department of Electronics and Communication Engineering, KL University, Guntur, Andhra Pradesh, India
e-mail: srinivasakarumuri@gmail.com

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Keywords Hybrid metaheuristics · Pelgroms model · Random offset voltage · Noise-power tradeoff · Low frequency applications

1 Introduction

In operational Transconductance Amplifier design (OTA), offset voltage is a very important design specification. High Offset voltage is undesirable because it impacts the accuracy and precision of other design parameters such as Gain, CMRR etc. in the amplifier [1]. Especially in case of low frequency systems such as Biomedical or Neural Amplifiers, as the signals themselves are of low amplitudes, a higher offset voltage would lead to erroneous results in other design specifications, thus affecting the precision of the design [2]. Thus, minimizing the offset voltages in such cases becomes even more important.

Over the years, various statistical methods and analysis have been proposed by researchers, for modelling circuit mismatch. Lakshmikumar [3] first proposed a statistical model for characterizing the mismatch among device parameters. The work focussed on developing theoretical model for understanding mismatch causes. Pelgrom et al. [4] then proposed the next breakthrough in the analytical model for random offset where he suggested that random mismatch among variables largely depends on standard deviation on device area and spacing among the matched devices. The present work also utilizes the Pelgrom's model for modelling the random offset of the two case studies considered. Kinget [5] investigated the trade-offs involved in improving transistor mismatches and concluded that matching is proportional to area and the accurate specifications requirement in any circuit imposes a minimum circuit area condition. In recent years, random offset and mismatch modelling has been done by for Differential Amplifier by Brito and Bampi [6]. Zhang et al. [7] presented an offset nullifying circuit for minimizing offset in bio-potential amplifiers. All these works have considered the statistical modelling of random offset voltages and follow a common approach for minimizing the random offset in amplifier using tedious analysis of the proposed models to improve the matching by using various modern manufacturing process, improved packaging materials, specialized layout techniques or additional offset nullifying circuits which again leads to higher area requirement. The proposed work proposes a new approach for reducing the random offset voltage, through the use of a new HWPSO algorithm [8] and has not been reported in any of the previous works. Only Sarkar et al. [9] has reported circuit sizing for Systematic offset minimization using Whale Optimization Algorithm (WOA), but no work on random offset minimization has been reported using optimization algorithms. The approach involves firstly, modelling the offset for any circuit by using the standard Pelgrom's Model so as to achieve a Cost Function involving standard deviation of Offset Voltage and then employing HWPSO to solve the derived Cost Function while satisfying minimum design constraints. HWPSO has been found to be satisfactory in optimization of benchmark mathematical functions and has also successfully minimized random offset in a Differential Amplifier [8].

A Two Stage OTA is widely used as front end amplifiers in low frequency applications [1]. In order to meet the minimum design specifications required for optimal performance in any low frequency system, the transistors have to be sized accordingly. A Miller Compensation capacitor is present in the OTA, the choice of which is in itself an important design criteria for low frequency, as it impacts two important design specifications Noise and Power, which have an inherent trade-off among themselves. If C_c is high, then noise can be improved but at the cost of an increased power dissipation. So, an optimum C_c has to be chosen. Thus, considering this trade-off, Mahatanakkul and Chutichatuporn [9], proposed a design rule for two stage OTA, based on which the objective function is solved. Simulations and comparative analysis have been performed. The results illustrate that HWPSO has been successful in minimizing random offset in two stage OTA while meeting the required design constraints with a least trade-off in noise and power. The results have been validated by redesigning the circuits in Cadence Virtuoso which are found to be in close agreement with algorithmic results.

2 Problem Formulation

The schematic of two stage OTA is shown in Fig. 1 from which it is seen that there are 8 transistors in this circuit. C_c is the Miller compensation capacitor used to improve the Phase Margin and stability of the OpAmp [9]. The important design specifications includes Gain, CMRR, ICMR, Slew Rate, Power dissipation etc. In order to meet the minimum design specifications required for optimal performance in any low frequency system, the transistors have to be sized accordingly.

For any process parameter P, the Pelgrom's model for matching can be defined as shown in Eq. (1) [4].

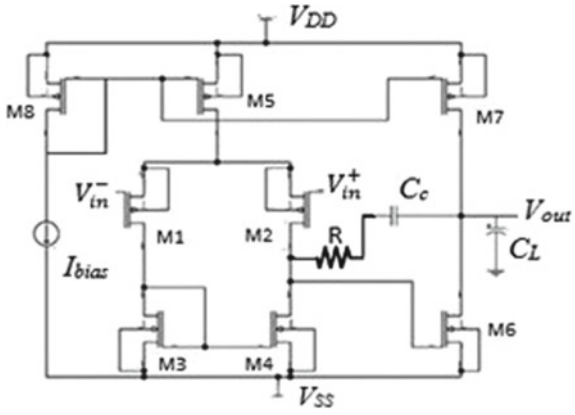

Fig. 1 A two stage operational transconductance amplifier (OTA) with PMOS differential pair

$$\sigma^2(\Delta P) = S_P^2 D_P^2 + \frac{A_P^2}{WL} \tag{1}$$

where $\sigma^2(\Delta P)$ is the variance of the difference of parameter P between the elements; A_P^2 and S_P^2 are the area and spacing proportionality constants for parameter P; W and L are the dimensions of each element; and D_x is the spacing between them. If the elements are laid out in close proximity with a layout style that eliminates most sources of systematic offset mismatch is mostly dominated by the term $\frac{A_P^2}{WL}$ and is given by Eq. (2).

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} \tag{2}$$

The most influential parameters representing P includes, the threshold voltage (V_{TH}), the current factor (β) [6]. The variance for drain current (I_{D}) and gate-source voltage (V_{GS}) can be expressed as a function of these two parameters [6]. The Offset Voltage for the OpAmp is given by the contributions of from the differential pair $M1$, $M2$ and the current mirror load $M3$ and $M4$. The common source 2nd stage do not contribute to offset voltage [10]. Using the Pelgrom's definition for mismatch for any parameter as shown in Eq. (2), the overall random offset voltage for the two stage OpAmp is given by Eq. (3).

$$V_{\mathrm{OS,2stage}} = \frac{A_{V_{\mathrm{TH}},\mathrm{PMOS}}}{\sqrt{W_{12}L_{12}}} + \frac{A_{V_{\mathrm{TH}},\mathrm{NMOS}}}{\sqrt{W_{34}L_{34}}}\left(\frac{\beta_N}{\beta_P}\right)^2 \sqrt{\left(\frac{L}{W}\right)_1 \left(\frac{W}{L}\right)_3} \tag{3}$$

where $\beta_N = \mu_N C_{\mathrm{OX}}(W/L)$, $\beta_P = \mu_P C_{\mathrm{OX}}(W/L)$, C_{OX} is oxide capacitance while μ_N, μ_P are mobility of NMOS and PMOS respectively. AV_{TH}, PMOS and AV_{TH}, NMOS are threshold process area for PMOS and NMOS respectively and are technology dependent constants.

The Eq. (3) forms the objective function for the problem and has to be minimized accordingly. From the above Eq. (3), it is clear that for minimization of random offset appropriate sizing for Width (W) and Length (L) of MOSFET's have to be done. These W and L however impact the other design specifications like Gain, Noise, Power, CMRR etc. defined previously and cannot be arbitrarily chosen. Thus, the design rules which relates the W and L to design specifications form the constraint for the problem. Now, the conventional design rule for Two Stage OTA as presented in Allen and Hollberg [10] does not take into account the noise-power tradeoff through C_c and thus the design rule proposed by Mahatanakkul and Chutichatuporn [9], which considers the trade-off is chosen while formulating the constraints. The overall problem formulation can be defined below and the constraints are presented from Eqs. (4)–(18).

$$\text{Minimize CF} = \frac{A_{V_{\mathrm{TH}},\mathrm{PMOS}}}{\sqrt{W_{12}L_{12}}} + \frac{A_{V_{\mathrm{TH}},\mathrm{NMOS}}}{\sqrt{W_{34}L_{34}}}\left(\frac{\beta_N}{\beta_P}\right)^2 \sqrt{\left(\frac{L}{W}\right)_1 \left(\frac{W}{L}\right)_3} \text{ Subjected to}$$

$$S_n(f) = \frac{16kT}{3\omega_u C_c}\left[1 + \frac{\mathrm{SR}}{\omega_u\left(V_{\mathrm{HR}}^{\mathrm{CM}-} - V_{tn} + V_{tp}\right)}\right] \tag{4}$$

$$I_{D7} = \mathrm{SR}(C_c + C_L) \tag{5}$$

$$L_6 = \sqrt{\frac{3\mu_n V_{\mathrm{HR}}^{\mathrm{out}-} C_c}{2\omega_u(C_c + C_L)\tan(\phi_M)}} \tag{6}$$

$$W_6 = \frac{2\mathrm{SR}(C_c + C_L)L_6}{\mu_n C_{ox}(V_{\mathrm{HR}}^{\mathrm{out}-})^2} \tag{7}$$

$$I_{D5} = \mathrm{SR}C_c \tag{8}$$

$$\left(\frac{W}{L}\right)_{1,2} = \frac{\omega_u^2 C_c}{\mu_p C_{ox}\mathrm{SR}} \tag{9}$$

$$\left(\frac{W}{L}\right)_{5,8} = \frac{2\mathrm{SR}C_c}{\mu_p C_{ox}\left(V_{\mathrm{HR}}^{\mathrm{CM}+} - V_{tp} - \frac{\mathrm{SR}}{\omega_u}\right)^2} \tag{10}$$

$$\left(\frac{W}{L}\right)_7 = \left(\frac{C_c + C_L}{C_L}\right)\left(\frac{W}{L}\right)_{5,8} \tag{11}$$

$$\left(\frac{W}{L}\right)_{3,4} = \frac{\left(\frac{w}{L}\right)_6\left(\frac{W}{L}\right)_{5,8}}{2\left(\frac{W}{L}\right)_7} \tag{12}$$

$$P = \mathrm{SR}(3C_c + C_L)(V_{\mathrm{DD}} - V_{\mathrm{SS}}) \tag{13}$$

$$A_V = \frac{2g_{m1}g_{m6}}{I_{D5}\cdot I_{D6}\left(\lambda_n + \lambda_p\right)^2} \tag{14}$$

where,

$$V_{\mathrm{HR}}^{\mathrm{CM}+} = V_{\mathrm{DD}} - V_{\mathrm{CM(max)}} \tag{15}$$

$$V_{\mathrm{HR}}^{\mathrm{CM}-} = V_{\mathrm{CM}\left(\mathrm{min}\right)} - V_{\mathrm{SS}} \tag{16}$$

$$V_{\mathrm{HR}}^{\mathrm{out}+} = V_{\mathrm{DD}} - V_{\mathrm{out(max)}} \tag{17}$$

$$V_{\mathrm{HR}}^{\mathrm{out}-} = V_{\mathrm{out}\left(\mathrm{min}\right)} - V_{\mathrm{SS}} \tag{18}$$

Table 1 Design specifications for use in low frequency systems (two stage OTA)

Design criteria	Specifications
Slew rate (V/μs)	≥10
Load capacitance, C_L (pF)	≥15
A_v (dB)	>40
f_u (MHz)	≥2
$V_{\text{CM(min)}}$ (V)	≥−1.6
$V_{\text{CM(max)}}$ (V)	≤1.6
CMRR (dB)	>60
PSRR (dB)	>60
Power dissipation, P (mW)	≤7
$V_{\text{out(min)}}$ (V)	≥−1.8
$V_{\text{out(max)}}$ (V)	≤1.8
Input referred noise, $S_{\text{n}}(f)$ (V/$\sqrt{\text{Hz}}$)	≤500 n

where, $\lambda_n$andλ_p are channel length modulation factors.

From Eqs. (4)–(13), it can be clearly seen that there is an inherent trade-off between Noise and Power as mentioned previously which has been addressed by the considered design rule. The design vector comprising of the design variables for the problem can be therefore defined as shown in Eq. (19) and the design specification for them is shown in Table 1. The remaining are technology constants as shown in Table 2.

$$X_{\text{OpAmp}}\left[\text{SR},\ f_u, \text{ICMR}_{\text{min}}, \text{ICMR}_{\text{max}}, A_v,\ P,\ S_n(f), \phi_M,\ V_{out(\text{min})},\ V_{\text{out(max)}}\right] \tag{19}$$

Table 2 Values of other technology constants used

Specification	Values used
V_{DD} (V)	1.8
V_{SS} (V)	−1.8
V_{tp} (V)	−0.42
V_{tn} (V)	0.42
K_n (μA/V^2)	355
K_p (μA/V^2)	75
$W1 = W2 = W5 = W6 = W7 = W8 = L3$	20 μm
AV_{THN}	5 nm
AV_{THP}	5.49 nm
C_C	0.35 C_L
Technology node	180 nm
λ_n	0.04
λ_p	0.05

From Eq. (19), it can be seen that the number of design variables is 10. Hence, the problem is 10 dimension problem and optimized for minimum circuit area such that the design specifications defined by minimum criteria required for low frequency applications as shown in Table 1 are met.

3 HWPSO Algorithm

The Hybrid Whale Particle Swarm Optimization (HWPSO) is a hybrid swarm based meta-heuristic algorithm, proposed by Laskar et al. [8] which takes into account the good qualities in two popular swarm based algorithm PSO [11] and WOA [12] to propose a high performance hybrid algorithm. PSO is based on food searching mechanisms of bird flocks and is characterized by two parameters: position and velocity. The optimal solution is given by the position of the global best particle. However, it suffers from the stagnation effect. Thus, a new simplified approach towards improving the performance of the PSO in terms of eliminating stagnation effect and improving convergence speed is proposed in HWPSO. This is done by incorporating the WOA search principle in PSO, thereby proposing the Hybrid Whale-PSO (HWPSO) algorithm. Whale Optimization Algorithm (WOA) is also a swarm-based algorithm proposed by Mirjalili et al. [12], inspired by the food searching mechanism of Humpback Whales. WOA has been found to have very good exploration capability and optimum for bowl shaped functions. But, it also has limitations in its exploitation phase, which leads to poor convergence speed in case of complex multiple minima functions.

The hybridization process presented in HWPSO is somewhat unique and different from that used in earlier reported works. Here, the exploration and exploitation phase of PSO and WOA is combined with the use of three different strategies to establish a new high-performance algorithm. The first strategy is the iterative hybridization process [8] which involves executing the two parent algorithms sequentially within primary and secondary iterations, to enhance the performance of the proposed algorithm. In the primary iteration, first PSO is used to find an initial tentative solution by exploring the search space and within it Whale search mechanism is used in secondary iterations as Whale can explore search space efficiently due to its spiral and logarithmic encirclement techniques. This results in complete exploration of search space by dodging all local minima.

Then two novel strategies of 'Forced' Whale and 'Capping' Phenomenon are introduced. 'Forced' Whale strategy is used to guide PSO during exploration phase to avoid local minima. With the concept of 'Forced' Whale phenomenon all the parameters of whale are made dependent not only on secondary iterations but also on number of primary iterations as defined by Eqs. (20) and (21).

$$a = 2 - \left[it \cdot \left(\frac{2}{\text{Max\_im}_2} \right) \right] \tag{20}$$

$$a_2 = -1 + \left[it \cdot \left(\frac{-1}{\text{Max\_im}_2} \right) \right] \tag{21}$$

where, '*it*' is primary iteration and Max_im_2 is maximum number of secondary iterations

'Capping' Phenomenon restricts the use of WOA searching mechanism in exploitation phase, thereby paving the way for PSO to converge the solution faster to a global optimum value. This is done by modelling the number of secondary iterations as per Eq. (22).

$$\text{Max\_im}_2 = [A \cdot (it) + C] \tag{22}$$

where 'im_2' is maximum number of iteration for WOA (secondary iteration), 'it' is primary iteration variable, '*A*' and '*C*' are constants and can be chosen based on the shapes and modes of function to be optimized.

As seen from Eq. (22), as the number of primary iterations increase, the number of secondary iterations decreases and eventually becomes zero. As a result, the WOA ceases to exist in the exploitation phase, which is then determined solely by PSO mechanism.

4 Results and Discussions

HWPSO is employed to minimize the random offset for the two stage OTA by minimizing the cost function defined in Eq. (3) subjected to the constraints as given in Eqs. (4)–(18) which are defined to meet the specifications shown in Table 1 and the optimal values of design variables in design vector of Eq. (19) are determined within these boundaries. Additionally, $1 \leq W_k/L_k \leq 100$ has to be met for each MOSFET. A population size of 50 has been considered and thus a 50×10 population matrix is formed while solving the problem. A maximum iterations of 100 is chosen. Thus, a total of around 2500 function evaluations has been made before recording the optimal data for 20 independent runs. A comparison with parent algorithms i.e. PSO, WOA and other state of art algorithms have been performed based on these parameters and by performing Friedmann's statistical test. The results are indicated in Tables 3 and 4, which indicates that HWPSO performs efficiently in giving a minimum random offset voltage than the other algorithms used. Validation of the HWPSO results is performed by redesigning the two stage OTA with optimal design parameters from best value of cost function obtained by the algorithms, in Cadence Virtuoso using 180 nm technology parameters and performing desired simulations. The results are in close agreement with each other as shown in Figs. 2 and 3. Figure 2 shows that Gain is 44.98 dB for HWPSO and rolls of at the rate of −3 dB/decade. However, the gain increases to 47 dB for HBPSO because of increase in $W1/L1$. For input noise, there is an increase a slight increase in case of HWPSO which gives a value of

Table 3 Comparative analysis of the best results obtained using HWPSO and other algorithms after 20 independent runs

Specifications	PSO	SSA	HBPSO	DA	WOA	HWPSO
Slew rate, SR (V/μs)	20	20	20	20.27	20.57	20.04
Unity gain frequency, f_u (MHz)	1.00	1.00	2.15	2.01	2.03	2.01
Compensation capacitance, C_c (F)	5p	5p	5p	5p	4.99p	4.95p
Load capacitance, C_L (F)	14.2p	14.2p	14.2p	14.29p	14.28p	14.17p
$V_{\text{CM(min)}}$ (V)	−1.55	−1.55	−1.26	−1.35	−1.36	−1.29
$V_{\text{CM(max)}}$ (V)	1.516	1.516	1.47	1.449	1.51	1.53
$V_{\text{out(max)}}$ (V)	1.794	1.794	1.797	1.798	1.789	1.798
$V_{\text{out(min)}}$ (V)	−1.23	−1.23	−1.43	−1.31	−1.29	−1.31
Phase margin, Φ_M (°)	75.36	75.36	59.33	65.05	66.11	67.22
Gain, A_v (dB)	43.30	43.30	47.41	45.13	44.97	44.98
Power dissipation, P (W)	3.49 μ	3.49 μ	2.75 μ	3.14 μ	3.23 μ	3.12 μ
Cut-off frequency, $f_{-3\text{dB}}$ (KHz)	6.91	6.91	10.56	11.16	11.48	10.96
CMRR (dB)	62.01	62.01	61.86	61.73	61.58	61.84
PSRR (dB)	69.06	69.06	71.14	68.94	67.35	67.29
Input noise, $S_n(f)$ (V/$\sqrt{}$Hz)	27n	27n	27.91	27.04n	27.83n	28.24n
Random offset (mV)	1.64	1.64	1.641	1.64	1.639	1.638

Table 4 Friedman's test result considering minimum area for 20 independent runs

Algorithm	Mean rank	Rank
PSO	4.4000	4
DE	5.6000	6
SSA	4.9500	5
DEPSO	7.5000	7
HBPSO	5.5000	5
DA	4.6500	3
WOA	2.0000	2
HWPSO	1.4000	1

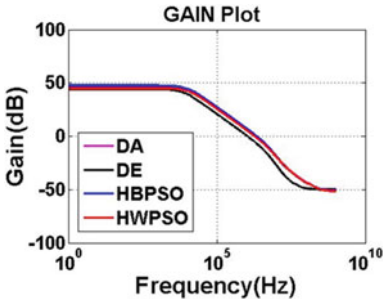

Fig. 2 Cadence virtuoso simulated gain plot for HWPSO algorithm

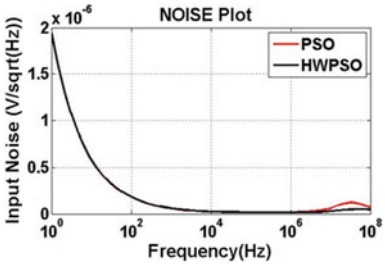

Fig. 3 Cadence virtuoso input noise plot for HWPSO algorithm

28.24 nV/$\sqrt{}$Hz due to increase in $W1/L1$ which is mainly responsible for low offset voltage. The decrease in C_c in PSO as compared to HWPSO is also responsible for reducing the random offset with an increase in input noise as evident from Table 3 and Fig. 3. Table 3 shows that HWPSO gives a minimum random offset voltage of 1.638 mV with an optimum circuit area of 3.51×10^{-9} m^2 with a low power dissipation of 3.12 mW which is suitable for low frequency applications. A small trade-off with input noise is done to achieve so. But the power dissipation in PSO optimized two stage OTA increases to 3.49 m and returns a higher random offset voltage of 1.64 m with a higher trade-off with circuit area which is in accordance with theory discussed in Sect. 2. For determining the random offset Monte Carlo simulations are performed and standard deviation is noted for sample values of 3σ. The results are shown in Fig. 4 which is in accordance with algorithmic values given in Table 3. However, a small deviation exists which may be due to certain higher order effects neglected during the modelling of random offset shown in Eq. (3).

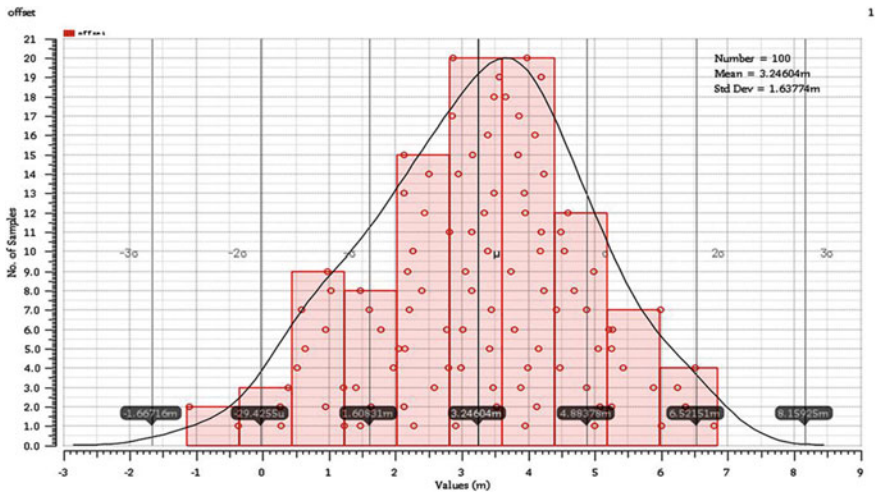

Fig. 4 Monte carlo simulation plot for random offset voltage using HWPSO algorithm

5 Conclusions

The proposed work introduces a new approach for minimizing the random offset volt-age in two stage OTA considering noise-power trade-off. The proposed work makes use of the Pelgrom's model to derive the random offset voltage for two stage OTA and then uses the new HWPSO to minimize it taking into consideration several design constraints and specifications required to be met for using these amplifiers in front end of low frequency system Simulations have been performed for more than 20 independent runs in MATLAB 2013 and comparative analysis with other state of art algorithms have been done for around 2500 function evaluations using statistical tests. The results illustrate that the HWPSO algorithm achieves a minimum random offset (best) with less power dissipation and low trade-off in noise and power as compared to state of art algorithms while meeting constraints and specifications required to be met for using two stage OTA in front end of low frequency system. The proposed work can be extended by modelling random offset for other OTA topologies such as Folded cascode and Recycling Folded cascode and minimizing the random offset using HWPSO which can be considered as a future enhancement to this work.

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Optical Simulation of III-V Semiconductor Nanowires/PEDOT: PSS-Based Hybrid Solar Cells: Influence of Polymer Coating Thickness and Geometrical Parameters on Light Harvesting and Overall Photocurrent

D. V. Prashant, Dip Prakash Samajdar, and Sachchidanand

Abstract Hybrid solar cells (HSCs) can be a new pathway for low-cost, flexible, and high efficiency solar cells. III-V nanowires (NWs) with sub-wavelength scale dimensions have shown excellent optical and electrical properties, and can be easily fabricated on thin substrates together with polymer materials. In order to obtain optimal design requirements for III-V NWs/PEDOT: PSS HSCs, optical simulations using finite-difference-time-domain (FDTD) method is performed. To enhance light absorption properties of NWs, the important geometrical parameter, namely the diameter (D) of the NWs is optimized. Further, to maximize short-circuit current density, polymer (PEDOT: PSS) coating thickness on the NWs is optimized. In comparison to NW/air system, optimized PEDOT: PSS-coated NWs have shown better intrinsic anti-reflection properties, broad absorption spectra, and enhanced optical generation rates.

Keywords Hybrid solar cells · III-V nanowires · PEDOT: PSS · FDTD · Lumerical software package

1 Introduction

In the recent few years, hybrid solar cells (HSCs) fabricated using both organic semiconducting polymer materials as well as inorganic semiconductor nanostructures have attracted a lot of research interest due to no lattice match concerns and judicious use of advantageous properties of both the material [1]. A hybrid heterojunction is formed between the p-type semiconducting polymer materials and n-type

D. V. Prashant · D. P. Samajdar (✉) · Sachchidanand
Department of Electronics and Communication Engineering, PDPM Indian Institute of Information Technology, Design and Manufacturing, 482005 Jabalpur, Madhya Pradesh, India
e-mail: dippraksh010@gmail.com

D. V. Prashant
e-mail: dvprashant1818@gmail.com

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inorganic semiconductor nanostructures [2, 3]. In HSCs, semiconductor nanostructures like NWs with sub-wavelength dimensions can promote energy harvesting by supporting localized optical resonant modes [4]. Additionally, they can also modify the bandgap, electrical conductivity, and absorption profile through the quantum confinement effects [5, 6]. Varieties of methods are available to grow and tune a wide range of NWs with different dimensions and to integrate them with a low-cost substrate [7, 8]. In numerous experimental and theoretical reports, it has been confirmed, that by optimizing the geometrical parameters like length (L), diameter (D), and filling ratio (FR) of semiconductor NWs, the optical as well as electrical properties of NWs can be tuned [9–12]. The organic semiconducting polymer materials, on the other hand, can be easily coated onto the NWs via spin-coating technique to give superior performance of the HSCs by improving optical absorption and by reducing the reflection and transmission of the incident light with subsequent improvement of the hole transport properties [13, 14].

One of the key areas of research in the field of HSCs is centered on the discovery of suitable combinations of organic and inorganic semiconductor materials to improve the efficiency of solar cells [15]. Poly (3-hexylthiophene) (P3HT) and poly (3, 4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT: PSS) are most widely used polymer materials in HSCs. Both P3HT and PEDOT: PSS possesses excellent optical and hole transport properties. In a number of experimental works, it is found that by optimizing the thickness of the semiconducting polymer materials, optical as well as carrier transport properties in HSCs can be enhanced [16]. Apart from silicon (Si)-based nanostructures, III-V semiconductor nanostructures have attracted lots of research on optoelectronic device applications including solar cells because they are non-toxic and have a wide range of materials with different band gap and other electrical properties [17, 18].

In this article, to evaluate optimum design requirements for efficient light trapping of polymer/NWA HSCs, an optical simulation of PEDOT: PSS/III-V semiconductor NWA HSCs with three different III-V materials are investigated using 3D finite-difference time-domain (FDTD) method.

2 Simulation Methodology

The optical simulations are performed using commercial FDTD solutions software of Lumerical Inc. The boundary condition in simulation is set as periodic boundary condition along x- and y-directions whereas perfectly matched layer (PML) condition is considered along z--direction. The system consists of a 200 nm thick Si substrate with III-V NWs grown over it. The geometric parameters of the structure are the length of the NWs (L) which is taken as 2 μm, diameter (D) which is varied from 120 to 270 nm, period of the square lattice (P) which is fixed at 0.5, and polymer coating thickness (T) which is varied from 10 to 80 nm. A plane wave optical source with wavelength ranging from 300 to 1100 nm is incident upon the NWs whose direction is perpendicular to the Si substrate. Frequency domain power monitors

are used to calculate the reflectance $R(\lambda)$ and transmittance $T(\lambda)$ from which the absorption $A(\lambda)$ is computed as follows:

$$A(\lambda) = 1 - R(\lambda) - T(\lambda) \tag{1}$$

The short-circuit current density, J_{sc}, which is an important photovoltaic parameter, is calculated under the excitation of the structure by the AM 1.5 solar spectrum assuming a unit internal quantum efficiency [19].

$$J_{sc} = \frac{e}{hc} \int_{300\text{ nm}}^{1100\text{ nm}} \lambda A(\lambda) I_{AM1.5}(\lambda) d\lambda \tag{2}$$

$I_{AM1.5}$ is the AM 1.5 solar spectral irradiance over the wavelength region of interest. The necessary refractive index data for GaAs, InP, InAs NWs, and Si substrate is provided in Palik material data base of Lumerical and the corresponding refractive index for PEDOT: PSS polymer material is modelled from the literature [20].

3 Results and Discussions

Two dominant processes decide the optical absorption of the NWAs: mode resonance controlled by NW diameter and periodicity of the reflection and transmission of the incident solar spectrum [21]. This necessitates the establishment of relationship among the geometrical parameters of the NWs and the corresponding light absorbing process to maximize light absorption. In our analysis, firstly, we have studied the effect of geometrical parameter variation on optical absorption of the InP NWAs and then carried out the same analysis for the GaAs and InAs NWAs. To find the optimal value of diameter, we have fixed the FR of the NWs to 0.5 and varied D from 120 to 270 nm. From Fig. 1a–c, it can be seen that the optical absorption of the NWAs is drastically improved in higher wavelength region ($\lambda > 700$ nm) with the variation of D. This variation in optical absorption can be understood through the concept of guided resonance modes. NWs with small diameters can support only few modes of resonance due to which most of the incident light cannot be guided into NWs properly and gets reflected. On the other hand, NWs with larger diameters promotes surface reflection, thereby leading to optical losses.

In Fig. 1b, c, it can be noticed that for lower values of diameter like $D = 120$ and 150 nm, very large reflectance and transmittance losses are observed, as the resonance modes are not supported by these structures. However, for comparatively larger values like $D = 180$ and 240 nm, very less reflectance and transmission losses are observed, which results in improved optical absorption (Fig. 1a). Further, as D is increased to 270 nm, the absorption is hindered in 600–900 nm wavelength region,

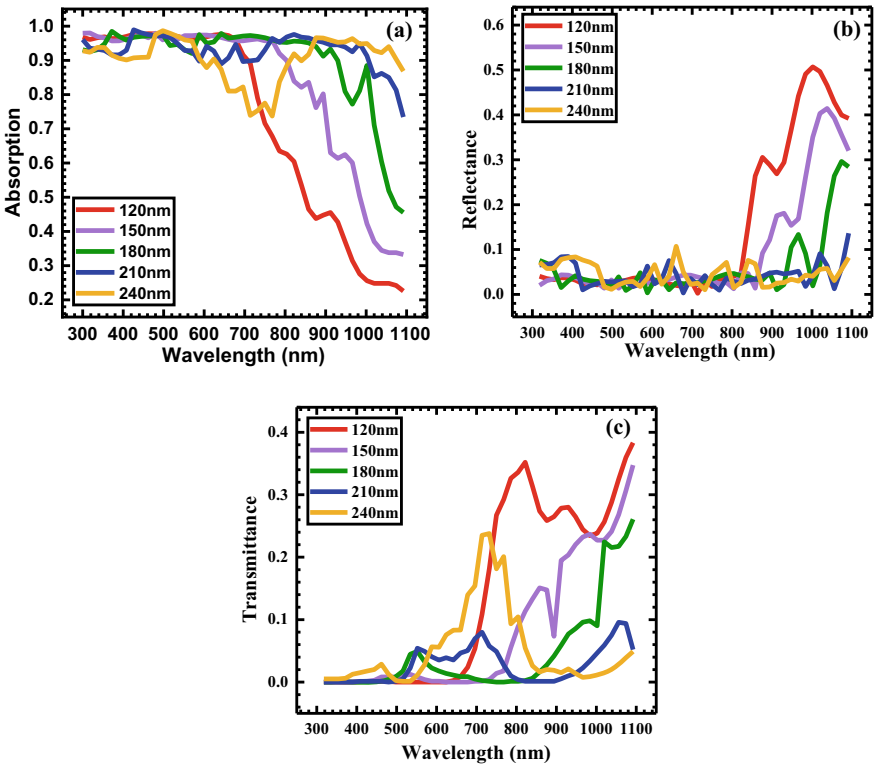

Fig. 1 Optical properties of InP NWAs at different diameters (D) at fixed FF = 0.5: **a** Absorptance, **b** Reflectance, and **c** Transmittance

which is due to the increased reflection of the incident light. In our case, NWs with diameter of 210 nm exhibit broad absorption throughout the wavelength regime.

Figure 2a reveals that optical absorption >75% throughout the wavelength regime 300–1100 nm can be achieved with all three NWs. From Fig. 2b, the value of J_{sc} increases with the value of D of the NWs and reaches to its maximum value at 210 nm (for all three materials under consideration) which is attributed to improved light absorption. However, further increase in diameter results in decrease of J_{sc} due to the increased surface reflection and insufficient field concentration [22]. Among the three NWs, InAs NWs have achieved maximum value of J_{sc} of 41.8 mA/cm^2, which is attributed to their broad absorption (> 90%) throughout the entire incident spectrum. For further investigation, we have fixed the diameter of the NWs at their optimized diameter of 210 nm.

After optimizing the diameter of the NWs, we have evaluated the optimal coating thickness of polymer that is to be coated onto the NWAs. In Fig. 3b, J_{sc} as a function of polymer coating thickness is plotted. The J_{sc} of the PEDOT: PSS/NWAs system increases linearly as the polymer coating thickness is increased and attains a maximum value for coating thickness of 50 nm (for all the three cases). The increment

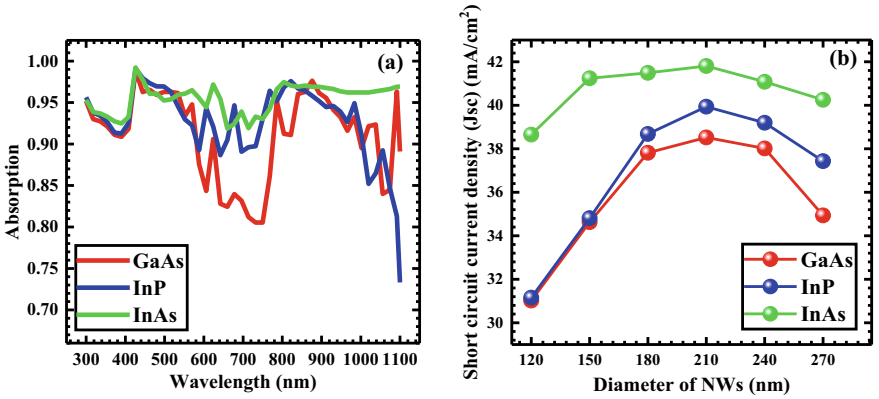

Fig. 2 **a** Absorptance plot of three different NWs at their optimized diameter ($D = 210$ nm) and **b** short-circuit current density of NWAs as a function of diameter D

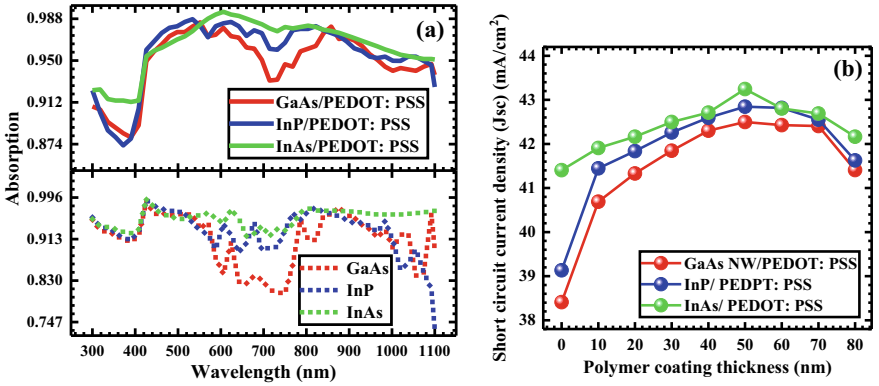

Fig. 3 **a** Absorptance plot of PEDOT: PSS-coated and PSS-uncoated NWAs at their optimized geometric configuration ($D = 210$ nm and coating thickness $= 50$ nm) and **b** short-circuit current density of PEDOT: PSS/NWAs as a function of polymer coating thickness

in J_{sc} is attributed to the improved optical absorption of the NWAs (in Fig. 3a), due to the presence of additional low-index PEDOT: PSS coating layer. Further, increase in the coating thickness (> 50 nm) results in decrease of J_{sc}, which is attributed to the decrease in transmission of incident light in PEDOT: PSS/NW structure due to an increase in the photoactive material, which results in absorption losses [23]. Similar results are observed for P3HT/Si and P3HT/GaAs HSCs [23, 24].

In Table 1, we have listed some important parameters of PEDOT: PSS/III-V NWA HSCs for the optimized geometric parameters.

Table 1 Maximum generation rate, maximum absorption, and maximum J_{sc} in visible wavelength region, and maximum absorbance in the long wavelength region of InP, GaAs and InAs NWs

Structure	$\lambda = 350$–650 nm		$\lambda = 650$–1100 nm		Max. J_{sc} (mA/cm^2)
	Max. gen. rate (cm^{-3}s^{-1})	Max. abs. (%)	Max. gen. rate (cm^{-3}s^{-1})	Max. abs. (%)	
PEDOT: PSS/InP	3.6e+028	98.51	1.1e+028	98.16	42.81
PEDOT: PSS/GaAs	3.2e+028	98.47	1.2e+028	97.27	42.42
PEDOT: PSS/InAs	4.3e+028	99.43	1.7e+028	98.89	43.24

4 Summary

In summary, we have investigated the performance of uncoated NWA and PEDOT: PSS/NWA systems using FDTD method. In this analysis, it has been observed that to guarantee maximal light absorption and $J_{sc,}$ the diameter of the NWs must be optimized. NWs with diameter of 210 nm have shown the best performance in terms of optical absorption and J_{sc} (for all three cases). In addition to this, conformal coating of PEDOT: PSS on the NWs further boost their absorption and optical generation rates throughout the incident spectrum. The simulation of our proposed structure for PEDOT: PSS/NWA system has achieved J_{sc} as high as 42.42, 42.81, and 43.24 mA/cm^2 for 50 nm PEDOT: PSS-coated GaAs, InP, and InAs NWAs, respectively. The optimized PEDOT: PSS/(III-V) NWA HSCs have achieved improvement in J_{sc} by 10, 7, and 3% in comparison to uncoated GaAs, InP, and InAs NWs, respectively.

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Reconstruction of Phylogenetic Tree for COX with DNA Sequences

D. Anurag, Chukka Santhaiah, N. V. Krishna Rao, V. JaswanthSai, P. Akash, and R. AnanthSai

Abstract The phylogenetic tree plays a major role in identifying the evolution of specie or evolutionary relationships. The aim of this study was to reconstruct phylogenetic tree for cyclooxygenase (COX) gene with DNA sequences. The COX gene (P22437.1) data is taken from the NCBI (National Centre for Biotechnology Information) repository. During the process of reconstruction, the data is always considered in FASTA format. Blast function is used on this data which helps in calculating optimal alignments in faster process and also searches for similarity scores in known DNA sequences or other organisms. Then, the ClustalW approach is used for reconstruction of the tree as it uses progressive alignment methods and also helps in reducing duplicate sequences.

Keywords Phylogenetic tree · ClustalW · COX · BLAST

1 Introduction

Proteins are the work horses of biology. Each cell in every living organism is very important role in life of living organism. Proteins are vital for the understanding of biology in healthy and unhealthy states in addition as providing drug targets against infective organisms and that they are even potentially drugs themselves. Protein consists of amino acids, and its sequence determines the chemical structure of protein. The protein sequence analysis is to identify homologous proteins, to classify protein families, and to construct evolutionary tree.

BLAST helps in comparing biological sequences such as proteins, DNA, or RNA. It takes user query as a sequence and identifies the similarities. The search results are shown within the kind of graphical representation, tables, order of significance, and alignments. In this work, TBLASTN has been used to find the DNA sequences with single protein sequence query and to get the BLAST results.

D. Anurag · Chukka Santhaiah (✉) · N. V. Krishna Rao · V. JaswanthSai · P. Akash · R. AnanthSai
Department of CSE, Institute of Aeronautical Engineering, Dundigal, Hyderabad, Telangana, India
e-mail: chukka.santh@gmail.com

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There are different algorithms available for multiple alignment. Each one has the advantages and disadvantages based on its parameters. The ClustalW is the one of the approaches for multiple alignments. It gives best results for multiple sequence alignment for phylogenetic tree.

2 Literature Survey

Wan and Che [1] discussed the approach for construction of phylogenetic trees with interacting pathways data, and they applied clustering methods on two organisms—eukaryotes and prokaryotes.

Makarenkov [2] was proposing a methodology for regenerating phylogenetic trees with help of partial distance matrices. This methodology combines the usage of ultrametric differences and four point conditions to unravel the lost entries.

Heymans [3] has displayed a new method based on underlying graphs for the phylogenetic analysis of pathways.

Toscano [4] presented an idea on COX-1 and COX-2 which are important and have different roles in functions of brain. Removing of COX-1 or COX-2 contrasts in brain levels of prostaglandin E2, suggesting that COX-1 and COX-2 both play different roles in brain acid metabolism and gene expression.

Vane [5] describes the prostaglandins preserves the abdomen lining and maintains the function of a kidney, which are produced by COX-1 is available in brain and spinal cord, which may be the cause for pain and fever during nerve transmission.

Hahn [6] discussed a study about determination of COX-1 geno type function which impacts (hemodynamic responses) HRs. Tim has used visual checkboard stimulations and double blind imaging approach for measuring the Hrs.

3 Implementation Methodology

ClustalW approaches like dynamic programming (DP) and multiple sequence alignment (MSA) for sequence alignment were available before ClustalW approach. Dynamic programming is an algorithm used for aligning sequences allowing for matches, mismatches, and gaps. The algorithm first finds the best alignment at the beginning of the sequences and then subsequently adds similar sequences until both sequences were aligned.

From the hierarchical approaches and non-hierarchical methods, there are many different methods used for multiple sequence alignment; here, reconstruction of phylogenetic tree for COX (Cyclooxygenase) gene with DNA sequences is done using ClustalW algorithm. The COX gene (P22437.1) data is taken from the NCBI (National Centre for Biotechnology Information) repository. During the process of reconstruction, the data is always considered in FASTA format. TBLASTN function is used on this data which helps in calculating optimal alignments in faster process

and also searches for similarity scores in known DNA sequences or other organisms. Then, the ClustalW approach is used for reconstruction of the tree as it uses progressive alignment methods and also helps in filling the missing data in the sequences. With the help of ClustalW, we can generate different phylogenetic trees which uses UPGMA algorithm at the time of creation of the tree. FAST tree is topologically more accurate. RAxML has more ML score than FAST tree. PhyML is faster but non partionable, whereas RAxML is partionable.

TBLASTN helps in comparing a protein sequence in the DNA database and aligns the protein sequence translated in six frames. In this function, the protein accession number's FASTA format data is searched and TBLASTN function is applied to reveal the corresponding DNA sequence accession numbers and then select the DNA sequence in FASTA Format based on DNA accession number.

ClustalW is used for continuous MSA methods because of its size and the speed. Its approach is used for reconstruction of the tree as it uses progressive alignment methods and also helps in reducing duplicate sequences. In this algorithm, the pairwise alignment is applied on the sequences, and if pairwise alignment is fast-appropriate, then read the corresponding parameters for fast-appropriate and then calculate score value and sum-of-pairs score

$$\mathrm{Sc}(A) = \sum_{i<j} \mathrm{SC}\left(P_{i,\,j}(A)\right) \tag{1}$$

where

A is the multiple sequence alignment (MSA) of $S_1, S2 \ldots S_n$,

$P_{i,j}$ is pair of ith row sequence with jth column sequence

If pairwise alignment is slow-accurate, then read the corresponding parameters for slow accurate and calculate weight matrix for sequences $S_1, S2 \ldots S_{n.}$

$$W(\mathrm{Si}) = \sum_{k=1}^{n} gk \tag{2}$$

where

$$g_k = l_k / n_k$$

l_k length of k and n_k number of sequences under k

n-number of sequence

k-number of characters in each sequence.

And last perform multiple alignments and call construction of Phylogenetic tree function.

4 Performance Analysis and Results

In the method of constructing of phylogenetic tree with single protein is given the foremost similar polymer (DNA) sequences of input protein sequences. Here, the foremost of the polymer sequences have the near relationship with protein sequence.

The protein sequence is operated TBLASTN operation to get the similar DNA sequences from the NCBI. When BLAST operation perform on DNA sequences it takes some time based sequence length. In the above protein sequence is operated TBLASTN operation get the similar polymer sequences from the NCBI. When BLAST operation performs on DNA sequences that takes the time for execution of BLAST supported the input sequence length and its offer 3 sections of output.

4.1 Graphic Summary

The graphic outline displays the colour image which is shown in Fig. 1. Query sequence data is at the high, and each bar represents the portion that is similar to input data and therefore the region of input sequence in which this similarity happens.

Red bars indicate the foremost similar sequences. The most effective advantage of this graphic shows that it will assist to see matches that do not extend the length of input query.

4.2 Hit List

The BLAST hit list shows the input sequence is like something that is already within the database and it is a trust hit for reference.

Figure 2 shows the taxonomy reports of the TBLASTN operation performed on the P22437.1 accession number which shows the number of hits of the main protein sequence when aligned to nucleotide database.

4.3 The Alignment

Figure 3 shows the blast results with sequence length and query process and TBLASTN operation alignment details of P22437.1 protein as an alignment it shows the score, expected strategies is compositional matrix adjustment, identity, positives, gaps and frames. Finally, the results describe that some similarity is there. Single portion of the pairwise alignment of input sequence phylogenetic tree without branch length for single protein is shown in Fig. 3.

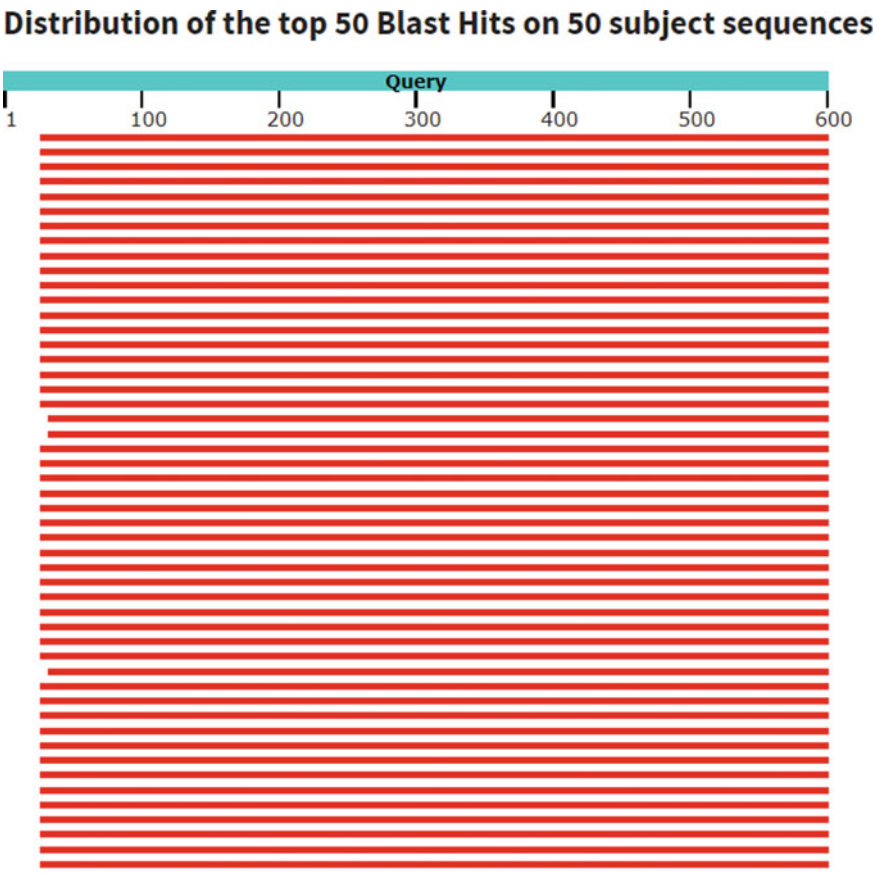

Fig. 1 BLAST graphic summary of the hit process

Figure 1 is a COX phylogenetic tree reconstructed using PhyMl using multiple sequence alignment. ML tree was inferred using PhyML v20160115 ran with model and parameters: -f m–alpha e–nclasses 4–bootstrap-2-o tlr–pinv e. Branch supports are the Chi2-based parametric values returned by the approximate likelihood ratio test.

Figure 1 is a COX phylogenetic tree reconstructed using RAxMl using multiple sequence alignment. ML tree was inferred using RAxML v8.1.20 ran with model GTRGAMMA and default parameters. Branch supports are SH-like values.

Organism	Blast Name	Score	Number of Hits	Description
root			51	
. Euarchontoglires	placentals		48	
. . Rodentia	rodents		39	
. . . Muroidea	rodents		37	
. . . . Muridae	rodents		30	
. . . . . Mus	rodents		21	
. . . . . Mus	rodents		20	
. . . . . Mus musculus	rodents	1213	19	Mus musculus hits
. . . . . Mus caroli	rodents	1203	1	Mus caroli hits
. . . . . Mus pahari	rodents	1195	1	Mus pahari hits
. . . . . Grammomys surdaster	rodents	1187	2	Grammomys surdaster hits
. . . . . Rattus norvegicus	rodents	1175	6	Rattus norvegicus hits
. . . . . Mastomys coucha	rodents	1149	1	Mastomys coucha hits
. . . . Mesocricetus auratus	rodents	1130	1	Mesocricetus auratus hits
. . . . Microtus ochrogaster	rodents	1127	1	Microtus ochrogaster hits
. . . . Cricetulus griseus	rodents	1127	1	Cricetulus griseus hits
. . . . Peromyscus maniculatus bairdii	rodents	1117	1	Peromyscus maniculatus bairdii hits
. . . . Peromyscus leucopus	rodents	1116	1	Peromyscus leucopus hits
. . . . Nannospalax galili	rodents	1112	2	Nannospalax galili hits
. . . Marmota marmota marmota	rodents	1104	2	Marmota marmota marmota hits
. . Nomascus leucogenys	primates	1105	1	Nomascus leucogenys hits
. . Macaca fascicularis	primates	1104	1	Macaca fascicularis hits
. . Homo sapiens	primates	1104	4	Homo sapiens hits
. . Papio anubis	primates	1104	1	Papio anubis hits
. . Carlito syrichta	primates	1104	1	Carlito syrichta hits
. . Chlorocebus sabaeus	primates	1104	1	Chlorocebus sabaeus hits
. synthetic construct	other sequences	1104	3	synthetic construct hits

Fig. 2 Taxonomy reports of the blast operation

Mus musculus 16 days neonate heart cDNA, RIKEN full-length enriched library, clone:D830039P19 product:prostaglandin-endoperoxide synthase 1, full insert sequence

Sequence ID: **dbj|AK142741.1|** Length: 2353 Number of Matches: 1

Range 1: 143 to 1870

Score	Expect	Method	Identities	Positives	Gaps	Frame
1131 bits(2925)	0.0()	Compositional matrix adjust.	576/576(100%)	576/576(100%)	0/576(0%)	+2

Features:

```
Query  27    ADPGVPSPVNPCCVYPCQNQGVCVRFGLDNYQCDCTRTGYSGPNCTIPEIWTWLRNSLRP  86
            ADPGVPSPVNPCCVYPCQNQGVCVRFGLDNYQCDCTRTGYSGPNCTIPEIWTWLRNSLRP
Sbjct  143   ADPGVPSPVNPCCVYPCQNQGVCVRFGLDNYQCDCTRTGYSGPNCTIPEIWTWLRNSLRP  322

Query  87    SPSFTHFLLTHGYWLWEFVNATFIREVLMRLVLTVRSNLIPSPPTYNSAHDYISWESFSN  146
            SPSFTHFLLTHGYWLWEFVNATFIREVLMRLVLTVRSNLIPSPPTYNSAHDYISWESFSN
Sbjct  323   SPSFTHFLLTHGYWLWEFVNATFIREVLMRLVLTVRSNLIPSPPTYNSAHDYISWESFSN  502

Query  147   VSYYTRILPSVPKDCPTPMGTKGKKqlpdvqllaqqlllRREFIPAPQGTNILfaffaqh  206
            VSYYTRILPSVPKDCPTPMGTKGKKQLPDVQLLAQQLLLRREFIPAPQGTNILFAFFAQH
Sbjct  503   VSYYTRILPSVPKDCPTPMGTKGKKQLPDVQLLAQQLLLRREFIPAPQGTNILFAFFAQH  682

Query  207   fthqffktSGKMGPGFTKALGHGVDLGHIYGDNLERQYHLRLFKDGKLKYQVLDGEVYPP  266
            FTHQFFKTSGKMGPGFTKALGHGVDLGHIYGDNLERQYHLRLFKDGKLKYQVLDGEVYPP
Sbjct  683   FTHQFFKTSGKMGPGFTKALGHGVDLGHIYGDNLERQYHLRLFKDGKLKYQVLDGEVYPP  862

Query  267   SVEQASVLMRYPPGVPPERQMAVGQEVFGLLPGLMLFSTIWLREHNRVCDLLKEEHPTWD  326
            SVEQASVLMRYPPGVPPERQMAVGQEVFGLLPGLMLFSTIWLREHNRVCDLLKEEHPTWD
Sbjct  863   SVEQASVLMRYPPGVPPERQMAVGQEVFGLLPGLMLFSTIWLREHNRVCDLLKEEHPTWD  1042

Query  327   DEQLFQTTRLILIGETIKIVIEEYVQHLSGYFLQLKFDPELLFRAQFQYRNRIAMEFNHL  386
            DEQLFQTTRLILIGETIKIVIEEYVQHLSGYFLQLKFDPELLFRAQFQYRNRIAMEFNHL
Sbjct  1043  DEQLFQTTRLILIGETIKIVIEEYVQHLSGYFLQLKFDPELLFRAQFQYRNRIAMEFNHL  1222

Query  387   YHWHPLMPNSFQVGSQEYSYEQFLFNTSMLVDYGVEALVDAFSRQRAGRIGGGRNFDVHV  446
            YHWHPLMPNSFQVGSQEYSYEQFLFNTSMLVDYGVEALVDAFSRQRAGRIGGGRNFDVHV
Sbjct  1223  YHWHPLMPNSFQVGSQEYSYEQFLFNTSMLVDYGVEALVDAFSRQRAGRIGGGRNFDVHV  1402

Query  447   LHVAVDVIKESREMRLQPFNEYRKRFGLKPYTSFQELTGEKEMAAELEELYGDIDALEFY  506
            LHVAVDVIKESREMRLQPFNEYRKRFGLKPYTSFQELTGEKEMAAELEELYGDIDALEFY
Sbjct  1403  LHVAVDVIKESREMRLQPFNEYRKRFGLKPYTSFQELTGEKEMAAELEELYGDIDALEFY  1582

Query  507   PGLLLEKCQPNSIFGESMIEMGAPFSLKGLLGNPICSPEYWKPSTFGGDVGFNLVNTASL  566
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Sbjct  1583  PGLLLEKCQPNSIFGESMIEMGAPFSLKGLLGNPICSPEYWKPSTFGGDVGFNLVNTASL  1762

Query  567   KKLVCLNTKTCPYVSFRVPDYPGDDGSVLVRRSTEL  602
            KKLVCLNTKTCPYVSFRVPDYPGDDGSVLVRRSTEL
Sbjct  1763  KKLVCLNTKTCPYVSFRVPDYPGDDGSVLVRRSTEL  1870
```

Fig. 3 Single portion of the pairwise alignment of input sequence

5 Conclusion

It has been shown to a good extent curiosity in phylogenetic systematic. The reason is that it is a way for biologists to generate the sequences that have helped in distribution and variety of life. It is required to develop tree building strategies that discover the process of evolution. These forms of strategies have gained importance with the advent of biological science. In this work, we have reconstructed the phylogenetic tree for COX with DNA sequences using the TBLASTN algorithm in the sequences which are used in reconstruction of the tree. The trees are generated using different algorithms in the ClustalW approach along with the multiple sequence alignment which mainly used the UPGMA algorithm for generating the trees like Fast tree, PhyMl tree, and RAxML tree.

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Photorealistic Image Synthesis Using SPADE Algorithm

Sai Charan Pedduri, Sai Ruchith Reddy Ginnavaram, Madhu Bala Myneni, and B. Padmaja

Abstract Synthesizing high-resolution photorealistic images is playing a vital role in construction of user control on semantic image information in visual processing applications. This is a major challenge in deep learning to address both semantic control and style in synthesizing images. The existing deep learning models will take input as semantic layout and processed through a number of convolution, normalization, and nonlinear layers. In this process, the semantic information of a given image is lost due to multilayer process. This paper explains an alternative approach to address the said issue with SPADE algorithm. Training and testing the model was performed with various sizes of data from COCO dataset.

Keywords Image-to-image translation · Semantic segmentation map · SPADE · Pix2pix · Pix2pixhd · Photorealistic image

1 Introduction

Photorealistic image synthesis is a process to generate an image that evoked from the visual perception system [1] by the authentic environment. In generative model research, the major aim is to learn the model to map from a semantic text to a complex RGB image space. The state-of-the-art deep generative models used in image-to-image translation are GAN [2] and variation auto-encoder (VAE). These are used for substantial applications like image synthesis, pix2pix translation [3], CRN [4], SIMS [5], Pix2PixHD [6], etc. Earlier methods like SIMS which is an image translation

S. C. Pedduri (✉) · S. R. R. Ginnavaram · M. B. Myneni · B. Padmaja
Institute of Aeronautical Engineering, Hyderabad, Telangana 500043, India
e-mail: charan.pedduri@gmail.com

S. R. R. Ginnavaram
e-mail: sairuchitreddy005@gmail.com

M. B. Myneni
e-mail: baladandamudi@gmail.com

B. Padmaja
e-mail: b.padmaja@gmail.com

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technique, which can produce images by stitching pieces from database of images, but this process requires large databases and the image produced is of low quality. In this paper, a novel end-to-end method is proposed to model with high-resolution image statistics and used to generate images with high quality.

This was implemented with PyCharm or any other python handling software which can integrate the hierarchy of the code. Python 3.6 interpreter was used with the following modules, keras, OpenCV, Pytorch, TensorFlow, with hardware support of Nvidia GeForce GTX 1070 ti GPU with 8 GB memory. The data used to train and test the model is in Giga bytes. Hence, it is highly recommended to use multiple GPU's or advanced GPU's like Nvidia titan, NvidiaRTX, which are having more memory (>4 GB) for faster results.

2 Generative Adversarial Network

Generative adversarial network (GAN) [2] is a deep neural network architecture which was introduced by Ian Good fellow and his colleagues in 2014. In this paper, authors has discussed that a generative adversarial network is one set of generative model which means they are able to generate new data content. The main focus of GAN is to generate data from scratch, i.e., a random noise, and the objective of this model is to generate and discriminate images using two neural networks, a generator and a discriminator, respectively.

Wang et al. [6] has introduced Pix2PixHD conditional GAN model used for high-resolution image synthesis and semantic manipulation. Pix2PixHD is an image-to-image translation technique which uses GAN [2] to generate a photorealistic image from a semantic mask. Unlike Pix2Pix, Pix2PixHD has evolved by using multilevel generator and discriminator which not only gives a good quality of image than cascaded refinement network but also gives an image of desired resolution. In this multiple generators are used for generating output data, and same number of discriminators is used to derive the accuracy of the output produced by the generators.

Isola et al. [3] proposed a novel image-to-image translation model with conditional adversarial networks. It is one type of generative model used to generate photorealistic images from a given semantic image. In this process, the random noise is given as input to the generator; then, it convoluted and upsampled to generate an image. Subsequently, this image is passed on to the discriminator along with the input semantic mask which is convoluted and downsampled. It produces output as a single value between 0 and 1 for determining the accuracy of generated image to be real or fake. If the value is fake image, then we back propagate to generator or discriminator for adjusting weights and to maximize error in generator and to minimize error in discriminator.

Chen and Koltun [4] introduced cascaded refinement networks—CRN for photographic image synthesis. In this paper, authors have explained about cascaded refinement network which is a process of rendering a photorealistic image from a two-dimensional semantic label map. The results obtained by CRN were stated to be

better compared to various generative models along with pix2pix [3]. Dumoulin et al. [7] have proposed an artistic style transfer technique with learned representation. This is the unique process of converting an image into a desired style of painting using style transfer network with conditional instance normalization. Qi et al. [5] have proposed a semi-parametric image synthesis for generating photorealistic image from a semantic segmentation mask. The process is explained by taking semantic layout with different semantic labels. The semantic layout and the canvas are then taken as input to synthesis network which fill the missing regions, arrange retrieved segments, and then adjust the boundaries to maintain a photorealistic appearance.

Kingma [9] have proposed a variation auto-encoder Bayes model [11]. It is a generative model. It has two networks and encoder and a decoder in which the encoder takes the data and converts that into a latent vector format. The latent vector is then reconstructed to its original form. Their focus is to represent a hidden representation of input by minimizing the reconstruction loss. GAN applications in various areas are natural image synthesis [12], contextual classes [13].

3 Deep Neural Network Architectures

Generative adversarial network (GAN) is a deep neural network architecture which was invented by Ian Goodfellow and his colleagues in 2014. Generative adversarial networks belong to the set of generative models which means they are able to generate new content.

The main focus of GAN [2] is to generate data from scratch, i.e., a random noise, and the objective of this model is to generate images using two neural networks, a generator and a discriminator. A simple architecture of GAN is shown in Fig. 1.

3.1 Generator

The generator's objective is to model data that is very similar to the training data. Generator needs to generate data that is indistinguishable from the real data. Generated data should be in such a way that the discriminator is tricked to identify it as a real image. A generator is a neural network used to generate fake data instances by using random noise. The random noise is obtained from latent space vector which

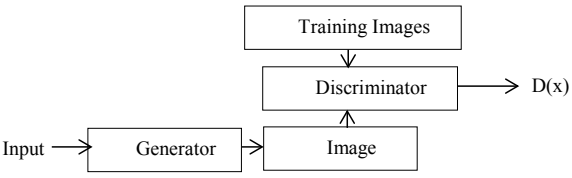

Fig. 1 Simple architecture of GAN

is in a vectorized format that can be obtained by passing an image through image encoder.

3.2 Discriminator

The discriminator's objective is to identify the data generated from the generator is real or fake. Discriminator gets two sets of input data: One is from the generator, and other is from the training dataset. Generator and discriminator are adversarial to each other; hence, it is named as generative adversarial network. The discriminator is a neural network, which gathers trained dataset and takes image generated by generator, and then evaluates the accuracy of the generated image between 0 and 1.

3.3 Training a GAN

Discriminator is trained with the help of generator, where both generator and the discriminator are trained together with the trained set images. Then, the images are fed into the discriminator with generated images and a latent space vector is passed to the generator to get a generated image as output, and then, it is passed as input to the discriminator which evaluates the image as real or fake. The two scenarios are shown in Figs. 2 and 3. If the result is a fake image, then it backpropagates to generator and

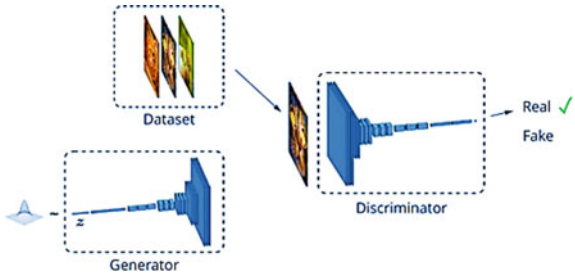

Fig. 2 Feeding a discriminator with data from dataset

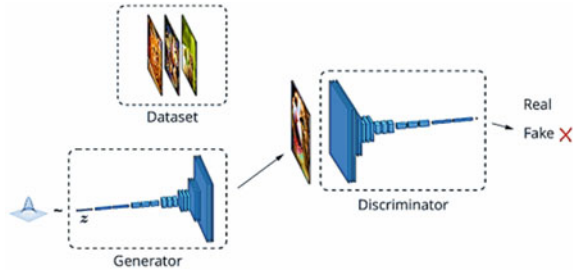

Fig. 3 Feeding data to discriminator which is generated from generator

discriminator to adjust the weight and bias for better results. This process is repeated until the generator is trained and the loss function is less, because it cannot be over trained, which generates photorealistic image.

3.4 Loss Function

Loss function is used to maintain the balance between the training of generator and the discriminator. This is not effective in practice when the generator is poor and the discriminator is good at finding fake images with high confidence. In general, the loss function should go up/down based on the learning levels of discriminator/generator. The loss function of the original GAN used to represent a measure of how often the discriminator classifies real images as real and how well it detects fake images.

$$L_{\text{GAN}} = \left[E_{(s,x)}\left[\log D(s, x)\right] + E_s\left[\log(1 - D(s, G(s))\right]\right]$$

In the Equation log $D(s, x)$ is used for identify the accuracy on real images and $\log(1 - D(s, G(s)))$ is used to identify the accuracy on fakes, where $D(s, x)$ is referred to as discriminator and $G(s)$ is referred to as generator.

3.5 Pix2PixHD

Pix2PixHD [6] is an image-to-image translation technique that uses GAN [2] to generate a photorealistic image from a semantic mask. Unlike Pix2Pix [3] which uses generative adversarial networks and has generator and discriminator networks which are used to generate the image from a semantic mask, Pix2PixHD has evolved by using multilevel generator and discriminator which not only give a good quality of image than any other models but also give an image of desired size. The simple Pix2PixHD generator is shown in Fig. 4.

Training a Pix2PixHD model for generating high-resolution images was done by using three discriminators of identical structure in which each output is of different scales (ordinary scale, downscaled 2x, and downscaled 4x) and for loss function VLSGAN [8] is used, and to make the generator output more realistic, we include

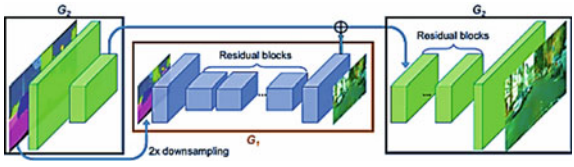

Fig. 4 Pix2PixHD generator

Fig. 5 Pix2PixHD discriminator

another designed term which helps fooling discriminator. A sample Pix2PixHD discriminator is shown in Fig. 5.

3.6 Variational Auto-encoder

Variational auto-encoder [9] is an auto-encoder technique used to encode and decode an image. In variational auto-encoder, the image is passed through different convolution layers and image downsampled by deriving two values mean and variance of image; then, depending on that, we derive a latent space vector representation as shown below; the latent space is then upsampled by using activation function. Additionally, we generate KL divergence loss to reconstruct loss for the output image. Image encoder in variational auto-encoder used to encode style image to generate mean (μ) and standard deviation (σ^2). The architecture of auto-encoder is shown in Fig. 6. Other variations in GAN architectures such as time scale update rule [14], geometric GAN [15,16], projection discriminator [17], Conditional image synthesis [18].

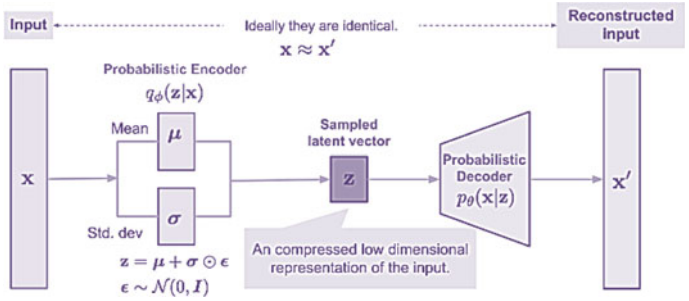

Fig. 6 Variational auto-encoder architecture

4 SPADE

Spatially adaptive denormalization (SPADE) [10] is an algorithm which was developed by Nvidia which aims to learn a mapping function which can convert an input segmentation mask to a photorealistic image.

SPADE is a generative neural network, which results in major similarities with the generative adversarial network, but there are some changes in the internal functionality of the generator and the discriminator.

SPADE algorithm aims to generate a photorealistic image by using Pix2PixHD method to form images according to the given segmentation mask which is explained in Fig. 7. The SPADE uses multiple generators and discriminators. In the generator, a customized residual block called SPADE ResBlk is used to generate the fake image. And in the discriminator to normalize the data, a spectral normalization is used instead of instance normalization. The architecture of SPADE is shown in Fig. 8.

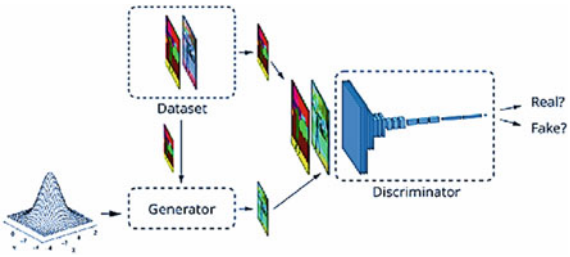

Fig. 7 Data flow in SPADE

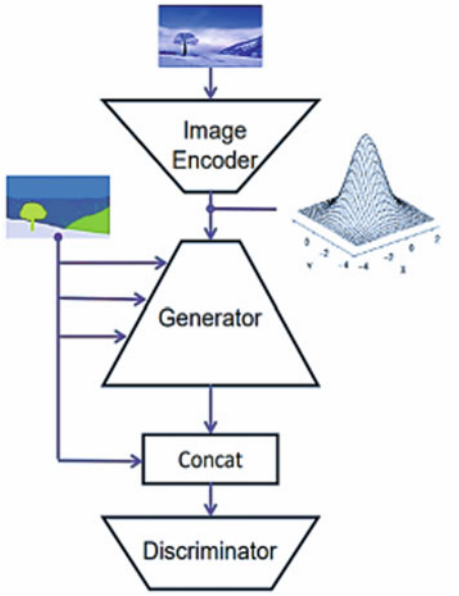

Fig. 8 SPADE architecture

4.1 SPADE Generator

The functioning of the SPADE [10] generator is similar to the generator used in generative adversarial network, with an exception of replacing the dense layers with the SPADE ResBlk blocks. In SPADE generator we sandwich the SPADE ResBlk between upsampling layers. Unlike Pix2PixHD, there is no need to give the segmentation mask as the input for the first layer of the generator. We can give the random vector as input to the first layer similar to the GAN. Now, the segmentation map has come to side of the hierarchy; i.e., we give segmentation mask as input to the SPADE ResBlk. The advantage of this process is that we can generate different images from single segmentation mask. Here, each SPADE block uses the segmentation mask to modulate the layer activations.

4.2 SPADE Discriminator

SPADE discriminator is similar to the discriminator of Pix2PixHD model, which uses a multilayer design with instance normalization, but the only difference is that we apply spectral normalization to all the convolutional layers. The discriminator takes concatenation of both the segmentation mask and the generated image from the generator as input and classifies it as fake or real.

In discriminator, we have used a 4×4 filters to downsample the data. These are convoluted with the help of spectral normalization. The images are convoluted with respect to the depth of the data. The number of layers increases accordingly the size will increase and finally the data is represented in a vector format to discriminate. Whether the given image is fake or real will decide with the help of the ground truth vector. The output is typically represented as a vector of numbers, where the number is from 0 to 1 representing the network's confidence that the image belongs to each class. With the help of the above vector, an error value between 0 to 1 is generated. If the error value is high (the value is nearing to zero or less than the required value for example if the confidence rate is fixed to 0.8, but the error rate is 0.75; then, it is considered to be fake), then the process is backpropagated.

4.3 Training SPADE

We start by providing a random noise to the SPADE generator which is upsampled and fed to the SPADE block inside the SPADE ResBlk. The data is then processed through the SPADE ResBlk; then, it is upsampled; this process is continued until the desired size of the image is obtained; this output image from the generated is the generated image or the fake image. By above training, the discriminator learns a loss

function for the generator, which helps in stabilizing training as the generator has to produce natural statistics at multiple layers.

The combination of all this loss is the reason for the better training of the SPADE [10] image than the Pix2PixHD [6] where both are generative models, and the aim is the same to generate images which look real. For every 10 epochs of training, there is a checkpoint created for discriminator and generator. Using this checkpoints, photorealistic image is generated for the given semantic map in testing phase.

5 Results and Discussions

The values of GAN, GAN-Feat represents the GAN loss and GAN feature loss respectively, which are obtained by the loss calculated while training the dataset. The GAN loss in SPADE [10] is obtained from the torch package in python by taking the minimum values out of each tensor and finding the mean of the minimum values. The VGG loss is obtained from a pretrained VGG network which is called as perceptual loss. The D_Fake and D_real loss are the loss values which are obtained due to the generated image and the real image which is sent to the discriminator while training these values are generated similar to the GAN loss.

5.1 Quantitative Results

As shown in Table 1, the values are obtained by training a set of 100 images from COCO dataset for a size of 50 epochs (an epoch is passing the dataset forward and backward through all the layers of a neural network). The average time taken by each epoch for training is 45 s, and the total time taken to complete the training is 38 min approx. The comparison of results on 100 sample image dataset consideration of 50 epochs on variant deep neural network architectures like GAN, GAN-Feat, D_Fake, and D_real is presented in Table 1.

The visual representation with comparison of semantic segmentation mask and results of SPADE model are given in Fig. 9.

6 Conclusion

Photorealistic images synthesis with deep neural network variants is discussed elaborately. With the help of SPADE algorithm, we can generate photorealistic images by training different dataset. As the training data in the dataset increases, the accuracy of generated image increases. Using this model, many applications can be built; depending on the use of the application, the suitable datasets should be created, and

Table 1 Values obtained by training 100 image data samples with 50 epochs

Epoch	GAN	GAN-Feat	VGG	D_Fake	D_real
1	−0.156	17.501	11.890	1.340	0.656
2	0.470	22.456	12.156	0.607	0.992
3	1.096	16.239	14.533	0.436	1.305
4	0.382	15.787	12.887	0.928	0.623
5	−0.628	13.836	9.905	1.847	0.398
6	0.865	15.747	11.236	0.405	0.719
7	0.208	13.018	10.882	1.872	0.246
8	1.261	9.409	9.388	0.713	1.667
9	0.143	8.041	5.373	1.004	1.141
10	0.636	15.275	13.577	0.591	0.257
11	0.701	17.626	10.608	0.767	0.106
12	0.786	16.446	11.341	0.982	0.040
13	0.182	10.644	9.804	0.617	0.672
14	0.984	11.797	9.405	0.211	1.200
15	0.746	12.441	9.553	0.422	0.217
16	1.420	12.607	13.612	0.080	1.218
17	1.197	14.747	12.245	0.454	0.200
18	−0.358	12.149	13.938	2.056	0.117
19	2.088	12.500	12.159	0.105	1.453
20	1.951	11.100	9.326	0.126	0.520
21	1.702	9.908	8.746	0.273	1.653
22	0.440	13.242	12.032	1.127	0.168
23	−0.305	10.607	13.378	1.790	0.167
24	1.172	12.427	13.019	0.212	0.625
25	0.177	10.648	12.795	0.902	0.316
26	1.282	9.640	11.542	0.417	1.802
27	−1.227	12.010	9.835	2.579	0.010
28	2.026	10.263	10.963	0.189	1.221
29	0.181	9.487	10.556	0.713	0.858
30	−0.012	12.296	12.988	1.576	0.017
31	0.948	9.496	10.278	0.728	0.643
32	0.197	13.415	11.890	1.025	0.413
33	0.300	8.801	9.271	0.829	0.858
34	0.040	8.900	10.980	1.371	0.182
35	1.267	12.390	9.858	0.293	0.157
36	1.520	12.826	12.171	0.178	0.307

(continued)

Table 1 (continued)

Epoch	GAN	GAN-Feat	VGG	D_Fake	D_real
37	1.545	10.867	13.317	0.448	1.191
38	0.737	10.740	10.405	0.320	0.909
39	1.826	11.579	14.663	0.072	1.014
40	1.263	10.513	13.146	0.533	0.340
41	1.662	11.813	10.745	0.173	1.130
42	0.995	11.118	13.296	0.261	0.913
43	2.151	8.782	11.509	0.075	1.502
44	1.086	4.520	4.209	0.126	2.166
45	0.658	9.668	10.317	0.789	0.683
46	0.886	9.442	13.035	1.080	0.281
47	1.094	11.723	13.731	0.680	1.023
48	1.522	11.510	11.224	0.276	0.721
49	0.589	10.404	14.023	1.038	0.332
50	0.908	11.697	15.162	0.567	0.083

Note These results are obtained by using SPADE model under some limited conditions, and these results may vary with respect to different datasets and different sizes of dataset

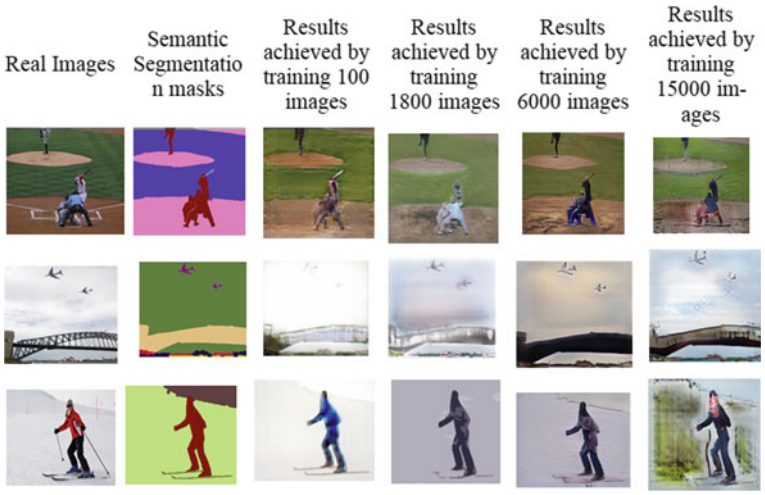

Fig. 9 Visual comparison of real images with semantic synthesis masks and result of SPADE model with 100 training dataset

by training the dataset, we can obtain a photorealistic image for the given semantic map.

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A Study on PKL Electrochemical Cell for Three Different Conditions

K. A. Khan, M. A. Saime, M. Hazrat Ali, S. M. Zian Reza, Nazmul Alam, Md. Afzol Hossain, M. N. F. Rab, and Shahinul Islam

Abstract It has been conducted this research work to measure the short-circuit current (I_{sc}) and capacity (C = AH) for different conditions of the PKL (Pathor Kuchi Leaf). The copper and zinc plates have been embedded between the two ends of the PKL for three different conditions like fresh leaves, dry leaves and living leaves to make PKL electrochemical cells. The plates were kept tightly binding by plastic clips. A sophisticated multimeter was used to measure the short-circuit current (I_{sc}). The short-circuit current was recorded after 12 h interval. It was seen that the obtained maximum current was 0.7 A for living PKL tree and the minimum current was recorded for dry PKL about 0.10 A for dry PKL. The variation between maximum and minimum short-circuit current difference is for dry PKL is 0.14 A, for

K. A. Khan (✉)
Department of Physics, Jagannath University, Dhaka 1100, Bangladesh
e-mail: kakhan01@yahoo.com

M. A. Saime
Dinajpur Polytechnic Institute, Dinajpur, Bangladesh
e-mail: abu.saime@gmail.com

M. Hazrat Ali
Department of EEE, European University of Bangladesh (EUB), Dhaka, Bangladesh
e-mail: ahazrat31@gmail.com

S. M. Zian Reza · N. Alam · S. Islam
Department of Physics, Uttara University, Dhaka, Bangladesh
e-mail: smzianreza@gmail.com

N. Alam
e-mail: nazmulalam.shovo@gmail.com

S. Islam
e-mail: ishahinul26@gmail.com

Md. Afzol Hossain
Department of Chemistry, University of Dhaka, Dhaka 1000, Bangladesh
e-mail: afzal.chemistry@gmail.com

M. N. F. Rab
Department of Basic Science, Primeasia University, Banani, Dhaka 1213, Bangladesh
e-mail: noorfazlerab@yahoo.com

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fresh PKL is 0.10 A and for living PKL tree is 0.00 A. The maximum capacity was 67.2 AH for living PKL tree and the minimum capacity was 2.16 AH for dry PKL. This type of works has been conducted by us for the first time in Bangladesh. It will help the poor for practical power applications with solar photovoltaic systems. There are some differences from the SPV (Solar Photovoltaic System). The SPV system did not work at night and rainy season. But these PKL power woks equally both day and night time. Furthermore, the PKL power technology is new and innovated technology in Bangladesh whereas the SPV device was innovated by a Russian scientist. For better performance of the PKL electrochemical cell, Some Performance and operation characteristics of the PKL electrochemical cell like input–output curves, efficiency curves, heat rate and incremental curves have been conducted. Finally, the performance of the PKL electrochemical extract cell has been studied by magnetic stirrer with hot plate. It is found that the performance of the PKL cell increases after making oscillation for PKL filtered extract by magnetic stirrer with hot plate.

Keywords Capacity · PKL electrochemical cell · Living leaves · Fresh leaves · Dry leaves · Short-circuit current · Operation characteristics

1 Introduction

Energy is the driving force of human civilization [1, 2]. To keep in mind it has been conducted research work on PKL power system [3, 4]. It is a very new and innovative work around the globe. It has been patented by the first author. Now a day some developing countries are facing problems with electricity. They are using solar electricity at the off-grid areas [5, 6]. Now it can be started PKL power for lighting purposes. The traditional source of electricity will be finished within 2100 across the globe [7, 8]. Then we have to depend on renewable energy sources. PKL power is the application of biomass energy. Our research work will be the guideline of practical applications of new electricity in the near future [9]. The definition of capacity of a PKL electrochemical cell is how much current you will get for how long time [10]. Most of the results have been tabulated and graphically discussed. The traditional sources of energy are diminishing rapidly day by day rapidly [11, 12]. That is why scientists are trying to face the future energy crisis through renewable energy [13, 14]. Biomass energy sources are one of the most important sources of renewable energy sources across the world [15]. In this research paper, biomass energy source has been used in a different and innovative way. For better working of the PKL electrochemical cell, some performance and operation characteristics of the PKL electrochemical cell like input–output curves, efficiency curves, heat rate and incremental curves have been conducted. PKL has been used in three different ways for electricity extraction. Finally, comparative studies have been conducted among three different PKL extracts based electrochemical cells.

2 Methodology

2.1 Capacity and Short-Circuit Current of and PKL Electrochemical Cell

The definition of capacity (C) of a PKL electrochemical cell is how much current you will get for how long time. The short-circuit current (I_{sc}) means—the current without load. Figure 1 shows the method of the experimental set up for measurement of short-circuit current (I_{sc}) and capacity (C = AH) of a PKL electrochemical cell for living PKL tree, dry PKL, and fresh PKL. It has been collected living PKL tree first. Then leaf has been picked from the living PKL tree. This leaf was treated as a fresh leaf. After collection of the leaf, it has been dried and treated as a dry leaf. The short-circuit current has been collected from living, fresh, and drying leaves with a calibrated multimeter. The tabulated data is shown in Table 1. The data was collected every 12 h interval.

(a) power from living PKL tree

(b) power from dry PKL

(c) power from fresh PKL

Fig. 1 Experimental set up for measurement of short-circuit current (I_{sc}) and capacity (C = AH) of a PKL electrochemical cell for living PKL tree, dry PKL and fresh PKL

Table 1 Data for collection of short-circuit current (I_{sc}) and capacity (C = AH)

Time duration (h)	Short-circuit current, I_{sc} (A) for dry PKL	Short-circuit current, I_{sc} (A) for fresh PKL	Short-circuit current, I_{sc} (A) for one living PKL	Capacity (C = AH) for dry PKL	Capacity (C = AH) for fresh PKL	Capacity ($C(a)$ = AH) for living PKL
12	0.18	0.20	0.7	2.16	2.4	8.4
24	0.24	0.30	0.7	5.76	7.2	16.8
48	0.20	0.25	0.7	9.6	12	33.6
72	0.15	0.23	0.7	10.8	16.56	50.4
96	0.10	0.20	0.7	9.6	19.2	67.2

2.2 Energy Cost of the PKL Electrical System

It consists the costs namely: (1) Cost of operating labour and materials, (2) Cost of supplies such as PKL extract treatment chemicals, PKL extract filtration cost, PKL extract preparation cost, PKL cultivation cost, Insulator box preparation cost, Connecting wire cost, Different helping Tools costs, Electrodes purchasing costs, and Maintenance costs. The total costs depend on the size and volume of the PKL power plant.

2.3 Performance and Operation Characteristics of the PKL Electrochemical Cell

PKL extract which acts as electrolyte and electrodes of PKL electrical system should work efficiently. Some curves are plotted to observe their performance. The various curves used are as follows:

1. **Input–output curves**: Performance of a PKL electrical system is precisely described by the input–output curve which is a graphical representation between the net energy output (L) and input (I).
2. **Efficiency curve**: The energy efficiency of the PKL cell $= E_D/E_C$, where, E_D = Total energy during charging, E_C = Total energy during discharging. Now, if V_c = Charging voltage (V), I_c = Charging current (A), T_c = Charging time (h). Therefore, $E_C = V_c\, I_c\, T_c$ and if $E_D = V_D\, I_D\, T_D$, where, V_D = discharging voltage (V), I_D = discharging current (A), T_D = discharging time (h). Therefore, energy efficiency $= E_D/E_C = (V_D\, I_D\, T_D)/(V_c\, I_c\, T_c) = (V_D/V_c)\,(I_D\, T_D)/(I_c\, T_c)$ = (Voltaic efficiency)(Columbic efficiency), where, Voltaic efficiency $= (V_D/V_c)$ and Columbic efficiency $= (I_D\, T_D)/(I_c\, T_c)$ (Table 2).
3. **Heat rate curve**: The ratio of input to output is known as heat rate (HR). Therefore, HR $= I/L$. where L = energy output and I = energy input.
4. **Incremental rate**: It is defined, IR $= \mathrm{d}I/\mathrm{d}L$, where, IR = Incremental rate, $\mathrm{d}I$ = change in input energy and $\mathrm{d}L$ = change in output energy.

2.4 Effect of Oscillation for the Filtrated Fresh PKL Extracts Use in PKL Electrochemical Cell

Figure 2a shows the open-circuit voltage before use stirrer. Figure 2b shows a magnetic stirrer with hot plate for use in PKL electrochemical cell to generate PKL electricity. The PKL extract after filtration was set up on the hot plate of the magnetic stirrer. It had been set up there on working condition around half an hour. It is mentioned that the amount of PKL extract was 250 cc. Then two Zn and Cu

Table 2 Table for energy efficiency of a PKL electrochemical cell

Time duration (h)	Voltage efficiency (%)	Columbic efficiency (%)	Energy efficiency (%)	Energy input, I (W)	Heat rate (HR) = I/L	Income rate (IR) = dI/dL	Energy output, L(W)
0	88	90	79.2	1.05	1.27	0	0.83
1	86	89	76.54	1.05	1.31	1	0.80
2	85.5	89	76.1	1.04	1.32	0	0.79
3	85	88	74.8	1.04	1.33	0	0.78
4	84	87	73.08	1.04	1.37	0	0.76
6	84	85.5	71.82	1.04	1.39	0	0.75
7	83.5	83.9	70.06	1.04	1.42	0	0.73
8	83	83.8	69.55	1.04	1.44	0	0.72
9	82	83	68.06	1.03	1.47	0.5	0.70
10	80	82	67.20	1.03	1.49	0	0.69

(a) Open circuit voltage before use of stirrer (b) Magnetic stirrer with hot plate (c) Open circuit voltage after use of stirrer

Fig. 2 An experimental set up for the use of magnetic stirrer with hot plate

electrodes were immersed partially in that fresh PKL extract to harness open-circuit voltage. The data have been tabulated (Table 2) and graphically represented. Figure 2c shows the open-circuit voltage before use of stirrer (Table 3).

3 Results and Discussion

Figure 3a shows the Variation of Short-circuit Current, I_{sc} (A) for (a) dry PKL (b) fresh PKL and (c) living PKL with the variation of time durations (h). It is also shown that the maximum current was 0.24 A and the minimum current was 0.10 A. It has been found the short-circuit current was increased up to 24 h that then it was decreased almost linearly up to 96 h. The difference between maximum and minimum short-circuit current is 0.14 A.

Figure 3b shows the Variation of Short-circuit Current, I_{sc} (A) for fresh PKL with the variation of time durations (h). It is also shown that the maximum current was 0.30 A and the minimum current was 0.20 A. It has been found the short-circuit

Table 3 Table for data collection of open-circuit voltage before and after using magnetic stirrer with hot plate

Time duration (h)	Open-circuit voltage, V_{oc} (V) before use magnetic stirrer	Open-circuit voltage, V_{oc} (V) after use magnetic stirrer
0	0.98	1.03
1	0.98	1.03
2	0.98	1.03
3	0.98	1.03
4	0.98	1.03
5	0.98	1.03
6	0.98	1.03
7	0.97	1.03
8	0.97	1.03
9	0.97	1.03
10	0.97	1.03

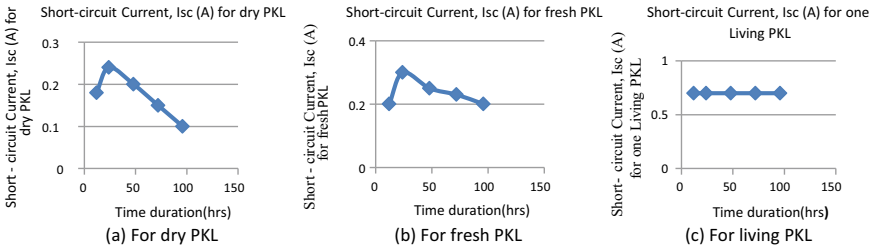


Fig. 3 Variation of short-circuit current, I_{sc} (A) for dry PKL, fresh PKL and living PKL with the variation of time durations (h)

current was increased up to 24 h that then it was decreased almost linearly up to 96 h. The difference between maximum and minimum short-circuit current is 0.10 A.

Figure 3c shows the Variation of Short-circuit Current, I_{sc} (A) for living PKL with the variation of time durations (h). It is also shown that the maximum current was 0.70 A and the minimum current was 0.70 A. It has been found the short-circuit current was almost constant up to 96 h. The difference between maximum and minimum short-circuit current is 0.00 A.

Figure 4a shows the variation of capacity ($C =$ AH) for dry PKL with the variation of time durations (h). It is also shown that the capacity ($C =$ AH) has been increased exponentially up to 96 h. The maximum capacity is 10.8 AH and the minimum capacity is 2.16 AH. The difference is 8.64 AH.

Figure 4b shows the variation of capacity ($C =$ AH) for fresh PKL with the variation of time durations (h). It is also shown that the capacity ($C =$ AH) has been increased almost linearly up to 96 h. The maximum capacity is 19.2 AH and the minimum capacity is 2.4 AH. The difference is 16.8 AH.

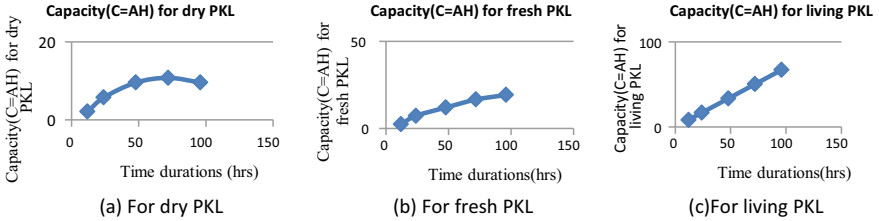


Fig. 4 Variation of capacity (C = AH) for dry PKL, fresh PKL and living PKL with the variation of time durations (h)

Figure 4c shows the variation of capacity (C = AH) for living PKL with the variation of time durations (h). It is also shown that the capacity (C = AH) has been increased linearly up to 96 h. The maximum capacity is 67.2 AH and the minimum capacity is 8.4 AH. The difference is 58.8 AH.

Figure 5a shows the energy input with the variation of energy input. It is shown that for a unit PKL electrochemical cell firstly the output and input energy is proportional and then constant and then after directly proportional and finally constant up to 10 h. Figure 5b shows the variation of energy output with the variation of time duration (h) for 10 h. It is shown that the energy output decreased linearly and slowly.

Figure 6a shows the variation of PKL energy efficiency with the variation of energy output for 10 h. It is shown that there is a correlation between output and input energy for PKL electrochemical cells. The efficiency is proportional to the energy output. Figure 6b shows the variation of PKL energy efficiency with the variation of time duration for 10 h. It is shown that the Columbic efficiency decreased linearly up to 10 h. Figure 6c shows the variation of PKL voltaic efficiency with the variation of time duration for 10 h. It is shown that the voltaic efficiency decreased up to 5 h linearly and then decreased exponentially up to 10 h. Figure 6d shows the variation of PKL Columbic efficiency with the variation of time duration for 10 h. It is shown that the Columbic efficiency decreased linearly up to 10 h.

Figure 7a shows the variation of heat rate with the variation of energy output. It is shown that the heat rate is always constant with the variation of energy output for 10 h. Figure 7b shows the variation of heat rate with the variation of time duration up

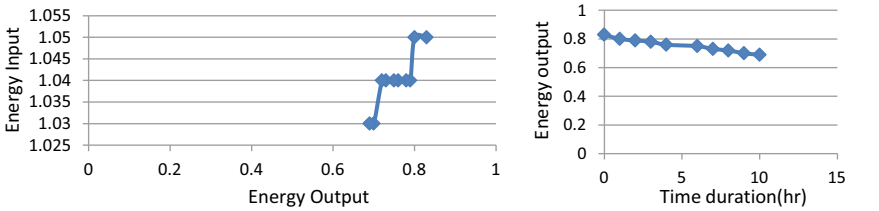
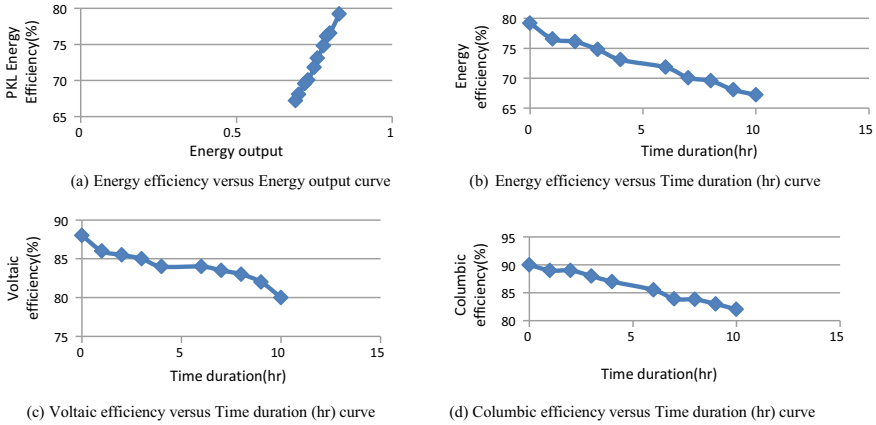


Fig. 5 Energy input versus energy output and time duration curve



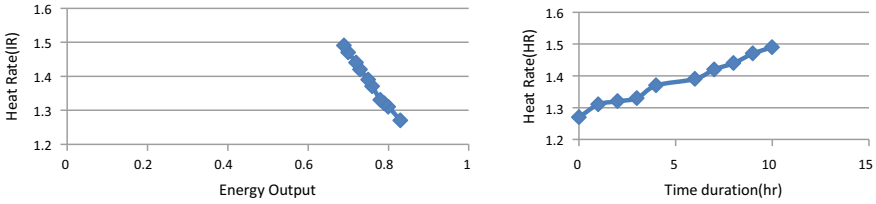
(a) Energy efficiency versus Energy output curve

(b) Energy efficiency versus Time duration (hr) curve

(c) Voltaic efficiency versus Time duration (hr) curve

(d) Columbic efficiency versus Time duration (hr) curve

Fig. 6 Energy, voltaic and Columbic efficiency versus energy output and time duration (h) curve



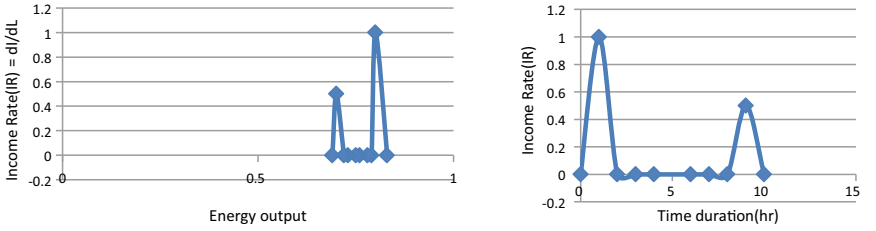
(a) Heat Rate (HR) versus Energy output curve

(b) Heat Rate (HR) versus time duration curve

Fig. 7 Heat rate (HR) versus energy output and time duration curve

to 10 h. It is shown that the heat rate increases linearly with the variation of energy output up to 10 h.

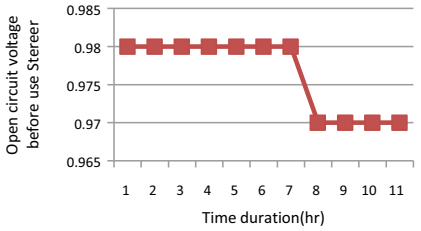
From Fig. 8a shows the variation of income rate (IR) with the variation of energy output for 10 h. It is shown that the income rate varies with the variation of change in energy output. From Fig. 8b shows the variation of income rate (IR) with the variation of time duration for 10 h. It is shown that the income rate varies with the



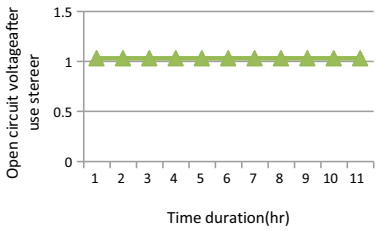
(a) Income Rate (IR) versus Energy output curve

(b) Income Rate (IR) versus time duration (hr) curve

Fig. 8 Income rate (IR) versus energy output and time duration (h) curve



(a) open circuit voltage versus time duration before use stirrer



(b) open circuit voltage versus time duration after use stirrer

Fig. 9 Variation of open-circuit voltage with the variation of time duration (h) using before and after magnetic stirrer with hot plate

variation of change in time duration. The variation is fluctuated with time duration up to 10 h.

From Fig. 9a, it is shown that variation of open-circuit voltage with the variation of time duration (h) using before magnetic stirrer with hot plate. It is shown that the voltage was constant up to 6 h and then after it has been decreased by 0.97 V from 0.98 V. Whereas From Fig. 9b, it is shown that the open-circuit voltage was constant for 10 h. The reason behind that due to applied magnetic oscillation the filtered PKL extract became more acidic.

4 Conclusions

- The obtained short-circuit current for living PKL tree is maximum among three conditions
- The obtained short-circuit current for dry PKL is minimum among three conditions
- The maximum capacity was 67.2 AH for living PKL tree
- The minimum capacity was 2.16 AH for dry PKL
- The living PKL tree is better than the other two conditions dry PKL and fresh PKL
- The performance of the PKL cell increases after making oscillation of the PKL extract by magnetic stirrer with hot plate.
- Some Performance and operation characteristics of the PKL electrochemical cell like input–output curves, efficiency curves, heat rate and incremental curves have been conducted.

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Optoelectronic Simulation of PEDOT: PSS/C-Si Hybrid Solar Cells for Different Combinations of Nanostructures

Sachchidanand and Dip Prakash Samajdar

Abstract The hybrid solar cells (HSCs) are most widespread solar cell structures among the researchers. Including nanostructure patterns in HSCs enhances its capability of trapping of light with broad range of absorption wavelength. In this chapter, we have analyzed the proposed PEDOT:PSS/c-Si HSCs with single and dual nanostructure with FDTD method by using *FDTD Solutions* and *DEVICE* software of Lumerical Inc. packages. The optical J_{sc} for each type of nanostructure-based HSC designs are obtained as 35.91 mA/cm^2 for single nanostructure-based HSC, like nanopyramids (NPs) and 36.47 mA/cm^2 and 40.94 mA/cm^2 for combined nanostructures like NP with Ag metal nanoparticles (MNPs) and NP with Al MNP, respectively. The electrical J_{sc} for the above structures are 23.66 mA/cm^2, 22.42 mA/cm^2, and 21.17 mA/cm^2, respectively. Among all these structures, HSCs with NP + Ag MNPs and MoO_3 coating achieved the highest open circuit voltage (V_{oc}) of 1.1 V, power conversion efficiency (*PCE*) of 20.36% and fill factor (*FF*) of 82.56%.

Keywords Hybrid solar cells · Nanopyramids · Metal nanoparticles · FDTD · Lumerical software package

1 Introduction

The basic principle of Photovoltaic Effect involves the generation of electron-hole pairs to produce photocurrent [1]. The absorption of the photons impinging on the SCs gives rise to this photocurrent, which makes possible the conversion of solar energy to its usable form of electrical energy [1]. Though the thin-film solar cells (TFSCs) are considered as viable options for sometime to replace the conventional SCs due to less consumption of materials and flexibility, they suffered from some serious

Sachchidanand · D. P. Samajdar (✉)
Department of Electronics and Communication Engineering, PDPM Indian Institute of Information Technology, Design and Manufacturing, Jabalpur, Madhya Pradesh 482005, India
e-mail: dippraksh010@gmail.com

Sachchidanand
e-mail: sachbade@gmail.com

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disadvantages which includes low power harvesting capability coupled with high processing cost [2]. The third generation polymer solar cells (PSCs), due to their low cost, light weight, mechanical flexibility and solution-based processing techniques, are considered to be potential alternatives to TFSCs. But these PSCs too have their drawbacks, out of which lifetime and stability are the two most vital issues, which need to be tackled [3]. Another serious concern with PSCs is low power conversion efficiency (PCE) in comparison to the older generation SCs which is mainly due to the low absorption coefficients and inefficient charge transport mechanisms in PSCs [4]. However, hybrid solar cells (HSCs), which consist of combinations of inorganic and organic active materials, constitutes the fourth generation of SCs and are significantly advantageous in terms of cost and manufacturing feasibility [5]. There are various nanostructure designs, like nanowires [6], nanopyramid [7], and metal nanoparticles [8], which enhance the light trapping properties and the absorption spectrum in HSCs.

In recent years, the effect of dual nanostructures is explored by the researchers worldwide. Wang et al. presented a double-sided nanocone structure and obtained an optimized optical short circuit current density (J_{sc}) of 34.6 mA/cm^2 [9]. J_{sc} as high as 40.67 mA/cm^2 is obtained with a unique design of nanopyramid with rear-located Ag nanoparticles [10].

In this chapter, we considered nanopyramids (NPs) and metal nanoparticles (MNPs) for PEDOT:PSS/c-Si HSCs. We have compared the effect of NP-based HSCs and NP embedded with MNP (oxide coated)-based HSCs. We have optically simulated the 3D models of both the designs using FDTD method for obtaining optical J_{sc}. For electrical simulations, the spatial distribution of light absorption is obtained with the help of the drift-diffusion and Poisson's equations. With the help of optical and electrical simulations, we have computed the electric field intensity profile, spatial power absorption profile, photogeneration rate profile, electrical J_{sc}, and $PCE(\eta)$.

2 Simulation Methodology

The optical simulation of HSCs based on different nanostructure-based designs such as NP and NP embedded with MNP (coated) is shown in Fig. 1. The FDTD method is implemented in the simulation with the help of *FDTD Solutions* software developed by Lumerical Inc. [11]. In this simulation, sunlight incident on HSCs is modeled using a plane-wave light source in the range of 300 nm to 1200 nm. We have assumed periodic boundary conditions along x- and y-direction and perfectly matched layer (PML) along z-direction as shown in Fig. 1. The frequency domain power monitors are placed above and below the c-Si substrate to visualize the reflectance ($R(\lambda)$) and transmittance ($T(\lambda)$), respectively. The total absorptance ($A(\lambda)$) can be written as:

$$A(\lambda) = 1 - R(\lambda) - T(\lambda) \tag{1}$$

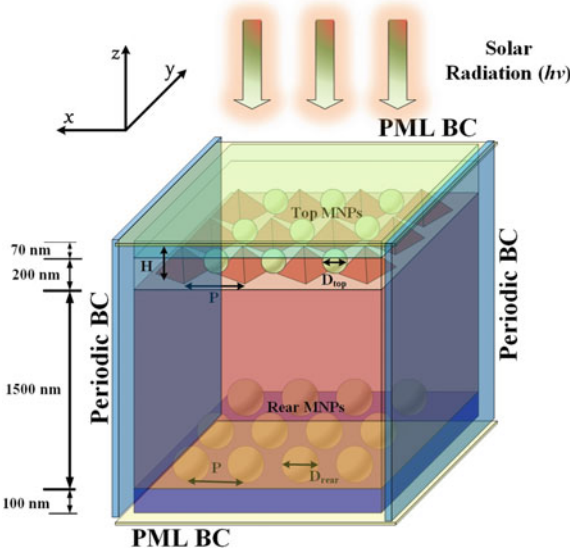

Fig. 1 Schematic of HSC designs with single and dual nanostructures

The effective thickness of c-silicon (c-Si) substrate taken as 1.5 μm for HSC designs acts as the active layer. Poly (3, 4-ethylenedioxythiophene): poly (styrene-sulfonate) (PEDOT:PSS) is chosen as the hole transport layer (HTL) [12]. Si-based NP structure can be fabricated by nano-texturing the top surface of Si substrate. Al and Ag are considered as MNP material with variable coating thickness. Palik's material database for optical data materials is used for all the materials used in the designs [13]. Al and the transparent conductor, indium tin oxide (ITO), are used as back and front end contacts, respectively. We have assumed that both types of HSC designs are periodic infinitely. Hence, the end contacts are not considered during the optical simulation.

Now, in mathematical form, we can conclude that the spatial power absorption is the product of electric field intensity and the permittivity of materials as a function of λ and the quantum efficiency (QE) of a solar cell is defined as the ratio of the number of electrons in the external circuit produced with the help of an incident photon for a specific λ and can be calculated as:

$$\mathrm{QE}(\lambda) = \frac{-0.5\omega|E(\lambda)|^2 \mathrm{Im}[\varepsilon(\lambda)]}{P_{in}(\lambda)} \tag{2}$$

where P_{in} (λ) are the powers of incident light within the HSCs, E is the intensity of electric field, ω is the angular frequency, and Ɛ is the permittivity of material. The electron–hole pairs producing the photon current can be written as:

$$J_{sc} = \frac{e}{c} \int_{300nm}^{1200nm} \lambda QE(\lambda) I_{AM1.5}(\lambda) d\lambda \tag{3}$$

where e is the charge on an electron, $\hbar$ is reduced Plank's constant, c is the speed of light in the free space, and $I_{AM1.5}$ is AM 1.5 solar spectrum.

J_{sc} can be calculated using *DEVICE* software of Lumerical Inc. with more accuracy. The drift-diffusion and Poisson's equations are calculated on finite mesh using the unit element method. The optical stimulus of total rate of solar generation from the optical simulation is imported to *DEVICE* for solving the continuity equation to obtain electrical outputs. For electrical simulation, Al and ITO are used as base and emitter electrodes with *n*- and *p*-type diffused doping of $2e + 016\ cm^{-3}$.

The electrical properties of c-Si, conductors, dielectrics, and bulk and surface recombination loss mechanisms are modeled from the predefined database of Lumerical software package [14]. Surface recombination at the two end electrodes is modeled with the assumption that the minority carriers are reflected away from end electrodes and move toward the junction [15].

3 Optimization of Nanostructures

3.1 Morphology for Nanopyramids (NPs)

The height of NP (H), base width of NP (A), and period of NP arrays (P) are optimized in terms of optical J_{sc} computed using FDTD. In our analysis, we have considered the Filling ratio (FR) of 1.0 for better optical coupling into the nanostructures because of flat bottom surface [10]. FR is defined as the ratio of A to P. The period P of NP is linked with the antireflection property of NP. The variation of J_{sc} as the function of P is shown in Fig. 2a for optimal P. From Fig. 3a, initially J_{sc} rises rapidly and reaches its maximum value at $P = 60$ nm and beyond 60 nm J_{sc} decreases steadily. The optimization of P is done in Fig. 2a with the height $H = 150$ nm and FR $= 1.0$.

For the NPs, height (H) is also an important geometric parameter in the design of SC because this significantly deteriorates the electrical performance of the SC by increasing the surface area [10]. We have considered $P = 60$ nm and FR $= 1.0$ for optimization of H. Figure 2b shows the variation of J_{sc} as the function of H of NP. As shown in Fig. 2b, J_{sc} continuously increases with increase in H of NP with highest J_{sc} at $H = 150$ nm and beyond 150 nm, J_{sc} decreases slowly. Figure 2b depicts the optimized value of H as 150 nm with $P = 60$ nm and FR $= 1.0$.

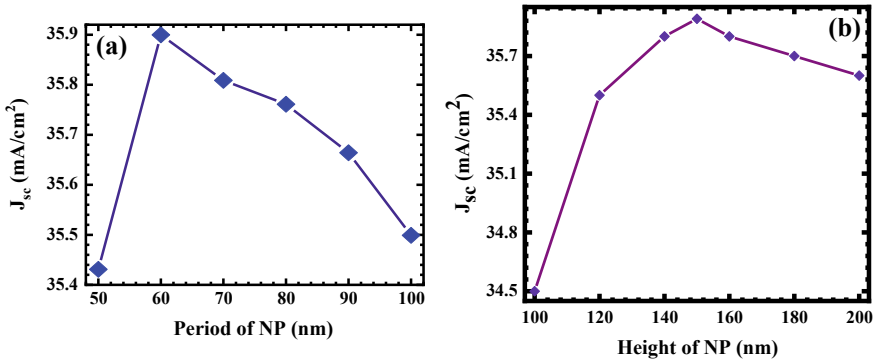

Fig. 2 Analysis of **a** period (P) and **b** height (H) of NP through variation in J_{sc}

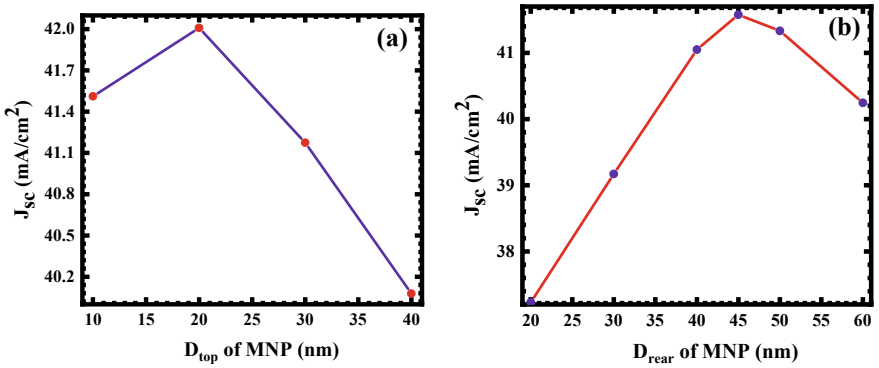

Fig. 3 J_{sc} as the function of **a** diameter of top and **b** rear MNP

3.2 Morphology for Metal Nanoparticles (MNPs)

MNPs are utilized in SC due to its plasmonic properties. To increase the light scattering in SCs and study the effect of localized surface plasmon resonances (LSPR), which helps to improve the optical absorption, we have considered two different locations of MNPs [16]. Figure 3a depicts the procedure for optimization of diameter for top MNP (D_{top}). It is evident from Fig. 3a that initially J_{sc} is constant and for $D_{top} = 20$ nm, J_{sc} increases. After $D_{top} = 20$ nm, J_{sc} decreases with increase in D_{top}. In Fig. 3b, we can see that the increase in diameter boosts J_{sc} and at $D_{rear} = 45$ nm, J_{sc} reaches its maximum value. With further increment in D_{rear}, J_{sc} reduces. Figure 3a, b depicts the optimal geometrical values of D_{top} and D_{rear} as 20 nm and 45 nm, respectively.

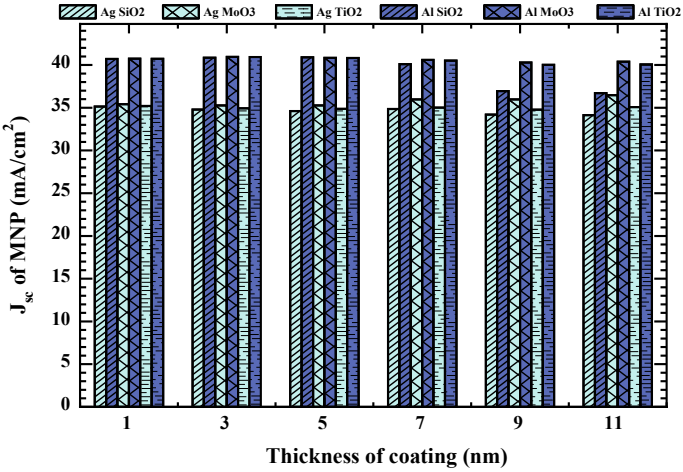

Fig. 4 Variation of J_{sc} with different oxide materials and coating thickness

3.3 Selection of Better Oxide Coating Material and Its Thickness

The oxidation of MNPS in ambient environment results in the loss of excitons which causes a significant degradation in the PCE of the SC structures [17]. In order to elimnate this serious issue, MNPS are often coated with dielectric material or polymers [18–21]. In this article, we have considered the three widely used dielectric materials such as silica (SiO_2), molybdenum trioxide (MoO_3), and titanium dioxide (TiO_2). The variation of J_{sc} using these three oxide material coatings on MNP is analyzed by varying the coating thickness from 1 to 11 nm. From Fig. 4, it can be concluded that, MoO_3 coated Al MNPs and Ag MNPs produces the highest values of J_{sc}.

4 Results and Discussions

The HSC consisting of PEDOT:PSS/c-Si with different optimized nanostructure designs by utilizing the optical J_{sc} and an assumption of 100% internal quantum efficiency (IQE) is shown in Fig. 1. Figure 5 depicts the solar spatial absorption, reflection, and transmission of incident solar power on the HSCs using Eq. 1. The absorption increases with the combination of nanostructure designs in comparison to single nanostructure due to the anti-reflection property of the HSCs [22]. As shown in Fig. 5, the absorption of NPs is high at lower wavelength region but in the higher wavelength regime, reflection increases. But, NPs embedded with MNPs exhibits a broader absorption spectra with sufficient reduction in reflection on even in the

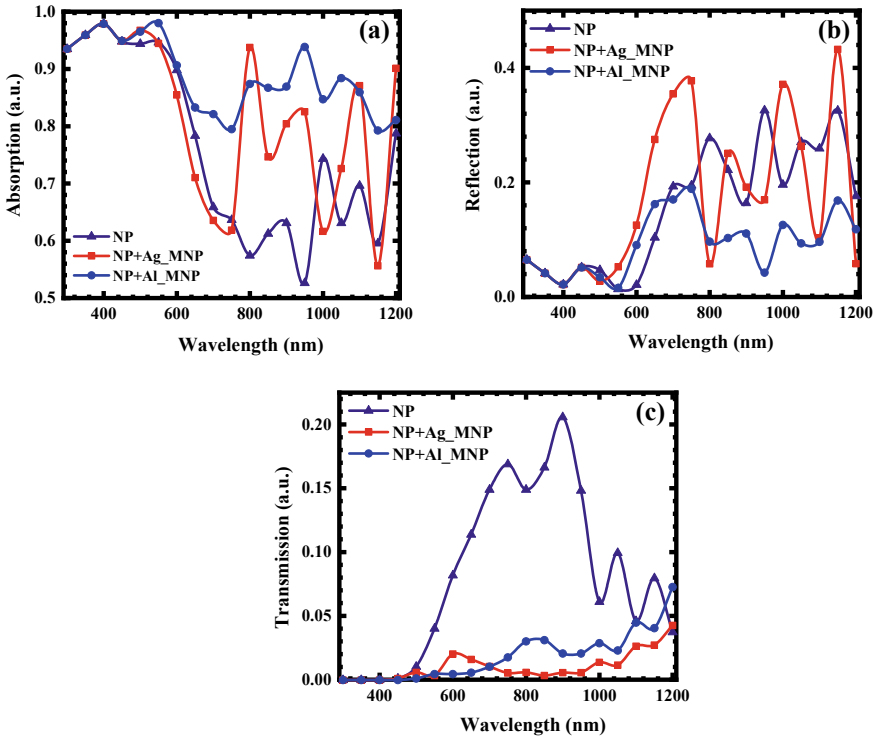

Fig. 5 **a** Absorption, **b** reflection, and **c** transmission spectrum as a function of wavelength of HSC designs

higher wavelength regime. This is also attributed to the increase in the total generation of electron–hole pair in HSCs embedded with MNPs. NPs array also show better optical coupling into c-Si substrate, which is evident from its higher absorption. Broader range of power absorption is achieved in NPs embedded with MNPs designs due to plasmonic effect of MNPs and also due to the scattering of photons due to these MNPS which traps the light within the active layer of HSCs [23].

The electrical parameters like electrical J_{sc}, open circuit voltage (V_{oc}), *PCE*, and *FF* are listed in Table 1 for all proposed HSC designs, and the maximum values of each parameter among all designs are highlighted. Figure 6 shows the *J-V* and *P-V* curves of all HSC designs including the surface and bulk recombination loss

Table 1 Electrical parameters of HSC designs

Name of design	Electrical J_{sc} (mA/cm^2)	V_{oc} (V)	η (%)	*FF* (%)
NP	**23.01**	0.48	8.73	78.37
NP + Ag_MNP (coated)	22.42	**1.1**	**20.36**	**82.56**
NP + Al_MNP (coated)	21.17	0.94	16.18	81.31

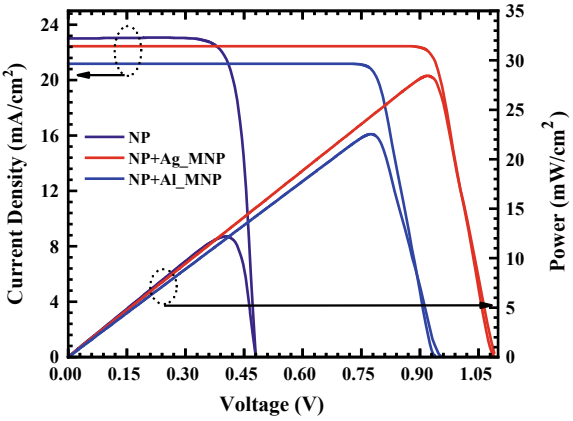

Fig. 6 *J-V* and *P-V* curves for different HSC Designs

mechanisms. The electrical J_{sc} and the overall efficiency can be calculated from the curves shown in Fig. 6 and also with the help of Eqs. 2 and 3, mathematically. The electrical J_{sc} is reduced in comparison to the optical J_{sc} due to additional bulk recombination loss mechanisms in the active layer [15].

In spite of having lower J_{sc}, the nanostructure based HSC designs have higher V_{oc}, *PCE* and *FF*. From Fig. 5b, it can be concluded that both the dual nanostructure-based HSCs help to minimize the reflections from the surfaces; however, NPs show an increment in the trapping of light in HSC designs and MNP increase the range of absorption wavelength due to near-field coupling and far-field scattering [24]. From Table 1, we can see that dual nanostructure-based HSCs have higher *PCE* and V_{oc} compared to single nanostructure-based HSC. Among all, NP embedded with Ag_MNP (MoO_3 coated) has achieved the highest *PCE* of 20.36% with J_{sc} of 22.42 mA/cm^2 and V_{oc} of 1.1 V. NP-based HSC exhibits the highest electrical J_{sc} of 23.01 mA/cm^2 but very less V_{oc} due to reverse bias saturation current and surface recombination in active layer [25]. As a result, the *PCE* is very less for NP-based HSC.

Hence, for some tricky designs such as single nanostructure-based HSC (NP-based HSC) and dual nanostructure-based HSC (NPs with MNP-based HSC), it is important to consider both optical and electrical simulation results to optimize the designs in terms of all photovoltaic parameters.

5 Conclusion

The PEDOT:PSS/c-Si HSC based on single nanostructure and dual nanostructures are simulated optically and electrically by using *Lumerical Software*. The unit cell is considered to be illuminated with a plane-wave source having power density of 100 mW/cm^2 (AM 1.5G Solar Spectrum). The optically simulated photogeneration rate profiles are imported to the DEVICE software to compute the electrical J_{sc}, V_{oc},

FF and *PCE* using suitable doping concentrations and in the presence of surface, and bulk recombination processes to obtain the best possible results close to the practical values. Thus the complete optoelectronic characterization of the nanostructure based SCs helps to a great extent to optimize the *PCE*. NPs with Ag_MNPs (MoO_3 coated) HSC yields the best results exhibiting *PCE* of 20.36%, electrical J_{sc} of 22.42 mA/cm^2, V_{oc} of 1.1 V and *FF* of 82.56% and optical J_{sc} of 36.47 mA/cm^2.

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Conflicts of interest The authors declare no conflict of interest.

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Comparative Study of Active Inductor-Based Low-Noise Amplifiers

Vikash Kumar, Shashank Kumar Dubey, and Aminul Islam

Abstract This paper presents the design of CMOS low-noise amplifier (LNA) using various types of active inductors. The inductive source degeneration topology for LNA is adopted, and three active inductors such as basic active inductor, Weng-Kuo active inductor, and regulated cascade active inductor are employed for the performance analysis. Further, the comparison of LNA characteristics such as gain and noise figure is drawn among all the designed LNAs. All the simulations have been carried out using 45-nm CMOS technology node.

Keywords Passive inductor · Active inductor · Low-noise amplifier · Gain · Noise figure

1 Introduction

The first integrated block in wireless radio frequency (RF) receivers is the low-noise amplifier (LNA). LNA is extremely significant in a receiver system where weak signals are received from an antenna and the signals are amplified to be fed to the subsequent stages. As the signal received by the LNA from the antenna is relatively weak, the LNA must have an adequate gain and noise factor (NF). The noise that is injected into the signal by the whole system is diminished by the gain of the LNA and the noise that the LNA generates is injected directly into the signal that is received. Thus, owing to the above conditions, the LNA must have a superior gain and a low noise so that good implementation of the receiver is ensured [1].

V. Kumar
Department of Electronics and Communication Engineering, Presidency University, Bangalore, KA, India
e-mail: vikashkumar@ieee.org

S. K. Dubey · A. Islam (✉)
Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra, Ranchi, JH, India
e-mail: aminulislam@bitmesra.ac.in

S. K. Dubey
e-mail: dubey.shashank1991@gmail.com

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Moreover, the physical area of the circuit needs to be as minimal as achievable, thus allowing more functional blocks to be integrated on the same chip. When the low-cost system-on-chip (SoC) applications are considering, the use of off-chip elements is a major drawback [2–4]. The design methodology brought forward can solve this problem because it is able to provide CMOS RF LNA that is fully integrated. In the proposed structure, the passive inductor is replaced with an active one, thereby decreasing the area of the circuit to a large extent. Thus, the LNA is capable of achieving a low noise factor even when on-chip inductors are used with a lower *Q*-factor than off-chip inductors or bond wires. Consequently, an active device sizing helps in achieving low noise figure at input power matching [5]. Traditional wideband low-noise amplifiers (LNAs) possess a disadvantage especially with shorter-channel devices that they are very much dependent on passive inductors which consumes a lot of area, to achieve the requirements for performance such as the matching of impedance, extension of bandwidth, and stability [6, 7]. The alternative for the area consuming passive inductors are the active inductors (AIs), i.e., the inductor made up of active element like MOSFET [8, 9]. The application of the active inductors is restricted to narrowband circuits only because of their operating bandwidth being narrow and requirement of large independent biasing current. In the narrowband circuits, these AIs achieve much larger quality factor as compared to the passive inductors [10–12]. A circuit with active inductors has smaller dimensions, quality factor that can be adjusted, inductance which can be tuned as per the requirement, and higher frequency of operation [13, 14]. In LNA, for the purpose of input and output impedance matching and output loading, inductors are used. However, due to large area consumption by the passive inductors, active inductors are suitable for this application with the restriction of being used in the narrowband frequency range. Therefore, in this paper, LNA using active inductors has been designed and implemented to operate in narrowband frequency range.

2 LNA Topologies

Several objectives are to be fulfilled while designing a LNA such as noise figure minimization of the amplifier, providing gain to the amplifier with linear characteristics, to match the impedance of 50 Ω to terminate the transmission line whose length is not known and which is responsible for the transfer of the signals from antenna to the amplifier. Several LNA topologies are used for the accomplishment of these objectives, such as:

- Common source (CS) amplifier
- Shunt–shunt feedback amplifier
- Inductive source degeneration amplifier
- Common gate amplifier.

In this paper, the inductive source degeneration amplifier topology is chosen as resistor is not used to control the input impedance (Z_{in}) in this architecture; instead,

the main component for controlling the same is the inductor. In addition, this topology has better noise figure and capable of providing specific value of input impedance at a particular frequency. The equation of gain (A_v) and noise figure (NF) of inductive source degeneration amplifier is given as

$$A_v = \frac{-g_m R_L}{2\omega_T R_s C_{gs}}, \tag{1}$$

$$NF = 1 + \frac{\gamma}{g_m R_s C_{gs}} \left(2\omega_T R_s C_{gs}\right)^2. \tag{2}$$

3 Passive and Active Inductor-Based LNA Design

This paper proposes the LNA structure incorporated with passive and active inductors. LNA with passive inductor requires larger area. Thus, MOS-based inductors are used to optimize several circuit parameters [15]. The configurations are:

a. LNA with passive inductor
b. LNA with active inductors (AI)
c. LNA with passive inductor
d. LNA with basic active inductor
e. LNA with Weng-Kuo active inductor
f. LNA with cascade active inductor.

3.1 LNA with Passive Inductors

The proposed LNA structure with passive inductor is shown in Fig. 1. Here, M_1 is the main transistor of the amplifier which provides good gain with low noise figure. The transistor M_1 along with source inductor (L_S) constitutes the inductive source degeneration amplifier. Input is provided at the gate of the transistor M_1 through gate inductor (L_G) and is coupled with the biasing arrangement for the proper functioning of the amplifier, thereby meeting the required outputs.

3.2 LNA with Basic Active Inductor

The main intention of implementing active inductor in place of passive inductor in the design is to avoid using inductors such as spiral and bonding wire inductor. The large die area requirement and a low value of fixed *Q*-factor of the passive inductor are because of CMOS providing a low resistive substrate. Moreover, they

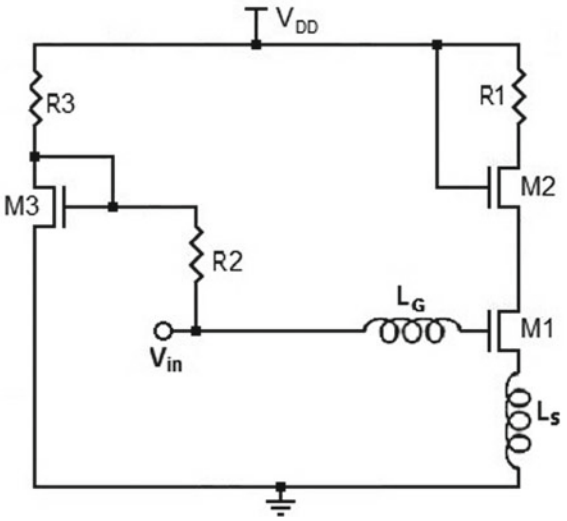

Fig. 1 Schematic diagram of LNA with passive inductor

also tend to give a single-band operation for the design due to their fixed inductance value. Despite so many techniques being proposed to enhance the Q-factor of spiral inductors in CMOS technology, the Q-factor which can be achieved is usually below 10. The other way to generate on-chip inductance is to use active devices [16]. Besides their compact implementation, the active inductors are able to achieve much higher Q-factor than their passive counterparts. The active inductor is chosen for the gain-peaking inductor to take advantage of their compact size.

The proposed LNA structure with basic active inductor is shown in Fig. 2. The characteristics of the inductor are obtained by inverting CS stage transistor (M_4) and non-inverting common drain stage transistor (M_5) which is in feedback. C_{GS4} and C_{GS5} are the parasitic capacitances of transistors M_4 and M_5, respectively. The

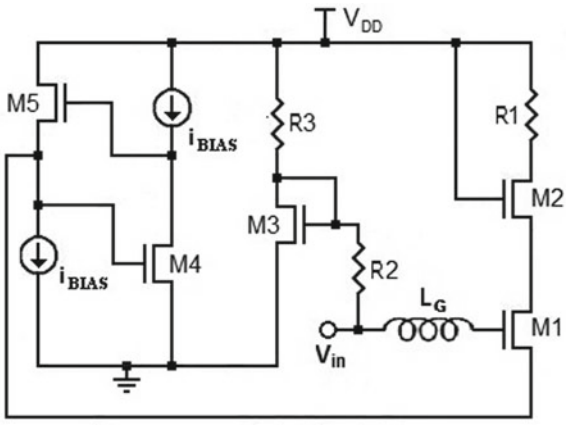

Fig. 2 Schematic diagram of LNA with basic active inductor

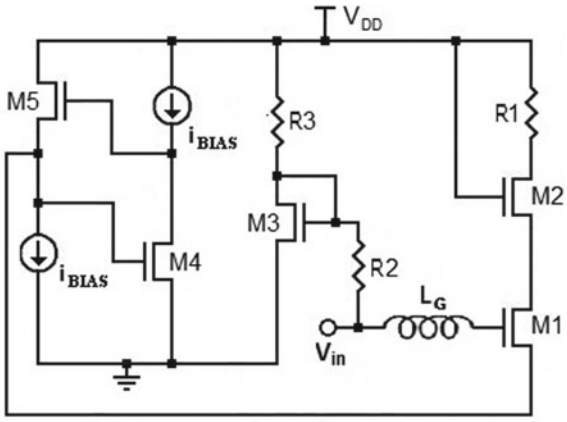

Fig. 3 Schematic diagram of LNA with Weng-Kuo active inductor

value of transconductances is changed by changing the value of current in current sources i_{BIAS} which ultimately changes the values of inductance (L). The available gain and noise figure of this LNA architecture is plotted, and it is found to show a better performance than the LNA with passive inductor.

3.3 LNA with Weng-Kuo Active Inductor

Figure 3 presents the LNA using Weng-Kuo active inductor circuit. In the Weng-Kuo active inductor, the reduction in series resistance (of basic active inductor circuit shown in Fig. 2) is obtained by a transistor which is added in cascade. As shown in Fig. 3, a transistor M_5 has been added between current source i_{BIAS} and transistors M_4. The inductance and quality factor are the parameters that can also be tuned independently by using transistor M_5. A current source i_{BIAS} has been used in the output stage. This current source is responsible for increasing the total current flowing through transistor M_4 and is also used to increase the self-resonant frequency and quality factor of the inductor.

3.4 LNA with Cascade Active Inductor

The proposed LNA structure with regulated cascade AI is shown in Fig. 4. In this configuration, the transistor M_4 and additional current source i_{BIAS} act as the feedback amplifier and regulate transistor M_6. This proposed architecture does not have requirement for an external bias for M_6 transistor. The inductive bandwidth and operation of M_6 transistor are not changed by the feedback amplifier as it is not located in the original path.

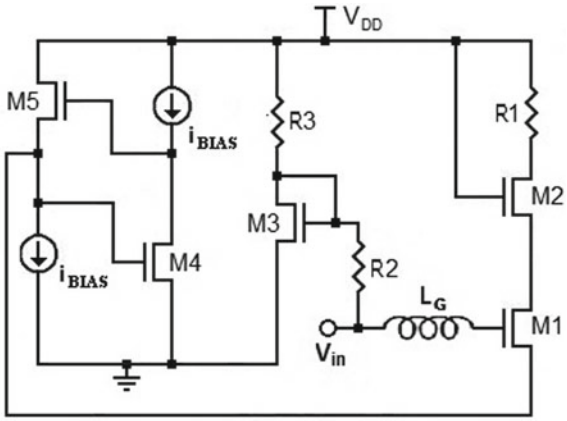

Fig. 4 Schematic diagram of LNA with cascade active inductor

4 Simulation Results

To justify the theoretical analysis, all the simulations have been carried out in virtuoso analog design environment of cadence at 45-nm CMOS technology node. The supply voltage is taken as $V_{DD} = 1.2$ V. The available gain frequency response of LNA with passive inductor, basic AI, Weng-Kuo AI, and regulated cascade AI is shown in Fig. 5 and achieves the gain value of 6.14 dB, 9.87 dB, 19.7 dB, and 24.69 dB, respectively. Similarly, the noise figure of passive inductor, basic AI, Weng-Kuo active inductor, and regulated cascade active inductor result in 3.0 dB, 3.4 dB, 4.1 dB, and 4.8 dB, respectively, and is shown in Fig. 6. Table 1 shows the performance comparison of all the inductor circuits.

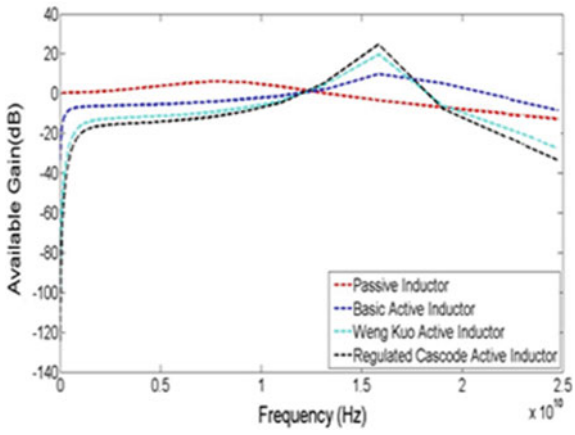

Fig. 5 Plot of available gain (dB) versus frequency (Hz) for LNA with various inductors

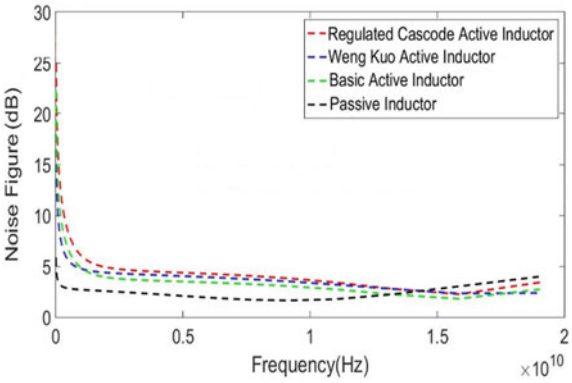

Fig. 6 Plot of noise figure (dB) versus frequency (Hz) for LNA with various inductors

Table 1 Performance comparison of LNA circuits

Parameters	LNA passive inductor	LNA using basic active inductor	LNA using Weng-Kuo active inductor	LNA using regulated cascade active inductor
Gain (dB)	6.14	9.87	19.7	24.69
Noise figure (dB)	3.0	3.4	4.1	4.8

5 Conclusion

In this paper, three different active inductors such as basic AI, Weng-Kuo AI, and regulated cascade AI are employed in the LNA architecture. It is concluded that the LNA using active inductors gives better performance in terms of available gain and noise figure as compared to LNA using passive inductors. Further, the circuit area is reduced drastically. Different topologies of the active inductors also show different performance characteristics.

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Diabetes Prediction Using Machine Learning Techniques: A Comparative Analysis

K. Pavani, P. Anjaiah, N. V. Krishna Rao, Y. Deepthi, D. Noel, and V. Lokesh

Abstract Nowadays, Machine Learning and Artificial Intelligence play a important role in the healthcare sector. Diabetes is one of the most populated diseases in the world according to WHO. It is caused due to the increased level of glucose in the body. There are some more attributes on which diabetes can be predicted. This work mainly focuses on building diabetes aided system which can predict the disease at the earliest possible stage. In this paper, we used different ML techniques to predict diabetes at initial phases. In Machine Learning, support vector machine, logistic regression, Decision Tree, Random Forest, gradient boost, K-nearest neighbor, Naïve Bayes algorithm are used. We measure these algorithms by using the following metrics (1) precision level, (2) accuracy level, (3) recall, (4) *F*-measure. The aim of this analysis is to compare different techniques to obtain better accuracy. It is observed that the Random Forest and naïve base algorithm obtained an accuracy of 80%.

Keywords Data mining · Decision Tree · Diabetes · Gradient boost · K-NN · Logistic regression · Naïve Bayes · Public health · Random Forest · SVM

1 Introduction

Blood glucose is our main source of energy, where it is obtained from the food which we intake. When the glucose level in blood is high the condition is considered to a diabetic. In our body pancreas produce a hormone called "insulin" which helps the glucose that is produced from the food gets into the cells which can be consumed as energy. In some cases or after a few years our body doesn't make sufficient insulin or stops making insulin, which leads the glucose stays back in the blood and doesn't reach the cells [1].

Over time of period, high blood sugar levels can lead to serious health problems, however, diabetes has no cure, but we can take steps towards a healthy lifestyle [2].

Diabetes is commonly classified into the following two types:

K. Pavani · P. Anjaiah · N. V. Krishna Rao (✉) · Y. Deepthi · D. Noel · V. Lokesh
Department of Computer Science and Engineering, Institute of Aeronautical Engineering, Hyderabad, Telangana 500043, India
e-mail: nvkrishnarao3@gmail.com

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Diabetes Type 1 It is the condition where our body stops making the insulin because our body immune system which usually safeguards our body from foreign invaders from causing infections and flu attack and demolishes the cells in the pancreas that produces the insulin. Type 1 diabetes people should take insulin every day in order to stay alive [3]. It is mostly seen in the children, however, it can appear at any age. This is mainly caused by genes and it depends on the environmental viruses that help initiating the diseases.

Diabetes Type 2 It is most commonly observed in middle-aged people and older people. In TYPE 2 DIABETES body doesn't cooperate in making a sufficient amount of insulin or in proper usage of the insulin. Large amount of glucose remains back in the blood and required amount of glucose doesn't reach the cells. It is more likely to be developed by people of age around 45 and above or having a family history of diabetes.

Statistics

- Diabetes cases in India are estimated up to 72.96 million.
- It statistically ranges from 10.9% in urban areas and 14.2% whereas in rural areas it is from 3.0 to 7.8%.
- Males showed a prevalence of 12% and whereas females had shown 11.7% [4].
- Among 63,000 of population aged up to 50 years or older has assisted a 90.1% of diabetes [5].

Because of diabetes, the people are facing many number of other health problems such as:

- Heart Attack
- Gastric problems
- Severe Nerve damages
- Dental diseases
- Kidney Damages
- Foot problems.

2 Literature Survey

Ayman Mir and Sudhir N. Dhage suggested a model with different algorithms such as SVM, Naïve Bayes, Simple CART algorithm, and Random Forest algorithm to predict diabetes dataset [6, 7].

Priyanka and Prof. K. Jaya Malini used ML algorithms such as Artificial Neural Networks, Naïve Bayes, Decision Tree, and SVM to save the people at initial phases of life suffering from diabetes [8].

Mr. MahaleKishor M. and Prof. DhomseKanchan B. with the ML techniques such as Decision Tree, SVM, Naïve Bayes, and by using PCA for special disease prediction [9].

V. Swathi, V. Nithya, K. Sripriya, C. Preethi, and K. Logeshwari suggested using ontology and ML techniques to predict patient diabetes risk levels [10].

Debadri Dutta, Debpriyo Paul, and Parthajeet Ghosh have analyzed feature importance for diabetes prediction using Machine Learning [11].

P. Suresh Kumar and V. Umatejaswi used the data mining algorithms such as Decision Tree, Naïve Bayes, SVM for predicting diabetes [12].

3 Proposed System

The proposed system uses the classification algorithms: Decision Tree, K-NN, Support Vector Machine, Gradient boost, Naïve Bayes, Random Forest, and Logistic regression for accuracy authentication.

Figure 1 represents the steps involved in predicting the results from data collection. Each step is briefly described below according to its functionality.

3.1 Dataset

Diabetes PIMA dataset [13].

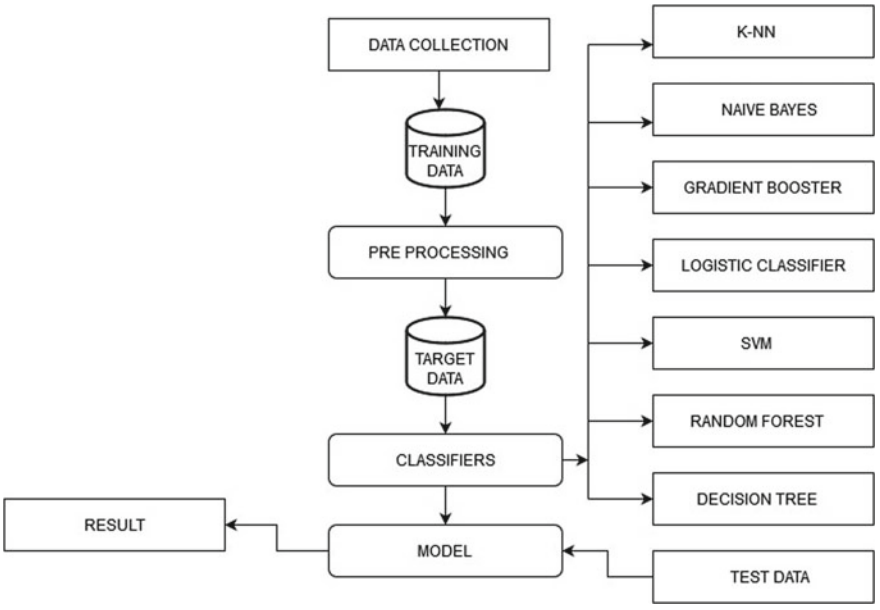

Fig. 1 Block diagram of our system

The dataset contains 768 instances and 9 features. The dataset contains the following attributes:

- Pregnancies
- Sugar level
- Blood Pressure (mmHg)
- BMI.
- Skin thickness
- Insulin content
- Pedigree factor
- Age of individual

Out of 768 instances we used 75% for training the model and the remaining 25% for testing.

3.2 Pre-processing

Pre-processing is the basic step involved before applying our data to the algorithm. It is used to convert raw data that is collected from different sources which are unsuitable for analysis into an understandable dataset.

4 Machine Learning Algorithms

4.1 Naïve Bayes

- It is a probabilistic classifier which is based on the Bayes theorem, with the strong individual assumptions and predicted values in the features.
- It is one of the simplest Bayesian models to be used and described.
- It has been broadly studied from 1960s.

4.2 SVM

- Support Vector Machine is a supervised learning model used for classification with algorithms that analyze the data in regression analysis.
- It is a model where points are in the space and are mapped to the examples of the different categories are separated perfectly and have a clear and wide gap to be distinguished in a proper way.
- Other new examples when they are mapped into the same space they are classified into that category based on the side which they are mapped.

4.3 Logistic Classifier

- It is a statistical model used to create or model a dependent variable by using logistic function.
- For modeling any certain class we use logistic technique.
- For example, Win/Lose, Alive/dead, Rich/Poor.

4.4 Random Forest

- Random forests or it is also classified as the Random Decision Forest is a group learning which is classified as a whole as one rather than individual variables for the classification.
- It also regulates with the other regression testing and other tasks that operate with a multiple decision trees at the probation time.
- The mode of classes by the outputs and the mean prediction of each individual tree.

4.5 Gradient Booster

- It is a machine language technique which is used for regression and classification solving.
- This forms prediction models in the form of multiple algorithms with weak prediction models which are basically decision trees. It is defined as the K- NN algorithm it is used for both regression and classification techniques.
- In both classified types, they contain K-nearest value, whereas the output is classified.

4.6 Decision Tree

- It is a flowchart type of structure.
- "test" of an attribute is represented by internal nodes.
- Outcome of the test is represented by each branch.
- Class label is represented by leaf node.
- This uses the tree structure of decisions and the possible outcomes of each decision including the possible consequences such as chance event outcomes, resource costs, and utility.

ML Matrix

Precision The precision represents the number of True Positive separated by the summation of True Positive and False Positive.

$$\text{Precision} = \text{True Positive}/(\text{True Positive} + \text{False Positive})$$

Recall The recall can be represented as the number of True Positives separated by the summation of True Positive and False Negative.

$$\text{Recall} = \text{True Positive}/(\text{True Positive} + \text{False Negative})$$

F-*Measure* F-Measure represents the relationship between recall and precision.

$$F\text{-measure} = 2 * (\text{Precision} * \text{Recall})/(\text{Precision} + \text{Recall})$$

5 Result Description

By applying the Machine Learning algorithms on the input dataset we will predict the results in the form of graph as shown below.

6 Results

After applying dataset to the algorithms the results obtained are categorized based on classifier algorithm which contains accuracy values on training set and test set, recall, precision, f-measure value.

6.1 K-Nearest Neighbor Algorithm

Accuracy	0.78 (Training set)
Accuracy	0.79 (Testing set)
Precision Rate	0.7142857142857143
Recall Rate	0.6716417910447762
F-measure	0.6923076923076923.

6.2 Logistic Algorithm

Accuracy	0.766 (Training set)
Accuracy	0.781 (Testset)
Precision Rate	0.6739130434782609
Recall Rate	0.5344827586206896
F-measure	0.5961538461538461.

6.3 Support Vector Machine Algorithm

Accuracy	0.75 (Training set)
Accuracy	0.79 (Test set)
Precision Rate	0.7755102040816326
Recall Rate	0.5671641791044776
F-measure	0.6551724137931034.

6.4 Decision Tree Algorithm

Accuracy	0.767 (Training set)
Accuracy	0.786 (Testset)
Precision Rate	0.7321428571428571
Recall Rate	0.6119402985074627
F-measure	0.6666666666666667.

6.5 Random Forest Algorithm

Accuracy	1.000 (Training set)
Accuracy	0.802 (Testset)
Precision Rate	0.7101449275362319
Recall Rate	0.7313432835820896
F-measure	0.7205882352941175.

6.6 Gradient Boost Algorithm

Accuracy	0.859 (Training set)
Accuracy	0.776 (Testset)
Precision Rate	0.782608695652174
Recall Rate	0.5217391304347826
F-measure	0.6260869565217392.

6.7 Naïve Algorithm Output

Accuracy	0.762 (Training set)
Accuracy	0.802 (Test set)
Precision Rate	0.7959183673469388
Recall Rate	0.582089552238806
F-measure	0.6724137931034483.

7 Conclusion

The values obtained are plotted using matplotlib in python.

Figure 2 represents a bar graph indicating the recall and f-measure values of each algorithm on test dataset.

Figure 3 represents a bar graph indicating the accuracy of each algorithm on training and test dataset.

Figure 4 represents a bar graph indicating the precision of each algorithm on test dataset.

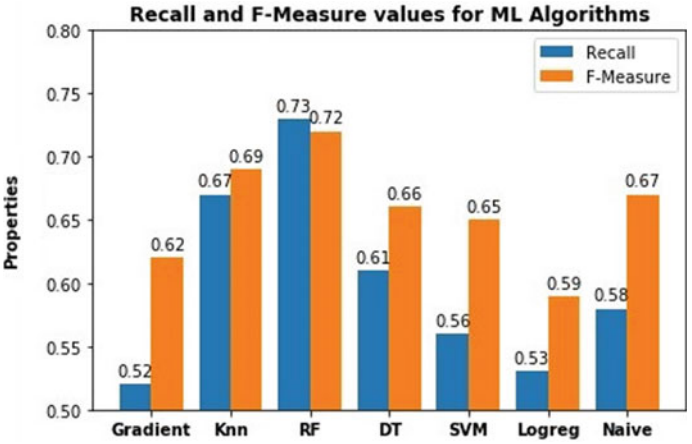

Fig. 2 Results for recall and f-measure values

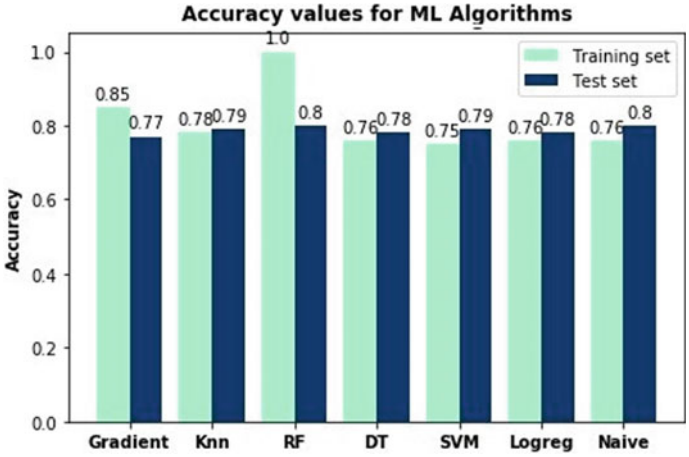

Fig. 3 Results of accuracy for training and test dataset

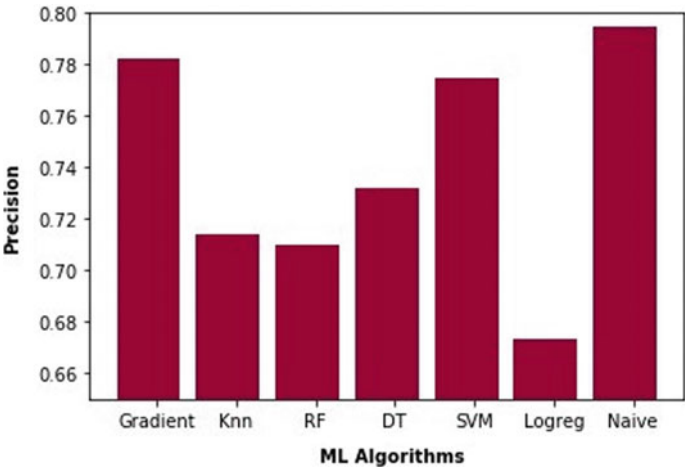

Fig. 4 Results of precision

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Design of Robust Ratioed CMOS SR Latch

Divya Sri Dodla, Sayonee Mohapatra, Yashasvi Vijayvargiya, Shashank Kumar Dubey, Vikash Kumar, and Aminul Islam

Abstract With emerging technology, devices are being scaled aggressively. Despite the benefits of scaling, variability has proved to be a major drawback of scaling. This paper presents a novel approach to alleviate the harmful effects of the process, voltage, and temperature (PVT) variations on design metrics of ratioed CMOS SR latch. In the proposed circuit the inverters are replaced by low voltage 4T Schmitt triggers which provide improved variability. The proposed circuit operates in near-threshold region. A comparison is made between the conventional and the new design using Monte Carlo simulation with a sweep of 5000 in SPICE @ 16-nm technology. A comparative analysis shows that the design metrics of the new circuit have less variability than the conventional circuit. The new technique is successful in mitigating the impact of the PVT variations in power, delay, PDP, and EDP of the ratioed CMOS SR latch.

Keywords Variability · SR · Ratioed

1 Introduction

While arithmetic and memory structures benefit from regularity, control structures usually do not. Hence, they are hard to design, test, and verify. Finite state machine is a sequential circuit and an example of control structure. Those circuits are called sequential circuits, which have combinational logic circuits and storage elements such as flip-flops/latches. Flip-flops/latches are also integral parts of various serial memory structures such as shift registers and queues. Sequential logic such as latches has been the basic building block of storage/register circuits. Plenty of Flip-flops/latches are used in configurable logic block (CLB) and input/output logic block IOB) of CPLDs/FPGAs to make them reprogrammable. Therefore, flip-flops/latches

D. S. Dodla · S. Mohapatra · Y. Vijayvargiya · S. K. Dubey · A. Islam (✉)
Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra, Ranchi, Jharkhand, India
e-mail: aminulislam@bitmesra.ac.in

V. Kumar
Department of Electronics and Communication Engineering, Presidency University, Bengaluru 560064, India

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are essential components of all control and memory circuits and hence they dominate in the entire practical devices/gadgets [1]. Among all other latches, SR type latches are more commonly in use in control and memory circuits. Improvement in the design metrics of SR latch can, therefore, enhance the design metrics of control and memory circuits resulting in the performance improvement of all practical gadgets.

The device count per chip doubles within [2] every two years and is true for decades, is the simple observation known as Moore's law [3–5]. CMOS technology has scaled aggressively to obtain higher speed of operation, greater integration density, and lower power dissipation. Scaling involves reduction in vertical (t_{ox}) and lateral (W and L) dimensions of the device. In order to maintain electrostatic control over the channel, supply voltage (V_{DD}) is reduced. To compensate for the reduced drive current and degraded performance of the device, threshold voltage is scaled. However, the scaling down of the transistors make them more sensitive to process, reliability, and environmental variability factors [6, 7]. Process variability is mainly responsible for the high delay and power consumption deviation according to [8]. Over the last 50 years due to aggressive CMOS technology scaling there are significant variations in process, voltage and temperature (PVT) parameters in ultra-deep sub-micron (UDSM) technology nodes such as 16-nm that affects the circuit's performance and limit the progress of Moore's law in future generations [9].

At advanced technology nodes, design metrics such as power-delay product-delay, power dissipation, etc. have become sensitive to fluctuations in PVT. Spreads in these design metrics due to such fluctuations have become significant, which were earlier negligible for earlier technology nodes. In ASIC (Application Specific Integrated Circuits) design, which involves bulk production of circuits, variability in design metrics results in each circuit having different behavior. This can increase the rate of circuit degradation and can make the circuit inappropriate for a given design specification [9]. This large delay/power deviations due to environmental and process variations make it is difficult to satisfy the tight bounds imposed by requirements, and thus degrades the product [10–13]. Hence, it is inevitably important to optimize the circuits not only in terms of speed, area, power, etc. but also in terms of robustness in the presence of PVT variations.

In subthreshold operation, supply voltage is less than the threshold voltage. The point of minimum energy lies in subthreshold region of operation of the MOS transistor for most of the logic families. Nevertheless, subthreshold operation offers huge performance penalty. It offers an exponential increase in delay with a decrease in V_{DD}, which causes leakage energy (the product of leakage current, V_{DD}, delay) to increase in a nearly exponential manner. Besides this, subthreshold circuits are more sensitive to parameter variations. The near-threshold region (NTR), where the supply voltage is approximately equal to or in the range of the threshold voltage of the transistors used, instead retains much of the energy savings of subthreshold operation with substantial performance and variability improvement [14, 15]. Hence to achieve the best possible tradeoff between energy and delay, the design in this paper has been proposed and simulated in NTR.

Among all the logic families, static complementary CMOS logic displays highest robustness. However, for each fan-in the number of transistors required is two. Therefore, as the fan-in increases, area required increases due to high number of transistors. In addition to this, high number of transistors provide greater load capacitance. Ratioed logic is an attempt to reduce the number of transistors required to implement a given logic function, often at the cost of reduced robustness and extra power dissipation [16].

In view of the above problems in rationed logic, this paper endeavors to make the following contribution:

- This paper proposes a circuit-level technique to reduce the sensitivity of ratioed CMOS SR latch in the presence of PVT variations.
- The key technique used here is to replace the two cross-coupled inverters in the conventional design by two Schmitt triggers.

The paper has been well ordered as follows. Section 2 introduces the proposed technique, followed by Sect. 3, which explains the simulation setup and discusses the outcomes of incorporation of proposed technique. Section 4 culminates the paper with a brief emphasis on the findings of the paper.

2 Proposed Design and Device Sizing

The SR latch circuit is shown in Fig. 1, consist of two cross-coupled CMOS inverters and two cross-coupled pseudo-NMOS inverters. The cross-coupled CMOS inverters

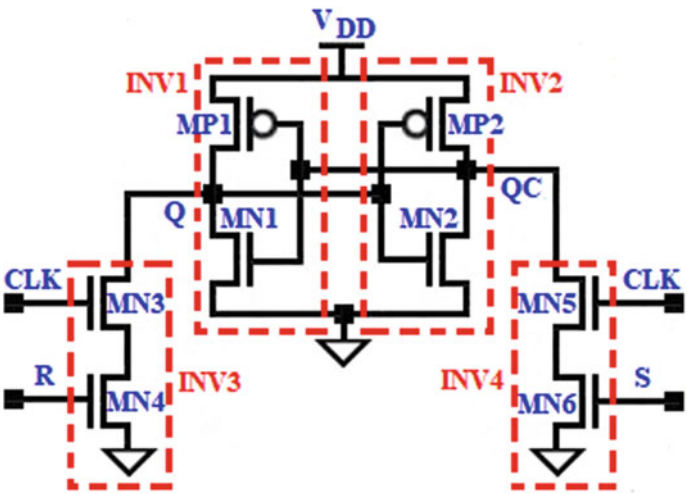

Fig. 1 Conventional ratioed CMOS SR latch consisting of a cross-coupled inverter pair and four transistors for providing the synchronization and driving the latch from one state to another

Table 1 Characteristic table of SR latch. For input $S = 0$, $R = 0$, latch retains the previous state; for the input $S = 1$, $R = 1$, output is uncertain which has been denoted as don't care term X

S	R	Q	QC
0	0	Q	QC
0	1	0	1
1	0	1	0
1	1	X	X

are composed of MN1/MP1 (INV1) and MN2/MP2 (INV2), whereas the cross-coupled pseudo-NMOS inverters are made up of MN3/4 (INV3) and MN5/6 (INV4). INV3 and INV 4 are clock-driven for its proper functioning. The state of the latch is changed only when CLK is asserted and S/R is applied.

It is desirable to keep switching voltage close to center of available voltage swing (i.e., $V_{DD}/2$) in order to achieve comparable high and low noise margin. Hence the device size for each transistor has been chosen such that switching voltage of the proposed latch is close to $V_{DD}/2$. The 1-bit data stored in the latch is changed by set and reset signals, gated with the clock. Table 1 depicts the characteristic table for SR latch and Fig. 2 illustrates the simulated waveform of the same.

Schmitt trigger exhibits the property of hysteresis by the virtue of which it can work on two different threshold voltages. To switch the output from high to low

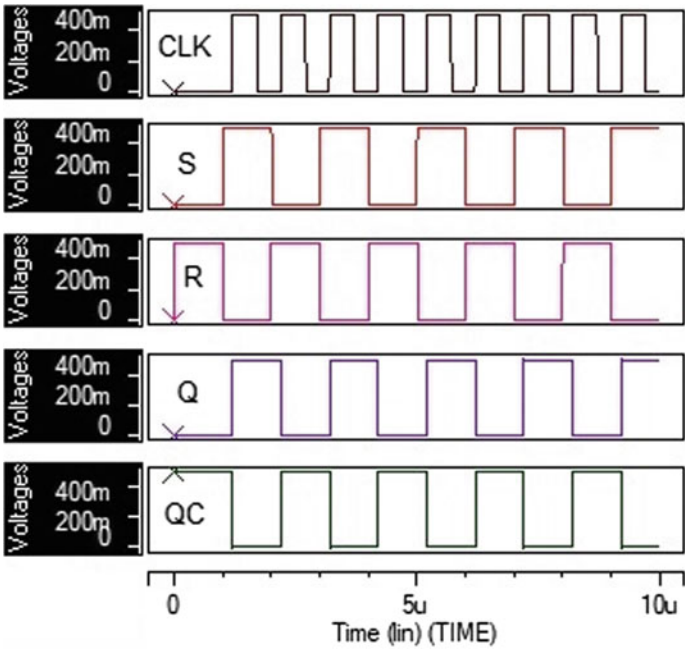

Fig. 2 Output waveforms of the conventional circuit. CLK, *S*, *R*, *Q*, *QC* in the respective order. The waveforms follow the characteristic table and the output swings fully from 0 to V_{DD}

level, the input has to surpass the upper threshold voltage whereas, for output to switch from low to high level, the input has to fall below the lower threshold voltage. Hence, for small input changes due to noise and other variations, the Schmitt trigger retains its output value. It switches its output only for large changes in input. In [17], a low voltage CMOS Schmitt trigger is proposed for operation at 3 V, where the lowering of operating voltage is limited by cascade architecture. In Ref. [18–20], Schmitt trigger has been used as the key method to enhance the noise immunity of circuits and mitigate the effects of PVT variations on circuit parameters. In [21, 22] Schmitt trigger-based soft error resistant latches have been proposed, eliminating the need for additional circuitry for error correction. In [23, 24] Schmitt trigger-based static CMOS NAND and NOR gates have been designed to improve static noise margin. The conventional 6T-CMOS Schmitt trigger has been proposed in [25]. Several modifications to the conventional design have been proposed in papers [26]. The specific parameters on which each of these designs work is controllable hysteresis, low power, high speed, gate oxide, reliability, and so on. With a view to keep the number of transistors as minimum as possible, 4T Schmitt triggers proposed in [27] has been incorporated in our design. The 4T Schmitt trigger is observed to exhibit better performance at low voltages (1 V and below) as compared to 6T conventional Schmitt trigger. This Schmitt trigger works on the concept of body biasing. Figure 3 shows the circuit diagram for the 4T Schmitt trigger. The inverting output is obtained from V_{out1} and noninverting output is V_{out2}. The forward and backward switching voltage of the Schmitt trigger depends on the threshold voltage of MOSFET used. The threshold voltage of a MOSFET depends on the voltage difference between source and body as per the equation below [16, 27]

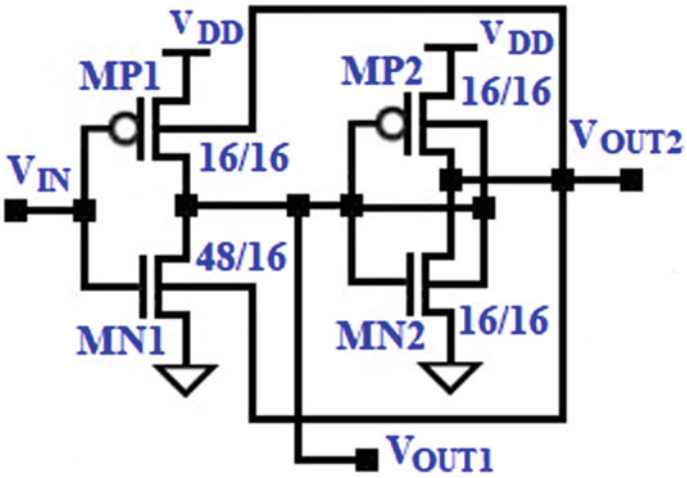

Fig. 3 4T CMOS Schmitt trigger—it works on the concept of dynamic body bias so that hysteresis offers better noise margin

$$V_{tn} = V_{tn0} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \tag{1}$$

$$V_{tp} = V_{tp0} - |2\phi_F| - \gamma\left(\sqrt{|2\phi_F| - V_{SB}}\right) \tag{2}$$

where V_{tn} is the threshold voltage of NMOS, V_{tp} is the threshold voltage of PMOS, V_{tn0} is the threshold voltage of NMOS with zero body bias with respect to the source and V_{tp0} is the threshold voltage of PMOS with zero body bias with respect to source, ϕ_F is the Fermi potential, V_{SB} is the source to body potential and γ is body effect coefficient.

It is observed that the threshold voltage increases as the V_{SB} increases. Initially, a low voltage is applied to V_{IN} which results in Vout1 to go high and V_{OUT2} to go low. This provides zero body biasing to MN1 and forward body biasing to MP1. MP1 conducts and MN1 stays OFF if V_{IN} is below the switching voltage. Since zero body bias in NMOS provides higher threshold voltage as compared to forward body bias ($V_{SB} < 0$), the switching voltage, in this case, has increased for high to low transition. The high to low switching voltage V_{HL} is calculated as below:

$$\frac{\beta_n}{2}(V_{HL} - V_{tn0})^2 = \frac{\beta_p}{2}(V_{DD} - V_{HL} - |V_{tp}|)^2 \tag{3}$$

$$V_{HL} = \frac{V_{DD} - |V_{tp}| + R \times V_{tn0}}{R + 1} \tag{4}$$

where $\sqrt{(\beta_n / \beta_p)} = R$, β_n and β_p are the transconductance parameters of NMOS and PMOS [28].

As V_{IN} increases, at the end of switching transient, zero body biasing is applied to MP1 and a forward body bias is applied to MN1. MP1 remains OFF and MN1 is ON as long as the V_{IN} is above the switching voltage. Since in the case of PMOS, the threshold voltage is lower for zero body biasing as compared to forward body bias ($V_{SB} > 0$), V_{IN} has to reach lower voltage to cause switching. Hence, the switching voltage for low to high transition is reduced. Using a similar analysis, the low to high switching voltage is calculated as [28],

$$V_{LH} = \frac{V_{DD} + R \times V_{tn} - |V_{tp0}|}{R + 1} \tag{5}$$

where all the symbols have the same meanings as defined above. The device sizing for each transistor of 4T Schmitt trigger has been mentioned in the circuit diagram. In this work, we have used this 4T Schmitt trigger to make the conventional latch illustrated in Fig. 1 variation-resistant against the PVT variations. We have replaced the CMOS inverters (INV1 and INV2) of Fig. 1 with two 4T Schmitt triggers. The proposed variation-resistant SR is illustrated in Fig. 4. The W/L dimensions in nanometer

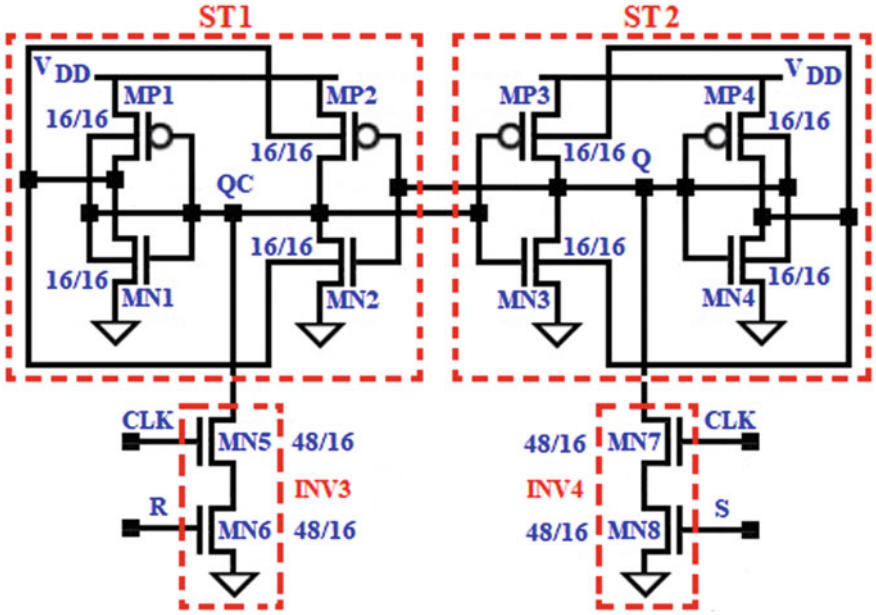

Fig. 4 Proposed ratioed CMOS SR latch. Cross-coupled inverter in the conventional circuit has been replaced by the 4T Schmitt trigger for improving robustness in the presence of PVT variations

have been shown in Fig. 4 itself. Since INV3 and INV4 in Fig. 4 are ratioed pseudo-NMOS logic-based inverters (INV3 and INV4), sizing for the MOSFETs are a critical design strategy. We have judiciously sized them for proper functioning. Moreover, sizing of all the devices has been done keeping design metrics such as propagation delay (t_{PD}), power dissipation, power-delay product (*PDP*), and energy-delay product (*EDP*) optimum. Figure 5 illustrates the simulation waveform of the proposed circuit shown in Fig. 4. As can be observed, the waveforms follow the characteristic table of the conventional latch given in Table 1, and the output swings fully from 0 to V_{DD}.

3 Explanation of Simulation Results

3.1 Simulation Setup

Our main aim in this section is to determine the improvement in the robustness of the design with incorporation of Schmitt trigger under PVT variations. Robustness of the conventional design and the proposed design is compared on the basis of variability of design metrics. A measure of dispersion is defined as the standard deviation(σ). Numerically, it can be stated as the extent of variation of the individual observations from the average [20]. The ratio of the standard deviation (σ) to the mean value

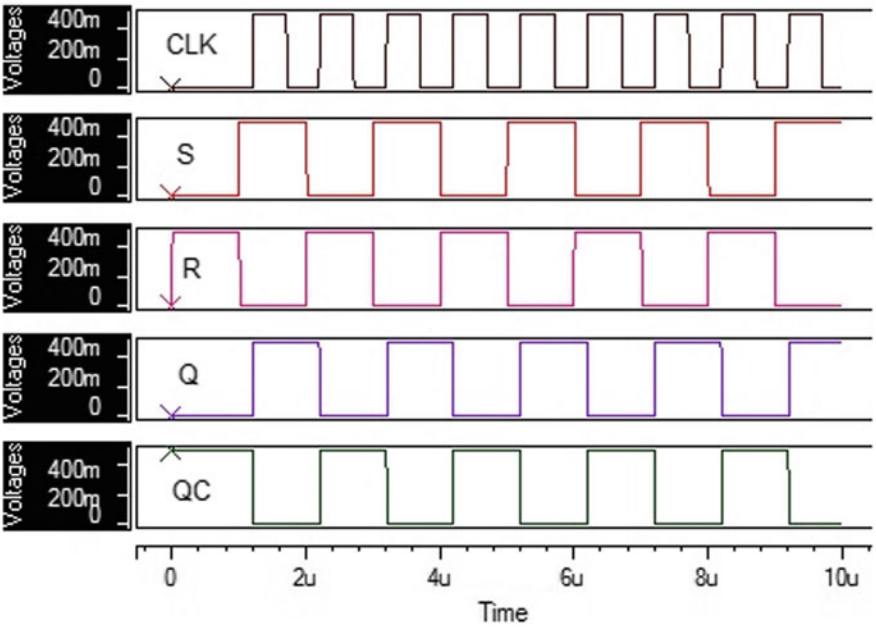

Fig. 5 Output waveforms of the proposed circuit. CLK, *S*, *R*, *Q*, *QC* in the respective order. The waveforms follow the characteristic table and the output swings fully from 0 to V_{DD}

(μ) of specified design metrics is known as variability. The design metrics may be power dissipation, delay time, energy-delay product (EDP), and product-delay product (PDP) in case of a digital circuit. Impact of variations in process parameters on variability of design metrics is captured by applying ~ 10% variation to threshold voltage about its nominal value. For 16-nm technology, threshold voltage for nMOS is 0.47965 V and that for pMOS is −0.43212 V. With a view to operate the design at NTR, nominal value of 0.45 V is chosen for V_{DD}. Supply voltage variations have been provided by scaling voltage from 0.5 V down to 0.4 V, giving a variation of $\pm$ 11.11%. Temperature is made to vary from −50 to 150°C. Variability in design metrics has been evaluated under each of the above-mentioned variations. In the estimation of standard deviation, lower than 4% inaccuracy is ensured for a sample space of 2000 [8]. For achieving even higher accuracy, in this work, design metrics are estimated with 5000 sample size. The other process parameters are assumed to have independent Gaussian distribution with a 3σ. In order to obtain realistic input and output waveforms, the input and output nodes have been loaded with minimum sized inverters. The observation made while performing the robustness analysis are reported in the following Sections.

Table 2 Variability in delay due to process variation-variability is captured by applying ± 10% variation to threshold voltage about its nominal value

Threshold voltage (V)	Variability of proposed SR latch for delay	Variability of conventional SR latch for delay	Ratio of variability
0.431685	0.000747	0.5802	776.7
0.47965	0.000712	0.284	399
0.527615	0.000507	0.5785	1141

Table 3 Variability in power due to process variation

Threshold voltage (V)	Variability of proposed ST-based SR latch	Variability of conventional SR latch	Ratio of variability
0.431685	0.84324	1.096	1.2997
0.47965	0.768	0.889	1.16
0.527615	0.813	1.096	1.348

Variability is captured by applying ± 10% variation to threshold voltage about its nominal value

3.2 Impact of Process Parameter Variation on Variability

Process variations affect the dimensions of device (channel width W, channel length L, oxide thickness t_{ox}), threshold voltage (V_t), substrate doping concentration. Second-order effects associated with short channel devices such as short channel effects, drain induced barrier lowering, random dopant fluctuation, line edge roughness have proved to be major causes of process variations. Variations in these parameters ultimately impact the threshold voltage.

Table 2 compares the variability of delay in Schmitt trigger-based circuit and the conventional circuit under applied threshold voltage variation. It is observed that the incorporation of ST has tremendously reduced spreads in delay. Table 3 presents the comparison between power variability of conventional and proposed design under applied threshold voltage variations. The proposed design has offered an average improvement of (1.269 ×) and the maximum improvement obtained is (1.348 ×).

3.3 Influence of Supply Voltage Fluctuations on Reliability

Supply voltage is subjected to variations due to tolerance of voltage regulator drop, line or IR drop, and di/dt noise. IR drop is caused due to voltage drop across parasitic resistance in the interconnect wires whereas di/dt is caused due to parasitic inductance in the interconnects. Saturation current is a function of supply voltage $V_{DD.}$ As explained earlier that propagation delay is dependent on the drain current I_{DS}. In this way, the propagation delay is influenced by supply voltage variations. The sensitivity

of t_{PD} to fluctuations in V_{DD} can be estimated as [8]

$$S_{V_{DD}}^{t_{PD}} = \frac{\Delta t_{PD}}{\Delta V_{DD}} \frac{V_{DD}}{t_{PD}} \tag{10}$$

Dynamic power dissipation accounts for the power dissipated during charging and discharging of load capacitor. It depends on the supply voltage as per the equation given below:

$$P_{dyn} = C_L V_{DD}^2 f_{\alpha_{0\to1}} \tag{11}$$

where f represents the maximum possible event rate of inputs (generally the clock rate) and $\alpha_{0\to1}$ is the probability that the event causes a transition $0 \to 1$ in the output [16]. Equation shows that dynamic power is a quadratic function of supply voltage. Hence variations in supply voltage directly affect power variability. Table 4 reports the delay variability due to variation in the supply voltage (V_{DD}) and the results have been observed by applying the variation of 11.11% to voltage about its nominal value. Table 5 shows the variability in power due to voltage variation about its nominal value and it is evident from the table that the proposed design has shown improvement in variability by an average factor of 1.162 when compared to the conventional one. The highest improvement of 1.34 × is achieved.

Table 4 Variability in delay due to voltage variation- variability is captured by applying ± 11.11% variation to voltage about its nominal value

Voltage (V)	Variability of proposed ST-based SR latch	Variability of conventional SR latch	Ratio of variability
0.5	0.000709	0.284	400
0.475	0.000742	0.339	457
0.45	0.000844	0.371	439
0.425	0.00105	0.393	373
0.4	0.00145	0.384	264

Table 5 Variability in power due to voltage variation

Voltage (V)	Variability of proposed ST-based SR latch	Variability of conventional SR latch	Ratio of variability
0.5	0.769	0.889	1.16
0.475	0.754	0.857	1.14
0.45	0.760	0.837	1.10
0.425	0.772	0.826	1.07
0.4	0.915	1.22	1.34

Variability is captured by applying ± 11.11% variation to voltage about its nominal value

Table 6 Variability in delay due to temperature variation

Temperature (°C)	Variability of SR latch using Schmitt trigger for Delay	Variability of SR latch using inverter for delay	Ratio of variability
−50	0.000656	0.220	335
0	0.000726	0.297	409
50	0.000718	0.265	369
100	0.000741	0.196	265
150	0.000560	0.291	519

Variability is captured by varying temperature from −50 to 150 °C

Table 7 Variability in power due to temperature variation

Temperature (°C)	Variability of SR latch using Schmitt trigger for power	Variability of SR latch using inverter for power	Ratio of variability
−50	0.377	0.420	1.11
0	0.696	0.773	1.11
50	0.582	0.946	1.63
100	0.127	0.938	7.40
150	0.158	0.911	5.77

Variability is captured by varying temperature from −50 to 150 °C

3.4 Influence of Temperature Fluctuations on Reliability

MOS parameters such as carrier mobility and threshold voltage are functions of temperature. As a result, temperature fluctuations impact the robustness of the circuit and causes thermal instability. Due to power dissipation in ICs, local and global temperature fluctuations occur. Table 6 shows delay variability for the applied temperature variation. We have observed huge reduction in spreads for delay of ST-based circuit as compared with that of conventional design. Table 7 draws the contrast between power variability of proposed circuit with the standard circuit under applied temperature variations. The proposed circuit offers an average improvement of (3.5756 ×) and the highest improvement of (9.18 ×).

4 Conclusion

In this paper, a new topology has been introduced where the cross-coupled inverters are replaced by Schmitt triggers, in ratioed CMOS SR latch. The results are indicative of improvements in variability of the investigated metrics, resulting in a more robust

circuit. It has also been verified that the proposed circuit works well under the applied variations in threshold voltage, temperature, and supply voltage. Although these improvements are at an expense of an increase in the mean values of design metrics, but such a cost is quite tolerable because of the improvements in variability, which is a critical design metrics in aggressively scaled technology nodes. Moreover, operation at NTR provides a balance between power dissipation and time delay. Such mitigation of variability makes way for technological progress as mentioned in Moore's law, in near future generation.

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Study of Solar Photovoltaic System with Utility Backup of an Educational Institute

Md Tabrez, Priyansu Raj, Rahul Raj, Anubhav Gupta, and Saket Kumar Singh

Abstract Various surveys tell us that due to excessive power consumption in the present time there is frequent power cuts in villages and cities of India. The use of solar photovoltaic system can reduce load on utility power and reduce pollution. Solar photovoltaic system may be stand-alone or grid-connected depending on capacity and load requirements. In this paper, a systematic study of the proposed rooftop stand-alone photovoltaic (PV) system on the top of the academic building of Motihari College of Engineering (Govt. of Bihar, India) is carried out. The study tells us the load requirements of the institute, amount of energy produced by using a solar photovoltaic system, and the payback period of the PV system.

Keywords Photovoltaic · Renewable · Solar

1 Introduction

There is a continuous increase in greenhouse gas levels, and so the fuel prices are increasing day by day. In India, due to an inadequate supply of electricity, a large section of the population is compelled to use LPG gas for the fulfillment of their daily needs. Low production of electricity has led to frequent power cuts as load demand is high. Although in metropolitan cities, load shedding is not high, in villages it has reached a very high level of up to 12 h per day and in some places about 18 h per day. Due to such frequent and longer duration load shedding, households in villages and cities have been forced to get himself provided an inverter with a battery backup system. Since a large section of the middle high-class society people have this system in their residences. This system fulfills the demand of electricity when there is a power cut from the state electricity supplies. The drawback of this system is that it uses energy coming indirectly from non-renewable resources. If we use solar panels for

Md Tabrez (✉) · P. Raj · R. Raj · S. K. Singh
Motihari College of Engineering, Motihari, Bihar, India
e-mail: mdtabrez2008@gmail.com

A. Gupta
National Institute of Technology Srinagar, Srinagar, Jammu and Kashmir, India

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providing power to inverter, the load on non-renewable resources can be reduced. The solar panels can easily be affixed either to rooftops or installed in backyards. Government of India many subsidized programs to promote the installation of solar PV systems for household applications, street lights, irrigation pumps, etc.

Solar energy presents an exciting opportunity for India as a renewable energy source. Though the current contribution of solar energy to the total India's energy needs is insignificant, by observing the current trend, it is expected that solar energy will contribute significant components to the energy mix of the country in the near future. The Electricity Act 2003 emphasizes the promotion of energy generation from renewable energy sources. The Government of India has taken several steps and enacted laws, policies, and regulations to promote renewable sources of energy. The government has created fiscal incentive instruments and also market-based instruments to promote energy generation from renewable sources. NAPCC (National Action Plan on Climate Change) program was announced in June 2008 emphasizing the seriousness of the Government of India to mitigate the impacts of climate change [1]. The key target of NAPCC is to have 15% of the total energy consumption in the country from renewable sources of energy by 2020 [2]. The present analyses is aimed to—(1) asses and define the solar resource potential at Motihari city of the state of Bihar, India, (2) predict the performance of 246.42 kWp stand-alone rooftop solar power plant, and (3) compare the annual energy yield, PR, and energy yield of the PV system from simulation results. A similar study is also reported in [3, 4].

In this study, it is proposed to install 246.42 kW PV system on the rooftop of the academic building of Motihari College of Engineering in order to evaluate the feasibility of such installations in every college of Bihar.

2 Materials and Methods

Mono-crystalline-based PV cell is selected in this study because its efficiency is at the higher side. The stand-alone PV system consists of solar arrays to absorb and convert sunlight into electricity, a solar inverter to convert the direct current output to alternating current, a mounting, cabling, and other electrical accessories. Solar PV modules are connected in series and parallel, depending on the solar PV array size and power. A schematic diagram of the proposed grid-connected PV system is shown in Fig. 1. The main component for grid-connected solar PV power systems comprises of—[5–7].

- Solar PV modules which are connected in series and parallel, depending on the solar PV array size, to generate DC power directly from the sun's intercepted solar power.
- MPPT to operate PV panel at peak power operating point.
- Battery bank to store surplus energy for use at night.

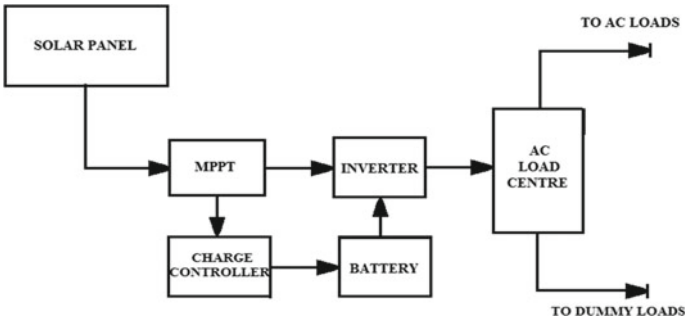

Fig. 1 Schematic diagram of rooftop PV system

- DC/AC inverter, that is a bidirectional power flow converter that converts generated DC power into AC power safely for utilization and feeding to grid and vice versa if demand in case of low or no solar power generation.
- Safety equipment like AC/DC circuit breakers, fuses, etc., that are required according to the local regulations. Grid-connected DC/AC inverter making sure the generated and converted AC power is safely fed into the utility grid whenever the grid is available. Grid connection safety equipment is like AC breakers, fuses, etc., according to the local utility's rules and regulations.

The load demand of Motihari College of Engineering is given in Table 1 as mentioned.

So, the total generated energy comes out to be = 3477.696 MJ.

It is assumed that the surface of the roof (as shown in Fig. 2) is completely flat and the rooftop is covered with the solar PV array. Below is the calculation of number of panels required.

Average length of panel for commercial use = 1.98 m.

Average width of panel for commercial use = 0.9906 m.

Average area of panel for commercial use = $1.98 \times 0.9906 = 1.9613\ m^2$.

Table 1 Load demand of Motihari college of engineering

Building	Equipment installed	Rated power (W)	Quantity	Total power (kW)	Operation hours	Power consumed (MJ)
	Tube light	40	207	8.28	8	238.46
Academic building	Fan	55	29	1.595	8	45.936
	Power socket	1000	100	100	8	2880
	Street light	200	10	2	8	57.6
		Total		120.755	Total = 966.04 units consumed daily	

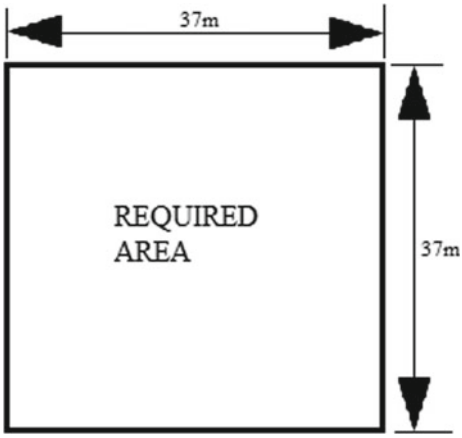

Fig. 2 Dimension of rooftop PV array to be installed

Hence, the total number of panels required = 1369 ÷ 1.9613 ≈ 698 .
Thus, number of solar panels required will be ≈698.

3 Results and Discussion

As per Bihar Renewable Energy Development Agency average solar insolation falling on 1 m^2 area is 1000 W [2]. Assume PV panel made of crystalline cells with an efficiency of 18%. Assuming an average sunlight of 8 hrs in a day. On the basis of these assumptions calculation of energy is tabulated in Table 2. Efficiency of solar PV array is assumed to be 18% [8]. Sample calculation of Energy (taking example of building ACADEMICS1) is shown.

Dimension of PV array at the rooftop of academic building = 37 m × 37 m = 1369 m^2.

Area of the roof = 1369 m^2.

Total power input Po = 1369 × 1000 = 1,369,000 W.

Thus, total power that we get as output for one hour will be = 1,369,000 × 0.18 = 246,420 W.

The area of the required rooftop of the college is calculated and mentioned in the Table 2.

Total power that we get in 8 h will be = 246.420 × 8 = 1971.36 kWh.

Table 2 Required area of rooftop of the college

Facility (solar PV system)	Dimension (L × B)	Area (m^2)	Input solar power (Pi) *n* KW	Output power of PV array (kW)
Required area	37 × 37	1369	1369	246.420
			Total=	246.420

Table 3 The installation cost of solar PV system for generating 1 kW

Item	Cost (₹)
Cost of a 1 kW rooftop solar plant	100,000.00
Subsidy @ 30%	30,000.00
Net cost after subsidy	*70,000.00*
Accelerated depreciation @ 80%	56,000.00
Tax rate	35%
Tax saved through depreciation	19,600.00
Net cost after both AD and subsidy	**50,400.00**

Thus, energy produced in 8 h = 246.42 × 3.6 × 1,000,000 × 8 = 7096.896 MJ.

3.1 Payback Period Calculation

The solar panel payback period is a calculation that estimates how long it will take for you to "break-even" on your solar energy investment and its calculation is as shown below [9, 10]. The installation cost of the solar PV system for generating 1 kW is mentioned in Table 3.

The average working year of a PV panel is 30 years. As our requirement of energy, we need a total of 120.755 kW but we are generating 246.42 kW.

Total cost of installation of solar PV panel for generating 246.42 kW = 246.42 × 50,400 = ₹ 1,24,19,568.

We need to store some energy (say 20 kW) for street lights and other works when sunlight is not present and the cost of the 5 kW battery = ₹72,8800.

For storing 20 kW we need 4 batteries of 5 kW.

So, for storing 20 kW power = 4 × 72,880 = 2,91,520.

Total installation cost with battery = Initial cost of PV panel + cost of battery.

Thus, total installation cost with battery = 1,24,19,568 + 2,91,520 = 1,27,11,088.

Total cost of consumption of electricity in the college for one month = ₹2,34,538/-.

The working period of the college in a year is about 10 months.

So total cost of consumption of electricity in the college for one year = ₹23,45,380.

Payback period = (total cost of installation)/(total cost of electricity in one year).

Thus,

Payback period = ₹ 1,27,11,088 ÷ ₹ 23,45,380 ≈ 5.41 years.

Thus, the total time in which we get back our investment = 5 years 6 months.

4 Conclusion

This proposal can be implemented to reduce the building's carbon footprint for environmental stewardship, the economic advantage of lowering a building's operational costs is reason enough for adoption to all educational institutions of the state of Bihar, India. Payback period comes out to be 5.41 years. And with 40 percent of global energy consumption going toward powering buildings, everyone from architects and designers to building owners and tenants are looking for ways to lower electricity expenses.

Luckily, new and innovative technologies are cropping up across the globe that can help alleviate both a building's operational costs and its environmental impact: solar-powered buildings. This study also supports the findings that a rooftop solar PV system can generate more energy than it consumes.

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Study and Analysis of AlInN/GaN Based High Electron Mobility Transistor

Shashank Kumar Dubey and Aminul Islam

Abstract In this paper, we propose a new HEMT structure with AlInN and GaN as a barrier and buffer layer, respectively, and AlN as a spacer between them. SiO_2 and Si_3N_4 multilayer dielectric films are used for gate isolation and passivation respectively. The structure is grown on SiC substrate which increased the breakdown voltage to 1500 V. A good ON/OFF current ratio of 10^{10} and an excellent subthreshold slope of 65 mV/decade is achieved due to the use of AlInN as the barrier layer. The gate leakage current was observed to be quite low of the order of 10^{-12} A as a result of the introduction of SiO_2. The small-signal model of the device is built including parasitic capacitance, inductors, and resistors. All the results were simulated using Silvaco Atlas.

Keywords AlInN/GaN · SiC · High electron mobility transistor (HEMT) · Breakdown voltage · Subthreshold slope · Spacer layer · Transconductance

1 Introduction

With the rise in demand for RF and microwave technology in the last couple of decades, the conventional semiconductors could not meet the demand due to various limitations in their high frequency and high-power applications. This has paved up the way for wide bandgap materials like GaN, SiC, etc. Among these, GaN-based heterostructure devices have shown great potential for the present and upcoming high power and microwave frequency application. This is because of its remarkable physical and electrical properties like high breakdown electric field, high saturation velocity, and electron mobility. The breakdown field of GaN devices is about ten times higher than that of Si devices, observed as high as 3.3 MV/cm. Further

S. K. Dubey (✉) · A. Islam
Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra, Ranchi, Jharkhand, India
e-mail: dubey.shashank1991@gmail.com

A. Islam
e-mail: aminulislam@bitmesra.ac.in

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improvement in the breakdown voltage and high-temperature operation capability is achieved with the introduction of wider bandgap semiconductor material SiC. High-electron-mobility transistor (HEMT) is a field-effect transistor where a channel is formed by a junction formed by two different wide bandgap materials. In case of GaN HEMTs, GaN is the thick epitaxial layer over which resides the thin barrier layer, and a highly mobile 2-Dimensional Electron Gas (2-DEG) is present at the heterointerface [1]. Due to their highly linear performance at high frequency, GaN-based HEMTs are widely utilized for high power applications, RF applications like cellular telecommunications, imaging, RADAR, and radio astronomy. Low noise amplifiers, oscillators, and mixers are designed using GaN HEMTs attributing to their low noise and better high-frequency performance [2].

In HEMTs, the two different bandgap materials are chosen such that they should be perfectly lattice-matched so that strain can be minimized at the junction of the material. Over the last two decades, a lot of research work has been conducted to upgrade the performance of HEMTs by using AlGaN as the barrier layer. By increasing the Al content in AlGaN, the sheet resistance is reduced resulting in an increase in the surface donor states density. But this is possible only up to a certain limit set by the start of degradation caused by strain relaxation in the barrier [3, 4]. To avoid the problem of strain and to provide a better lattice-matched structure AlInN is used in this literature instead of AlGaN. As shown in previous studies, $Al_{1-x}In_xN$/GaN heterostructures with 17% Indium-content shows strong spontaneous polarization and better lattice-matched AlInN barrier [4, 5]. The 2-dimensional electron gas (2-DEG) density observed in AlInN/GaN is higher than that in AlGaN/GaN structures reflecting a corresponding increase in surface donor states density. Often, to reduce alloy scattering in 2-DEG, AlN spacer layer is used in between AlInN and GaN. This results in enhanced 2-DEG density and high electron mobility values [6, 7]. Devices passivated with Si_3N_4 exhibits higher breakdown voltage [3]. Hence, we used Si_3N_4 to passivate our device in this work. The materials for modeling the device are selected by observing their lattice constants as shown in Table 1.

GaN-based devices have relatively high sub-threshold slope as compared to that of silicon-based devices which have an ideal sub-threshold slope value of 60 mV/decade [8, 9]. Sub-threshold slope is a very crucial factor in digital applications; lower value of sub-threshold slope corresponds to a faster transition from low state to high state. To achieve lower sub-threshold slope different structures were proposed by authors in [6, 10–13]. H. W. Then, et al. got an ideal sub-threshold slope of less than 60 mV/decade but the drain current examined was in the orders of nA/mm, which

Table 1 Lattice constants

Material	Lattice constants
GaN	3.19
AlN	3.11
SiC	3.08
AlGaN	3.17
AlInN	3.15

is not at all enough for its thought-out operation [13]. It is well-known fact that sub-threshold slope and maximum ON/OFF current ratio is strongly related to sub-threshold leakage current, lower the sub-threshold slope higher is the ON/OFF current ratio and lower is the sub-threshold leakage current [8]. Since GaN-based HEMTs are utilized for high power, it is desirable for them to have a high breakdown voltage. Breakdown voltage can be increased by reducing the electric field at the drain edge of the gate. This can be done by introducing a field plate, but they increase parasitic capacitances and can deteriorate the performance of the device. A more preferred way of increasing the breakdown voltage is the introduction of a passivation layer with high dielectric constant. With the increase in dielectric constant of the passivation layer, a commendable raise in off-state breakdown voltage is observed due to the reduction in the field at the drain edge of the structure [6, 14, 15]. Digital applications require high-frequency switching devices. These characteristics are obtained by using SiC, as the R_{ON} of SiC is very small compared to Si, which also results in the reduction of parasitic capacitance, thereby reducing the switching time.

This paper deals with the following:

- Introduction of an AlN spacer layer at the junction of AlInN and GaN layers, which reduces the problem caused by the excessive hot electrons.
- The presence of AlN spacer aids to get rid of strain at the heterointerface as well as to enhance the AlInN film quality.
- Reduction in gate leakage current is done by introducing thinner oxide layer of 1 nm in between gate and AlInN which also resulted in lower value of sub-threshold slope and higher value of ON/OFF current ratio.
- The Si_3N_4 passivated HEMT grown on SiC substrate exhibited an excellent breakdown voltage (BV) of 1500 V.
- Breakdown voltage variation with gate length variation is also presented in the paper. Moreover, the proposed device showed a high ON/OFF current ratio of 10^{10}.

The rest of the paper is arranged in the following manner. Section 2 illustrates the device structure. Device model and the device parameters are described in Sect. 3. Section 4 shows the results after simulating the proposed device model. Section 5 finally concludes the paper.

2 Device Structure

The cross-sectional view with the dimensions and materials used for the proposed AlInN/AlN/GaN/SiC HEMT device is illustrated in Fig. 1. The layer structure of this HEMT has 72 nm thick GaN buffer layer and a 20 nm thick AlInN barrier layer with 17% mole fraction of Indium with an 8 nm thick AlN spacer layer in between them.

A 1 nm thin oxide layer is introduced between the gate and the barrier layer to reduce gate leakage current. To minimize the source access resistance, we used the

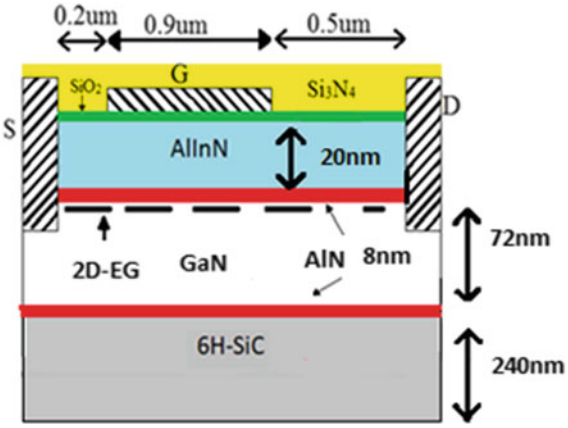

Fig. 1 Cross-sectional view of the proposed AlInN/AlN/GaN/SiC HEMT structure

source-gate length small in this design. Quasi-saturation of electron velocity at high electric fields can cause an increase in the source access resistance with the increase in drain current, leading to nonlinearity in transconductance [16]. AlInN has a wide bandgap with energy ranging from 0.69 to 6.25 eV. The GaN and AlN have bandgap energy of 3.4 eV and 6.2 eV, respectively. 2-DEG is formed at the heterointerface of two materials one with a wideband gap (AlInN in this case) and other with narrow bandgap (GaN in this case). The device is passivated by depositing Si_3N_4 passivation layer.

3 Device Model

GaN HEMTs with a thin barrier of AlInN experience weaker surface depletion effects than with AlGaN barrier and hence possess high 2-D electron gas channel densities [17]. In the proposed model, AlInN is used instead of AlGaN because of certain advantages. AlInN/AlN/GaN/SiC HEMTs have two main advantages over AlGaN/AlN/GaN HEMTs

- Spontaneous polarization induces almost three times higher charge which allows larger current densities.
- No mechanical constraints are observed in the epitaxial structures since $Al_{0.83}In_{0.17}N$ and GaN are lattice-matched.

Reliability of the devices is degraded due to these mechanical constraints present at the origin of trapping centers in transistors [18]. The increase in sheet carrier concentration (i.e., of 2-D electron gas) with the increase in AlN spacer thickness is the result of enhancement of polarization-induced sheet charge at the AlN/GaN interface. This effect gives the same result as increasing of Al mole fraction in AlInN barrier. Strong polarization effect is observed after exceeding the AlN spacer

thickness beyond a critical thickness causing an increase in dipole scattering which further results in deteriorating the 2-DEG's mobility. Below the critical thickness, the AlN spacer enhances the conduction band offset what effectively reduces the penetration of the wave-function into AlInN barrier and thus reduces the effect of alloy disorder scattering. This is consistent with theoretical calculations. The sub-threshold attribute of the AlInN/GaN HEMT structure is given by

$$S = \frac{kT}{q}(1+\eta)\ln 10 \tag{3}$$

where η is a non-ideality factor related to trap density. The proposed structure shows the sub-threshold characteristics as shown by authors in [8]. The value of η is calculated for the observed value of sub-threshold slope (S) and is found to be 0.1158 for the proposed AlInN/AlN/GaN/SiC structure.

There is strong correlation between the transistor sub-threshold characteristics and the sub-threshold leakage current: higher value of ON/OFF current ratio and steeper sub-threshold slope are seen for lower sub-threshold leakage. To reduce the gate leakage current we used SiO_2 between AlInN and gate. The gate leakage of the proposed structure comes out to be of the order of 10^{-12} A and the ON/OFF ratio is about 10^{10}.

In this model, at the junction of AlInN and GaN layers, we included a spacer layer to overcome the problem due to excessive hot electrons. This also raised the current confinement in the channel and hence the model was improved remarkably. Breakdown voltage for the proposed device is found to be 1500 V, which is more than twice when compared to the previous literature. In power electronics applications, it is a very important requirement to achieve a very low on-resistance just after switching from high-voltage OFF state to low-voltage ON state [19]. A low value of on-resistance is obtained due to the high mobility of charged carriers in the 2-D electron gas, which results in increase of the RF power added efficiency [20]. RF power performance is degraded due to dynamic switching caused by drain lag effects, gate lag, and current collapse. R_{on} (on resistance) is also dependent on temperature, as mobility of 2-D electron gas decreases with an increase in temperature, thereby increasing R_{on} significantly [21]. Assume a HEMT with gate width of W_g, source to drain distance of L_{ds} and 2-D electron gas density of n_s. For a vertical device structure with a uniform doping profile, the on-resistance of a FET may be expressed by [22]

$$R_{on} = \frac{4V_{BR}^2}{\varepsilon_r \mu_n E_c^3} \tag{4}$$

where V_{BR} is the break down voltage, E_C is the critical electric field, ε_r is the relative permittivity of GaN and μ_n is the mobility of electron. Channel resistance can be formulated as

$$R = \frac{L_{ds}}{q\mu_n W_g n_s}\ [\Omega] \tag{5}$$

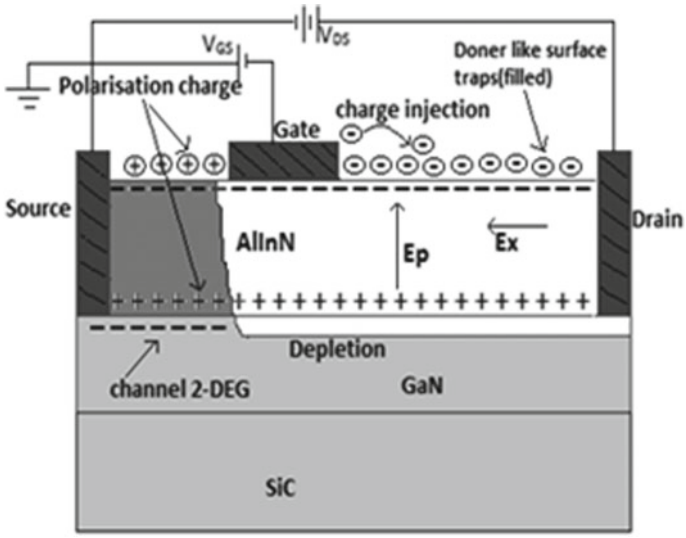

Fig. 2 OFF-STATE AlInN/GaN/SiC HEMT (under positive drain bias and pinched off)

In order to achieve high breakdown voltages, doping level should be reduced so that the depletion length is extended. There is a trade-off between breakdown voltage and on-resistance. Reduction in doping level to increase the breakdown voltage increases the on-resistance subsequently leading to switching loss. The electrons move as a 2-dimensional gas in the AlInN/GaN heterojunction channel. In an undoped GaN HEMT, usually it is observed that strong polarization field in the AlInN layer induces the electrons in the channel from the donor-like surface traps by the, and hence the empty traps leave the surface as positively charged as shown in Fig. 2. The 2-D electron gas density depends solely on Aluminum composition in AlInN layer.

The polarization field E_p is very strong in AlInN. Though only the net polarization is considered (the polarization difference between AlInN and GaN is deducted), E_p is as high as several MV/cm and cannot be ignored in the analysis. Therefore, the total field (E_{total}) in the depletion region is a combination of E_x (lateral field due to the applied voltage across the drain-source terminal) and E_p (vertical field due to the polarization effect), hence E_{total} is formulated as

$$E_{tot}^2 = E_x^2 + E_p^2 \tag{6}$$

If one assumes the gate-drain region is fully depleted when the device is biased to breakdown, then $E_x = V_{BR}/L_{gd}$, and E_{total} equal to E_c, the critical electric field of AlInN. Together with (5) and $L_{gd} \approx L_{ds}$, the on-resistance can be expressed as

$$R_{on} = \frac{V_{BR}^2}{q\mu_n n_s\left(E_c^2 - E_p^2\right)} \tag{7}$$

Equation 5 reveals that, for GaN HEMTs, the on-resistance still follows a square rate with the breakdown voltage. Since the critical field of AlInN is also a linear extrapolation of that of GaN and AlN, n_s can be related to E_c directly as $qn_s = \varepsilon E_c$, where ε is a constant with a unit of [F/cm]. Equation 5 is re-formatted as

$$\frac{V_{BR}^2}{R_{on}} = \varepsilon R_c \mu_n \left(E_c^2 - E_p\right)^2 \tag{8}$$

Keeping the short channel effects in consideration, model equations for current can be written as

$$I_{DS} = k(V_{DS})k_n \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{9}$$

For $V_{DS} \leq (V_{GS}–V_T)$ and

$$I_{DS} = k(V_{DS})k_n \frac{W}{L}(V_{GS} - V_T)^2 \tag{10}$$

where k_n is a proportionality constant. The k_n gives the measure of mobility degradation. The degree of velocity saturation, $k(V)$ is expressed as

$$k(V) = \left(1 + \frac{V}{E_c L}\right)^{-1} \tag{11}$$

where E_c represents the critical electrical field at which drift velocity of the carrier saturates.

4 Simulation Results and Discussion

Extensive simulations were carried out to verify our results using Silvaco Atlas [23]. Improved results were obtained by adjusting the value of saturation velocity and the parameters for transverse and lateral fields given in the Yamaguchi model. HEMT with AlInN instead of AlGaN gives better performance. The breakdown voltage of the AlGaN/AlN/GaN HEMT proposed by authors in [6] was reported to be 780 V. Another author in [11] proposed AlInN/AlN/GaN MOSHEMT which exhibited a breakdown voltage of 1162 V. Figure 3 shows that the breakdown voltage of the device proposed in this work is 1500 V. Breakdown voltage as a function of gate length is shown in Fig. 4. It can be observed that with an increase in gate length breakdown voltage also increases and this increase is linear with the gate length.

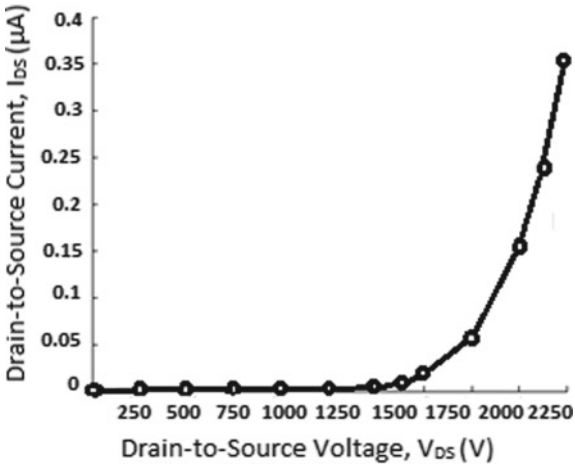

Fig. 3 Breakdown voltage characteristics

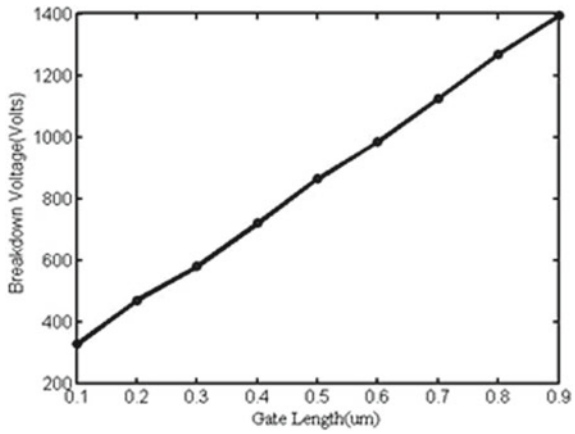

Fig. 4 Dependence of breakdown voltage on gate length

Figure 5 shows an exponential dependence of I_{DS} on V_{GS} for the proposed device. Figure 6 shows I_{DS}-V_{DS} (output) characteristics of the presented device structure. Strain due the lattice mismatch at the AlInN-GaN layer interface is reduced due to the introduction of AlN spacer layer. Thus, inclusion of AlN results in enhancement of the carrier mobility in the device, which in turn increases the drain to source current (I_{DS}). For the different thickness of spacer layer, simulations results were obtained. The I_{DS}-V_{GS} curve of the given structure is shown in Fig. 6. Current in the device depends mainly on two factors, mobility and carrier concentration. With the decrease in scattering the depth of the quantum well increases resulting in increase of mobility of the charge carriers. Enhancement in mobility is achieved with the presence of AlN spacer layer. AlInN and AlN are ternary and binary compounds, respectively, former having the greater alloy scattering. A much better subthreshold slope is seen

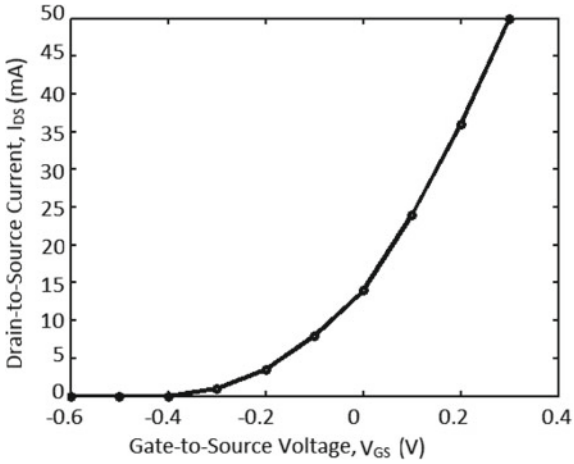

Fig. 5 I_{DS}-V_{GS} characteristics

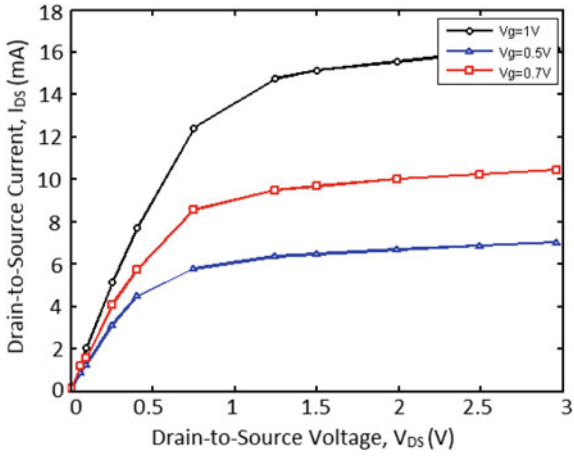

Fig. 6 I_{DS}-V_{DS} characteristics

in AlInN/GaN devices grown on SiC substrate as compared to that of the conventional AlGaN/GaN devices. Low power dissipation in digital circuits and systems corresponds to lower value of the subthreshold slope. Hence, a lower subthreshold slope is required for a commendable upgrade in the device performance. An average subthreshold slope of 65 mV/decade is achieved for the proposed structure, as shown in Fig. 7.

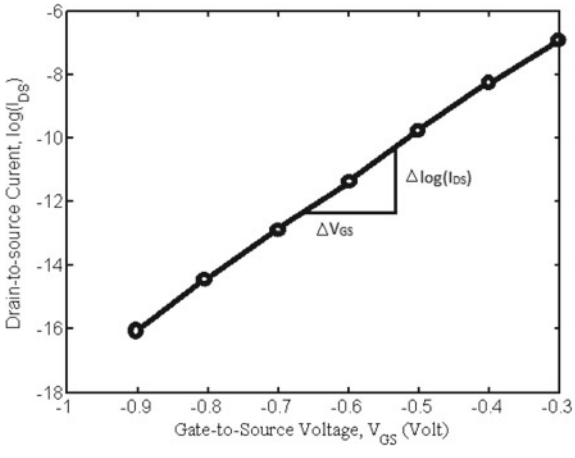

Fig. 7 Subthreshold characteristics

5 Conclusion

This paper successfully examines AlInN/GaN/SiC-based HEMT structure, which offers improved performance compared to AlGaN/GaN-based HEMT. The subthreshold slope is found to be closer to the ideal value and ON/OFF current ratio is found to be quite high. The observed breakdown voltage is high due to the device modeled on a high thermal conductivity substrate SiC and due t the use of Si_3N_4 passivation. The use of AlN spacer layer increased the mobility of charge carriers. Our findings prove it to be a very promising device to operate even at very high temperatures.

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Optical and Electrical Simulation of Single GaAs Nanowire/Ge Solar Cells

Akshaya Kumar, Dip Prakash Samajdar, and V Sachchidanand

Abstract In this chapter, we perform a detailed analysis of the optical and electrical properties of GaAs nanowire (NW) over Ge bottom cell, which is significantly influenced by the structural morphology of the NWs. This necessitates the need for geometric optimization of the NWs to enhance the performance metrics of the solar cells. The absorption efficiency per unit volume over traditional bulk and thin-film counterpart are much improved due to the intrinsic antireflection, strong excitation of resonance modes, and optical antenna effects. We show that the diameter optimization of GaAs NW for a fixed D to P ratio of 0.5 resulted in an ideal short circuit current density of 42.32 mA/cm^2 with the help of 3D Finite Difference Time Domain method under standard AM 1.5G illumination. The optimized photogeneration profile is then imported to the DEVICE Module for electrical simulation resulting in a PCE of 18.61%, which is significantly higher than its planar counterpart.

Keywords GaAs NW · III-V nanowires · Power conversion efficiency · Short circuit current density · Open-circuit voltage · Optical antenna effect · Resonance modes

1 Introduction

In order to harness the available solar irradiance, Photovoltaic (PV) modules with superior power conversion efficiency (PCE) and lower fabrication cost are required. Thin film solar cells with lesser material consumption are the intense topic of research recently attracting the researchers worldwide though it needs convincing improvement in absorption efficiency. Meanwhile, nanostructure-based solar cells paved the way towards material consumption less than half of the bulk and best absorption

A. Kumar · D. P. Samajdar (✉) · V. Sachchidanand
Deparment of Electronics and Communication Engineering, Indian Institute of Information Technology, Design and Manufacturing, Jabalpur, Madhya Pradesh 482005, India
e-mail: dipprakash010@gmail.com

A. Kumar
e-mail: 1712302@iiitdmj.ac.in

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efficiency per unit volume. Out of the different nanostructured solar cells available in the literature, semiconductor NW based solar cells act as potential candidates for new-generation high-efficiency PV modules because of their ability to extract the maximum energy from the available solar spectrum through minimization of reflection losses, maximization of light trapping, and enhancement in bandgap tuning [1–3]. In addition to these advantages, combined effect of intrinsic antireflection and efficient excitation of resonance modes helps semiconductor NWs to predominate over its thin-film counterpart [4]. The presence of coupled optical antenna effect (Absorption of photons beyond cross-section of NW for a specific wavelength region) and other resonant modes in NW cavity makes the absorption characteristics of NWs distinct than traditional bulk and thin-film solar cells [5]. Si is considered to be the most dominant material for realizing solar cells with various topologies, as it is highly abundant. The suitable geometrical morphology of III-V semiconductors NWs helps to enhance the absorption efficiency by broadening the absorption spectra with the optimized set of optical and electrical parameters [6]. GaAs and Ge have nearly the same lattice constant which is one of the prime factors for achieving the high absorption efficiency and perfect absorption band with combination of GaAs NW over Ge bottom cell [7–10].

In this paper, we perform the coupled optoelectronic simulations to find out the optimized optical and electrical performance parameters for GaAs single NW over Ge bottom cell (Vertical Junction GaAs NW Solar Cell) for the first time to the best of our knowledge. We have also computed the maximum photogeneration rate (G), ideal short circuit current density (J_{sc}), open-circuit voltage (V_{oc}), Fill Factor (FF), and PCE. We have optimized the length (L) and diameter (D) of NW for fixed D to P ratio of 0.5 (P = Pitch) to get the best results in terms of J_{sc} and absorption efficiency per unit volume using 3D Finite Difference Time Domain (FDTD) simulation method [11]. Next, we have obtained the optimized photogeneration profile for vertical junction GaAs NW Solar Cell. Finally, the optimized photogeneration profiles are imported to the vertical junction GaAs NW Solar Cell for electrical simulation by taking into consideration the surface recombination velocity (SRV) losses between the interfaces, thereby resulting in $J_{sc} = 28.16$ mA/cm^2, $V_{oc} = 0.7917$ V, FF = 83.5%, and PCE = 18.61%.

2 Simulation Methodology

We have used 3D Finite Difference Time Domain (FDTD) commercial software package of Lumerical, Inc. for optical simulation [12]. The length (L) of GaAs NW and Ge bottom cell are fixed to 1200 nm and 200 nm, respectively, along with fixed D to P ratio of 0.5, whereas, diameter (D) of GaAs NWs is varied from 50 nm to 200 nm to find the optimized one. The system under investigation is illuminated with AM 1.5G (Plane Wave with wavelength ranging from 300 nm to 2000 nm) with the periodic boundary condition for the x and y directions PML (Perfectly Matched Layer) along z-direction. Frequency domain power monitors are used to calculate

the reflectance ($R(\lambda)$) and transmittance ($T(\lambda)$) from which the absorptance ($A(\lambda)$) can be computed from the following relation:

$$A(\lambda) = 1 - R(\lambda) - T(\lambda) \tag{1}$$

The parameters that we have obtained from the optical simulations are ideal short circuit current density, maximum photogeneration rate, and maximum electric field distribution. Further, the photogeneration profile is incorporated into the Lumerical Device Module, which utilizes the charge transport solver (Physics-based Electrical simulation tool for semiconductor Devices) to solve the system of equations expressing the Poisson's equation (Electrostatic Potential) and Drift–Diffusion equation (Density of free carriers). This DEVICE tool employs boundary conditions in the form of Poisson's equation and Drift–Diffusion equation.

3 Results and Discussions

Figure 1 shows the schematic of vertical junction GaAs NW solar cell in which the system of GaAs single NW over Ge bottom cell is subjeted to perpendicularly incident solar spectrum for the optical simulation. The axial p and n type GaAs NW is grown over 200 nm Ge substrate and the length of NW is fixed to 1200 nm. The ideal short circuit current density J_{sc} as a function of the diameter of NWs and fixed D/P ratio is shown in Fig. 2. J_{sc} first starts increasing up to 170 nm as larger diameter supports more guided resonance modes for light decoupling. However, further increment in diameter leads to a reduction of J_{sc} due to inefficient light absorption and enhanced reflection at the top facet of NW [4, 13]. A maximum J_{sc} of 42.32 mA/cm^2 is achieved for the diameter of 170 nm and fixed D/P ratio of 0.5.

For the optical analysis of vertical junction GaAs NW solar cell, we have assumed PML boundary condition [14] which considers additional lossy media around the simulation region. This results in the matching of intrinsic impedance, thereby producing zero reflection from the interfaces. The electromagnetic field is attenuated during propagation interior to the media at the top and bottom of the GaAs NW and Ge subcell, respectively. The absorptance, reflectance, and transmittance analysis are performed after the optimization of diameter of the NWs to obtain the best performance.

Figure 3a-c shows the absorption, reflectance and transmittance spectra for a fixed diameter of 170 nm of the axial GaAs NW. The peak of absorptance near to unity starts to decrease in the long-wavelength region ($\lambda > 800$ nm) because of the high extinction coefficient of GaAs and the large bandgap difference between GaAs NW and Ge bottom cell. The dip in the absorptance spectra for the wavelength region 900–1500 nm is due to the enhancement in the reflection losses in this regime. To minimize this loss, a material having bandgap between GaAs and Ge can be used. Reflectance starts to predominate after $\lambda > 1800$ nm as the system of NW and bottom cell becomes transparent after that range.

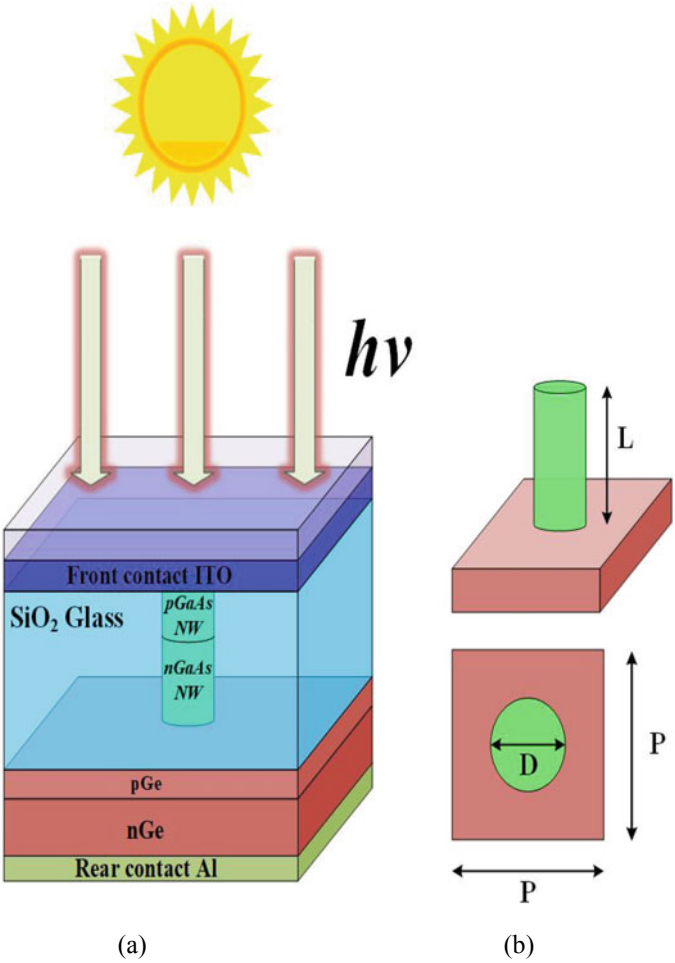

Fig. 1 Schematic of vertical junction GaAs NW solar cell, with its different geometrical parameters

Figure 4b shows the maximum generation rate along the length of the NW. The formation of lobes along the axis of the NW, and maximum photogeneration at the upper surface of the NW indicates that the distinct guided modes are efficiently confined inside the GaAs NW for specific wavelengths. However, towards the base of the NW, the generation rate starts decreasing due to the short absorption length of GaAs [4].

Figure 4b shows the average electric field distribution in the wavelength range of 1500 nm < λ < 1800 nm indicating the presence of strong coupled optical resonance mode inside the GaAs NW. The variation of electric field with the wavelengths induces distinct guided resonance modes [15] that are dependent on the structural morphology of NW. Additionally, the subwavelength size of NW converts

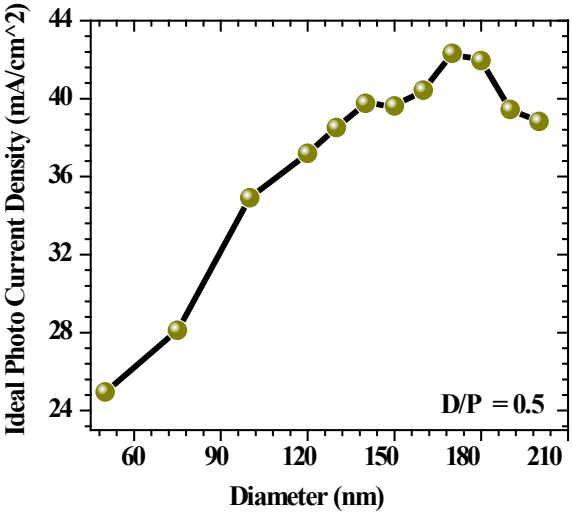

Fig. 2 Ideal short circuit current density versus the diameter (D) of the NWs for vertical junction GaAs NW solar cell with *D* to *P* ratio of 0.5

the incoming optical field into intense localization of the field distribution around the NWs in the deep wavelength region [16] and due to the optical antenna effect [5, 17] the absorption in the NW solar cell is more than the conventional solar cell.

The investigation of vertical junction GaAs NW solar cell after the 3D FDTD simulation is to incorporate the optimized 3D photogeneration profile obtained for 170 nm diameter to the device tool of Lumerical software package to calculate the J_{sc}, V_{oc}, PCE of the simulated device under AM 1.5G illumination. The system consists of single GaAs NW of length 1200 nm, Ge substrate of 200 nm, SiO_2 glass as insulator around the NW, and Al and ITO as the back and front electrodes, respectively. Electrical simulation takes into account the assumption of the Slootboom convergence model, Caughey Thomas mobility model Auger, Radiative, and Shockley–Reed–Hall (SRH) recombination, and surface recombination velocity (SRV) at the interfaces. Ge bottom cell comprises of a pn junction similar to that of the axial pn junction formed in case of vertical GaAs NWs.

The current-voltage (I-V) and power-voltage (P-V) characteristics of simulated vertical junction GaAs NW solar cell are shown in Fig. 5. The solar cell exhibits J_{sc} of 28.16 mA/cm^2, V_{oc} of 0.79 *V*, FF = 83.5%, and PCE of 18.61% as can be extracted from the I-V and P-V curves. The electrical J_{sc} of 28.16 mA/cm^2 is much smaller in comparison to the optical J_{sc} of 42.32 mA/cm^2 due to the assumption of 100% Internal Quantum Efficiency for the calculation of optical J_{sc} in FDTD calculations [18, 19].

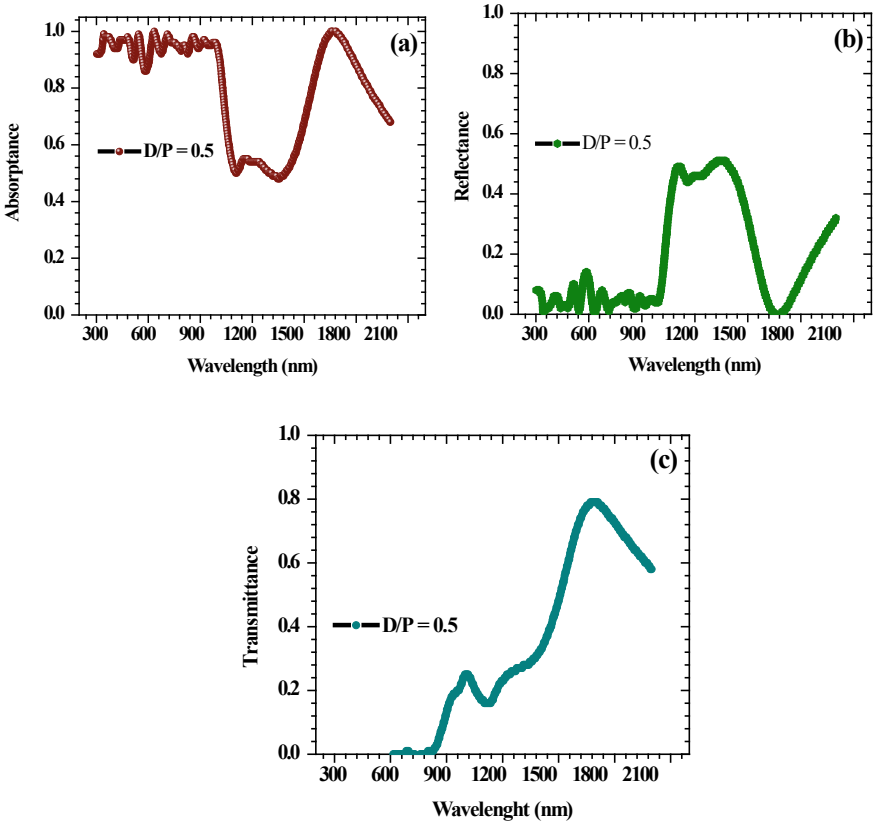

Fig. 3 **a** Absorptance. **b** Reflectance. and **c** Transmittance of vertical junction GaAs NW solar cell

4 Conclusions

To summarize, we performed the detailed analysis of GaAs NW/Ge solar cells through perfect optimization of geometrical parameters of NWs to obtain absorption efficiency per unit volume and J_{sc}. We achieved the values of the photovoltaic parameters such as $J_{sc} = 28.16$ mA/cm^2, $V_{oc} = 0.79$ V, FF = 83.5%, and PCE = 18.61% for GaAs NW/Ge solar cells by means of the geometric optimization of GaAs NWs using 3D FDTD method and DEVICE Module of Lumerical software package.

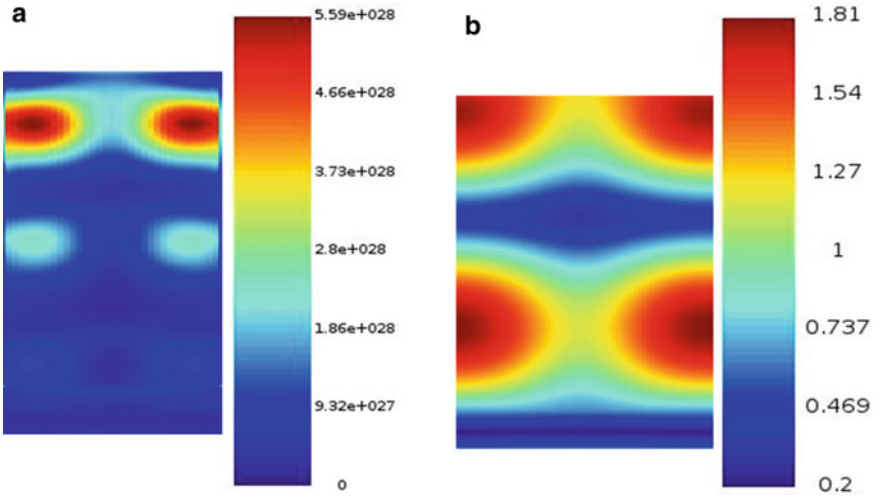

Fig. 4 **a** Maximum photogeneration rate. **b** Maximum electric field distribution of vertical junction GaAs NW solar cell

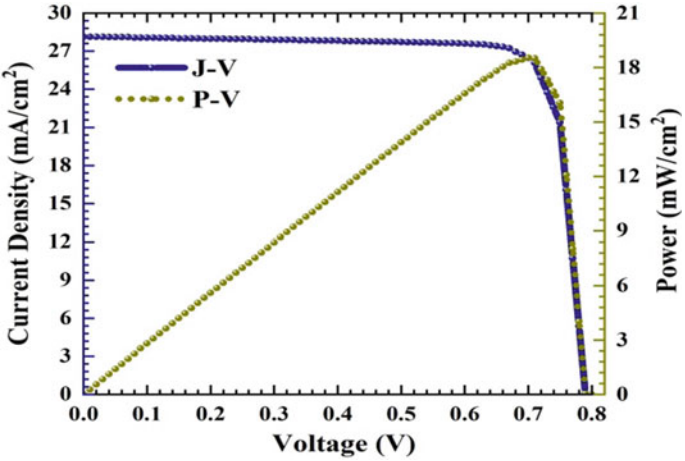

Fig. 5 Current-voltage and power-voltage characteristics for vertical junction solar cell

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A Technique to Design Robust Single-Stage Operational Amplifier

Abhinit Saurabh, Amresh Kumar, Shashank Kumar Dubey, and Aminul Islam

Abstract This paper proposes an appropriate biasing technique for a differential amplifier with active load to make the amplifier circuit immune to process, voltage and temperature (PVT) variations. The impact of the PVT variations on differential gain was investigated and the sensitivity analysis on process variations was also performed. The results of the investigation were compared with the results of differential amplifier, which was biased with two other different biasing techniques. The findings of the investigation and comparison reveal that the proposed biasing technique makes the differential amplifier robust to endure the PVT variations.

Keywords Differential amplifier · Monte Carlo simulation · Variability · Biasing topology · Transconductance (g_m)

1 Introduction

A differential amplifier is a two-input circuit that amplifies the difference of the signals applied to its two inputs and suppresses any signal common to the two inputs. It is widely used in situations where a signal relative to another signal is to be amplified or in circuits that require negative feedback or in general in any application that requires an amplifier with two inputs. Due to aggressive technology scaling, process, voltage and temperature (PVT) variations are large and have made it difficult to achieve the specification targets such as gain and linearity. Thus, PVT variations have

A. Saurabh · A. Kumar · S. K. Dubey · A. Islam (✉)
Department of Electronics and Communication Engineering, Birla Institute of Technology Mesra, Ranchi, Jharkhand, India
e-mail: aminulislam@bitmesra.ac.in

A. Saurabh
e-mail: abhinit.saurabh@gmail.com

A. Kumar
e-mail: amreshkumar@bitmesra.ac.in

S. K. Dubey
e-mail: dubey.shashank1991@gmail.com

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posed major challenges for an analog circuit designer to design a reliable and robust analog circuit [1, 2]. Process variations can be of two types: (a) global variations (inter die); (b) local variations (intra die). Global variations include wafer to wafer, die to die and lot to lot variations whereas the local variation occurs within a die. Local variations are classified as systematic variation and random variation [3–5].

Many strategies have been suggested in the literature to overcome the mentioned problem of PVT variation. A biasing technique was proposed for CMOS radio frequency amplifiers by the authors in [3]. Authors in [4] suggested that variation in threshold voltage was the main contributor to gain variation and a compensation scheme was proposed that processed changes in threshold voltage and generated bias signal to reduce voltage gain variation. A post-fabrication method to reduce PVT variations was proposed in [6]. Since the differential amplifier is one of the most useful amplifier circuits, it needs to be made robust so that it can tolerate PVT variations [7]. In view of the above, this paper proposes a biasing topology, which decreases the impact of PVT variations on the design metrics of the differential amplifier. Intensive simulations on Cadence Virtuoso Analog Design Environment have been performed to carry out robustness study using 45 nm technology model parameters. The rest of the paper is sequenced as follows. Section 2 describes differential amplifiers and three different biasing techniques. Impacts of temperature, process and supply variations on differential gain are studied in Sect. 3. Finally, conclusion is drawn in Sect. 4.

2 Differential Amplifier and Various Biasing Techniques

A differential amplifier is a circuit that amplifies the difference between its two inputs. In this paper, a single-ended output differential amplifier is used as shown in Fig. 1. All the transistors are biased into the saturation region and the output DC voltage is kept at $V_{DD}/2$ so that the maximum room is available for the output to swing about the output DC value.

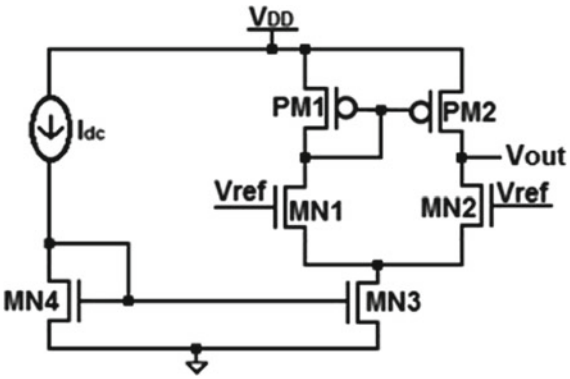

Fig. 1 Single-ended output differential amplifier

In this differential amplifier circuit, by equating the currents in the NMOS and PMOS transistors we can easily determine the bias voltage. Since, the diode-connected MOSFET always operates in the saturation region for the gate biased above the threshold voltage, hence, using the current equation for the saturation region

$$\frac{\beta_N}{2}(V_{\text{ref}} - V_{tn})^2 = \frac{\beta_P}{2}\left(V_{\text{DD}} - V_{\text{ref}} - |V_{tp}|\right)^2 \tag{1}$$

where β_N and β_P are the β ($=\mu C_{ox} W/L$), called gain factor) of the NMOS and PMOS transistors, respectively, V_{ref} is the DC bias voltage and V_{tn} and V_{tp} are the threshold voltages for the NMOS and PMOS transistors, respectively. Solving for V_{ref} from the above equation, we get

$$V_{\text{ref}} = \frac{V_{\text{DD}} - |V_{tp}| + \sqrt{\frac{\beta_N}{\beta_P}}(V_{tn})}{\sqrt{\frac{\beta_N}{\beta_P}} + 1}. \tag{2}$$

Since the differential pair MN1 and MN2 have active loads MP1 and MP2, respectively, this circuit is also known as an active-loaded MOS differential amplifier, which is also known as single-stage operational amplifier or transconductance amplifier.

A total of three different biasing topologies are considered to identify the one that is the most suitable for biasing the differential amplifier to make it immune to PVT variations. The first two biasing topologies (see Fig. 2a, b) were used to bias the single-stage operational amplifier, which was analysed by varying supply voltage and the results were compared with that of the proposed biasing topology.

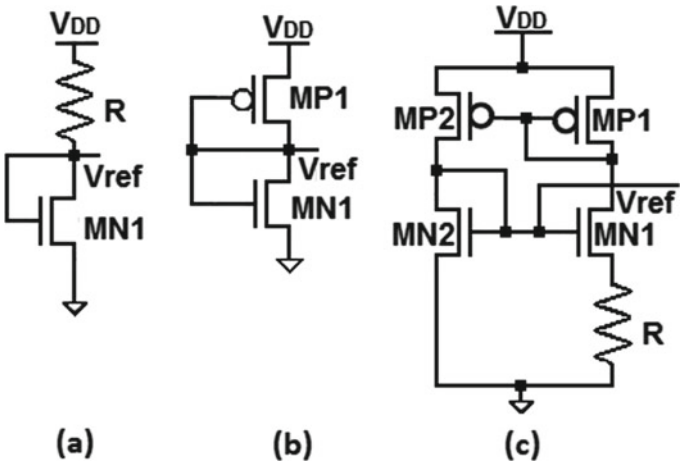

Fig. 2 **a** First bias MOSFET-resistor bias. **b** Second bias comprises of only MOSFETs and **c** constant transconductance (g_m) biasing circuit

The proposed biasing topology (see Fig. 2c), the constant transconductance (g_m) biasing circuit, was found to be the most suitable when it was subjected to voltage variation and design metrics of single-stage operational amplifier were analysed. The comparison suggested that the proposed biasing topology was able to bias the single-stage operational amplifier to make it robust against voltage variation [8].

3 Impacts of Temperature and Supply Variations on Differential Gain

In general, a differential amplifier with active load has a voltage gain of [9].

$$A_V = g_{m(\mathrm{MN2})}\left(r_{ds(\mathrm{MN2})} \| r_{ds(\mathrm{PM2})}\right) \tag{3}$$

where r_{ds} is the small-signal output resistance of the MOSFET (when it is in the saturation region). In a short-channel device, if the channel length modulation effect is considered then the small-signal output resistance is no more infinite, rather it has a finite value [10] given by the inverse of the slope of $I_D - V_{DS}$ curve.

$$r_{ds} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)^{-1} = \frac{1}{\lambda I_D}. \tag{4}$$

here, λ is called the channel length modulation coefficient and I_D is the drain current flowing through the MOSFET. The transconductance (g_m) is the slope of the $I_D - V_{\mathrm{GS}}$ curve at the operating point and is defined in the saturation region as

$$g_m = \frac{\partial I_D}{\partial V_{\mathrm{GS}}} = \mu_n C_{ox} \frac{W}{L}(V_{\mathrm{GS}} - V_{tn})(1 + \lambda V_{DS}) \tag{5}$$

where μ_n, C_{ox}, W, L, V_{GS}, V_{tn}, V_{DS} are electron mobility, gate oxide capacitance per unit area, channel width, channel length, gate-to-source voltage, threshold voltage of NMOSFET, drain-to-source voltage, respectively [11, 12]. From (3) the gain is

$$A_V = g_{m(\mathrm{MN2})}\left(r_{ds(\mathrm{MN2})} \| r_{ds(\mathrm{PM2})}\right). \tag{6}$$

Since, from (5), neglecting channel length modulation, transconductance (g_m) can be written as

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{tn}}) \tag{7}$$

Let $K = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}$ putting in (7), we get

$$g_m = 2K(V_{GS} - V_{tn}) \tag{8}$$

since

$$I_D = K(V_{GS} - V_{tn})^2 \tag{9}$$

Equation (9) can be rewritten as

$$(V_{GS} - V_{tn}) = \sqrt{\frac{I_D}{K}} \tag{10}$$

Substituting $(V_{GS} - V_t)$ in (8), we get

$$g_m = 2\sqrt{(K I_D)} \tag{11}$$

For MN1, transconductance (g_m) is given by

$$g_{m(\mathrm{MN1})} = 2\sqrt{\left(K_{\mathrm{MN1}} I_{D(\mathrm{MN1})}\right)} \tag{12}$$

And since

$$g_{m(\mathrm{MN2})} = g_{m(\mathrm{MN1})} \tag{13}$$

$$g_{m(\mathrm{MN2})} = 2\sqrt{\left(K_{\mathrm{MN1}} I_{D(\mathrm{MN1})}\right)} \tag{14}$$

And, since in this circuit the PMOS are connected in current mirror configuration and the size of PMOS in the current mirror of the differential amplifier is equal,

$$I_{D(\mathrm{MN1})} = I_{D(\mathrm{MN2})} \tag{15}$$

$$I_{\mathrm{SS}} = I_{D(\mathrm{MN1})} + I_{D(\mathrm{MN2})} \tag{16}$$

where I_{SS} is the DC bias current through MN3 and is the sum of the DC currents through MN1 and MN2

From (15) and (16)

$$I_{\mathrm{SS}} = 2I_{D(\mathrm{MN1})} \tag{17}$$

Hence, from (3), (4), (6), the voltage gain A_v can be written as

$$A_v = 2\sqrt{\left(K_{\mathrm{MN1}} I_{D(\mathrm{MN1})}\right)} \frac{1}{\lambda_{\mathrm{MN2}} I_{D(\mathrm{MN2})} + \lambda_{\mathrm{MP2}} I_{D(\mathrm{PM2})}} \tag{18}$$

Using (15),

$$A_v = \sqrt{\left(\frac{K_{\mathrm{MN1}}}{I_{D(\mathrm{MN1})}}\right)} \frac{2}{(\lambda_{\mathrm{MN2}} + \lambda_{\mathrm{MP2}})} \tag{19}$$

Let $K_{\mathrm{MN1}} = \frac{1}{2} K'_{\mathrm{MN1}} \frac{W_{\mathrm{MN1}}}{L_{\mathrm{MN1}}}$, using (17)

$$A_V = \frac{2}{\lambda_{\mathrm{MN2}} + \lambda_{\mathrm{MP2}}} \left(\frac{K'_{\mathrm{MN1}} W_{\mathrm{MN1}}}{I_{\mathrm{SS}} L_{\mathrm{MN1}}}\right)^{\frac{1}{2}} \tag{20}$$

3.1 Impact of Temperature Variations on Differential Gain

The voltage gain A_V varies with temperature mainly due to variations of mobility (μ) and threshold voltage (V_t). The dependence of the mobility (μ) on the temperature is given by

$$\mu(T) = \mu(T_0)\left(\frac{T_0}{T}\right)^m \tag{21}$$

And the dependence of threshold voltage (V_t) on temperature is given by

$$V_t(T) = V_t(T_0) - K(T - T_0) \tag{22}$$

where T_0 is the reference temperature (300 K), K is the threshold voltage temperature coefficient whose typical value is 2.5 mV/K and m is the mobility temperature exponent whose typical value is 1.5 (ideally 1) [5, 13].

Differentiating (21) and (22) with respect to temperature,

$$\frac{\partial \mu}{\partial T} = -\frac{m\mu(T)}{T} \tag{23}$$

$$\frac{\partial V_{\mathrm{tn}}}{\partial T} = -K \tag{24}$$

Similarly,

$$\frac{\partial V_{\mathrm{tp}}}{\partial T} = -K \tag{25}$$

Hence, mobility and threshold voltage both have negative dependence on temperature as can be observed from Eqs. (23) and (24), respectively [14]. Since in the

differential pair, the NMOS transistors are assumed to be matched, so the DC bias current flowing through them can be assumed to be approximately equal [15]. Hence, approximately, I_{SS} can be assumed to be equal to twice the current through MN1, i.e.

$$I_{SS} \approx 2I_{D(MN1)} \tag{26}$$

Using the Eq. (26) and Eq. (20)

$$A_V = \frac{2}{\lambda_{MN2} + \lambda_{MP2}} \left\{ \frac{\mu_n C_{ox} W_{MN1}}{\mu_n C_{ox} \frac{W_{MN1}}{L_{MN1}} \left(V_{ref} - V_{D(MN3)} - V_{th}\right)^2 L_{MN1}} \right\}^{\frac{1}{2}} \tag{27}$$

Equation (27) on simplification yields,

$$A_V = \frac{2}{\lambda_{MN2} + \lambda_{MP2}} \frac{1}{\left(V_{ref} - V_{D(MN3)} - V_{tn}\right)} \tag{28}$$

From (2),

$$V_{ref} - V_{tn} = \frac{V_{DD} - \left|V_{tp}\right| + \sqrt{\frac{\beta_N}{\beta_P}}(V_{tn})}{\sqrt{\frac{\beta_N}{\beta_P}} + 1} - V_{tn} \tag{29}$$

which yields,

$$V_{ref} - V_{tn} = V_{DD} - \left|V_{tp}\right| - V_{tn} \tag{30}$$

Substituting Eq. (30) in Eq. (28) results in,

$$A_V = \frac{2}{\lambda_{MN2} + \lambda_{MP2}} \frac{1}{\left(V_{DD} - \left|V_{tp}\right| - V_{tn} - V_{D(MN3)}\right)} \tag{31}$$

The negative temperature dependence of the threshold voltage V_{tn} and V_{tp} results in decreased threshold voltage values, hence, the term $V_{DD} - \left|V_{tp}\right| - V_{tn}$ increases. Hence, increase in the temperature causes the overall gain to decrease which can be verified from Fig. 3.

3.2 Impact of Process Variation on Differential Gain

The variation of the voltage gain with the variation in channel length of the inverting transistor is as shown in Fig. 4. The voltage gain decreases with the increase in channel length.

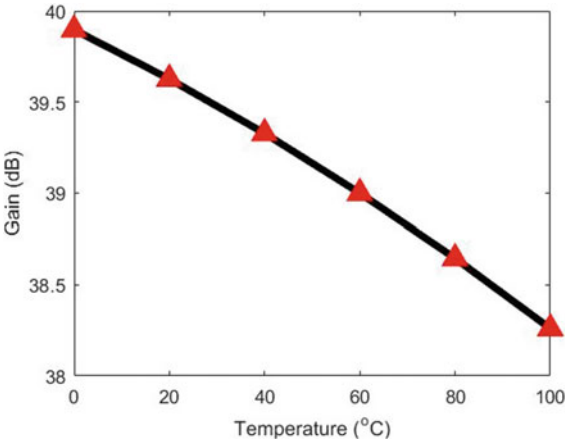

Fig. 3 Gain versus temperature for bias 3. As can be observed, the gain decreases with the increase of the temperature

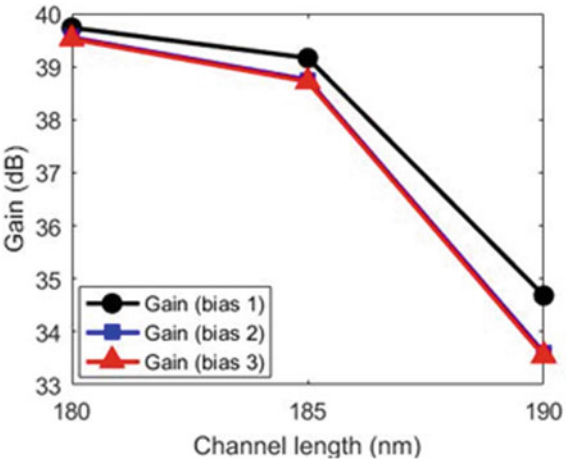

Fig. 4 Variation of voltage gain with the variation of channel length of inverting transistor

The variations of the voltage gain with the channel width of the inverting transistor are as shown in Fig. 5. The voltage gain increases with the increase of the channel width.

3.3 Impact of Voltage Variation on Differential Gain

Similarly, the variation of the voltage gain A_V with the supply voltage variation is also analysed and it is observed that the voltage gain increases with the increase in supply voltage as shown in Fig. 6.

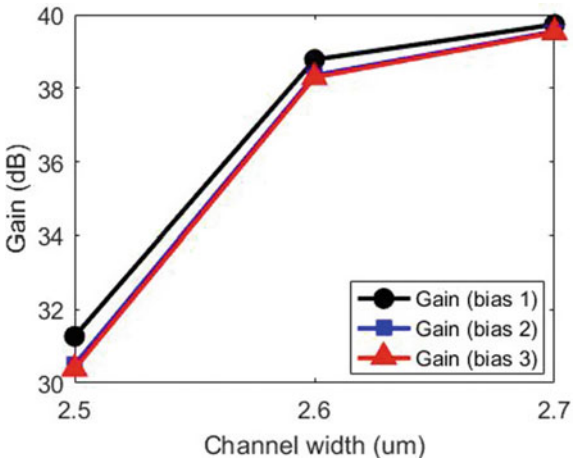

Fig. 5 Variation of voltage gain with the variation of channel width of inverting transistor

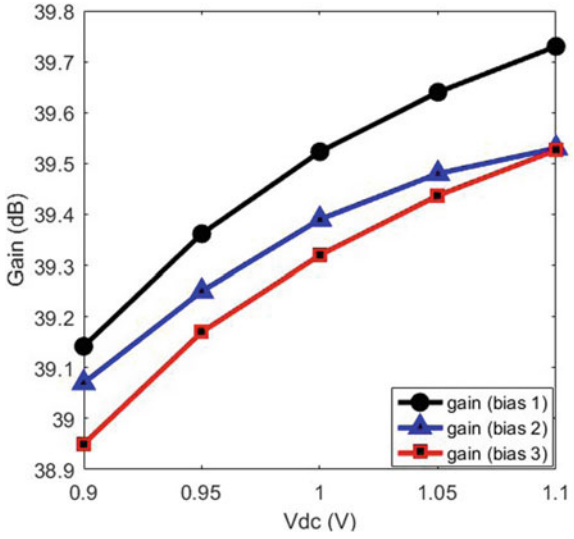

Fig. 6 Voltage gain versus supply voltage (V_{DD})

4 Conclusion

This paper proposes an active-loaded differential amplifier with a constant g_m biasing circuit which has enhanced immunity of the amplifier to PVT variations. The impact of PVT variations on the differential gain was analysed and it was observed that the differential gain has (a) Negative dependence on the temperature; (b) Positive dependence on the supply voltage; Negative dependence on channel length and positive dependence on the channel width.

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A Compact Microstrip-Fed Dual Band Printed Antenna with Enhanced Bandwidth Incorporating L-Shaped DGS for Wireless Applications

Binoy Kumar Paul, Apurba Chowdhury, Sudipta Das, and Swarup Sarkar

Abstract A miniaturized defected ground plane microstrip antenna fed by a microstrip line is presented in this paper. The proposed antenna offers multiresonant wideband characteristics by defecting its ground plane using an L-shaped slot having unequal arms. The dimension of the proposed antenna is only 448 mm^2 (24.7 mm $\times$ 18.17 mm) and the designed structure is very simple. The designed antenna simultaneously offers both the narrowband and wideband resonance characteristics. The presence of L-shaped DGS broadens the bandwidth of the antenna and also offers miniaturization by lowering the first resonant frequency at 2.44 GHz. The simulated results show that the proposed antenna offers a fractional bandwidth of 6.55 (2.36–2.52 GHz) and 38.8% (6.96–10.32 GHz) for $S_{11} \leq -10$ dB which supports a number of modern wireless application bands such as IEEE 802.11.b (2.400–2.484 GHz), WLAN (2.4–2.484 GHz), Wi-Fi (2.412–2.4835 GHz), X-band satellite communication (6.75–7.5 GHz), ITU-8 GHz band communication services (7.9–8.5 GHz), and RN band (9.0–10.0 GHz).

Keywords Microstrip antenna · L-shaped slot · Defected ground structure (DGS) · Wireless communication

B. K. Paul · S. Das
Department of Electronics and Communication Engineering, IMPS College of Engineering & Technology, Malda, India
e-mail: binoy931@gmail.com

S. Das
e-mail: sudipta.das1985@gmail.com

A. Chowdhury (✉)
Mallabhum Institute of Polytechnic, Bishnupur, Bankura, India
e-mail: 2apurba@gmail.com

S. Sarkar
Department of Electronics and Communication Engineering, Sikkim Manipal Institute of Technology (SMIT), Majitar, Sikkim, India
e-mail: swarup.s@smit.smu.edu

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1 Introduction

In recent years, rapid developments have been observed in the field of wireless communication systems. In recent days, the developed modern communication systems are very compact in size. Actually, the dimensions of those wireless systems depend on the space occupied by the several wireless pieces of equipment, whose dimensions, in turn, depends on the size of the discrete components used inside these wireless devices. The antenna plays a vital role as a key component for the establishment of an efficient wireless communication system. Hence, the demand for small, efficient, multiband/wideband and lightweight microstrip patch antennas has been increased due to the miniaturization of wireless equipment. The implementations of separate antennas for separate application bands are usually restricted due to the limited space and cost constraints of the systems. So, the design aspects of multiband antenna or an antenna with wide operating bandwidth has become a topic of interest among the researchers. But the serious problem of the microstrip patch antennas is its narrow bandwidth (2–3%). Researchers have suggested many design methods to reach the goal of achieving enhanced bandwidth to support multiple communication systems simultaneously using a single antenna. The reported design techniques for achieving bandwidth enhancement include L probe feeding [1], I-slotted rectangular patch [2], asymmetric U slot patch [3], E-H shaped patch [4], Zig-Zag slots [5], meandering slots [6], stacked patch configuration [7], etc. Many researchers have also proposed the modified monopole configurations [8–14] to realize bandwidth enhanced operation.

This work also represents the design of a wideband antenna with dual band performance. The design objective of the present paper is to achieve dual band characteristics with sufficient operating bandwidth to support the bandwidth requirements of multiple wireless communication systems. In this article, a miniaturized bandwidth enhanced printed dual band antenna is proposed. An L-shaped DGS is incorporated at the ground plane of the antenna to support some crucial requirements of modern wireless communication systems like size reduction and wideband operation. The advantages of the proposed antenna may be summarized as follows:

1.1 Simple Structure

The structure of the antenna is very simple and designed using FR-4 substrate. A simple L-shaped DGS with unequal arms is embedded at the backside of the antenna and no modifications have been made in the geometry of the patch. The patch is fed by microstrip line and hence it can be easily integrated for practical applications.

1.2 Small Size

The compact dimension is another attractive feature of the designed antenna. The proposed antenna occupies an area of only 448 mm^2 (24.7 mm × 18.17 mm).

1.3 Wide Operating Bandwidth

The proposed antenna offers sufficiently broad dual frequency bands of 160 MHz (2.36–2.52 GHz), and 3360 MHz (6.96–10.32 GHz).

1.4 Less Interference

The proposed dual band antenna shows a centre frequency ratio of about 3.54 which signifies less interference between the operating frequency bands and better frequency rejection.

1.5 Better Gain

The peak gain of the suggested antenna has reached a value of 4.71 dBi while maintaining wide operating bandwidth, which confirms its applicability for the desired area of applications.

1.6 Wide Range of Applications

The bandwidth achieved by the proposed antenna for dual operating bands cover IEEE 802.11.b (2.400–2.484 GHz), WLAN (2.4–2.484 GHz), Wi-Fi (2.412–2.4835 GHz), X-band satellite communication (6.75–7.5 GHz), ITU-8 GHz band communication services (7.9–8.5 GHz), and RN band (9.0–10.0 GHz). So, the novelty of the proposed model is that the single designed model covers many design considerations of a microstrip antenna such as reduced size, dual band, good gain, and wide operating impedance bandwidth.

2 Antenna Design

The complete designed structure of the proposed antenna is shown in Fig. 1. The proposed antenna is designed using a low-cost FR-4 substrate of thickness 1.6 mm and dielectric constant of 4.4. The method of moment-based electromagnetic simulator IE3D [15] is used for the geometry and simulated results analysis of the proposed antenna structure. The top side of the proposed antenna consists of a simple rectangular radiating patch of size 16 × 12 mm^2 and a 50 Ω microstrip feed line of width 2 mm and length 8 mm. The backside of the antenna consists of a ground plane of size 18.17 mm × 24.7 mm. An L-shaped DGS with unequal arms is introduced at the back of the antenna to lower the resonant frequency of the lower band to support WLAN and also to improve the bandwidth performance at the upper band to support X-band satellite communication. The design parameters are optimized to achieve the required bandwidth for supporting X-band satellite communication and WLAN applications. The optimal dimensions are $L_P = 12$ mm, $W_P = 16$ mm, $W_f = 2$ mm, $L_f = 8$ mm, $W_g = 24.7$ mm, $L_g = 18.17$ mm, $W_1 = 3$ mm, $L_1 = 11$ mm, $W_2 = 4$ mm, $L_2 = 13$ mm.

2.1 Design Evolution of Proposed Antenna

The stepwise evolution of the desired antenna from the basic structure is shown in Fig. 2. The corresponding simulated results (S_{11} parameter) for different design cases

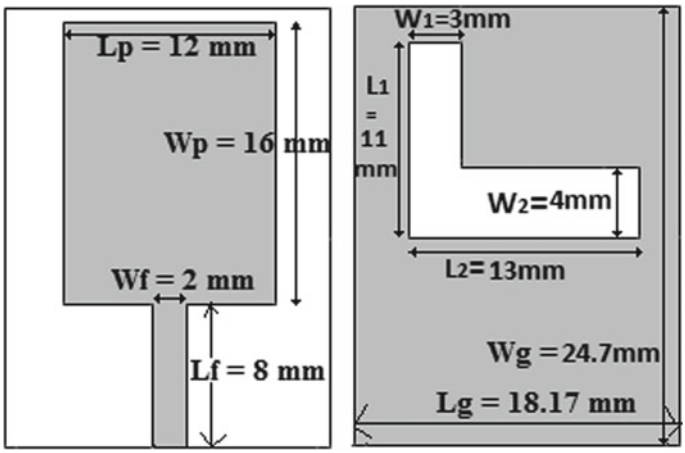

Fig. 1 The structure of the proposed antenna **a** top view (patch with microstrip feed line), **b** back view (defected ground plane structure)

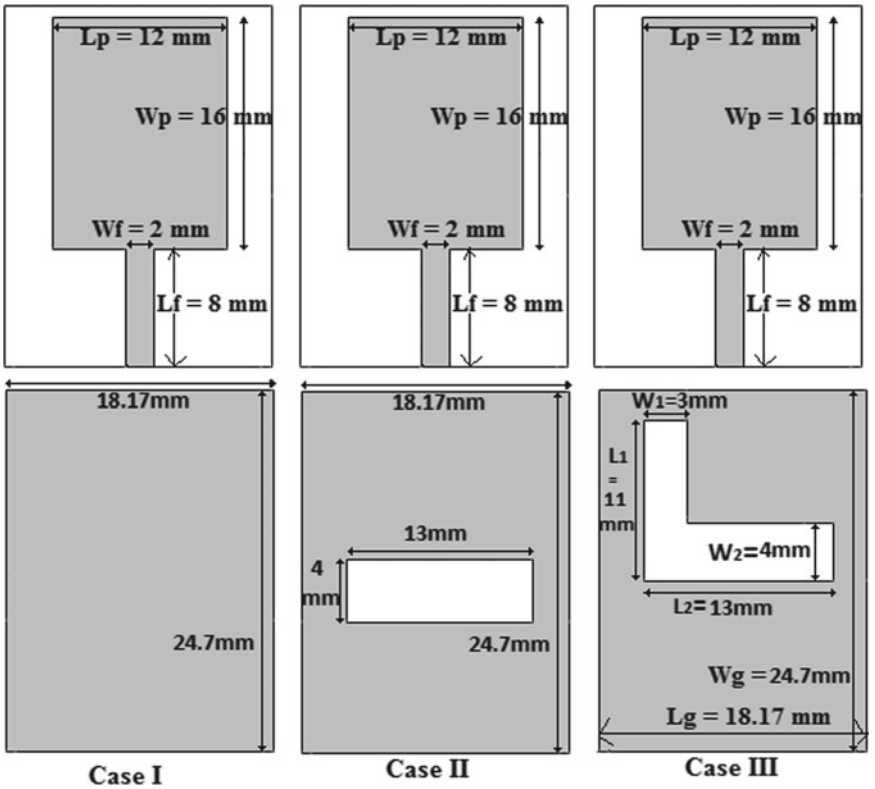

Fig. 2 Design evolutions of the proposed antenna

are shown in Fig. 3. The resonance response of the antenna structures in each of the design steps is analyzed using IE3D simulation software. In Case I, the first resonant frequency is cantered at 4.8 GHz with a reflection coefficient of about −27 dB, and also dual band characteristics are obtained for $S_{11} < -10$ dB ranging from 6.96 to 8.2 GHz and 9.1 to 10.2 GHz. The insertion of a wide horizontal slot in the ground plane has changed the resonance response of the antenna [Case II]. Although the first resonant frequency remains almost unaltered there is a slight improvement in terms of bandwidth for the first band. The second resonant frequency is shifted to 6.4 GHz for this case. The −10 dB bandwidth for the third band reaches 1700 MHz (8.2–9.9 GHz) due to the presence of a wide horizontal slot. But the presence of wide notched band blocks working frequency band (6.75–7.5 GHz) of X-band satellite communications. In Case III, the addition of a wide vertical slot in the ground plane (forming an L-shaped DGS) has further lowered the resonant frequency to 2.44 GHz with −10 dB impedance bandwidth of 84 MHz (2.36–2.52 GHz), which covers the bandwidth requirements of IEEE 802.11.b (2.400–2.484 GHz), WLAN (2.4–2.484 GHz), Wi-Fi (2.412–2.4835 GHz). Due to the presence of this L-shaped DGS, the existing notched band as observed in Case II has been removed and the antenna offers wide operating

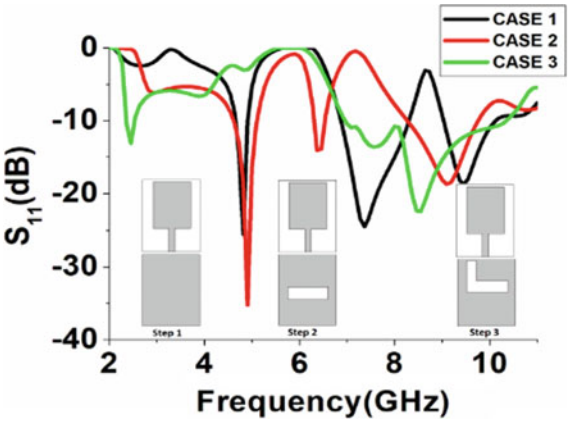

Fig. 3 Simulated reflection coefficient (S_{11}) for different cases

bandwidth. The operating bandwidth at the upper band is enhanced by 1660 MHz and the new operating band is extended from 6.96 to 10.32 GHz which can cover the frequency band designated for X-band satellite communication (6.75–7.5 GHz), ITU-8 GHz communication (7.9–8.5 GHz), and RN band (9.0–10.0 GHz).

3 Effect of Structural Parameters

The dominant effects of each structural parameter on the resonance response of the antenna are examined through a parametric study. The effects of the design parameters with a significant effect are observed and analyzed by changing a single geometry parameter at a time while all other structural parameters remain fixed at the time of the simulation. The parameters L_1 of horizontal slot and L_2 of vertical slot have a major influence on the bandwidth and reflection coefficients of the proposed antenna. The variations of L_1 do not have any prominent effect on the bandwidth of the upper band. According to Fig. 4, when L_1 decreases to 2 mm, the antenna is not properly excited and does not radiate below -10 dB level for the lower band. But the value of S_{11} must be at least -10 dB for an antenna to be treated as an efficient radiator in the far-field region. Again, when the parameter L_1 is increased to 4 mm, the operating bands remain almost the same for both the lower and upper bands. However, the best impedance matching for the lower band is achieved for $L_1 = 3$ mm. Simulated S_{11} curves for different values of L_2 are illustrated in Fig. 5. The parameter L_2 has a significant effect on the lower band. For the lower band, when $L_2 =$ 12 mm, the antenna offers poor impedance matching. For $L_2 = 14$ mm, the antenna offers excellent impedance matching with maximum reflection coefficient but the operating frequency is shifted to 2.3 GHz (2.21–2.39 GHz) which does not cover the intended WLAN applications. So, $L_2 = 13$ mm is selected as an optimum parameter. For the upper band, the variation of L_2 does not have any major influence on the upper band except for $L_2 = 12$ mm, for which the impedance matching degrades

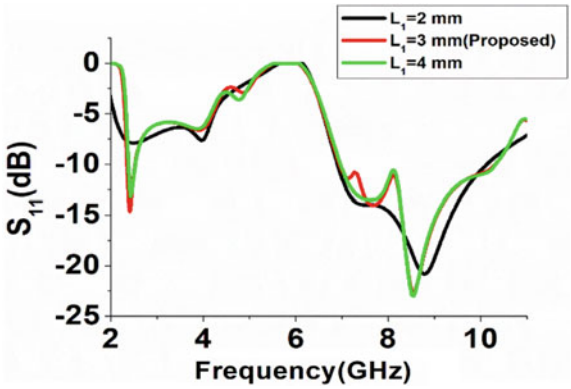

Fig. 4 S_{11} variations as a function of L_1 parameter

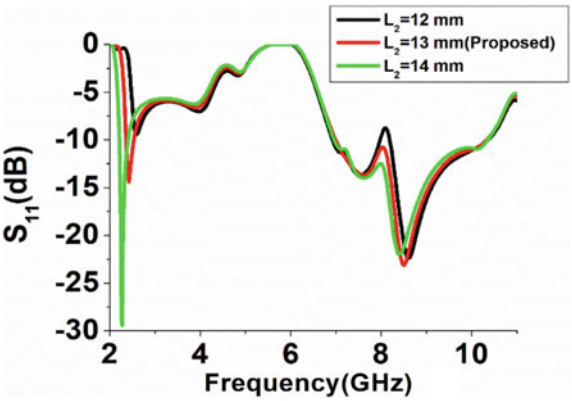

Fig. 5 S_{11} variations as a function of L_2 parameter

at the upper band. The current distributions of the proposed antenna for the dual band operation are shown in Fig. 6. For the lower band at 2.36 GHz operation (see Fig. 6a), a highly concentrated current density is observed around the L-shaped slot. It is also observed from Fig. 6b that for the upper band, the surface current is mainly concentrated around the vertical arm of the L-shaped DGS of the ground plane.

4 Results and Discussion

The simulated reflection coefficient of the proposed antenna is depicted in Fig. 7. The proposed antenna offers dual band characteristics with much-improved bandwidth at the upper band due to the presence of an L-shaped DGS on the ground plane of the designed antenna. The proposed antenna is capable to operate with a bandwidth of 160 MHz (2.36–2.52 GHz), which is 6.55% bandwidth around the centre frequency 2.44 GHz. Another wide operating bandwidth of 3360 MHz is obtained from 6.96

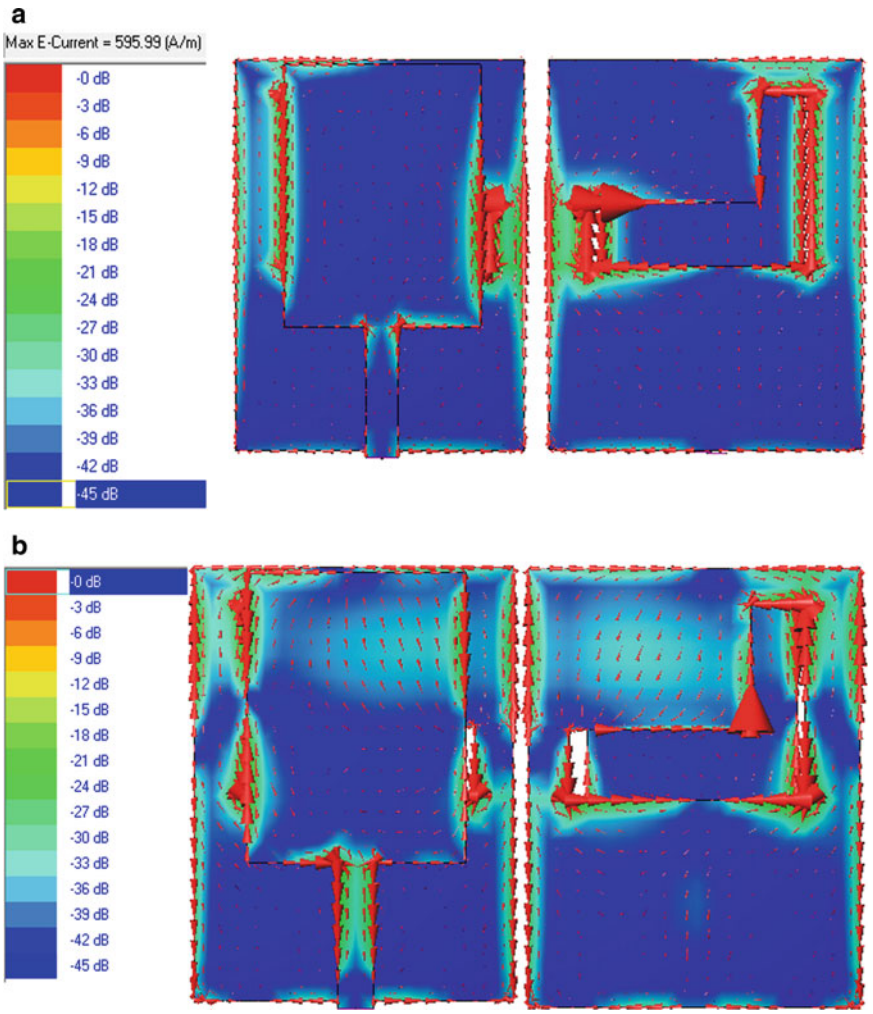

Fig. 6 **a** Current distribution of the designed antenna at 2.36 GHz. **b** Current distribution of the designed antenna at 8 GHz

to 10.32 GHz, which is 38.8% bandwidth around the centre frequency of 8.64 GHz. The simulated gain and directivity are shown in Fig. 8. It is observed from Fig. 8 that the antenna has attained a peak gain of 4.71 dBi at 6.96 GHz. The directivity of the designed antenna attains a maximum value of 7.31 dBi at 7.18 GHz. The E plane co-pol and cross-polarization radiation patterns for 2.36 GHz, 7.1 GHz, and 8 GHz are shown in Fig. 9a–c, respectively. The H plane patterns for the same frequencies indicating the variations of co and cross-pol are illustrated in Fig. 9d–f. The proposed antenna shows bidirectional radiation characteristics and this may

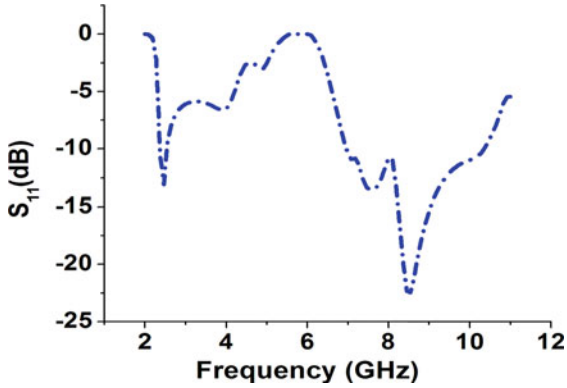

Fig. 7 S_{11} parameter of the proposed antenna

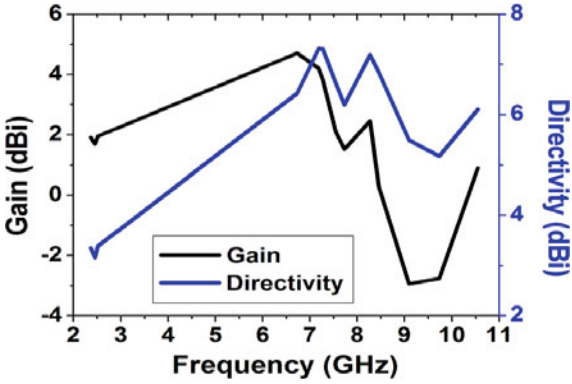

Fig. 8 Gain and directivity of the proposed antenna

be due to the change in surface current distributions because of the presence of L-shaped defect at the backside (ground plane) of the antenna. The voltage standing wave ratio (VSWR) of the designed antenna is also predicted in Fig. 10. The VSWR lies within 2, which confirms practical acceptable mismatch loss throughout dual operating bands. The mapped 3D radiation patterns are depicted in Figs. 11, 12 and 13 for a better presentation of the radiation characteristics of the proposed antenna.

5 Performance Comparison of Some Dual Band Antennas with the Proposed Antenna

The performance characteristics parameters of the suggested antenna with respect to the dimension, bandwidth at dual operating band and gain with some other related dual band antennas [8–11] is shown in Table 1. It can be concluded that the proposed antenna offers best performance in terms of size, gain, fractional bandwidth compared to reported dual band antennas.

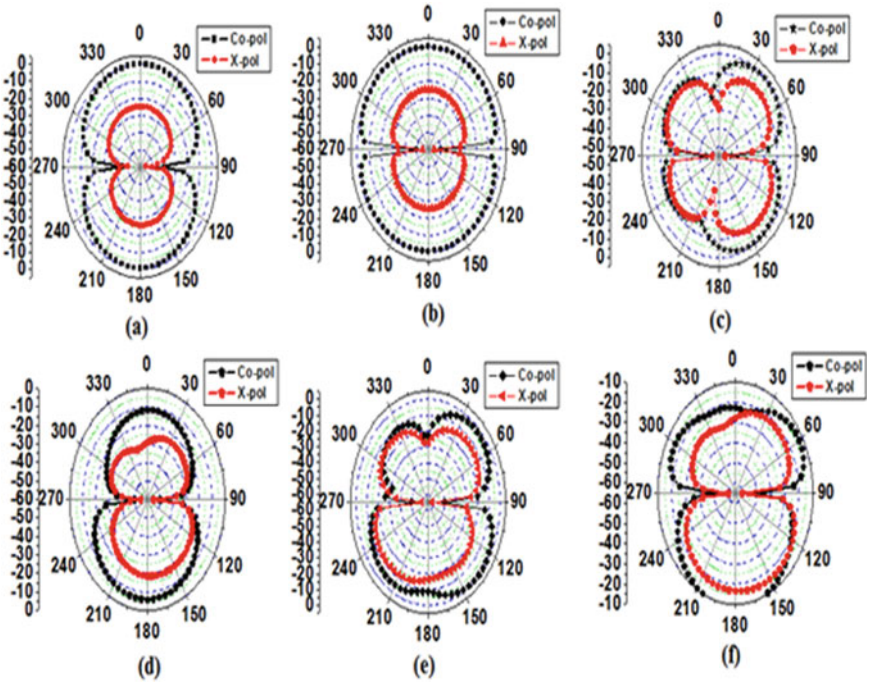

Fig. 9 Simulated E plane radiation patterns at **a** 2.36 GHz, **b** 7.1 GHz and **c** 8 GHz and H plane patterns at **d** 2.36 GHz, **e** 7.1 GHz and **f** 8 GHz

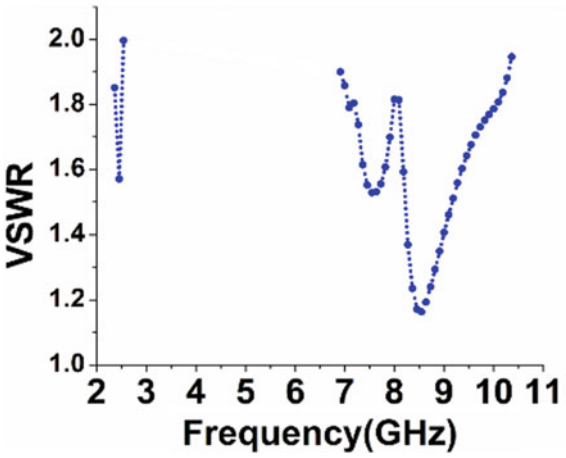

Fig. 10 VSWR versus frequency of the proposed antenna

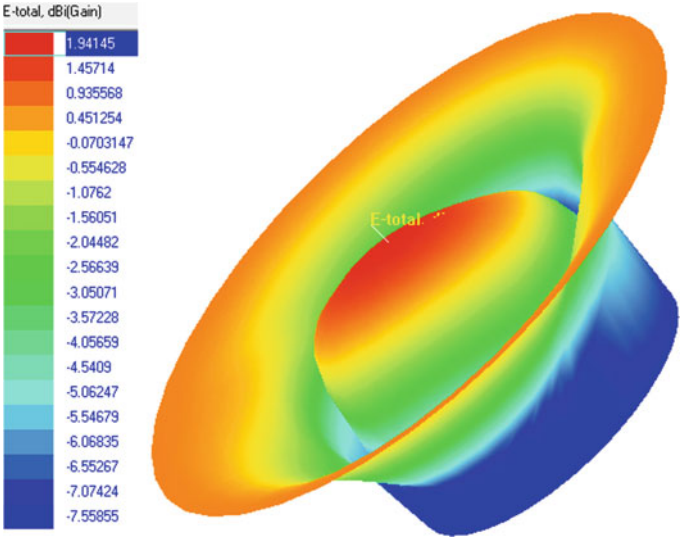

Fig. 11 3D radiation pattern at 2.36 GHz

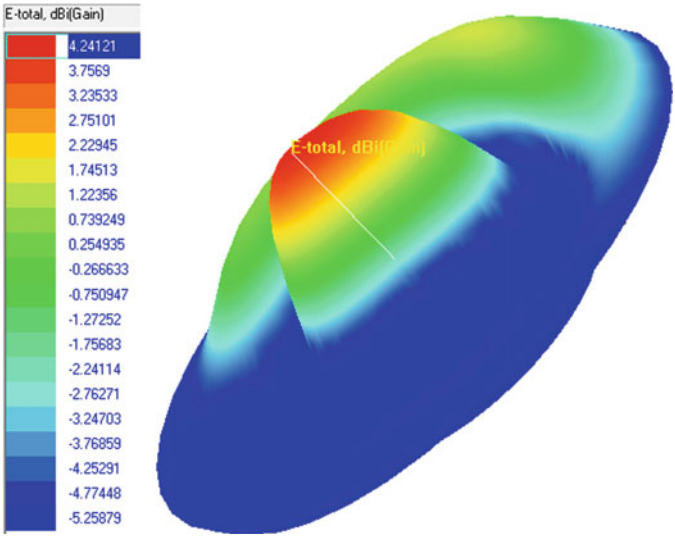

Fig. 12 3D radiation pattern at 7.1 GHz

6 Conclusion

A miniaturized dual band antenna using an L-shaped DGS is discussed. The proposed antenna shows dual band (2.36–2.52 GHz) and (6.96–10.32 GHz) operations which

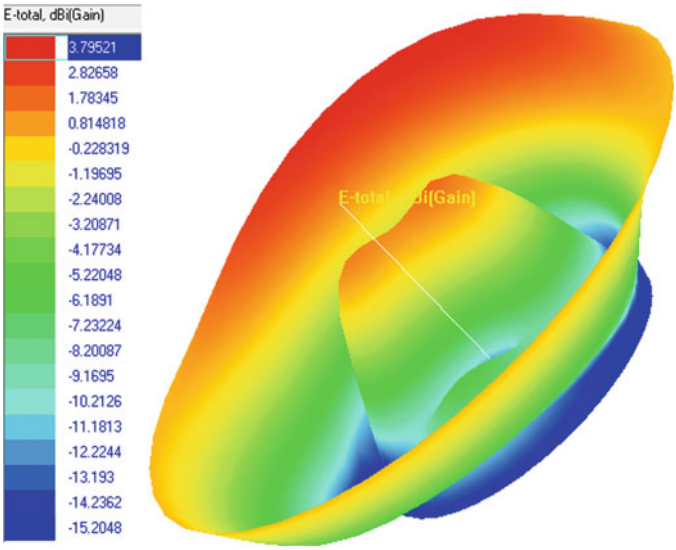

Fig. 13 3D radiation pattern at 8 GHz

Table 1 Performance comparison of some dual band antennas with the proposed antenna

Reference No	Antenna size (mm^2)	−10 dB bandwidth (GHz)		Bandwidth (%)		Peak gain (dBi)
		First band	Second band	First band	Second band	
[8]	60 × 50	2.4–2.5	5.725–5.875	4.08	2.58	2.8
[9]	38 × 38	2.4–2.48	5.15–5.825	6.1	23.2	4.03
[10]	50 × 30	2.386–2.51	4.878–6.0	5.1	22.4	4.3
[11]	50 × 45	2.4–2.49	5.15–5.93	3.68	14.07	3.04
Proposed	24.7 × 18.17	2.36–2.52	6.96–10.32	6.55	38.8	4.71

covers the frequency bands: IEEE 802.11.b (2.400–2.484 GHz), WLAN (2.4–2.484 GHz), Wi-Fi (2.412–2.4835 GHz), X-band satellite communication (6.75–7.5 GHz), ITU-8 GHz band (7.9–8.5 GHz), and RN band (9.0–10.0 GHz). The designed planar antenna is very simple to fabricate using FR-4 substrate. Such type of antenna may be applicable in wireless communication systems where simple geometry, good gain, wide bandwidth, stable radiation patterns, lightweight, and compact dimension is highly desirable.

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A Current-Mode Memristor Emulator Circuit

Vikash Kumar, Shashank Kumar Dubey, and Aminul Islam

Abstract In this paper, a new current-controlled memristor emulator circuit based on voltage differencing transconductance amplifier (VDTA) as an active circuit element is proposed. The proposed emulator circuit is simulated on the 180 nm CMOS technology node making it both cost and power-efficient emulator circuit. All the analytical derivations mentioned in this research work have been verified by simulation results obtained using virtuoso custom design platform of Cadence. The non-volatile nature of the proposed circuit has also been validated.

Keywords Current-controlled memristor · Voltage differencing transconductance amplifier · Electronically tunable · Voltage multiplier

1 Introduction

Fano et al. listed the fourth unknown fundamental circuit element in [1] and later on it was mathematically realized by Prof. Leon Chua, in his paper [2] and this unknown element is named after its characteristic behavior as memristor (resistor + memory). The announcement of the practical realization of nanoscale memristor using TiO_2 by the HP team [3] has attracted interest from the researchers towards it. The practical realization has provided a reference model that led to the proposition of several emulator circuits [4–8] as physical memristor is not commercialized till date. As such a linear resistor forms a relation between "voltage" and "current" and the two other fundamental elements capacitor and inductor form the relation between

V. Kumar
Department of Electronics and Communication Engineering, Presidency University, Bengaluru, Karnataka 560064, India
e-mail: vikashkumar@ieee.org

S. K. Dubey · A. Islam (✉)
Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra, Ranchi, Jharkhand, India
e-mail: aminulislam@bitmesra.ac.in

S. K. Dubey
e-mail: dubey.shashank1991@gmail.com

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"voltage" and "charge" and "current" and "flux", respectively. Similarly, the two-terminal passive elements, memristor, form the missing relation between "flux" and "charge". The memristance, which exhibits pinched hysteresis behavior, depends on the direction of current flow, i.e., when current is allowed to pass in one direction, the memristance increases whereas it decreases once the direction of current is changed. The memristor is a versatile element due to its non-volatile behavior and therefore are used in high-density memory circuits [9–11] and neuromorphic systems [12–14]. A memristor can also be employed in various analog and digital applications such as programmable sinusoidal oscillators [15, 16], adaptive filters [17], chaotic circuits [18], logic gates [19], and digital multipliers [20].

In this paper, a new model that produces pinched hysteresis behavior of a memristor has been realized using voltage differencing transconductance amplifier (VDTA) and voltage multiplier.

The paper is organized as follows. In Sect. 2, CMOS realization of voltage differencing transconductance amplifier and Gilbert-cell-based four-quadrant voltage multiplier are explained. Section 3 provides the configuration of the proposed emulator circuit. Section 4 includes the simulation results from the emulator circuit. Finally, Sect. 5 reflects the conclusions obtained from the work done.

2 Active Blocks of Proposed Emulator

The two active blocks used for realizing the memristor emulator circuit are voltage differencing transconductance amplifier [21] and Gilbert-cell-based four-quadrant analog voltage multiplier. Figures 1 and 2 shows block diagram of VDTA and its CMOS technology realized schematic [22]. Basically, a VDTA consists of two operational transconductance amplifiers (OTAs) cascaded together as seen in Fig. 2.

The following matrix equation shows the current and voltage relations of VDTA's input–output ports:

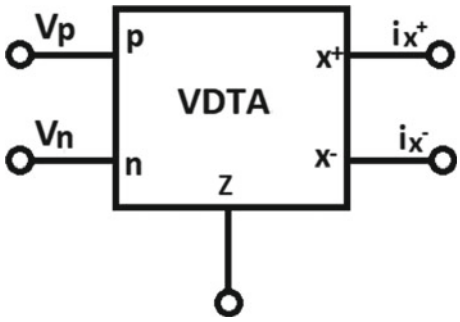

Fig. 1 Block diagram of VDTA

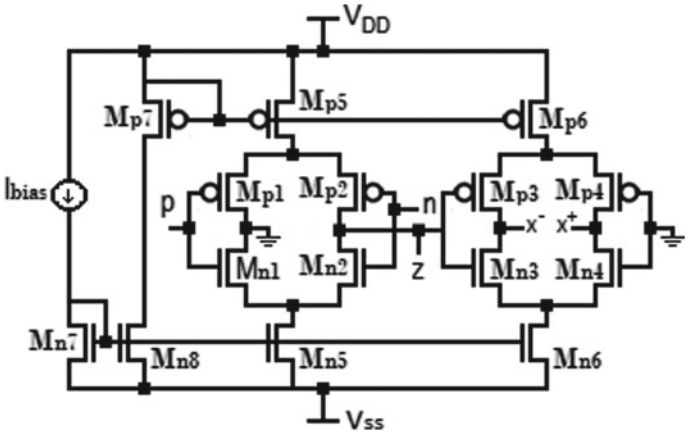

Fig. 2 Schematic of CMOS realized VDTA

$$\begin{bmatrix} i_z \\ i_{x^+} \\ i_{x^-} \end{bmatrix} = \begin{bmatrix} g_{\mathrm{mf}} & -g_{\mathrm{mf}} & 0 \\ 0 & 0 & g_{\mathrm{ms}} \\ 0 & 0 & -g_{\mathrm{ms}} \end{bmatrix} * \begin{bmatrix} V_p \\ V_n \\ V_z \end{bmatrix}. \tag{1}$$

Here, V_p, V_n, V_z, V_{x^+}, V_{x^-}, and i_{x^+}, i_{x^-}, i_z are potential drops and currents at their respective VDTA ports. Current in p and n ports equal to zero due to very high impedance across them. g_{mf} and g_{ms} are effective transconductances of first and second OTAs, respectively, and are given as [23]

$$g_{\mathrm{mf}} = \frac{g_{\mathrm{mn1}} * g_{\mathrm{mn2}}}{g_{\mathrm{mn1}} + g_{\mathrm{mn2}}} + \frac{g_{\mathrm{mp1}} * g_{\mathrm{mp2}}}{g_{\mathrm{mp1}} + g_{\mathrm{mp2}}}, \tag{2}$$

$$g_{\mathrm{ms}} = \frac{g_{\mathrm{mn3}} * g_{\mathrm{mn4}}}{g_{\mathrm{mn3}} + g_{\mathrm{mn4}}} + \frac{g_{\mathrm{mp3}} * g_{\mathrm{mp4}}}{g_{\mathrm{mp3}} + g_{\mathrm{mp4}}}. \tag{3}$$

where $g_{\mathrm{m1}}, g_{\mathrm{m2}}, g_{\mathrm{m3}} \ldots g_{\mathrm{m7}}, g_{\mathrm{m8}}$ are individual transistor transconductances and can be calculated by using the following relation:

$$g_{\mathrm{mk}} = \sqrt{2 * \beta * I_{\mathrm{DS}}} \text{ and } \beta = \frac{\mu_k * C_{\mathrm{ox}}}{2}\left[\frac{W}{L}\right] \tag{4}$$

Here, μ_k is the mobility of kth transistor, C_{ox} is the ratio of oxide permittivity to its thickness, W and L are transistor dimensions and I_{DS} is drain-to-source current.

Figure 3 shows the voltage mode continuous signal multiplier block based on Gilbert cell. It consists of two differential pairs cross-coupled whose branch currents are controlled by one of the input sources [24]. The symmetry of the cell makes it a perfect replica as such of actual multiplication.

The output voltage (V_0) of the multiplier for a given voltage inputs (V_{in1}, V_{in2}) at "x" and "y" ports is given by

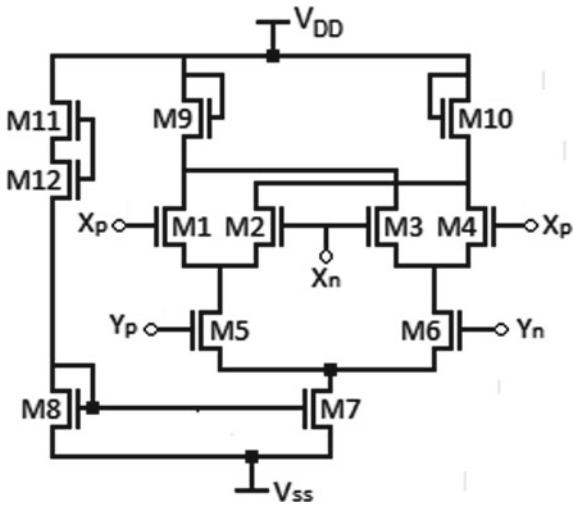

Fig. 3 Schematic of Gilbert-cell-based voltage multiplier

$$V_0 = \eta * V_{\text{in1}} * V_{\text{in2}}, \tag{5}$$

where η is the multiplier constant and is process dependent.

3 Emulator Circuit

The proposed emulator circuit for depicting the behavior of memristor is shown in Fig. 4. In this emulator, the excitation signal is provided at the p port and x^- port of VDTA-1, and the output obtained from the x^+ port is fed to resistor R_2. The corresponding potential developed is fed to VDTA based integrator circuit and to the voltage multiplier. Another input of voltage multiplier comes from x^+ port

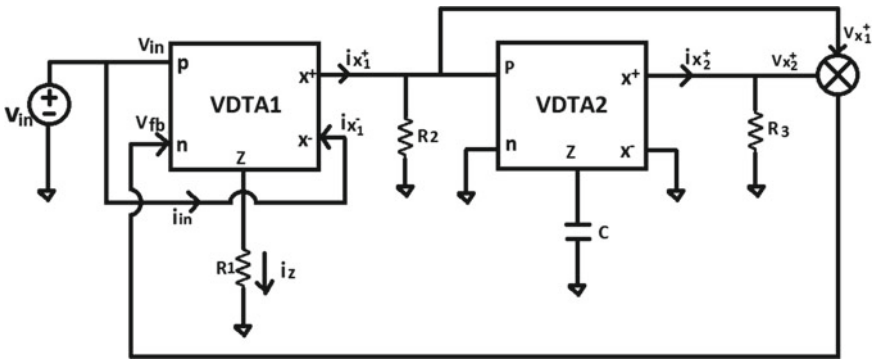

Fig. 4 Memristor emulator schematic based on VDTA

of VDTA-2. Finally, the output of the voltage multiplier is fed back to n port of VDTA-1.

Instead of several macro models for memristor available to-date, real-world requires physical implementation of models to better test its ability for a particular application and this is where an emulator comes into the picture. The drain-to-source current (I_{DS}) is controlled using bias current (I_{bias}) as shown in Fig. 2 making the proposed emulator regulatable. Symmetrical structures of both VDTA and multiplier makes it possible to have lower mismatches during the fabrication and making it a versatile device to use in emulator design.

Following derivation shows how memristance is obtained using transfer characteristics of the aforementioned active devices.

From VDTA-1

$$V_{p1} = V_{\mathrm{in}} \tag{6}$$

$$V_{n1} = V_{\mathrm{fb}} \tag{7}$$

$$i_{z1} = g_{\mathrm{m}} * (V_{\mathrm{in}} - V_{\mathrm{fb}}) \tag{8}$$

$$V_{z1} = i_{z1} * R_1 = g_{\mathrm{m}} * (V_{\mathrm{in}} - V_{\mathrm{fb}}) * R_1 \tag{9}$$

$$i_{x1}^{+} = g_{\mathrm{m}} * V_{z1} = g_{\mathrm{m}}^2 * (V_{\mathrm{in}} - V_{\mathrm{fb}}) * R_1 \tag{10}$$

$$i_{x1}^{-} = i_{\mathrm{in}} = -g_{\mathrm{m}} * V_{z1} = -g_{\mathrm{m}}^2 * (V_{\mathrm{in}} - V_{\mathrm{fb}}) * R_1 \tag{11}$$

$$V_{x1}^{+} = i_{x1}^{+} * R_2 = g_{\mathrm{m}}^2 * (V_{\mathrm{in}} - V_{\mathrm{fb}}) * R_1 * R_2 \tag{12}$$

From VDTA-2

$$V_{p2} = V_{x1}^{+} \tag{13}$$

$$V_{n1} = 0 \tag{14}$$

$$i_{z2} = g_{\mathrm{m}} * V_{X1}^{+} = g_{\mathrm{m}}^3 * R_1 * R_2 * (V_{\mathrm{in}} - V_{\mathrm{fb}}) \tag{15}$$

Using the above relation, we have

$$V_{z2} = \frac{1}{C} * \int i_{z2} * \mathrm{d}t = \frac{g_{\mathrm{m}}^3 * R_1 * R_2}{C} * \int (V_{\mathrm{in}} - V_{\mathrm{fb}}) * \mathrm{d}t \tag{16}$$

$$i_{x2}^{+} = g_{\mathrm{m}} * V_{z2} = \frac{g_{\mathrm{m}}^{4} * R_1 * R_3}{C} * \int (V_{\mathrm{in}} - V_{\mathrm{fb}}) * \mathrm{d}t \tag{17}$$

$$V_{x2}^{+} = i_{x2}^{+} * R_3 = \frac{g_{\mathrm{m}}^{4} * R_1 * R_2 * R_3}{C} * \int (V_{\mathrm{in}} - V_{\mathrm{fb}}) * \mathrm{d}t \tag{18}$$

From Multiplier:

$$V_{\mathrm{fb}} = \eta * V_{x1}^{+} * V_{x2}^{+} \tag{19}$$

Substituting (12) and (18) in (19), we get

$$V_{\mathrm{fb}} = \eta * \{R_2 * (-i_{\mathrm{in}})\} * \left\{ \frac{g_{\mathrm{m}}^{2} * R_2 * R_3}{C} * \int (-i_{\mathrm{in}}) * \mathrm{d}t \right\} \tag{20}$$

This implies

$$V_{\mathrm{fb}} = \frac{\eta * g_{\mathrm{m}}^{2} * R_2^{2} * R_3}{C} * i_{\mathrm{in}} * \int i_{\mathrm{in}} * \mathrm{d}t \tag{21}$$

Eliminating V_{fb} in (11) using (21), we get

$$\frac{-i_{\mathrm{in}}}{g_{\mathrm{m}}^{2} * R_1} = V_{\mathrm{fb}} - \frac{\eta * g_{\mathrm{m}}^{2} * R_2^{2} * R_3}{C} * i_{\mathrm{in}} * \int i_{\mathrm{in}} * \mathrm{d}t \tag{22}$$

Thus, the proposed circuit realizes a current-controlled memristance.

$$R_{\mathrm{m}} = \frac{V_{\mathrm{in}}}{i_{\mathrm{in}}} = \frac{-1}{g_{\mathrm{m}}^{2} * R_1} + \frac{\eta * g_{\mathrm{m}}^{2} * R_2^{2} * R_3}{C} * \int i_{\mathrm{in}} * \mathrm{d}t \tag{23}$$

4 Simulation Results

All the simulations are performed using 180-nm CMOS technology with virtuoso analog design environment of Cadence. All the transistors are biased into saturation with dual rail power supply of ±900 mV and bias current of 50 μA. Bias current can be varied in order to tune the prototype circuit externally.

Figure 5 shows the pinched hysteresis behavior of memristor with variations in frequency. It can be observed that as the frequency of the excitation source increases, the hysteresis curve moves towards horizontal axis and lobe size decreases. The characteristics show linear I-V behavior as a resistor after 500 kHz frequency range. Figure 6 shows the stable behavior of input current and voltage at 1 kHz excitation

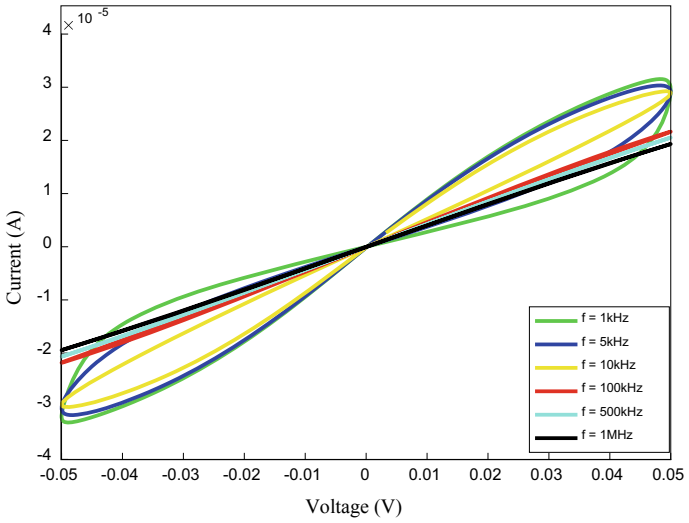

Fig. 5 V-I characteristics from proposed emulator circuit at different frequencies

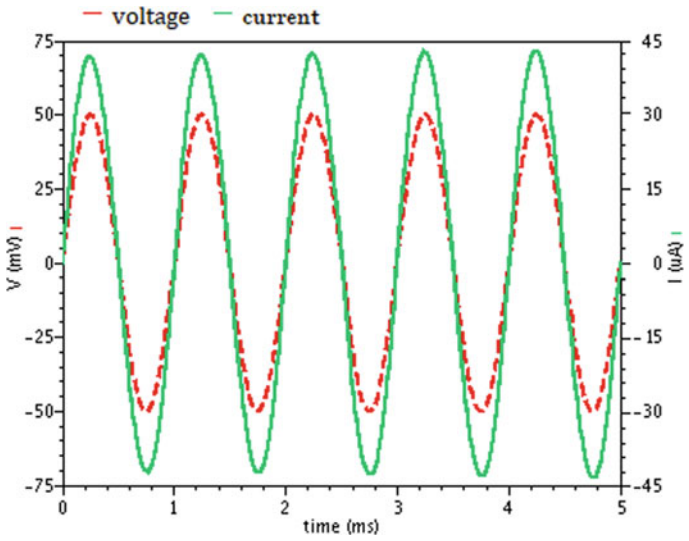

Fig. 6 Transient response of V-I at 1 kHz frequency

frequency. Figure 7 shows the transient response of memristance for the proposed emulator circuit with a sinusoidal input of 50 mV peak-to-peak and 1 kHz frequency.

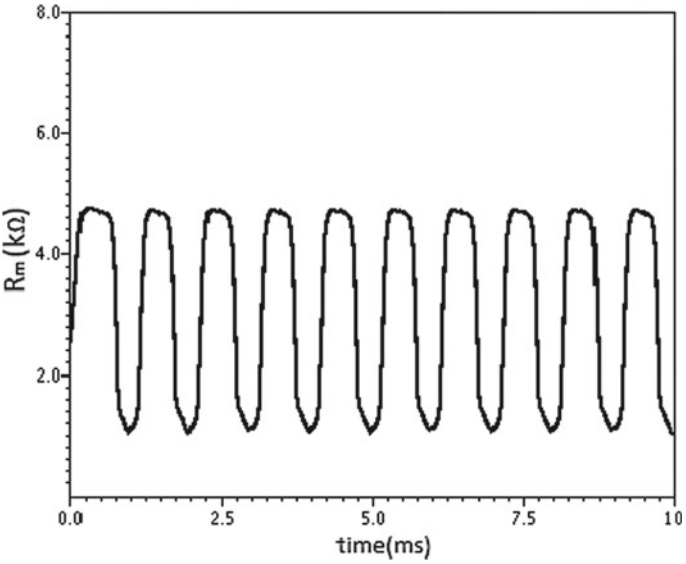

Fig. 7 Transient response of memristance with 50 mV sinusoidal excitation at 1 kHz frequency

5 Conclusion

A new VDTA based memristor (charge controlled) emulator circuit is proposed in this paper. The proposed circuit employs all the grounded circuital elements (three resistors, one capacitor), two VDTAs, and one voltage signal multiplier. The design is verified using Cadence virtuoso graphical tool using 180-nm CMOS technology node with ±0.9 V supply voltage. The non-volatile nature of the memristor has also been presented. From the simulation results, it is observed that maximum frequency of operation is 1 MHz and the frequency range can be increased by decreasing the capacitance values. The simulations presented here support the theoretical derivations thereby making it a robust and versatile emulator. Further, the tunability via varying the bias current overcomes the process mismatches that occur during fabrication.

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Vehicle Detection and Counting the Number of Vehicles for Intelligent Traffic Control Using LabVIEW—An Image Processing Approach

Prakash Majumder and Saurabh Chaudhury

Abstract Across the globe traffic lights are used to manage the vehicle movement on road. There have been many developments in this field but yet Static lights are used in most of the cases. With the rising number of vehicles on road there is a significant amount of congestion that leads to delay and many a times due to improper management may cause accidents. This problem thereby leads to a situation where need of a smart system that can efficiently handle traffic congestion is very prominent. This paper discusses about the implementation of various image processing methodology that can be used for detection and counting of vehicles. These methodologies help in counting of vehicles on road or at traffic junctions such that exact density of vehicles on each lane can be determined. The image processing methodologies like edge detection, background subtraction, and pattern matching algorithms has been implemented and tested using LabVIEW and Vision Assistant module. The headlights of the cars appear as a bright blob on captured images. Since the distance between the headlights of an vehicle are constant for a particular type of vehicle it can be used as an criteria for pattern matching and detection of vehicles specially after dusk. The detected vehicles gives the count of number of vehicle at halt on each lanes, depending upon which a suitable lane switching algorithm is implemented, where the most congested lane is most likely to be freed first. The real time monitoring system keeps track of vehicle count on each lane in real time and controls the traffic lights of the lanes such that waiting time can be minimized.

Keywords Image processing · Basic morphological processing · Edge detection · Background subtraction · Pattern matching · LabVIEW · Vision assistant module

P. Majumder (✉) · S. Chaudhury
Department of Electrical Engineering, National Institute of Technology Silchar, Silchar, Assam 788010, India
e-mail: Prakashm94@hotmail.com

S. Chaudhury
e-mail: saurabh@nits.ac.in

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1 Introduction

Knowledge of traffic density and count of vehicles on road is very essential nowadays for an effective traffic management. With extortionate rate of population growth in country like India, there has been a significant rise in vehicles on road. The inadequate and outdated infrastructures with the heavy volume of vehicles are causing irrational distribution at lanes leading to longer waiting time and accidents in some cases. Varying from country to country and regions 30–60% of traffic accidents occurs at the junctions and intersections. Therefore, it is a basic practice to monitor the vehicles on road mostly at intersections and junctions to implement an Intelligent Traffic Control System. For monitoring and detection purpose microwave radar system or inductive loops were commonly used in public roadways. These systems turned out to be cost inefficient due to need of frequent maintenance. Detection of vehicle and its type, using magnetic loop has been implemented in [1]. Real time image processing techniques and algorithms have brought a revolution in vehicle detection leading to a better traffic management system. Several modern image processing techniques have been discussed in [2–4]. Cheung et al. [5] presents a similar work that uses image processing to detect on-road vehicles and use WAKA neural network software for identification of the type of car. Traffic parameters like presence, vehicle count, density and speed, etc. of vehicles can be determined and utilized for generation of traffic signal to avoid blockage or accidents especially at the junctions. The exact count of vehicle would generate real time density data on each lane that can be used for proper control of traffic light switching. Proper traffic light switching will lead to lesser waiting time and avoid congestion at junctions. This paper is organized as follows. Firstly, basic morphological processes are applied for detection of vehicle from a live video. Next some advanced forms of image processing techniques are applied, such as edge detection, background subtraction and template matching has been implemented in LabVIEW interface for improvement in detection of the vehicles and its counting [6, 7]. Later from the collected count of vehicles, density of the vehicles has been calculated for each lane. This density data is feed to another algorithm where decision is taken which lane is too freed first. This data is then feed to an ATmega328P based Arduino UNO kit micro controller for switching of traffic lights.

LabVIEW is graphical programming software that allows for instrument control, data acquisition, and pre-/post-processing of acquired data. There would not be any need to write lines of coding since it provides a Graphical Programming Environment. To describe the program graphical symbols are used instead of textual languages. Big projects can be developed more efficiently in terms of manpower, time and money.

NI Vision Assistant module of LabVIEW provides step-by-step instructions for prototyping a vision application. Vision Assistant is a tool for prototyping and testing image processing applications. To prototype an image processing application, custom algorithms can be structured with the Vision Assistant scripting feature. The scripting feature records every step of the processing algorithm. After completing the algorithm, it can be tested on other images to check its credibility.

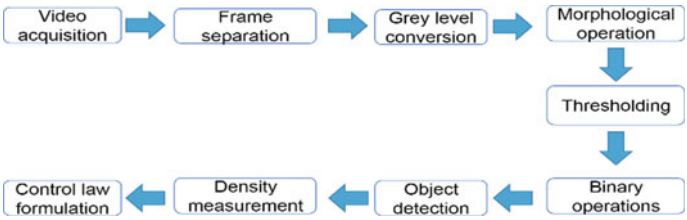

Fig. 1 Flow diagram of the overall process

2 Methodology—Application of Image Processing Techniques

The continuous video data from the cameras at a traffic intersection may have many disturbances in the form of people, shadows, pavements, poles etc. that causes error in detection of vehicles on road. Proper image processing techniques are needed to be applied for proper vehicle detection and count. Accurate identification of presence of vehicle will lead to better accuracy in density measurement. LabVIEW Vision Acquisition Software live video stream were separated into image frames. Image on each frame were converted to grayscale image. Using the Vision Assistant Module various morphological processes of image processing have been applied on each image frames. Further, the processed images were applied with threshold mask for extraction of specific objects (i.e., vehicles on road). Masking is the process of convoluting a mask over an image also called as filtering. Filtering can be classified in two broad classes of linear or smoothing filter and frequency domain filter. Followed by the frequency domain filtering (thresholding) some binary filtering were applied for removal of unwanted objects on each frames. A search area was then defined in which based on pixel count/density presence of an object is determined. A block diagram representation of implemented methodology for the work is shown in Fig. 1.

3 Simulation Results and Discussion

LabVIEW stands for Laboratory Virtual Instrument Engineering Workbench, provides a graphical programming platform that helps in easy implementation of required image processing techniques and its real time execution by testing on videos. This paper gives an insight of the image processing techniques that when implemented can detect and count cars in real time and generate density data on each lane. The techniques include edge detection method, background subtraction, frame differencing, blob analysis, template matching, etc.

Fig. 2 Detected cars after application of basic morphological processes

3.1 Basic Morphological Processing

As a primitive technique for detection of cars some basic morphological processing were applied. First the image obtained from Vision Acquisition Module had been converted into 8-bit grayscale image. Further in the process auto-median filter was applied over the image frames for removal of noise from the image then local thresholding (Background correlation) was applied. The auto-median filter spawns simpler particles that have lesser details, it uses a combination of two images to select the filtered image, where the first image is produced by removing bright pixels in dark regions and the second one is formed by removing dark pixels in brighter region. Local thresholding operation separate the object based on its pixel value. A comparison is made between a pixel values to its nearby pixels by applying a 3×3 mask. Threshold algorithm calculates local pixel intensity statistics such as range, variance, surface fitting parameters, or their logical combinations. A comparison between the intensity values for the pixel under consideration to its local threshold value is made and it is determined whether the pixel belongs to an object or the background. Small false objects (with low pixel area) are removed and objects with large pixel values are considered using binary filtration. Figure 2 shows the results of the operations on image frames.

3.2 Edge Detection Methodology

Generally an edge detection methodology involves a first order derivative of the input image, followed by convolution by an adapted mask. This mask generates a gradient of the image from which edges are detected by thresholding. Most classical operators like Sobel, Prewitt, and Robert explained in paper [5] are first order derivative operators. These operators are also called as gradient operators. The gradient operator detects edges by searching for maximum and minimum of the intensity values. The operator examines the distribution pattern of intensity values in the neighborhood of a selected pixel and determines if the pixel is to be considered as an edge. For detection of cars edge detection masks are applied over each image with the help of Vision assistant tool box. The type of mask depends mainly upon the parameters like brightness of the subject to be detected correlated to its background. For detection

Fig. 3 Detected cars after application of edge threshold algorithm

of vehicle in this case a local average mask of size (3×3) is applied for removal of noises. Then Sobel operator (3×3) has been applied over the image for detection of edges. Sobel filter is a high-pass filter that takes out the outer contours of the object. Significant variations of the light intensity along the vertical and horizontal axes are highlighted. Then a threshold algorithm was applied such that for each threshold, a value determined by the surfaces representing the initial gray scale is calculated. The smallest value is considered as optimal threshold value. Depending upon which the size small objects are removed and a rectangular box is created across the objects with greater pixel numbers with the co-ordinate extraction feature of LabVIEW. Figure 3 shows the raw image after the operations along the detected object form the real video stream.

3.3 Background Subtraction

Bakoglu and Meindl [2] have presented a comparative study between the existing background modeling and foreground detection techniques. A comparison between ViBe, SOBS, and PBAS techniques has been presented. Alpert et al. [3] has presented an algorithm based on Bayes method of classification between background and foreground. The algorithm updates the selected reference background with an infinite impulse response. The philosophy for background subtraction method is to utilize the difference between two consecutive frames or a few image frames for target detection. Following steps has been followed for detection of vehicles on road: firstly, the difference between the n and $n - 1$ frame is calculated in the video/image sequence by fixing an image with no cars on road (empty road) as the basic image to be subtracted. Later, a threshold was selected that transforms the difference image into binary values. As pixel value of the processed image crosses the given threshold, the pixel is treated as foreground pixel, rests of the pixels are considered as background pixel. To eliminate the hollow pixel, connectivity between the foreground pixels is performed. A size threshold was then set based on which when pixels of the connected area is greater compared to threshold size, a moving object was considered to be detected. Figure 4 shows the results of the detected vehicles from a video sequence.

Fig. 4 Detection and counting of cars after application of background subtraction

The direct differential of the adjoining frame often contains a lot of noises, splits and parts. Therefore, we can perform some post-processing in order to ascertain the accuracy in the detection. The brightness of the image is first adjusted followed by that a local averaging mask (5×5) was applied for smoothing. Then a Laplacian mask (5×5) was applied for detection of edges. Thresholding operation using Inter-class variance is applied. An optimal threshold is determined by maximizing the between-class variation with respect to the threshold. Objects large pixel areas were considered to be vehicles on the road.

3.4 Blob Analysis and Template Matching

Due to low lighting condition at night it is very tough to apply any method for detection of cars. During night the vehicles have their headlights turned ON. These headlights appear as blob on the image. A specific variety of vehicle generally has similar spacing between the two head lights. So this information can be applied for matching template for detection of vehicle on the road. The Vision Assistant produces co-ordinate information regarding the location and size of matched template. The co-ordinate information on the image frame helps in tracking the object. An overview on template matching techniques has been presented in [8].

The brightness of the image frames from the Vision Acquisition blocks are adjusted to highlight the blobs created from car headlights. Then a pattern was selected and saved in the template matching module. The pattern selection procedure can be seen in Fig. 5.

Depending upon the spacing between two headlights a few number of the templates were selected the results after implementation of the methodology can be seen in Fig. 6.

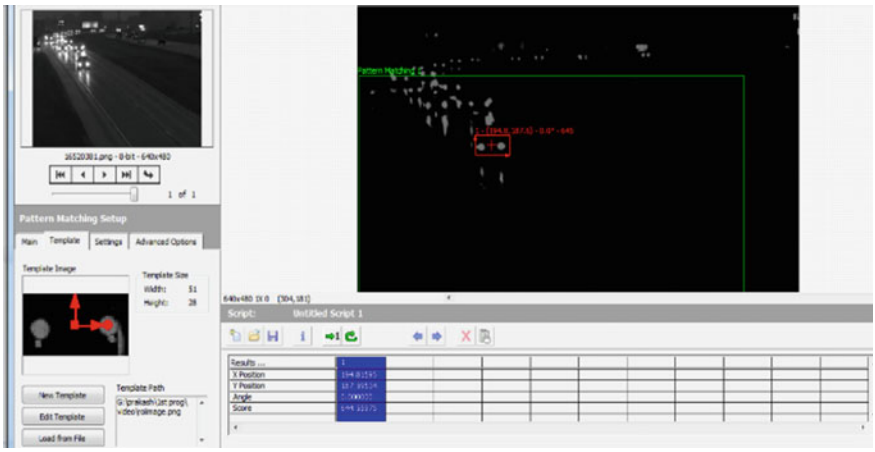

Fig. 5 Selection of template for a detection of cars on road

Fig. 6 Results showing detection of vehicle based on matched template

4 Implementation of Traffic Control Methodology

The vehicle count generated after processing the images assists the traffic light switching. The proposed method produces exact count of standstill vehicles at each junction [9]. The lane with highest number of vehicles at stand still is given the priority. The vehicle detection and counting algorithm passes the real time vehicle count form each lane. The algorithm finds the lane with highest number of vehicles at halt and produces a sequential yellow (10 s) followed by green (30 s). The algorithm keeps track of the count in real time whenever the count of the other lane reaches the highest the respective lane is set free. In case of equal number of count in two lanes the consecutive lanes are freed one after another. A block diagram representation of the proposed algorithm is presented in Fig. 7.

The states of the traffic light are named as A, B, C and D. The denotation for A, B, C and are derived from Table 1 as given. A donates the states of the traffic lights

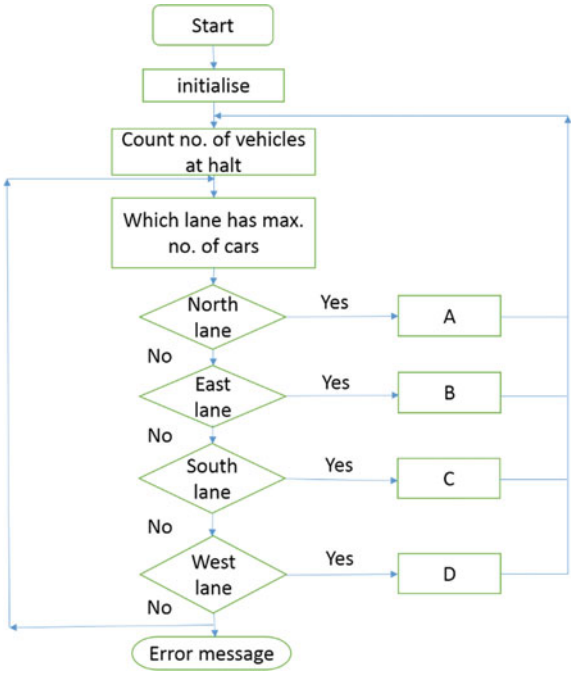

Fig. 7 Proposed algorithm for traffic light switching

Table 1 States of the traffic light for various lanes

Lane	R	Y	G	R	Y	G	R	Y	G	R	Y	G
A (North)	0	1	0	1	0	0	1	0	0	1	0	0
	0	0	1	1	0	0	1	0	0	1	0	0
B (East)	1	0	0	0	1	0	1	0	0	1	0	0
	1	0	0	0	0	1	1	0	0	1	0	0
C (South)	1	0	0	1	0	0	0	1	0	1	0	0
	1	0	0	1	0	0	0	0	1	1	0	0
D (West)	1	0	0	1	0	0	1	0	0	0	1	0
	1	0	0	1	0	0	1	0	0	0	0	0

when North lane is set free and so on for the other states. Among the two states of North lane the first states denotes the transition stage, where for 10 s yellow light is ON. Latter state denotes the 30 s of green light. The algorithm has been implemented in such a way that if the same lane has the highest vehicle count the yellow light transition is skipped and 30 s more is added to the same lane.

Applying the edge detection methodology the vehicles were detected. The count of vehicles detected in each lane is feed to an array, with dimension 1×4. Each

element of the array represents the count generated from each lane. This array is feed to another VI file where the maximum value in the array gives the index number. The index number generates a switch case, depending upon which the lighting sequence of is followed. For the interfacing with the hardware module an extension is included named LINX by Makerhub [10]. LINX open was used to open the connection to the hardware module form the desired COM port. COM 4 was selected and set as a constant for every operation. LINX write N-channel function block takes two inputs. The first input is the digital port number where the data needed to passed. The second input node takes input as an 1-D array where the present states of the LEDs were supplied. LINX close was used to close the connection after finishing an operation. A feedback node was used to implement the operation of shift register. A shift register stores data from previous execution and updates new data after each a loop cycle. The shift register was initialized with the data from the first sequence block of flat sequence. The data gets updated after the delay time of the first sequence gets over.

To implement the lighting sequence RYB Boolean LEDs were selected. To implement on four lane 12 Boolean LEDs were selected and local reference were created for each LED. These local references were given True/False control inputs based on their sequence and states as show in Table 1.

The hardware module takes 9 s to start receiving data from the software module. Figure 8, shows the yellow light transition for the WEST lane, whereas Fig. 9, shows 30 s green light for the same lane. The rest of the lanes are set to RED condition for first 30 s after a 30 s mark recalculated results for number of vehicle on each lane was determined based on which some other lane was set for 30 s green.

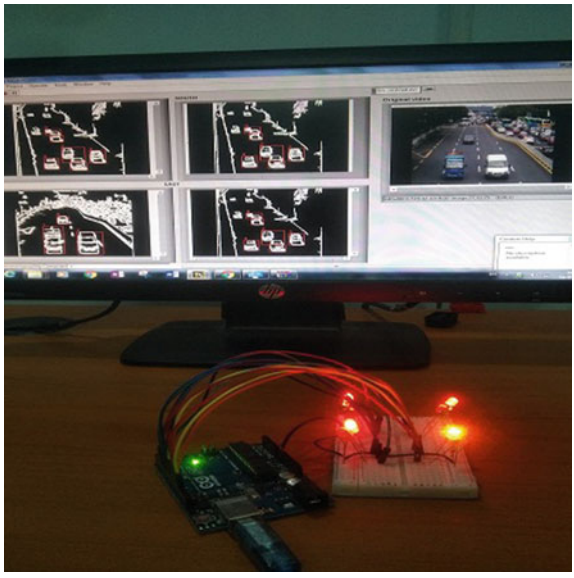

Fig. 8 Results showing 10 s yellow light for WEST lane

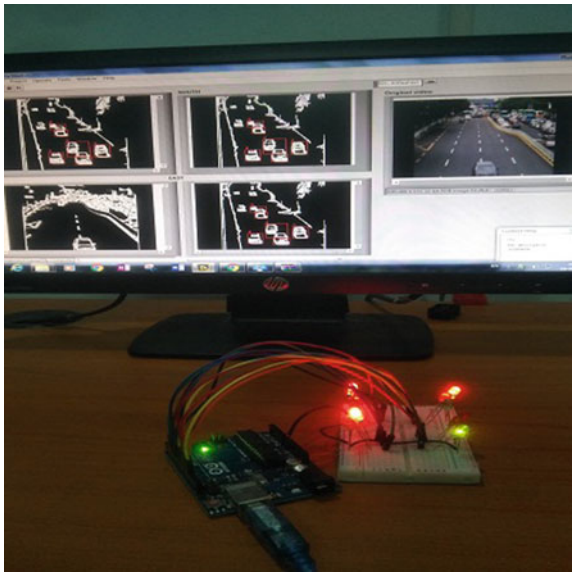

Fig. 9 Results showing 30 s green light for WEST lane

5 Conclusion

The main objective behind the paper is to design a dynamic time traffic light controller which takes into account the real time traffic scenario. The major challenge was to get an exact count of number of vehicles on road. To overcome this problem image processing methodologies were employed. Basic morphological processes, Edge based detection technique and subsequent frame difference techniques were employed to detect the vehicles. Edge based detection technique proved to be more accurate among these methodologies. To extend the scope of the project template matching technique was employed for detection of vehicles at night. Templates of blob obtained from the headlights of vehicles were used for the detection purpose. Template matching technique proves to work properly for detection of vehicles but some erroneous results were obtained due to improper alignment of vehicle. This error can be minimized by using neural network training of various blobs generated by different types of vehicles.

The second stage of the paper contains the process to design an algorithm that uses the real time vehicle count to assign proper time slot to the lanes with higher vehicle count. The designed algorithm uses a sequential yellow and green light pattern for lanes with higher vehicle count. The algorithm takes real time data generated from the vehicle detection algorithm and gives preference to the lane with higher vehicle count. The algorithm proves to work sufficiently well for all the cases. In case if the lane with highest vehicle count repeats after a cycle of 30 s. The algorithm efficiently identifies such case and keeps the green light ON again for next 30 s. This is to be taken as a note that the 10 s (yellow) and 30 s (green) timings were selected just

for testing purpose. The timer values can be changed depending upon the need at various locations around the globe. This is another field where modifications can be involved. Fuzzy rules can be applied to determine the sequence timings based on the density of vehicles at a location. The vehicle detection algorithms not only takes count of the vehicles stationary at the junction but also counts the number of moving vehicle from a junction at a period of time. This data can be utilized to assign timing cycles to the sequences. For example, for a location with high vehicle density the yellow light timing can be minimized to 5–8 s whereas green light timings can be increased to 60 s/cycle. Fuzzy logic based rule base can prove very efficient in decision making for such conditions.

Finally it can be said that the implemented methodologies can successfully detect and count the vehicles on road, and can generate a dynamic timing sequence of the traffic lights. The dynamic timing sequence will aid toward smoother and faster traffic flow and road clearance. The transitions between switching lanes were taken care of to avoid accidental hazards and chaos. Further improvements can be done in both detection and decision making algorithms to end up with more sophisticated results.

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Performance Analysis of Color Image Watermarking with Lifting Scheme

Mahendra Kumar Pandey, Girish Parmar, and Afzal Sikander

Abstract To prevent the illegal copying and sharing of digital content, the need for security for digital data is highly demanded. Among various available techniques, digital watermarking is an effective solution to protect confidential data. This paper presents the performance analysis of color image watermarking based on lifting scheme in which color image watermark has been used. Peak signal-to-noise ratio (PSNR), Structural similarity (SSIM) index and normalized correlation coefficient (NCC), etc. have been used as fidelity parameters to test the effectiveness of presented work both quantitatively and qualitatively.

Keywords Image watermarking · Copyright · Lifting scheme · PSNR · Structural similarity (SSIM) index · NCC

1 Introduction

Need for trusted and highly secured copyright protection techniques for digital data is highly required in recent years due to rapid development in internet technology. Among existing techniques and due to excellent features, the digital watermarking is an effective solution to protect multimedia data in various fields. Digital watermarking technique implants a watermark by slightly modifying the data of host image without noticeable changes [1]. An effective watermarking technique must satisfy the properties of transparency, robustness, security, and complexity. Generally, image watermarking is divided in two subcategories; spatial and transform domain [2]. The

M. K. Pandey · G. Parmar
Department of Electronics Engineering, Rajasthan Technical University, Kota, Rajasthan 324010, India
e-mail: mahendra2003in@yahoo.co.in

G. Parmar
e-mail: girish_parmar2002@yahoo.com

A. Sikander (✉)
Department of Instrumentation and Control Engineering, Dr. B. R. Ambedkar National Institute of Technology, Jalandhar, Punjab 144011, India
e-mail: afzal.sikander@hotmail.com

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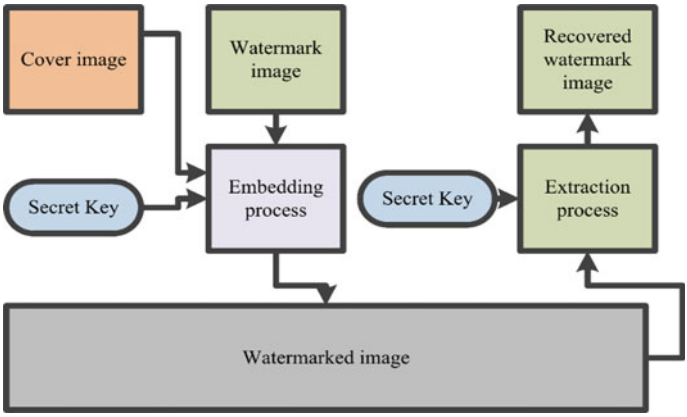


Fig. 1 A generic diagram of digital watermarking

use of spatial or frequency domain based watermarking depends on a particular application. In the spatial domain, watermark can be inserted via directly modifying the pixels. While in the frequency domain, the watermark can be embedded via changing the coefficients. In literature, it has been found that the transformed based frequency domain watermarking techniques are more efficient in terms of imperceptibility and robustness [3] (Fig. 1).

Numerous transform-based frequency domain techniques such as Discrete Wavelet Transform (DWT), Discrete Cosine Transform and Stationary Wavelet Transform, etc. are available [4]. To decompose an image in hierarchical order, DWT is a popularly used technique that decomposes an image using filters with downsampling into its sub-bands. Downsampling rejects certain information which is not important. Hence, due to this, some shift in the recovered image is found which produces inaccurate recovery of image. To resolve this associated problem with DWT, the lifting scheme based watermarking in combination with singular value decomposition (SVD) has been presented here.

The rest of the paper is organized as follows: Sect. 2 describes the methodologies and security. The implementation of the watermarking technique has been presented in Sect. 3; whereas Sect. 4 provides the experimental results with observation. Comparative performance analysis with other existing techniques has been explained in Sect. 5. Finally, the concluding remarks have been given in Sect. 6.

2 Preliminaries

2.1 Overview of Lifting Scheme

To build wavelet completely in spatial domain, lifting scheme was proposed in the year 1999 by Sweldens [5]. Lifting scheme consists of three main stages [6]:

- Split
- Primal Lifting or Predict
- Dual Lifting or Update.

The lifting scheme has the following benefits over other wavelets:

1. It requires less memory.
2. It is much faster than DWT due to floating-point coefficients of the wavelet transform.
3. It provides the lossless recovery of an image.
4. It does not require temporary arrays in the calculation steps.

2.2 Overview of SVD

To indicate the intrinsic properties, an image ($n \times n$) can be decomposed into its components which are expressed as

$$C = U_c S_c V^T \tag{1}$$

where U_c and V_c are the orthogonal $n \times n$ matrix having left-handed singular and right-hand singular vectors. S_c is a diagonal $n \times n$ matrix having nonnegative singular values arranged in descending order [7]. When small changes occur in singular values of an image, it produces an unnoticeable change in the original image.

2.3 Security

To enhance the robustness and security features of the watermarking technique, image scrambling, and descrambling using Arnold transform with N iteration have been used [8]. Here, the number of iterations will act as a security key which is required for the exact recovery of an image (Fig. 2).

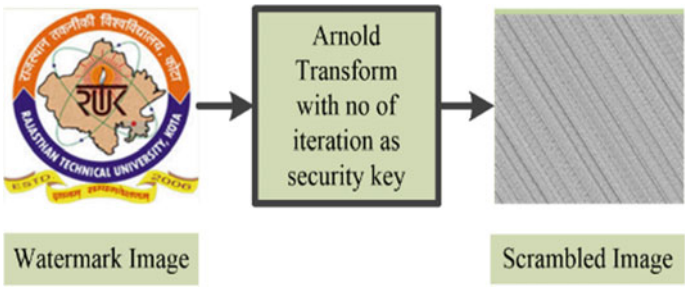


Fig. 2 Scrambling process

3 Implementation of Watermarking Technique

The implementation of watermarking technique can be done with two main processes; embedding and extraction as shown in Figs. 3 and 4.

3.1 Embedding Process

During the embedding process, first of all, choose the images for pre-processing prior to embedding the watermark image. In image pre-processing, images are transformed into YCbCr color space. After transformation, Arnold transformation based image scrambling has been applied on watermark image to enhance robustness and security. By applying the following steps shown in Fig. 3, watermarked image has been constructed.

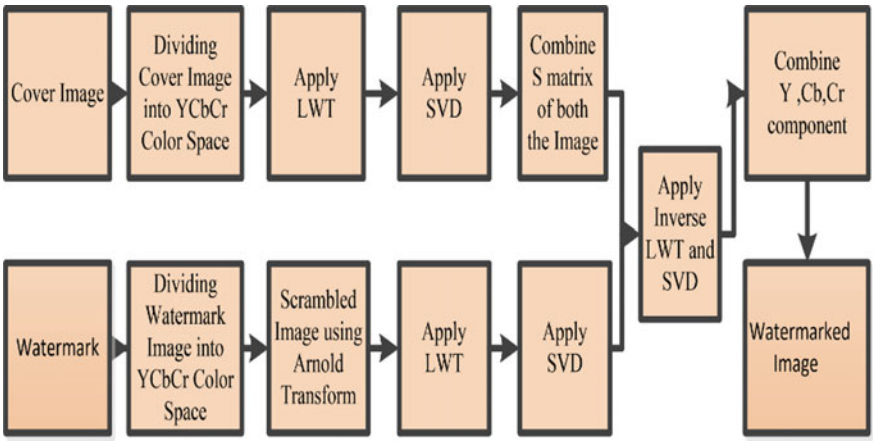


Fig. 3 Embedding process

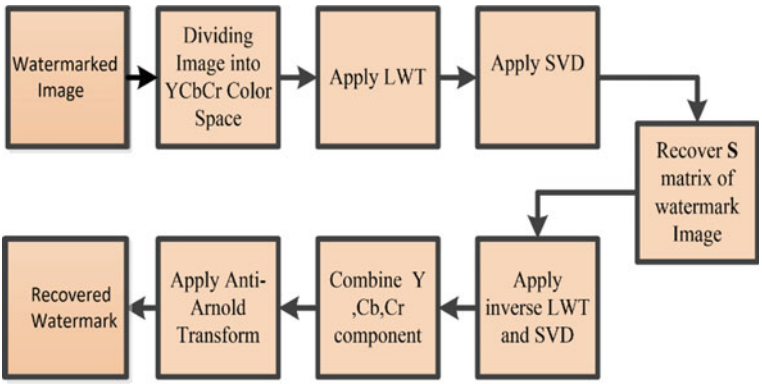


Fig. 4 Extraction process

3.2 Extraction Process

To extract the hidden/secret data from watermarked image via extraction process, first of all, watermarked image is transformed into YCbCr color space and then LWT-SVD operation is applied to it. Recovery of watermark image is done by applying the inverse process with security key on the recovered S matrix as shown in Fig. 4.

4 Results and Discussions

In this section, for the comparative analysis of watermarking technique, RGB color images namely; Lena, RTU logo images (24-bit) are taken from USC-SIPI image database [9] and fidelity parameters have been calculated (Fig. 5).

4.1 Evaluation of Fidelity Parameters

- **Peak signal-to-noise ratio (PSNR)**

For measurement of imperceptibility, PSNR in dB is given by:

$$\text{MSE} = \frac{1}{NM} \sum_{i=1}^{N} \sum_{j=1}^{M} (f_c(i, j) - f_{\text{wm}}(i, j)) \tag{2}$$

$$\text{PSNR} = 10 \log_{10} \frac{f_c^2(i, j)}{\text{MSE}} \tag{3}$$

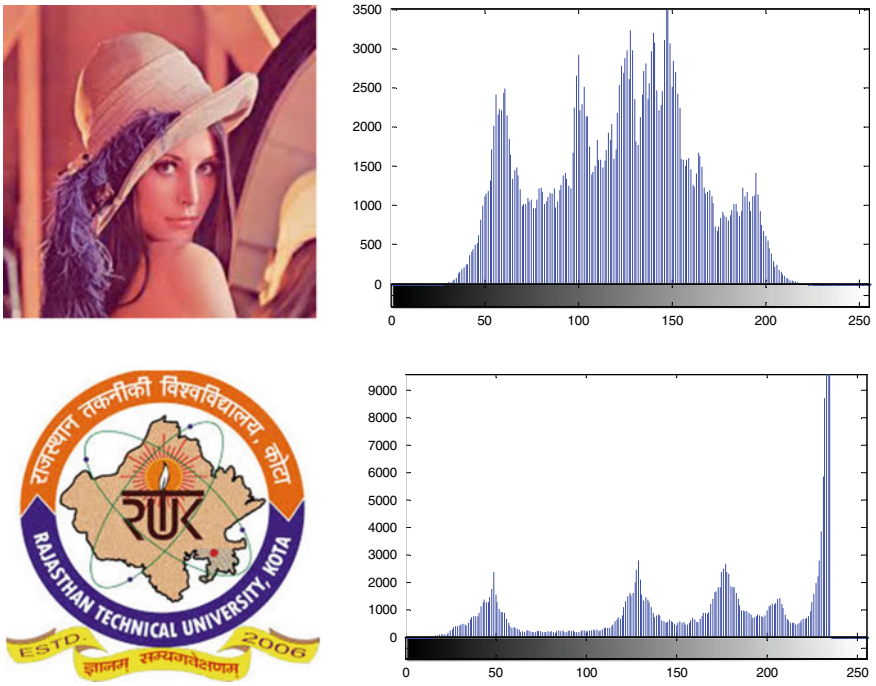


Fig. 5 Test images with histogram

where $f_c^2(i, j)$ indicates the peak brightness value of pixel and f_c, f_{wm} represent the brightness of host and watermarked images at different pixels values.

- **Normalized correlation coefficient (NCC)**

To check the robustness and image quality, the value of normalized correlation coefficient (NCC) is measured by

$$\mathrm{NCC} = \frac{\sum_{i=1}^{N}\sum_{j=1}^{M} g_w(i, j) * g'_w(i, j)}{\sqrt{\sum_{i=1}^{N}\sum_{j=1}^{M} g_w^2(i, j)}\sqrt{\sum_{i=1}^{N}\sum_{j=1}^{M} g_w^2(i, j)}} \tag{4}$$

where g_w and g'_w are the brightness level of original and extracted watermark at different values of pixel [10].

Table 1 Fidelity parameters

S.F.	Proposed scheme		
α	PSNR	SSIM	NCC
0.01	42.71	0.9989	0.9981
0.015	39.02	0.9985	0.9989
0.02	36.38	0.9981	0.9992
0.025	34.33	0.9976	0.9993
0.03	32.67	0.9969	0.9993
0.05	28.07	0.9963	0.9991
0.10	22.03	0.9775	0.9970
1	6.7	0.4102	0.6989

4.2 Simulation Results

Simulation results on MATLAB platform with lifting scheme based watermarking technique in terms of fidelity parameters have been presented by considering Lena and RTU Logo as a host and watermark image respectively.

It has been concluded from the simulation results presented in Table 1 that the fidelity parameter highly depends upon the scaling factor as shown in Figs. 6, 7 and 8. For different values of scaling factors, presented work yields good values of PSNR and SSIM at an acceptable level. It is also found that the robustness of presented work at different scaling factors is also up to the mark and in acceptable range as shown in Table 1.

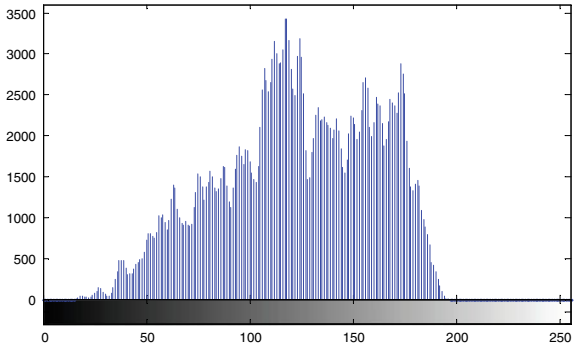


Fig. 6 Histogram of Watermarked image

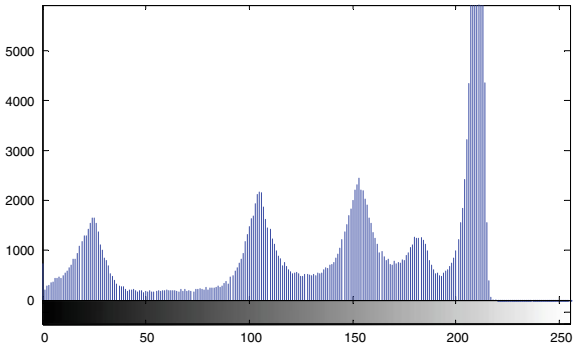


Fig. 7 Histogram of recovered RTU logo

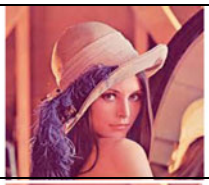
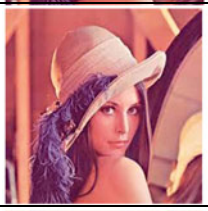
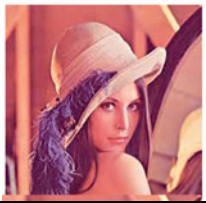
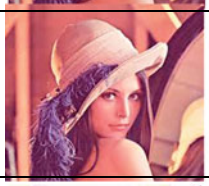
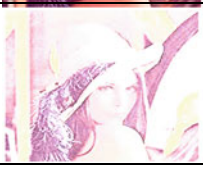
S.F.	Watermarked image	Recoverd watermark image
0.015		
0.03		
0.05		
0.10		
1.0		

Fig. 8 Watermarked and recovered watermark image

Table 2 Comparison of imperceptibility

Watermarked image	Watermark	Proposed	Ref. [11]	Ref. [12]
Lena	RTU logo	39.02	35.92	36.74

Table 3 Comparison of average subjective equality

Watermarked image	Watermark	Proposed	Ref. [11]	Ref. [12]
Lena	RTU logo	5	5	5

5 Comparative Performance Analysis with Other Existing Techniques

Comparative performance analysis of presented work with other existing techniques has also been carried out on the basis of imperceptibility and average subjective equality.

From simulated results given in Tables 2 and 3, it can be concluded that lifting scheme based watermarking technique is more efficient, fast, and capable of lossless recovery of image with effective payload capacity in comparison to other available techniques. It is also observed from subjective equality point of view that lifting scheme based technique also yields good results and is capable to resolve problems encountered in DWT based methods.

6 Conclusions

The performance analysis of lifting scheme based watermarking has been presented. From the simulated results obtained in MATLAB platform, it can be concluded that lifting scheme based image watermarking gives better results in terms of execution speed, memory requirement, and lossless recovery of data. It is also concluded that lifting scheme based watermarking yields better results in terms of fidelity parameters for copyright protection. From the simulated results, it too can be summarized that the presented scheme is easy to implement, more efficient, and reversible with data hiding capabilities to satisfy the requirements of human vision system (HVS).

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Design of Reconfigurable Antenna with RF-MEMS for Satellite Applications

B. V. S. Sailaja and Ketavath Kumar Naik

Abstract This paper presents the design and simulation of a reconfigurable MEMS antenna. The elliptical-shaped patch antenna is presented. The nonuniform meandered MEMS switch is embedded on to the patch. The circular CSRR is etched on to the elliptical patch. The proposed antenna resonates at 10.46 GHz return loss of −37.6 dB used for satellite applications. The MEMS switch is having low actuation voltage 7.9 V. The proposed MEMS switch actuates under two conditions (ON and OFF) states. When the switch is ON state, the proposed antenna resonates at 10.57 GHz return loss of -30 dB. Similarly, when the switch is in OFF state it resonates at 10.53 GHz return loss of −47.6 dB. The isolation of the proposed switch shows better performance is used to validate the switch behaviour. The obtained insertion and return losses are minimum. The reconfiguration frequency is observed for different conditions of the reconfigurable elliptical patch antenna. The impedance matching is presented for the antenna and the switch. The frequency reconfigurable MEMS antenna is used for satellite applications.

Keywords Reconfigurability · CSRR · RF-MEMS · Elliptical-shaped patch antenna

1 Introduction

The reconfigurable antennas with multiple frequency bands for commercial applications are most convincing for transmitting and receiving different frequency applications. In the design of reconfigurable antennas, slot antennas are considered as building blocks, these are considered for ultra-high frequency [1, 2]. Reconfigurable patch antennas are additionally intended to work in both *L* and *X*-frequency bands [3]. The frequency reconfigurable antennas are having lower in size and cost compared to the traditional antennas. Generally, reconfigurability of an antenna is acquired by varying the frequency of operation, improving the radiation patterns.

B. V. S. Sailaja · K. K. Naik (✉)
Department of Electronics and Communication Engineering, KLEF (Deemed to be University), Vaddeswaram, Guntur 522502, India
e-mail: drkumarkn@hotmail.com

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The reconfigurable antenna governs the resonating frequency of the antenna and assists to resonate at different frequency bands. Variable solutions are available for matching networks among them impedance matching network is the best possible solution is used to estimate the characteristic impedance of the device [4, 5]. MEMS switches offer better performance compared to the traditional RF devices. Most of the RF-MEMS devices are available in the market among them switches are used on to the patch antennas to yield better results and the interference can be reduced by introducing switches on to the patch antennas [6–15]. The gain improvement is presented with circular patch antennas, CPW-fed on patch for enhancement of bandwidth is proposed on [13–15].

In this work, reconfigurable elliptical-shaped mems antenna is presented. The MEMS switch is actuated only when the actuating voltage is applied. The reconfigurability in terms of frequency is obtained. The impedance matching is presented for the antenna and the switch. The return loss and the radiation patterns are presented for different conditions and the analysis of the switch is presented below.

2 Antenna Design

The Fr-4 substrate material (ε_r is 4.4, $h = 1{,}6$ mm) is considered for designing of the proposed antenna. The close view of the antenna is presented in Fig. 1. The proposed switch consists of gold material and silicon nitride as dielectric.

A circular-shaped CSRR slot is etched on to the elliptical patch. The switch is integrated on to the patch. The reconfigurable antenna with MEMS switch is

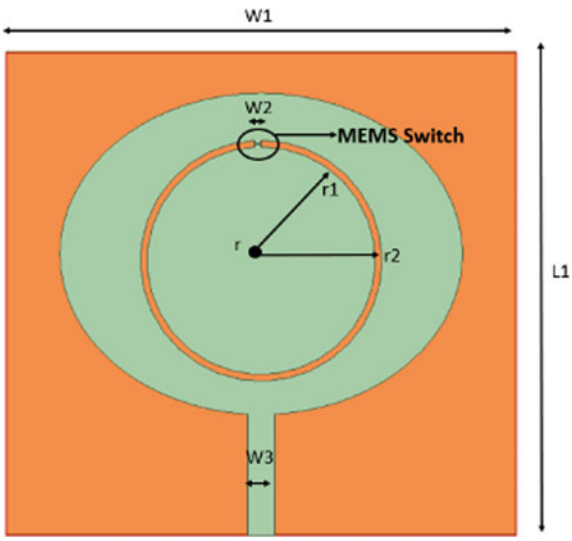

Fig. 1 The proposed antenna with RF-MEMS switch

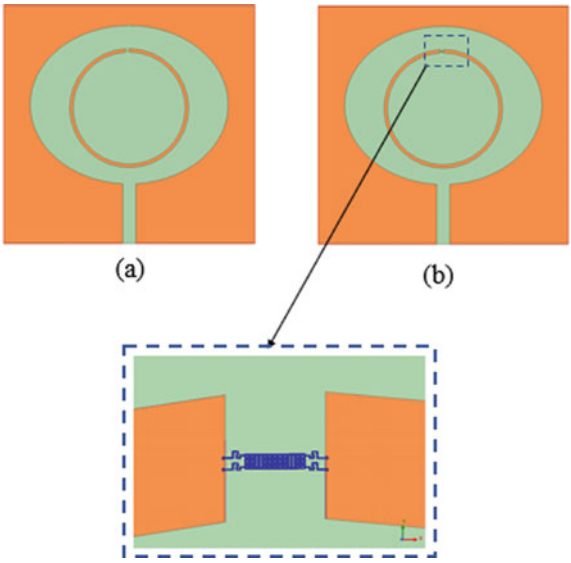

Fig. 2 The proposed antenna. **a** Having no switch, **b** having with switch

presented in Fig. 2. Here, $W_1 = 38$, $W_2 = 0.5$, $W_3 = 2$, $L_1 = 36$, $r_1 = 8$, $r_2 = 9$ all the units are considered in mm.

3 Results and Discussions

The proposed antenna is designed and analysis is carried out with HFSS simulation. Figure 3 represents the simulated return loss of the proposed antennas model.

Reflection Loss

Reflection loss is characterized as the measure of power loss caused by reflection of power at a line interruption. It is communicated in terms of decibels (dB) and the return loss is conveyed in Eq. (1).

$$R_{\mathrm{L}}(\mathrm{dB}) = -20 \log 10(\tau) \tag{1}$$

where τ is the reflection loss of proposed antenna

The return loss of the proposed elliptical structured patch antenna and the other two conditions sustained with MEMS switch ON and OFF state are shown in Fig. 3. The reconfigurability can be observed in the figure at different conditions of the switch. The proposed antenna exhibits maximum reflection loss at antenna with switch in OFF state.

To ensure the proper matching the input impedance should meet the focal point of the smith chart. If the input impedance is away from it the condition mentioned

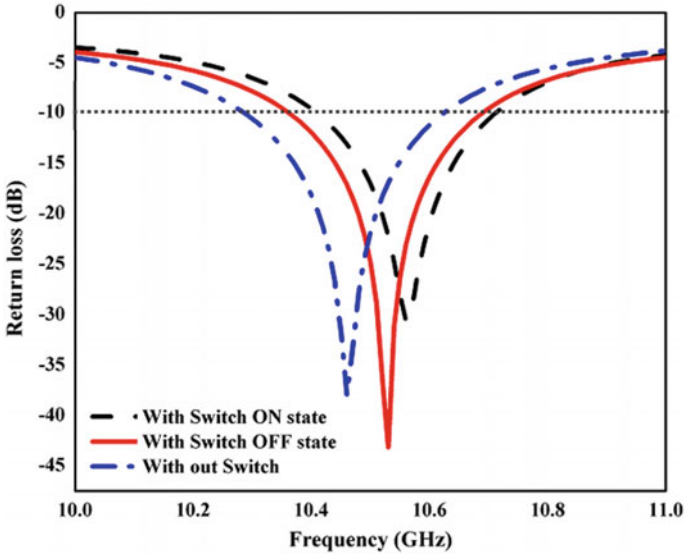

Fig. 3 The reflection loss of the proposed antenna

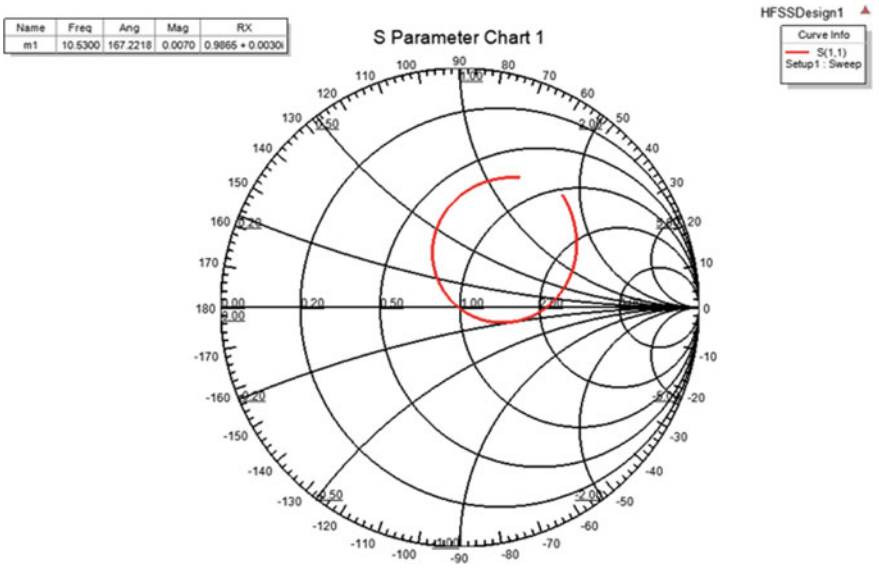

Fig. 4 Impedance matching of the proposed antenna in smith chart

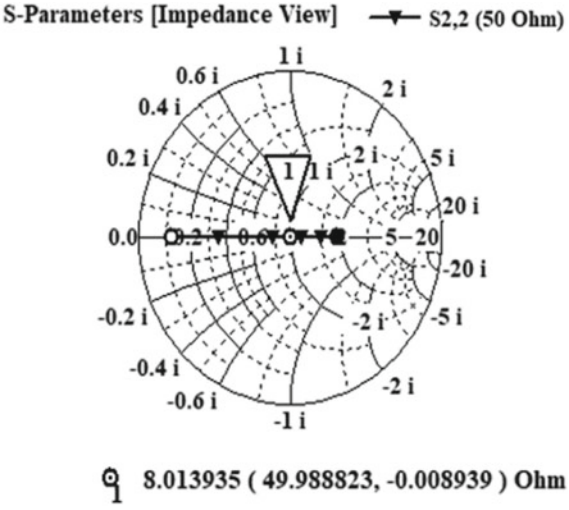

Fig. 5 The impedance matching network of the proposed switch in smith chart

above will not be satisfied. The impedance ought to be considered is 50 Ω. Figures 4 and 5 represent the matching technique antenna and the switch, respectively.

Radiation Patterns

The elliptical-shaped antenna (ESPA) is presented for various far-field conditions. The radiation patterns of the proposed antenna at $\varphi = 0$, $\varphi = 90$, and the outlines for these conditions are observed when the switch is ON and OFF states, it is represented in Figs. 6, 7 and 8, respectively.

MEMS Switch Performance Analysis

The performance analysis of the switch is presented here. The proposed switch is validated with isolation performance and the return loss and insertion loss of the switch. The isolation is observed at 8 GHz@−76 dB is shown in Fig. 9. The return loss and the insertion loss of the proposed switch is −75 and −0.07 dB at 8 GHz frequency respectively is shown in Fig. 10.

4 Conclusions

In this paper, an elliptical-shaped reconfigurable patch antenna with MEMS switch is presented. The proposed switch with nonuniform meanders is used to reduce the actuating voltage. The elliptical patch is etched with CSRR. The proposed antenna resonates at two conditions of the switch. The reconfigurability in frequency is observed. The proposed antenna is used for satellite applications.

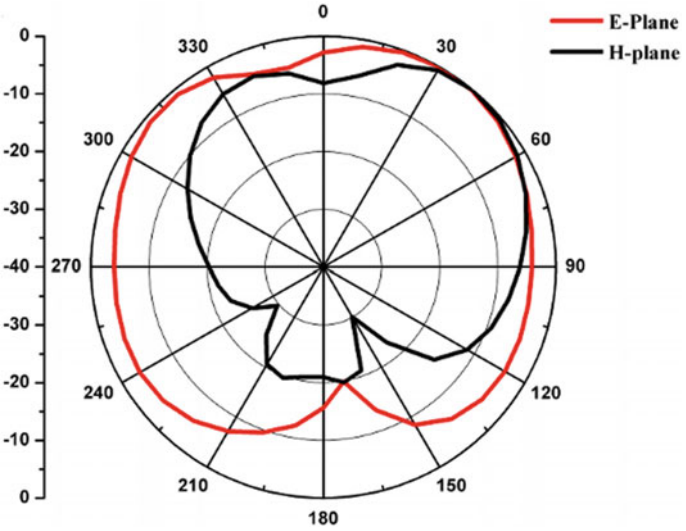

Fig. 6 Patterns of the proposed elliptical-shaped antenna

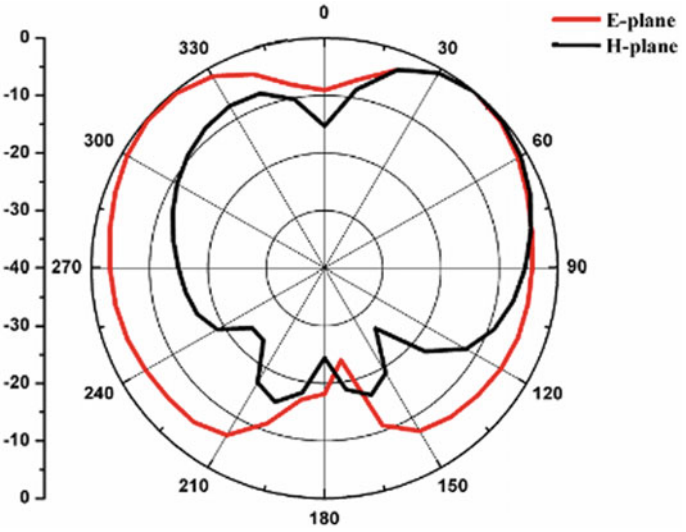

Fig. 7 Patterns of the proposed elliptical-shaped antenna with switch in ON state

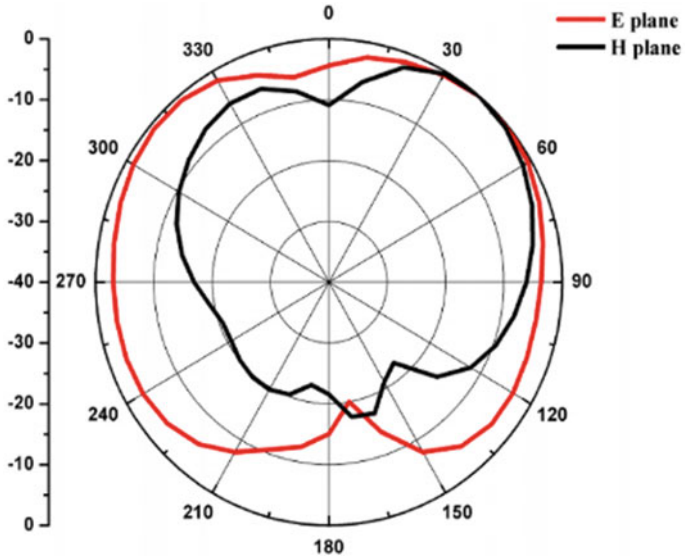

Fig. 8 Patterns of the proposed elliptical-shaped antenna with switch in OFF state

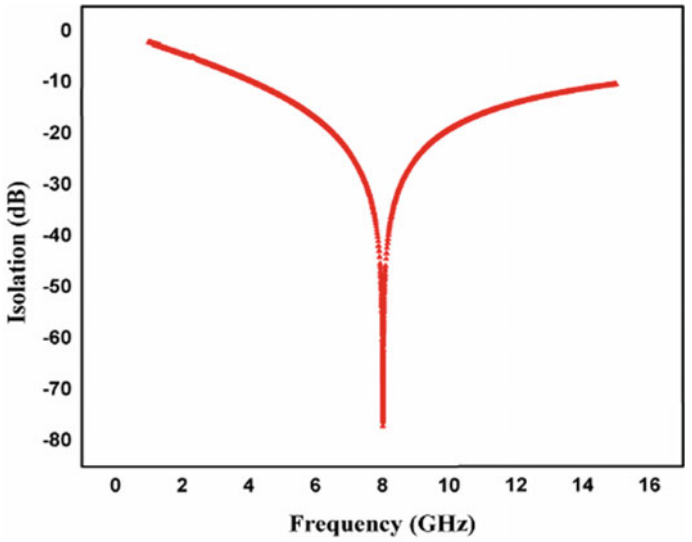

Fig. 9 The isolation performance of the switch

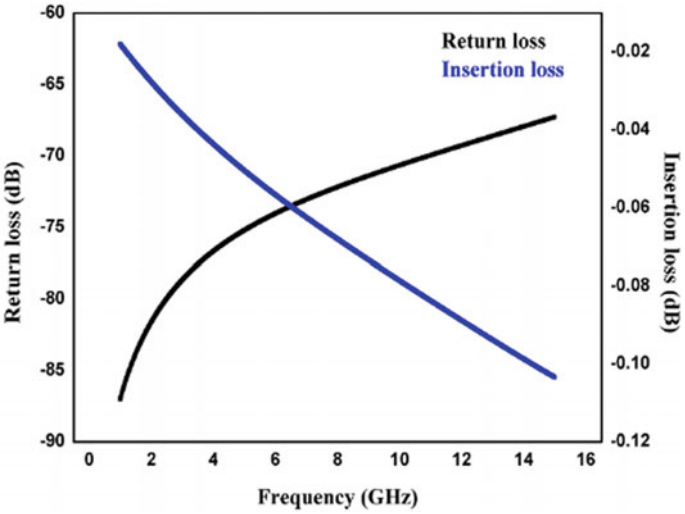

Fig. 10 The return loss and the insertion loss of the proposed switch

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Design of Fractional-Order Low-Pass and High-Pass Filter

Vikash Kumar and Aminul Islam

Abstract This paper presents an electronically tunable current-mode fractional-order filter based on voltage differencing transconductance amplifier (VDTA) as an active element. Two-filter realizations i.e., low-pass and high-pass filter have been implemented in the paper. The configuration uses two fractional capacitors of non-integer order α and β, where $0 < \alpha, \beta < 1$. The circuit has the added advantage of providing electronically tunability of cut-off frequency (ω_0) and Q-factor (Q). The suggested filter is analyzed using Virtuoso Analog design Environment of Cadence.

Keywords Voltage differencing transconductance amplifier · Fractional-order · Current mode · Low-pass filter · High-pass filter

1 Introduction

Electronic filters circuits perform signal processing and hence find applications in almost all communication systems. High-pass filters attenuates the signal higher than cut-off frequency and low-pass filters attenuates the signals below cut-off frequency. Active filter employs active components for circuit implementation and hence in this paper, voltage differencing transconductance amplifier (VDTA) for the proposed filter design [1]. VDTA is known for its versatility and flexibility of operation. Further, VDTA provides electronic controllability by adjusting the external dc bias current.

Fractional-order systems are defined using fractional-order differential equations. Research work in fractional-order filters is developing because it provides an extra degree of flexibility and opportunity of scaling effect on frequency, which leads to better designing of filter. Fractional-order filters employs fractance device or a

V. Kumar
Department of Electronics and Communication Engineering, Presidency University, Bangalore, KA 560064, India
e-mail: vikashkumar@ieee.org

A. Islam (✉)
Department of Electronics and Communication Engineering, BIT, Mesra, Ranchi, Jharkhand, India
e-mail: aminulislam@bitmesra.ac.in

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fractional-order element that has the properties of fractional-order impedance [2]. There are various approximations for studying the characteristics of a fractance device. Some of them include continued fraction approximation (CFE) [3], Carlson approximation [4] etc. Fractional-order systems unlike to the integer order counterpart, have unlimited memory as they are infinite dimensional and hence are a better model for the real life circuit design. In addition, the increasing use of fractional-order filters, especially in the fields of biotechnology and neurosciences is leading to further exploration and researches in the implementation and modeling of fractional-order systems. This paper proposes a multiple input single output (MISO) high-pass and low-pass filter response employing VDTA and using two fractional capacitors.

2 Voltage Differencing Transconductance Amplifier (VDTA)

The modern active element, VDTA (Voltage differencing transconductance amplifier), has been recommended by Biolek in 2008 [5]. Several applications of VDTA have been reported, notably the filters [6] and oscillators [7]. VDTA is a two-stage amplifier that contains two Arbel-Goldminz transconductances (g_{mf} and g_{mf}). The first stage transforms the differential voltages from input ports "p" and "n" into output current at intermediate port "z" with first transconductance (g_{mf}). While, the second stage transforms the voltage at intermediate port "z" into output currents at output ports "x^-" and "x^+" with second transconductance (g_{ms}). The block-level representation of VDTA showing the associated port voltages and currents is depicted in Fig. 1. The relation between the port voltages and currents of VDTA is expressed as [8]

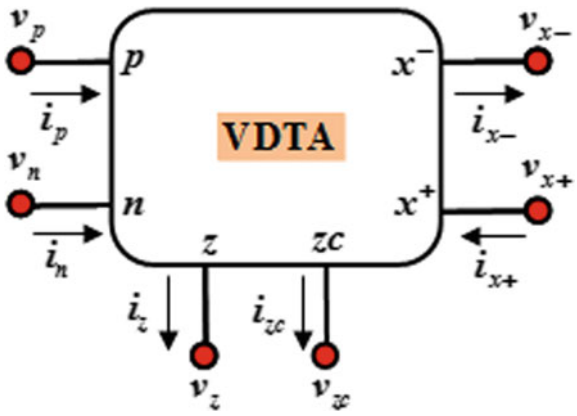

Fig. 1 Block-level representation of VDTA

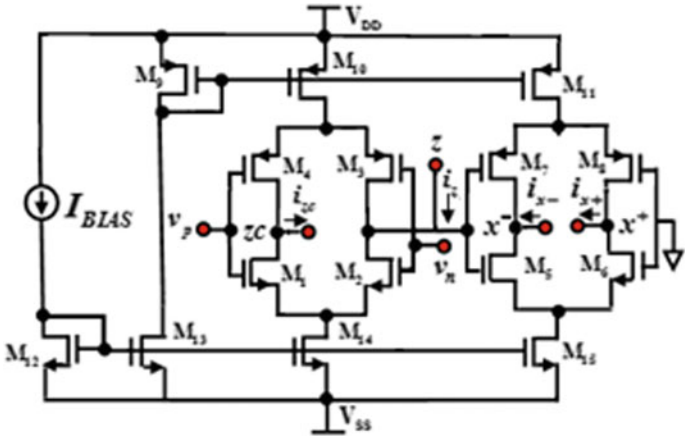

Fig. 2 Transistor-level representation of VDTA

$$\begin{bmatrix} i_z \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} g_{mf} & -g_{mf} & 0 \\ 0 & 0 & g_{ms} \\ 0 & 0 & -g_{ms} \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix}, \tag{1}$$

where the Arbel-Goldminz transconductances (g_{mf} and g_{ms}) are defined as

$$g_{\text{mf}} = \frac{g_1 g_2}{g_1 + g_2} + \frac{g_3 g_4}{g_3 + g_4}, \tag{2}$$

$$g_{\text{ms}} = \frac{g_5 g_6}{g_5 + g_6} + \frac{g_7 g_8}{g_7 + g_8}, \tag{3}$$

where

$$g_j = \sqrt{\mu C_{\text{ox}} (W/L)_j I_{\text{bias}}} \tag{4}$$

is the transconductance and $(W/L)_j$ is the aspect ratio of jth MOS transistor. The value of j varies from 1 to 6. μ is effective carrier mobility; C_{ox} is the oxide capacitance and I_{bias} is external DC bias current of VDTA. The transistor level diagram of VDTA is shown in Fig. 2 [9].

3 Fractional-Order Element (FOE)

The impedance of a fractional-order element is defined as $Z(s) = \alpha s^{\alpha}$ where α is defined as the order of the fractional-order element [10] and takes the value as $-1, 0,$ 1 for capacitance, resistance and inductance respectively. An important factor about

a fractional-order element is that the magnitude function of the impedance function is dependent on the frequency but the phase value is constant with frequency and changes only with the value of the fractional order, α. Hence also termed as constant phase element. Since there is no commercial fractional-order element available at present, so the element can be realized using high-order RC or RLC networks. The biggest advantage of fractional-order elements (FOEs) is that it increases the range for obtaining responses in fractional domain, other than only integer order subset.

4 Proposed Filter Configuration

The proposed filter configuration is shown in Fig. 3. The proposed circuit represents a current-mode multiple input single output (MISO) filter, which contains two grounded capacitors which have been replaced by fractional-order capacitors of impedance, $Z(s) = 1/s^{\alpha}C$. To select the model for fractional capacitor Carlson's method is used. This method leads to the approximation of fractional Laplacian operator that can be realized using RC ladder networks. The approximated RC ladder network is shown in Fig. 4.

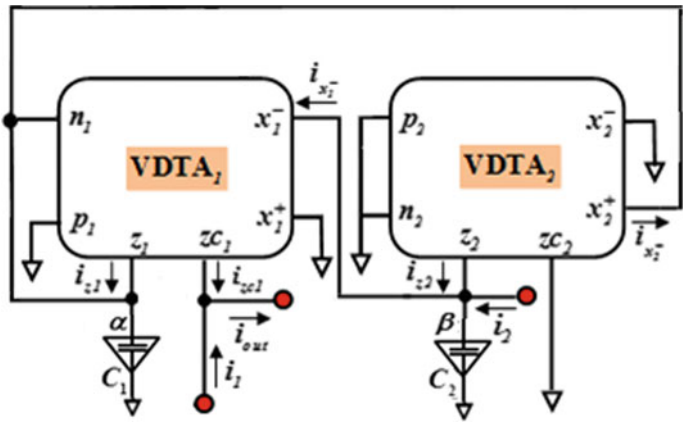

Fig. 3 Proposed filter configuration

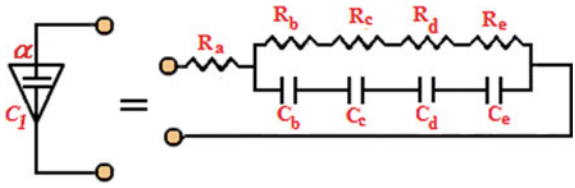

Fig. 4 RC ladder network to realize 4th order approximated fractional Laplacian operator

In order to compare the performance of fractional-order filter with traditional filter, the transfer functions of both types of filters are evaluated. For traditional filters with standard capacitors (C_1, C_2), i.e., $\alpha = \beta = 1$, the configuration shown in Fig. 3 provides low-pass and high-pass filtering functions on giving particular inputs.

1. If $i_1 = 0$, and $i_2 = i_{\text{in}}$ is the input current, and $i_{\text{out}} = i_{\text{LPF}}$, then transfer function of current-mode low-pass filter (LPF) response is obtained as

$$\frac{i_{\text{LPF}}}{i_{\text{in}}} = \frac{g_{\text{mf1}} g_{\text{ms2}}}{s^2 C_1 C_2 + s C_2 g_{\text{mf1}} + g_{\text{ms1}} g_{\text{ms2}}}. \tag{5}$$

2. If $i_1 = i_2 = i_{\text{in}}$ is the input current, and $i_{\text{out}} = i_{\text{HPF}}$ then transfer function of current-mode high-pass filter (HPF) response is obtained as

$$\frac{i_{\text{HPF}}}{i_{\text{in}}} = \frac{g_{\text{mf1}} g_{\text{ms2}}}{s^2 C_1 C_2 + s C_2 g_{\text{mf1}} + g_{\text{ms1}} g_{\text{ms2}}}. \tag{6}$$

For fractional-order filter, standard capacitors are replaced by fractional-order capacitors (i.e., $0 < \alpha, \beta < 1$) with impedances $Z_{C_1} = \frac{1}{s^\alpha C_1}$ and $Z_{C_2} = \frac{1}{s^\beta C_2}$. On putting these impedance values the modified fractional-order low-pass filter (FLPF) and fractional-order high-pass filter (FHP) transfer functions are as follows:

$$T_{\text{FLPF}} = \frac{i_{\text{FLPF}}}{i_{\text{in}}} = \frac{g_{\text{mf1}} g_{\text{ms2}} / C_1 C_2}{s^{\alpha+\beta} C_1 C_2 + s^\beta g_{\text{mf1}} C_2 + g_{\text{ms1}} g_{\text{ms2}}} \tag{7}$$

$$T_{\text{FHPF}} = \frac{i_{\text{FHPF}}}{i_{\text{in}}} = \frac{s^{\alpha+\beta} C_1 C_2}{s^{\alpha+\beta} C_1 C_2 + s^\beta C_2 g_{\text{mf1}} + g_{\text{ms1}} g_{\text{ms2}}} \tag{8}$$

The magnitude and phase response of the fractional low-pass filter is

$$|T_{\text{FLP}}| = \left|\frac{i_{\text{LP}}}{i_{\text{in}}}\right| = \frac{\frac{g_{\text{mf1}} g_{\text{ms2}}}{C_1 C_2}}{\sqrt{\begin{array}{l} 2 g_{\text{ms1}} g_{\text{ms2}} \cos\left(\frac{(\alpha+\beta)\pi}{2}\right) \omega^{\alpha+\beta} \\ +2 \frac{g_{\text{ms1}} g_{\text{ms1}}}{C_1 C_2} \frac{g_{mf1}}{C_1} \cos\left(\frac{\beta\pi}{2}\right) \omega^{\beta} \\ +2 \frac{g_{\text{mf1}}}{C_2} \cos\left(\frac{\alpha\pi}{2}\right) \omega^{\alpha+2\beta} + \left(\frac{g_{\text{mf1}}}{C_1}\right)^2 \omega^{2\beta} \\ +\left(\frac{g_{\text{mf1}} g_{ms1}}{C_1 C_2}\right)^2 + \omega^{2(\alpha+\beta)} \end{array}}} \tag{9}$$

$$\underline{|T_{\text{LPF}}} = \underline{\left|\frac{i_{\text{LP}}}{i_{\text{in}}}\right|} = \tan^{-1}\left(\frac{\omega^{\alpha+\beta} \sin\left(\frac{(\alpha+\beta)\pi}{2}\right) + g_{\text{mf1}} C_2 \omega^\beta \sin\left(\frac{\beta\pi}{2}\right)}{\omega^{\alpha+\beta} \cos\left(\frac{(\alpha+\beta)\pi}{2}\right) + g_{\text{mf1}} C_2 \omega^\beta \cos\left(\frac{\beta\pi}{2}\right) + g_{\text{ms1}} g_{\text{ms2}}}\right) \tag{10}$$

The magnitude and phase response of the fractional high-pass filter is

$$|T_{\mathrm{HLP}}| = \left|\frac{i_{\mathrm{HP}}}{i_{\mathrm{in}}}\right| = \frac{\omega^{\alpha+\beta}}{\sqrt{\begin{array}{l} 2g_{\mathrm{ms1}}g_{\mathrm{ms2}}\cos\left(\frac{(\alpha+\beta)\pi}{2}\right)\omega^{\alpha+\beta} \\ +2\frac{g_{\mathrm{ms1}}g_{\mathrm{ms2}}}{C_1C_2}\frac{g_{\mathrm{mf1}}}{C_1}\cos\left(\frac{\beta\pi}{2}\right)\omega^{\beta}+\left(\frac{g_{\mathrm{mf1}}}{C_1}\right)^2\omega^{2\beta} \\ +2\frac{g_{\mathrm{mf1}}}{C_2}\cos\left(\frac{\alpha\pi}{2}\right)\omega^{\alpha+2\beta}+\left(\frac{g_{\mathrm{mf1}}g_{\mathrm{ms1}}}{C_1C_2}\right)^2+\omega^{2(\alpha+\beta)} \end{array}}} \tag{11}$$

$$\underline{|T_{\mathrm{HPF}}} = \underline{\left|\frac{i_{\mathrm{HP}}}{i_{\mathrm{in}}}\right.} = \tan^{-1}\left(\frac{s^{\alpha+\beta}\sin\left(\frac{(\alpha+\beta)\pi}{2}\right)+g_{\mathrm{mf}}C_2s^{\beta}\sin\left(\frac{\beta\pi}{2}\right)}{s^{\alpha+\beta}\cos\left(\frac{(\alpha+\beta)\pi}{2}\right)+g_{\mathrm{mf}}C_2s^{\beta}\cos\left(\frac{\beta\pi}{2}\right)+g_{\mathrm{ms1}}g_{\mathrm{ms2}}}\right) \tag{12}$$

5 Results and Discussions

To justify the theoretical analysis of the proposed filters discussed in the previous section, the filters are designed and simulated in Virtuoso Analog design Environment of Cadence at CMOS 45-nm CMOS process node. The traditional low-pass filter (LPF) and high-pass filter (HPF) with standard capacitors are designed for order $\alpha = \beta = 1$, i.e., 2. The fractional-order low-pass filter (FLPF) and high-pass filter (FHPF) are designed for order $\alpha = 1$ and $\beta = 0.5$, i.e., 1.5. The current-mode gain responses of both filers are shown in Figs. 5 and 6 respectively. The total consumption with and without using a fractional capacitor is 1.08mW.

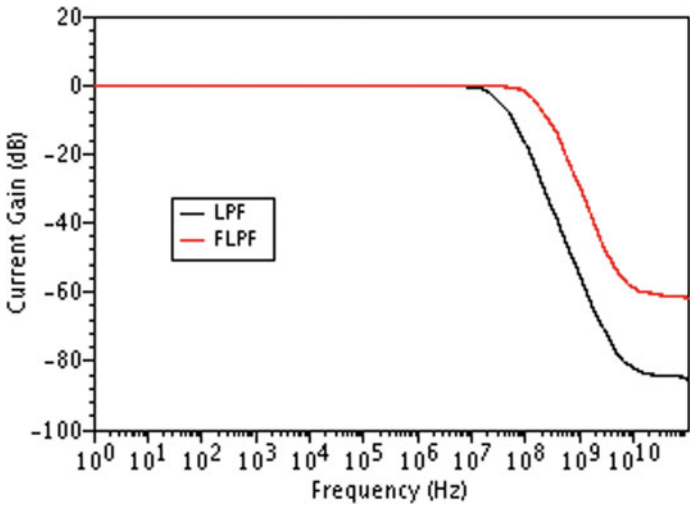

Fig. 5 Gain response of current-mode traditional low-pass filter (LPF) and fractional-order low-pass filter (FLPF)

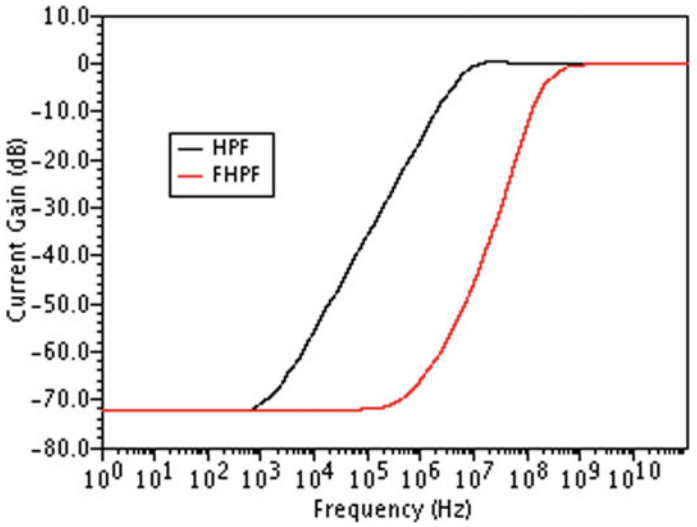

Fig. 6 Gain response of current-mode traditional high-pass filter (HPF) and fractional-order high-pass filter (FHPF)

6 Conclusion

This paper presents an electronically tunable fractional-order current-mode filter design using a two VDTA and two fractional capacitors. The proposed circuit realizes LPF and HPF configurations. The proposed structure includes two fractional capacitors of the order α and β, respectively. Simulation results have been carried out to characterize fractional capacitors of order 1.5 ($\alpha = 1, \beta = 0.5$). The fractional-order filters have the added advantage of frequency scaling.

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VLSI Implementation of Adiabatic Logic-Based 4 × 4 Multiplier for Low Power Applications

Dinesh Kumar and Manoj Kumar

Abstract Very large scale integrated circuits are the backbone of modern semiconductor industry to fulfill the need of high speed and low power electronic systems. High speed data processors consist of arithmetic logic units and multiplier is a major part of these logic units. In this paper, a high speed low power 4 × 4 multiplier has been implemented using an adiabatic logic-based full adder. The proposed design of multiplier consumes a power of 0.018 μW as compared to 1.78 μW double pass transistor with asynchronous adiabatic logic-based multiplier reported in literature with a frequency of 100 MHz. The performance of proposed design has been verified at varying voltage supply and temperature conditions. The simulated results show that the proposed architecture of multiplier is a better option for low power VLSI circuits.

Keywords Arithmetic logic unit · CMOS · Multiplier · Power delay product

1 Introduction

With the exponential increase in demand of portable and automatic electronic systems in modern electronic industry prolonged battery life becomes a prime concern for researchers. To prolong the battery life with high speed operation, researcher's investigating hybrid and new technologies for low power VLSI circuits. All high speed digital signal processing units and modern electronics systems need arithmetic logic units. These units consist of high speed adders and multipliers, which is responsible for a substantial part of power dissipation in circuits. There are various multipliers which are reported in literature to achieve high performance. Complementary pass transistor logic-based multiplier has been reported in [1]. Makoto Suzuki et al. presented a double pass transistor logic-based ALU in [2] where as a pass transistor-based multiplier has been reported in [3]. Some new techniques which have been used for the implementation of multiplier have been reported in [4–7]. Some techniques

D. Kumar (✉) · M. Kumar
USICT, GGSIP University Delhi, New Delhi, India
e-mail: dinesh4saini@gmail.com

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perform better in terms of power dissipation and some have high speed operation with some limitation such as drive capability and logic swing. With the increasing limitations of technology nodes, due to reduction in the future size of complementary metal-oxide semiconductor (CMOS) devices, researchers are exploring new techniques of power reduction. One of the prominent techniques is adiabatic logic which can reduce the power requirements of modern electronics circuits. In this paper, the author has presented a multiplier with adiabatic logic-based full adder [8].

1.1 Fundamentals of Adiabatic Logic

The term adiabatic is a Greek word which means "impassable" it fundamentally belongs to thermodynamic. According to adiabatic logic, there is no heat transfer in or out in a system ideally. In case of low power electronics, it is used in reference with charge stored at capacitive nodes. There should not be any loss or gain of charge in a circuit ideally, in low power circuits, it is used to recover the stored charge or to feedback the stored charge to main power supply. In case of a CMOS inverter, circuit CV_{dd}^2 energy is consumed. The output node capacitance stores $1/2CV_{dd}^2$ and rest $1/2CV_{dd}^2$ energy is dissipated in the form of heat by the resistance of PMOS in ON state during charging of output node capacitance. Conventionally, $1/2CV_{dd}^2$ energy will go to the ground via pull down network (NMOS) and wasted away during discharging. Whereas adiabatic logic circuits try to recover this energy and feedback to the power supply which eventually reduces the power dissipation. The energy dissipation reduction can also be achieved by using the time-varying supply *RC* circuit as shown in Fig. 1.

Where C is the capacitance of output node which is charged through an pull up (PMOS) network. And R represents the resistance of pull up network in ON state and the capacitance C is charged with the help of constant current $I(t)$ source as compared to a fixed voltage V_{dd} in conventional CMOS inverter. The voltage across capacitor is given by $V_c(t)$, if the capacitor is discharged initially, then the voltage is given by the following expression.

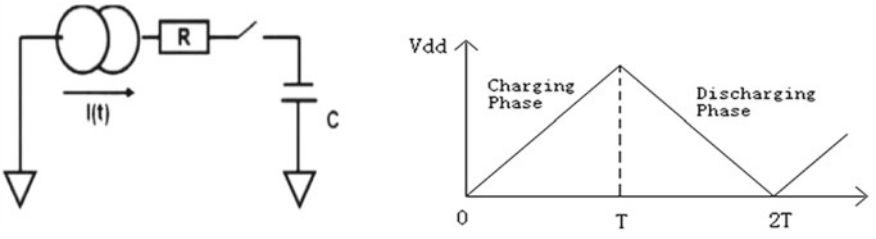

Fig. 1 Adiabatic charging

$$V_c(t) = \frac{1}{C} i(t) * t \tag{1}$$

and

$$i(t) = C \frac{V_c(t)}{t} \tag{2}$$

The dissipated energy can be evaluated by the following equation.

$$E_{\text{diss}} = R \int_0^T i^2(t) \mathrm{d}t = R i^2(t) * T = \frac{RC}{T} C V_c^2(T) \tag{3}$$

where $V_c(T)$ is the output node capacitance voltage at time T. It is depicted from (3) that the energy consumption decreases as compared to traditional charging at V_{dd} supply voltage, when $T > 2RC$. The energy dissipation can be reduced by keeping large value of T appropriately, i.e., by using a slowly time-varying voltage supply. The energy loss can be minimized by using the value of R appropriately. In this paper, a adiabatic logic-based full adder has been used in multiplier which is reported in [8]. This adder used two complementary time-varying supply and energy is recovered which reduces the power dissipation significantly.

1.2 Multiplier Architecture and Its Functionality

Multiplier fundamentally does the multiplication of bits and results are used in various applications in arithmetic logic units and digital signal processing applications (filtering, Fourier transformations, etc.). There are different types of multiplier which are reported in literature. And broadly they can be classified in accordance with type of word accessing [9], in first type words are accessed are serially in which operands are entered serially one by one. However, the required chip area is small for the operation but the speed of such circuits becomes a limitation. In second type, all the inputs take place simultaneously same time and delay time is very small with fast operation but the area required on the chip increased. In third type, the combination of serial and parallel is used in this the circuit has advantages of both serial and parallel with reasonable limitations. In this paper, a 4×4 combinational multiplier has been used which consist of gates, half adders and full adders. For a $N \times N$ bit multiplication the output result will be in 2 N bits. Multiplication of binary numbers requires adders for summation. Let the two numbers of four bit each are A3, A2, A1, A0 (1010) and B3, B2, B1, B0 (1011) then the final product must be P7, P6, P5, P4, P3, P2, P1, P0 (01101110). This multiplication can be understood with the help of an example as given below.

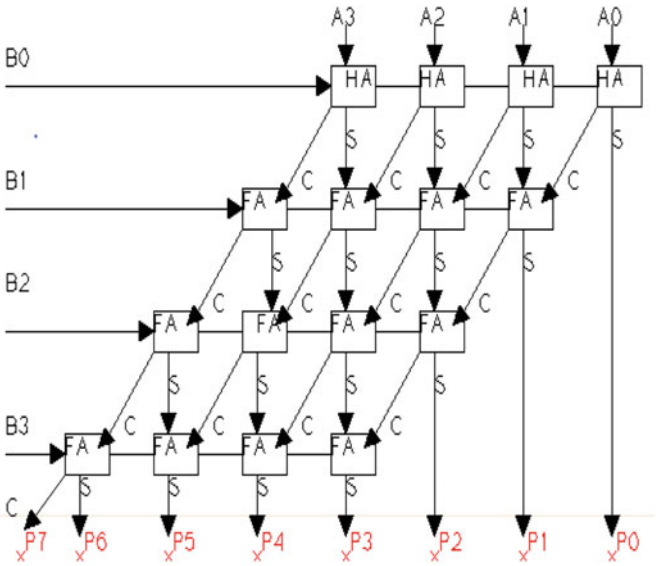

Fig. 2 Architecture of 4 × 4 multiplier

$$
\begin{array}{r}
1010\textbf{(10)} \\
\underline{\times\ 1011\textbf{(11)}} \\
1010 \\
1010 \\
0000 \\
\underline{1010\qquad\quad .} \\
\underline{01101110\ \textbf{(110)}}
\end{array}
$$

Block diagram of a 4 × 4 multiplier is given in Fig. 2 and the blocks consist of some AND gate with half adders and full adders. Adders add the partial product terms (A0 × B0, A1 × B1, etc.) and sum and carry propagates as shown in diagram to give final product in terms (P0—P7).

2 Proposed Work and Result Considerations

In this work, all the results are simulated on 0.18 μm CMOS technology. The proposed design of multiplier is based on the full adder given in Fig. 3. Each block of full adder consists of adiabatic logic-based full adder cell.

The results design in terms of power and delay has been obtained at varying temperature condition 10–50 °C and with a supply voltage range of 1.2–2.4 V and given in Tables 1 and 2, respectively. The power efficiency (PDP) has been calculated

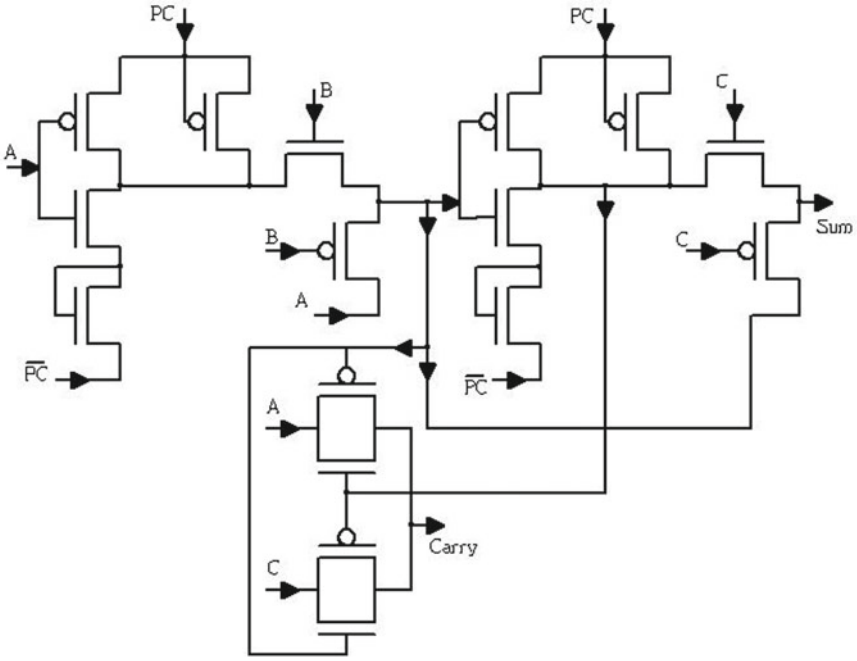

Fig. 3 2PASCL-based full adder [8]

Table 1 Power and delay results with varying temperature

Temperature (°C)	Power (nW)	Delay (μS)	PDP (pJ × 10^{-4})
15	17.63	16.02	28.24
20	17.89	16.81	30.07
25	18.45	17.18	31.69
30	19.58	17.74	34.73
35	20.69	18.11	37.46
40	20.95	19.42	40.68
45	23.46	20.30	47.62
50	25.49	21.79	55.54

and analyzed at varying supply voltage and temperature conditions. The power delay product shows the better performance of proposed design at varying temperature and voltage conditions. The results of new architecture have been compared with the existing results of some architectures reported in literature in Table 3 (Figs. 4 and 5).

Table 2 Power and delay results with varying voltage

Supply voltage (V)	Power nW)	Delay (μS)	PDP (pJ × 10^{-4})
1.2	7.69	8.34	6.41
1.3	9.42	9.64	9.08
1.4	10.68	10.27	10.96
1.5	12.49	14.93	18.64
1.6	14.89	15.30	22.78
1.7	16.75	16.36	27.40
1.8	18.67	17.37	32.42
1.9	20.98	19.87	41.68
2.0	23.65	21.92	51.84
2.1	26.26	26.80	70.32
2.2	28.87	27.94	80.66
2.3	31.28	31.34	98.03
2.4	34.59	35.04	121.20

Table 3 Comparison with existing designs

Technology (μm)	Power (μW)	Design
0.5	0.12	Domino logic [10]
0.18	2.74	CMOS logic [7]
0.18	1.75	DPTAAL [7]
0.18	0.018	Proposed

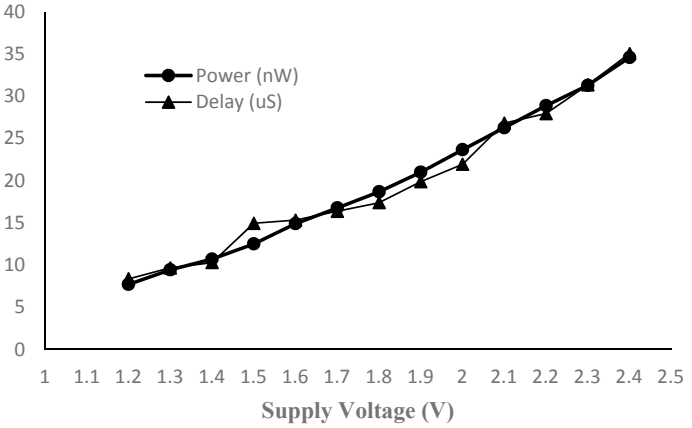

Fig. 4 Power and delay with supply voltage

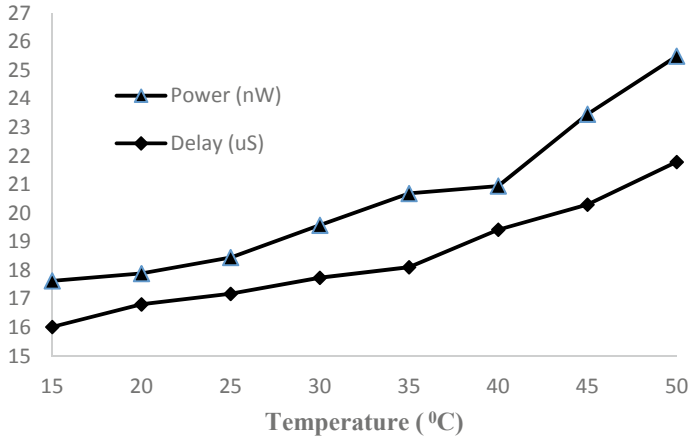

Fig. 5 Power and delay with temperature

2.1 Waveforms

Figure 6 shows the input A0, A1, A2, A3 and B0, B1, B2 and B3 which has taken in example with output of multiplier as P0–P7. It is clearly depicted from the waveform that the logic level achieved at the output of multiplier is sufficient for the functioning of the proposed design.

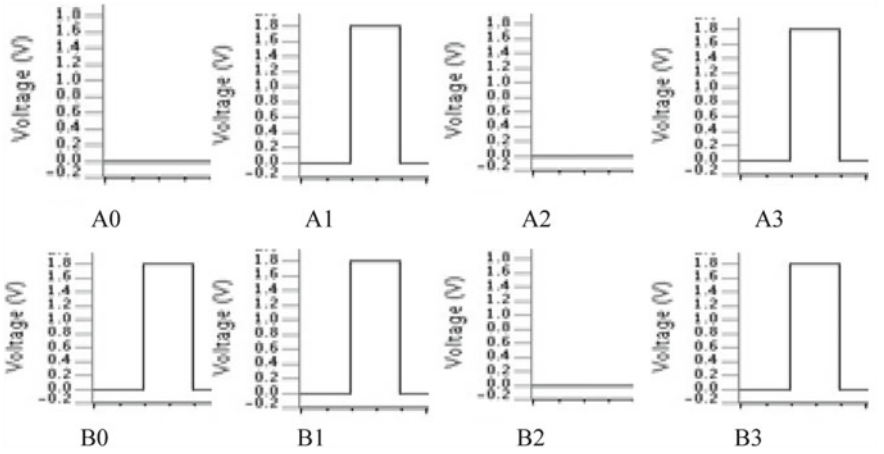

Fig. 6 Wave forms of input and outputs

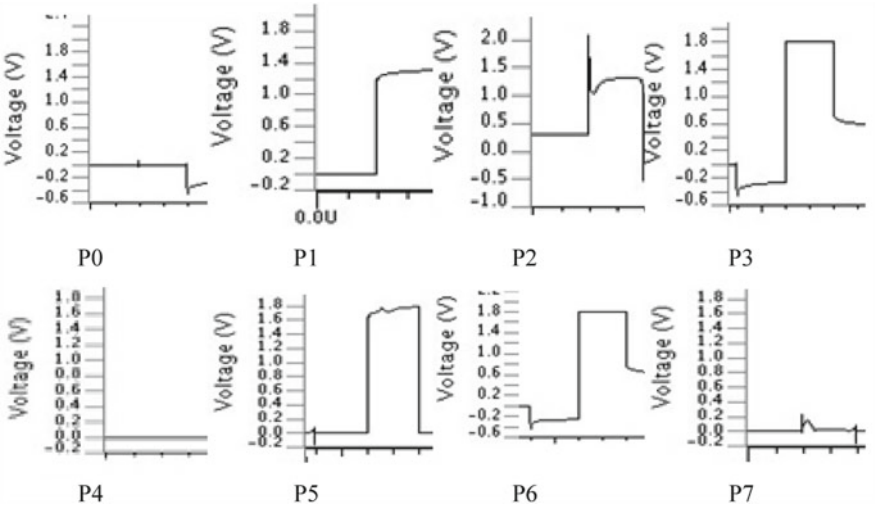

Fig. 6 (continued)

2.2 Comparison with Existing Designs

The proposed design of multiplier using adiabatic logic-based full adder has been compared with results of existing architectures reported in the literature on the base of power and technology used in Table 3.

3 Conclusion

A low power multiplier based on adiabatic logic has been reported in this paper. It is clearly depicted from the simulation results that the PDP of proposed multiplier is 32.42×10^{-4} pJ which is better as compared to existing designs reported in literature at a supply voltage of 1.8 V. Functionality of the proposed design also analyzed at varying temperature conditions with a frequency range of 10–100 MHz. It is depicted from the waveform that the proposed architecture performs better in terms of PDP as compared to other designs. As the limitations of reduction in feature size increases, the adiabatic logic-based designs become a better candidate for low power applications. As a future work, author is working toward the implementation of adiabatic logic-based multiplier in arithmetic and logic units.

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A Fully Integrated Tunable Memristor Emulator Circuit

Vikash Kumar, Indrajit Pal, and Aminul Islam

Abstract This chapter introduces the design of a memristor emulator which can be used for fully integrated circuit applications. The design employs a single voltage differencing transconductance amplifier (VDTA) as the active building block for simulating emulator behavior. Further, the design also contains one active analog multiplier, one passive grounded resistor, and capacitor, respectively. The proposed emulator circuit is simulated on the 45 nm CMOS technology node making it both cost and power-efficient emulator circuit. All the analytical derivations mentioned in this research work have been verified by simulation results obtained using Virtuoso custom design platform of Cadence. The non-volatile nature of the proposed circuit has also been validated.

Keywords Voltage differencing transconductance amplifier · Memristor emulator · Voltage mode · Memductance · Hysteresis loop

1 Introduction

Memristor, which is the abbreviation of two words "Memory" and "Resistor," is a nonlinear two terminal element. Memristor theory is initially introduced by Leon Chua in 1971 [1]. Later in 2008, memristor fabrication was successfully carried out by Stanley Williams from the Hewlett-Packard Company using titanium oxide (TiO_2) [2]. Before the introduction of memristors, there were three basic passive

V. Kumar
Department of Electronics and Communication Engineering, Presidency University, Bengaluru, KA 560064, India
e-mail: vikashkumar@ieee.org

I. Pal · A. Islam (✉)
Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra, Ranchi, Jharkhand, India
e-mail: aminulislam@bitmesra.ac.in

I. Pal
e-mail: pal.indrajit99@gmail.com

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elements, i.e., resistor, capacitor, and inductor. As such, a linear resistor forms a relation between "voltage" and "current" and the two other fundamental elements capacitor and inductor form the relation between "voltage" and "charge" and "current" and "flux," respectively. Similarly, the two terminal passive element, memristor, forms the missing relation between "flux" and "charge." Memristor possesses memristance, which exhibits pinched hysteresis behavior. Memristance depends on the direction of current flow; i.e., when current is allowed to pass in one direction, the memristance increases whereas it decreases once the direction of current is changed. The memristor is a versatile element due to its non-volatile behavior and therefore is used in high-density memory circuits [3] and neuromorphic systems [4]. A memristor can also be employed in various analog and digital applications such as programmable sinusoidal oscillators [5], adaptive filters [6], chaotic circuits [7], logic gates [8], and digital multipliers [9].

Since the commercial viability of physical memristor is complex and expensive, researchers have focused their attention toward emulating the behavior of TiO_2 memristor as the reference model. Several research papers have been published on memristor emulator circuits which can be physically implemented [10–13]. Nevertheless, such emulators lack certain features such as use of more number of passive elements, electronic tunability, pinch hysteresis loop at reasonably lower frequencies, lower power dissipation, etc. This paper proposes a fully integrated memristor emulator circuit which employs the active element as voltage differencing transconductance amplifier (VDTA). The proposed circuit reports desirable memristor features such as tunability, lesser number of passive elements, and lower power consumption.

2 VDTA

The active block used for realizing the memristor emulator circuit is voltage differencing transconductance amplifier (VDTA) [14, 15]. Figures 1 and 2 show block diagram of VDTA and its CMOS technology realized schematic. Basically, the VDTA

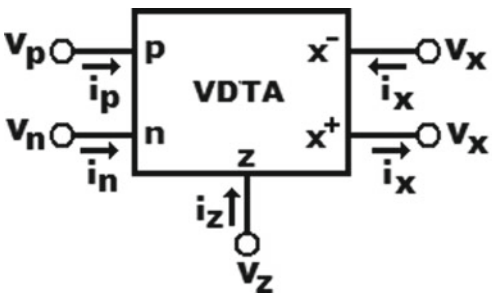

Fig. 1 Block diagram of VDTA

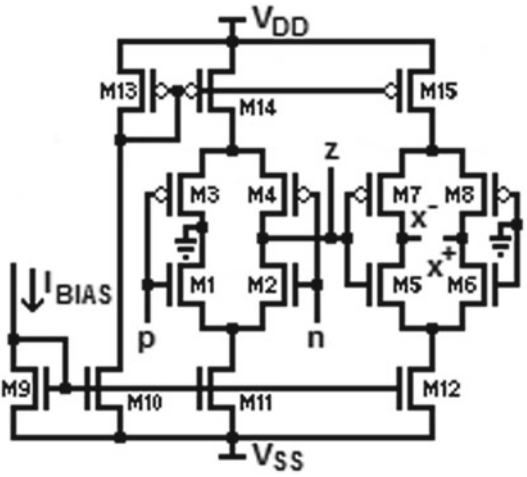

Fig. 2 Schematic of CMOS realized VDTA

consists of two operational transconductance amplifiers (OTAs) cascaded together as seen in Fig. 2.

The following matrix equation shows the current and voltage relations of VDTA's input–output terminals:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_{x-} \\ i_{x+} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ g_{\mathrm{mf}} & -g_{\mathrm{mf}} & 0 \\ 0 & 0 & g_{\mathrm{ms}} \\ 0 & 0 & -g_{\mathrm{ms}} \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix}. \tag{1}$$

Here, v_p, v_n, v_z, v_{x+}, v_{x-} and $i_{x+,}$ $i_{x-,}$ i_z are potential drops and currents at their respective VDTA ports. Current in p and n ports equals to zero due to very high impedance across them. g_{mf} and g_{ms} are effective transconductances of first and second OTAs, respectively, and are given as

$$g_{\mathrm{mf}} = \frac{g_{\mathrm{m1}} g_{\mathrm{m2}}}{g_{\mathrm{m1}} + g_{\mathrm{m2}}} + \frac{g_{\mathrm{m3}} g_{\mathrm{m4}}}{g_{\mathrm{m3}} + g_{\mathrm{m4}}}, \tag{2}$$

$$g_{\mathrm{ms}} = \frac{g_{\mathrm{m5}} g_{\mathrm{m6}}}{g_{\mathrm{m5}} + g_{\mathrm{m6}}} + \frac{g_{\mathrm{m7}} g_{\mathrm{m8}}}{g_{\mathrm{m7}} + g_{\mathrm{m8}}}. \tag{3}$$

where g_{m1}, $g_{\mathrm{m2,}}\ldots$, g_{m8} are individual transistor transconductances and can be calculated by using following relation

$$g_{\mathrm{mk}} = \sqrt{2\beta I_{\mathrm{DS}}}, \tag{4}$$

where

$$\beta = \frac{\mu_k C_{\text{ox}}}{2}\left(\frac{W}{L}\right). \tag{5}$$

Here, μ_k is mobility of kth transistor, C_{ox} is the ratio of oxide permittivity to its thickness, W and L are transistor dimensions, and I_{DS} is drain-to-source current.

3 Memristor Emulator Circuit

The presented memristor emulator circuit introduces the change in resistance by changing the value of applied voltage, v_{in}. The emulator circuit employs one VDTA as active element, two grounded passive elements, i.e., one resistor and one capacitor, an inverting/non-inverting buffer together with an analog multiplier. The configuration is shown in Fig. 3. The presented memristor emulator contains only active elements and grounded passive elements. Nonetheless, the earlier published emulator circuit comprises discrete multiplier circuits, which presents higher complexity, higher power, higher cost, etc. In this paper, the presented design consists of CMOS Gilbert cell-based analog voltage multiplier circuit which is fully integrated and consumes less power [16, 17].

Analyzing the circuit proposed Fig. 3 and using the current and voltage equations from [1], we obtain:

$$i_z = g_{\text{mF}}(v_p - v_n) = \mp g_{\text{mF}} v_{\text{fb}}, \tag{6}$$

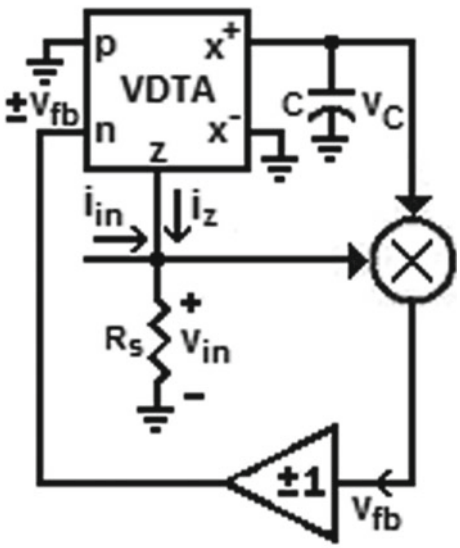

Fig. 3 Proposed VDTA-based memristor emulator

$$v_{\text{in}} = (i_{\text{in}} + i_z)R_{\text{s}} = (i_{\text{in}} \mp g_{\text{mF}} v_{\text{fb}})R_{\text{s}}. \tag{7}$$

Using (6) and (7), the current at the x^+ terminal is found to be:

$$i_{x^+} = g_{\text{mS}} v_z = g_{\text{mS}} v_{\text{in}} = g_{\text{mS}}(i_{\text{in}} \mp g_{\text{mF}} v_{\text{fb}})R_{\text{s}}. \tag{8}$$

The potential across capacitor *C,* i.e., v_{C}, is given by the integral of i_{x^+}. From (8), v_{C} is given as,

$$v_{\text{C}} = \frac{g_{\text{mS}}}{C} \int v_{\text{in}} \text{d}t. \tag{9}$$

The feedback voltage v_{fb} is obtained through CMOS Gilbert cell-based analog voltage multiplier circuit and is given by the multiplication of v_{C} and v_{in}, i.e.,

$$v_{\text{fb}} = v_{\text{C}} v_{\text{in}} = \frac{g_{\text{mS}} v_{\text{in}}}{C} \int v_{\text{in}} \text{d}t. \tag{10}$$

Putting (10) in (7), we get

$$i_{\text{in}} = v_{\text{in}} \left[\frac{1}{R_{\text{s}}} \pm \frac{g_{\text{mF}} g_{\text{mS}}}{C} \int v_{\text{in}} \text{d}t \right]. \tag{11}$$

Therefore, the memductance G_{M} is given by,

$$G_{\text{M}} = \frac{1}{R_{\text{s}}} \pm \frac{g_{\text{mF}} g_{\text{mS}}}{C} \int v_{\text{in}} \text{d}t. \tag{12}$$

From (12), the mathematical model of the presented memristor emulator shows incremental (+)/decremental (−) mode of operations.

4 Simulation Results

The presented emulator circuit has been implemented at CMOS 45-nm technology node using Virtuoso ADE of Cadence. $V_{\text{DD}} = -V_{\text{SS}}$; i.e., the power supply is considered as ±0.95 V. The passive component values are selected as $R_{\text{S}} = 1\ \text{K}\Omega$, $C = 10\ \text{nF}$. For a sinusoidal input signal (i_{in}) with amplitude of 50 μA, the behavior of characteristic frequency-dependent pinched hysteresis loop of the presented memristor emulator with variations in frequencies, i.e., at $f = 500$ Hz, $f = 1$ kHz, $f = 5$ kHz, and $f = 10$ kHz is shown in Fig. 4(a)–(d), respectively. The power dissipation of the emulator is calculated to be 3.956 mW.

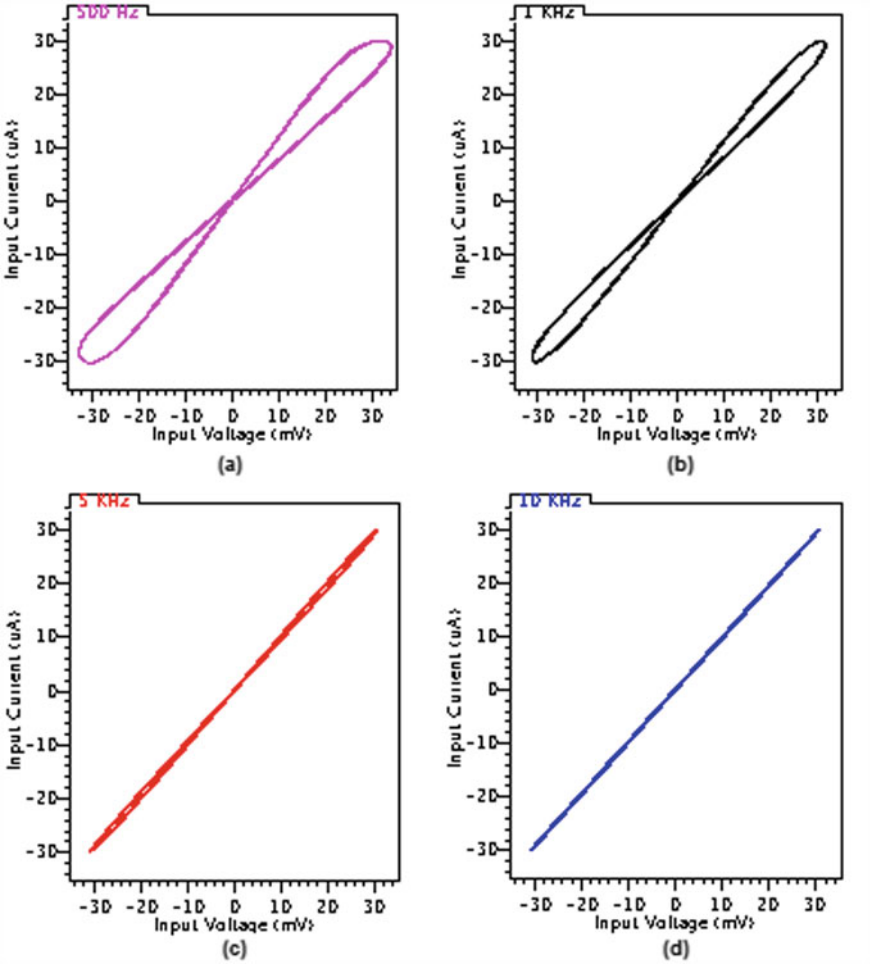

Fig. 4 Characteristic pinched hysteresis loop *I*–*V* plot of the presented memristor for sinusoidal input at amplitude 50 μA and frequency **a** 500 Hz **b** 1 kHz **c** 5 kHz and **d** 10 kHz

The controllability of bias current (I_{BIAS}) on the transconductance (g_{m}) is used for tuning the memductance presented by the presented memristor emulator. In accordance with (12), the memductance gradually increases/decreases with the increase in bias current. This tunable nature of the proposed memristor emulator circuit is advantageous for integrated circuit applications. Further, the change in memconductance when a train of pulse is applied across the presented memristor emulator circuits showing its incremental and decremental operations is shown in Fig. 5a–b, respectively.

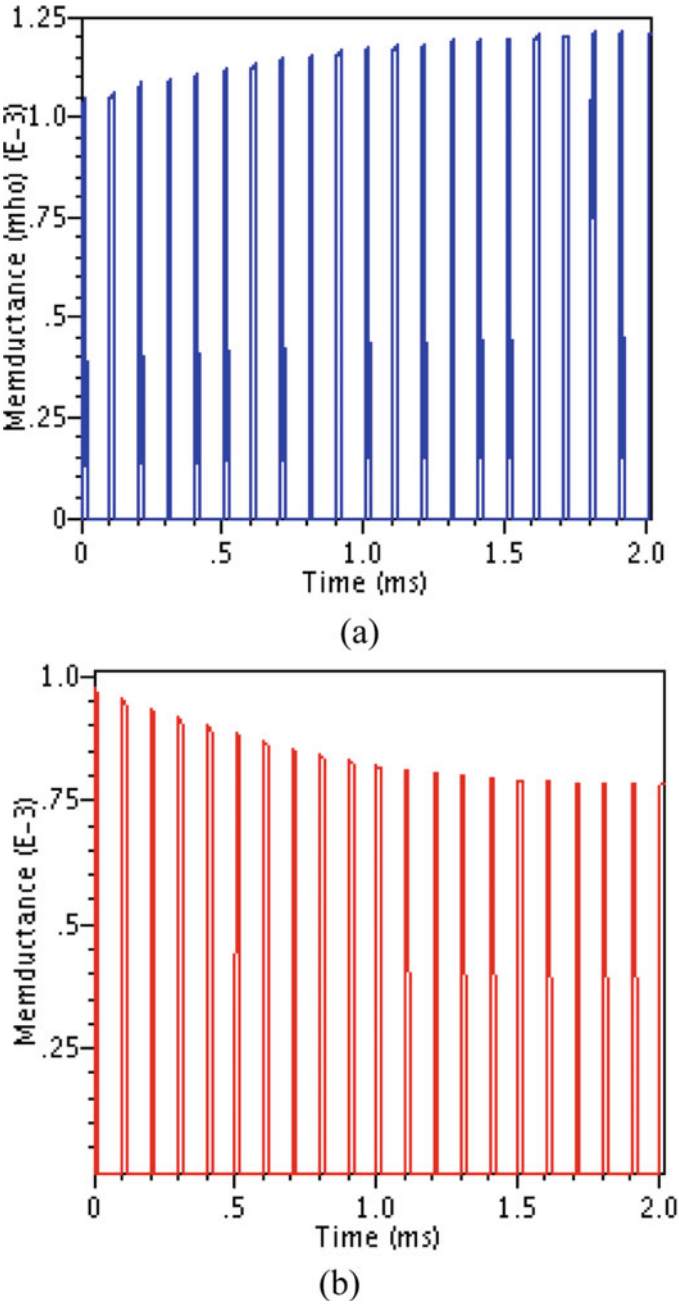

Fig. 5 Change in memconductance when a train of pulse is applied across the presented memristor emulator circuits **a** incremental **b** decremental memristor

5 Conclusion

A VDTA-based fully integrated grounded memristor emulator circuit is presented and designed using one VDTA, one four quadrant analog multiplier, two grounded passive elements, i.e., one capacitor, one resistor, and one inverting/non-inverting buffer. The presented emulator has simple circuit topology, fully integrated configuration, and low power consumption. The simulations presented here support the theoretical derivations, thereby making it a robust and versatile emulator. Further, the tunability via varying the bias current overcomes the process mismatches that occur during fabrication.

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Disease Prediction Based on Symptoms Using Machine Learning

Y. Deepthi, K. Pavan Kalyan, Mukul Vyas, K. Radhika, D. Kishore Babu, and N. V. Krishna Rao

Abstract The healthcare domain is one of the prominent research fields in the current scenario with the rapid improvement of technology and data. It is difficult to handle the huge amount of data of the patients. It is easier to handle this data through Big Data Analytics. There are a lot of procedures for the treatment of multiple diseases across the world. Machine Learning is an emerging approach that helps in prediction, diagnosis of a disease. This paper depicts the prediction of disease based on symptoms using machine learning. Machine Learning algorithms such as Naive Bayes, Decision Tree and Random Forest are employed on the provided dataset and predict the disease. Its implementation is done through the python programming language. The research demonstrates the best algorithm based on their accuracy. The accuracy of an algorithm is determined by the performance on the given dataset.

Keywords Big data analytics · Machine learning algorithms · Decision tree · Random forest · Healthcare · Naive Bayes · Python

1 Introduction

As we know that health is the priority even before the technology exists. Talking about the research field in terms of healthcare, there is a lot of scopes and it is evolving at a faster rate. To upgrade the existing model or technology, research on healthcare will affect totally in terms of humanity. Nowadays, healthcare communities are storing patient data so that they can use in the research area and can be used in developing new technology. Storing the tremendous data involved in big data and where big data analytics comes into action [1].

Big data is consists of humongous with complex data which is difficult to understand. It provided by the organization to store, handle and manage the data properly. To understand big, it also provides the solution to store and analyze unstructured and structured data in an effective manner rather than using RDMS (relational database

Y. Deepthi (✉) · K. P. Kalyan · M. Vyas · K. Radhika · D. K. Babu · N. V. Krishna Rao
Department of CSE, Institute of Aeronautical Engineering, Dundigal, Hyderabad, Telangana, India
e-mail: deepthisagar7@gmail.com

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management system). Big data provides the solution to handle the problem occurs in medical in term of data and prediction analysis is always being better when it comes to big data [2]. Big data Analytics is applied often in healthcare and it is used to handle and analyze the huge data [3] long term. Greater the time it takes to analyze the invasion, the greater are the chances that the system becomes vulnerable [1]. Any software or hardware which has higher computation capacity it least time is chosen over other existing tools.

Machine learning is a program that is used to perform some tasks. The machine takes some decision and predicts results [4]. The machine learning topic is getting popular which is used to solve real-time examples. Coming to the healthcare topic, prediction of the disease can be done by using the machine learning algorithm [1].

Our paper is all about predicting diseases based on symptoms using three classifiers, i.e. random forest, decision tree and Naive Bayes. Here, while predicting the diseases we are finding the accuracy which will help to make a decision appropriately.

Our paper consists of a section which is as follows: Second section provides the analysis of the existed paper used for the proposed project. Third section is about the methodology for predicting diseases based on different algorithms. Fourth section gives the output of the proposed project. At last, the 5th section will provide a conclusion.

2 Literature Survey

This section provides a survey on the already existed system approaches and understands the challenges behind it. It also provides the loophole present in the existing system so that we can overcome those loopholes and make it as a proposed system. In this paper, it is based on the prediction of disease which is diabetes disease using machine learning algorithms. Four machine learning algorithms are used to predict diabetes disease on Weka tool. The four algorithms, i.e. Simple CART, Naive Bayes, SVM and random forest are used for prediction and analyze the diabetes data. All four algorithms are built to compare against each other by their accuracy. The best model for predicting the diabetes disease of a patient is SVM because SVM is giving the best result when we compare with other algorithms while predicting diabetes diseases [1].

In this paper, it is based on heart disease prediction using machine learning such as SVM, Naive Bayes and Decision Tree. All four classifiers are applied with and without using PCA (Principle component analysis) on the dataset. They are using PCA as it is used to reduce the attributes from the dataset. After reducing the dataset, they observed that SVM is performing better than Naive Bayes and random forest. So, SVM can be used to predict heart disease. The result of this paper is to predict the disease like heart disease and diabetes diseases using Weka tool [5].

In this manuscript, it's about the prediction of diabetes disease using data mining. According to this paper, KNN and Naive Bayes algorithms are being used for prediction of disease and comparing accuracy against each other based on the disease

dataset. For the prediction of disease, they were using the disease dataset and by analyzing and processing that dataset to produce the appropriate output. Datasets consist of around 2000 diabetic patient data. When they compare both algorithm Bayesian and KNN based on accuracy, both of them gives better accuracy on larger dataset than smaller datasets [6].

In this manuscript, it's about predicting liver disease using a classification algorithm, i.e. logistic regression, SVM and KNN have been used to predict liver disease. All algorithms are being compared based on their accuracy through a confusion matrix. The liver disease dataset being downloaded from UCI with an instance of 567, whereas data is collected from the ILPD (Indian Liver Patient dataset). From the collected result and after analyzing of the result, they got to know that two algorithms, i.e. KNN and Logistic regression is having the best accuracy compared with other algorithms and out of these two algorithms, logistic regression is best and highly responsive in term of true positive rate or recall. So, the best model for liver disease prediction is logistic regression which is giving the best accuracy among all other algorithms [7].

In this paper, the author was telling about the heart disease is being predicted based on the machine learning algorithm. This paper consists of two algorithms, i.e. decision tree and Naive Bayes. Now, they are comparing those algorithms based on their accuracy and they are using the python programming language which helps them to find the accuracy with the appropriate result and helps them to figure out which algorithm is best for their proposed model. Dataset is being downloaded from the UCI machine learning repository containing 300 instances. Therefore, the result is to check whether a person having heart disease or not based on two classifiers. These two algorithms are producing accuracy one of them is the decision tree with 91% and Naive Bayes with 87% [8].

3 Methodology

This topic describes the approaches that we are using to build our project and how we are analyzing our project.

3.1 Anaconda Python Software

The features of anaconda software are as follows:

It used in machine learning applications, data science, predictive analytics, etc.
Developed by anaconda, Inc. and written in python.
The following software's are provided in Anaconda Navigator are as follows:

JupyterLab
JupyterLab Notebook

R-Studio
Spyder, etc

The current version of anaconda software is used based on the python version, i.e. 3.7.

3.2 Disease Dataset

The disease dataset is used and downloaded from the Kaggle website. Approximately 4000 instances are present in our disease data set. Attributes describe symptoms and prognosis which means it contains diseases. Datasets are divided into two set testing sets and training set with a size of 13.5 KB and 1.4 MB, respectively. About the disease dataset, it is used to find disease based on symptoms and these data are being used by the machine learning algorithms so that prediction can be done with correct accuracy.

4 Flow Chart of Our Proposed System

The proposed model is made for disease prediction based on symptoms and it takes the input from the dataset for symptoms and its correspondence diseases. The data, i.e. the symptoms that are entered by the user is taken by the software are being processed by the algorithms and these algorithms will analyze the data and produce the accuracy and come to a conclusion and show the result, i.e. disease based on symptoms. In the proposed model, the result is produced after processing and analysis of algorithms and we will print the disease with accuracy given by each algorithm.

Figure 1 shows the method that has been applied by our proposed model.

5 Algorithms

This subtopic describes the algorithms that are used in our proposed system which as follows: Naive Bayes Algorithm, Decision Tree Algorithm and Random Forest Algorithm.

5.1 Naive Bayes Algorithm

Naive Bayesian algorithm is a simple technique used for the purpose of classification. The workflow of the algorithm is based on the probabilistic method. The method

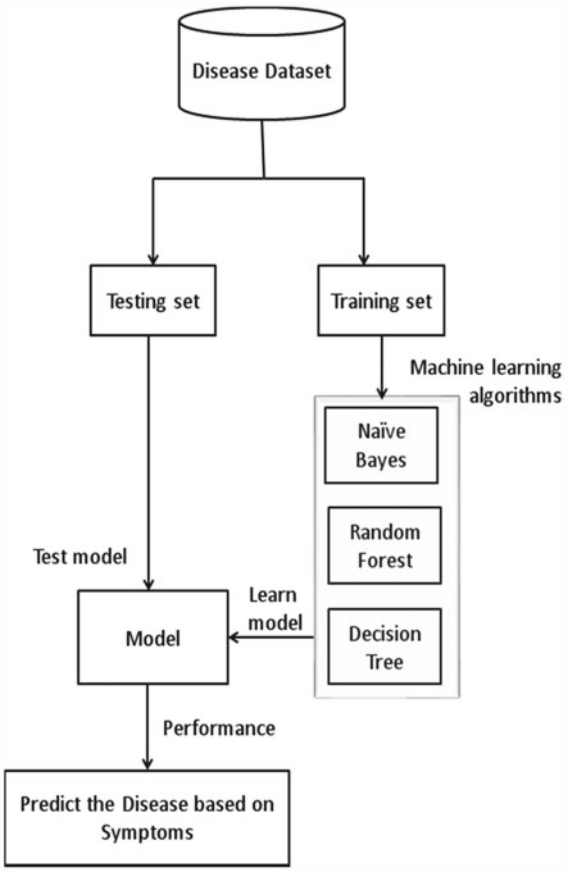

Fig. 1 Low representation of the proposed model

includes strong independent assumptions. So it is well known as probabilistic classifier. It provides the feature to construct the classifier models that assign class labels to problem instances.

The general formula for calculating the conditional probability is

$$P(H|E) = (P(E|H) * P(H))/P(E) \tag{1}$$

$P(H)$ = probability of Hypothesis H being true.
$P(E)$ = probability of Evidence
$P(E|H)$ = probability of Evidence given that Hypothesis is true
$P(H|E)$ = probability of Hypothesis given that Evidence is present

5.2 Work Flow of Naive Bayesian

1. First, collect the dataset and split it into two datasets namely training dataset and testing dataset.
2. Second, perform the training model on Training dataset.
3. Take the input from the training dataset.
4. Let the model classify and make prediction based on given inputs.
5. Perform Normal distribution on the dataset to calculate the accuracy.

Decision Tree Algorithm

Decision tree algorithm is one of the Machine Learning Algorithm. It falls under the category of supervised learning techniques. It is used for the analysis of classification. However, it is also useful in regression analysis. Decision tree uses a set of tree-like models of decisions and its possible consequences to make the decisions in an optimized manner. These decisions are to be resolved by using conditional control statements. Thus, in simple terms, we can conclude that decision tree algorithm is a set of trees that include bunch of conditions to generate a model of data at every node of a tree.

Work Flow of Decision Tree

The following steps are to be considered in the decision tree algorithm.

1. Consider we have taken a dataset that includes the features and target attribute.
2. Now give the training dataset to an algorithm, i.e. decision tree algorithm, it will generate a model that is used for classification and prediction. This is how it will create tree-structured classifier.
2. Now, the model will take the dataset as an input and based on what mechanisms says or whatever the rules defined in the model it will provide a class or target attribute, which will tell us that given input belongs to a particular class or target attribute.
3. Here, the decision tree performs its operations in an if-else conditional manner as it consists of a lot of decision trees and our task is to find the best solution for the given input.

Random Forest Algorithm

Random forest is a type of algorithm which is used for classification and regression. As we know the random forest is a one of supervised learning algorithm which means random forest algorithm uses the technique based on supervised learning if we talk about supervised learning in simple word supervised means a supervisor which gives the instruction, i.e. training data which gives input and output and based on the input and output of training data we are going to prepare a model and we will give new input to that model and check the output whether the valid output is coming or not.

The random forest is a type of ensemble classifier which is using the decision tree algorithm in a randomized fashion. It consists of many trees which are called

decision trees and these trees are of different structures and to make a decision tree we are choosing features and samples randomly from the training dataset and that's how we construct many decision trees and combined all the decision trees makes a random forest. Here, we are going to explain how a random forest works:

1. Initially, we should have training data which consist of various attributes and target attribute.
2. Now, we have to make a decision tree, to make a decision tree we have to generate BD (Bootstrap dataset) and to make BD we have to do sampling which means we have to pick any sample randomly from the training dataset and put it into Bootstrap dataset. Duplication is allowed with less frequency.
3. Using BD we have to plot a decision tree in a randomized fashion and calculate how we can choose the root node from the BD which is producing the best split of samples.
4. Again do the splitting of features for child node and provide the leaf node to the child node after splitting of features.
5. Repeat steps 2–4 and makes as many decision trees as we can.
6. Take the test tuple and let the model classify and predict the output of the given test tuple.
7. Now, calculate the votes produced by various decision trees.
8. Consider the majority of votes produced for the target attribute of test tuple and that will be a final prediction.

6 Result and Discussion

In our paper, we are checking what type of disease a person has based on symptoms through machine learning. Here, our project will predict the disease by applying machine learning algorithms namely decision tree, Naive Bayes and Random Forest. These algorithms predict a similar disease with different accuracy.

The accuracy of the random forest is 94.6% which is highest among all other algorithms. The accuracy of Naive Bayes is 84.5% which is highest than the decision tree and the accuracy of the decision tree is 78.5%. Overall, we can get to know that random forest is effective in terms of predicting diseases. Below bar graphs are used to compare different algorithms based on accuracy with different types of diseases (Figs. 2, 3 and 4).

From this experiment, we got to found out that with the highest accuracy the random forest is the best model compared to other algorithms. So, for the prediction of diseases, we shall use the random forest as a default model to give better results and accuracy.

Fig. 2 Comparison between three different algorithms while predicting Jaundice based on symptoms and from the graph, we got to know that random forest is having the highest accuracy

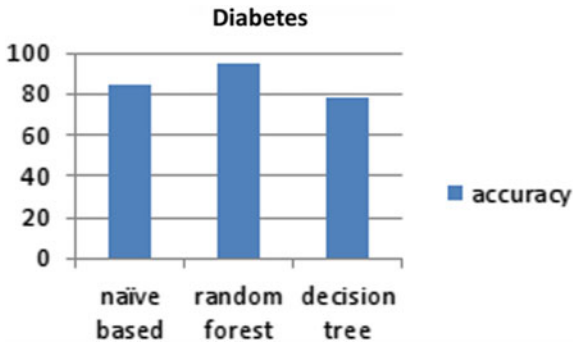

Fig. 3 Comparison between three different algorithms while predicting diabetes based on symptoms and from the graph, we got to know that random forest is having the highest accuracy

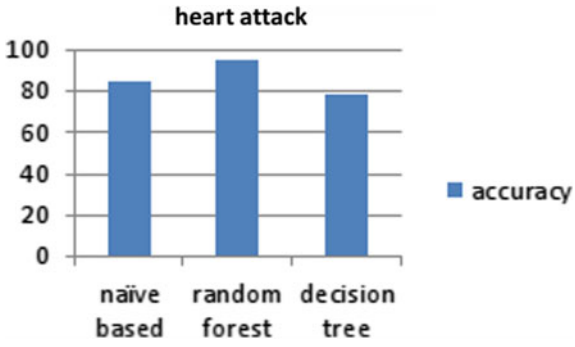

Fig. 4 Comparison between three different algorithms while predicting heart attack based on symptoms and from the graph, we got to know that random forest is having the highest accuracy

7 Conclusion

From our research paper, we conclude that we are using three machine learning algorithms, i.e. random forest, Naive Bayes and decision tree for predicting diseases based on symptoms. These algorithms are used to predict disease based on symptoms and are being compared through their accuracy against each other. From the experiment, we get to know that random forest has the highest accuracy among other algorithms.

Therefore, it can conclude that random forest is appropriate for predicting diseases based on symptoms.

In the future, we can upgrade our project by adding some other machine learning algorithms and can compare their accuracy against each other so that it will be easy to find out the disease based on symptoms.

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A New Hybrid Method Approach for Linear System Approximation

Arvind Kumar Prajapati, Nimisha Bharti, Afzal Sikander, and Rajendra Prasad

Abstract A new system simplification hybrid method is proposed in this article. In this hybrid method, the advantages of two different approaches are being employed in order to simplify the higher dimensional systems. The unknown constant of denominator polynomial is derived using Routh stability whereas improved Padé approximation is employed to achieve numerator polynomial coefficient of the targeted simplified/micro-system. The proposed hybrid method is validated by simplifying standard higher dimensional systems available in the literature. It reveals that the simplified/micro-system derived by using proposed hybrid method holds the essential characteristics of original system that is stability and time response specifications.

Keywords Improved Padé Approximation · Higher dimensional systems · System approximation · Stability

1 Introduction

System simplification is the mathematical tool for approximating the higher dimensional systems to the lower dimensional systems. This system simplification terms as model order reduction also which is having less number of states compared to original systems. The Padé approximation, based on moment matching [1], is one of the

A. K. Prajapati (✉)
VIT-AP University, Amaravati, Andhra Pradesh, India
e-mail: arvindawr1990@gmail.com

N. Bharti · A. Sikander
Department of Instrumentation and Control Engineering, Dr. B. R. Ambedkar National Institute of Technology, Jalandhar 144011, Punjab, India
e-mail: nimiranjan38@gmail.com

A. Sikander
e-mail: afzals@nitj.ac.in

R. Prasad
Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee 247667, India
e-mail: rpdeefee@iitr.ac.in

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simplest methods for deriving reduced order model in frequency domain. But Padé approximation sometimes gave unstable approximants. Thus, Routh Padé approximation [2] and other methods like stability equation method [3], clustering methods [4, 5], etc., were developed to ensure the stable models. The methods developed for continuous time (s-domain) were also applied to discrete time systems (z-domain). In discrete time domain, order reduction may be achieved directly as in [6] or by using transformation to some other form [7]. The process of reduction is carried out by transformation in the continuous time domain. Using inverse transformation, the original system is retrieved.

In addition, different techniques of order reduction are discussed as optimal Hankel norm approximation [8], proper orthogonal decomposition [9], balanced realization [10] and Krylov subspace techniques [11] for large-scale systems. In [12] translation of Hankel matrix to Hermit form is suggested to obtain reduced order model. In comparison, an updated Hankel matrix is suggested in [13]. But again, the changed matrix often resulted in inconsistent second-order versions. Clustering of poles and Pade approximation is used in combined form in [14]. However, this method makes the system unstable and non-minimum phase. In addition, the [15] method of factor division is proposed on the basis of geometric analysis, which helps in selecting the factor to be omitted at each stage, and a modified Lucas approach is given on the impulse-response energy response.

Some methods based on time moments and Markov parameters approximate unstable reduced systems even though the original systems are stable [1, 16]. However some methods of reduction failed for some system, [17] addressed certain type of systems in which Padé approximation and time-moment matching methods have failed. In order to solve this problem and get the stable model, various hybrid system simplification methods have been proposed [18–22]. These mixed methods guarantee the stability better performance of reduced models when the higher dimension systems are stable.

Numerous system simplification methods are floated in the literature which are independent from the time moments matching and Markov parameters. Such approaches are given in [23–28], etc. Among these methods, method discussed in [28] is very popular method in the time domain. This method has been implemented in different era of science and engineering [29, 30]. In this method, the problem of mismatching of steady-state value persists. In order to deal this situation, three types of methods, based on balanced truncation, are suggested [31–33]. In the field of engineering and sciences, rather than balanced truncation, other model reduction techniques are also useful for the simplification and synthesis of high-dimensional dynamical systems [34–39].

2 Problem Statement

An *nth*-order high-dimensional single output input (SISO) model is governed by the below mathematical relationship

$$G(s) = \frac{N(s)}{D(s)} = \frac{d_{11}s^m + d_{21}s^{m-1} + d_{12}s^{m-2} + d_{22}s^{m-3} + \cdots + d_{2,(m-2)}s^2 + d_{1,(m-1)}s + d_{2,m}}{e_{11}s^n + e_{21}s^{n-1} + e_{12}s^{n-2} + e_{22}s^{n-3} + \cdots + e_{2,(n-2)}s^2 + e_{1,(n-1)}s + e_{2,n}} \quad (1)$$

where $m < n$. The main goal of this study is to advise a technique to formulate the following simplified/micro-system of rth-order ($r < n$) model described as follows:

$$R_r(s) = \frac{Q(s)}{P(s)} = \frac{q_0 + q_1 s + q_2 s^2 + \cdots + q_{r-1}s^{r-1}}{p_0 + p_1 s + p_2 s^2 + \cdots + p_{r-1}s^{r-1} + p_r s^r} \quad (2)$$

where $q_0, q_1, q_2 \ldots$ *and* $p_0, p_1, p_2 \ldots$ are the unknown constants.

3 Proposed Approximation Method

Steps for obtaining approximate model are given below:

Step 1: Procedure for obtaining the denominator polynomial of rth-order approximated system by using Routh stability technique [23]

To obtain the denominator of the estimated model, the Routh stability arrays for the denominator of the actual system (1) are given in Table 1. In this Routh stability array, the first two rows of Table 1 are built from the polynomial denominator coefficients of the actual system (1) as follows.

After formulating first two rows, the remaining rows of the Routh stability table are constructed by the well-known formula discussed in [23]. This formula is defined as follows

$$e_{i,j} = e_{i-2,j+1} - \left(e_{i-2,1}.e_{i-1,j+1}\right)/\left(e_{i-1,1}\right)$$

For $i \geq 3$ and $1 \leq j \leq \left[\frac{n-i+3}{2}\right]$.

Table 1 Routh table

e_{11}	e_{12}	e_{13}	e_{14}	...
e_{21}	e_{22}	e_{23}	e_{24}	...
e_{31}	e_{32}	e_{33}	...	
e_{41}	e_{42}	e_{43}	...	
$e_{n-2,1}$	$e_{n-2,2}$			
$e_{n-1,1}$	$e_{n-1,2}$			
$e_{n,1}$				
$e_{n+1,1}$				

The coefficients of the denominator of the rth-order reduced model are computed by using the $(n+1-r)$th and $(n+2-r)$th rows of the Routh stability table and can be written as

$$\begin{aligned} P(s) &= p_0 + p_1 s + p_2 s^2 + \cdots + p_{r-1} s^{r-1} + p_r s^r \\ &= \left\{ e_{n+1-r,1} s^r + e_{n+2-r,1} s^{r-1} + e_{n+1-r,2} s^{r-2} + \cdots \right\} \end{aligned} \tag{3}$$

Step 2: The procedure of computing the numerator polynomial of the estimated system using the improved Padé approximation method [40]

The transfer function $G(s)$ can be written in power series form

$G(s)$ about $s = \infty$, i.e.

$$\begin{aligned} G(s) &= M_0 s^{-1} + M_1 s^{-2} + \cdots + M_{2r} s^{-2r-1} + \cdots \\ &= \sum_{i=0}^{\infty} M_i s^{-i-1} \end{aligned} \tag{4}$$

$\{M_i : i = 1, \ldots, \infty\}$ are known as Markov parameters and 'r' is the order of approximated model.

$G(s)$ can be expanded in power series form

$$\begin{aligned} G(s) &= c_0 + c_1 s + c_2 s^2 + \cdots + c_{2r} s^{2r} + \cdots \\ &= \sum_{i=0}^{\infty} c_i s^i \end{aligned} \tag{5}$$

The parameters $\{c_i : i = 0, 1, 2, \ldots, \infty\}$ are time moments of system.

The coefficients of numerator of rth-order approximated model can be obtained by using (6) discussed in [40]

$$\begin{aligned} q_0 &= c_0 p_0 \\ q_1 &= c_1 p_0 + c_0 p_1 \\ q_2 &= c_2 p_0 + c_1 p_1 + c_0 p_2 \end{aligned} \tag{6}$$

$$\begin{aligned} q_{\alpha-1} &= c_{\alpha-1} p_0 + c_{\alpha-2} p_1 + \cdots + c_1 p_{\alpha-2} + c_0 p_{\alpha-1} \\ q_{r-\beta} &= M_{\beta-1} p_r + M_{\beta-2} p_{r-1} + \cdots + M_1 p_{r-\beta+2} + M_0 p_{r-\beta+1} \\ q_{r-\beta+1} &= M_{\beta-2} p_r + M_{\beta-3} p_{r-1} + \cdots + M_1 p_{r-\beta+3} + M_0 p_{r-\beta+2} \\ &\vdots \\ q_{r-2} &= M_1 p_r + M_0 p_{r-1} \\ q_{r-1} &= M_0 p_r \end{aligned}$$

4 Numerical Problems

To demonstrate the importance of proposed method over the another popular model diminution technique, the ISE and RISE of their lower order systems are computed and defined as [22, 41]

$$\begin{cases} \text{ISE} = \int_0^\infty [y(t_i) - y_r(t_i)]^2 \mathrm{d}t \\ \text{RISE} = \int_0^\infty [y(t_i) - y_r(t_i)]^2 \mathrm{d}t \Big/ \int_0^\infty \left[\hat{y}(t_i)\right]^2 \mathrm{d}t \end{cases} \tag{7}$$

Two more performance indices IAE and ITAE are calculated to compare the efficiency and accuracy of original and approximated model [31, 42]

$$\begin{cases} \text{IAE} = \int_0^\infty |y(t_i) - y_r(t_i)| \mathrm{d}t \\ \text{ITAE} = \int_0^\infty t|y(t_i) - y_r(t_i)| \mathrm{d}t \end{cases} \tag{8}$$

where $y(t_i)$ and $y_r(t_i)$ are the step responses of large-scale and simplified models at t_i time, respectively.

Example 1 Closed loop transfer function of single area power system is [42]

$$G(s) = \frac{250}{s^3 + 15.88s^2 + 42.46s + 106.2} \tag{9}$$

By using technique mentioned in Sect. 3, the denominator of reduced model is obtained as

$$P(s) = 15.88s^2 + 35.77s + 106.2 \tag{10}$$

By using (6), the coefficients of the numerator are obtained by using ($c_0 = 2.354$, $M_0 = 0$) with ($\alpha = 1$, $\beta = 1$) and the approximated system computed using proposed technique is

$$R_2(s) = \frac{-15.74s + 250}{15.88s^2 + 35.77s + 106.2} \tag{11}$$

Time response of large-scale system and approximated models using different reduction techniques is shown in Fig. 1. From this plot, it can be noticed that the responses of reduced micro-systems resulting from the proposed method and Routh stability scheme [16] indicates the best approximation towards the original system. The different performance indices of various model simplification methods are presented in Table 2. It can be concluded that the proposed scheme has lower

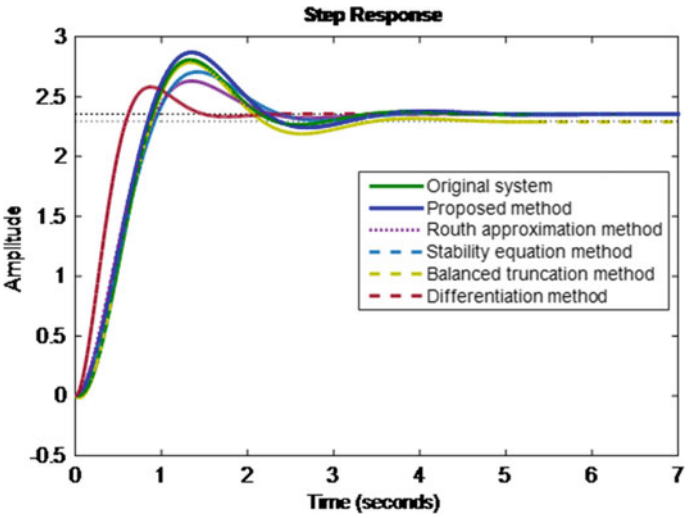

Fig. 1 Comparison of time responses of original and reduced systems

Table 2 Comparative analysis of approximation techniques for example -1

Method	Simplified system	ISE	RISE	IAE	ITAE
[44]	$\frac{250}{5.293s^2+28.307s+106.2}$	5.0625	0.0615	9.2619	9.6414
[28]	$\frac{-0.8056s+16.81}{s^2+2.391s+7.327}$	3.5183	0.0428	58.9888	.029887
[45]	$\frac{-33.321s+250}{5.293s^2+28.307s+106.2}$	2.1753	0.0264	6.7339	10.6854
[26]	$\frac{18.817}{s^2+2.594s+7.994}$	0.4661	0.0057	2.7715	10.2811
[21]	$\frac{-0.00045s+18.6863}{s^2+3.1737s+7.939}$	0.3506	0.0043	3.1688	19.6397
[41]	$\frac{0.00011557s+18.6863}{s^2+3.1737s+7.939}$	0.3506	0.0043	3.1219	17.1278
[19]	$\frac{-0.0046s+250}{15.88s^2+42.46s+106.2}$	0.1783	0.0022	2.2553	5.8739
[27]	$\frac{15.74}{s^2+2.674s+6.88}$	0.1782	0.0022	2.2124	3.5368
[25, 46, 47]	$\frac{250}{15.88s^2+42.46s+106.2}$	0.1782	0.0022	2.2124	3.5368
[18, 48]	$\frac{-15.748s+249.995}{15.88s^2+35.772s+106.2}$	0.1641	0.0020	2.3106	6.4905
[23]	$\frac{250}{15.88s^2+35.772s+106.2}$	0.1621	0.0020	2.1555	3.3033

value of error indices compared to other standard model reduction methods. It can be seen that the proposed and Routh stability methods give same error indices. But proposed method guarantees the matching of first few time moments and Markov parameters of reduced model with original system. Static and dynamic responses of original and approximated model are guaranteed by matching the time Markov parameters and time moments, and its reason is given in [43].

Example 2 A ninth-order stable linear system is given below

$$G(s) = \frac{s^4 + 35s^3 + 291s^2 + 1093s + 1700}{s^9 + 9s^8 + 66s^7 + 294s^6 + 1029s^5 + 2541s^4 + 4684s^3 + 5856s^2 + 4620s + 1700} \tag{12}$$

The approximated system obtained through proposed technique with $[(\alpha = 2, \beta = 0)$ so it needs $(c_0 = 1, c_1 = -2.0747)]$ is given follows

$$R_2(s) = \frac{-1539.7677s + 1700}{800s^2 + 1987.2323s + 1700} \tag{13}$$

Figure 2 shows the step responses of approximated model and original system obtained using proposed hybrid technique and some other standard model reduction techniques. The proposed hybrid technique indicates the closer approximation as compared to standard model reduction techniques. Various model reduction methods are compared in terms of different performance error indices and are shown in Table 3. From Table 3, it can be observed that performance indices values of proposed method are lower than the standard simplification methods [28, 31, 41, 46, 48]. From Table 3, it can also be observed that as reduced models obtained by Pal [18], Singh et al. [48] and by proposed techniques are almost similar, but the proposed technique guarantees the matching of first few time moments and Markov parameters of original and reduced models.

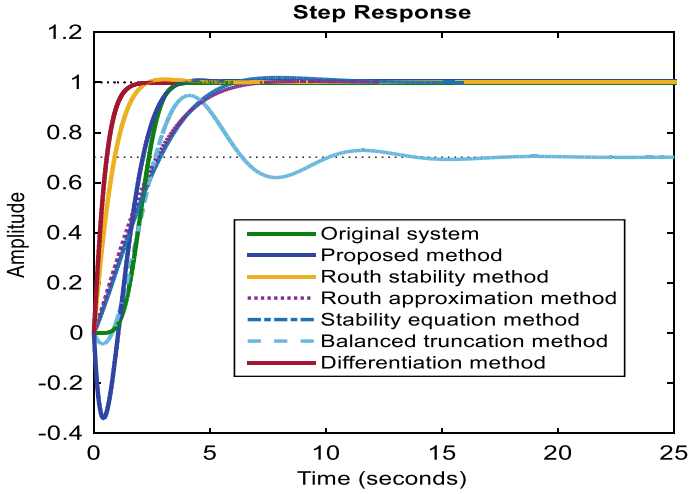

Fig. 2 Comparison of step responses of original system and reduced models obtained by various reduction schemes

Table 3 Comparative analysis of reduction methods for Example-2

Method	Approximated model	ISE	RISE	IAE	ITAE
[28]	$\frac{-0.2466s+0.5583}{s^2+0.593s+0.7956}$	85.1787	18.1032	286.8248	14903.07
[45]	$\frac{-4.5354e8s+3.084e8}{2.951e7s^2+1.863e8s+3.084e8}$	13.116	2.7876	15.9915	17.8332
[23]	$\frac{863.9525s+1700}{800s^2+1987.2323s+1700}$	7.9082	1.6807	14.1305	20.6298
[31]	$\frac{-1.0576s+0.7956}{s^2+0.593s+0.7956}$	7.1615	1.5220	24.5150	117.233
[44]	$\frac{4.958e7s+3.084e8}{2.951e7s^2+1.863e8s+3.084e8}$	10.9331	2.3236	16.2998	21.9267
[21, 24, 41]	$\frac{0.2645s+0.4114}{s^2+1.118s+0.4114}$	1.3177	0.2801	7.8301	20.8253
[47]	$\frac{1093s+1700}{5856s^2+4620s+1700}$	1.2093	0.2570	8.6629	32.7897
[19, 25, 46]	$\frac{1093s+1700}{5031.0743s^2+4620s+1700}$	1.1921	0.2533	7.9397	25.1436
[18, 48]	$\frac{-1539.7677s+1700}{800s^2+1987.2323s+1700}$	0.9609	0.2042	4.7371	6.4700

5 Conclusion

This paper leads to a new hybrid approach for the comparison of a large-scale structure to a functional simplified/micro-system. The current approach of model reduction is a stable reduction model approach and provides better, unique and improved response compared to the other standard techniques of model approximation. Denominator and numerator polynomial are obtained by two different techniques in this hybrid method of model approximation. The methodology provided ensures that the core characteristics of the high-dimensional original system, such as the steady-state value and consistency of the estimated reduced model, are preserved. It is evident from both the basic examples given in this reference that the suggested simplification strategy offers better results and lower performance indices of error. This renders the new methodology compatible with other current reduction systems. This approach can be also used for the simulation of large-scale multi-variable structures and the design of the controller.

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Organic Solar Cell

B. Navothna, T. Saritha Kumar, B. Chandana, V. Manasa, and G. Pranathi

Abstract The research for an organic solar cell has started from the past 3 decades, but especially in the last 10 years, all looked towards this cell because of the enormous increase in power consumption. This cell has attracted economic and scientific interests by the increase inefficiencies of power conversion and this got succeed with the usage of new materials, developed material engineering, and advanced device structures. Nowadays, with the help of many device concepts, we can increase efficiencies more than 3% of solar power converters. The field of OSCs has developed from the concepts of radiation emitting diodes based on similar technologies. OSCs have drawn attention in society due to its unique characteristics like lightweight in nature, flexibleness, effective cost fabrication and also improvements made in the energy conversion efficiency. But still, these improvements did not increase the efficiencies of organic solar cells more than that of inorganic solar cells. If we can increase the working-efficiency of the organic solar cell to half of the working-efficiency of the inorganic cell then automatically the production cost will be reduced. This take will give a rough overview of the history of solar cells, its working and also about its structure. The comparison of OSCs and its applications, current situation, environmental impacts will be described.

Keywords Organic solar cell (OSC) · Inorganic solar cell (ISC)

B. Navothna (✉) · T. Saritha Kumar · B. Chandana · V. Manasa · G. Pranathi
Department of Electrical and Electronics Engineering, Institute of Aeronautical Engineering, Hyderabad 500 043, India
e-mail: navothna9999@gmail.com

T. Saritha Kumar
e-mail: tmsaritha@gmail.com

B. Chandana
e-mail: chandanashiney98@gmail.com

V. Manasa
e-mail: vanammanasa8@gmail.com

G. Pranathi
e-mail: sonypranathi11@gmail.com

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1 Introduction

In the current scenario, energy requirement is increasing on daily basis. As per the estimation, till the end of the year twenty fifty, the world requires thirty tera-watts of energy. This is due to all the equipment relies on energy. To meet energy demand, renewable energy resources are required. And by employing renewable energy sources as primary resources of energy as they have capacity to reduce the dependency on fossil fuels. The major problem for reducing the use of non-renewable sources it produces lot of environmental defilement as it creates lopsidedness in the environment and also they are on the edge of being exhausted.

The best solution for the above mentioned problem is using renewable energy source such as wind and solar energy in order to meet large energy demand and also to prevent the atmosphere from the environmental pollution. Solar energy is a clean form of energy and cannot be depleted easily. The complete energy consumption of world till the year 2040 is as represented in Fig. 1. The graph indicates that by the end of the year 2050 the energy demand is very high and it is fulfilled by both solar and wind energy [1].

A photovoltaic material is a tool that converts light energy in form of electrical energy. Using photovoltaic effect, the generation of electricity is from radiant energy from sunlight. The number of solar cells is connected in series and parallel combination or together, to generate desired solar power. This complete arrangement of these photovoltaic cells is known as PV modules or solar panels [2].

There are three types of solar cells.

- First era—Si photovoltaic cell
- Second era—Thin-film photovoltaic Cell
- Third era—Organic photovoltaic Cell.

A thin layer of organic semiconductor material forms the third era- organic solar cell. Hence the name is given as 'Organic Solar Cell'. Sunlight is composed of radiant

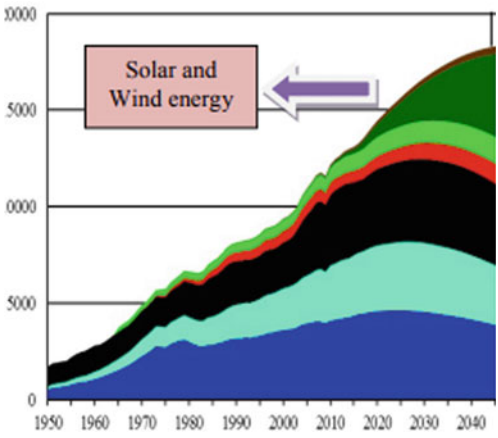

Fig. 1 Total world energy consumption

particles known as photons. The major problem nowadays global warming is one of the major problems. So to reduce global warming we have to search for another method to produce energy without the harmful atmospheric gases. OSC is made of high rate as it has low cost of assembly, flexibility, low-temperature process [1, 3]. We can gather energy from sunlight by using a technology known as photovoltaic. This is the main component of energy generation [3].

2 Structure of Organic Solar Cell

The basic structure of organic solar cell is as shown in Fig. 2. In-between two thin-film electrodes the photoactive layer is placed. One of the electrodes is a flexible transparent substrate; this flexible transparent substrate material that passes sun illumination to enter into cell. From two various forms of semiconductors, i.e. donor and acceptor the photoactive layer is made, which form multi-barrier similar to the p-n junction ISC. By the transfer of charge carriers, it will generate electron-hole pair. To increase the efficiency the structure should be consists of thick layers. Optical losses can be reduced by coating the anti-reflection coating material to the surface of the layers.

Basic structure of OSC is as shown in Fig. 2. Organic solar cell consists of a layer which is active and made of organic semiconductor which is connected between 2 electrode plates that is positive (cathode) and negative (anode) terminals. In which one of the electrode plates is positive which a cathode is and the other terminal is negative which is an anode and one of the electrode plates is formed translucent to devour the sun's useful radiation. At the moment the sun's radiation, i.e. which

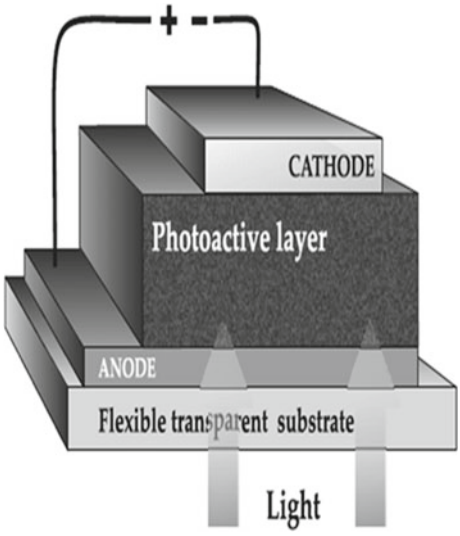

Fig. 2 Basic structure of OSC

comprises group of photons, i.e. energy strikes the cell top layer then small part of the radiation it reflects and certain amount of radiation of sun is absorbed. When the photon is absorbed completely, an electron present in the highest occupied molecular orbit (HOMO) gains some amount of energy and travels to the lowest occupied molecular- orbit (LUMO). The energy level range is in between these two orbits i.e., HOMO and LUMO ranges between one electron volt (eV) to four electron volt (eV) [4]. The photons which are important source of energy and having an energy level more than that of the band gap can take place in the working of the organic photovoltaic cell (or) solar cell. As we know, the components with a low band gap are preferred to upgrade the energy in watts efficiency of the cell. The movement of an electron from the highest occupied molecular orbit helped in production of the hole and electron-hole pair is created known as excitons. The dielectric constant of an active layer is very low in between three-four So, by Columbic force of attraction, the excitons are strongly bounded. According to law of nature the coulomb force of attraction is inversely proportional to dielectric constant. The diffusion vertical area of the exciton is ten nano metre then the exciton can diffuse within this diffusion region in its time period. The Exciton separation takes place in between donor and acceptor material.

Negatively charged particles move from the acceptor layer and holes move from the donor layer next to the exciton separation [5]. The negative terminal which is anode it collects the holes and cathode is the positive terminal collects the electrons. Lowest occupied molecular orbit offset has a important role in exciton separation. The offset cannot be too high or too low; it should be limited in the between the values ranging from of 0.3 to 0.9 eV. Range both of LUMO and HOMO of donor and acceptor components as given in Fig. 3. And application of very low forward bias potential, negative charges move through the electrode plates and thus current is developed. The process of diffusion in exciton affects the improvement in organic cells [6].

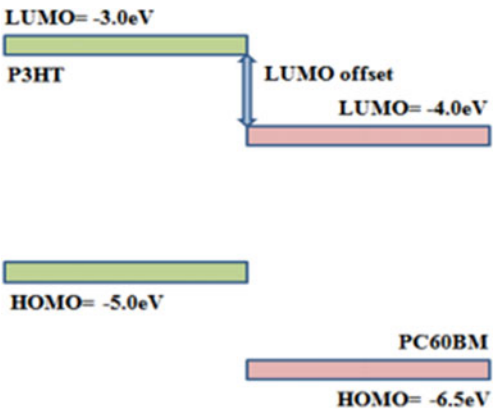

Fig. 3 Range of HOMO and LUMO of donor and acceptor component

3 Working of OSC

From sunlight the photon is absorbed by photoactive layer. This absorption of solar radiation develops excitons, i.e. closely packed electron-hole pair which travel towards Donor-Acceptor interface where they get dissociates into charge carriers at the interface. After completion of diffusion step, electrons travels towards acceptor component and holes move towards donor components. As a result the steady flow of charges flows in the external circuit, collection of charges at relative electrodes results into production of electricity. In other words we can explain this process, in three steps. Step one absorption of sunlight into solar cells take place. In step two, absorption of photons which will create the excitons. Step three, these excitons recombined with holes-pairs which will create the free charge carries results in generation of electric power.

When the photons which can do work or to produce energy inbuilt in the sunlight hits the organic semiconductor cell or device from the transparent negative terminal of the semiconductor material. They creates exciton in the outer most shell of the semiconductor. The operating principle of an organic photovoltaic cell or OSC as represented in Fig. 4. These excitons are consisting of both positively charged particles which are holes and negatively charged particles which are electrons and have a complete span at that time the materials which cannot be separated they combine together to generate energy and when no electricity is produced. Or else, if these charges are separated in between by electrostatic forces of anode and cathode then they can be used as current by passing through the load. Because of the presence of the potential barrier in 'Schottky contact' strong electric field may be a developed in a single layer organic solar cell (Fig. 5).

In an organic photovoltaic device, dissociation of exciton depends mainly on potential gradients across acceptor ions donor ions interface, which results from photons creates transfer of charge between donor and acceptor materials [7]. The

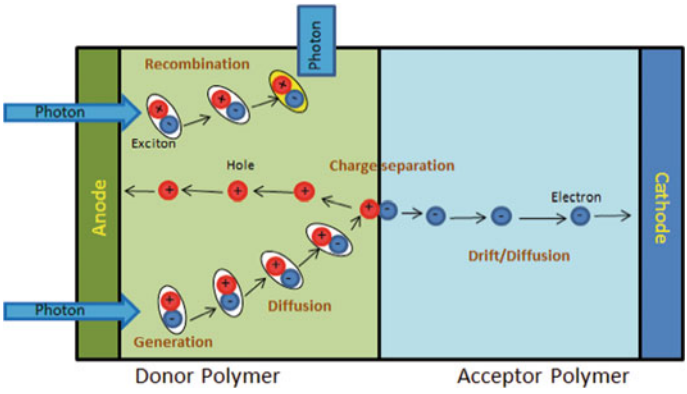

Fig. 4 Symbolic representation of the hardware structure of a polymer bulk-heterojunction solar cell [2]

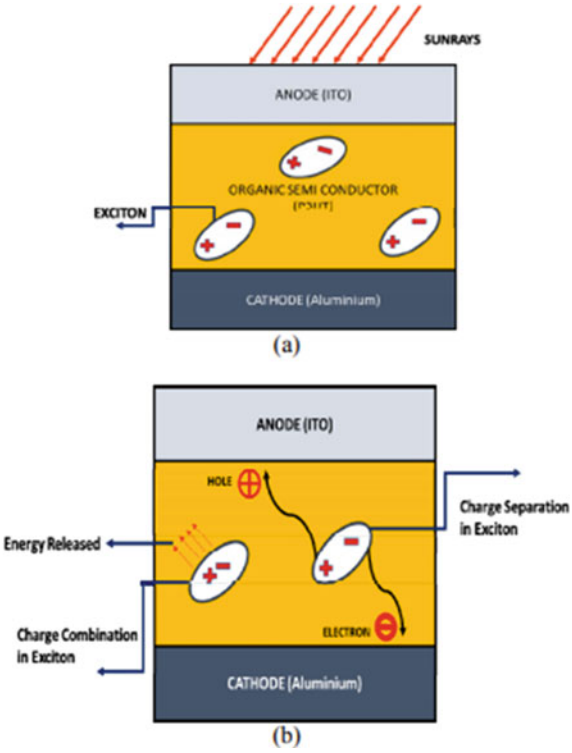

Fig. 5 **a**, **b** Single layer organic solar cell (OSC) with excitons and charge transportation respectively

graphical representation for the maximum power curve of the organic photovoltaic or OSC is as shown in Fig. 6.

The ratio of the $V_{MPP} \cdot I_{MPP}$ (the maximum power) and $V_{OC} \cdot I_{SC}$ is called the fill factor (FF), and hence, power output is written in the equation given below:

$$P_{OUT} = P \max = V_{OC} \cdot I_{SC} \cdot \mathrm{FF}$$

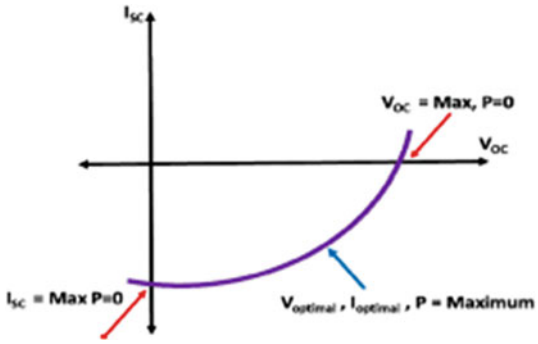

Fig. 6 Graphical representation for maximum power curve of OSC

Division for the output power by the incident light power resulting in the power efficiency as given in equation below:

$$\eta_{\text{power}} = \frac{P_{\text{OUT}}}{P_{\text{IN}}} = \frac{V_{\text{MPP}} I_{\text{MPP}}}{P_{\text{IN}}} = \frac{\text{FFI}_{\text{SC}} V_{\text{oc}}}{P_{\text{IN}}}$$

To move these charges and then the available photocurrent must be dependent on electric field, V_{oc} the is considered to be close to internal electric field and decreased for working in the extraction of the developed charge carriers that are less efficient, and leads to limitations for fill factor.

4 Conclusion

4.1 Applications, Environmental Impact, Current Situation of OSC

Applications
Organic solar cells are mostly used for personal mobile chargers and small electronic devices. These can be used by the soldiers in their defence equipment's like night vision cameras and GPS. Building integrated photovoltaic like blinder or window, building's exterior walls.

Environmental Impact
The energy consumption is low for manufacture of organic solar cell as it has less and thin layers. It is eco friendly to the environment as we use polymers for preparation. As we are making use of solar energy globally, the usage of non-renewable resources decreases.

Current Situation
The main aim is to improve the standards of organic solar cells by improving the nano scale morphology combination with the development of low band gap materials and hence expecting the efficiency to approach nearly 10%. The current international research in developing various methods and combinations to achieve low cost and high efficiency. Capable of producing the most economical organic photovoltaic cell is the adjective for coming generations.

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Autonomy Oriented Computation for Direct AC-AC Cascaded Boost Converter

Titas Kumar Nag, Avik Datta, and Pradip Kumar Sadhu

Abstract Techno-economic analysis of full/half bridge inverter-based domestic induction heating system is required to achieve low unit cost in near future. It may help to replace the existing liquid petroleum gas (LPG) system. This research focuses on techno-economic approach for direct AC-AC cascaded boost converter-based induction heating system. In order to achieve better efficiency, losses of the inverter should be minimized. There are several procedures to minimize the loss. In this research work, autonomy-oriented approach has been adapted to achieve the goal. Proposed computation technique is implemented on a direct AC-AC cascaded boost converter. The proposed computation technique could be a better techno-economic solution for better output power. A flowchart is prepared to minimize the converter losses.

Keywords Autonomy-oriented computation · Self-control strategy · Boost converter

1 Introduction

There are many advantages of induction heating [1] over the other traditional heating techniques that can provide faster heating and improved efficiency [2, 3], consistency, advanced process quality and safety. Faraday's law of induction is the main working principle of induction heating, and Joule's heating effect is the main cause of heat production in workpiece. Different inverter topology can be utilized to get the desired output. Switching losses can be minimized through zero voltage switching (ZVS) or zero current switching (ZCS) operations. In order to obtain improved efficiency, soft-switching techniques can be utilized [4–6]. Most preferable operating frequency for

T. K. Nag (✉) · A. Datta · P. K. Sadhu
Electrical Engineering Department, Indian Institute of Technology (ISM), Dhanbad 826004, India
e-mail: nag.titas@gmail.com

A. Datta
e-mail: avikdutta1985@gmail.com

P. K. Sadhu
e-mail: pradip@iitism.ac.in

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high-frequency inverter-based induction heating system is 15 kHz to approx 1 MHz. If losses are minimized, then the efficiency can achieve a good value. Losses can be controlled by implementing the self-control model strategy. Autonomy-oriented computation is a new approach to encounter the switching loss problem.

This research work consists of three major parts. First part provides the proposed circuit and its analysis followed by autonomy-oriented computation [7–15] approach. Third part of the work deals with the flowchart of the proposed computation methods.

2 Proposed Circuit and Analysis

Present research work focuses on techno-economic [16, 17] solution of cascade connection half bridge inverter-based induction heating system.

Proposed circuit diagram (Fig. 1).

Above-mentioned cascade connection of half bridge boost inverter circuit is working by the following procedure (Fig. 2).

With the activation of switch S_1 and S_3, the load current flows through the coil, and on other hand source, inductance is energized for boost operation.

Source inductance starts discharging through the DC-link capacitor C band, and at the same time, switch S_4 is turned on to maintain the continuous current conduction mode as shown in Fig. 3.

With the activation of switches S_2 and S_4, the load current flows through the coil, and on other hand source, inductance is energized for boost operation (Fig. 4).

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Source inductance starts discharging through the DC-link capacitor C band, and at the same time, switch S_3 is turned on to maintain the continuous current conduction mode as shown in Fig. 6.

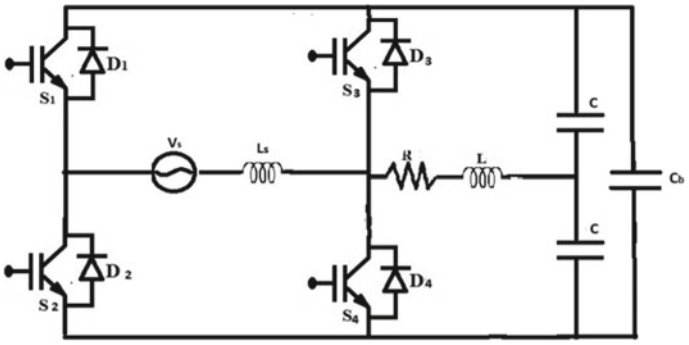

Fig. 1 Cascade connection of half bridge boost inverter

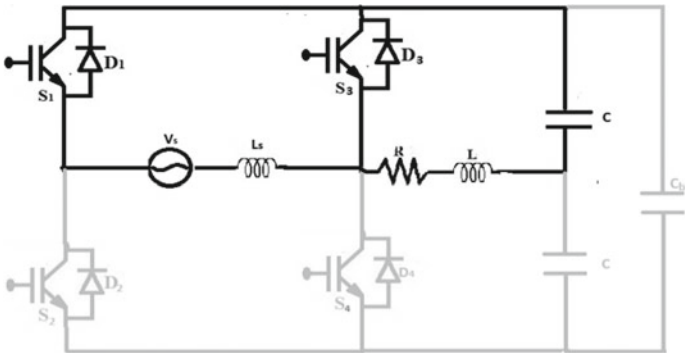

Fig. 2 Boost operation of upper part of circuit

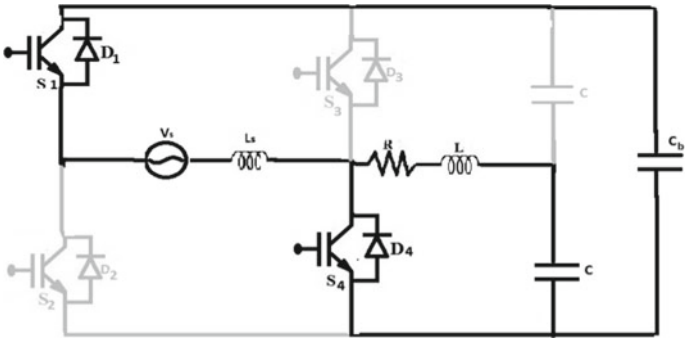

Fig. 3 Continuous current-conducting mode for upper circuit

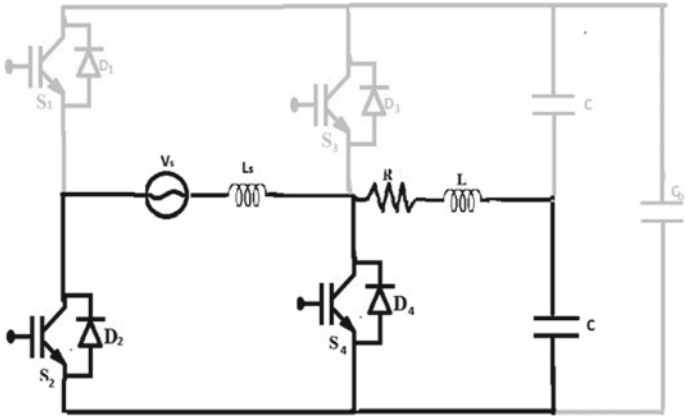

Fig. 4 Boost operation of lower part of circuit

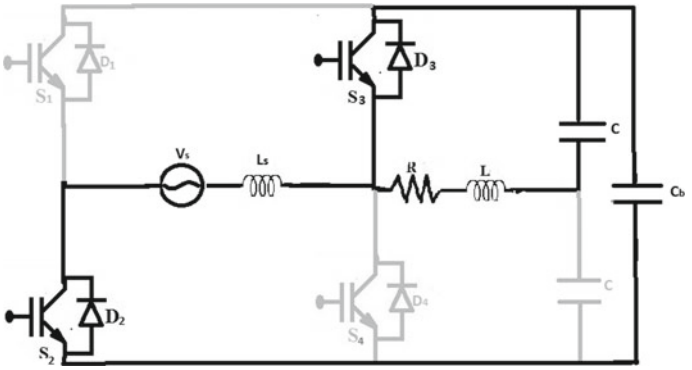

Fig. 5 Boost operation

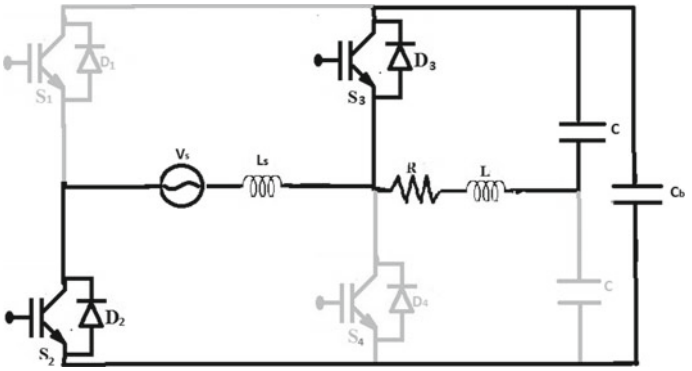

Fig. 6 Continuous current-conducting mode for lower circuit

2.1 Boost Equivalent Circuit Topology

The following circuit is a direct boost AC-AC circuit that creates high current through the load inductance to get higher efficiency. The losses of the converter can be minimized with the help of autonomy-oriented computation (Fig. 7).

3 Circuit Response

3.1 Specification Table

See Table 1.

Fig. 7 Boost circuit

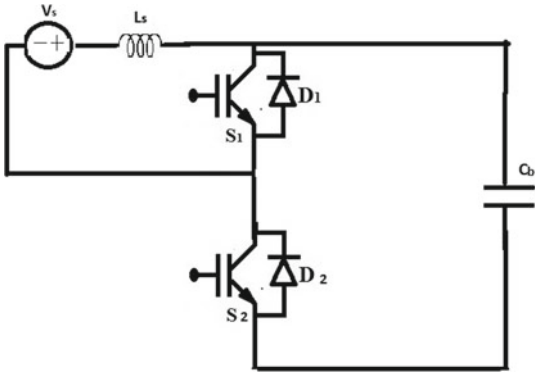

Table 1 Specification table

Items	Symbols	Values
Items	Symbols	Values
Load resistance	R	1 O
Load inductance	L	150 μH
Series capacitance	Cr	470 pF
DC-link capacitance	Cb	470 pF
Switching Frequency	FSW	80 kHz
Source voltage	VS	230 V
Source inductance	LS	500 pF

3.2 Load Output Current

See Fig. 8.

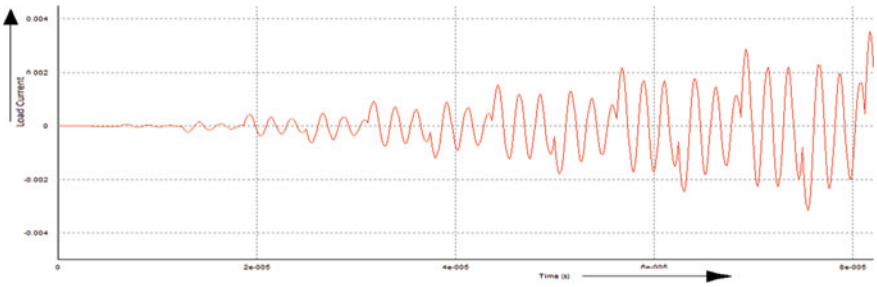

Fig. 8 Output current waveform

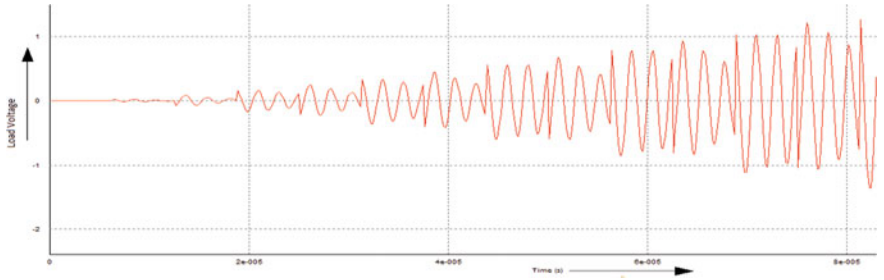

Fig. 9 Output voltage waveform

3.3 Load Voltage Output

See Fig. 9.

3.4 Boost Circuit Response

See Figs. 10, 11, and 12.

One of the big issues in the system is switching loss and input inductance loss. Figure 3 presents the load current waveform which is continuous mode of operation [18]. The average value of voltage across the inductor under steady state is zero [18], thus

$$V_{\mathrm{s}}\mathrm{DTSW} + (V_{\mathrm{s}} - V_{\mathrm{b}})(1 - D)T_{\mathrm{sw}}0 = 0 \tag{1}$$

The voltage ratio is the same as in a boost converter

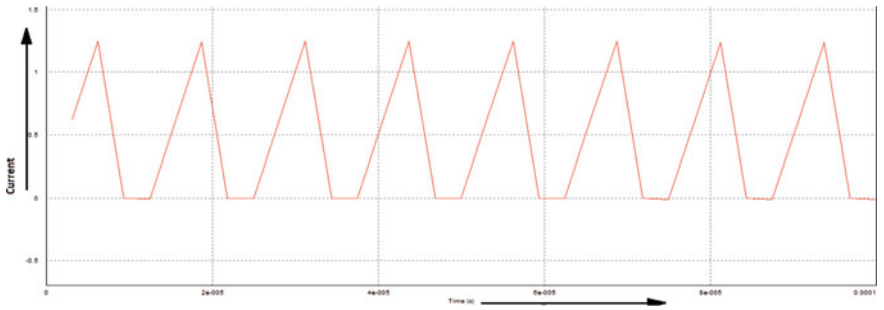

Fig. 10 Source inductance current versus time for boost equivalent circuit

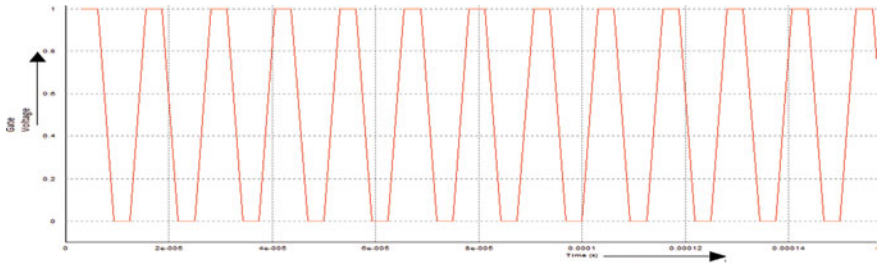

Fig. 11 Gate voltage for switch-1 for boost equivalent circuit

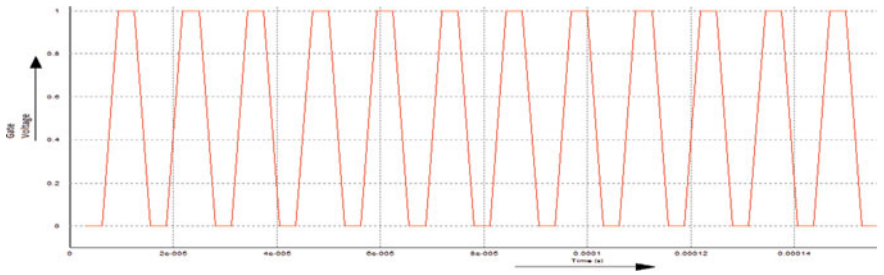

Fig. 12 Gate voltage for switch-2 for boost equivalent circuit

$$\frac{V_{\mathrm{b}}}{V_{\mathrm{S}}} = \frac{1}{1-D} \tag{2}$$

The waveform can be modified with the modification of ripple current

$$\Delta I_{\mathrm{s}} = I_{\mathrm{s,D}} - I_{\mathrm{s,O}} = \frac{V_{\mathrm{s}}}{L_{\mathrm{s}}} D T_{\mathrm{SW}} \tag{3}$$

If duty cycle is constant, then the conduction losses can be written as

$$P_{\mathrm{on,S}} = R_{\mathrm{on,S}} \left[\frac{P_{\mathrm{o}}}{R_{\mathrm{eq}}} + \left(I_{\mathrm{s}}^2 + \frac{(\Delta I)^2}{12} \right) + \frac{2}{T_{\mathrm{sw}}} \int_0^{T_{\mathrm{sw}}} i_{\mathrm{s}}(t) i_0(t) \mathrm{d}t \right] + v_{\mathrm{on,S}} I_{\mathrm{s}} \tag{4}$$

Input inductance losses

$$P_{\mathrm{on,L}} = R_{\mathrm{L,DC}} I_{\mathrm{s}}^2 + R_{\mathrm{L,AC}} \frac{1}{2} (\Delta I) 2 \tag{5}$$

Switching losses are defined as the function of the switching frequency and the turn off losses energy.

$$P_{SW} = f_{SW}\left(E_{off,H} + E_{off,L}\right) \tag{6}$$

The turn off current of switching devices.

$$I_C(t) = I_C\left(1 - \frac{\beta}{t_f}t\right), \left(0 \le t \le t_f\right)$$
$$I_C(t) = I_C(1-\beta)\left(1 - \frac{t - t_f}{t_f}\right), \left(t_f \le t \le t_{f+t_t}\right) \tag{7}$$

4 Autonomy-Oriented Computing (AOC) Approach

Autonomy-oriented computation [19] involves defining and deploying a system of **autonomous entities** that can directly or indirectly interact among themselves. The elements can be considered as subsystem as well.

Step-1:

- Identify the global objective that makes induction heating system [3] efficient, cost-effective, and technically accepted [20].
- Delimit the corresponding input and output as per the required efficiency level. The existing component and their energy loss need to be optimized. Switching loss and component loss need to be monitored [21].
- Inputs are connected with the local variables. They are identified by analyzing the local properties. Boost circuit and half bridge inverter are connected in cascade fashion. Here boost circuit is considered as the input to half bridge inverter. In this case, component count is reduced, and thus loss is minimized [22, 23]. Losses will be further minimized by using switching frequency and duty cycle.
- Output refers to the microscopic structure and/or behavioral patterns/characteristics, and those are dominated by the system level; that is, output current can be controlled by the implementation of self-control property [24]. In this case, ripple factor is the key parameter as it is presented in Eqs. (4) and (5). These two equations can control the total losses of the proposed circuit as shown in Fig. 1.

Step-2: (Modeling and Mapping)

- A model of local autonomy is composed of internally and/or externally triggered/influenced parameters. Operations begin with controlled behaviors of 'b' in set β that is duty cycle and switching frequency as mentioned in Eq. (3).
- Inverter model will be designed based on existing equations, and those are present in set$\{R\}$ where all equations will be utilized to create a proper rules.
- Entities have to evaluate their state and utilities using set F and u, that is, losses and output power.

- Observation of performance is required as per their selection behaviors 'b' in set β.
- If the result is not satisfactory, go to the previous steps.
- For unsatisfactorily results, we have to add some external operators like filter and series capacitor which have to be added as set 'O' to satisfied value of F and u.
- The evaluations and interactions will be considered for coupling relationship of entities that is Eqs. (4) and (5) which are depending upon ripple current (ΔI) of Eq. (3) will be considered as set 'C'.

Step for execution:

To get maximum efficiency and also cost-effectiveness of proposed circuit diagram, the following steps may be considered. These steps provide self-oriented computation method by individual entities based on their local autonomy:

1. Assess 'F' of curtain stage.
2. Behavioral rules in 'R' are applied.
3. Activate selection behaviors b for set 'β'.
4. Aggregate the effect of 'O'.
5. Adjust stages and utilizes 'u'.
6. If necessary adapt behavioral rules and control for parameter based on feedback of 'F' and 'u'.

5 Flowchart

In order to improve the self-adaptive nature of the system, some hybrid approaches can be introduced. In future, unsupervised learning technique which is known as self-organizing maps might be implemented to get a better result (Fig. 13).

6 Conclusion

Present research shows that the presentation of half bridge cascade connection results in the reduction of component count in the converter. As a consequence of this, losses are also reduced. The ripple current can be controlled by modifying the switching frequency and duty cycle. Autonomy-oriented computation method could be utilized to get a better output. An algorithm has been proposed to reduce the losses. This idea can be implemented for multizone inverter base induction heating system.

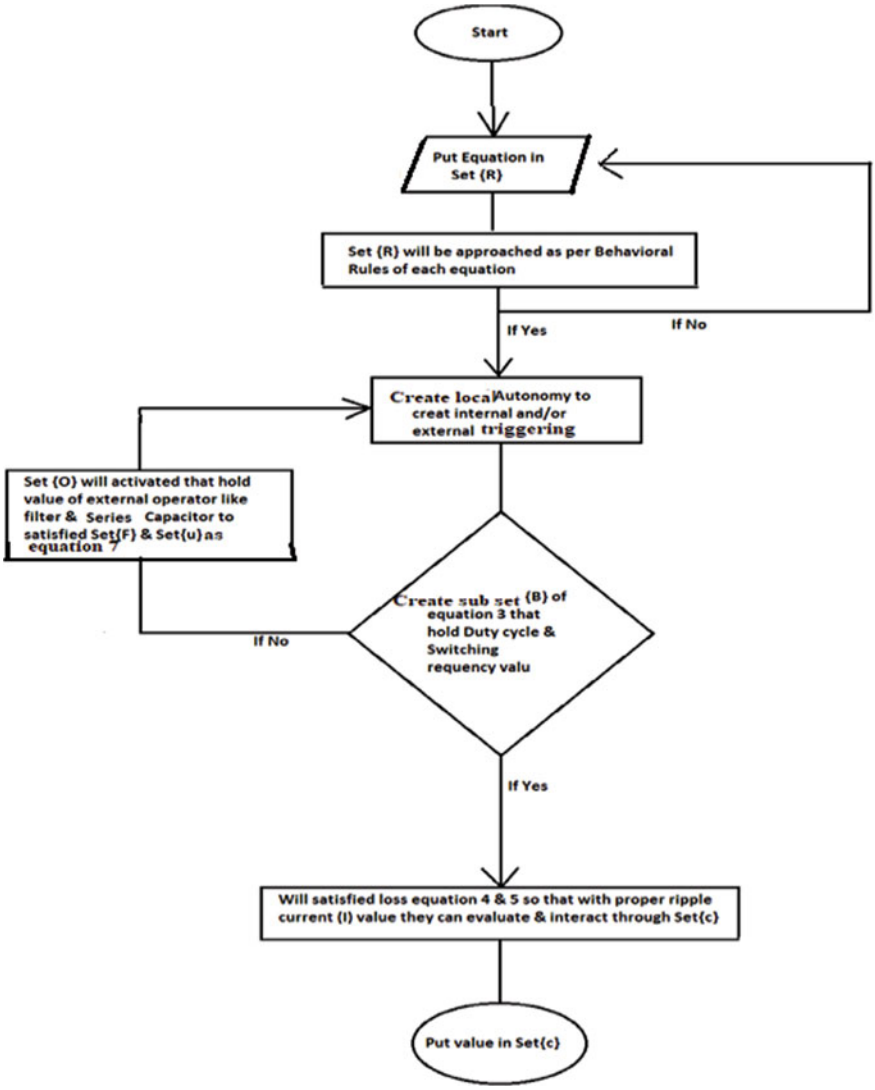

Fig. 13 Flowchart of algorithm

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Associative Array Architecture to Use Each Change of Series of Changes in Reversible Computing

Supriya Chakraborty and Ankit Deb

Abstract The energy-saving and quick computations are getting momentum among the researchers across the globe. Reversible computing pays significant contributions from architectural, instructional and logical perspectives in the literature. The present nature of data and complex applications involve many series of changes, however, past data are compared for decision making or backtracking to draw the inference. In this regard, dynamic dispatch with the lexical scoping was combined to access the series of changes that were most recent advancement. However, the loosely coupled data structure is the fundamental drawback to achieve the advantages of reversible computing in all directions. In this work, architecture is proposed that uses the novel associative array in the underlying combination of dynamic dispatch with lexicographic scope. The solution is abstracted as a memory management scheme. The procedural and object orientation paradigm could use such proposed architecture in the programming level. The advancement of the proposed work is supported with results.

Keywords Associative array · Register · Logical · Build time · Series of changes · Complex application

1 Introduction

In recent days, reversible computation is getting the attention of the researchers. In the entire history of computing, the loss of information and generation of heat (energy) in the series computations observed. The real concern of the future market is the energy-efficient computations on behalf of global concern against the mammoth energy exhaust for computing across the globe. This writ in the subsequent paragraphs illustrates the specific technical gaps of reversing the series of computations and provides an efficient solution in the successive section.

S. Chakraborty (✉) · A. Deb
AMITY University, Kolkata, India
e-mail: schakraborty5@kol.amity.edu

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Janus, procedural language thoroughly discusses the notion of reversible computation in [1, 2]. Joule made the advancement [3] by incorporating object-oriented language features for reversible computing. However, the Joule traditionally depends on compiler-generated dispatch method to achieve reversibility.

Many related but different works have observed with their specific purpose and scopes in the field of reversible computing. [4] has attempted to extend the object-oriented language features in reversible machines. The advantages of object-oriented features have already realized as best practices in Industry for the past few years. However, a related work, Taffoli network is space-inefficient for irreversible function [5]. In this work, a simple space-efficient method has proposed with the extension of object-oriented features for reversing the computation. There is always a challenge for the system that demands irreversibility; however, the reversible function does not exist for the purpose.

In this regard, two closest work [6] that describes the complete description of the semantics of reversible object-oriented programming language and [4] that attempted dynamic dispatch method using virtual method to achieve reversibility. Broadly, the virtual method call consists of three steps—Lookup, Jump and Cleanup. However, reversibility is not persistent and the use of program stack limits the flexibility of the language, the series of changes are out of the scope of [4].

In this work, the extension of PISA [4] has proposed by introducing a hypothetical heap memory on top of the object instance. The physical size of the heap memory is subject to number of fields in the object. A default value for each field is considered in this work.

This writ organized as follows. The paper starts with a brief description of the problems and challenges regarding reversible computing. The problem space has been elaborated with a summary of the previous works in the Introduction section In this section, the specific shortcomings have been identified and technical extension over the related work has been specifically mentioned. The proposed methodology has discussed in detail with diagrams in Sect. 2 and its sub-sections. The proposed claim has justified with the experimental details and results set in Sect. 3. A conclusion has drawn in Sect. 4. This paper has ended with the reference section.

2 Related Work

Pendulum Instruction Set (PISA) is an instruction set for reversible computing. The architecture is the modification of a cross between RISC and PDP-8 machines to support reversibility. The notion is also to support energy efficiency computations. The list operations are Add, Add Immediate, And Immediate, And-XOR, Branch or Equal to Zero, Branch or Less Than Zero, Exchange, Or Immediate-XOR, Or XOR, Reverse Direction- Branch On Equal to Zero, Reverse Direction- Branch On Less Than Zero, Rotate left, Rotate Right, Shift Left Logical-XOR, Shift Right Arithmetic XOR, Exclusive OR, XOR Immediate. The authenticate syntax and usage are available in [7].

The objective of the reversible computing is to support logical reversibility of operations and be implemented in a physically reversible technology. Freedkin [8] demonstrated that billiard ball collisions are capable of simulating any logic function.

Energy recovering integrated circuit technique, e.g. Split-level charge recovery logic reduces power consumption in logic circuits.

The Pendulum processor is based on the MIPS R2000. MIPS R2000 lets the mapping between instruction set architecture and register transfer level functional architecture. The primitive model executes the instruction in five cycles where each cycle resembles an appropriate pipeline stage. Two are dedicated to instruction fetch and decode, while the three remaining stages perform register access, operation execution or memory access and register write back. Processor direction is controlled by an external signal. The signal is synchronized with instruction execution so that the currently executing instruction completes execution before the processor direction is changed.

Read/Read^{-1} and Write/Write^{-1} imply the Pendulum register file and its connection. Copying information from one location to another involves losing the information, which was stored at the destination. Reading and writing information is therefore done as a swap. Reading from a memory location clears it, and only memory locations, which are clear, maybe written to. This suggests that the inverse of the reading a value, and the inverse of writing value is reading a value.

3 Associative Array Architecture

In a broader sense, two types of approaches have been summarized for reversibility. In the first approach, the right-hand side is never reversible for expression if the left-hand side is dependent on the right-hand side [9]. The further restrictions in the variant of Janus also do exist, one variable is passed to only one parameter during function call, and class field is not possible to pass in the method call of the same class. The major reason, the compiler does the simple compile-time analysis and detection for reversibility.

In contrast to the above approach is the continuous checking for updating variables on run time. The continuous checking is very time consuming, the slightly better approach is the period checking. Still, the threshold value for the period is subject to determination and accuracy is in question for all the changes. In this regard, a complete different thing is that compiler does not check the variable at run time if it detects early that the update is irreversible.

To achieve the reversibility, object uses lexical scoping for class fields; such lexical scoping implies that the object fields would create in program stack, but not in the reversible heap memory.

3.1 Memory Management

The proposed method extends the memory usage in PISA to use the reversible heap memory. The constraint is that the proposed method is not applicable for objects when created in system stack. When an object instance is called, instance is created in memory heap, and a corresponding memory heap is also created hypothetically on top of the object. Initially, such memory heap would be filled by zero to conform to the rule, no unused memory contains non-zero value [10]. In this work, an associative array structure is proposed to contain the series of changes; such an associative array structure is possible for both hardware and software (logical). In this section, we present the concept in terms of logical implementation. The memory is assumed to be created just top of the data to accommodate the associative array into working memory. The memory representation of the memory structure is specified in Fig. 1. The associative memory contains the list of operations that is applied on data v in the first level of the array. In the second level, the series of changed values are contained.

Initially, the hash function is applied to reach to each operation. If the same operation is applied multiple times, a time probed from the system clock is appended with each operation to make applicable the hash function.

The challenge is to make optimize policy for the dynamic growth of the associative array [11–19]. Several possible solutions exist. Few of them are described below:

- *Double the size*—This is a completely logical scheme. The size of the associative array can hold eight values. After exhausting the space, the growth of the associative array will be doubled. The run time environment of the Instruction Set manages such growth.
- *Physical Implementation*—Eight registers are internal could be used to accommodate changes. After exhausting the space, the changed values are copied to the logical unit of the associative array, and the registers are ready to handle the recent changes. The size of the associative array grows with the multiple of eight. The logical array works as a virtual unit of the physical registers of the associative array. The schematic diagram of the scheme is depicted in Fig. 2.

In accordance with the scope of the application, operations could be substituted by values. However, it is strongly recommended that either a very small dataset is chosen for the first-level associative array or each value must be unique. The result section shows that this scheme is best suited for both the above situations. However,

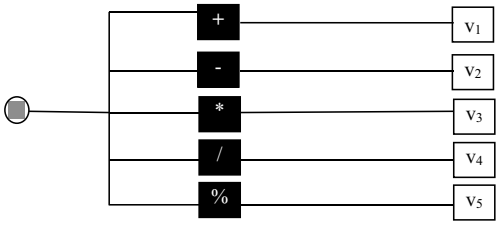

Fig. 1 The heap memory location of the object

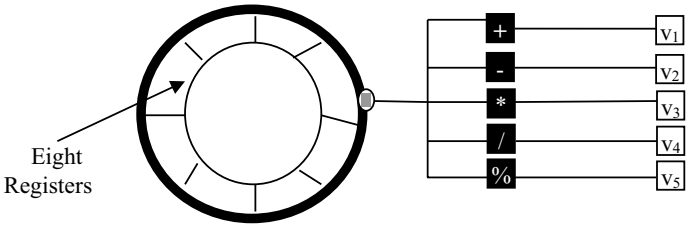

Fig. 2 The interfacing between registers and logical unit in case of overflow of changes in registers

results are degraded in other cases. In the subsequent paragraphs, the operations of PISA are discussed to support the proposed scheme.

Each change contains the previous image of the update operation of the field of the object. The previous image consists of V_i implies the value and t_j imply the timestamp on which the update operation is occurred. If the system does not require reversing the operation without any time constraint, the t_i could be omitted. For each update operation, the previous image is inserted to the top of the list and points to its immediate next node. The order of node implies the order of changes for the field of object. The list has maintained by header node *ObjectName.Fieldname*. This *Objectame.Fieldname* simply identifies the object and the corresponding field that has changed in series during the lifetime of the object within heap memory. It is true that the object name must be unique in the environment to maintain the consistency of reversibility. *ObjectName.Fieldname* refers to the latest value that has changed in the field of the object.

In PISA, the following operations are documented to update the variable:

$$++, -, <==>, +=, -=, =, <->$$

For a detail description of each operation, please refer [20]. In object-oriented paradigm, the field of the object would be refereed with the following syntax:

ObjectName.FieldName

The each PISA operation could be used after syntax *ObjectName.FieldName* to apply the changes.

3.2 Extended Operations and Code Generation

The field of the object as referred simply by adding the offset with the base address of the object. Such object-oriented syntax with the above-enlisted operations are lexically determined the chance of update in the compilation time. In such cases, the compiler generates the following extension code:

```
-----------------------------------------------------------------
CREATENODE          Node_i
ASSIGN Node_i    Node_i-1
ASSIGN ObjectName.FiledNameIdentifier Node_i
MOVELOC ObjectName.Fieldname Node_i
…..
……
MOVEREG   reg   ObjectName.FieldName
-----------------------------------------------------------------
```

To execute the operation, the following statements have been proposed that extend the language PISA [20, 21] and translation schema from Jenus to PISA [10].

The *MOVEREG*, *MOVELOC* are already defined as primitive operations in *PISA*. The following two operations are advised to be included in the PISA instruction list:

- CREATENODE and
- ASSIGN.

The proposed operation *CREATENODE* crates one new node in the heap memory following the data structure in Fig. 2. *ASSIGN* operation provides old value to the newly created node and adjusts the reference that refers to the newly created node by the header node *ObjectName.Fieldname*. The change that affects the existing list is as the old node $NODE_i$ becomes node $Node_{i-1}$ in the list.

ObjectName.Fieldname and *ObjectName.FieldName* are different things. The first one is the header that maintains the series of changes in heap memory whenas the second one is the reference to the object in the working memory.

3.3 Persistence of Old Image

In the documentation of PISA, instruction is not enlisted to store the values persistently. The history of changes that are stored in the top of the object memory could be persistently stored using the integration with the *R* compiler. The modern R package reader is fast and provides both a wide range of file formats and functions to store values persistently. The *R* compiler translates the *R* source code into assembly code of PISA.

4 Experiment and Results

A simulation with the proposed techniques has done to generate the result with the following characteristics:

Transistor density 180×10^6 transistor/cm^2
Chip Size before subsequent shrinks 750 nm^2

On chip local Clock Frequency 10 GHz
Supply Voltage for Minimum Logic power 0.6–0.5
Maximum power consumption for high-performance processor with heat sink 75 W
μP drawn channel length 35 nm
DRAM ½ pitch 50 nm
T_{ox} equivalent < 1 nm
CV/I delay 3–4 ps
VT 3σ varia. 40 ± mV
Src./drn. Junction depth 10–20 nm

The above values have used to examine the reversibility of the experiment enlisted in Table 1. The column attribute of Table 1 enlisted the details of the experiments and adjacent columns contain the corresponding number.

Result of the experiments has depicted in Fig. 3.

Reversibility with series of changes has achieved. In the simulation, the heap memory for the reversibility has created in multiple of 512 KB. The determination of the size of heap memory for reversibility at compilation time is possible only approximately. Figure 3 shows the reversible time consumes less time with the increase number of updates. In accordance with the exhaustive number (400) update operations as an average of 33.33% of time decreased for reversibility.

The access result of different schemes (Logical and Register) following three scenarios are depicted in Fig. 4:

- The first-level operations are small comparing over large dataset,
- The first-level operations are large enough but unique,
- The first-level operations are large enough but not unique.

Table 1 Details of the experiment

Attributes	Number			
Number of objects	5	10	15	20
Existing number of fields	15	30	45	60
Number of update in the same field	5	10	15	20
Number of update in total number of fields	25	100	225	400

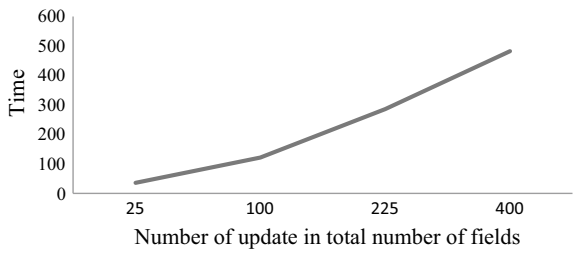

Fig. 3 Reversible time in ms against the number of update in total number of fields

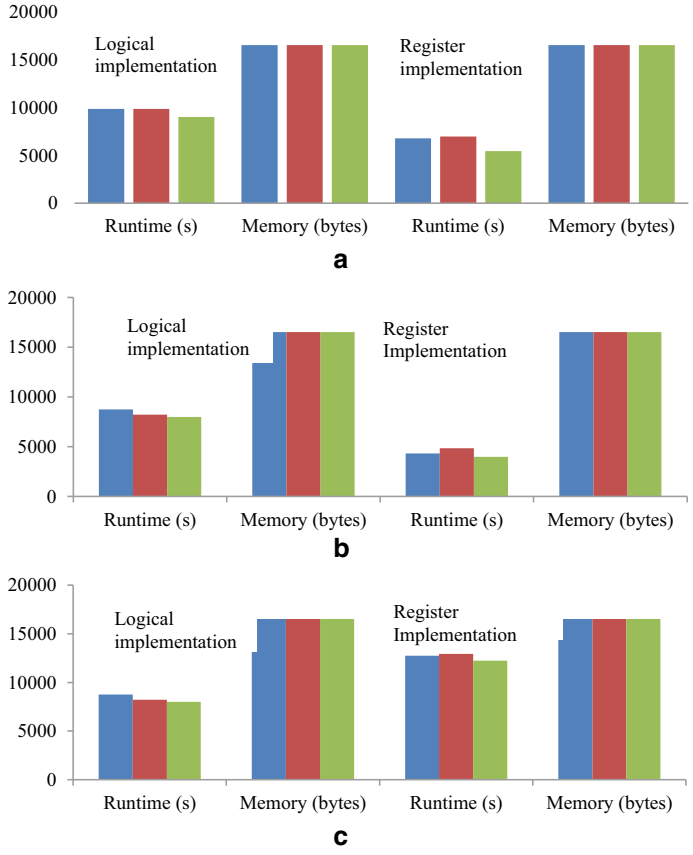

Fig. 4 **a** The runtime performance comparison for small set of operations (8) between logical and register implementation on 541,450,384 Bytes with 32,768 changes. **b**. The runtime performance comparison for large set of unique operations (1000) between logical and register implementation on 541,450,384 Bytes with 32,768 changes. **c**. The runtime performance comparison for large set of redundant operations between Logical and Register Implementation on 541,450,384 Bytes with 32,768 changes

For each test, three run times have been tested and shown in different colors. The data set size remains the same, only synthetically design according to the requirement of the above three scenarios.

The build time of the associative array is a major constraint. The choice between logical or register implementation is dependent on the performance requirement of the application and the scenarios mentioned above. A build time (s) on the same set of data is depicted in Fig. 5.

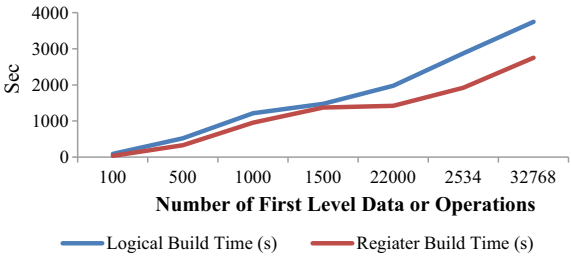

Fig. 5 The build time comparison between logical- and register-based associative array

5 Conclusion

The associative array implementation outperforms the performance requirement for a series of changes on large data set. The choice of implementation of the associative array is dependent on the scenario and performance requirement of the application. For the unique set and small set of operations, register implementation is 60% better in performance over logical whereas for non-unique large set of operations the performance of register implementation degraded substantially over logical implementation.

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Smart Grid Initiatives in India

Thumma Saritha Kumari, K. Anil Kumar Reddy, P. Avinash, M. Pavan, and A. Balakrishna

Abstract About 3.4% of worldwide energy utilization is taking place in India, a better way of serving energy needs with an increase in reliability and decrease in gap between demand and supply is very important. To meet those conditions and enable the unification the information communication technology and renewable energy sources, India has to restructure its energy distributing structure. Smart grid, i.e., the renovation of the power grid is a developing combination of different technologies planned at submitting an extreme change in the electricity grid. The segments of automated grid and its necessity in the Indian situation have been examined. This work encloses for accelerating the smart grid formation, and many facilitator projects introduced by the Government of India. Further, a complete assessment of Indian grid automation motivation and adventures is presented. Further for smart grid formation, the potential barriers and solutions are analyzed. This paper emphasizes the automation of the present power grid for producing assured and clean energy.

Keywords Renewable energy sources · Indian smart grid · Smart grid projects

T. S. Kumari (✉) · K. A. K. Reddy · P. Avinash · M. Pavan · A. Balakrishna
Department of Electrical and Electronics Engineering, Institute of Aeronautical Engineering, Hyderabad 500043, India
e-mail: tmsaritha@gmail.com

K. A. K. Reddy
e-mail: anilkatam143@gmail.com

P. Avinash
e-mail: avinashchintu09@gmail.com

M. Pavan
e-mail: pavanraja.m2030@gmail.com

A. Balakrishna
e-mail: aalebalakrishna910@gmail.com

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1 Introduction

At present today, our country India is the world's 6th largest energy consumer. It had recently experienced at an average of 3.6 percent per year over the last 30 years, the growth and demand rate for energy. By the year 2030, in India the total demand for power is guessed to be cross 9, 50,000 MW. The factors which determine the need for smart grid over power grid are:

- There is a very high change in supplying power and demand required.
- Huge losses in transmission and distribution systems.
- Lack of knowledge on the usage of advanced technology.

Present and Past Indian Power Grid:

In the year 1897, the first electric supply in India was taken place with 130 kw hydroelectric power station around Darjeeling. In 1899, the earliest thermal power station was planted by the Calcutta Electric supply corporation in India. During the period from 1920 to 1940 due to the increase of development in usage of technology in industries, the power field became strong and at the end of 1940 the total installed capacity reached to almost 1250 MW. During the period from 1930 to 1934, first interconnection of grid system is the Ganga Canal grid came into existence in India. As of now the grid system of India is divided based on regional basis which are Northern Grid, Eastern Grid, Western Grid, North Eastern Grid, Southern Grid.

2 Smart Grid

Smart grid is an electric grid which includes sensors, smart meters, digital communication, advance technology, automatic controls, and renewable power sources are used to increase constancy and efficiency of power grid. The power flow earlier concept was primarily one-way in character, i.e., electrical power is produced at generating plants and dispatched to the consumers. Depending on the required load demand, the generating stations work to generate the required electrical energy. The government relished a supremacy over energy sector all components, viz. generating, transmitting, distributing, trading the power, etc. With the arrival of the renovation of keep going technologies and novelties, the distributing system "the grid," the biggest human-created engineering wonder of the twentieth century has also undertaken and still undergo restructuring creating it more strong, stable, and smart, hence the name "smart grid." The automated grid is the brilliant integration of generation, transmission, distribution to effectively dispatch feasible, assured and affordable electrical power. It allows many brilliant and automated uses such as smart grids [1, 2], smart metering infrastructure, response of demand, management of advanced distribution [3], energy storage in intellectual way [4, 5], smart power marketing [6, 7], and integration of electrified vehicles [8, 9]. Due to progress in the unification of distributed power sources especially non-conventional power resources, the flow of

power is elegant multi-directional, i.e., generation of power is not centralized. The customers are also dynamically partaking in the organization of electricity. They are intimated and have options, incentives, and disincentives which alter their electrical power buying figure and behavior [10]. These choices were ruling the arrival of modern technologies and markets. The power sector of central government is noticing big-scale private involvement, thereby rising ambitiousness, liability, and duty.

2.1 The Characteristics of a Smart Grid

1. Safe and Reliable: When compared with present electric grid, the automated grid system is very safer and added trustworthy. Also, least are the losses.
2. Efficient and Economical: Through the policy inventiveness and the efficiency of energy, and market ambitiousness, the automated grid is able to upgrade the settlement economically. To give balanced allocations of resource, power network is more supported. With the electricity market, it stops power deals effectively to minimize energy loss and increases system productivity.
3. Hygienic and Verdant: The smart grid system is very much hygienic and green, and it works in superior working situation. And this system is nature amiable.
4. Optimization: This system provides very much suitable price of electrical power to the society. It enhances utilization resources, which reduces cost of investment. This system also minimizes the maintenance and operation costs.
5. Self-healing: Self-healing is the main feature of smart grid. This is used to enhance the quality services, increase reliability, and minimize costs. It discovers the fault.
6. Flexible and Consistent: It can be assisted right, suitable union of the renewable power resource, and it is the relevant for the mixture of the distributed generation and the electric grid. Besides, it can upgrade and progress the tasks of the management to achieve the productive association abilities with the consumers. It is amiable with the existing power grid also.
7. Integrated: It offers Guinness program, and design is implemented on the grid. This system can be secured high-caliber of composition and data gives out to the electric grid and is attained the standard, prescriptive and treats management that unifies framework. In this systems, like wind energy, solar power, PV cell are assimilated in the system. It is more productive and also money-making.

2.2 The Advantages of Smart Grid to Indian Power Sector (in Terms of)

- Economics:

Table 1 Benefits of smart grid when compared to normal power grid

Characteristic	Power grid	Smart grid
Self-healing capacity	No	Yes
Flexible to attacks	Vulnerable	Flexible
Quality of power	Less quality	Good quality
Meeting increasing demand	May not reach	It meets the increasing demand
Communicating process	By one way	By two way

  - Because of the reduction in peak load, economy in cost.
  - Lowered maintenance and operational cost.
  - Decreased cost to industrial consumers.

- Services:
  - Progress in the reliability of electrical supply.
  - Improvement in quality of power.
  - In the transmission, aggregate technical and commercial (AT and C) losses reduction [11].
  - Transmitting of power is efficient.
  - Security of grid is improved.
  - Management of man intercession in power grid.

- Environmental:
  - Deduction in greenhouse effect and CO_2 emission.
  - Improve perforation of non-conventional sources depend on hygienic power.
  - Consumer involvement in power supervision (Table 1).

The five important technical areas of a smart grid are:

- Integrated communication technology.
- Measurement and sensing technology.
- Advancement of power electronic components.
- Advancement of protection.
- Improvement in decision.

3 Initiatives of Smart Grid in India

Power grid systems in India are having problems like ineffective procedure, insufficient production, less quality of power. Government of India has announced the Indian Electricity Act (IAE) in 2003 and programs like Accelerated Power Development and Reforms Program (APDRP) due to the increase of power usage. It is must

to change to smart grid to achieve the present and future demand of power. Hence, there is much need to identify and start implementing this smart grid system to make the power grid sector strong.

Types of inventive to reform 100 existing cities into smart in 2010, taken by the Government of India (GoI) at nationwide as well as domestic level are:

3.1 Indian Smart Grid Task Force (ISGTF)

- Creating awareness on different smart grid activities.
- Developing centers like R&D in the related technology.

Indian smart grid task force formed five types of groups—they are:

- Educating and training of new technology.
- Decreasing the losses.
- Equal power distribution.
- Installation of distributed Generations.

3.2 Indian Smart Grid Forum (ISGF)

Government of India introduced a public and private partnership called Indian Smart Grid Forum in order to develop smart grid technology in the country. ISGF mainly introduced to attain the important requirements of industry for implementing a good and strong smart grid in the country.

ISGF main objectives are:

- Helping Indian power grid sector to introduce the technologies of smart grid in a well-organized way.
- Regulations should be bought for smart grid.
- Conducting research on the availabilities of smart grids centers in the Indian using case studies and conducting experiments.

3.3 BESCOM Project

One of the Indian's leading distribution companies is Bangalore Electric Supply Company (BESCOM) the colonist in the area of the distribution computerization. BESCOM is functioning on an automated grid forecast in the field of electric city. This is one of the best examples of industrial communication of smart grid. Hence, the implementation of distribution automation in the green city Bangalore will improve the quality of power. The estimation of this project is Rs.563 Cr. Hence to achieve

this in Bangalore City seeking the financial support from the Japan International Cooperation Agency (JICA) of Rs. 417 Cr for this project.

The main objectives of BESCOM Project are:

- Providing assured quality power supply.
- Improving the quality of service management and satisfying the customer.

Apart from projects of smart cities, GoI has demanded below programs for the continuation of the smart grid as the equipping framework:

- Ceaseless electric supply.
- By 2022, with 100 GW from solar a total renewable energy of 175 GW.
- Transport system entire electrification as a target by 2030, National Mission on electric Mobility.
- Within the next four years, 35 million smart meters.
- By 2030, from renewable sources generating 40% of electricity.
- Under the scheme of Atal Mission for Rejuvenation and Urban Transformation (AMRUT), renewal of 500 towns.

Below programs of GoI are in accomplishment level focusing to update the power grid.

R-APDRP (Restructured Accelerated Power Development and Reforms Program): This scheme was commenced in 2008 with the intension to minimize AT&C losses and with sanctioned cost of Rs 51,577 crores, to equip the services with information and communications technology (ICT). It has two parts A and B.

Part A deals with the arrangement of baseline data for the project location including, indexing of consumer, automatic data logging, and metering of distribution feeders and transformers. Out of 1405, approved 1356 towns have already finished work in Part A.

Part B necessitates remodel, modernization, and boosting the distributing network. Out of 1227, the 863 towns have so far boosted their urban distributing network [12].

This scheme is now mixed with IPDS.

Integrated Power Development Scheme (IPDS): It was started in 2015, this program is attentive on the intensifying of sub-transmission and distribution system, upgrading of the metering system and assimilation of ICT in the distributing system. With Rs 48,081 crore support from GoI, total cost to accomplish this program is around at Rs 76,623 crores. Till date, Rs 25,913 crores have been sanctioned [13].

Ujjwal Discom Assurance Yojana (UDAY): In 2015, the GoI introduced the UDAY program for economical reconstructing and accomplishment improvement of power distributing organizations (DISCOMs). This program emphasizes on rising running productivity. It also invites to increase 'last-mile' transmission and distribution, removing the imbalance in the middle of revenue collection average and the purchasing average cost by 2018–19 [14].

Deen Dayal Upadhyaya Gram Jyoti Yojana (DDUGJY): With Rs 75,600 crores budget, for rural electrification it was started in 2015 by GoI. Under this program, to

electrify 5,97,464 non-electrified villages and give free electricity services to 397.45 lakh BPL rural households, GoI has permitted 921 projects. 594,159 villages (99.4%) have been electrified till date [15].

Energy Efficiency Services Limited (EESL): Under the Ministry of Power, GoI, EESL started in 2015, an undertaking of public sector undertaking (PSU) promotes accomplishment of energy productivity projects. LED bulbs of 25.61 crores, energy-efficient ceiling fans of 11.64 lakh, and LED tube lights of 30.85 lakh are distributed and lakh street lights modernized with LED lights under EESL [16].

4 Smart Grid Projects in India

For assessing the viability of automated grid and for discovering many challenges in accomplishing automated grid in India, the GoI has sanctioned in different states 14 pilot projects in 2012. In these 14 projects, canceled projects were two (Baramati, Jaipur). Further, in 2014 project of one more in Kanpur and in Manesar one resource center the GoI launched.

In 2016, (NSGM) National Smart Grid Mission was started by GoI, under that pilot smart grid projects of 4 were began. And 4 more projects sanctioned under NSGM in 2018.

Other projects have been started by GoI apart from above pilot projects in Odisha, Bangalore, Chhatarpur, Delhi, Kolkata, etc. (Tables 2 and 3).

5 Potential Barriers and Solutions

In India, the obstacles in accomplishing automation of grid are enormous losses in transmitting network, fluctuations in voltage, persistent collapse in rural and semi-urban areas, interruptions in urban areas, electricity supply lack. The main obstacles can be mentioned as:

- No chances of commercial feasibility for countrywide automated grid accomplishment.
- For automated grid deployment, national road map is non-coordinated.
- For state-owned power companies, poor financial condition.
- Not-sufficient skill and knowledgably persons to operate new equipments, new communication technologies, new systems.
- Remarkable capital costs.

Tremendous technical and economical investments compel the accomplishment of automated grid, considering into view the various requirements of the utilities, regulatory circumstances, power sources, and present system. To control the obstacles

Table 2 Status of active smart grid pilot projects

S. No.	Utility name	Area	Functionalities	Consumers	Present status [17]
1	IIT Kanpur Smart City	Kanpur–Uttar Pradesh	AMI,SCADA, DG, HAS	–	Project completed
2	CESC, Karnataka	Mysore–Karnataka	AMI, OMS, PLM, MG/DG	21,824	Project completed
3	UHBVN, Haryana	Panipat–Haryana	AMI, PLM, OMS	10,188	Project completed
4	Smart grid resource center, Manesar	Manesar–Haryana	AMI, OMS, MG/DG, EV with charging infrastructure	–	Project completed
5	HPSEB, Himachal Pradesh	Kala Amb Industrial Area–Himachal Pradesh	AMI-I, OMS, PLM,PQ	1335	Project completed
6	UGVCL, Gujarat	Naroda–Gujarat	AMI, OMS, PLM, PQ	22,230	Project completed
7	PED, Puducherry	Division 1 of Puducherry	AMI	33,499	Project approved on 28.12.2018 Completed the site survey. Smart meters testing and certification is done. Approved the DRS and FAT. Control centre is under construction
8	WBSEDCL, West Bengal	Siliguri Town–West Bengal	AMI, PLM	5265	Project approved on 31.12.2018 Completed the site survey. Smart meters DRS and DCU sanctioned. Control center DRS under review. 1000 smart meters FAT finished

(continued)

Table 2 (continued)

S. No.	Utility name	Area	Functionalities	Consumers	Present status [17]
9	TSECL, Tripura	Electrical Division No.1, Agartala–Tripura	AMI, PLM	45,290	Project approved on 30.06.2019 Smart meters of 10,085, DCUs of 95 located and authorized MDM and control center are functioning. Assimilation with R- APDRP incomplete
10	TSSPDCL, Telangana	Jeedimetla Industrial Area–Telangana	AMI, PLM, OMS, PQ	11,906	Project approved on 30.03.2019 Field survey of this is completed. For proof of concept study 28 smart meters (20 single-phase, 6 three-phase, 2 CT) placed
11	APDCL, Assam	Guwahati Division–Assam	AMI-R, AMI-I, OMS, PLM, PQ, DG	14,519	Project approved on 02.05.2019 with AMI
12	AVVNL, Ajmer	Ajmer City, Rajasthan	AMI	1000	Project under implementation

in automated grid deployment, few solutions for Government of India are given below:

- Technical assistance to utilities and commercial businesses in terms of investigation, education, and shared experiences.
- Safety and confidential computes in addition of ability to hold huge data.
- Improved perception and acceptance in the consumers outlaying the benefits of approval of automated grid.
- Full and planned national road map for automated grid accomplishment addressing concerns of both state and private players.
- Sponsorship to state services and application of fine for non-performance.

Table 3 Status of NSGM smart grid projects

S. No.	Utility name	Area	Functionalities	Consumers	Present status [17]
1	CED, Chandigarh	Sub-Division 5 of Chandigarh	AMI, DTMU, SCADA	29,433	50 smart meters installed in field. Second lot of 5000 smart meters dispatched. HES and MDMS integration are under progress
2	JBVNL, Jharkhand	Ranchi–Jharkhand	AMI, DT monitoring	3.6 lakh	Bid evaluation completed. Approval under process for award
3	OPTCL, Odisha	Rourkela–Odisha	AMI, DT monitoring, Substation Automation	0.87 lakh	Utility decided to drop the implementation of SCADA till overlapping of scope of works under ongoing schemes is ascertained
4	CED, Chandigarh	Complete city–Chandigarh	AMI, DT monitoring, substation automation	1.84 lakh	Approval under process at MHA for balance 70% funding arrangement
5	JVVNL, Rajasthan	6 Urban Towns	AMI	1.5 lakh	Sanction letter issued on 10.01.2020
6	KSEB, Kerala	Kochi–Kerala	AMI, PLM, DT monitoring, EV with charging infrastructure, PV	0.9 lakh	Project cancelation letter issued on 13.01.2020 and utility confirmation received on 21.1.2020

Abbreviations
DG distribution generation; *MG* micro-grid; *DCU* data concentration unit

6 Conclusion

The demand for electricity running ahead of supply because need for it in India has grown enormously. The country's plan to supply steadfast and economical power supply, to meet these challenges with the existing conventional energy resources, India needs to put forward attempts in experimentation and development to find non-conventional renewable sources like solar and wind. It is also necessary to update the existing grid and make it smarter. By making it smarter, it not only reduces the technological and commercialized losses but also reduces carbon. Hence, the implementation of smart grid development plays a key role for meeting up the growing demand of electricity, and it can also be used to implement through a long process.

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Ferroelectric FET as a Low-Power Device with Reduced SCEs and RDF Effect

Ullas Pandey, Koushik Guha, K. L. Baishnab, and Brinda Bhowmick

Abstract It is known that for a classical field-effect transistor (FET), the subthreshold swing (SS) cannot be reduced below the Boltzmann limit of 60 mV/dec. Recently, it has been proposed that by instilling a ferroelectric material in the gate stack the SS can be reduced below 60 mV/dec limit, which also defines the minimum limit of power dissipation. Simulations were carried out using Sentaurus TCAD for the Ferroelectric FET having Si doped HfO_2 as a ferroelectric material and SiO_2 as a linear dielectric in the gate stack and results show that SS is brought down below 60 mV/dec, with high I_{ON}/I_{OFF} ratio and low threshold voltage. Short-channel effect (SCE) and random dopant fluctuation (RDF) is also investigated for various channel length and channel doping concentration.

Keywords Negative capacitance · Subthreshold swing (SS) · Short-channel effects (SCEs) · Surface potential and ferroelectric · Threshold voltage (V_{th})

1 Introduction

The scaling in microelectronics has been impelled by the quest for higher density integration, since the switching energy and the switching delay of MOSFET is directly proportional to channel length, the aim of having faster and more energy efficient devices also leads to aggressive scaling. With miniaturization of MOSFET, the device geometry such as channel length, junction depth and oxide thickness have been reduced but for maintaining a low power density, the applied voltage V_{DD} should also be scaled down. As, the V_{DD} decreases the gate overdrive voltage also decreases which negatively affects device performance by decreasing I_{ON} (On-current), I_{ON}/I_{OFF} ratio and dynamic speed. To meet the I_{ON} requirement V_{th} (Threshold Voltage) should be brought down, but with threshold voltage reduction the I_{OFF} (Off-current) increases exponentially. So, to meet a sufficiently high I_{ON} with respect to I_{OFF}, Subthreshold Swing (SS) should be small. However, for conventional

U. Pandey · K. Guha (✉) · K. L. Baishnab · B. Bhowmick
Department of Electronics and Communication Engineering, National Institute of Technology Silchar, 788010 Silchar, Assam, India
e-mail: koushikguha2009@gmail.com

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MOSFET the SS cannot be less than 60 mV/dec because of Boltzmann tyranny. In order to evade this limitation, a number of devices have been proposed such as Impact Ionization MOSFET [1], Feedback-FET [2], Suspended Gate MOSFET [3], Tunneling FET [4], FeFET [5, 6]. Salahuddin et al. [7] theoretically demonstrated that by embracing a ferroelectric material in the top of silicon dioxide in Metal–Oxide–Semiconductor structure, the surface potential can be highly boosted leading to a steep transition. Ferroelectric materials during polarization switching show the transient phenomenon of negative capacitance. By the virtue of this property, ferroelectric materials can act as an inner voltage amplifier to enhance the surface potential and thus opening a new way for the apprehension of transistors with steeper subthreshold characteristics (SS < 60 mV/decade) without changing the essential physics of the FET.

This paper discusses the TCAD Sentaurus design and simulation of SOI-based FeFET. It shows how negative capacitance of ferroelectric material (Si doped HfO_2) causes lowering of threshold voltage and early arrival of surface inversion in the device which leads to sharper subthreshold transition and thereby smaller subthreshold swing. This paper also investigates the short-channel effects like DIBL (Drain Induced Barrier Lowering) and V_{th} roll-off in FeFET as well as the effect of RDF on V_{th}.

2 Theory

At a given V_{DD}, in order to achieve energy efficient switches $I_{\text{ON}}/I_{\text{OFF}}$ ratio has to be as high as possible and to increase the ratio, the subthreshold swing needs to be small. The Subthreshold swing (SS) is defined as-

$$\text{SS} = \frac{\partial V_g}{\partial(\log I_d)} = 2.3\frac{K_B T}{q}\left(1 + \frac{C_s}{C_{\text{ox}}}\right) \tag{1}$$

where K_B is the Boltzmann constant, T is the absolute temperature and q is the unit charge. C_s and C_{ox} denotes the depletion capacitance and oxide capacitance respectively. The first term $2.3\frac{K_B T}{q}$ denotes that the transport in subthreshold region is dominated by diffusion transport of excess minority carriers and is defined by the Boltzmann statistics of electrons/holes, which limits the SS to 60 mV/dec. Recently, it has been found that the ferroelectric thin films show the phenomenon of negative capacitance due to the negative slope of polarization-electric field (P-E) curve. Thus, if ferroelectric material is used as a gate insulator, the factor $\left(1 + \frac{C_s}{C_{\text{ox}}}\right)$ can be made less than one and thus the Subthreshold Swing (SS) can be further brought down below 60 mv/dec.

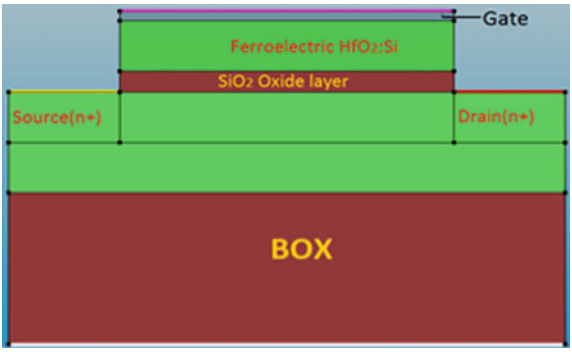

Fig. 1 Proposed structure of ferroelectric FET

3 Proposed Design and Simulation Method

In this paper, an n-type Silicon On Insulator (SOI) ferroelectric FET is proposed. The device is shown schematically in Fig. 1. This is a simple and symmetric MOSFET structure, where aluminum is used as a gate material with work function of $\emptyset m = 4.1$ eV. The gate length along with the channel length is varied from 40 to 60 nm to avoid any overlapping or underlapping. The doping concentration of the channel is varied from 8×10^{17} to 4×10^{18}, the highly doped n^+ source concentration is 10^{20} cm^{-3} and n^+ drain concentration is 10^{19} cm^{-3}. In the gate stack SiO_2 is used as an oxide layer and silicon-doped HfO_2 is utilized as ferroelectric layer due to its unique property of exhibiting the ferroelectricity even in a 5 nm thin film [8, 9]. Thickness of oxide layer is varied from 0.8 to 2 nm and thickness of ferroelectric layer is varied from 5 to 15 nm. Thickness of Ferroelectric material, thickness of oxide layer, channel length, channel doping concentration are denoted by t_{fe}, t_{OX}, L_{CH} and N_{CH} respectively. Simulations are performed by Sentaurus TCAD. Ferroelectric Model is activated in the physics section. Size of the memory is set at 20 turning points for each element and each axis. Values of remanent polarization, saturation polarization and coercive field are mentioned in parameter file to characterize the properties of ferroelectric material. Since for indistinguishable particles such as electrons Fermi-Dirac statistics are valid [10] and it also becomes important for stating high values of carrier densities, in the active region of a silicon device, Fermi-Dirac distribution is used throughout the simulation. In addition to this, a bandgap narrowing model and Shockley–Read–Hall (SRH) recombination model are also activated in the simulation [11]. To consider the mobility effect, a Philips unified mobility model is enabled [11].

4 Results and Analysis

As per the capacitive model shown above in Fig. 2. The voltage balance equation can be written as

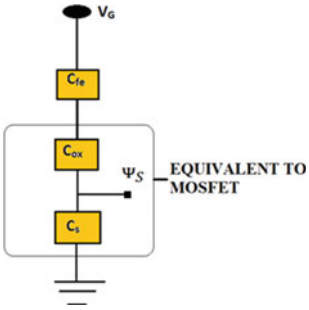

Fig. 2 Capacitive model of FeFET

$$V_G = V_{\text{FB}} + V_{\text{fe}} + V_{\text{OX}} + \Psi_S \tag{2}$$

where V_G is the gate voltage applied, V_{FB} is called Flat-band voltage, $V_{\text{OX}} = Q'_G/C'_{\text{OX}}$ is the potential drop across the oxide layer, Ψ_S is the surface potential, V_{fe} is the potential drop across ferroelectric layer which will obtain a negative value during the polarization switching on account of the property of negative capacitance. Now we know that, V_G and V_{FB} are fixed and if V_{fe} becomes negative, to maintain the balance of the equation V_{OX} and Ψ_S will be boosted. Now if the value of C'_{OX} is made higher (by making the oxide layer thickness smaller, since $C'_{\text{OX}} = \varepsilon/t_{\text{OX}}$), bigger part of boosted potential can be offered to Surface potential Ψ_S. As a result, charge per unit area in the channel can be greatly enhanced by the relation given by in traditional MOSFET system.

$$Q'_C = -\operatorname{sgn}(\Psi_S)\sqrt{2q\varepsilon_S N_A} \left[\varphi_t e^{\frac{-\Psi_S}{\varphi_t}} + \Psi_S - \varphi_t + e^{-\frac{2\varphi_F}{\varphi_t}}\left(\varphi_t e^{\frac{\Psi_S}{\varphi_t}} - \Psi_S - \varphi_t\right)\right]^{1/2} \tag{3}$$

Figure 3 shows the boosted potential of FeFET in comparison to the traditional MOSFET. Thus, by selecting thicker ferroelectric layer and thinner oxide layer in the gate stack, subthreshold-transition of FeFET is observed to be faster than traditional MOSFET and because of SOI-based structure device is more stable and provides higher $I_{\text{ON}}/I_{\text{OFF}}$ ratio as given in Table 1. TCAD simulation of traditional MOSFET

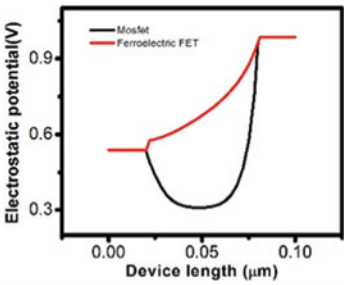

Fig. 3 Surface potential of FeFET and MOSFET

Table 1 I_{ON}/I_{OFF} ratio for SOI-based structure

t_{fe} (nm)	I_{ON} (A)	I_{OFF} (A)
5	0.00862	5.95×10^{-16}
10	0.00517	6.81×10^{-17}
15	0.0032	7.34×10^{-18}

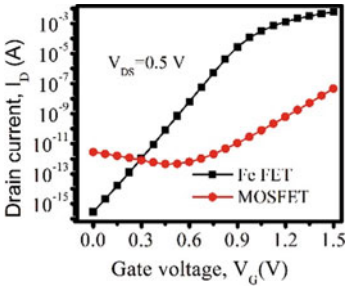

Fig. 4 Log I_d/V_g curve for FeFET and MOSFET

and SOI-based FeFET for subthreshold characteristics is shown in Fig. 4. It exhibits that subthreshold swing is appreciably improved and is found to be 52 mv/dec.

Further inquiring the subthreshold region, it is revealed that voltage amplification has major impact on Threshold voltage of FeFET. In MOSFET [12], V_{th} is given by Eq. (4) and in weak inversion, the relation of Gate voltage and surface potential is given by Eq. (5).

$$V_{th} = V_{FB} + \emptyset_o + \gamma\sqrt{\emptyset_0 + V_{SB}} \tag{4}$$

$$V_{GB} = V_E + \psi_S + \gamma\sqrt{\psi_S} \tag{5}$$

If $V_{SB} = 0$, Using Eqs. (4) and (5), we get

$$V_{th} = V_{GB} + \emptyset_0 + \gamma\sqrt{\emptyset_0} - \psi_S - \gamma\sqrt{\psi_S} \tag{6}$$

In Eq. (6) we can observe that if the first three terms of right hand side remain constants and ψ_S increases because of voltage amplification on account of negative capacitance V_{th} will decrease. TCAD simulations also validates that voltage amplification has major impact on Threshold voltage. Threshold Voltage is reduced to very low values in FeFET and it also shows the dependence of V_{th} on gate voltage V_g, oxide layer thickness and ferroelectric layer thickness. It is observed that thicker ferroelectric layer over oxide layer leads to sharper decline of Threshold voltage (V_{th}) as shown in Fig. 5. whereas the same phenomenon is observed with thinner oxide layer as shown in Fig. 6.

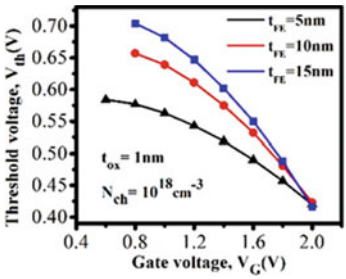

Fig. 5 V_{th}/V_g curve for different t_{fe}

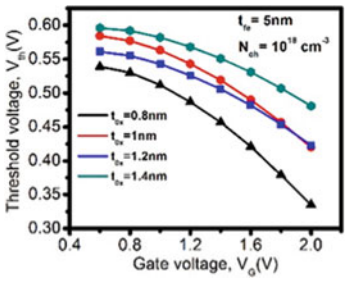

Fig. 6 V_{th}/V_g curve for different t_{OX}

4.1 RDF and Short-Channel Effects

The quest for smaller devices and large scale integration led to scaling. Scaling laws as proposed by Dennard [13] leads to shrinking of channel length which affects the ideal behavior of the device and causes deviations. With aggressive technology scaling short-channel effects has to be circumvent to maintain the reliability of the device. The foremost reliability issues associated with shorter channel lengths are a shift in threshold voltage with decreasing channel length, DIBL or lack of pinch-off. Based on TCAD, this section investigates the short-channel effects like DIBL and Threshold voltage roll-off and it has been found that FeFET shows reduced short-channel effects compared to traditional MOSFET as shown in Fig. 7 and 8.

RDF is an intrinsic variation source in CMOS structure caused by manufacturing limits and fundamental physics. It is regarded as a major constriction in the path

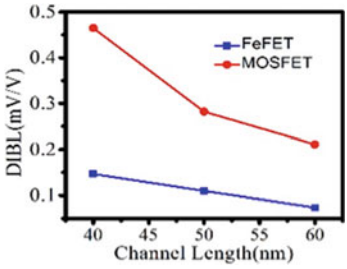

Fig. 7 DIBL effect on varying channel lengths

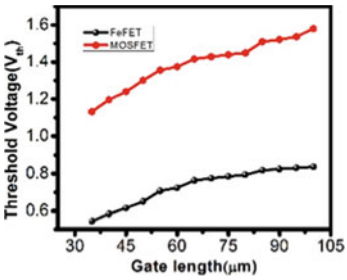

Fig. 8 Dependence of V_{th} on different channel lengths

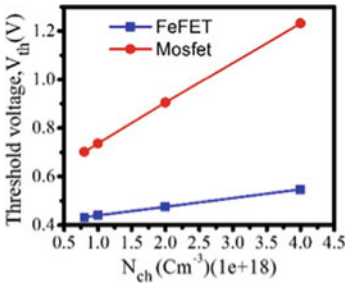

Fig. 9 Dependence of V_{th} on different channel doping concentration

of large scale integration. RDF results because of the variation in the implanted impurity concentration, which can alter transistor's properties like threshold voltage. Here RDF effect is also investigated using TCAD and it is observed that in FeFET, threshold voltage is far less sensitive to channel doping variations than the classical MOSFET as shown in Fig. 9. Thus a highly stable V_{th} is gained in FeFET.

5 Conclusion

A comparative examination of MOSFET and FeFET has been done using Sentaurus TCAD simulation tool. It is found that with thicker ferroelectric layer and thinner oxide layer, FeFET shows steeper and better subthreshold transition, having a higher I_{ON}/I_{OFF} ratio of 10^{15} and SS of 52 mV/dec. It also revealed that the RDF effect is greatly reduced in FeFET and SCEs like DIBL and V_T roll-off are reasonably smaller compared to MOSFET.

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Semantic Segmentation Using ENet Architecture

P. Mohan Sai Kumar, N. V. Krishna Rao, Ch. Manish Kumar Reddy, Jyothi Ranjan Mohanty, B. Ramyasree, and Y. Deepthi

Abstract Interests in augmented reality wearable's, automated devices used in home, self-driving vehicles are in high demand, which uses semantic segmentation. The methodology includes the consideration of each and every pixel, i.e., every pixel may belong to any one category and can be operated in real-time applications on less-power mobile devices. Although, huge availability of data sets and many machine learning algorithms outstrip the performances of this kind of application but as a penalty in floating-point operators which increases the running time. In order to classify the spatial images along with the meaningful segmented regions, numerous Neural Networks are proposed includes Signet or Fully CNN for multiple class classification. In this work, we used the newly introduced model ENet also called Efficient Neural Network, which is specially designed for tasks requiring low latency operations. This model is 18× times faster, using less number flops, i.e., 75× less, and uses less number of parameter, i.e., 79× less. The proposed method uses Cityscapes database for the experiments and the results are compared with other conventional techniques.

Keywords ENet architecture · Semantic segmentation · Autonomous driving vehicles

1 Introduction

Modern camera systems can be mounted in many ways with advanced technology, from mobile phones, autonomous vehicles, and surveillance systems, to capture images with quality, low cost. Consequently, the demand for devices that are capable of understanding and reading such images will increase. For years there has been a change in the approach of interpretation of images. Nevertheless, the importance of scanning these images for object identification has not been changed. The learning

P. Mohan Sai Kumar · N. V. Krishna Rao (✉) · Ch. Manish Kumar Reddy · J. R. Mohanty · B. Ramyasree · Y. Deepthi
Department of Computer Science and Engineering, Institute of Aeronautical Engineering, Dundigal, Hyderabad, Telangana, India
e-mail: nvkrishnarao3@gmail.com

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problems visual information is divided into three groups, called image recognition, localization and object identification, and semantic image segmentation. The method of mapping and classifying the nature for critical applications like scene understanding and self-driving cars, etc. is called Semantic image segmentation. Semantic segmentation, which is a classification of images at pixel level is important for scene understanding. This is because each and every pixel is identified as an object that belongs to a particular semantic class. In urban scene data set we have different objects like traffic light, pedestrian, persons, etc. In the near future, autonomous driving will impact the people of industrially developed countries. Rapidly increasing performance of several deep learning vision based algorithms such as object detection, road segmentation, and traffic signals recognition, several research groups have contributed to the development of autonomous driving systems. An autonomous vehicle needs to feel the surroundings and behave safely to reach a certain destination. Such functionality is carried out by using several types of classifiers.

Different Types of image classification techniques:

There are mainly three kinds of classification techniques are there:

i. Image classification: "Identify what the image is"
ii. Object detection: "Identify where in the image"
iii. Semantic Segmentation: "Identify the meaning" Existing Methodologies.

Different Techniques of classifications:

a. Region-based segmentation
b. Fully CNN
c. Weakly supervised semantic segmentation.

We present a detailed literature survey in the next section.

2 Literature Survey

2.1 The Cityscapes Dataset for Semantic Urban Scene Understanding

The authors in [1] described the general information on how deep learning approach attracted attention in machine learning sector and an application about semantic segmentation is run to assist autonomous driving vehicles. This application is implemented with Fully Convolutional Network (FCN) architectures which are obtained by modifying the Convolutional Neural Network (CNN) architectures supporting deep learning. They also stated that deep learning can be a fast-growing machine learning approach to understand and perceive large amounts of information [2].

2.2 *Decoupled Deep Neural Network for Semi-supervised Semantic Segmentation*

The authors in [3] worked on cityscape datasets for semantic urban scene understanding. They also stated that visual comprehension of complex urban road scenes is an empowering factor for many applications. There has been an enormous benefit of object detection in large-scale datasets within in deep learning context. There are no other cityscape datasets that capture the real-world urban scene complexity. This cityscape dataset is consisting of an outsized, various set of video sequences recorded in streets out of those images 5000 images have high-quality pixel-level annotations, additionally, 20,000 images have coarse annotations.

2.3 *Convolutional Networks for Images, Speech, and Time Series*

The authors of [4] proposed a completely unique deep neural specification for semi-supervised semantic segmentation using heterogeneous annotations. This algorithm learns a separate network for every task by decoupling segmentation and classification which is contrary to existing approaches.

2.4 *Imagenet Classification with Deep Convolutional Neural Networks*

The authors of [5] used convolutional neural network [6] to calculate the depth and accuracy of the large-scale image recognition setting. Their main contribution is a radical evaluation of networks that accelerate the depth of architecture with very small (q3 $\times$ 3) convolutional filters which shows that an enormous improvement is achieved by pushing depth to 16–19 layers.

3 Implementation Methodology

Here we are using ENet architecture which gives better results than the existing architecture. The architecture of our network is divided into several stages. We adopt a view of ResNets which depicts them as having one primary branch and augmentations with convolutional channels that break free it, at that point converge back with a component shrewd expansion. Each block consists of a 1 $\times$ 1 projection to reduce the dimensionality, a main convolutional layer, and a 1 $\times$ 1 expansion. Between all

convolutions, we place PReLU and batch normalization. They are the modules of bottleneck.

If a bottleneck is downsampling then we add a max pooling layer.

Also, a convolution of 2×2 with stride 2 replaces the primary 1×1 projection in both dimensions. We zero pad the activations, to match the amount of feature maps. Conv is also referred to as deconvolution or fractionally strided convolution with 3×3 filters. Sometimes we replace it with a sequence of 5×1 and 1×5 convolutions, i.e., asymmetric convolution.

We use Spatial Dropout to regularize, with $p = 0.01$ before bottleneck2.0, and $p = 0.1$ afterwards. In the initial stage, we contain one block. Stage 1 consists of 5 bottleneck blocks, while stage 2 and stage 3 have a structure which is equivalent, we omit the 0th bottleneck because at the start stage 3 doesn't downsample the input. We name these three stages as encoder. The decoder consists of Stage 4 and Stage 5. In any of the projection, we did not use bias terms, in order to scale back the amount of kernel calls and overall memory operations, as separate kernels for bias addition and convolution are used by cuDNN. The accuracy is not impacted by this. We use batch normalization In between each convolutional layer and following non-linearity. The decoder replaces max pooling with max unpooling, and spatial convolution disinterestedly replaces padding. As the initial block operated on the three channels of the input frame, while the ultimate output has C feature maps (the number of object classes), we didn't use pooling indices within the last upsampling module. Also, for performance reasons, we decided to put only a bare full convolution because of the last module of the network, which alone takes up a sizeable portion of the decoder time of processing.

4 Performance Analysis

We have used Open CV library in our model to perform semantic segmentation. This enables us to get better performance of the model in real-time applications. Our model performance will be better in NVIDIA and GPU.

Table 1 Performance analysis

Performance analysis												
NVIDIA TXI							NVIDIA TitanX					
480 × 320			640 × 320		1280 × 720		640 × 360		1280 × 720		1920 × 1080	
	ms	fps	ms	fps	ms	fps	ms	fps	ms	fps	ms	fps
SegNet	757	1.3	1251	00.8	–	–	69	14.6	289	3.5	637	1.6
ENet	47	21.1	69	14.6	262	3.8	7	135.4	21	46.8	46	21.6

Table 2 Hardware requirements

Hardware requirements			
	GFLOPS	Parameters (M)	Model size (fp1) (MB)
SegNet	286.03	29.46	56.2
ENet	3.83	0.37	0.7

To hurry up all networks we merge dropout layers and batch normalization into convolutional filters. The performance comparison is described in two tables (Table 1 and 2).

5 Results

We have performed the semantic segmentation on cityscape dataset and obtained the desired results. The results obtained are of high quality compared to the results that are obtained using Fully CNN architecture. The time taken to process results is very low and offers better quality images. This processing time can be reduced further by using GPU (Graphics Processing Unit). The amount of memory used by the application is very less compared to Fully CNN architecture. We can perform semantic segmentation for different datasets using this application. Our model used OpenCV library to perform training and testing and performance is evaluated (Fig. 1).

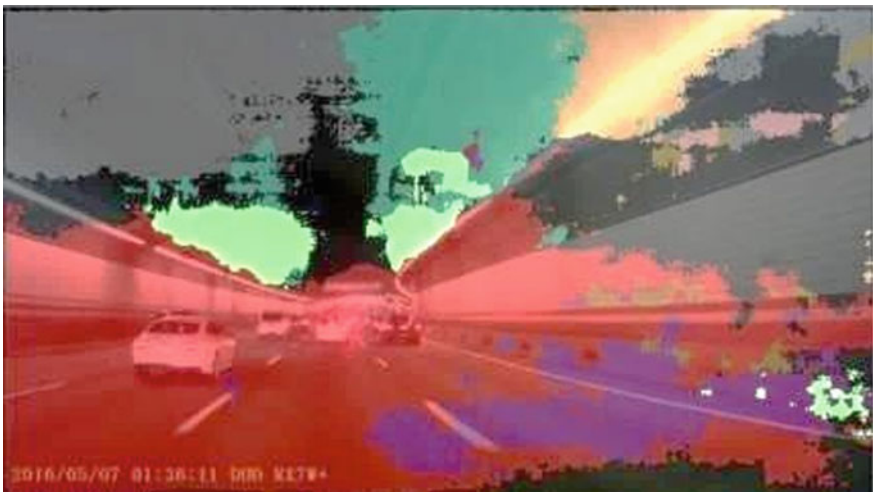

Fig. 1 Output for video

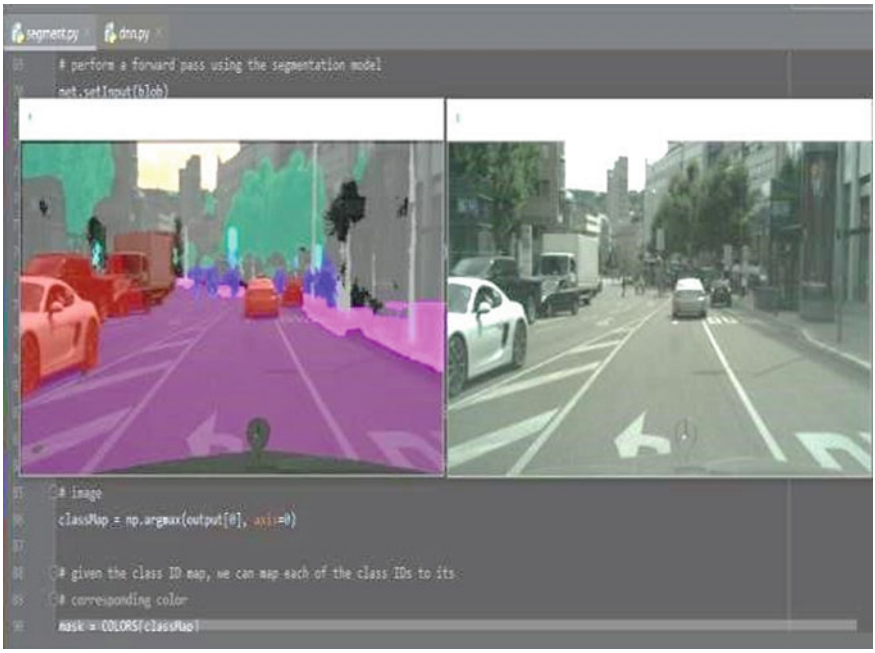

Fig. 2 Input and output for image

The above two images are the outputs for video and image of cityscape dataset, respectively. These outputs are obtained by our model which uses ENet deep learning architecture (Fig. 2).

6 Conclusion

We have proposed a system that performs semantic segmentation using ENet architecture. This ENet architecture provides better results than the existing systems which use Fully CNN or SigNet architectures. These architectures are not suitable for videos. Though they provide better results for images, they cannot be used for videos. The ENet architecture can also be used for real-time processing which is not possible by existing architectures.

The results of segmented images are far better than the results obtained from the SigNet or Fully CNN architectures.

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Electronic Amplifier Based on Hall Effect Principle

Abhimanyu Kumar, Souvik Ganguli, Shuvangi Sinha, and Raju Basak

Abstract The Hall effect refers to the generation of voltage across a conductor when placed in a transverse magnetic field, which is perpendicular to the current through it. The physics of this effect is elaborated along with the relevant mathematical expressions. Later on, a detailed account of Hall effect-based devices is given. The emphasis of this work is, however, on the voltage amplifier device. A short general discussion of an amplifier is done, after which the amplifier design employing the Hall effect principle is introduced. The concept is explained, and expression for the amplification factor is derived. This work shall further instigate new ideas in the minds of interested researchers. Finally, overvoltage protection is discussed along with the temperature and noise compensation measures, which are required for the appropriate functioning of the Hall-based amplifier.

Keywords Hall devices · Amplifier · Temperature sensitivity · Overvoltage protection

1 Introduction

The Hall effect refers to the generation of potential difference across a conductor when placed in a transverse magnetic field, which is perpendicular to the electric current through the material [1]. Material scientists and metallurgy engineers use Hall effect for the study of materials [2] and for the determination of the sign and density of the charge carriers in a given sample. Hall effect measurements also allow the electrical characterization of semiconductor materials using magnetic fields.

Since the discovery of this effect in 1879, it has gained immense importance in measurement theory and popularized due to application in transducer and sensors. In literature, the integrated Hall sensors have been divided into three categories, which are discussed in detail in the subsequent section.

A. Kumar · S. Ganguli (✉) · S. Sinha · R. Basak
Thapar Institute of Engineering and Technology, Patiala 147004, India
e-mail: souvik.ganguli@thapar.edu

Techno India University, Kolkata 700091, India

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- Linear output devices
- Switches and Latches
- Speed and timing sensors.

The focus of this work, however, will be specifically on the use of Hall effect in devices and will discuss the potential use of this effect in amplifier technology. Amplifiers are devices that are used to magnify a given input. They have numerous applications such as in speakers, transmitters, communications equipment, control circuits, etc. [3]. The amplification is possible due to the presence of an active device in the circuit such as vacuum tubes, or a solid-state component like transistors. Earlier amplification was achieved using vacuum tubes, and eventually with transistors, and presently it is majorly replaced by semiconductor-based amplifiers [4]. This change in technology is caused due to the need for a reduction in cost and space.

This work is conducted for the exploration of the potential use of the Hall effect for amplification purposes. The paper is organized as follows: Sect. 2 describes the Hall effect and its physics, Sect. 3 provides a detailed account of the devices based on Hall effect present in the literature and available commercially, Sect. 4 describes the key design characteristics of a Hall-based device and Sect. 5 explores the use of Hall device as an amplifier along with appropriate additional circuitry. Finally, Sect. 6 discusses the protection of the device and Sect. 7 concludes the discussion.

2 The Hall Effect

The basic configuration of the Hall device is shown in Fig. 1a, in which current flows from the battery with potential E_o through the strip, and magnetic field B is perpendicular to the strip.

Consider a conductor strip, as shown in Fig. 1b, with length l in the x-direction, breadth w in the y-direction and thickness h in the z-direction. Assume that the conductor has charge carrier of charge e with n number of carriers per unit volume (i.e. charge number density). Let v_x be the drift velocity when current I_x flows in the x-direction.

Each charge carrier moves randomly within the conductor, but when under the influence of applied fields, there is a net movement of charge carriers, thus drift velocity is the average velocity of the carriers over the entire volume. The current $I_x = J_x wh = nev_x wh$ where J_x is current density and wh is the cross-sectional area. The current I_x is caused due to the applied electric field E_x along the length of the conductor.

As per Ohm's law, we have $J_x = \sigma E_x$ where σ is the conductivity of the material. Assuming that the conductor is kept in a perpendicular magnetic field, the charge carriers will experience Lorentz force $q(v \times B)$ that will deflect them towards one side of the strip.

Consequently, this deflection causes an accumulation of charges along one side of the strip which creates an electric field E_y counteracting the force due to magnetic

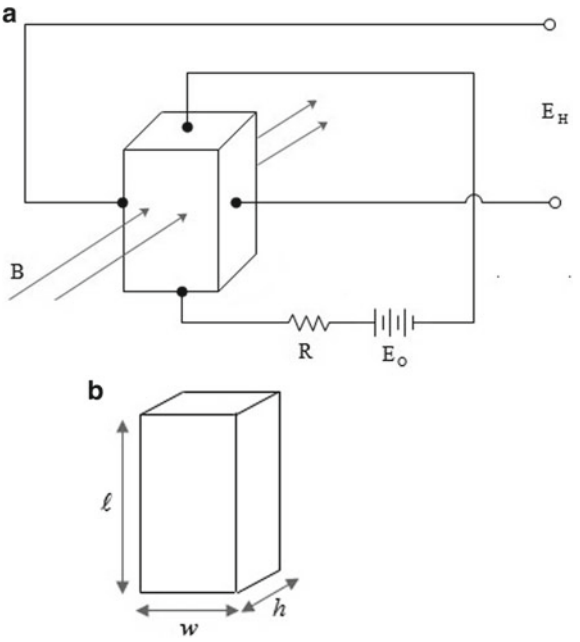

Fig. 1 **a** Hall effect device, **b** dimensions of conductor

field. In steady-state, $E_y = v_x B_z$ where E_y is the Hall field. Thus, the generated Hall voltage V_H is given by

$$V_H = R_H \frac{I_o B}{h} \tag{1}$$

where $R_H = \frac{1}{ne}$ is the Hall-coefficient. From an electrical perspective, the Hall device is modeled as depicted in Fig. 2.

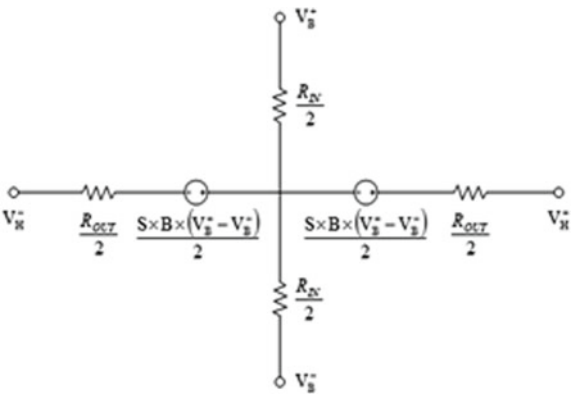

Fig. 2 The electrical model of Hall device

3 Devices Based on Hall Effect Principle

As mentioned earlier, the Hall effect is useful for the development of magnetism-based sensors and technology for the determination of electrical/magnetic parameters. A Hall-effect transducer can be used in numerous low-power applications as a magnetic measuring instrument with the addition of just a power source and a sensitive voltmeter. Petruk et al. [5] discussed the current transformer using the Hall sensor. A Hall effect proximity transducer is also available [6]. Hall effect is also employed in displacement sensors [7]. Several advances have been made by the gradually increasing use of Hall magnetic sensors in the computer industry. In this section, we will specifically paper we shall focus only on the devices which are related to the Hall effect. This effect has found a huge application in sensors and measurement theory.

3.1 Linear Hall Sensor

Depending on the magnetic field, the output of a linear Hall sensor does not have a discrete switching state, but the output signal it produces is directly proportional to the magnetic field. An accurate and cost-efficient linear hall sensor with digital output is available [8]. For different applications, different requirements are to be fulfilled. Initially, the Hall ICs were pre-programmed at the time of manufacturing on a one-time basis. However, the field programmable linear sensors allow the end-user to make adjustments in the Hall device before using it in the end product. These provide better compatibility and often better accuracy [9] with a potential application in the automobile industry.

3.2 Switches and Latches

In many applications, the exact value of the magnetic field strength is not of concern, and it is just necessary to ensure whether the applied magnetic field is above a threshold or not. Thus, Hall-effect switches are developed. Since the Hall switch has an on/off state analogous to the digital binary, these are often referred to as digital Hall-effect sensors. A digital Hall-effect sensor is nothing but a simple linear sensor with a threshold detector and an output driver.

Hall effect switch turns on in the presence of a south pole on its face or north pole on the opposite side. It will turn off in the absence of magnetism. Hall effect switches have a potential application wherever voltage control is required, like in an electrostatic spray gun. The spraying voltage is controlled using Hall-effect circuitry [10]. Hall effect latch works like a switch with the only difference that it stays on

even when the magnet is removed. It turns off if the north pole is faced or power is turned off.

There are three types of digital Hall sensors: unipolar, bipolar and omnipolar. Unipolar sensors require either of the two magnetic poles to operate. These turn on when the magnetism exceeds a certain threshold. In the absence of magnetic field, it may or may not latch, i.e. it can function as a switch or as a latch or even as a north pole switch. Bipolar sensors turn ON when they are in proximity to one magnetic pole and turn OFF when they are brought in proximity to the opposite magnetic pole. These sensors retain their present state in the absence of magnetism. Omnipolar sensors turn on when they are in proximity to a strong magnetic field of either polarity. The removal of the magnetic field turns them OFF. The omnipolar sensor can be constructed using a pair of unipolar sensors mounted in the opposite direction with their output wired together.

3.3 Speed and Timing Sensors

The necessity to sense the speed/position of gears occurs in numerous factories. The device to convert the passing teeth to an electrical impulse has been investigated for decades. Purely mechanical systems used have the issue of wear and tear, thus limiting its use to only low-speed applications.

Hall effect gear tooth sensing makes use of Hall principle for sensing the variation in flux found in the air gap between a magnet and rotating ferrous gear teeth [11]. Since the magnetic flux tends to follow a path with lower reluctance, as a tooth moves across the magnet, flux passes through the lower reluctance path offered by the gear tooth. When this occurs, the flux density measured by the Hall element increases. These signals from the Hall element are then converted into digital data and then subjected to digital signal processing to get final digital output. This concept is employed to determine the air gap between a magnetic pole and a ferrous material or the proximity of ferrous material.

Magnetic targets, fixed to the shaft as they move past the hall sensor, are used for speed sensing. The magnetic targets are usually discrete or ring magnet. In discrete magnetic targets, the successive magnets can either be of the same polarity or of the alternating polarity. Both settings are present in devices. Using ring magnet targets with alternating pole faces, Hall effect sensors can also be used to determine the rotational direction. If the sensors are placed half a pole spacing apart, two signals are obtained at the output, with the leading edge of one coming before/after the leading edge of other. The direction of target rotation determines which signal leads or lags. An assembly for an angular position encoder is also available [12]. Hall effect is also employed in devices for the determination of angular shaft position [13]. Hall-effect based direction sensors can be used for autopilot applications [14, 15].

4 Key Design Considerations of Hall-Based Devices

From the above discussion, the following key characteristics are isolated. These characteristics are associated with the design of a device based on the Hall effect. These characteristics ensure the behavior of a device; thus, these are necessary to be taken care of while working on new technology.

4.1 Sensitivity with Respect to Input Parameters

A sensor that produces a greater change in the output signal is said to be more sensitive, and it often requires simpler and less expensive support electronics. Sensitivity can be characterized in two ways:

- Voltage per unit magnetic field $\frac{V}{B}$ for a unit ampere input current.
- Voltage per unit input current $\frac{V}{I}$ for a unit Tesla magnetic field.

4.2 Temperature Sensitivity

For a Hall-effect transducer, the sensitivity varies with temperature. These variations must be accurately accounted and corrected to get high degree of measurement. When a Hall-effect device is operated with a constant-voltage bias source, sensitivity variations with temperature are considerably greater than those obtained when operating the device from a constant-current bias source are obtained. An integrated three-terminal device of GaAs Hall sensor, comparator, and a TTL output buffer was developed in [16]. GaAs integrated Hall sensor was developed in [17] where Itakura et al. experimentally fabricated IC with new circuit to achieve high-temperature performance.

4.3 Linearity

As Hall-based devices are passive devices, the output voltage cannot exceed the input voltage. In case, where the Hall voltage is small, Hall sensors behave linearly, with linearity errors of less than 1% over the operating ranges. To measure very large magnetic fields (of the order of 100,000 gauss), instrumentation-grade sensors are constructed with low sensitivity so that they do not easily saturate.

4.4 Input and Output Impedance

The impedance parameters influence the design of the bias circuitry and the amplifier used to condition the signal. Designing an amplifier with limited information of the impedance of the source feeding it may either compromise performance or cost. To ensure low-noise, the output impedance is of major concern. For transducers biased with constant-current, the bias voltage is simply proportional to the device's resistance.

4.5 Noise

Hall-effect transducers present electrical noise in their output. The most fundamental electrical noise is called Johnson noise, which is the result of thermally induced motion of electrons (or other charge carriers) in a conductive material. It is solely a function of the resistance of the device and the operating temperature. Popovic et al. [18] proposed the use of self-calibration and combining magnetic concentrators on sensor chip to remove the problem of packaging stress and switching noise.

Due to above-mentioned characteristics, numerous applications require electronic processing of the obtained output. The electronic circuit used with the transducer is called an interface, and the major prerequisite for a good interface is that the input range should be compatible with the variation in the transducer output signal. Maupin and Geske [19] described the technology of combining Hall effect sensors with various conditioning circuits on monolithic Si integrated circuits.

5 Amplifier Technology Using Hall Effect

The voltage buffer is a common type of amplifier circuit used in electronics, often referred to as a voltage follower. This circuit has two simple forms, one using single transistor and the other employing an operational amplifier (op-amp). A transistor amplifier class-A uses a single transistor to produce a load signal. Typically, a common collector topology is used. Class-B transistor amplifier, also called push–pull amplifier, uses a pair of transistors to generate a load output [4]. Nevertheless, operational amplifiers found their way into mainstream electronics because they are a very close approximation of an ideal amplifier with zero output impedance and infinite input impedance. Thus, op-amps are suitable for achieving an ideal DC amplification. The operational amplifier circuitry is relatively easy than several other circuits.

Now, our purpose is to achieve amplification by the use of the Hall device. This change in technology is proposed due to the need and use of a low-power application.

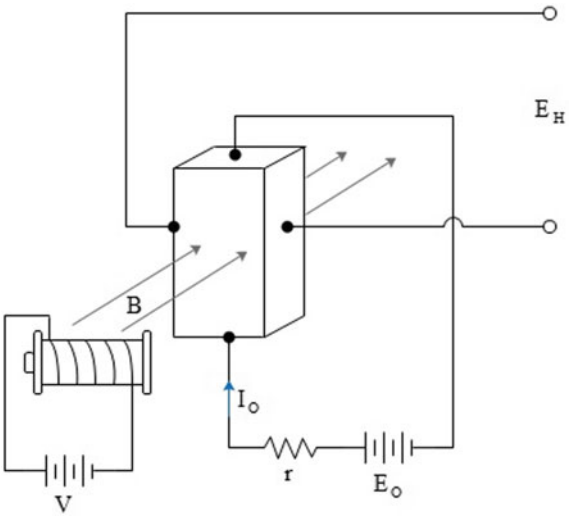

Fig. 3 Circuit diagram of MCA

Considering high electron mobility of pure InSb, Ross, and Thompson [20] presented a power amplification device using the Hall effect. An obvious technique for amplification involves the increase of the magnetic field for increasing the output voltage. It is known as the Hall effect multiplier, and however, in this paper, it is regarded as a Magnetic Control Amplifier (MCA). In this scenario, the input current is simply amplified by the amount of magnetic field applied, as shown in Fig. 3.

As an increase in magnetic field has a saturating effect on Hall voltage, therefore this method would not cause huge change in Hall voltage at high magnetic fields. MCA causes amplification at the expense of the magnetic field for materials with a significant Hall-coefficient only. Thus, MCA has serious limitations. This demands an improvised technique called Thickness Control Amplifier (TCA) [21], which is discussed below.

As shown in Fig. 4, TCA has a single voltage source E_o which feeds the Hall device, as well as is used to power an electromagnet for producing the required magnetic field. This technology reduces the dependence on any external source of a magnetic field. The material used in the Hall device is compressible and is placed between two plates. Let the actual length be h_o and the change in length be Δh then

$$E_H = R_H \frac{I_o B}{h_o - \Delta h} \tag{2}$$

Substituting strain $\varepsilon = \frac{\Delta h}{h_o}$ in terms of stress $\sigma = Y\varepsilon$ then

$$E_H = R_H \frac{I_o B}{(1-\varepsilon)h_o} \tag{3}$$

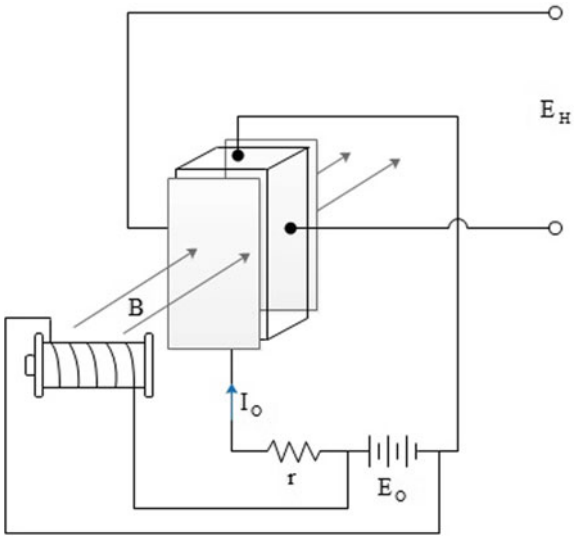

Fig. 4 Circuit diagram of TCA

$$E_H = R_H \frac{I_o B}{\left(1 - \frac{\sigma}{Y}\right) h_o} = A_v I_o \tag{4}$$

where Y is Young's modulus and A_v is amplification factor. Clearly, amplification is caused due to the application of stress.

For $B = 0.14$ T, $h_o = 2$ mm, and $R_H = 0.003090$, Fig. 5 shows the variation of amplification factor with $\frac{\sigma}{Y}$. It depicts that with appropriate material and dimensions, a large amplification factor can be achieved.

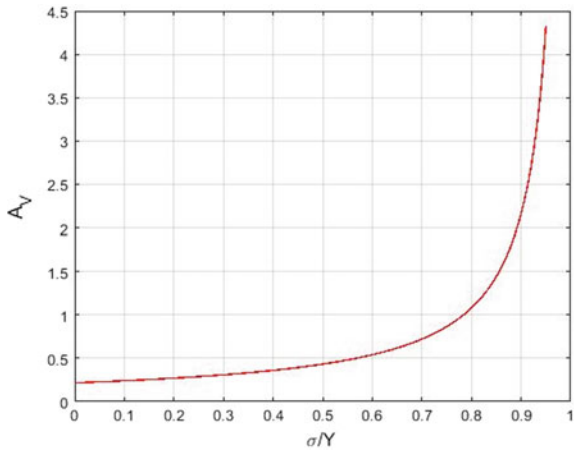

Fig. 5 Curve of amplification factor A_v versus $\frac{\sigma}{Y}$

6 Protection of the Apparatus and Error Compensation

An amplifier circuit not only produces but also sustains the amplified voltage, thus the safety of the components is also important. A controlled switch can be used for this purpose. Placing SCR/thyristor, with an appropriate forward break-over voltage across the output port, will also ensure safety by acting as a short wire when the hall voltage exceeds the break-over voltage. This protects the device from overvoltage. As Hall device operates at low current, therefore overcurrent problem never arises. Hence, no additional circuitry is required.

With a continuous flow of current, heat is generated in the device. If this generated heat is not properly dissipated, then it causes temperature rise. Based on the type of application such as commercial, industrial or automotive, linear Hall-effect sensors are available over a number of operating temperature ranges [22]. There are specifically constructed sensors that can withstand temperature ranging from −270 to 300 °C by enclosing them in a specially designed package to survive under extreme temperatures. Expensive and bulky amplifiers and compensation circuitry are often used to achieve linearity over some specific temperature range. However, this can be economically achieved using a different IC design in which the elements are formed in the same epitaxial layer, providing precise temperature compensation [23].

Apart from this, linear electronic Hall sensors also suffer from the problem of noise at lower frequencies. A capacitor is connected with the supply to reduce the noise from the system, and since these sensors are susceptible to electrical damage, proper care is required so that their ratings aren't exceeded. It has been observed that sometimes a potential difference is developed in the conducting material with the flow of electric current even in the absence of magnetism. This potential difference is called the offset voltage, which is usually caused due to geometric imperfections. The voltage offset can be reduced in Hall sensors as given in [24].

7 Conclusions

This work discusses the use of the Hall effect principle in designing electronic amplifiers. The Hall effect refers to the phenomenon of voltage production across a conductor which is placed within a magnetic field with current passing through it. An entire section is based on the physics of this effect and the electrical model of a Hall device. Further, a detailed discussion of the existing Hall-enabled devices is presented, viz. linear Hall sensors, switches, latches, and speed and timing sensors. The key characteristics of a Hall effect-based device are deduced from this discussion, which is important to be noted when designing a new device. This work, however, focuses on the voltage amplifier technology. The existing amplification components such as a transistor and operational amplifiers are mentioned, after which the Hall effect-based amplification is elaborated. Magnetic control amplifier (MCA) and Thickness Control Amplifier (TCA) are mentioned, each with their own merits

and demerits, eventually establishing TCA as a technology suitable for amplification. At last, protection measures and temperature and noise compensation techniques are discussed as they influence the proper functioning of the device.

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Design of Patch Antenna with Strip Lines and Slots for Biomedical Applications

Ketavath Kumar Naik, Seelam Chaitanya Satya Teja, and B. V. S. Sailaja

Abstract This paper presents the design of 2.45 GHz patch antenna for biomedical applications. The radiating patch consists of strip lines and with defects on ground plane is designed. The inverted T-shaped patch with inverted two L-strip lines is added on both side and also added one strip line on the patch. On the ground plane center, two hexagonal split rings are etched. The proposed antenna is resonated at 2.57 GHz with return loss −16.8 dB in free-space and at 2.45 GHz frequency when placed on the single-layer skin tissue of human body. A gain is observed −1.84 dB and specific absorption rate (SAR) of 1.2 W/Kg at free-space and 1.0 W/Kg at skin cum cotton layer is found. The radiation pattern is observed for E-plane and H-plane at free-space of proposed antenna with co-polarization and cross-polarization. The proposed antenna surface current distribution is observed 2.423A/m at free-space. The simulation results of reflection coefficient are presented.

Keywords Radiating patch · Strip lines · Defected grounds · Radiation pattern

1 Introduction

In recent years, the demand of portable patch antennas has been increased in the field of biomedical applications. The implantable patch antennas are used in communication system and act as a barrier between human body and external monitoring system. Biocompatibility, miniaturization, and patient safety make the design of implantable antennas highly challenging.

To enhance the wireless link quality through multi-polarization reconfigurable circular antenna [1] for body-centric wireless communication, four dipole radiators have been designed. In this, the antenna resonates from 2.2 to 3.1 GHz frequency with a bandwidth of 34%. A maximum peak gain of 5.2 dBi has been observed. A double-layered bow tie antenna [2] is proposed with a miniaturization technique to increase the electrical length. In [3], a center slot is etched to the circular polarization,

K. Kumar Naik (✉) · S. C. S. Teja · B. V. S. Sailaja
Department of Electronics and Communication Engineering, KLEF (Deemed to be University), Vaddeswaram, Guntur 522502, India
e-mail: drkumarkn@hotmail.com

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implanted patch antenna for miniaturization and to enhance the impedance matching. A conformal antenna with rectangular slot and split ring resonators (SRR) [4] has been designed for an antenna to operate for ISM band biomedical application. The proposed antenna has frequency range of 2.41 GHz to 2.81 GHz and impedance bandwidth of 400 MHz. Using the square shape complementary SRR [5] is improved antenna impedance matching and reduce the observed power inside the body for biomedical telemetry application.

The irregular shapes of the patches provide irregularity in current distribution over the radiating patch, which produces limited polarization and asymmetry in radiation patterns compared to general rectangular patch antennas. A circular ring antenna [6] was proposed to obtain circular polarization. To improve bandwidth of proposed antenna, double element ring-slot antenna has been designed [7]. The proposed antenna has resonating band from 4.25 to 12.5 GHz frequency. In [8], study of directional, omnidirectional, and pattern radiation characteristics is playing antenna on or near the human body.

From the literature survey, various antenna designs have proposed to resonate the antenna for WBAN application. A coplanar waveguide (CPW) feeding antenna [9] has proposed for in-body WBAN system. A split-triangular antenna [10] has designed for WiMAX application. In [10], antenna operates at 3.55 GHz with return loss −24.45 dB. A folded UWB antenna [11] is designed for WBAN applications shown a low SAR and a truncated structure to be suitable for on-body applications. A conformal metamaterial antenna with 2 × 2 array of H-shape unit cell [12] has been designed for an antenna to operate for WBAN communication. The antenna resonates for two frequency bands 3–2 GHZ to 3.5 GHZ and 3.9 GHZ to 4.3 GHZ frequency with max gain of 4.54 dBi and 4.71 dBi. Swastika shape slot [13] has designed for an on-body application in WBAN applications [14–18].

The advantage of hexagonal ring structure compared to the ring or conventional structures is the reduced interface and it improved the gain of hexagonal ring shapes.

2 Antenna Design

The geometry-proposed patch antenna is shown in Fig. 1. A polyimide l with (εr) 3.5, and δ is 0.004 is considered. The length ($L1$) and width ($W1$) of polyimide with a height (h) of 0.07 mm are considered.

Here, $L_1 = 25$, $L_2 = 21$, $L_3 = 7$, $L_4 = 1$, $W_1 = 20$, $W_2 = 2$, $W_3 = 6$, $W_4 = 14$, $W_5 = 0.5$, $r_1 = 7$, $r_2 = 6.4$, $r_3 = 6.2$, $r_4 = 5.5$ (units in mm).

The rectangular shape parasitic elements are considered as radiating elements and are coated on the kapton polyimide with a thickness of 0.01 mm as presented in Fig. 1a. Two hexagonal shape ring slots with radii r_1, r_2, r_3, and r_4 are etched from the ground plane as shown in Fig. 1b (Fig. 2).

The proposed PEPA antenna operates at 2.57 GHz with a reflection coefficient of −20.5 dB in simulation and 2.45 GHz with reflection coefficient of −25.7 dB in measurement (Fig. 2). The return loss plot for antenna placed in free-space

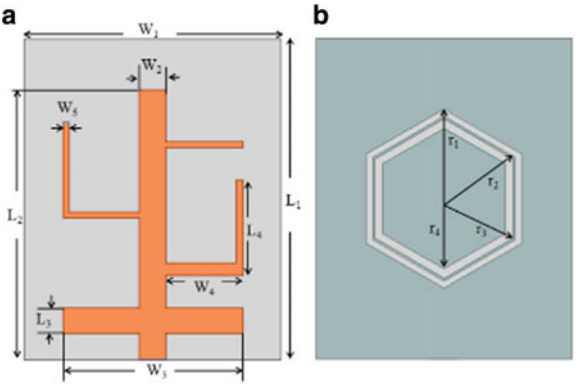

Fig. 1 Design of proposed antenna **a** Top view, **b** ground plane

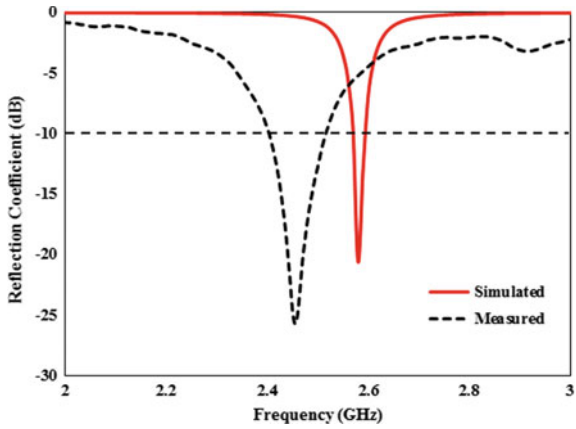

Fig. 2 Reflection coefficient (dB) of PEPA

and on the skin tissue with 1 mm cotton material in between skin and antenna is presented in Fig. 3. The antenna placed on the skin layer operates at 2.44 GHz with a reflection coefficient −12.28 dB. The measurement setup of PEPA antenna with network analyzer is presented in Fig. 3. The experimental setup of antenna in anechoic chamber is presented in Fig. 5.

The guided wavelength of the rectangular strip is

$$\lambda_g = \frac{\lambda_0}{\sqrt{\varepsilon_1}} \tag{1}$$

λ_0 Free-space wavelength

$$\varepsilon_1 = \frac{\varepsilon_r + 1}{2} \tag{2}$$

Fig. 3 Measuring the reflection coefficient with network analyzer

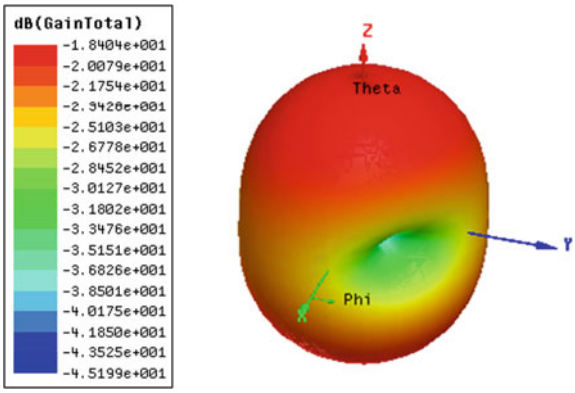

Fig. 4 3D-gain plot of the proposed PEPA

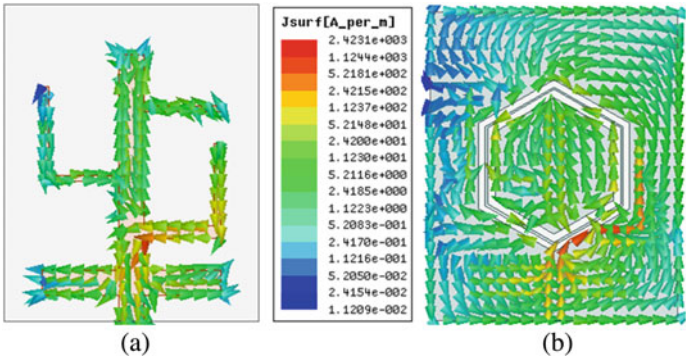

Fig. 5 Surface current distribution of PEPA at (a) radiating patch and (b) ground plane

The length of the rectangular strip is $L_4 = 0.5\lambda_g$.

Therefore, $L_4 = 1$.

The 3D-gain plot of antenna at 2.57 GHz frequency is shown in Fig. 4. From the Fig. 4a, minimum gain of −1.84 dB is observed at 2.57 GHz frequency.

The surface current distribution (SCD) for the PEPA antenna is depicted in Fig. 5. The maximum SCD of 2.423A/m is observed at 2.57 GHz frequency.

The radiation plot for the PEPA antenna resonated at 2.57 GHz is presented in Fig. 6. A bi-directional radiation pattern with major radiation at the 33^0 and 21^0 angles is observed and 10 dB isolation is seen between co-polarization and cross-polarization.

The SAR value of the PEPA antenna in free-space and on the skin layer tissue is presented in Fig. 7. The antenna in free-space and on the skin-cotton layer shows low SAR values with 1.2 W/Kg and 1.01 W/Kg which is less than 1.6 W/Kg as per IEEE standards.

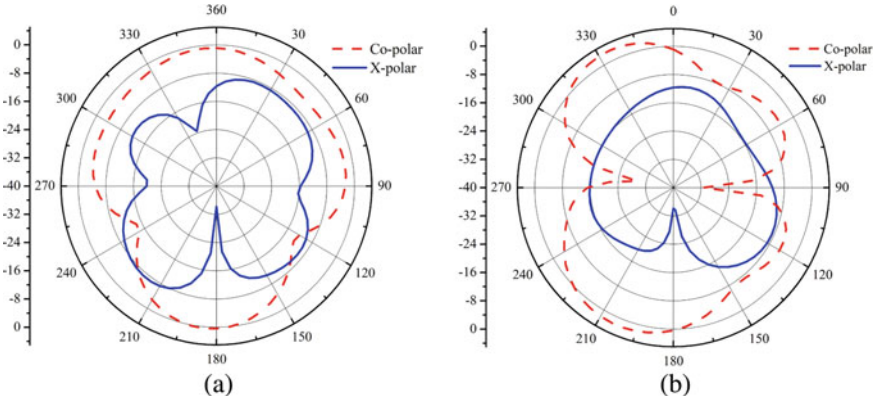

Fig. 6 Gain pattern of PEPA antenna (a) E-plane (b) H-plane

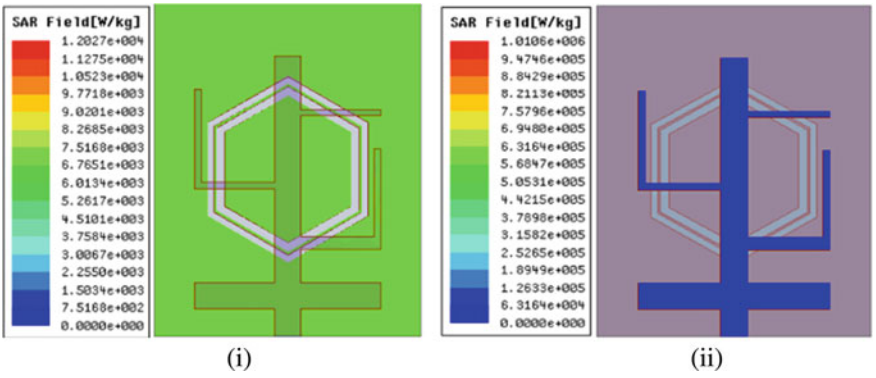

Fig. 7 SAR of the PEPA (i) free-space, (ii) skin-cotton layer

3 Conclusion

In this paper, the designed and tested PEPA antenna for the on-body application at ISM band. The PEPA antenna is a parasitic structure with hexagonal ring in the ground plane. The designed antenna resonates at 2.57 GHz and measurement result showed the resonance at 2.455 GHz. This proves the similarity between the experimental and simulated results. The pattern characteristics of PEPA antenna are bi-directional and a 10 dB isolation is observed between co-polar and cross-polar.

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Design a Tri-Band Hexagonal Patch Antenna for Wireless Applications

Ketavath Kumar Naik, T. V. Ramakrishna, T. L. Charan, and B. V. S. Sailaja

Abstract Design of tri-band hexagonal patch antenna for wireless applications is presented in this paper. The proposed antenna is operated at ultra-wide band at 4.2 GHz, 7.2 GHz, and 10.42 GHz frequencies at wireless applications. The coplanar waveguide (CPW) feeding is considered and slits at four sides and hexagonal split are etched at the center of the patch to operate tri-bands. The proposed antenna parametric analysis has carried out for optimized design. The parametric analysis considered with two parameters and presented in the design. The proposed antenna radiation pattern is observed for E-plane and H-plane at three bands and presented in the results. The gain 3D plots and current distribution plots are also presented in the results at tri-bands. The proposed antenna is fabricated and tested. The simulation results of reflection coefficient with measured results of reflection coefficient are presented. The comparison table is also presented with present work to existing works. These tri-bands are useful for wireless applications.

Keywords Hexagonal patch · CPW-fed · Tri-band · Wireless applications

1 Introduction

The biomedical antennas act as a transducer. The use of antenna in IMDs is to transmit and receive the data through external communication system. The ultra-wideband (UWB) is considered because [1] it offers a low radiation power with a high data rate. A double-layered bow tie antenna [2] is proposed with a miniaturization technique to increase the electrical length of the antenna with a coaxial feeding method. A folded UWB antenna [3] is designed for WBAN applications shown a low SAR and a truncated structure to be suitable for on-body applications. A compact monopole [4] UWB antenna is simulated and tested on a human hand model and vixen phantom for on-body communications. The results were compared, and a two-thirds muscle phantom is considered. Different types of radiation patterns are analyzed [5] such as

K. K. Naik (✉) · T. V. Ramakrishna · T. L. Charan · B. V. S. Sailaja
Department of Electronics and Communication Engineering, KLEF (Deemed to be University), Vaddeswaram, Guntur 522502, India
e-mail: drkumarkn@hotmail.com

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omnidirectional, directional, and pattern diversity radiation characteristics of UWB antennas by placing them on the body. A flexible substrate antenna [6] using a polyimide substrate is presented to have a dual-band operation.

The effect of the human head is investigated by using a numerical model [7] developed by RAMCOM using XFDTD simulator. This is shown to increase the gain and radiation characteristics of the antenna. Homogeneous and head phantom models [8] are considered for analyzing the electromagnetic energy absorption due to UWB models for on-body wearable antennas. An on-body channel for UWB has proposed [9] with a channel modeling for transmitter and receiver, and the FDTD method is used for obtaining the numerical analysis. In [10], the study is carried on human body with the millimetric wave interactions over very high frequency for different scientific approaches at on-body and off-body conditions.

Body-area networks (BAN) are used in wireless communication between on-body and implanted devices which are used in multimedia and medical applications. The design a radiating patch with circular/strips using different techniques [11–20] to improve the bandwidth and gain is presented. However, the present design is proposed with small patch antenna for wireless applications.

In this paper, the hexagonal patch antenna is operated at tri-band for biomedical applications. The proposed antenna is designed on flexible materials.

2 Antenna Design

The hexagonal patch with slits and slots antenna is proposed at tri-band for biomedical applications. The polyamide flexible material is considered with $\varepsilon_r = 4.3$ with loss tangent of 0.004. A hexagonal-shaped patch is considered, and the substrate height is 0.08 mm. A hexagonal-shaped split ring is considered and etched from the center of the radiating patch with slot width of S_6, four parallel rectangular slits with Length I_3 and width S_5 etched on the radiating patch are represented in Fig. 1. The CPW-fed is considered as feed line with an input impedance of 50Ω. The split ring considered is 0.2 mm.

Here, $S = 18$, $I = 20$, $S_1 = 5.5$, $S_2 = 9$, $I_1 = 2$, $I_2 = 7.5$, $S_3 = 1$, $S_4 = 1.25$, $S_5 = 0.2$, $S_6 = 0.2$, $I_3 = 3.25$, $I_4 = 4.33$, $R_1 = 5$, $R_2 = 2$ (all units are in mm).

To obtain the tri-band at ultra-wide frequency, the optimization is analyzed with HFSS and presented the design and results in Fig. 2 and also in Fig. 3 of the proposed hexagon slits and slots patch antenna.

The resonant frequency of hexagon patch is given with the following equation [13–15] as,

$$f_r = \frac{8.794}{r_e\sqrt{\varepsilon_r}} \tag{1}$$

The substrate is metallized with dual hexagonal patch and the side length (L_4) can be calculated by the following equation

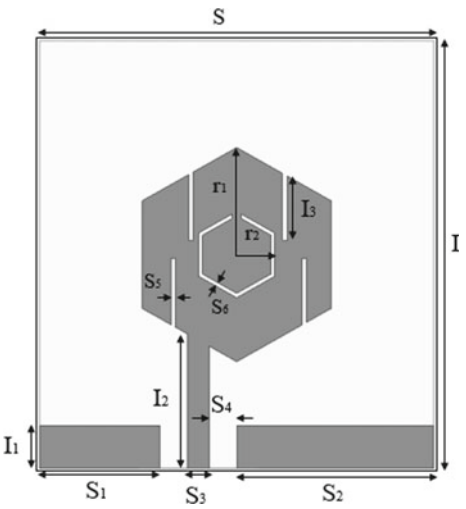


Fig. 1 Proposed hexagon slits and slots patch antenna

Fig. 2 Fabricated prototype of the proposed hexagon slits and slots patch antenna

$$L_4 = 2r_1 \sin\left(\frac{\pi}{n}\right) \tag{2}$$

n number of sides;
r_1 radius

As the slits and slots patch antenna is designed for ultra-wide application, the dimensions of the proposed antenna are very compact and flexible. The dimensions of the antenna are given as 20×18 mm^2.

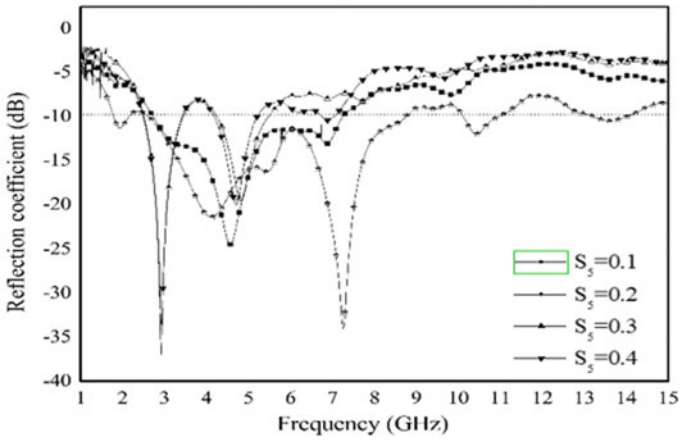


Fig. 3 Parametric sweep of hexagon slits and slots patch antenna for S_5

3 Results and Discussions

The antenna is designed and analyzed using Ansys HFSS simulation software. Figure 3 represents the reflection coefficient of the hexagon slits and slots patch antenna. The hexagon slits and slots patch antenna resonates for entire ultra-wide frequency. The prototype of hexagon slits and slots patch antenna is given in Fig. 2.

Parametric Analysis

In the process of optimization, to enhance the parameters of the antenna, a parametric set has been considered, and the width of the slots is varied to obtain a better S_{11} in. Figure 2 shows the reflection coefficient plot of parametric analysis.

The parametric analysis for the hexagon slits and slots patch is considered to get better understanding of the antenna. Two parameters are considered which might enhance the operation of the antenna to broadband. The parameters S_5 and S_6 are considered for optimization of the results. Figure 2 represents the optimizations analyzed for parameter S_5, width of the slits. The values range from 0.1 mm to 0.4 mm. The better result is observed when S_5 is 0.2 mm.

The second parameter considered for the optimizations is S_6, width of the split. The splits are considered to increase the current path. The width is varied from 0.4 mm to 0.1 mm. The proposed antenna is optimized at 0.2mm width and the best result in the considered width range. Figure 4 represents the S_{11} for the optimizations analyzed for S_6.

Table 1 shows the reflection coefficient values for the optimization analysis of S_5 and S_6. Each of the parameter is varied for four steps and plotted the reflection coefficient comparison. The simulated and measured reflection coefficient pattern are presented in Fig. 5.

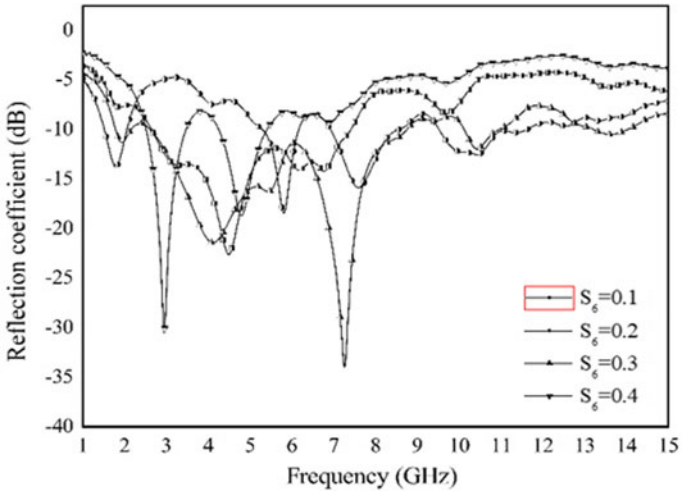
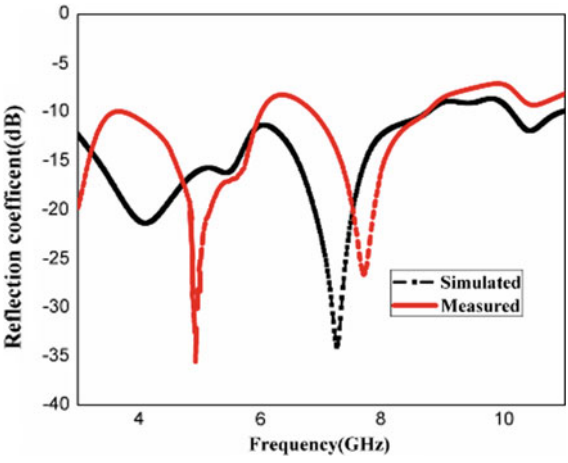


Fig. 4 Parametric sweep of hexagon slits and slots patch antenna for S_6

Table 1 Parametric analysis of the proposed antenna

S. No.	S_5	Reflection coefficient (dB)	S_6	Reflection coefficient (dB)
1	0.1	−24.455, −13.01, −13.07	0.4	−22.58, −14.09
2	0.2	−21.42, −34.01, −11.96	0.3	−18.40, −15.86, −12.59
3	0.3	−33.56, −19.58	0.2	−21.425, −34.01, −11.96
4	0.4	−36.95, −20.01, −10.42	0.1	−30.56, −18.68

Fig. 5 Simulation and measurement return loss



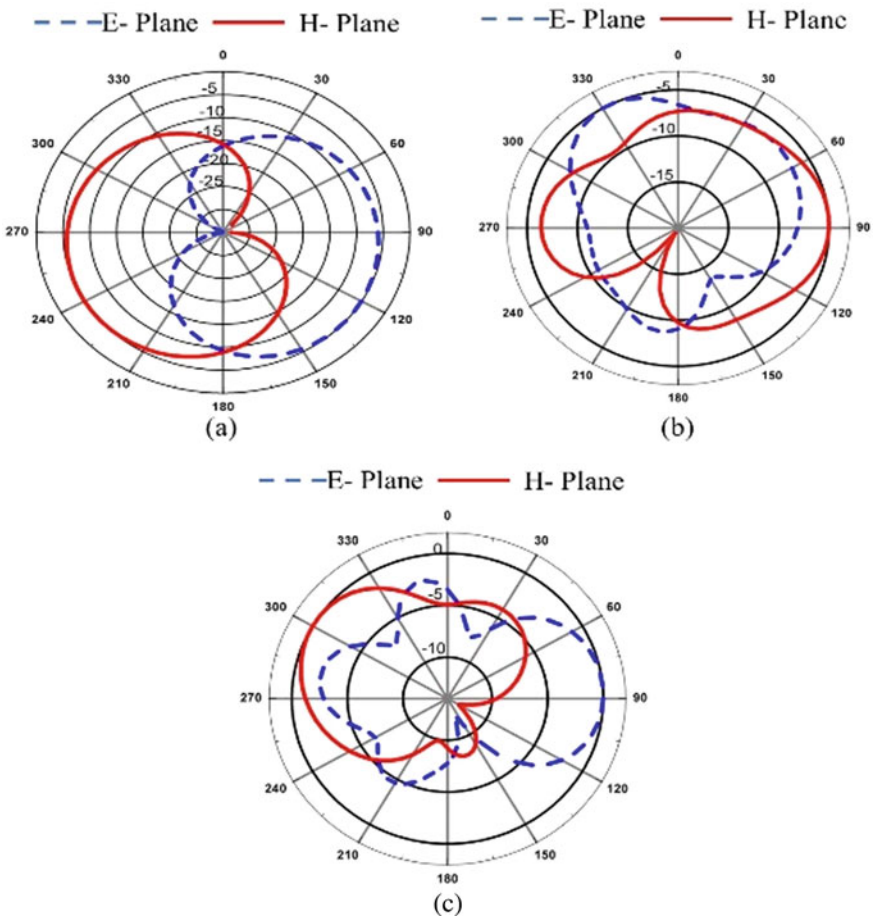


Fig. 6 Radiation patterns for the proposed antenna model **a** 4.2 GHz. **b** 7.2 GHz. **c** 10.42 GHz

Figure 6 represents the radiation patterns for designed antenna. At operating frequency of 4.2 GHz, the antenna radiates maximum at 130° (E-Plane) and 235° (H-Plane), at resonant frequency of 7.2 GHz, major radiation is at 335° (E-Plane) and 85° (H-Plane), and for operating frequency of 10.42 GHz maximum radiation is at 85° (E-Plane) and 300° (H-Plane).

Figure 7 shows the gain observed for proposed antenna at three operating frequencies 4.2 GHz, 7.2 GHz, 10.42 GHz are −8.74 dB, −16.38 dB, -9.33dB respectively, and the negative gain is due to the lossy tissue surrounding the CHCP antenna.

Figure 8 shows the current distribution (CD) of the proposed antenna at frequency 4.2 GHz, 7.2 GHz, and 10.42 GHz. The below figure shows current density of proposed antenna along with current density meter for each operating frequency. The comparative analysis of the proposed antenna with existing antennas is tabulated in Table 2.

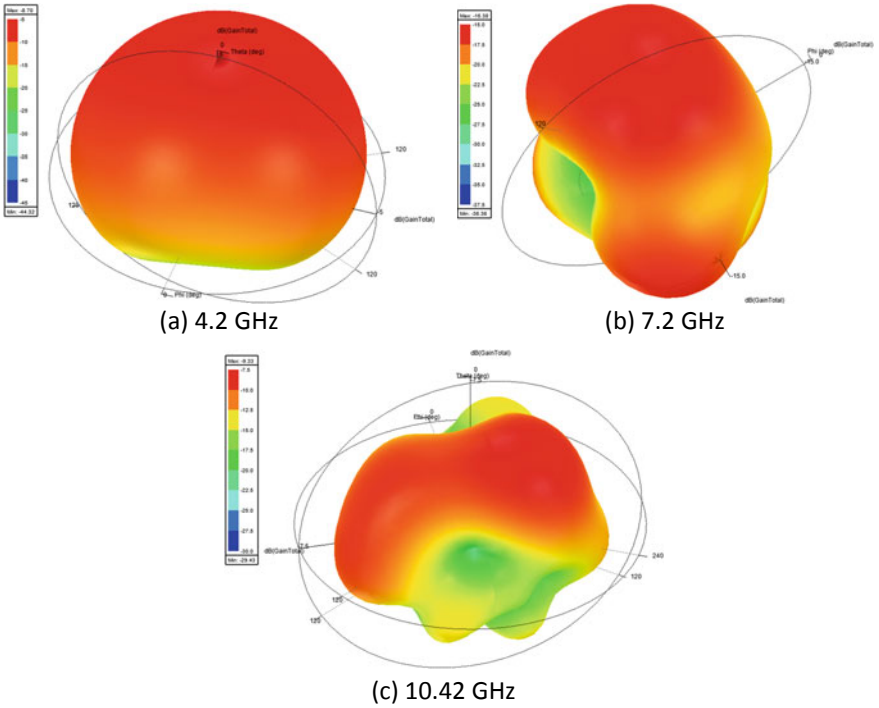


Fig. 7 Gain of the antenna **a** 4.2 GHz. **b** 7.2 GHz. **c** 10.42 GHz

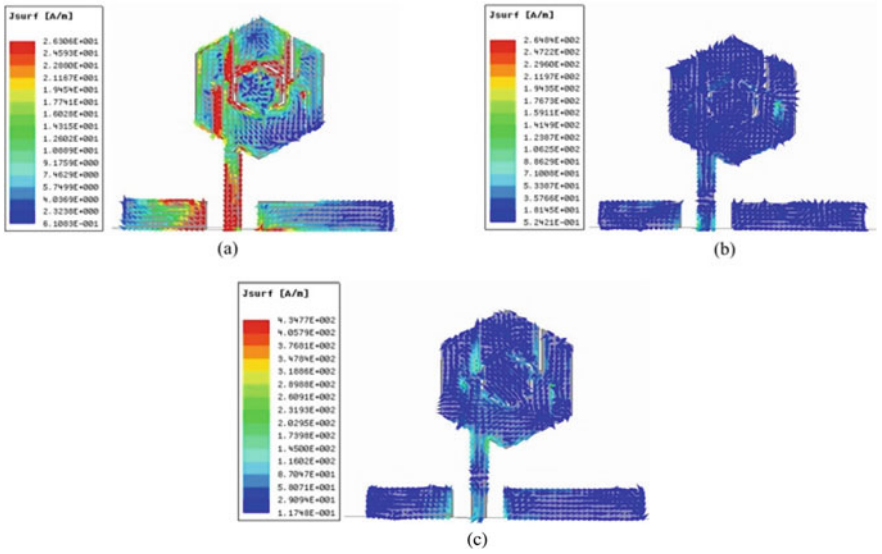


Fig. 8 Current distribution of the hexagon slits and slots patch antenna at **a** 4.2 GHz. **b** 7.2 GHz. **c** 10.42 GHz

Table 2 Comparative study of proposed antenna with existing works

Reference number	Antenna size (L × W × h) in mm	Return loss (dB)	Operating frequency (GHz)
3	25 × 22 × 10	−40	6
5	25 × 10 × 1.6	−30	7
7	27 × 27 × 1.6	−30	4.2
8	26.5 × 25 × 0.07	−30	2.4
Proposed work	20 × 18 × 0.07	−21.42 −34.01 −11.96	4.2 7.2 10.42

4 Conclusions

In this paper, we have designed and tested an UWB antenna for the on-body application. We proposed the antenna as a repeater by incorporating it into the on-body configuration. This can be done by placing the antenna on the skin to repeat the signals sent by the IMD. The process of repeating saves the power utilized by the IMD. The PEPA antenna is operating entirely in UWB band.

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Computationally Efficient Direction of Arrival Estimation of Coherent Signals for Three Parallel Uniform Linear Arrays

Kumar Gowri, Ponnusamy Palanisamy, and Chintagunta Srinivas

Abstract This chapter investigates the problem of two-dimensional (2D) direction of arrival (DOA) estimation of coherent signals with low complexity and automatic pairing of 2D angles. The new method incorporates the unitary ESPRIT into three parallel uniform linear array structures. Due to real-valued operations in unitary ESPRIT, the proposed method is computationally efficient. Further, without any additional processing, the proposed one resolves the coherent signals with automatic pairing the 2D angles. Simulation results are performed to demonstrate the efficacy of the proposed method and compared with the Cramer–Rao lower bound and the propagator method that are available in the existing literature. The results achieved by the proposed method were found to be significant in terms of estimation accuracy, resolution, and the computational complexity.

Keywords Coherent signals · Unitary ESPRIT · Low complexity · Automatic pairing

1 Introduction

Direction of arrival (DOA) estimation using sensor arrays has been playing an important role in array signal processing applications, including radar, sonar, wireless communications, and so on [1, 2]. In these applications, various subspace-based methods such as MUSIC [3], ESPRIT [4], and the propagator method (PM) [5–7] have been widely used for the direction finding. The MUSIC and ESPRIT methods

K. Gowri (✉) · P. Palanisamy
Department of Electronics and Communication Engineering, National Institute of Technology, Tiruchirappalli 620015, India
e-mail: gowri.nitt@gmail.com

C. Srinivas
Department of Electronics and Communication Engineering, International Institute of Information Technology, Bhubaneswar, India

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need eigenvalue decomposition of received signal covariance matrix which is computationally expensive. The PM is based on just the linear operations of the covariance matrix and does not require any eigenvalue decomposition. Thus, the PM is computationally efficient as compared to the ESPRIT and MUSIC.

The methods of [3–8] mainly focus on linear array and only one-dimensional DOA can be estimated. For estimating the two-dimensional (2D) DOAs that is both the azimuth and elevation angle, the MUSIC method requires 2D searching which is heavier computational load and the other two methods require a planar kind of array geometry.

For 2D-DOAs estimation, various array geometries such as rectangular array [9, 10], L-shaped array [11, 12], and parallel array [6, 7, 13, 14] have been developed. In particular, the parallel array-based structures have attracted much attention due to its simplicity and effectiveness. Wu et al. [15], Li et al. [16] developed propagator method for the two parallel array structures. Tayem and Kwon [6] constructed a structure based on three parallel arrays and showed that it has significant improvement in performance as compared to the two parallel array structures developed by Wu et al. [15], Li et al. [16]. Further, the 2D angles are automatically paired with the structure [6], whereas the structure developed by Li et al. [16] requires additional processing for pair-matching. Though the three parallel array structure has advantages, the method by Tayem and Kwon [6] exhibits worse performance and resolves less number of signals. This is due to the propagator method exploited for estimation where the propagator matrix misses some elements. Recently, considering the same three parallel array structures, Chen et al. [7] proposed the propagator-based approach by making the full use of elements which lead to the improvement in angle estimation performance. Moreover, the above-said methods developed by considering the received signals are uncorrelated, but in practice, coherent signals will occur frequently. The PM method in [6, 7, 13, 14] as well as the MUSIC [3, 8] and ESPRIT [4] fails when the received signals are coherent because of deficiency in the rank of a covariance matrix. Though the spatial smoothing is a classical preprocessing algorithm to resolve the rank deficiency [13, 17], it diminishes the effective aperture length of the array which leads to the reduction in performance as well as the number of resolvable signals.

Therefore, the objective of this paper is to propose a method for estimating the 2D-DOAs of coherent signals with reduced complexity as well as the improved estimation performance. To attain the objective, this paper considers the optimum structure that is three parallel uniform linear arrays and then the unitary ESPRIT is incorporated into the structure for desired parameter estimation. The proposed approach resolves more number of signals by making the full use of elements of the structure than the method by Tayem and Kwon [6], Chen et al. [7]. In particular, it is computationally efficient than the method by Chen et al. [7] which is due to the presence of real-valued operations in the unitary ESPRIT. Further, the proposed methodology resolves coherent signals without any preprocessing and also exhibits significant improvement in performance than the method by Chen et al. [7]. As like the pairing property of [6, 18–20], the azimuth and elevation angles can pair automatically without any additional processing in the proposed method.

1.1 Notations

Throughout the paper, vectors and matrices are represented with the lowercase and uppercase bold characters, respectively. The superscripts $(.^*)$, $(.^T)$, $(.^{-1})$, $(.^H)$, and $(.^\#)$ denote the conjugate, transpose, inversion, Hermitian transpose, and the Moore–Penrose inverse, respectively. $E[.]$ is the expectation operator, $\otimes$ indicates the Kronecker product, and $\odot$ indicates the Hadamard-product. Re{.} and Im{.} give the real and imaginary values of the entries, respectively. I_n is an $n \times n$ identity matrix, and $O_{m\times n}$ is the $m \times n$ zeros matrix. diag{.} constructs the diagonal matrix with all entries on its main diagonal.

2 Signal Model

Consider three uniform linear arrays parallel to the y-axis as shown in Fig. 1 in which each array comprises M sensors with $d = \lambda/2$ inter-sensor spacing. Suppose the array positioned along the y-axis is reference array. The other two arrays are placed next to the reference array with distance $d = \lambda/2$ in z-direction and x-direction, respectively. There are K far-field narrow band signals with different DOAs impinging on the structure as shown in Fig. 1. Let ϕ_k and θ_k be the azimuth and elevation angle of the kth signal $s_k(l), k = 1, \ldots, K$. Then, the output of each array at lth snapshot can be expressed as,

$$y_i(l) = \boldsymbol{A}_i \boldsymbol{s}(l) + \boldsymbol{w}_i(l); i = 1, 2, 3 \tag{1}$$

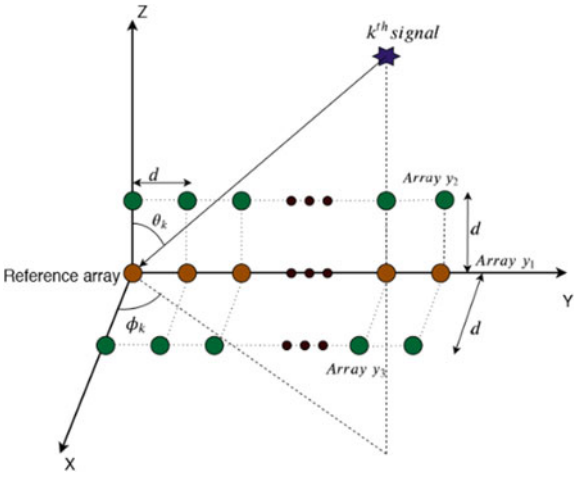

Fig. 1 Three parallel array configurations for 2D DOA estimation

where $y_1(l)$, $y_2(l)$ and $y_3(l)$ are the outputs of the arrays in y-axis, yz plane, and the xy-plane, respectively; $\boldsymbol{A}_1 = [a_1(\theta_1, \varphi_1), \ldots, a_1(\theta_K, \varphi_K)]$ denotes steering matrix of the array along y-axis in which $a_1(\theta_k, \varphi_k) = \left[1, \alpha_k, \ldots, \alpha_k^{M-1}\right]^T; 1, \ldots, K$ being the steering vector with a progressive phase-shift factor $\alpha_k = \mathrm{e}^{-j2\pi \frac{d}{\lambda} \sin\theta_k \sin\varphi_k}$ concerning the kth signal; $\boldsymbol{A}_2 = [a_2(\theta_1, \varphi_1), \ldots, a_2(\theta_K, \varphi_K)]$ denotes the steering matrix of the array in yz-plane in which $a_2(\theta_k, \varphi_k) = \left[\beta_k, \beta_k\alpha_k, \ldots, \beta_k\alpha_k^{M-1}\right]^T; 1, \ldots, K$ being the steering vector with $\beta_k = \mathrm{e}^{-j2\pi \frac{d}{\lambda} \cos\theta_k}$; $\boldsymbol{A}_3 = [a_3(\theta_1, \varphi_1), \ldots, a_3(\theta_K, \varphi_K)]$ denotes the steering matrix of the array in xy-plane in which $a_3(\theta_k, \varphi_k) = \left[\gamma_k, \gamma_k\alpha_k, \ldots, \gamma_k\alpha_k^{M-1}\right]^T; 1, \ldots, K$ being the steering vector with $\gamma_k = \mathrm{e}^{-j2\pi \frac{d}{\lambda} \sin\theta_k \cos\varphi_k}$. $S(l) = [s_1(l), \ldots, s_k(l)]^T$ represents the source signals complex coefficient vector; and $w_i(l); i = 1, 2, 3$ represents the noise vectors at the output of the concerning arrays. The composite signal $y(l)$ of the structure in Fig. 1 can be expressed as [1],

$$\boldsymbol{y}(l) \triangleq [\boldsymbol{y}_1^T(l), \boldsymbol{y}_2^T(l), \boldsymbol{y}_3^T(l)]^T = \boldsymbol{A}\boldsymbol{S}(l) + \boldsymbol{w}(l) \tag{2}$$

where $\boldsymbol{A} = \left[\boldsymbol{A}_1^T(l), \boldsymbol{A}_2^T(l), \boldsymbol{A}_3^T(l)\right]^T$ and $\boldsymbol{w} = \left[\boldsymbol{w}_1^T(l), \boldsymbol{w}_2^T(l), \boldsymbol{w}_3^T(l)\right]^T$. Therefore, the covariance matrix of $\boldsymbol{y}(l)$ can be expressed as,

$$\boldsymbol{R}_y = E\left[\boldsymbol{y}(l)\boldsymbol{y}^H(l)\right] = \boldsymbol{A}\boldsymbol{R}_s\boldsymbol{A}^H + \boldsymbol{R}_w \tag{3}$$

where $\boldsymbol{R}_s = E\left[\boldsymbol{s}(l)\boldsymbol{s}^H(l)\right]$ is the source signals covariance matrix and $\boldsymbol{R}_w = E\left[\boldsymbol{w}(l)\boldsymbol{w}^H(l)\right]$ is the noise covariance matrix. Although the structure shown in Fig. 1 has an improved angle estimation performance [7], the method employed for estimation has a tremendous calculation burden and also fails when the signals are coherent. The former fact is because of exploiting the complex-valued data, whereas the later one is due to rank inadequacy of the covariance matrix $\boldsymbol{R}_y$. Consequently, this paper proposes an approach for the structure shown in Fig. 1 to estimate the 2D-DOAs of coherent signals with reduced complexity as well as improved angle estimation performance which is described in detail in the following section.

3 Proposed Method for 2D DOA Estimation

This section describes the proposed approach that is unitary ESPRIT based on the structure as shown in Fig. 1, for estimating the 2D-DOAs of coherent signals. The proposed approach firstly constructs two new data vectors $\boldsymbol{x}_1(l)$ and $\boldsymbol{x}_2(l)$ by concatenating $\boldsymbol{y}_1(l)$, $\boldsymbol{y}_2(l)$ and $\boldsymbol{y}_1(l)$, $\boldsymbol{y}_3(l)$, respectively.

The new data vectors $\boldsymbol{x}_1(l) \in C^{2M\times 1}$ and $\boldsymbol{x}_2(l) \in C^{2M\times 1}$ can be expressed as,

$$\boldsymbol{x}_l(l) = \left[\boldsymbol{y}_1^T(l), \boldsymbol{y}_2^T(l)\right]^T = \boldsymbol{B}_1\boldsymbol{S}(l) + \boldsymbol{n}_1(l) \tag{4}$$

$$\boldsymbol{x}_2(l) = \left[\boldsymbol{y}_1^T(l), \boldsymbol{y}_3^T(l)\right]^{\boldsymbol{T}} = \boldsymbol{B}_2\boldsymbol{S}(l) + \boldsymbol{n}_2(l) \tag{5}$$

where $\boldsymbol{B}_1 \triangleq [b_1(\theta_1, \varphi_1), \ldots, b_1(\theta_K, \varphi_K)] = \left[\boldsymbol{A}_1^T, \boldsymbol{A}_2^T\right]^T$, $\boldsymbol{n}_1 = [\boldsymbol{w}_1^T, \boldsymbol{w}_2^T]^T$; $\boldsymbol{B}_2 \triangleq [b_2(\theta_1, \varphi_1), \ldots, b_2(\theta_K, \varphi_K)] = \left[\boldsymbol{A}_1^T, \boldsymbol{A}_3^T\right]^T$, $\boldsymbol{n}_1 = [\boldsymbol{w}_1^T, \boldsymbol{w}_3^T]^T$. Now, the unitary ESPRIT is employed on the signal models $\boldsymbol{x}_l(l)$ in (5) and $\boldsymbol{x}_2(l)$ in (6). It, initially, comprises doubling the number of snapshots and then transforming into the real-valued data via unitary transformation. Let $\boldsymbol{X}_1 = [\boldsymbol{x}_l(l), \ldots . \boldsymbol{x}_l(L)]$ and $\boldsymbol{X}_2 = [\boldsymbol{x}_2(l), \ldots . \boldsymbol{x}_2(L)]$ be the data matrices composed of L snapshots of $\boldsymbol{x}_l(l)$, and $\boldsymbol{x}_2(l)$, $1, \ldots, L$, respectively. The extended data matrices with $2L$ snapshots can be defined as $\boldsymbol{Z}_1 = \left[\boldsymbol{X}_1\boldsymbol{\Pi}_{2M}\boldsymbol{X}_1^*\boldsymbol{\Pi}_L\right] \in C^{2M\times 2L}$ and $\boldsymbol{Z}_2 = \left[\boldsymbol{X}_2\boldsymbol{\Pi}_{2M}\boldsymbol{X}_2^*\boldsymbol{\Pi}_L\right] \in C^{2M\times 2L}$ where $\boldsymbol{\Pi}_n$ is an $n \times n$ exchange matrix with ones on its anti-diagonal and zeros elsewhere. It can be exhibited that $\boldsymbol{Z}_1$ and $\boldsymbol{Z}_2$ are centro-Hermitian matrices [30]. Then, the unitary transformation of the complex-valued matrices $\boldsymbol{Z}_1$ and $\boldsymbol{Z}_2$ to the real-valued ones $\boldsymbol{Z}_1^{(r)} \in \mathbb{R}^{2M\times 2L}$ and $\boldsymbol{Z}_2^{(r)} \in \mathbb{R}^{2M\times 2L}$, respectively, can be obtained as,

$$\boldsymbol{Z}_t^{(r)} = \boldsymbol{Q}_{2M}^H\boldsymbol{Z}_t\boldsymbol{Q}_{2L}; t = 1, 2 \tag{6}$$

where $\boldsymbol{Q}_n$ is the $n \times n$ sparse unitary matrix. As $n = 2M$ or $n = 2L$ that is always even, $\boldsymbol{Q}_n$ can be expressed as,

$$\boldsymbol{Q}_n = \frac{1}{\sqrt{2}}\begin{bmatrix} \boldsymbol{I}_{n/2} & j\boldsymbol{I}_{n/2} \\ \Pi_{n/2} & -j\boldsymbol{I}_{n/2} \end{bmatrix} \tag{7}$$

Therefore, using the maximum likelihood estimation, the real-valued covariance matrix of $\boldsymbol{Z}_t^{(r)}, t = 1, 2$ can be estimated as,

$$\hat{\boldsymbol{R}}_t^{(r)} = \frac{1}{2L}\boldsymbol{Z}_t^{(r)}\left(\boldsymbol{Z}_t^{(r)}\right)^H, t = 1, 2 \tag{8}$$

The vector $b_1(\theta_k, \varphi_k)$; for all $k = 1, \ldots, K$ satisfies the shift-invariance property in two different ways—one is with phase-shift α_k and the other is with phase-shift β_k. Thus, these invariance properties concerning all the signals can be expressed as,

$$\boldsymbol{J}_1\boldsymbol{B}_1\Phi_\alpha = \boldsymbol{J}_2\boldsymbol{B}_1 \text{ and } \boldsymbol{J}_3\boldsymbol{B}_1\Phi_\beta = \boldsymbol{J}_4\boldsymbol{B}_1 \tag{9}$$

where $\boldsymbol{J}_1 = \boldsymbol{I}_2 \otimes [\boldsymbol{I}_{M-1}|\boldsymbol{O}_{(M-1)\times 1}]$; $\boldsymbol{J}_2 = \boldsymbol{I}_2 \otimes [\boldsymbol{O}_{(M-1)\times 1}|\boldsymbol{I}_{M-1}]$; $\boldsymbol{J}_3 = [\boldsymbol{I}|\boldsymbol{O}] \otimes \boldsymbol{I}_M$ and $\boldsymbol{J}_4 = [\boldsymbol{O}|\boldsymbol{I}] \otimes \boldsymbol{I}_M$ are the appropriate selection matrices; $\Phi_\alpha = \text{diag}\{\alpha_1, \ldots, \alpha_K\}$ and $\Phi_\beta = \text{diag}\{\beta_1, \ldots, \beta_K\}$. Similarly, the two invariance properties of the matrix $\boldsymbol{B}_2$ can be expressed as,

$$\boldsymbol{J}_1\boldsymbol{B}_2\Phi_\alpha = \boldsymbol{J}_2\boldsymbol{B}_2 \text{ and } \boldsymbol{J}_3\boldsymbol{B}_2\Phi_\gamma = \boldsymbol{J}_4\boldsymbol{B}_2 \tag{10}$$

where $\Phi_\gamma = \text{diag}\{\gamma_1, \ldots, \gamma_K\}$. As the data model $\boldsymbol{Z}_t^{(r)}; t = 1, 2$ in Eq. (6) is real-valued, the complex-valued invariance properties represented in (9) and (10) can be transformed into the real-valued one,

$$\begin{aligned} \boldsymbol{K}_1 \boldsymbol{D}_t \Gamma_u &= \boldsymbol{K}_2 \boldsymbol{D}_t; t = 1, 2 \\ \boldsymbol{K}_3 \boldsymbol{D}_1 \Gamma_v &= \boldsymbol{K}_4 \boldsymbol{D}_1 \\ \boldsymbol{K}_3 \boldsymbol{D}_2 \Gamma_w &= \boldsymbol{K}_4 \boldsymbol{D}_2 \end{aligned} \tag{11}$$

where $\boldsymbol{D}_t = \boldsymbol{Q}_{2M}^H \boldsymbol{B}_t; t = 1, 2$ denotes the transformed steering matrix; $\boldsymbol{K}_1 = 2\text{Re}\{\boldsymbol{Q}_{2(M-1)}^H \boldsymbol{J}_2 \boldsymbol{Q}_{2M}\}$; $\boldsymbol{K}_2 = 2\text{Im}\{\boldsymbol{Q}_{2(M-1)}^H \boldsymbol{J}_2 \boldsymbol{Q}_{2M}\}$; $\boldsymbol{K}_3 = 2\text{Re}\{\boldsymbol{Q}_M^H \boldsymbol{J}_4 \boldsymbol{Q}_{2M}\}$ and $\boldsymbol{K}_4 = 2\text{Im}\{\boldsymbol{Q}_M^H \boldsymbol{J}_4 \boldsymbol{Q}_{2M}\}$ are the transformed selection matrices. $\Gamma_u = \text{diag}\{\tan\frac{\pi d u_1}{\lambda}, \ldots, \tan\frac{\pi d u_k}{\lambda}\}$; $u_k = \sin\theta_k \sin\varphi_k$, $\Gamma_v = \text{diag}\{\tan\frac{\pi d v_1}{\lambda}, \ldots, \tan\frac{\pi d v_k}{\lambda}\}$; $v_k = \cos\theta_k$, and $\Gamma_w = \text{diag}\{\tan\frac{\pi d w_1}{\lambda}, \ldots, \tan\frac{\pi d w_k}{\lambda}\}$; $w_k = \sin\theta_k \cos\varphi_k$, with $k = 1, \ldots, K$ are the real-valued phase-shift factors and contain the desired *DOAs* information. Although $\boldsymbol{D}_t, t = 1, 2$ is not available at the receiver associated with a particular signal, it can estimate from the signal subspace of the covariance matrix $\hat{\boldsymbol{R}}_t^{(r)}$. Let $\boldsymbol{E}_1$ and $\boldsymbol{E}_2$ be the real-valued signal subspace of $\hat{\boldsymbol{R}}_1^{(r)}$ and $\hat{\boldsymbol{R}}_2^{(r)}$, respectively. In no noise situation, $\boldsymbol{E}_1$ and $\boldsymbol{E}_2$ can be related to $\boldsymbol{D}_1$ and $\boldsymbol{D}_2$ as $\boldsymbol{E}_1 = \boldsymbol{D}_1 \boldsymbol{T}$ and $\boldsymbol{E}_2 = \boldsymbol{D}_2 \boldsymbol{T}$, respectively, where $\boldsymbol{T}$ is the $k \times kk \times k$ non-singular matrix. Thus, exploiting $\boldsymbol{D}_1 = \boldsymbol{E}_1 \boldsymbol{T}^{-1}$ and $\boldsymbol{D}_2 = \boldsymbol{E}_2 \boldsymbol{T}^{-1}$, the real-valued invariance properties in Eq. (11) can be expressed as,

$$\begin{aligned} K_1 E_t \Omega_u &= K_2 E_t t = 1, 2 \\ K_3 E_1 \Omega_v &= K_4 E_1 \\ K_3 E_2 \Omega_w &= K_4 E_2 \end{aligned} \tag{12}$$

where $\Omega_u = \boldsymbol{T}^{-1} \Gamma_u \boldsymbol{T}$, $\Omega_v = \boldsymbol{T}^{-1} \Gamma_v \boldsymbol{T}$, $\Omega_w = \boldsymbol{T}^{-1} \Gamma_w \boldsymbol{T}$. It signifies that the diagonal elements of Γ_u, Γ_v, Γ_w are the eigenvalues of Ω_u, Ω_v, Ω_w can be obtained from the least squares solution of the concerning invariance relation in (12). Further, as Ω_u, Ω_v, Ω_w are real-valued matrices, both $\Omega_u + j\Omega_v$ and $\Omega_u + j\Omega_w$ can be spectrally decomposed as,

$$\Omega_u + j\Omega_v = \boldsymbol{T}^{-1}(\Gamma_u + \text{j}\Gamma_v)\boldsymbol{T} \text{ and } \Omega_u + j\Omega_w = \boldsymbol{T}^{-1}(\Gamma_u + j\Gamma_w)\boldsymbol{T} \tag{13}$$

From Eq. (13), the automatically paired $\{u_k \& v_k\}/\{u_k \& w_k\}, k = 1, \ldots, K$ can be obtained from the real and imaginary eigenvalues of $\{\Omega_u + j\Omega_v\}/\Omega_u + j\Omega_w$, respectively.

Therefore, the mutually paired $\{u_k, v_k, w_k\}\{u_k, v_k, w_k\}; k = 1, \ldots, K$ are,

$$u_k = \frac{\lambda}{\pi d} \tan^{-1}\left(\text{Re}\left\{\left[\text{eig}\{\Omega_{uv}\}\right]_{kk}\right\}\right) \text{or}$$
$$\frac{\lambda}{\pi d} \tan^{-1}\left(\text{Re}\left\{\left[\text{eig}\{\Omega_{uv}\}\right]_{kk}\right\}\right)$$

$$v_k = \frac{\lambda}{\pi d}\tan^{-1}\left(\mathrm{Im}\left\{\left[\mathrm{eig}\{\Omega_{uv}\}\right]_{kk}\right\}\right)$$
$$w_k = \frac{\lambda}{\pi d}\tan^{-1}\left(\mathrm{Im}\left\{\left[\mathrm{eig}\{\Omega_{uw}\}\right]_{kk}\right\}\right) \quad (14)$$

where $\Omega_{uv} = \Omega_u + j\Omega_v$ and $\Omega_{uw} = \Omega_u + j\Omega_w$. Hence, the automatically paired elevation and azimuth angle estimates are,

$$\hat{\theta}_k = \sin^{-1}\left(\sqrt{u_k^2 + v_k^2}\right)\hat{\theta}_k = \sin^{-1}\left(\sqrt{u_k^2 + v_k^2}\right) \text{and}\, \hat{\theta}_k = \sin^{-1}\left(\frac{u_k}{w_k}\right) \quad (15)$$

4 Cramer–Rao Lower Bound and Computational Complexity Analysis

CRB of 2D direction of arrival estimation [31] is given by,

$$\mathrm{CRB} = \frac{\sigma^2}{2L}\left\{\mathrm{Re}\left\{F^H\left(\Pi\frac{1}{A}\right)\mathrm{F}\odot\hat{P}_y^T\right\}\right\}^{-1} \quad (16)$$

where $\sigma^2\sigma^2$ is the variance of Gaussian white noise, $F \triangleq \left[\frac{\partial a_1}{\partial\theta_1},\ldots,\frac{\partial a_K}{\partial\theta_K},\frac{\partial a_1}{\partial\phi_1},\ldots,\frac{\partial a_K}{\partial\phi_K}\right]$ with a_i being the ith column of $\boldsymbol{A}$, $\hat{P}_y = \begin{bmatrix}\hat{P}_s & \hat{P}_s\\ \hat{P}_s & \hat{P}_s\end{bmatrix}$ with $\hat{\boldsymbol{P}}_{\boldsymbol{s}} = \frac{1}{\boldsymbol{L}}\sum_{l=1}^{\boldsymbol{L}}\boldsymbol{s}(l)\boldsymbol{s}^H(l)$ and $\Pi\frac{1}{A} = \boldsymbol{I}_{3M} - \boldsymbol{A}\left(\boldsymbol{A}^{\boldsymbol{H}}\boldsymbol{A}\right)^{-1}\boldsymbol{A}^{\boldsymbol{H}}$. We evaluate the computational complexity of the proposed method and compare it with the method by Chen et al. [7], which is shown in Fig. 2. The complexity of the proposed method mainly depends on the computation of covariance matrix (8), eigenvalue decomposition, finding the solutions of invariance Eqs. (12), spectral decomposition (13), and 2D DOA estimation. The complexity of (8) is $O\left(8M^2L\right)$, and its eigen decomposition requires $O\left(8M^3\right)$. The complexity to find the least squares solution of the invariance equations (13) involves $O\left(K^2 + 2K^2M\right)$ [32]. $O\left(K^3 + 2K^2\right)$ is required for spectral estimation (13) and DOA estimation. The computational complexity of the propagator method by Chen et al. [7], is $\mathrm{O}\left(4(3\mathrm{M}+1)^2\mathrm{L} + \mathrm{K}(3\mathrm{M}+1)(3\mathrm{M}+2-\mathrm{K}) + 12\mathrm{K}^3 + 2\mathrm{K}^2\right)$ per trial. A great reduction in complexity of the proposed method is due to real-valued computations. Figure 2 illustrates that the proposed method has significantly lower computational complexity than propagator method [7].

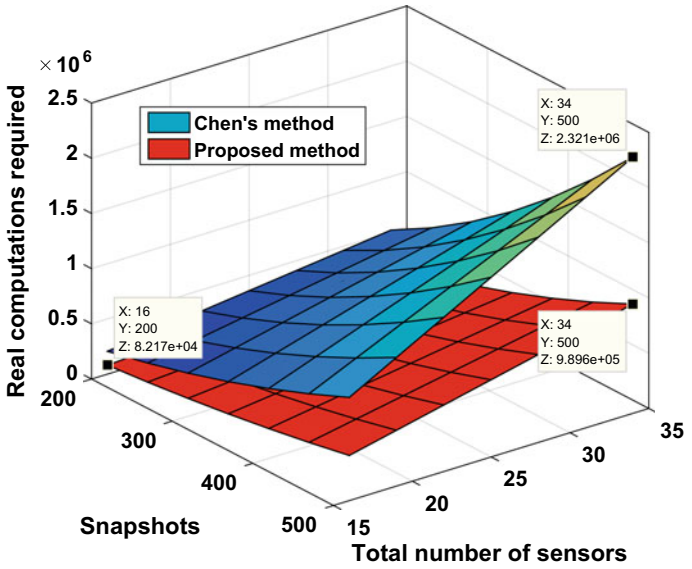

Fig. 2 Complexity performance comparison for equal number of sensors

5 Simulation Results

This section presents the Monte Carlo simulations to evaluate the effectiveness of the proposed method and compare with the CRB and the propagator method described in [7]. The effectiveness is measured concerning the accuracy, resolution, and the computational complexity. Accuracy is evaluated by the root-mean-squared error (RMSE) and scatter plot, whereas the resolution is done by the detection probability. The RMSE of a particular parameter estimation is defined by,

$$\text{RMSE}(\chi) = \sqrt{\frac{1}{N_s K} \sum_{k=1}^{K} \sum_{n=1}^{N_s} \left(\hat{\chi}_{k,n} - \chi_k\right)^2}; \chi = \theta, \phi \tag{17}$$

where χ represents the azimuth angle (ϕ) or elevation angle (θ) of kth signal, $\hat{\chi}_{k,n}$ denotes the estimated value of χ_k at nth Monte Carlo run, and N_s is the total number of Monte Carlo runs. The detection probability is computed statistically from the successful Monte Carlo runs. The Monte Carlo run is successful when the absolute estimation error is below a certain threshold. These accuracy and resolution performance attributes are evaluated on both the coherent and uncorrelated sources. The coherent sources are modeled as $s(l) = \boldsymbol{\rho} s_0(l)$ where $s_0(l) = e^{j\pi l/3L}$ and $\boldsymbol{\rho} \epsilon C^{k\times 1}$ denotes the magnitude and phase relationship among the sources. Throughout the simulation we consider the number of sensors $M = 6$, inter-sensor spacing $d = \lambda/2$,

number of snapshots $L = 300$, and the noise is white Gaussian with zero mean. All the simulations are conducted over $N_s = 1000$ Monte Carlo runs.

Figure 3 depicts the RMSE versus signal to noise ratio (SNR) performance for three sources. In Fig. 3, Fig. 3a illustrates the RMSE of elevation angle, whereas Fig. 3b illustrates the RMSE of azimuth angles. The directions of the three sources are considered as $\theta = (16°, 28°, 40°)$ and $\phi = (12°, 52°, 40°)$. For coherent sources generation, we set $\boldsymbol{\rho} = [1, 1 + j0.2, 0.8660 + j0.5]^{\boldsymbol{T}}$ for three sources. In case of three uncorrelated sources as shown in Fig. 4, performance of the proposed method is significantly good as compared to the method in [7]. For coherent sources, performance of the method in [7], is poor and constant even at high SNR whereas performance of the proposed method is significant irrespective of the sources are coherent or uncorrelated which is due to the existence of inherent forward-backward smoothing in unitary ESPRIT.

Figure 4 shows the RMSE performance versus angular separation δ between two sources at a fixed SNR of 5 dB. Thus, directions of the two sources are taken as $(\theta_1, \phi_1) = (35°, 25°)$ and $(\theta_2, \phi_2) = (35 + \delta°, 25 + \delta°)$ in which δ is ranging from 1^o to 10° with a grid of 1°.

Figure 5 illustrates the average detection probability of the azimuth and elevation angle versus SNR. In this analysis, two sources are considered with directions $\theta = (45°, 70°)$ and $\phi = (50°, 30°)$. The threshold for making a decision to a successful run is taken as 0.2°. The coefficient vector $\boldsymbol{\rho}$ for coherent sources generation is same as that in Fig. 3. From the results in Fig. 6 we observe that the proposed method able to detect the two sources significantly, e.g., at SNR $= -1 \sim$ dB, the detection probability is 100% and 99% respectively for uncorrelated and coherent sources, whereas the method by Chen et al. [7], fails for coherent signals and even the performance is lower for uncorrelated signals.

The scatter diagram of the proposed method for uncorrelated and coherent sources is presented in Fig. 6a, b, respectively. For this simulation, three sources are considered with $\theta = (30°, 15°, 45°)$ and $\phi = (10°, 55°, 40°)$ and SNR of 5 dB is considered. For coherent sources, the coefficient vector $\boldsymbol{\rho}$ is same as that in Fig. 3. The scatter points in Fig. 6 signify that the azimuth and elevation angles are accurately paired with high precision and accuracy.

6 Conclusions

In this paper, we incorporated the unitary ESPRIT into three parallel uniform linear array structures for estimating the 2D-DOA of coherent signals. The resulting approach estimates the azimuth and elevation angles through the estimation of mutually paired three directional cosines of the signal, and thus the angles are automatically matched. Because of the inherent smoothing and the real-valued operations in unitary ESPRIT, the proposed methodology resolves the coherent signals without any additional preprocessing technique and estimates the 2D-DOAs with reduced complexity. Simulation results signify that the estimation accuracy, resolution and

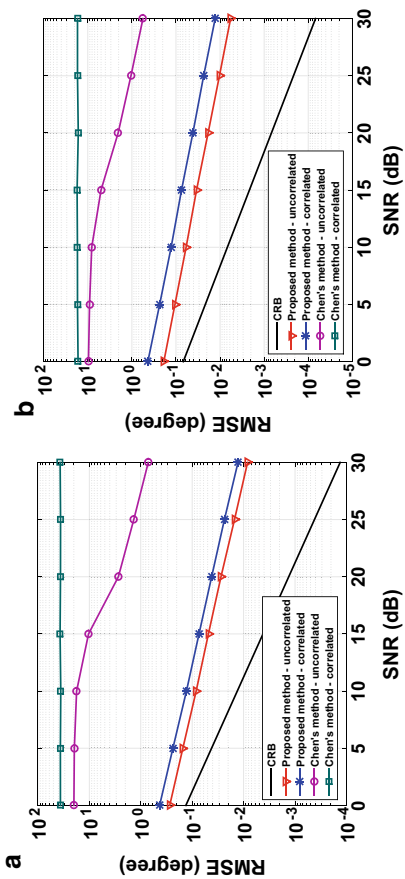

Fig. 3 RMSE versus SNR for three sources at $\theta = (16°, 28°, 40°)$ and $\phi = (12°, 52°, 40°)$. **a** For elevation angles, **b** for azimuth angles

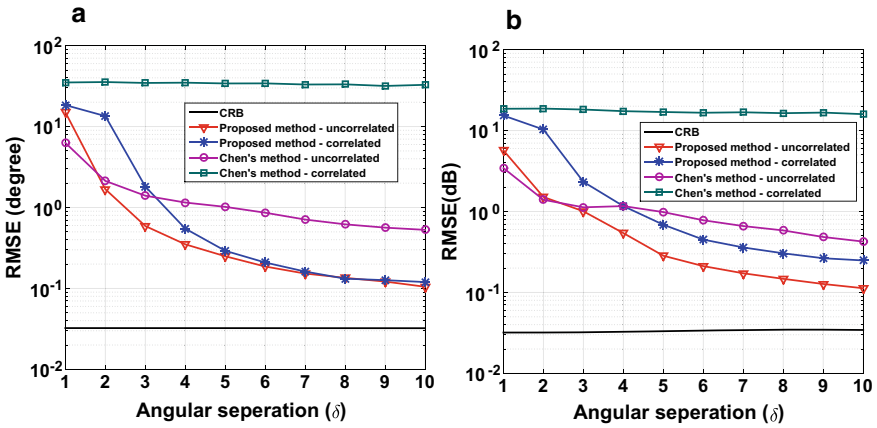

Fig. 4 RMSE of the DOA estimates versus angle shift at SNR = 5 dB. **a** For elevation angles, **b** for azimuth angles

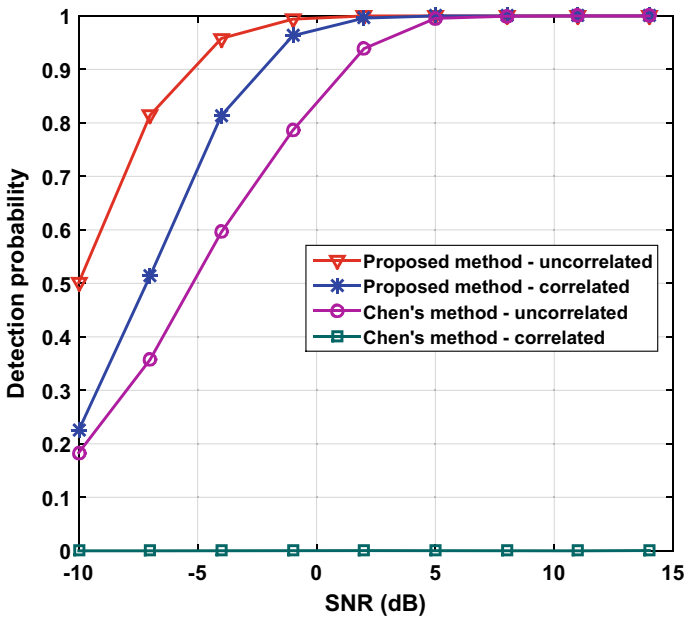

Fig. 5 Detection probability versus SNR for uncorrelated and coherent sources

the computational complexity performances of the proposed method are significantly better than the existing propagator method.

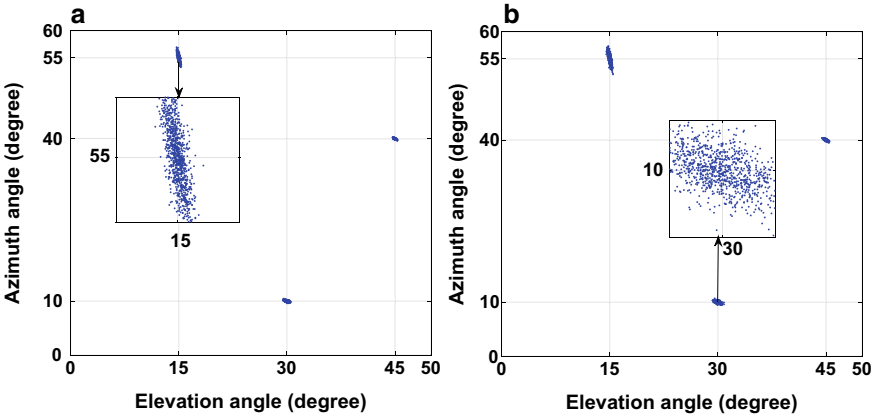

Fig. 6 Scatter diagram for uncorrelated and coherent signals of the proposed method. **a** For uncorrelated signals, **b** for coherent signals

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A Unique Case Study on Real-Valued Cost Analysis of a Small Solar Plant

Suman Ghosh, J. K. Das, and Chandan Kumar Chanda

Abstract Solar energy is emerging as one of the most promising sustainable energy sources. Solar photovoltaic systems vary greatly in terms of size and cost. Understanding the economics of a solar photovoltaic (PV) system is one of the most effective considerations when deciding on solar energy. In this paper, we focus on the cost analysis of a 5 kWp (Kilo Watt Peak) solar plant. Here, we calculate the payback period as well as the efficiency of the small solar plant. We also estimate the carbon footprint which is a very important factor for our environment.

Keywords Solar PV module · Monthly power consumption · Simple payback period · Carbon footprint

1 Introduction

In solar photovoltaic (PV) systems, solar energy is directly converted into electrical energy. PV Systems can be any size from a single panel about 200 W to hundreds of panels totaling tens of thousands of Watts [1, 2]. This paper aims to estimate real value cost analysis of the 5 kWp (Kilo Watt Peak) solar power plant at JIS College of Engineering (Fig. 1). This paper focuses on

- Estimation of cost for installation of 5 kWp solar photovoltaic power plant.
- Observation of the month-wise (Jan to Dec) consumption of power throughout the year.
- Simple payback period calculation of a 5 kWp solar photovoltaic (PV) power plant and payback period calculation with respect to changing the value of the money over time and degradation of the power generation of the system [3, 4].
- Estimation of carbon footprint.

S. Ghosh (✉) · J. K. Das
Department of Electrical Engineering, Guru Nanak Institute of Technology, Kolkata, India
e-mail: suman.ghosh@gnit.ac.in

C. K. Chanda
Department of Electrical Engineering, Indian Institute of Engineering Science and Technology, Shibpur, Kolkata, India

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Fig. 1 Solar photovoltaic power plant at JIS College of Engineering

2 Estimation of the Installation Cost of 5 kWp Solar PV Module

2.1 Cost of Solar Panels

The solar panels used here are manufactured by Sova Power Limited. The modules used are SS250P series 60 cells 250 Wp. The cost of a single panel is Rs. 11,102. Fifteen such panels are used. So, the total cost comes to Rs. 2,22,043. After including VAT at the rate of 5%, the final cost of the panels is Rs. 2,33,730.

2.2 Cost of Inverters

The inverter and power conditioning unit used are manufactured by KACO. The model is Powador 5002. The cost of the inverter is Rs. 1,18,000. After including VAT at the rate of 5%, the final cost of the inverter comes to Rs. 1,23,900.

2.3 Cost of Other Accessories

Other accessories used include 4 in 1 array junction box, module mounting structures, LT panel, cables, earthing system, lightning arrester, energy meter, temperature sensor, and other materials as per requirements is Rs. 3,40,370. So the total cost for setting up the plant comes to Rs. 6,98,000. Therefore, Cost/Wp = Rs. 6,98,000/5000 = Rs. 139.60.

3 Efficiency of PV Module

The efficiency of PV modules is calculated as follows:

A commercially available module has the following given parameters. The peak power rating of the module (Wp) and the area of the module (m^2). Dividing the peak power rating by the area of the module, we get Wp/m^2 [5, 6]. Since the modules are rated at STC of 1000 W/m^2, the efficiency of the module can be written as:

$$\text{Efficiency} = \left(\text{Wp}/\text{m}^2\right)/\left(1000\ \text{W}/\text{m}^2\right) \times 100\%$$

Now, the area of one module is $1.639 \times 0.639 = 1.609498\ m^2$

So, efficiency of our module = ((250/1.609498)/1000) × 100% = 15.53%

The efficiency rating of the modules provided by Sova Solar is 15%, so we have to take it for all calculations.

4 Observation of Month-Wise Power Consumption

The control room of the 5 kWp solar PV plant collects several values continuously. Here, we collect values like daily peak power, kWh, CO_2 savings, Mt. output in h., Opt. hrs for a day, energy meter readings, and load in kWh for the year 2014. The values of these parameters are collected month wise. Here, three sample month's (March, April, and May) energy consumption is given. In this way, energy consumption throughout a year is collected and analyzed (Tables 1, 2, 3 and 4).

5 Payback Period Analysis

A simplified form of cost/benefit analysis is a simple payback technique. In this method, the total cost of the system is divided by the first-year energy cost savings produced by the system [7].

Simple payback time (years) = Total cost of the system/Annual saving. The simple payback period is only a simplistic measure and gives the number of years needed for a system to pay itself off. It is considered that the modern, high quality solar panels have an expected life of approximately 30 years [8].

This method omits several significant cost factors, including the cost escalation rate and the cost of capital. Thus, simple payback analysis can overestimate the actual payback period and, consequently, the length of time to recoup the investment.

Total cost of the system = Rs. 6,98,000.

Electricity rate = Rs. 6/unit (according to WBSEDCL for the year 2013-14). (1unit = 1kWh).

Energy consumed by the plant in 1st year = 5222.5 kWh.

Table 1 Energy consumption for March 2014

Date	Daily peak power (KW)	Meter yield (kWh)	Yield today (kWh)	CO_2 savings (kg)	Mt. opt. hrs	Opt. hrs. today	Opt. hrs. total	Energy meter (kWh)	Load (kWh)
1st	3.535	742.1	12.300	406	470:18	3:35	470:18	753.0	7.8
2nd	Sunday								
3rd	3.976	758.1	16.143	423	494:50	11:25	494:50	773.0	9.5
4th	3.856	781.2	23.100	436	506:15	11:30	506:15	795.9	10.4
5th	3.912	804.3	23.125	448	519.17	11:30	519:18	818.9	11.3
6th	1.251	825.8	21.500	460	531:34	11:30	531:34	840.4	12.2
7th	3.743	850.5	24.729	474	543:33	11:21	543:33	864.9	13.7
8th	3.624	871.9	21.400	482	554:54	03:40	554:54	885.9	13.9
9th	Sunday								
10th	4.313	914.7	19.407	510	580:43	11:23	580:43	928.8	14.2
11th	3.430	935.8	21.072	522	592:06	11:35	592:06	949.8	15.0
12th	3.624	955.3	19.500	533	605:39	11:50	605:39	969.2	15.5
13th	3.068	970.3	15.057	541	617:49	11:39	617:49	984.3	19.8
14th	3.511	992.5	22.146	553	630:18	11:44	630:18	1006.0	22.9
15th	1.367	994.2	6.700	557	642:02	03:35	642:02	1011.5	25.3
16th	Sunday								
17th	H0LI								
18th	2.127	1007.2	13.000	562	645:37	10:50	645:37	1021.3	28.5
19th	2.115	1024.3	17.100	571	656:27	11:10	656:27	1039.5	34.0
20th	1.238	1042.2	17.870	581	667:37	11:17	667.37	1060.2	40.3

(continued)

Table 1 (continued)

Date	Daily peak power (KW)	Meter yield (kWh)	Yield today (kWh)	CO_2 savings (kg)	Mt. opt. hrs	Opt. hrs. today	Opt. hrs. total	Energy meter (kWh)	Load (kWh)
21st	1.709	1062.3	20.100	592	678:54	11:07	678:54	1081.4	42.9
22nd	3.127	1088.4	26.13	606	690:01	03.37	690:01	1107.3	44.3
23rd	SUNDAY								
24th	2.923	1114.5	26.150	623	710:47	10:10	710:47	1138.7	46.3
25th	3.666	1140.7	26.200	636	720:57	11:12	720:57	1159.2	47.3
26th	2.051	1149.6	8.900	641	732:09	10:37	732:09	1168.0	48.5
27th	3.503	1171.6	21.500	653	742:02	10:16	742:02	1190.4	51.6
28th	3.692	1194.4	22.800	666	752:18	06:55	752:18	1213.7	52.8
29th	3.424	1200.8	6.400	670	759:13	03.25	759:13	1217.5	53.6
30th	Sunday								
31th	3.349	1210.8	10.000	675	762:38	11:30	762:38	1230	56.1

Table 2 Energy consumption for April 2014

Date	Daily peak power (KW)	Meter yield (kWh)	Yield today (kWh)	CO_2 savings (kg)	Mt. opt. hrs	Opt. hrs. today	Opt. hrs.total	Energymeter (kWh)	Load (kWh)
1st	3.813	1228.8	18	685	774:08	12:10	774:08	1247.9	58.3
2nd	3.212	1248.2	19.45	697	786:18	11:35	786:18	1267.7	60.1
3rd	3.425	1267.7	19.45	707	797:53	12:10	797:53	1287.5	61.5
4th	3.854	1287.8	20.1	719	810:03	11:43	810:03	1308.7	67.1
5th	3.102	1300.1	12.35	727	821:46	3:40	821:46	1315.4	68.7
6th	Sunday								
7th	3.219	1355.1	21.23	756	850:54	11:47	850:54	1374.4	70.2
8th	3.074	1374	18.9	766	862:01	11:48	862:01	1393.2	70.8
9th	3.104	1391.2	17.2	776	873:49	11:24	873:49	1410.4	73.5
10th	3.264	1413.1	21.9	788	885:13	11:35	885:13	1432.1	76.5
11th	1.578	1428.2	15.1	797	896:48	11:40	896:48	1447.9	78.1
12th	2.843	1438.7	10.5	805	908:28	3:40	908:28	1455.8	79.1
13th	SUNDAY								
14th	3.221	1494.2	28.7	833	930:15	12:15	930:15	1482.5	80.5
15th	BENGALI NEW YEAR								
16th	3.033	1543	19.5	861	954:35	12:30	954:35	1562.2	84.2
17th	3.756	1572.1	29.1	872	967:05	12:35	967:05	1579.5	85.3
18th	Good Friday								
19th	2.972	1593.7	18.4	888	1002:45	3:43	1002:45	1599.8	86.1
20th	Sunday								
21st	2.425	1612.1	19.65	899	1030:15	12:08	1030:15	1631.4	87.3

(continued)

Table 2 (continued)

Date	Daily peak power (KW)	Meter yield (kWh)	Yield today (kWh)	CO_2 savings (kg)	Mt. opt. hrs	Opt. hrs. today	Opt. hrs.total	Energymeter (kWh)	Load (kWh)
22nd	3.05	1630.8	18.7	910	1042:23	12:30	1042:23	1650.2	88.8
23rd	2.977	1650.2	19.4	921	1054:53	12:19	1054:53	1669.6	90.9
24th	3.002	1668.8	18.6	931	1067:12	12:07	1067:12	1688	93.5
25th	3.434	1691.6	22.8	943	1080:22	12:30	1080:22	1710.6	95.2
26th	3.221	1703.2	11.6	950	1092:52	3:25	1092:52	1723.8	96.1
27th	Sunday								
28th	2.707	1737.2	16.87	969	1121:13	12:17	1121:13	1756.3	97.5
29th	2.783	1749.7	17.86	976	1133:30	12:30	1133:30	1772.3	102.3
30th	2.753	1767.6	17.86	986	1146:12	12:24	1146:12	1787.7	108.3

Table 3 Energy consumption for May 2014

Date	Daily peak power (kW)	Meter yield (kWh)	Yield today (kWh)	CO_2 savings (kg)	Mt. opt. hrs	Opt. hrs. today	Opt. hrs. total	Energy meter (kWh)	Load (kWh)
1st	May Day								
2nd	2.864	1802.7	17.46	1006	1172:47	12:17	1172:47	1822.7	111
3rd	3.414	1811.9	9.2	1013	1185:04	3:35	1185:04	1835.5	112.6
4th	Sunday								
5th	3.588	1847.7	22.1	1031	1213:05	12:15	1213:05	1867.8	114
6th	3.743	1869.1	21.4	1043	1225:20	12:25	1225:20	1889.1	115.8
7th	4.14	1891	21.9	1055	1237:45	12:30	1237:45	1910.1	117.2
8th	2.156	1909	18	1066	1250:15	12:43	1250:15	1932.6	119.1
9th	2.075	1931.1	22.1	1078	1262:53	12:07	1262:53	1954.6	121
10th	2.707	1944.3	13.2	1086	1275:00	3:25	1275:00	1964.7	121.9
11th	Sunday								
12th	3.321	1989.5	22.33	1110	1307:25	12:20	1307:25	2013.8	123.5
13th	2.841	2011	21.4	1122	1319:45	12:45	1319:45	2034.7	124.1
14th	3.2	2032.5	21.5	1134	1332:30	12:38	1332:30	2056	125.8
15th	3.5	2055.1	22.6	1147	1345:08	12:20	1345:08	2078.5	127.5
16th	3.29	2077.6	22.5	1159	1357:28	12:30	1357:28	2100	129
17th	3.121	2087.7	10.7	1167	1369:58	3:34	1369:58	2112.4	130.1
18th	Sunday								
19th	3.068	2139.7	20.98	1194	1402:14	12:48	1402:14	2162.7	131.7
20th	3.108	2161	21.3	1206	1415:02	12:43	1415:02	2183.9	133.2
21st	3.371	2181.9	20.9	1218	1428:03	12:19	1428:03	2204.8	134.7

(continued)

Table 3 (continued)

Date	Daily peak power (kW)	Meter yield (kWh)	Yield today (kWh)	CO_2 savings (kg)	Mt. opt. hrs	Opt. hrs. today	Opt. hrs. total	Energy meter (kWh)	Load (kWh)
22nd	3.245	2202.2	22.3	1225	1440:22	12:30	1140:22	2224	136.8
23rd	3.238	2222.5	20.2	1240	1452:52	12:28	1452:52	2245.6	145.4
24th	3.332	2235.7	13.2	1250	1465:30	3:30	1465:30	2258.9	146.1
25th	Sunday								
26th	4.186	2262.2	10.21	1262	1497:21	12:08	1497:21	2285.3	148.2
27th	4.188	2267.2	5	1265	1509:29	12:46	1509:29	2290.4	149.8
28th	4.157	2285.2	18	1275	1522:15	12:28	1522:15	2308.6	151.9
29th	3.617	2304.7	19.5	1286	1534:43	12:23	1534:43	2328	154.1
30th	3.282	2325.2	20.5	1298	1547:06	12:14	1547:06	2348.5	157
31th	3.125	2333.6	8.4	1305	1559:20	3:30	1559:20	2356.7	158.1

Table 4 First year's (2014) revenues from energy saved at present cost

Month	Total reading of energy meter (kWh)	Per unit cost (Rs.)	Total cost (Rs.)
January	225.3	6	1351.8
February	(740.7 − 225.3) = 515.4	6	3092.4
March	(1230 − 740.7) = 489.3	6	2935.8
April	(1787.7 − 1230) = 557.7	6	3346.2
MAY	(2356.7 − 1787.7) = 569	6	3414
June	(2811.5 − 2356.7) = 454.8	6	2728.8
July	(3236.6 − 2811.5) = 425.1	6	2550.6
August	(3719.6 − 3236.6) = 483	6	2898
September	(4150.2 − 3719.6) = 430.6	6	2583.6
October	(4465.4 − 4150.2) = 315.2	6	1891.2
November	(4791.1 − 4465.4) = 325.7	6	1954.2
December	(5222.5–4791.1) = 431.4	6	2588.4
Total energy saving (2014)	5222.5	6	31,335

Therefore, annual savings from the power plant = 5222.5 * 6 = Rs. 31,335.
Therefore, simple payback time = (6,98,000/31,335) = 22.27 Years.

6 Calculation of Payback Period with Respect to Changing Value of Money Over Time

It is considered that per unit electricity bill is increasing at a rate of 6% and also the power generation of the solar panel is reducing at a rate of 1%. Practically, it may not happen as linearly as mentioned above. It is only our preassumption (Tables 5 and 6).

Consequently, it is calculated by 16 years (From 2014 to 2029) and it is found that the total amount of saving cost is Rs. 7,35,872. So after 16 years, the 5 kWp system will be fully offset. The warranty period of the photovoltaic module is 25 years and that is why the next 9 years (From 2029–2038) calculation is also conducted (Figs. 2 and 3).

Table 5 Year-wise cost-saving calculation for 25 years

Year	Per unit rate (Rs.)	Total energy consumption (kWh)	Total rate (Rs.)
2014	6	5222.5	31,335
2015	6.36	5170.2	32,883
2016	6.74	5118.5	34,499
2017	7.14	5067.3	36,180
2018	7.57	5016.6	37,976
2019	8.02	4966.4	39,831
2020	8.50	4916.7	41,792
2021	9.00	4867.5	43,807
2022	9.54	4818.8	45,971
2023	10.11	4770.6	48,231
2024	10.71	4722.9	50,582
2025	11.35	4675.6	53,069
2026	12.03	4628.8	55,685
2027	12.75	4582.5	58,427
2028	13.51	4536.6	61,290
2029	*14.32*	*4491.2*	*64,314*
2030	15.17	4446.3	67,450
2031	16.08	4401.8	70,781
2032	17.04	4357.8	74,256
2033	18.06	4314.2	77,914
2034	19.14	4271.0	81,748
2035	20.28	4228.2	85,750
2036	21.50	4185.9	89,997
2037	22.79	4144.0	94,442
2038	24.15	4102.5	99,076

7 Estimation of Carbon Footprint

A carbon footprint is the total sum of greenhouse gas (GHG) emissions caused by an organization, event, product, or a person. If we are aware, the increasing concentration of GHGs in the atmosphere can accelerate climate change and global warming, and it is very necessary to measure these emissions from our day to day activities. The first step toward managing GHG emissions is to measure them.

According to the Government of India, CO_2 Emission Factor (EF) for electricity is 0.82 kg CO_2 per kWh [9]. Now, for the year 2014, the kWh energy consumption from solar panel is 5222.5 kWh. Our day-to-day activities are moreover dependent on electricity which is mostly coming from coal-based power plants.

Table 6 Twenty-five years (2014–2038) revenues from energy saved at changing value of money over time

Year	Total cost (Rs.)	Total cost with previous year (Rs.)
1st year (2014)	31,335	31,335
2nd year	32,883	64,218
3rd year	34,499	98,717
4th year	36,180	1,34,897
5th year	37,976	1,72,873
6th year	39,831	2,12,704
7th year	41,792	2,54,496
8th year	43,807	2,98,303
9th year	45,971	3,44,274
10th year	48,231	3,92,505
11th year	50,582	4,43,087
12th year	53,069	4,96,156
13th year	55,685	5,51,841
14th year	58,427	6,10,268
15th year	61,290	6,71,558
16th Year (2029)	*64,314*	*7,35,872*
17th year	67,450	8,03,322
18th year	70,781	8,74,103
19th year	74,256	9,48,359
20th year	77,914	10,26,273
21th year	81,748	11,08,021
22th year	85,750	11,93,771
23th year	89,997	12,83,768
24th year	94,442	13,78,210
25th year (2038)	99,076	14,77,286

So without using solar energy, if we use electricity, then the amount of CO_2 emission is = Input value (in kWh/Year) × 0.82 (Emission factor) = 5222.5 kWh × 0.82 = 4282.45 kg. Divide final value with 1000, so that we get total carbon footprint in ton of CO_2. So the final carbon footprint in tons of CO_2 (tCO_2) is 4.28 tCO_2. Thus, if we use solar energy, then this much of CO_2 emission can be reduced.

8 Conclusion

The guaranteed period of solar photovoltaic system is almost 25 years. For new construction, it can be used to evaluate conventional construction to energy-efficient

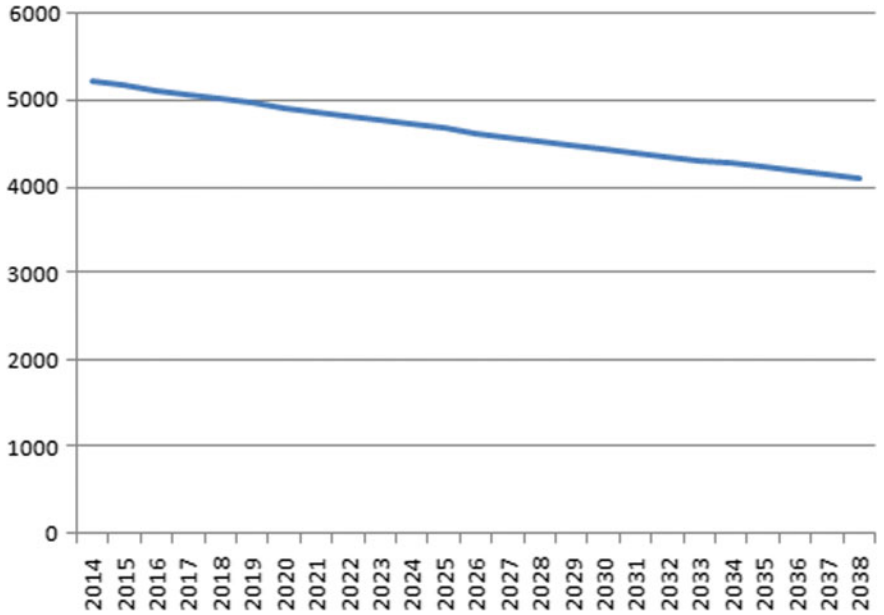
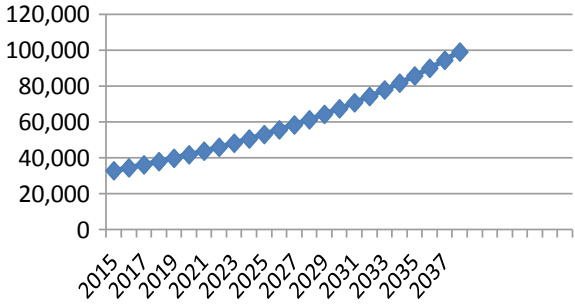


Fig. 2 Variation of power consumption with respect to year

Fig. 3 Variation of economical status with respect to year



design alternative. In simple payback analysis, it is assumed that the service life of the energy efficiency measure will equal or exceed the simple payback time. An investment with a longer payback period may be more profitable than an investment with a shorter payback period if it continuous to yield saving for a longer period. Over the last 20 years, the cost of solar system has come down seven-fold. As the demand for system rises and manufacturing volume increases, cost will decrease, and economic payback time will decrease.

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*hy*GWO-PS Tuned FOPID for AGC of Three Area Interconnected Hydro-Thermal Power System

Vikas Soni, Girish Parmar, and Afzal Sikander

Abstract In the present work, the application of a mixed/hybrid algorithm: grey wolf optimization-pattern search (*hy*GWO-PS) has been elaborated for automatic generation control (AGC) of three area interconnected hydro-thermal power system. The fractional-order proportional-integral-derivative (FOPID) controller has been incorporated in each area of the investigated power system and controllers' parameters have been tuned/optimized using the *hy*GWO-PS algorithm. For this purpose, a constrained control optimization problem has been defined with minimum and maximum ranges of controllers' parameters in which objective function: integral of time multiplied absolute error (ITAE) is minimized. The application of *hy*GWO-PS algorithm to tune the controllers' parameters for the same is abbreviated as *hy*GWO-PS/FOPID approach. The results carried out using the proposed approach for the investigated system have also been compared with some existing approaches and the results reveal that the proposed approach: *hy*GWO-PS/FOPID for the aforesaid power system produces the better performance in terms of ITAE, settling times/peak overshoots, number of oscillations and speed of frequency and tie line power deviations while comparing with some other approaches in the literature. The percentage reduction in ITAE, settling times, and overshoots with respect to other techniques have also been evaluated which shows the improvement in aforesaid parameters with respect to other existing techniques.

V. Soni (✉)
Department of Electronics and Communication Engineering, MIT, Kota, Rajasthan 324010, India
e-mail: vikassonieck@gmail.com

G. Parmar
Department of Electronics Engineering, UTD, Rajasthan Technical University, Kota, Rajasthan 324010, India
e-mail: girish_parmar2002@yahoo.com

A. Sikander
Department of Instrumentation and Control Engineering, Dr. B. R. Ambedkar National Institute of Technology, Jalandhar, Punjab 144011, India
e-mail: afzals@nitj.ac.in

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Keywords Load frequency control (LFC) · Interconnected hydro-thermal power system · Fractional-order PID controller (FOPID) · Grey wolf optimization (GWO) · Pattern search (PS) · Generation rate constraints (GRC)

1 Introduction

The interconnected power system is composed of two or more interconnected control areas or power plants for which AGC is an important control mechanism that maintains the tie line power and system frequency close to nominal values [1].

It has already been found in the literature that the better interconnected AGC/LFC can be achieved by attempting various control schemes like modern control theory (MCT) [2, 3], neural network (NN) [4], fuzzy system theory (FST) [5], reinforcement learning (RL) [6], and ANFIS approach [7] with complex structure of controllers. The various controllers' structures have been reported in the literature of AGC such as I-, PI-, ID-, PID- and IDD- and the comparison of them for AGC/LFC can be found in [8].

Nowadays, development of new evolutionary algorithm to tune the parameters of aforementioned frequency controllers has become an active area of research in order to improve AGC/LFC performance of interconnected power systems. The performances of BFOA tuned PI-controllers, classical and GA optimized controllers have been compared for two areas interconnected non-reheat thermal power system [9, 10]. A gain scheduled PI controller has been designed for interconnected thermal power system with some nonlinearity [11]. The numerous evolutionary techniques with controllers' structures for LFC/AGC can be found in the literature like ICA tuned PID-controllers for three area interconnected power system [12], tuned differential evolution (TDE) and teaching learning based optimization (TLBO) algorithms for P-, PI- and PID-controllers in LFC of a MSPS for thermal, hydro and gas power plants [13, 14], emotional learning approach for improving the LFC system with generation rate constraint (GRC) and neuro-fuzzy system [15], FA with an online wavelet filter for three unequal areas interconnected reheat thermal power AGC system [16], ABC algorithm for PI- and PID-controllers [17] and GSA for PI- and PIDF controller in AGC of interconnected power systems [18].

The performance of interconnected power systems is further required to be improved or enhanced in terms of time-domain specifications, like; overshoots, settling times, damping ratio, and steady-state error for which hybrid algorithms have come in the picture. **A** hybrid BFOA-PSO algorithm [19] has been proposed for various controllers in AGC systems, hybrid PSO-PS algorithm was designed for fuzzy PI-controllers [20] and *hy*GWO-PS algorithm has been given in order to tune the parameters of 2DOF-PID controllers for two area interconnected thermal power system and three area interconnected hydro-thermal power system [21–24].

It has already been found that the performance of the system depends on artificial techniques used, structure of the controller and selection of objective function. In this regard, the present attempt is towards the application of hybrid grey wolf

optimization-pattern search (*hy*GWO-PS) algorithm to optimize/tune the parameters of fractional-order proportional-integral-derivative (FOPID) controllers instead of P-, PI-, PID, IDD-, and 2DOF-PID- in AGC of three area interconnected hydro-thermal power system using ITAE as an objective function over well defined constrained control optimization problem. FOPID controller has been incorporated in each area of investigated power system. *hy*GWO-PS algorithm [27–30] is the hybridization of grey wolf optimization based on the hunting strategy of grey wolves [25] and a local search algorithm; pattern search (PS) [26].

2 Background Concepts

In this section, three area interconnected hydro-thermal power system and fractional-order PID (FOPID) controller have been discussed.

2.1 Three Area Interconnected Hydro-Thermal Power System

Three area interconnected hydro-thermal power system [7, 18–23] is shown in Fig. 1 in which two thermal and one hydro unit have been considered with nonlinearities

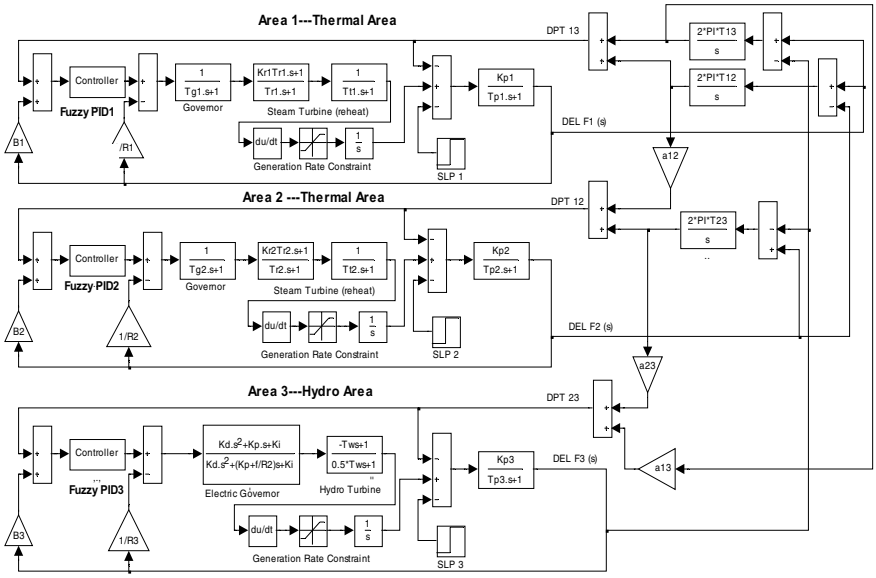


Fig. 1 AGC model of three area hydro-thermal power systems

and multiple tie-lines. The investigated power system consists of three dissimilar FOPID controllers.

2.2 *Fractional-Order Proportional-Integral-Derivative (FOPID) Controller*

The FOPID controller (Fig. 2) consisting of a differentiator and an integrator of fractional orders λ and μ exhibits a larger range of control action [27–30]. The following expression is given for FOPID [27–29].

$$u(t) = K_{\mathrm{p}}e(t) + K_{\mathrm{I}}D^{-\lambda}e(t) + K_{\mathrm{D}}D^{\mu}e(t) \tag{1}$$

where D denotes d/dt. The s-domain equation of FOPID controller is given as:

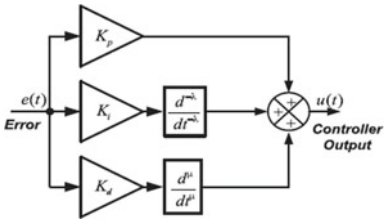
$$G_{\mathrm{fopid}}(s) = K_{\mathrm{Pf}} + \frac{K_{\mathrm{If}}}{s^{\lambda}} + K_{\mathrm{Pf}}s^{\mu} \tag{2}$$

where K_{Pf}, K_{If}, K_{Df}, λ and μ are controllers' parameters to be tuned optimally. In the present work, *hy*GWO-PS algorithm has been used for optimal tuning of FOPID controllers and the detailed descriptions including the mathematical modeling, pseudo codes, and flow charts of both the algorithms; grey wolf optimization and pattern search can be obtained in [21–23, 25, 26].

3 Objective Function and Constrained Control Optimization Problem

In the present work, objective function: ITAE has been considered as an objective function for proper tuning of controllers' parameters instead of ISE, IAE, ITSE, and ISTE. ITAE is given as:

Fig. 2 TF model of FOPID



$$J = \int_0^{t_{\text{simulation}}} (|\Delta w_1| + |\Delta w_2| + |\Delta w_3| + |\Delta P_{t13}| + |\Delta P_{t12}| + |\Delta P_{t23}|) \cdot t \cdot \mathrm{d}t \quad (3)$$

where ΔP_{t13}, ΔP_{t12} and ΔP_{t23} are tie line power deviations between respective areas.

$t_{\text{simulation}}$ = simulation time.

The optimization problem is given as:

Minimize J

Subject to

$$\begin{cases} K_{\text{Pmn}} \le K_{\text{P}} \le K_{\text{Pmx}} \\ K_{\text{Imn}} \le K_{\text{I}} \le K_{\text{Imx}} \\ K_{\text{Dmn}} \le K_{\text{D}} \le K_{\text{Dmx}} \\ \lambda_{\text{mn}} \le \lambda \le \lambda_{\text{mx}} \\ \mu_{\text{mn}} \le \mu \le \mu_{\text{mx}} \end{cases} \quad (4)$$

The [min, max] values of K_{P}, K_{I}, and K_{D} lie in the interval [−2, +2], the [min, max] values of λ and μ are in the interval [0, 1].

4 *hy*GWO-PS Algorithm for Three Area Interconnected Power System

Here, the *hy*GWO-PS algorithm (Fig. 3) is applied to the investigated system consisting of three numbers of FOPID controllers with dissimilar characteristics by considering ITAE as an objective function. A 0.1 p.u. step load perturbation in area-1 is applied at time $t = 0$ s. The same procedure of application of *hy*GWO-PS algorithm given in [21–23] has been used for proper tuning of FOPID controllers in AGC of investigated power systems. The parameters used for the implementation of PS algorithm are as follows:

Mesh size (MS) = 01; Mesh Expansion Factor (MEF) = 02; Mesh Contraction Factor (MCF) = 0.5; Maximum number of function estimation (MFE) = 10; Maximum number of iterations ($I_{\max}$) = 10.

5 Results and Discussions

In the present work, the same generation rate constraints (GRC) for two thermal units and one hydro unit are also considered [20]. The optimal parameters of controller obtained for each area using *hy*GWO-PS algorithm are mentioned in Table 1.

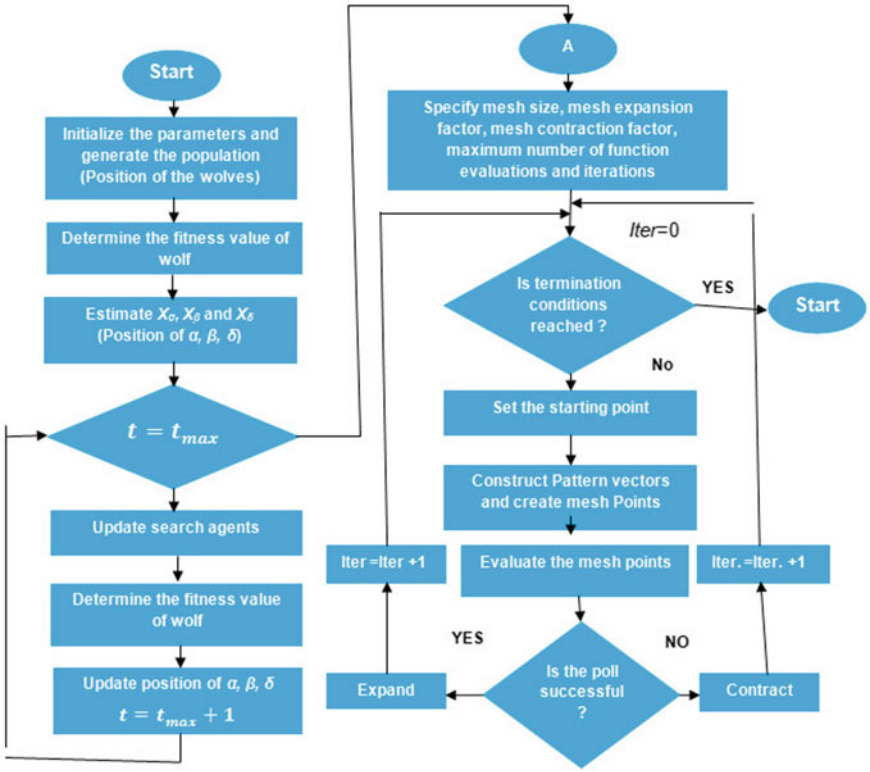


Fig. 3 Flow-chart of *hy*GWO-PS algorithm

Table 1 Optimal parameters of FOPID controllers obtained by *hy*GWO-PS algorithm for investigated system

Prescribed area	K_P	K_I	K_D	λ	μ
Area-1	1.7315	1.7135	0.2595	0.8200	0.0110
Area-2	1.8920	1.3062	0.4512	0.8456	0.9954
Area-3	0.0894	1.4313	0.0553	0.9121	0.1810

5.1 Frequency and Tie Line Power Deviations with and Without hyGWO-PS Approach

The *hy*GWO-PS has been applied to tune the FOPID controllers' parameters for the system under investigation. The controllers are of dissimilar characteristics and this approach is called *hy*GWO-PS/FOPID throughout the present work. The system dynamic responses with and without *hy*GWO-PS/FOPID have also been analyzed and shown in Figs. 4, 5, 6, 7, 8, and 9, and the comparison demonstrates that the

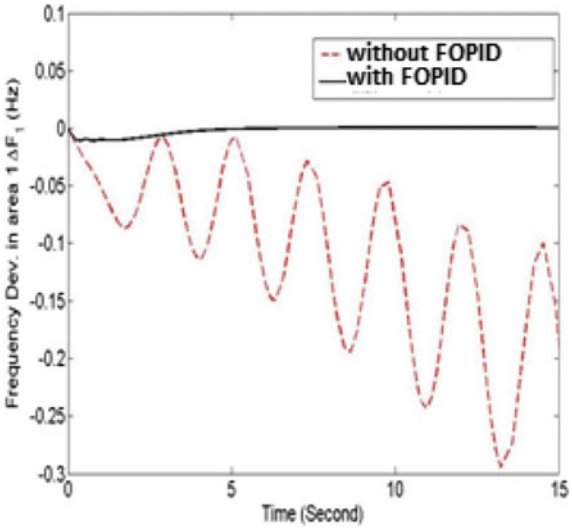


Fig. 4 Frequency deviation at area 1; ΔF_1, with and without FOPID

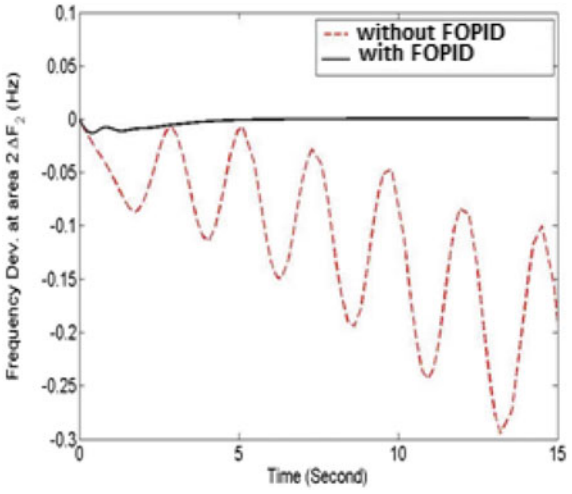


Fig. 5 Frequency deviation at area 2; ΔF_2, with and without FOPID controllers

dynamic responses of the system with *hy*GWO-PS/FOPID approach are less oscillatory, stable, exhibits less settling times and fast response while the dynamic responses without the proposed approach are highly oscillatory and unstable.

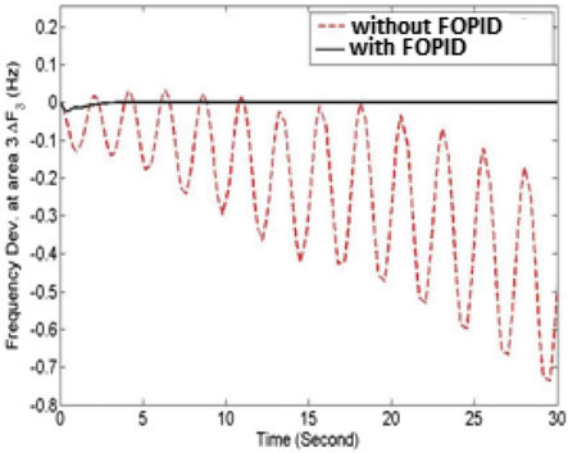


Fig. 6 Frequency deviation at area 3; ΔF_3, with and without FOPID controllers

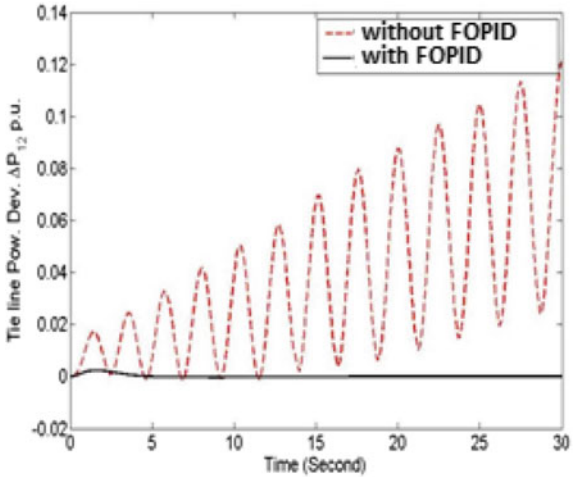


Fig. 7 Tie line power deviation at area 1; ΔP_{tie1}, with and without FOPID controllers

5.2 *Comparison of ITAE Value Obtained by hyGWO-PS/FOPID Approach*

A significant reduction in ITAE has been obtained using the proposed *hy*GWO-PS/FOPID approach (ITAE value = 1.1243). The comparison of ITAE obtained by the proposed approach with other existing approaches is mentioned in Table 2 which reveals that the proposed approach gives less ITAE value as compared to other existing approaches. The same comparison is also shown in Fig. 10.

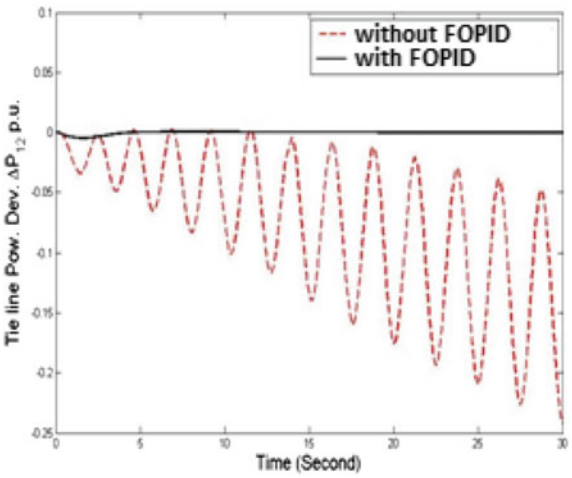


Fig. 8 Tie line power deviation at area 2; ΔP_{tie2}, with and without FOPID controllers

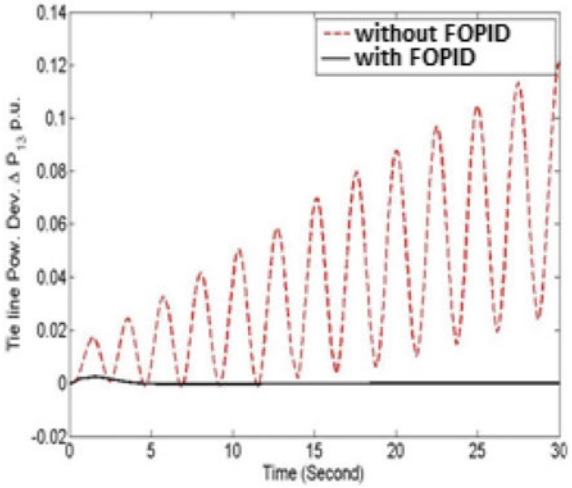


Fig. 9 Tie line power deviation at area 3; ΔP_{tie3}, with and without FOPID controllers

Table 2 Comparison of ITAE

Proposed approaches	ITAE value
*hy*GWO-PS/FOPID (proposed approach)	1.1243
*hy*GWO-PS/2DOFPID [21–23]	1.2595
GA/fuzzy PI [10]	2.4873
GSA/fuzzy PI [18]	1.7805
DE/fuzzy PI [13]	1.6857
FA/fuzzy PI [16]	1.5344
*h*PSO-PS/fuzzy PI [20]	1.3999

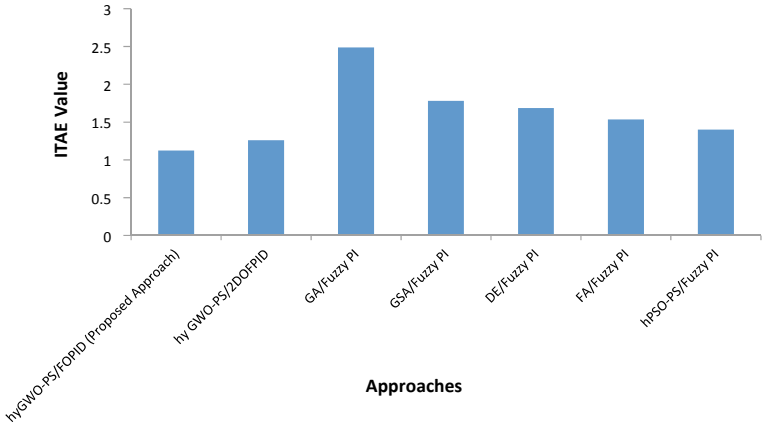


Fig. 10 Bar chart representation of ITAE comparison

5.3 Comparison of Dynamic Responses

Figures 11, 12, 13, 14, 15, and 16 show that the proposed *hy*GWO-PS/FOPID approach exhibits better dynamic response/behavior when compared with ANFIS [7], *h*BFOA-PSO [19] and *hy*GWO-PS [21–23] approaches in terms of less settling times/overshoots, oscillations and fast response. The settling times and peak overshoots of frequency and tie line power deviations in area 1, 2, and 3 are also compared with aforementioned approaches and have also been tabulated as given in Tables 3 and 4. It can be seen in Tables 3 and 4 that a satisfactory level of reduction in settling times and peak overshoots has been obtained using the proposed *hy*GWO-PS/FOPID approach as compared to ANFIS [7], *h*BFOA-PSO/PI [19] and *hy*GWO-PS/2DOFPID [21–23].

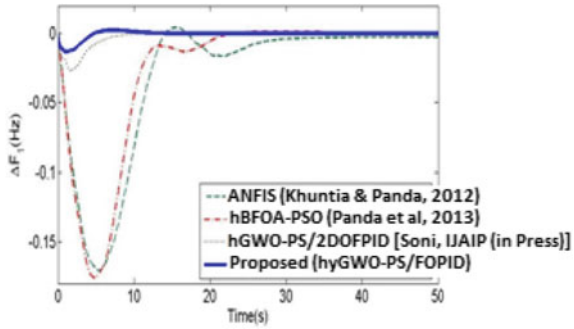


Fig. 11 Dynamic responses of frequency deviation at area 1; ΔF_1

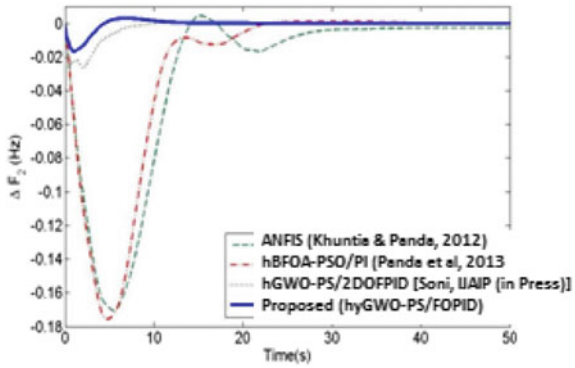


Fig. 12 Dynamic responses of frequency deviation at area 2; ΔF_2

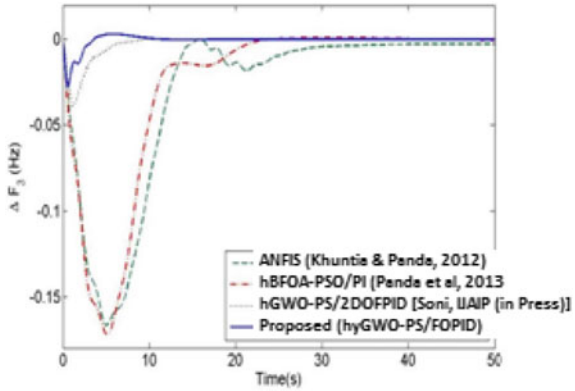


Fig. 13 Dynamic responses of frequency deviation at area 3; ΔF_3

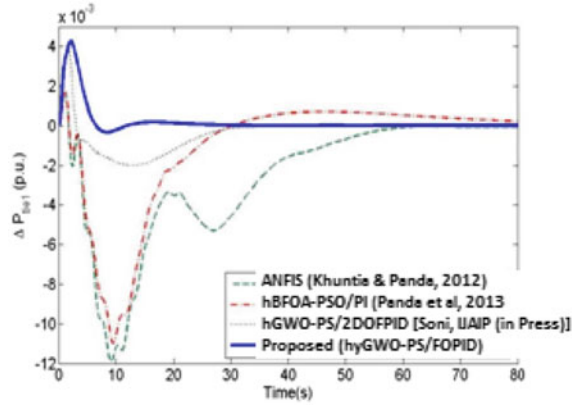


Fig. 14 Dynamic responses of tie line power deviation at area 1; ΔP_{tie1}

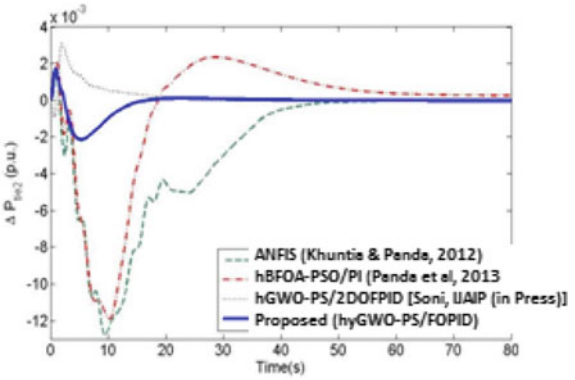


Fig. 15 Dynamic responses of tie line power deviation at area 2; ΔP_{tie2}

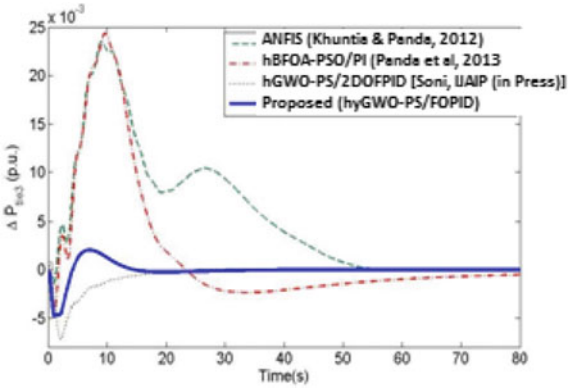


Fig. 16 Dynamic responses of tie line power deviation at area 3; ΔP_{tie3}

Table 3 Comparison of settling times

Approach	Settling times (2% tolerance band)			Settling times (2% tolerance band)		
	ΔF_1	ΔF_2	ΔF_3	ΔP_{tie1}	ΔP_{tie2}	ΔP_{tie3}
ANFIS [7]	32.2	30	30.89	61.53	47.87	55.1
*h*BFOA-PSO/PI [19]	21.44	21.99	22.61	38.22	69.99	59.45
*hy*GWO-PS/2DOFPID [21–23]	8.80	8.80	8.30	19.97	15.53	13.3
*hy*GWO-PS/FOPID (proposed)	8.50	8.50	8.10	19.31	15.23	13.01

Table 4 Comparison of peak overshoots

Approach	Peak overshoots			Peak overshoots		
	ΔF_1	ΔF_2	ΔF_3	ΔP_{tie1}	ΔP_{tie2}	ΔP_{tie3}
ANFIS [7]	0.1700	0.170	0.166	0.0119	0.0127	0.0230
*h*BFOA-SO/PI [19]	0.1753	0.175	0.172	0.0108	0.0119	0.0243
*hy*GWO-PS/2DOFPID [21–23]	0.0120	0.016	0.027	0.0040	0.0010	0.0040
*hy*GWO-PS/FOPID (proposed)	0.0020	0.006	0.017	0.0040	0.0010	0.0040

Table 5 Percentage reduction in settling times obtained by proposed approach with respect to other existing approaches

Approach	Settling times (2% tolerance band)			Settling times (2% tolerance band)		
	ΔF_1	ΔF_2	ΔF_3	ΔP_{tie1}	ΔP_{tie2}	ΔP_{tie3}
ANFIS [7]	73.6	71.6	73.77	68.6	68.18	776.38
*h*BFOA-PSO/PI [19]	60.35	61.34	64.17	49.47	78.23	78.11
*hy*GWO-PS/2DOFPID [21–23]	3.40	3.40	2.40	3.30	1.93	2.18

Table 6 Percentage reduction in overshoots obtained by proposed approach with respect to other existing approaches

Approach	Peak overshoot			Peak overshoot		
	ΔF_1	ΔF_2	ΔF_3	ΔP_{tie1}	ΔP_{tie2}	ΔP_{tie3}
ANFIS [7]	98.82	96.47	89.75	66.30	92.12	82.60
*h*BFOA-PSO/PI [19]	98.85	96.57	90.12	57.14	91.59	83.53
*hy*GWO-PS/2DOFPID [21–23]	83.33	62.5	37.03	0	0	0

5.4 Percentage Reduction in Settling Times and Overshoots Obtained by Proposed Approach with Respect to Some Existing Approaches

Tables 5 and 6 show that how much the proposed approach *hy*GWO-PS/FOPID for AGC of the investigated system is better than some other existing approaches. The results show that the proposed approach gives a better reduction in settling times and peak overshoots, i.e., better improvement. In the present work, 0.01 p.u. step load perturbation in all areas at $t = 0$ s has been considered.

6 Conclusions

In the present work, the *hy*GWO-PS algorithm has been employed for optimal tuning of FOPID controllers' parameters used in AGC of the discussed system by considering ITAE as an objective function. The simulation results obtained with the proposed approach: hyGWO-PS/FOPID have also been compared with some existing approaches available in the literature for the same power system and same ITAE and comparative study reveals that the proposed approach is better than some discussed popular approaches in terms of ITAE, settling times and overshoots, speed of response and number of oscillations. The percentage reduction in settling times and overshoots obtained by the proposed approach with respect to some other approaches have also been computed.

Acknowledgements All authors are very much thankful to TEQIP-III RTU ATU for a collaborative research scheme (CRS) under which the research project entitled "*Design of fractional order PID controller for AGC of interconnected power systems*" **has been assigned to** us. In this Chapter, a work entitled "*hyGWO-PS tuned FOPID for AGC of* ***three area interconnected hydro-thermal power system***" has been presented.

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Outlier Detection for Data Using Density-Based Technique

KiritiMotkuri, N. Jayanthi, Mahadev Hasnabade, Sreenath Reddy, Y. Deepthi, and N. V. Krishna Rao

Abstract Handling anomalies in high-dimensional information viably and effectively is as yet a difficult issue in AI. Distinguishing anomalies has an expansive scope of true applications. High-dimensional information may trigger the separation fixation issue, though the exception discovery requires fitting qualities for parameters, making models high unpredictable and progressively touchy. To defeat these issues right now idea called nearby projection score (LPS) is acquainted with speak to deviation level of perception to its neighbors.

Keywords Outlier ranking · Nearest neighbors · Determining · Low-rank

1 Introduction

With the headway of developing advances, an expanding measure of information is getting accessible in true applications. Inside the monstrous information, some of them instigate strange practices or examples raised from an assortment of angles including malfunctioned equipment or malevolent exercises. Such extraordinary practices or conflicting examples, otherwise called exceptions, irregularities, variations from the norm, curiosities, or degenerates, don't agree to a very much characterized thought of ordinary conduct of the information. Truly, they frequently display as the portrayals of commotions or intriguing realities, for example, digital interruption and psychological militant exercises, as indicated by various purposes.

Recognizing anomalies out from information is of extraordinary enthusiasm to the networks of AI and information mining, since it can uncover irregular practices, fascinating examples, and remarkable occasions from the information. To be sure, recognizing or disposing of anomalies turns into a fundamental preprocessing stage in

KiritiMotkuri · N. Jayanthi (✉) · M. Hasnabade · S. Reddy · Y. Deepthi · N. V. Krishna Rao
Department of Computer Science and Engineering, Institute of Aeronautical Engineering, Dundigal, Hyderabad, Telangana, India
e-mail: jneelampalli.office@gmail.com

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information examination. For instance, clamor evacuation can improve model execution, because of the way that commotions may upset the revelation of significant data,[1] while irregular access discovery by inspecting access records in a firewall at a time can assist us with isolating interruption from organize get to. Exception discovery (otherwise called peculiarity location) is a procedure of uncovering sudden perceptions that goes amiss such a great amount from the remainder of the perceptions. Since exception identification can carry noteworthy advantages to choice examination, it has increased significant interests in an assortment of fields and applied in an enormous number of spaces, for example, wrongdoing and psychological militant location, deficiency troubleshooting, and determination, organize interruption, misrepresentation revelation, restorative and wellbeing checking, signal investigation, picture handling, irregular climate discovery, strange group conduct estimation, video reconnaissance, and numerous different zones. The wide assorted variety in genuine applications mirrors a reality that exception discovery is a generally explored subject.

where the previous offers a positioning rundown of the perceptions, everyone with a score, in view of given measurements. The perceptions with high scores rank on the highest priority on the rundown if a bigger worth represents a more noteworthy variation or odd degree. The last decides exceptions as indicated by the positioning rundown. From this viewpoint, anomaly positioning assumes a center job in recognition. Of these, anomaly positioning and exception recognition are two terms utilized most ordinarily in the writing; once in a while conversely.

The anomaly location calculations can be generally classified into the accompanying gatherings, for example, measurements-based, separation-based, thickness-based, and bunching-based techniques. Among these discovery techniques, the separation-based and thickness-based recognition ones have gotten uncommon fascination and broadly contemplated, because of the way that their thoughts are natural and can be effectively actualized. The rank-based identification calculation (RBDA) and the neighborhood anomaly factor (LOF) are regular instances of these two sorts, separately.

There are two primary provokes should have been additionally explored for anomaly location. The first is the high dimensionality of information. The high dimensionality may raise the following two inescapable issues:

1. the so-called curse of dimensionality and
2. the distance concentration.

[1] A huge assemblage of exception discovery strategies have been created. In fact, the methodology of distinguishing exceptions comprises of two principle stages:

1. Outlier positioning
2. Determining

2 Literature Survey

Anomaly detection

Authors: J. Liu and H. Deng, "Outlier detection on uncertain data based on local information," Know. Based Syst., vol. 51, pp. 60–71, Oct. 2013.

Information processing is having the greater significance for business organizations to take management and financial decisions. The complete KDD process can be applied over the raw input dataset to identify the analytical observations.

Various feature selection methods, clustering, and classification algorithms are proposed by the researchers to improve the accuracy. In this paper, a descriptive study of advanced work carried out in various associated work stages of KDD process. The paper has recognized the contribution of researchers with effective observation on methodology, scope, and significance of their contribution [1]. The paper has explored the various functional stages of data processing including data cleaning, feature generation, clustering, classification, and outlier detection. Each stage is here described with a descriptive approach, significance, application domain, and the relative scope.

Authors: V. Riffo and D. Mery

Stuff assessment utilizing X-beam screening is a need task that decreases the danger of wrongdoing and fear-based oppressor assaults. Manual discovery of risk things is dull in light of the fact that not very many packs really contain dangerous things and the procedure requires a high level of fixation. A computerized arrangement would be an invite improvement right now. We propose a technique for programmed recognition of risk objects utilizing single X-beam pictures. [2]Our methodology is an adjustment of a system initially made for perceiving objects in photos dependent on certain shape models. Our location strategy utilizes a visual jargon and an event structure created from a preparation dataset that contains agent X-beam pictures of the risk article to be distinguished. Our strategy can be applied to single perspectives on grayscale X-beam pictures got utilizing a solitary vitality procurement framework. We tried the adequacy of our technique for the recognition of three diverse risk objects: (1) extremely sharp edges; (2) shuriken (ninja stars); and (3) handguns. The testing dataset for every risk object comprised of 200 X-beam pictures of sacks. The genuine positive and bogus positive rates (TPR and FPR) are: (0.99 and 0.02) for disposable cutters, (0.97 and 0.06) for shuriken, and (0.89 and 0.18) for handguns. In the event that other delegates preparing datasets were used, we accept that our system could help in the recognition of different sorts of risk objects.

3. Outlier detection for temporal data

Authors: M. Gupta, J. Gao, C. C. Aggarwal, and J. Han

[2]Our strategy begins to recognize k closest neighbors (kNNs) for every perception. The local data is then anticipated into a low-dimensional space through the system of low-position lattice guess.

In the insights network, exception location for time arrangement information has been read for quite a long time. As of late, with progresses in equipment and programming innovation, there has been a huge assortment of work on worldly exception locations from a computational point of view inside the software engineering network. Specifically, progresses in equipment innovation have empowered the accessibility of different types of fleeting information assortment components, and advances in programming innovation have empowered an assortment of information the executive's instruments. This has filled the development of various types of informational indexes, for example, information streams, spatiotemporal information, appropriated streams, transient systems, and time arrangement information, produced by a large number of utilizations [2]. There emerges a requirement for a composed and itemized investigation of the work done in the territory of anomaly recognition regarding such fleeting datasets. Right now, give an exhaustive and organized diagram of a huge arrangement of intriguing exception definitions for different types of worldly information, novel strategies, and application situations in which explicit definitions and systems have been generally used. Best rehearses in big business approval: The RBAC/ABAC crossbreed approach.

LOF: Identifying density-based local outliers [3]

Authors: M. M. Breunig, H.-P. Kriegel, R. T. Ng, and J. Sander

For some KDD applications, for example, distinguishing crimes in E-business, finding the uncommon occasions or the exceptions, can be more intriguing than finding the regular examples. Existing work in exception recognition views being an anomaly as a paired property. Right now, fight that for some situations, it is progressively significant to dole out to each question a level of being an exception. This degree is known as the nearby anomaly factor (LOF) of an item. It is nearby in that the degree relies upon how segregated the item is concerning the encompassing neighborhood. We give a point by point formal investigation indicating that LOF appreciates numerous attractive properties. Utilizing genuine world datasets, we show that LOF can be utilized to see exceptions that show up as significant, yet can in any case not be related to existing methodologies. At long last, a cautious exhibition assessment of our calculation affirms we show that our methodology of discovering nearby exceptions can be functional.

4. Adaptive Intrusion Detection of Malicious Unmanned Air Vehicles Using Behavior Rule Specifications

Authors: R. Mitchell and L-R. Chen

Right now, propose a versatile particular-based interruption recognition framework (IDS) for distinguishing pernicious unmanned air vehicles (UAVs) in an airborne framework where congruity of activity is absolutely critical. An IDS reviews UAVs in a disseminated framework to decide whether the UAVs are working regularly or are working under malignant assaults. We examine the effect of foolish, irregular, and sharp assailant practices (modes which numerous verifiable digital assaults have utilized) on the adequacy of our conduct rule-based UAV IDS (BRUIDS) which puts together its review with respect to conduct rules to rapidly survey the survivability of the UAV confronting pernicious assaults. Through a relative investigation with the

multiagent framework/subterranean insect province grouping model, we show a high location exactness of BRUIDS for agreeable execution. By changing the discovery quality, BRUIDS can viably exchange higher bogus positives for lower bogus negatives to adapt to increasingly advanced arbitrary and crafty assailants to help ultra protected and secure UAV applications.

3 Implementation Methodology

This strategy begins to recognize k closest neighbors (kNNs) for every perception.

The local data is then anticipated into a low-dimensional space through the system of low-position framework guess to assess Local Projection Score (LPS) of the perception.

Thus, all the perceptions are positioned in a plunging request as indicated by their scores.

At long last, the perceptions with high scores are selected and taken as exceptions.

4 Performance Analysis and Results

Right now can distinguish the event of exceptions.

This is finished by utilizing Local Projection.

The perceptions with high scores are selected and taken as exceptions.

Low-Rank Approximation

Step by step instructions to manage high-dimensional information is a despite everything testing issue in the network of AI. A much of the time utilized arrangement truly is to perform measurement decrease, which extends a high-dimensional space into a low-dimensional one by mapping systems. There are a few traditional measurement decrease strategies accessible, for example, standard segment examination, outrageous learning machine, and direct discriminant investigation. A famous decrease strategy is low-position network estimation, which looks for a diminished position lattice to around speak to the first one. Lattice rank is a central and significant idea in direct variable-based math. It alludes to the quantity of driving sections that relate to straightly autonomous lines or segments of the network. Then again, the rank is the quantity of nonzero particular estimations of the grid. Assume that the high-dimensional information is orchestrated as the segments of an enormous framework $D \in Rn \times m$, where n and m mean the quantities of perceptions and highlights (factors), individually. Thinking about the strategy of solitary worth disintegration (SVD), D can be deteriorated as follows:

$$D = \text{USVT} \tag{1}$$

where $U \in Rn \times r$ and $V \in Rm \times$ rare left and right solitary vectors, separately. $S \in Rr \times r$ is the corner to corner network comprising of solitary estimations of D, i.e., $S = \text{diag}\ \{\sigma_1, \sigma_2, \ldots, \sigma_r, 0, 0, \ldots, 0\}$, where the particular qualities are arranged in diminishing request, $\sigma_1 \geq \ldots \geq \sigma_r > 0$. In this way, the position of D is r, i.e., rank $(D) = r$ and $r \leq \min\{n, m\}$ [4].

The rank is a successful apparatus to gauge the sparsity of grid. The lower the position, the more scanty the framework. In certifiable applications, information are regularly produced from low-dimensional spaces. Hence, the positions of the relating information lattices are low. Be that as it may, clamors raised from an assortment of angles lead to the information grids with high position. Subsequently, it is important to expel clamors from the high-dimensional information grids and recoup the frameworks with low position for information investigation.

Low-position estimate is an adaptable method to speak to and recuperate information inside low-dimensional subspaces from high-dimensional ones. It intends to limit the framework error between a high-dimensional information lattice D and its decreased network $D\approx$, i.e., looking for a low-position grid D^- for D [4]. Officially, the numerical model of low-position estimation is to discover the framework D^- inside a low-dimensional subspace, with the end goal that the accompanying imperative is limited:

$$\min_{\overline{D}} ||D - D||_F \tag{2}$$

$$\text{S.t. rank}(\overline{D}) \leq t \tag{3}$$

where $\|X\|_F = \sqrt{\sum_i \sum_j x_{ij}^2}$ is the Frobenius norm of X. For the optimization problem above, It is general combinatorial and know to be NP-hard.

In this manner, making the minimization issue identifiable by loosening up the requirement is by all accounts an achievable arrangement. A well-known technique is to change (2) into the accompanying raised improvement problem. There are a few successful answers for the enhancement issue of (3), for example, iterative thresholding, quickened proximal angle, enlarged Lagrange multipliers, and rotating heading strategies. To all the more likely comprehend the thought, here we resort to the procedure of solitary worth thresholding (SVT) to take care of the atomic standard minimization issue helpfully. It is perceptible that (3) has the same solution to the following optimization problem:

$$\min_{\overline{D}} \frac{1}{2}(D - \overline{D}(2_F + \lambda||\overline{D}\|_* \tag{4}$$

Local Projection Score

As examined over, a central supposition basic the separation-based and the thickness-based anomaly recognition strategies is that they misuse neighborhood data of a perception to decide if the perception is an exception or not [4]. The sparser

the area of the perception, the higher likelihood of being anomaly the perception. This notwithstanding is steady with the improvement issue of the atomic standard referenced previously. Truth be told, the atomic standard $D^* = r\, i = 1\, \sigma_i$ can successfully gauge the disparity (or data measure) of D, since every solitary worth σ_i alludes to a size of D on the ith rule segment, yielding the projections of D onto the subspace spread over by the r particular vectors of D.

Normally, we abuse the atomic standard as our odd score to gauge the uniqueness level of neighborhood. Given a perception x, its local data $N(x)$ ordinarily contain closest neighbors of x. $N(x)$ can be gotten by the off-the-rack learning calculations like kNN, i.e., $N(x) = \{x_1, x_2, \ldots, x_k\}$, where x_i is the ith closest neighbor of x. For instance, the closest neighbors of A_n and B in Fig. 1 are those focuses set apart with strong circles and ran circles, separately, if $k = 3$ is considered in kNN. It ought to be called attention to that for the typical focuses, their neighbors are near one another firmly, though the exceptions are a long way from their neighbors.

To depict such attributes of information dispersions, we receive the atomic standard of neighborhood as our abnormal degree called LPS.

$$\text{lps}(x) = N(X)||_*. \tag{5}$$

Local Reachability Density

Local reachability density is used in the place of lps. In this method, it calculate the reachability density by the below formula. LRD is calculated for all the points and they are sorted and ranked. By this method, we can detect the outliers.

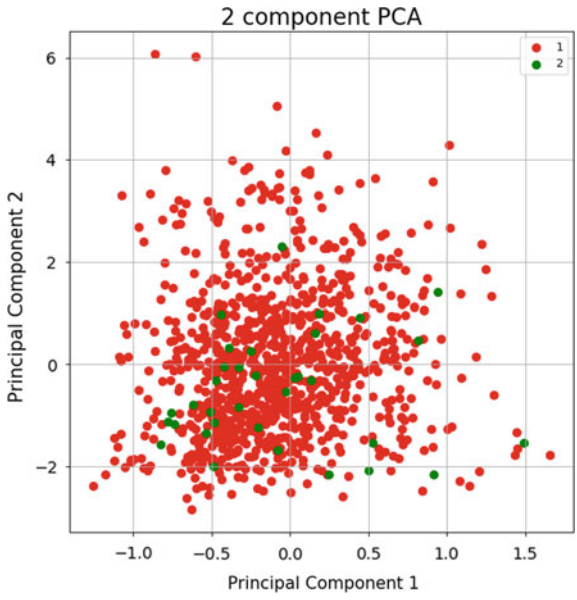

Fig. 1 Outliers are obtained when the k value is 32. Red dots represent the data and the green represents outliers. This output is obtained by ranking based on lrd

$$Ir\, d_k(0) = \frac{\|N_k(0)\|}{\sum_{0'' \in N_k(0)} \text{reachdist}_k(0' \leftarrow 0)} \tag{6}$$

$\text{reachdist}\, t_k\big(o \leftarrow o'\big) = \max\big\{\text{dist}_k(o), \text{dist}\big(o, o'\big)\big\}$
$\|N_k(o)\|$ means the number of objects in $N_k(o)$.

Objectives
Right now can identify the event of exceptions.

This is finished by utilizing Local Projection.

Our strategy begins to recognize k closest neighbors (kNNs) for every perception. The local data is then anticipated into a low-dimensional space through the method of low-position grid guess.

The perceptions with high scores are selected and taken as exceptions.

Info information portrayal:

As we are managing information it itself goes about as information.

The information can be of different structures.

Right now are thinking about arbitrary produced information and information put away in records.

Information is solicited during execution from code.

Anticipated results
The yield is as chart.

Right now is circulated dependent on its lps score.

Exceptions are demonstrated with a hover around the information.

Underneath figure portray the yield group.

5 Conclusion

Right now exhibited a half and half pointer generator design with inclusion, and indicated that it lessens mistakes and reiteration. We applied our model to another and testing long content dataset, and significantly beat the abstractive best in class result. Our model displays numerous abstractive capacities, yet achieving more significant levels of deliberation stays an open research question

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