

A Unique Multiple DGs Allocation Technique for Loss Minimization in Distribution System



Ankush Tandon and Sarfaraz Nawaz

Abstract Nowadays, distributed generation units are used in distribution systems for active power loss minimization. It is pre-requisite to compute the appropriate size and location of DGs (solar PV module) and capacitors to achieve maximum loss reduction. The prominent aim of this paper is to maximize percentage loss reduction of distribution systems. An innovative mathematical term, Loss Constant (LC), is anticipated in this paper. The LC determines rating and position of multiple DG and Capacitors units separately. The above method is experienced on IEEE 69 bus standard distribution system. The efficacy of above methodology is proved by considering three different load levels for aforesaid test system. Results are found encouraging and optimistic for both test systems.

Keywords Real power loss (RPL) · Loss constant (LC) · Distributed generation (DG) · Distribution systems (DS)

1 Introduction

In India, the RPL of distribution network are on higher side (around 25%). In distribution systems, DG is incorporated for active power loss reduction. In DG technology, both conservative and non-conservative energy sources are adopted. In conventional sources gas turbine, fuel cells, reciprocating engines, micro-turbine are utilized while biomass, cogeneration, wind power plant, solar PV array falls in the category of non-conventional sources. Placing of DG units is the predicament of determining suitable location and its rating, while satisfying the cost constraints. Optimal sizing of isolated hydropower plant is calculated by tabu search in [13]. The DG allocation problem is resolved by analytical method in RDS [3, 9]. Genetic algorithm technique has been utilized in [16, 17] to evaluate optimal location and rating of DG units. In [14], conventional linear programming (LP) method is adopted to solve DG place-

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ment problem. Classical Kalman filter approach is adopted in [18]. Tabu Search (TS) methodology is adopted for RPL in [20]. In [4] genetic algorithm is utilized to solve the allocation problem. ABC algorithm [2] has been applied to determine the best location and size of multiple DGs. Zhang et.al [28] adopted integrated energy model for allocating DG units in. In [11], Injeti and Kumar applied new method to diminish the RPL in distribution system. Evolutionary technique such as simulated annealing are used to decide both position and rating of DG units. In [21], sensitivity analysis technique is presented to resolve OPDG problem. In [27], an analytical approach is projected to resolve OPDG problem in balanced DS.

Reactive power compensation is habitually done by shunt capacitors. It is desirable to allocate capacitors at optimal location with appropriate size for reduction of RPL and for enhancement of voltages. The rating and position of capacitors are calculated by particle swarm optimization in [23], simulated annealing [5], cuckoo search algorithm [6], optimization technique based on teaching learning algorithm [25], based on flower pollination [1], heuristic algorithm [10], genetic algorithm [26] are applied in literature to solve capacitor placement problem.

A new approach has been presented here for finding optimal position and rating of DG and capacitor units. A simple and new mathematical expression, line constant (LC), is formulated to resolve DG and capacitor units allocation problem. Rating and location of both units are identified by line constant separately. The method is tested on conventional IEEE 69 bus system. The results for same systems are found promising and optimistic. The same results have outperformed other latest techniques proposed in the literature.

2 Problem Statement

The aim of this work is to scale down real power losses which occurred in distribution system. For minimizing power losses, it is essential to install the DG and capacitor units of suitable rating at best possible places. A simple line diagram of bus a and b is shown in Fig. 1. Capacitor units or DG are placed at bus b. The RPL for n-bus system is calculated by using:

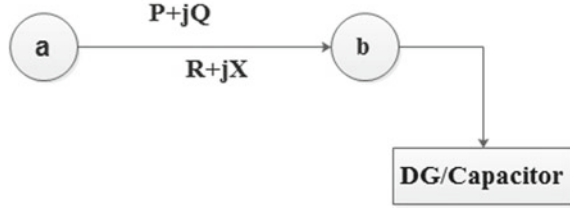
$$RPL_n = \sum_{a=1}^n \sum_{b=1}^n \frac{|V_a|^2 + |V_b|^2 - 2|V_a||V_b|\cos\theta_{ab}}{Z^2} R \quad (1)$$

It is mandatory for optimal placement of DG or capacitor units that the ratio of real power losses (after and before shunt compensation) is to be minimum.

Hence, the objective function of the problem is :

$$Min.(f) = RPL_n \quad (2)$$

Fig. 1 Line diagram of bus a and b



The operational constraints are as follows:

1. Power balance rule should not be violated.
2. The total generated power of DG and capacitor units should be less than the load of the system.
3. Voltage profile of each bus should maintain Indian standards ($\pm 5\%$).
4. The line current should remain between its minimum and maximum values.

3 Proposed Approach

In this paper, a latest method is adopted to minimize RPL in DS. The RPL are reduced by inserting DG or capacitor units at appropriate positions. The ratio of P_2 and P_1 is termed as “Loss Constant (LC)” and is expressed as:

$$LC = \frac{P_2}{P_1} \tag{3}$$

where,

P_1 : RPL for base case before compensation. P_2 : RPL after shunt compensation.

The value of P_2 is required to be minimum in order to identify the position as well as rating of DG or capacitor. Loss Constant (LC) value is determined at each bus with explicit DG size for calculating the location and range of DGs. Candidate bus position of DG is identified by determining LC values, and the bus which have minimum LC value will be the candidate bus for appointment of DG unit.

The steps involved in computational procedure are mentioned below:

1. Calculate real power losses for base case (P_1).
2. Initiate with 1% DG or capacitor value of total load of the system (PD and QD).
3. Compute P_2 and “LC” of the system bus using equation no 3.
4. Increase DG/ capacitor size in minute step and calculate P_2 and “LC.”
5. Minimum amount of “LC” value yields optimal DG/ capacitor size.
6. Stop the program when there is change in bus number.
7. The meticulous bus will be the optimal location.
8. To determine more sites of DG or capacitor units repeat Steps 4–7.

4 Results

Standard IEEE 69 bus system [23] is used to examine the above approach. The projected technique is tested by considering three different loading levels also. The code for the proposed methodology is written in MATLAB software.

4.1 Test System I (Standard IEEE 69 Bus System)

Figure 2 exhibits line diagram of test system-I. Total real and reactive load of the system is 3802 kW and 2694 kVAr [23], respectively. The different cases are as follows:

- I: Placement of DG only
- II: Placement of Capacitor only
- III: Placement of DGs & capacitors concurrently.

All the three different cases mentioned above are tested on three different loading conditions which are as follows: Light load (50%), nominal load (100%) and heavy load (160%) (Figs. 3 and 4).

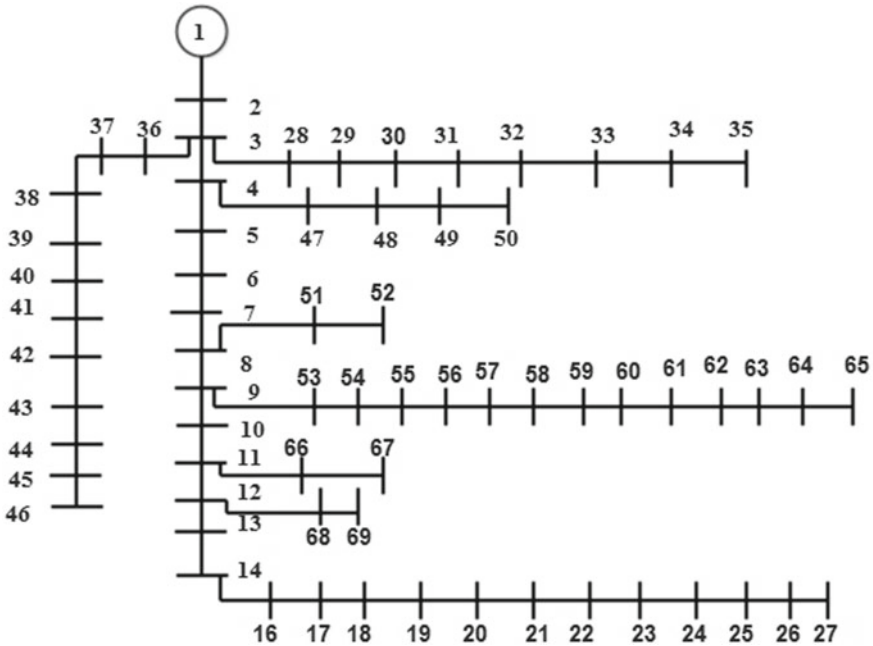


Fig. 2 IEEE-69 bus distribution system

Fig. 3 Voltage outline of 69 bus system (Nominal loading level for CASE-III)

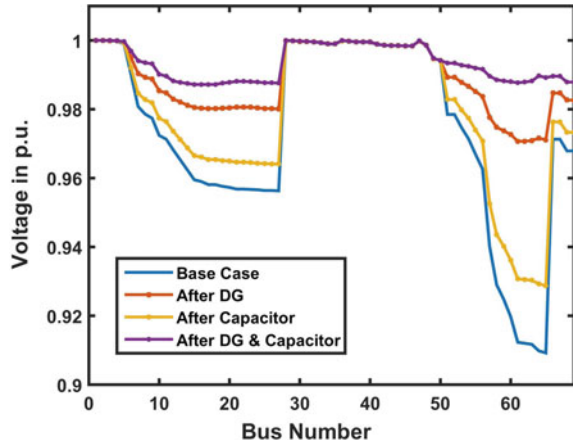
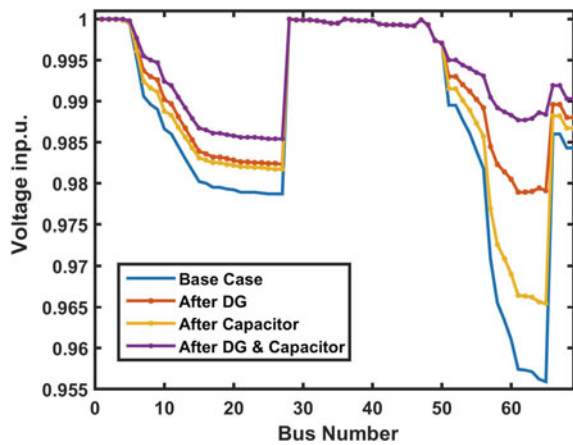


Fig. 4 Voltage outline of 69 bus system (light loading level for CASE-III)



1. Case-I: DGs (Solar PV Module) placement only:

By using proposed method, the size and position of DG units are identified. The candidate buses are selected while taking into account a ceiling of 50% DG penetration level. Table 1 exhibits the results of standard 69 bus system. The most favorable place for DG is determined at bus no. 21, 61 and 64. The real power losses after DG allotment are 77 kW (nominal load), 25 kW (light load) and 210 kW (heavy load). Table 2 justifies that percentage RPL reduction is remarkable of the projected technique as compared to other techniques proposed in the literature. The minimum voltage profile after applying proposed technique is 0.9708 pu which is appreciably better as the DG size is 1.80 MW. The basis of comparison is total size of DG in MW, minimum bus voltage in per unit and percentage loss reduction.

Table 1 Result of CASE-I for 69 bus system

Cases	Parameter	Load levels		
		50%	100%	160%
Before compensation	P_{loss} (kW)	53.31	225	643
	V_{min} (pu)	0.956	0.909	0.846
After compensation with DG	Rating of DG (location)	319(61) 281(64)	300(21) 949(61) 551(64)	382(21) 1569(61) 749(64)
	DG rating (kW)	600	1800	2700
	P_{loss} (kW)	25	77	210
	V_{min} (per unit)	0.98	0.97	0.95
	Percentage RPL	54	66	67

Table 2 Results of comparison for CASE-I

Method	DG rating (kW)	V_{min} (per unit)	Percentage RPL reduction
Bacterial foraging technique (BFT) [22]	2020	0.98	62.2
Modified BFT [22]	1870	0.97	63.2
Combined GA and PSO [23]	3000	0.99	64
Harmony search [25]	1780	0.96	62
Analytical [26]	1840	0.97	64
Proposed	1800	0.97	66

2. Case-II: Shunt Capacitor placement only:

In this case, shunt capacitors are placed for RPL reduction. Capacitors optimum location and its size are determined by the same technique. Table 3 shows results of three different loading conditions. Similarly, the best location of capacitor banks is found at bus no. 21, 61 and 64. The real power losses are reduced to 150 kW from 225 kW at nominal load level after installation of 1300 kVAR capacitors. The percentage loss reduction at all three loading levels is remarkable. The results after capacitor allocation are compared with latest optimization technique like DSA [24], FPA [1]. Table 4 exhibits the comparison of results for Case-II on various parameters such as real power loss, percentage loss reduction, minimum voltage profile, rating and size of capacitors with other proposed techniques in the literature. It is quite evident to say that percentage loss reduction for the proposed technique accounts for 33.34% which is better than FPA [1] which yields 32.44% of RPL reduction. Analogously the voltage profile is also enhanced considerably after placement of capacitor units. It is clearly reported from results reported

Table 3 Result of Case-II for 69 bus system

Load levels		50%	100%	160%
After capacitor allotment only	Rating of capacitor (kVAr) with position	420(61)	720(61)	1550(61)
		70(21)	230(21)	220(21)
		160(64)	350(64)	620(64)
	Total size (kVAr)	640	1300	2390
	Prealloss (kW)	37	150	400
	V_{min} (pu)	0.97	0.931	0.88
Power loss reduction in %		30.6	33.34	37.8

Table 4 Results compared with other techniques for test system-I (CASE-II)

Parameters	Without capacitor	DSA [24]	FPA [19]	Proposed
Real power loss (kW)	225	147	152	150
% loss reduction	–	34.66	32.44	33.34
V_{min} (pu)	0.909	0.93	0.93	0.93
Rating of capacitor (location) (kVAr)	–	900(61)		720(61)
		450(15)	1450(61)	230(21)
		450(60)		350(64)
Total size in kVAr	–	1800	1450	1300

above that losses reduce significantly with simultaneously decrease in capacitor size as compared to other contemporary approaches.

3. Case-III: Placement of DGs and capacitor concurrently:

Table 5 exhibits brief picture of results for concurrent allotment of DG and capacitor of 69 bus system. At nominal load level, a reduction of 94.05% is observed for real power losses in Table 5. The size identified by the proposed technique for both DG and capacitor are 1800 kW and 1300 kVAr, respectively, as shown in Table 6. It can be observed from the table; the size of DG units investigated by PSO, IMDE, BBO, ICA, IPSO techniques is more than the proposed technique for nearly same loss reduction (Fig. 5).

Table 5 Result of CASE-III

Case	Items	Loading levels		
		Light loading (50%)	Nominal loading (100%)	Heavy loading (160%)
Base case	P_{loss} (kW)	51.61	225	652.47
	Reactive power loss (kVAr)	24.28	102.15	290.25
	V_{min} (pu)	0.956	0.9092	0.845
Allocation of DG and capacitor	DGs size (kW)	600	1800	2700
	Capacitors size (kVAr)	660	1300	2340
	Ploss (kW)	8.60	13.05	38.9
	% real power loss reduction	83.33%	94.05%	94%
	Reactive power loss	5.04	10.35	30.23
	% Reactive power loss reduction	79.4%	90%	89.5%
	V_{min} (pu)	0.985	0.99	0.974

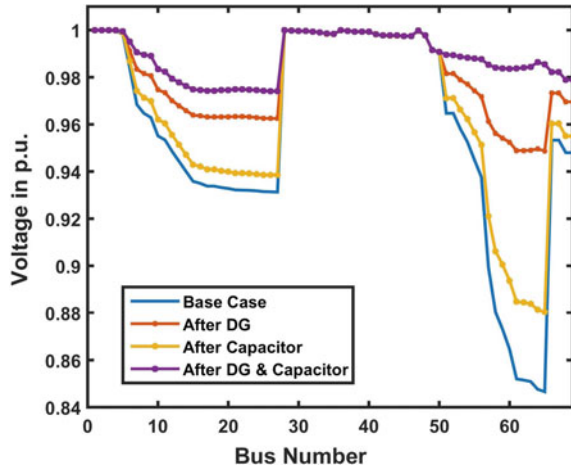
Table 6 Comparative results for CASE-III

Parameters	PSO [12]	IMDE [15]	BBO [7]	ICA [22]	IPSO [8]	Proposed
DGs size in MW	1.82	2.21	2.32	1.83	1.81	1.8
Capacitors size in MVar	1.3	1.3	2.7	1.3	2.1	1.3
RPL in kW	23.2	13.9	55	23.21	17.32	13.05
% loss reduction (%)	89.70	93.85	75.6	89.68	92.3	94.05
V_{min} (pu)	0.98	0.99	0.97	0.972	0.9775	0.99

5 Conclusions

A novel and simple technique is presented here to minimize RPL in DS. The prominent objective of power loss has been attained by appropriate allotment of DG and capacitors. A new mathematical formulation, Loss Constant (LC), is formulated for finding candidate bus position and rating. The efficacy of projected method is examined on standard 69 bus system at three different loading conditions. Results of

Fig. 5 Voltage outline of 69 bus system (heavy loading level for CASE-III)



standard test system are compared with latest optimization approaches and achieved optimal for all load levels. The proposed technique yields significant upgrading in bus voltages and RPL reduction after placement of DG and capacitor unit simultaneously.

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