Design of Low Standby Power 10T SRAM Cell with Improved Write Margin

R. Manoj Kumar and P. V. Sridevi

Abstract There is a growing concern regarding the increased standby power and reduced stability of SRAM due to continued scaling in technology node. So, there is a necessity to design a new SRAM cell which addresses the concerns related to SRAM cell. So, 10T SRAM cell is proposed with reduced standby power and enhanced stability in read, write and hold modes of operation. There is a reduction in standby power because of the usage of stacked transistors. P10T SRAM cell has decreased the standby power while holding 1 by 4.9%, 15.99% and 1.68% compared to 8T, 8TG and 9T respectively at the worst process corner FF at 0.9 V V_{DD}. There is an increase of 262.89, 47.566, 261.75% write margin compared to 6T, 8TG, 9T SRAM cells at 0.9 V supply voltage for TT corner. The influence of process and voltage variations on write margin was studied on available and proposed SRAM cells. All designs are designed using in cadence virtuoso in 45 nm CMOS technology node.

Keywords Static noise margin · Write margin · Process corners · Standby power

1 Introduction

In computing systems, static random access memory (SRAM) forms the basic building block which occupies considerable area and consumes considerable amount of power. This necessitates stable and low standby power SRAM for portable devices [1]. Applications like implantable biomedical devices, wireless sensor networks (WSN), and battery-based electronic devices often require low power consumption in the present trend. Devices using FPGA are increasingly preferred day by day, because of its reconfigurability and prototyping capability, to develop advanced embedded applications [2, 3]. FPGA based on SRAM forms a significant portion of overall FPGA market. Reduction in power supply voltage quadratically decreases active power and linearly decreases standby power but restricted by PVT variations

R. Manoj Kumar (✉) · P. V. Sridevi
Department of Electronics and Communication Engineering, Andhra University College of Engineering (A), Andhra University, Visakhapatnam, Andhra Pradesh 530008, India
e-mail: manojkumar.rongali@gmail.com

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[4]. As the supply voltage is decreased, standby power dominates the active power [5]. This significant increase in standby power is going to have an increased impact in SRAM cells as most of the cells tend to operate in standby mode [6].

6T SRAM cell suffers from read–write sizing conflict and also the RSNM degradation. In [7], asymmetric sizing was used to improve the stability of SRAM cell but with increased leakage currents. In [8], 4T read port is used to reduce the leakage but at the expense of increased area and less write margin. Chang et al. [9] proposed an 8T SRAM cell which isolates the read path from the storage nodes to increase RSNM. But it suffers from low write margin. A multi-threshold 9T SRAM was proposed in [10] for the energy efficiency, but it requires extra boosted supply. SRAM cell in [11] has P-P-N devices. It has low leakage power, but the cell has degraded write ability. In [12, 13], reduction in leakage power was reported with slight increase in area. In [14], data-dependent power supply SRAM cell for low leakage has been reported.

Static noise margin is used to determine the SRAM cell stability in hold and read modes of operation, respectively. In write operation, stability is determined by write margin (WM).

The paper is comprised of the following. Section 2 explains the existing SRAM designs. Section 3 describes the proposed SRAM design with operation. Section 4 compares the existing SRAM cells with the proposed SRAM cell w.r.t. standby power, HSNM, RSNM, and write margin. Section 5 concludes.

2 Existing SRAM Designs

6T SRAM cell shown in Fig. 1 is the conventional design which is formed using two cross-coupled inverters to latch the data while the access transistors are separately used to perform either read or write operation. Cell ratio and pull up ratio decide the stability in read and write operation, respectively. In 8TG SRAM cell [15] is similar to 6T SRAM cell, but the access transistors are replaced with transmission gates. In [9], read port has been isolated which gives an option to optimize the read and write SNMs individually. In [16], an addition NMOS has been added to the read port for further reduction of leakage power.

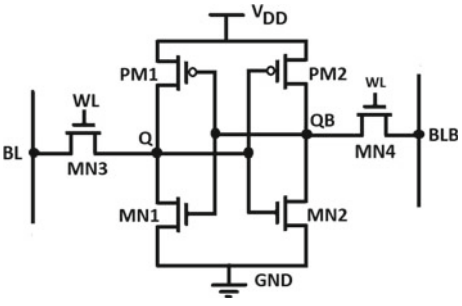

Fig. 1 6T SRAM cell

3 Proposed 10T SRAM Cell (P10T)

Existing SRAM designs suffer from one of the aspects like high leakage power, less write stability, and less read stability. So, in order to maintain the stability with less leakage power, a new SRAM cell is proposed with 10 transistors (P10T) as shown in Fig. 2. Table 1 lists different control signals status in different modes of operation. Stacked transistors PM3 and MN2 were used which reduces leakage. PM3, PM4, MN2, and MN4 assist in high write ability.

3.1 Write Operation

While performing write operation PM3 and MN2 are disconnected from the power supply rails by keeping the control signals WLPU and WLPD at Logic 1 and 0, respectively. This brings down either *Q* or QB from its stored value to its complement at a faster pace. When Logic 0 is stored, WL is enabled, BL is set to Logic 1 and its complement to BLB, RWL is disabled, WLB is enabled which performs write 1 into

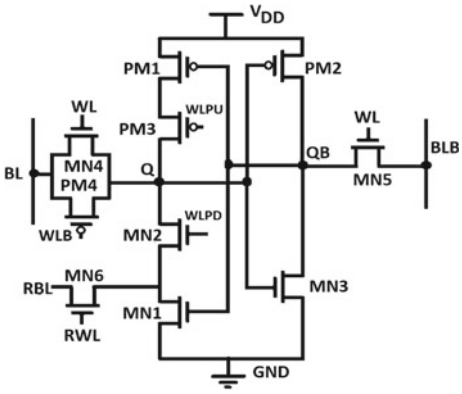

Fig. 2 Proposed 10T SRAM cell

Table 1 Control signals for P10T SRAM cell

	Hold	Read	Write 1/0
BL	1	1	1/0
BLB	1	1	0/1
WL	0	0	1
WLB	1	1	0
WLPU	0	0	1
WLPD	1	1	0
RWL	0	1	0
RBL	1	1	0

the storage node Q. When Logic 1 is stored, WL is enabled, BL is set to Logic 0 and its complement to BLB, RWL is disabled, WLB is enabled which performs write 0 into the storage node Q.

3.2 Read Operation

In read mode, WL and WLB are disabled, WLPU and WLPD are kept at Logic 0 and Logic 1, respectively, RWL is enabled which turns ON MN6, RBL is precharged to V_{DD}. When $Q = 0$, MN1 is ON creating a path for RBL to be discharged to ground. When $Q = 1$ and $QB = 0$, MN1 is OFF creating no path for RBL to discharge to ground. Based on the value of RBL, sense amplifier senses and gives the output.

3.3 Hold Operation

WL, WLB, and RWL are disabled, WLPU and WLPD are kept at Logic 0 and Logic 1, respectively, which forms the cross-coupled inverters to latch the data.

4 Results and Discussion

4.1 Standby Power

As the majority of SRAM cells operate in standby mode, standby power or leakage power reduction is essential. It is estimated as the multiplication of supply voltage and the current flowing through it [17]. Standby power is analyzed in the proposed SRAM (P10T) cell along with the other SRAM cells available in the literature. Figure 3 shows standby power at different process corners at 0.9 V V_{DD}. There is

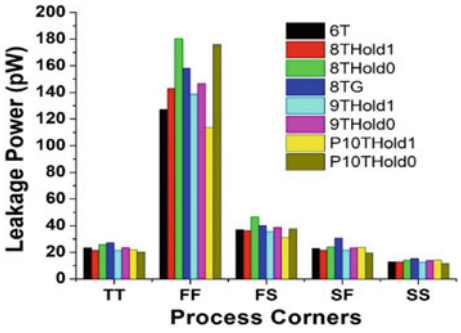

Fig. 3 Standby power comparison at 0.9 V supply voltage for all process corners

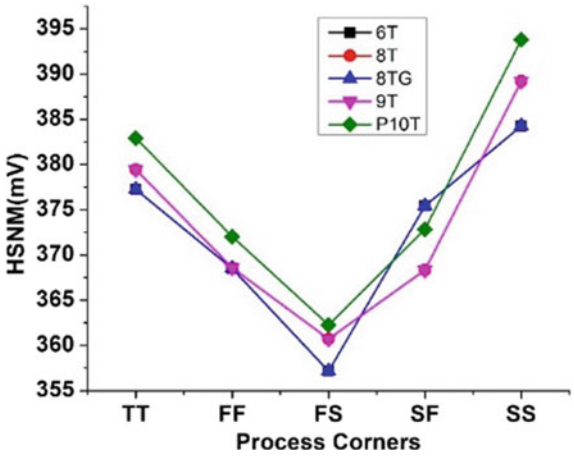

Fig. 4 HSNM comparison at 0.9 V supply voltage for all process corners

a significant reduction in standby power due to the usage of stacked transistors in pull down and pull up network. P10T SRAM cell decreased the standby power while holding 1 by 4.91%, 15.99% and 1.68% compared to 8T, 8TG and 9T respectively at the worst process corner FF. Hold 1 power of P10T has also decreased by 7.5%, 4.62%, 19.03% compared to 8TG at TT, FS and SF corners respectively.

4.2 Hold Stability

While SRAM is operating in hold mode, stability can be determined by HSNM which can be estimated by the butterfly curve. As the control signals of transistors PM3 and MN2 are kept at Logic 0 and 1, respectively, both the transistors are turned ON which replicates the two back to back inverters similar to 6T SRAM cell. From Fig. 4, HSNM slightly increased at all process corners except at SF corner.

4.3 Read Stability

Read stability is analyzed using the metric RSNM. Side length of largest square that can be fitted in the butterfly curve gives RSNM [18]. Read current through the storage nodes degrades RSNM. Due to this 6T, 8TG, P10T SRAM cell has lower RSNM. 8T, 9T SRAM cells have isolated the flow of read current through the storages nodes which leads to higher RSNM as shown in Fig. 5.

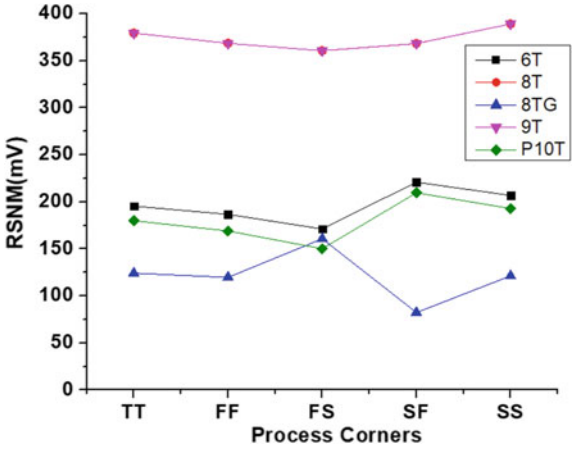

Fig. 5 RSNM comparison at 0.9 V supply voltage for all process corners

4.4 Write Stability

In 6T, 8TG SRAM cells, enhancement of write margin is restricted by the sizing of access transistor, pull down and pull up transistors. So read port is isolated in 8T, 9T, and P10T SRAM cells which gives freedom to separately size the devices which further enhances read and write stability individually. In P10T SRAM cell, PM3 and MN2 are disconnected to the power rails by the control signals WLPU and WLPD, respectively, and the usage of transmission gate enhances the write stability. Write margin is calculated using World Line sweep method [19]. Figure 6 shows the estimated write margin values at all process corners.

In Fig. 7, write margin is also observed for wide supply voltage range at TT corner. It clearly indicates P10T has enhanced write stability than other SRAM cells.

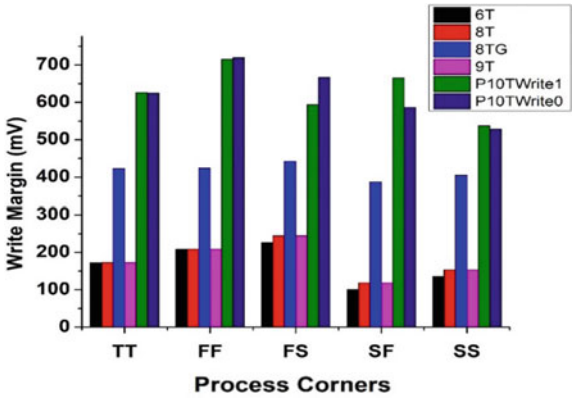

Fig. 6 Write margin comparison at 0.9 V supply voltage for all process corners

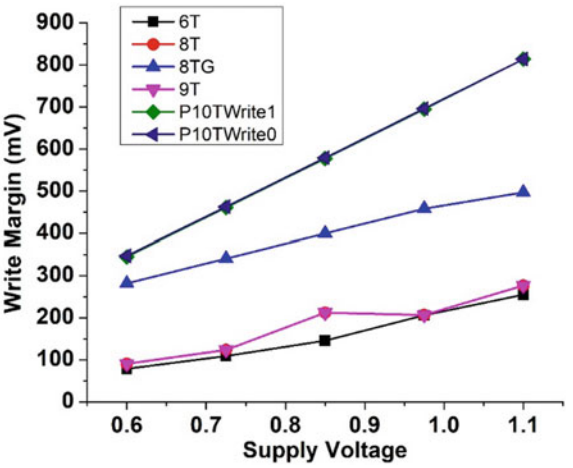

Fig. 7 Write margin comparison at various supply voltages for TT corner

5 Conclusion

Design metrics like standby power and stability are the major parameters that need to be considered while designing the SRAM cell. Though available SRAM cells excel in one of the design metrics, they suffer degradation in other design metrics. The proposed 10T (P10T) cell provides less standby power and enhanced write margin while having decent HSNM.

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