Single-Ended Low Power Robust 9T Static Random Access Memory Using FinFETs

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Abstract Advancement in CMOS technology has made the Static Random Access Memory (SRAM) design to be very demanding. The designers face several challenges in improving the performance by improving read stability, write ability and leakage power. The design in the proposed design uses power gating strategy to lower leakage power. It is known that for 2 bit-line scheme of SRAM, some amount of power is wasted in the form of charging or discharging the bit-lines. The design in the proposed cell dissipates 67.7% less leakage power, 58.18% less writing power and 70.78% less reading power when compared to the double bit-line SRAM at 1 V of supply voltage. In addition to it, the design has good read stability, write ability and better read/write performance.

Keywords N-curve · Low leakage current · FinFETs · SRAM

1 Introduction

The performance of any system greatly depends on SRAM as it is the key contributor to the area in any system. In addition to it, the demand for mobile gadgets and also various applications such as wireless body sensing networks that is due to the tremendous growth in technology has led to the need for low power SRAM designs. Hence, the research in the area of SRAM towards developing the designs that are of high speed and low power has gained importance in recent years [1–3]. The designer will face many challenges while designing the low power SRAM as it is known that at deep sub-micrometer technology, the design margin and process variation makes it very difficult for subthreshold operation. The amount of leakage power in total

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power dissipation is also increasing with technology node [4], [5] and this leads to an enormous expansion in Read Static Noise Margin (RSNM) that might lead to increase in the read failure rate [4]. Fin Field Effect Transistors(FinFET) are the promising technology that can replace the conventional Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET).

The read stability and write ability of 6T SRAM cell degrades with V_{dd} scaling and these degrade to undesired levels with very low supply voltage which has become quite common due to advancement in CMOS processes. Several designs have been already proposed to overcome the problems explained before. Some of them are 7T [6], 8T [7], 9T [8], 10T [9]. In all these proposed designs, the core of the cell is isolated from the read path so that the read-write disturbance that was faced by 6T SRAM cell can be eliminated. There are separate bit-lines for reading and writing and read path consist of two extra transistors and this makes 8T SRAM [7] structure which increases the (Static Noise Margin) SNM but will also increase leakage power due to the use of two transistors in read path and moreover this increase with V_{dd} scaling. A differential scheme that uses differential read and write was proposed in [8] wherein more number of transistors are attached to the bit-lines. Due to the increase in the number of connections to the bit-line, the parallel use of the SRAM bit-line is limited and this affects the array that is to be implemented using this structure. In [9], a new structure that uses 10T which is very suitable for bit interleaved architecture was designed. The buffers were used to decrease the leakage power but due to the use of two transistors in the write path, the write margin was decreased which reflected the difficulty in write operation.

Looking into above-specified constraints and solutions, we have proposed a new SRAM structure that consists of 9T and this will consume less power and also dissipate low leakage power. The proposed design is robust as it takes less time for both read and write operations when compared to other existing designs.

2 Proposed 9T SRAM Cell Design

The design of the proposed 9T SRAM design is shown in Fig. 1. There are two isolated bit-lines for read and write operations and these are termed as Read-bit-line (RBL) and Write-bit-line(WBL). The other control signals are write word-line (WWL), read word line (RWL) and SLEEP control signal. The SLEEP control signal is provided as a part of power gating strategy. Except for hold operation, for all the other operations, the circuit will be connected to full power supply and for the hold operation, it will be connected to half of the power supply. This will help to decrease the leakage power during the standby mode of operation.

Since the proposed design has single-end write, to facilitate the write operation, Virtual Ground (VGND) pin is provided. The condition of different control signals is shown in Table 1.

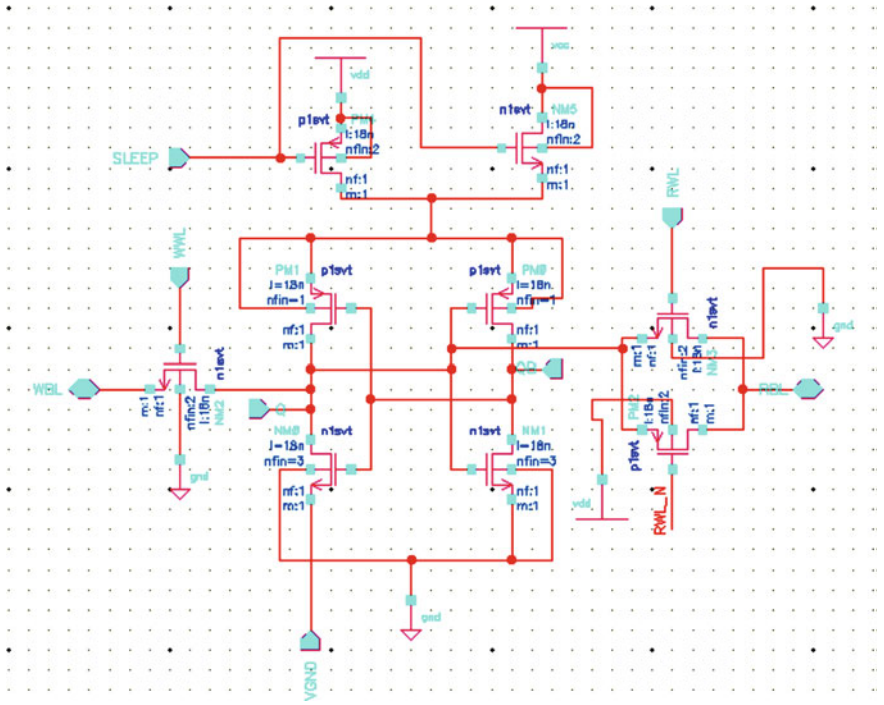

Fig. 1 Schematic of the proposed design

Table 1 Operation table of the proposed 9T SRAM cell

Signal	Hold	Read	Write
WBL	–	–	VDD/GND
WWL	GND	GND	VDD
RWL	GND	VDD	GND
VGND	GND	GND	FLOAT
SLEEP	VDD	GND	GND

3 Simulation Setup

The proposed cell is simulated for its functionality and different performance measures are calculated using Cadence Virtuoso tool. The technology used is FinFET based and is of 18 nm. The different parameters considered for comparison are read stability, write ability, read and write access time, read and write power and leakage power.

The stability of any SRAM design is decided by the Static Noise Margin (SNM). The noise margins must be measured to confirm that there is no destruction of data stored in the cell takes place. Static noise margin is usually measured with the help

of butterfly curve [10]. It is already shown that N-curve gives better information regarding stability [11].

- Read Stability and Write Ability: As explained earlier, the static power noise margin gives information regarding the read stability. More the SPNM more is the read stability. Write Trip Power (WTP) acts as a parameter to compare the write ability of different cells.
- Read and Write Access time: It is the time taken for the activation of the word-line responsible for the read operation to the change in the bit-line value to reach the stored bit value. The thresholds considered for this operation were 10% of the low voltage value to 90% of the high voltage value. Write access time '1' is described as the time required for writing, logical '1' is the time duration between the activation of the word-line responsible for the write operation to that of the time taken to change the output node 'Q' to '1'. Similarly, write access time '0' is described as the time required for writing, logical '0' is the time duration between the activation of the word-line that is responsible for the write operation to that of the time taken to change the output node 'Q' to '0'.
- Read/Write Power: The amount of power dissipated for successful write operation is known as write power and the amount of power dissipated doing a successful read operation is known as read power.
- Leakage power: The subthreshold leakage at deep sub-micrometer technology nodes in embedded cache is a very serious issue [12]. The major source for the leakage power is the cross coupled inverter which is the core of any SRAM cell that helps in storing the data of interest indefinitely given that the power supply is present. For the proposed design, the transistors are maintained to be of minimum size. Since the proposed design uses power gating strategy, the leakage power dissipation should be minimum.

4 Results

The simulation is done to validate the functionality of the proposed cell. The graphs of various simulation results are shown in the following figures. Figure 2 shows the simulation of write, hold and read operation in the proposed design. As shown in Fig. 2, all the operations can be performed successfully in the proposed design. Table 2 shows the comparison of physical features that are considered for comparison.

Table 3 shows the comparison of performance parameters between SRAM cells. If SVNM and SINM are considered that tells about the read stability, it can be observed that for SVNM the proposed design has the least value but for SINM it has the highest value. Thus, to overcome this confusion, SPNM can be considered and it can be observed that the proposed cell has the best read stability. For write ability, the WTV and WTI must be minimum and it can be observed that for WTV, the proposed cell has very high value and WTI is very less thus to actually determine the write ability, we need to consider the WTP and it can be seen that the proposed cell has

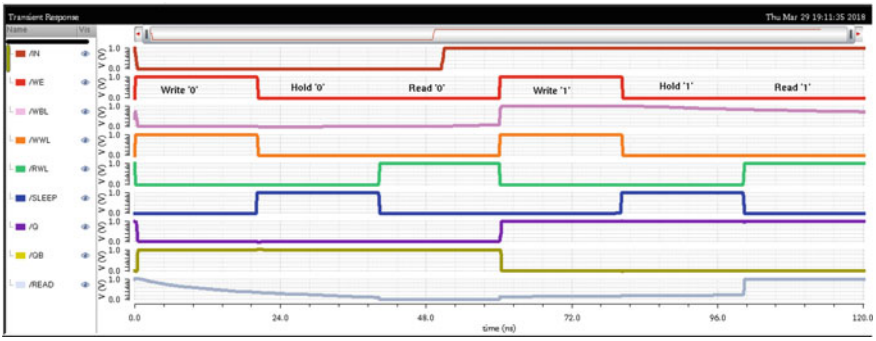

Fig. 2 Write, hold and read operation

the lowest value thus showing that the proposed cell has the best write ability. The read and write access time are comparable with the existing designs. For the read and write power although the proposed design doesn't consume the least power but will consume very less power compared to [9]. The leakage power is reduced to greater extent due to the use of the power gating strategy.

5 Conclusion

A robust single-ended low power 9T SRAM cell is designed and is tested for its operations. Further, the designed SRAM cell is correlated with the existing designs and it is observed that the proposed cell has good read stability and write ability. Due to the use of transmission gate in the read path, the read access time is reduced to a greater extent. Due to the use of power gating strategy, the leakage power is also reduced to a greater extent. If the proposed is compared with the dual bit-line scheme of SRAM that has same number of transistors, i.e. [9] then it can be said that the proposed cell dissipates 67.67% of less leakage power and consumes approximately 26%, 43.42% less power for reading and writing data '0'and 70.8%, 58.18% less power for reading and writing data '1'. The access time to read '0' is little high due to the use of single-ended scheme but it is compensated in the form of less power consumption for read and write operations.

Thus it can be said that the designed 9T single bit-line cell while maintaining the performance measures shows very low power consumption with less leakage power dissipation.

Table 2 Comparison of physical features of SRAM cell comparison

Cell feature	Conv. 6T	Ramy. 7T [6]	Fried. 8T [7]	Liu. 9T [8]	Wen. 8T [13]	Chang. 10T [9]	ST1 [14]	ST2 [15]	Prop novel 9T SRAM
Reading/ Write	Diff/Diff	SE/SE	SE/Diff	Diff./Diff	SE/SE	Diff/Diff	Diff/Diff	Diff/Diff	SE/SE
Bit-lines	2-BL	1-WBL 1-RBL	1-RBL 2- WBL	2-BL	1-WBL 1-RBL	2-BL	2-BL	2-BL	1-WBL 1-RBL
Control signals	1-WL	1-WL 1-W 1-R	1-WWL 1-RWL	1-WR 2-RD	1-WWL 1-WL 1-RWL	1-WWL 1-WL 1-VGND	1-WL	1-WL 1-WWL	1-WWL 1-RWL 1-VGND 1-SLEEP
No. of tran in read path	2	2	2	2	2	2	2	2	2

Diff—Differential, BL—Bit-line, SE—Single-Ended, WBL—Write BL, RBL—Read BL, WWL—Write BL, RBL—Read BL, VGND—Virtual Ground

Table 3 Performance parameter comparison of SRAM cells

Performance parameter	Conv. 6T	Ramy. 7T [6]	Fried. 8T [7]	Liu. 9T [8]	Wen. 8T [13]	Chang. 10T [9]	ST1 [14]	ST2 [15]	Prop novel 9T SRAM
SVNM	0.416 V	0.416 V	0.452 V	0.472 V	0.472 V	0.472 V	0.592 V	0.467 V	0.363 V
SINM	50.59 µA	42.5 µA	24.85 µA	26.85 µA	30.5 µA	26.84 µA	36.85 µA	31.35 µA	32.5 µA
SPNM	14.09 µW	11.924 µW	18.63 µW	18.6361 µW	20.76 µW	18.632 µW	25.55 µW	20.39 µW	27.26 µW
WTV	0.582 V	0.582 V	0.527 V	0.527 V	0.3042 V	0.5273 V	0.406 V	0.535 V	0.635 V
WTI	−19.1 µA	−19.08 µA	−18.24 µA	−18.242 µA	−30.06 µA	−18.24 µA	−18.2 µA	−18.2 µA	−15.46 µA
WTP	−8.342 µW	−8.34 µW	−13.2 µW	−13.43 µW	−22.47 µW	−13.43 µW	−12.75 µW	−13.52 µW	−7.31 µW
Read access time ‘0’	64.36 ps	6.37 ps	24.79 ps	9.85 ps	33.32 ps	12.72 ps	12.45 ps	6.9 ps	20.44 ps
Read access time ‘1’	71.88 ps	21.88 ps	30.23 ps	16.04 ps	26.3 ps	14.64 ps	14.64 ps	25.74 ps	15.35 ps
Write access time ‘0’	92.97 ps	100.3 ps	103 ps	138.7 ps	95.32 ps	113.3 ps	98.82 ps	111.3 ps	82.52 ps
Write access time ‘1’	92.47 ps	67.75 ps	94.26 ps	160.1 ps	112.3 ps	152.5 ps	116.4 ps	104 ps	119.5 ps
Read power ‘0’	72.54 nW	398 nW	131.1 nW	219.4 nW	142.4 nW	2930 nW	3869 nW	2464 nW	162.3 nW
Read power ‘1’	74.31 nW	244.1 nW	74.22 nW	218.8 nW	3025 nW	2930 nW	3369 nW	44.92 nW	63.84 nW
Write power ‘0’	107.3 nW	124.3 nW	125.4 nW	200.3 nW	194.8 nW	168.2 nW	158.6 nW	110.8 nW	110.2 nW
Write power ‘1’	2931 nW	160.4 nW	87.61 nW	214.2 nW	194 nW	151.9 nW	167.2 nW	85.69 nW	89.57 nW
Leakage power	13.37 µW	15.48 µW	14 µW	9.9 µW	50 µW	15.48 µW	18.22 µW	10.25 µW	3.26 µW

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