Chapter 11
Integrated Full-Duplex Radios: System Concepts, Implementations, and Experimentation

Tingjun Chen, Jin Zhou, Gil Zussman, and Harish Krishnaswamy

Abstract This chapter reviews recent research on integrated full-duplex (FD) radio systems using complementary metal oxide semiconductor (CMOS) technology. After a brief review of challenges associated with integrated FD radios, several CMOS FD radio designs, particularly those developed at Columbia University, are discussed with self-interference (SI) suppression at antenna interface, and in RF, analog, and digital domains. This chapter also reviews the system design and implementation of two generations of FD radios developed within the Columbia FlexICoN project (Columbia full-duplex wireless: From integrated circuits to networks (FlexICoN) project, https://flexicon.ee.columbia.edu) using off-the-shelf components and a software-defined radio (SDR) platform. The performance evaluation of these FD radios at the node- and link-level is also reviewed.

11.1 Introduction

Recent demonstrations leveraging off-the-shelf components and/or commodity SDRs (such as [4–12]) have established the feasibility of FD wireless through SI suppression at the antenna interface and SI cancellation (SIC) in the RF, analog, and digital domains.

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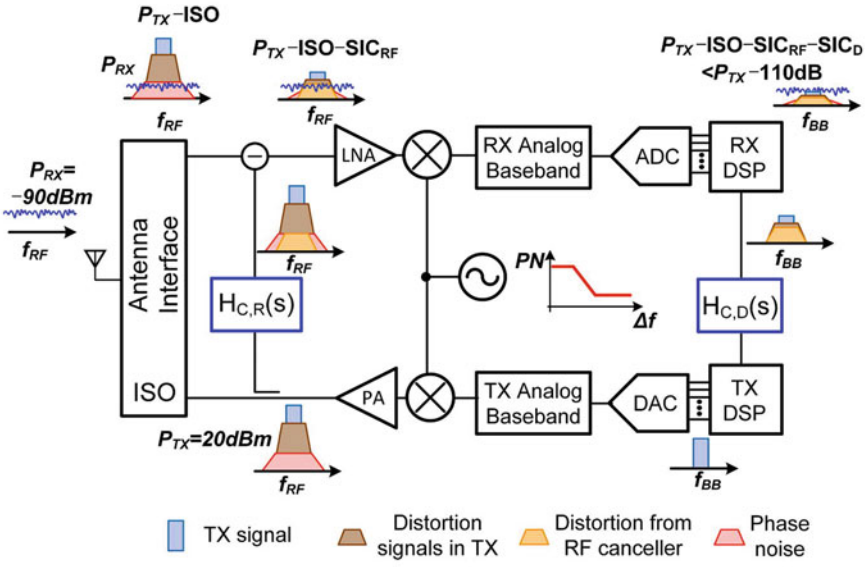
From the recent advancement in CMOS IC technology, complex digital SIC algorithms that offer about 50 dB SIC can be readily implemented [7]. However, many existing FD demonstrations rely on RF/analog cancellers and antenna interfaces (such as ferrite circulators) that are bulky, use off-the-shelf components, and do not readily translate to compact and low-cost IC implementations. For example, a pair of separate TX and RX antennas was considered in [4, 6], a single antenna with a coaxial circulator was used in [7], and dually polarized antennas for achieving SI isolation was utilized in [8]. Moreover, these FD radios are often equipped with an RF canceller implemented using discrete components [7, 9], where the techniques applied are usually difficult to be realized in RFIC. Below, we first present challenges associated with the design and implementation of IC-based FD radios, followed by an overview of the research efforts in this area within the Columbia FlexICoN project.

11.1.1 Challenges Associated with Compact and Low-Cost Silicon-Based Implementation

Realizing RF/analog SIC and FD antenna interface in an IC is critical to bring FD wireless technology to mobile devices, such as handsets and tablets [3, 13–24]. Figure 11.1 depicts the block diagram of an FD radio that incorporates antenna, RF and digital SI suppression. The indicated transmitter and minimum received signal power levels are typical of Wi-Fi applications. Also depicted are various transceiver non-idealities that further complicate the SI suppression problem.

11.1.1.1 Achieving >100 dB SI Suppression

The power levels indicated in Fig. 11.1 necessitate >110 dB SI suppression for Wi-Fi like applications. Such an extreme amount of cancellation must necessarily be achieved across multiple domains (here, antenna, RF, and digital), as >100 dB precision from a single stage or circuit is prohibitively complex and power inefficient. For example, [7] demonstrated 60 dB and 50 dB SIC in the RF/analog and digital domains, respectively, with +20 dBm average TX power and −90 dBm RX noise floor. The suppression must be judiciously distributed across the domains, as suppression in one domain relaxes the dynamic range requirements of the domains downstream. Furthermore, all cancellation circuits must be adaptively configured together—optimization of the performance of a single cancellation stage alone can result in residual SI that is sub-optimal for the cancellers downstream.



		Specifications	
System Definition	TX average output power (P_{TX})	20 dBm	
	Signal Bandwidth	20 MHz	
	RX Noise Floor (P_{RX})	-90 dBm%	
	Total SIC	110 dB	
SIC in the Antenna and RF Domains	Antenna Isolation (ISO)	30 dB	50 dB
	RF SIC (SIC_{RF})	20 dB	20 dB
Analog/RF Front-End Circuit Performance	DR_{ADC}*	72 dB	52 dB
	RX Effective IIP_3#	-3 dBm	-23 dBm
	RF Canceller OIP_3#	-3 dBm	-23 dBm
	VCO Phase Noise @ 1MHz offset$	-106 dBc/Hz	-86 dBc/Hz
Digital SIC Budget	Digital SIC – Linear	60 dB	40 dB
	Digital SIC – IM3	60 dB	40 dB

* 12 dB margin has been added to DR_{ADC}.

Assume the SI-induced IM3 at the ADC input has the same power level as the residual SI after RF SIC.

% Assume 11dB implementation loss and noise figure from RX

$ Assume 10ns delay in the SI channel [41, 42].

Fig. 11.1 Block diagram of an FD radio featuring antenna, RF and digital SI suppression, along with a depiction of the various transceiver non-idealities that must also be managed for effective FD operation

11.1.1.2 Transceiver Non-idealities

The extremely powerful nature of the SI exacerbates the impact of non-idealities such as nonlinearity and phase noise, particularly for IC implementations. For instance, nonlinearity along the transmitter chain will introduce distortion products. Antenna and RF cancellation that tap from the output of the transmitter will suppress these distortion products, but linear digital cancellation will not as it operates on the undistorted digital signal. Depending on the amount of antenna and RF cancellation achieved, the analog receiver front-end may introduce distortion products as well, as may the RF cancellation circuitry. Nonlinear digital cancellation may be employed to recreate and cancel these distortion products, but the associated complexity and power consumption must be considered. Local oscillator (LO) phase noise can pose problems as well. If a common LO is used for the transmitter and the receiver, the phase noise in the transmitted and the received SI will be completely correlated, enabling its cancellation in the receiver downmixer. However, delay in the SI channel will decorrelate the phase noise, resulting in residual SI that cannot be canceled. Figure 11.1 depicts transceiver performance requirements calculated for two different SIC allocations across domains—one antenna-heavy and the other digital-heavy.

11.1.1.3 SI Channel Frequency Selectivity and Wideband RF/Analog SI Cancellation

The wireless SI channel can be extremely frequency selective. For example, a large amount of the SI signal power results from the antenna return loss in a shared antenna interface. Compact antennas can be quite narrowband, and the front-end filters that are commonly used in today's radios even more so. The wireless SI channel also includes reflections off nearby objects, which will feature a delay that depends on the distance of the object from the radio. This effect is particularly significant for hand-held devices due to the interaction with human body in close proximity. Performing wideband RF/analog cancellation requires recreating the wireless SI channel in the RF/analog domain. Conventional RF/analog cancellers feature a frequency-flat magnitude and phase response, and will therefore achieve cancellation only over a narrow bandwidth. Wideband SIC at RF based on time-domain equalization (essentially an RF finite impulse response [FIR] filter) has been reported in [7] using discrete components. However, the integration of nanosecond-scale RF delay lines on an IC is a formidable (perhaps impossible) challenge, and therefore alternate wideband RF/analog SIC techniques are required.

11.1.1.4 Compact FD Antenna Interfaces

FD radios employing a pair of antennas, one for transmit and one for receive, experience a direct trade-off between form factor and transmit–receive isolation

arising from the antenna spacing and design. Therefore, techniques that can maintain or even enhance transmit–receive isolation, possibly through embedded cancellation, while maintaining a compact form factor are highly desirable. Compact FD antenna interfaces are also more readily compatible with MIMO and diversity applications, and promote channel reciprocity, which is useful at the higher layers. For highly form-factor-constrained mobile applications, single-antenna FD is required, necessitating the use of circulators. Traditionally, circulators have been implemented using ferrite materials, and are costly, bulky, and not compatible with IC technology. Novel techniques for high-performance non-magnetic integrated circulators are of high interest.

11.1.1.5 Adaptive Cancellation

The SIC in all domains must be reconfigurable and automatically adapt to changing operation conditions (e.g., supply voltage and temperature) and most importantly, a changing electromagnetic (EM) environment (i.e., wireless SI channel), given the high level of cancellation required. This requires the periodic (or perhaps even continuous) usage of pilot signals to characterize the SI channel, the implementation of reconfigurable cancellers (which is more challenging in the antenna and RF domains), and the development of canceller adaptation algorithms.

11.1.1.6 Resource Allocation and Rate Gains for Networks with Integrated FD Radios, and Rethinking MAC Protocols

The benefits of enabling FD are clear: the uplink (UL) and downlink (DL) rates can theoretically be doubled (in both random access networks, e.g., Wi-Fi, and small cell networks). That, of course, is true, provided that the SI is canceled such that it becomes negligible at the receiver. Hence, most of the research on FD at the higher layers has focused on designing protocols and assessing the capacity gains while using models of recent laboratory benchtop FD implementations (e.g., [7]) and assuming perfect SI cancellation. However, given the special characteristics of IC-based SI cancellers, there is a need to understand the capacity gains and develop resource allocation algorithms while taking into account these characteristics. These algorithms will then serve as building blocks for the redesign of MAC protocols for FD networks with integrated FD radios.

11.1.2 Overview of the Columbia FlexICoN Project

The Columbia full-duplex Wireless: from Integrated Circuits to Networks (FlexICoN) project [1, 2] was initiated in 2014 with a special focus on the development and implementation of IC-based FD radios. To utilize the benefits of these small-form-

factor monolithically integrated FD system implementations, a careful redesign of both the physical and MAC layers and the joint optimization across these layers are needed. Moreover, the performance of the IC-based FD radios is evaluated using custom-designed prototypes and testbeds.

Figure 11.2 shows the overview of this interdisciplinary project with highlights on some of the advances on the IC design and testbed evaluations. In particular, we

1. developed novel antenna interfaces such as integrated CMOS non-reciprocal circulators that utilize time-variance to break Lorentz reciprocity;
2. developed several generations of FD radio ICs employing RF/analog SIC circuits to combat noise, distortion, and bandwidth limitations;
3. implemented FD radio prototypes and evaluated their performance using an SDR testbed in various network settings;
4. developed resource allocation and scheduling algorithms in the higher layers.

In this book chapter, we review some of the recent advances within the Columbia FlexICoN project on the design and implementation of CMOS circulators and IC-based FD radios (Sect. 11.2). We also review the design and implementation of two generations of FD radio prototype using an SDR testbed and their experimental evaluation (Sect. 11.3).

11.2 Integrated Full-Duplex Radios

As mentioned in Sect. 11.1.1, despite many challenges associated with compact and low-cost silicon-based FD radio implementation, many recent works have demonstrated integrated FD radios with SI suppression in different domains and at RF and millimeter-wave frequencies. Integrated wideband RF SIC receiver front-ends have been demonstrated using time-domain and frequency-domain equalization techniques [20, 25]. Compared to a time-domain approach, a frequency-domain-equalization-based design allows generation of large group delay on chip [25]. Other recently reported wideband RF SIC includes an FD receiver using baseband Hilbert transform equalization [26] and an FD transceiver using mixed-signal-based RF SIC [21]. The integrated Hilbert transform-based wideband RF SIC is similar to that in [25] and has the additional advantage of requiring a fewer number of canceller taps. The mixed-signal-based RF SIC [21] has great flexibility thanks to the powerful DSP but cannot cancel the noise and nonlinear distortion generated in the transmitter chain. At the antenna interface, integrated electrical-balance duplexers [27–30] have been demonstrated. However, these reciprocal antenna interfaces feature a fundamental minimum of 3 dB loss (typically higher when parasitic losses are factored in). A CMOS passive non-magnetic circulator has been reported lately in [31] and is integrated with an SI-canceling FD receiver in [18]. Complete integrated FD transceivers have also been reported and showed promising results at RF and millimeter-wave frequencies [15–17, 23, 24]. In this remaining of

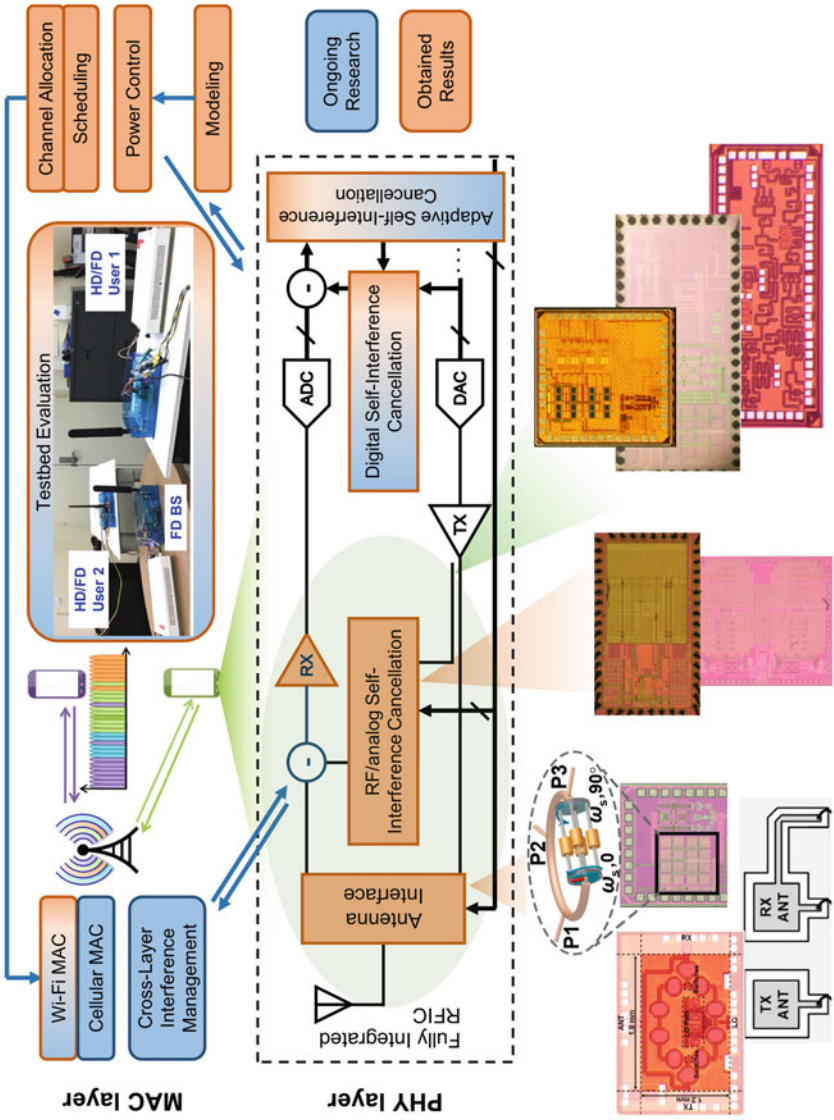


Fig. 11.2 Overview of the Columbia FlexICoN project

this section, we focus on integrated FD radio systems that developed at Columbia University.

11.2.1 Integrated RF Self-Interference Cancellation

To address the challenge related to integrated RF cancellation across a wide bandwidth, we proposed a frequency-domain approach in contrast to the conventional time-domain delay-based RF FIR approach [25]. To enhance the cancellation bandwidth, second-order reconfigurable bandpass filters (BPFs) with amplitude and phase control are introduced in the RF canceller (Fig. 11.3). An RF canceller with a reconfigurable second-order RF BPF features four degrees of freedom (amplitude, phase, quality factor, and center frequency of the BPF). *This enables the replication of not just the amplitude and phase of the antenna interface isolation* $[H_{SI}(s)]$ *at*

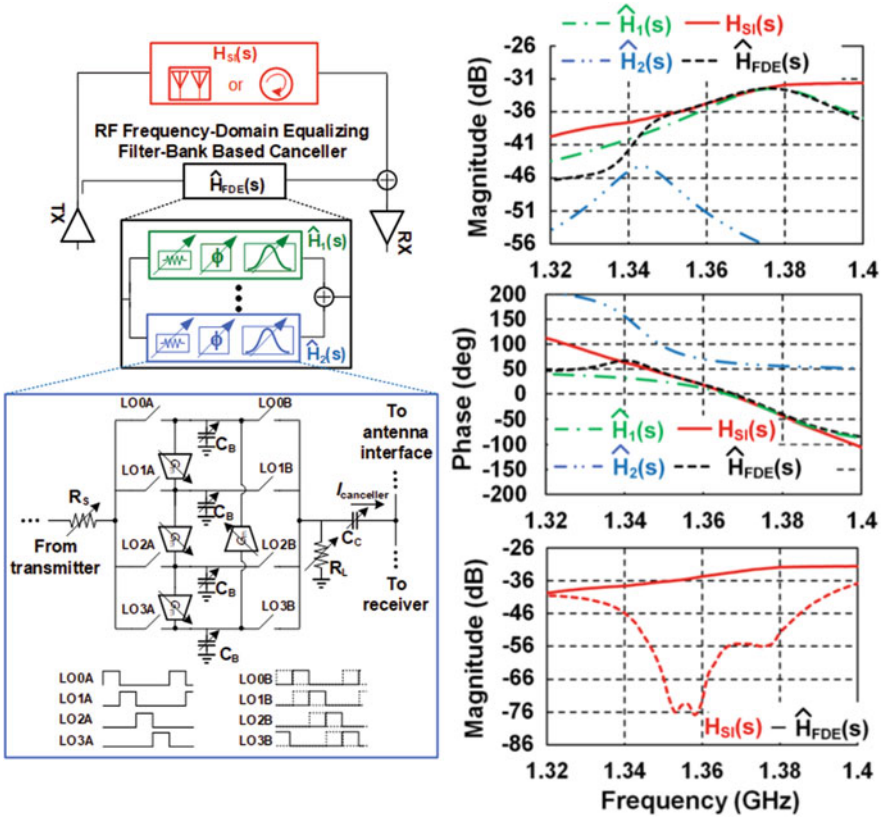


Fig. 11.3 Integrated wideband RF SIC based on frequency-domain equalization (FDE): FDE concept and two-port G_m-C N-path filter with embedded variable attenuation and phase shift

a frequency point, but also the slope of the amplitude and the slope of the phase (or group delay). The use of a bank of filters with independent BPF parameters enables such replication at multiple points in different sub-bands, further enhancing SIC bandwidth. Essentially, this approach is frequency-domain equalization (FDE) in the RF domain. In Fig. 11.3, which represents a theoretical computation on the measured isolation of a pair of 1.4 GHz antennas that are described in greater detail below, two BPFs with transfer functions $\hat{H}_1(s)$ and $\hat{H}_2(s)$ emulate the antenna interface isolation in two sub-bands resulting in an order of magnitude improvement in the SIC bandwidth over a conventional frequency-flat RF canceller.

For FDE, reconfigurable RF filters with very sharp frequency response (or high quality factor) are required. Assuming second-order BPFs with 10 MHz bandwidth are used for FDE-based SIC, a filter quality factor of 100 is required at 1 GHz carrier frequency. Furthermore, the required filter quality factor increases linearly with the carrier frequency assuming a fixed absolute filter bandwidth. The achievable quality factor of conventional LC-based integrated RF filters has been limited by the quality factor of the inductors and capacitors that are available on silicon. However, recent research advances have revived a switched-capacitor circuit-design technique known as the N-path filter that enables the implementation of reconfigurable, high-quality filters at RF in nanoscale CMOS IC technology [32]. Figure 11.3 depicts a two-port N-path filter, where R_S and R_L are the resistive loads at the transmit and receive sides, respectively. C_C weakly couples the cancellation signal to the receiver input for SIC. The quality factor of an N-path filter may be reconfigured via the base-band capacitor C_B, given fixed R_S and R_L. Through clockwise/counterclockwise (only counterclockwise connection is shown in Fig. 11.3 for simplicity) connected reconfigurable transconductors (G_m), an upward/downward frequency offset with respect to the switching frequency can be introduced without having to change the clock frequency [32]. Variable attenuation can be introduced by reconfiguring R_S and R_L relative to each other. *Interestingly, phase shifts can be embedded in a two-port N-path filter by phase shifting the clocks driving the switches on the output side relative to the input-side clocks as shown in Fig. 11.3 [25].* All in all, the ability to integrate reconfigurable high-quality RF filters on chip using switches and capacitors uniquely enables synthesis of nanosecond-scale delays through FDE over time-domain equalization.

A 0.8–1.4 GHz FD receiver IC prototype with the FDE-based RF SI canceller was designed and fabricated in a conventional 65 nm CMOS technology (Fig. 11.4) [25]. For the SIC measurement results shown in Fig. 11.4, we used a 1.4 GHz narrowband antenna-pair interface with peak isolation magnitude of 32 dB, peak isolation group delay of 9 ns, and 3 dB of isolation magnitude variation over 1.36–1.38 GHz. The SI canceller achieves a 20 dB cancellation bandwidth of 15/25 MHz (one/two filters) in Fig. 11.4. When a conventional frequency-flat amplitude- and phase-based canceller is used, the SIC bandwidth is about 3 MHz ($>8\times$ lower). The 20 MHz bandwidth over which the cancellation is achieved allows our FD receiver IC to support many advanced wireless standards including small-cell LTE and Wi-Fi.

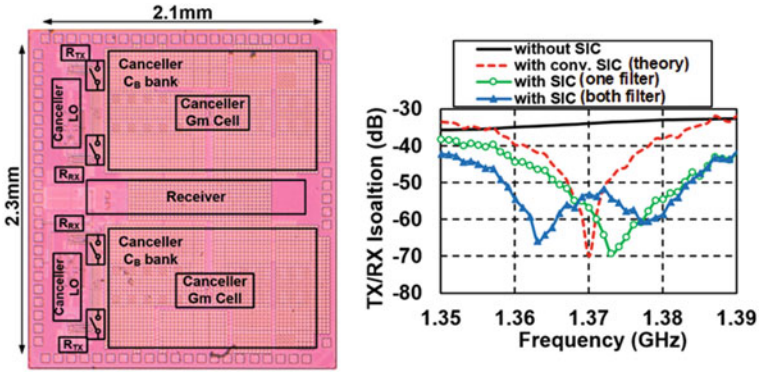


Fig. 11.4 Chip photo of the implemented 0.8–1.4 GHz 65 nm CMOS FD receiver with FDE-based SIC in the RF domain featuring a bank of two filters (left); transmit–receive isolation of an antenna pair without SIC, with conventional SIC (theoretical), and with the proposed FDE-based SIC (right)

11.2.2 Full-Duplex Receiver with Integrated Circulator and Analog Self-Interference Cancellation

Mobile applications constrained by form factors, particularly at RF frequencies where the wavelength is considerably higher, require single-antenna solutions. Single-antenna FD also ensures channel reciprocity and compatibility with antenna diversity and MIMO concepts. However, *conventional single-antenna FD interfaces, namely non-reciprocal circulators, rely on ferrite materials and biasing magnets, and are consequently bulky, expensive, and incompatible with silicon integration.* Reciprocal circuits, such as electrical-balance duplexers [27], have been considered, but are limited by the fundamental minimum 3 dB loss in both TX-antenna (ANT) and ANT-RX paths.

As mentioned earlier, non-reciprocity and circulation have conventionally been achieved using the magneto-optic Faraday effect in ferrite materials. However, it has recently been shown that violating time-invariance within a linear, passive material with symmetric permittivity and permeability tensors can introduce non-reciprocal wave propagation, enabling the construction of non-magnetic circulators [33, 34]. However, these initial efforts have resulted in designs that are either lossy, highly nonlinear, or comparable in size to the wavelength, and are fundamentally not amenable to silicon integration. *Recently, we introduced a new non-magnetic CMOS-compatible circulator concept based on the phase non-reciprocal behavior of linear, periodically time-varying (LPTV) two-port N-path filters that utilize staggered clock signals at the input and output [31].*

N-path filters, described earlier in the context of FDE, are a class of LPTV networks where the signal is periodically commutated through a bank of linear, time-invariant (LTI) networks. We found that when the non-overlapping clocks

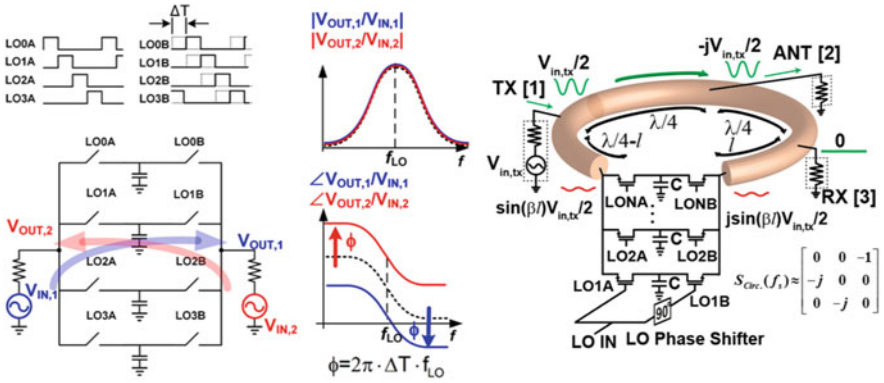


Fig. 11.5 Integrated non-magnetic circulator for single-antenna FD: non-reciprocity induced by phase-shifted N-path commutation (left); 3-port circulator structure obtained by placing the non-reciprocal two-port N-path filter with ±90° phase shift within a 3λ/4 transmission line loop (right)

driving the input and output switch sets of a two-port N-path filter are phase shifted with respect to each other, a non-reciprocal phase shift is produced for signals traveling in the forward and reverse directions as they see a different ordering of the commutating switches (Fig. 11.5). The magnitude response remains reciprocal and low-loss, similar to traditional N-path filters. To create non-reciprocal wave propagation, an N-path-filter with ±90° phase shift is placed inside a 3λ/4 transmission line loop (Fig. 11.5). This results in satisfaction of the boundary condition in one direction (−270° phase shift from the loop added with −90° from the N-path filter) and suppression of wave propagation in the other direction (−270°+90° = −180°), effectively producing unidirectional circulation. Additionally, a three-port circulator can be realized by placing ports anywhere along the loop as long as they maintain a λ/4 circumferential distance between them. Interestingly, maximum linearity with respect to the TX port is achieved if the RX port is placed adjacent to the N-path filter ($l = 0$), since the inherent TX–RX isolation suppresses the voltage swing on either side of the N-path filter, enhancing its linearity.

A prototype circulator based on these concepts operating over 610–850 MHz was implemented in a 65 nm CMOS process. Measurements reveal 1.7 dB loss in TX-ANT and ANT-RX transmission, and broadband isolation better than 15 dB between TX and RX (the narrowband isolation can be as high as 50 dB). The in-band ANT-RX IIP3 is +8.7 dBm while the in-band TX-ANT IIP3 is +27.5 dBm (OIP3 is +25.8 dBm), two orders of magnitude higher due to the suppression of swing across the N-path filter. The measured clock feedthrough to the ANT port is −57 dBm and IQ image rejection for TX-ANT transmission is 49 dB. Techniques such as device stacking in SOI CMOS can be explored to further enhance the TX-ANT linearity to meet the stringent requirements of commercial wireless standards. Clock feedthrough and IQ mismatch can be calibrated by sensing and injecting appropriate

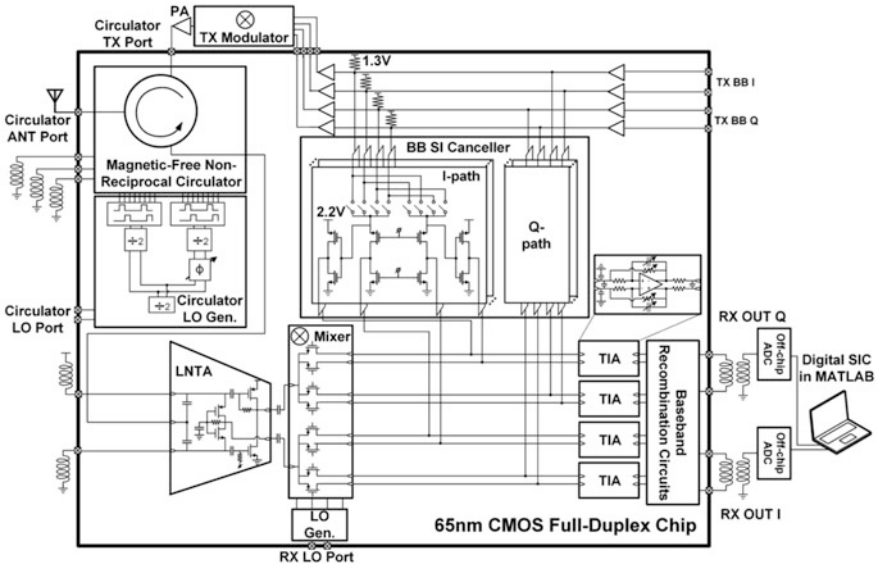


Fig. 11.6 Block diagram and schematic of the implemented 65 nm CMOS FD receiver with non-magnetic circulator and additional analog BB SI cancellation

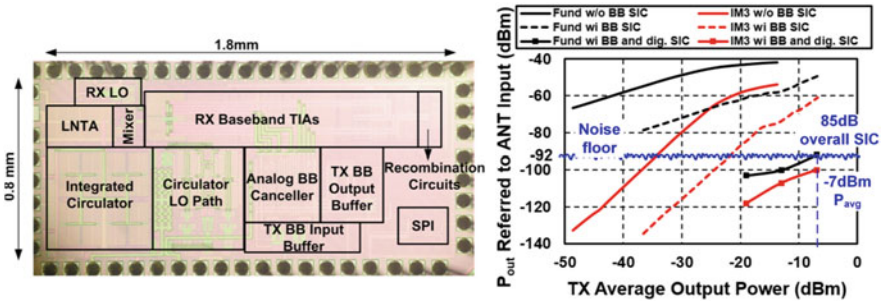


Fig. 11.7 Chip microphotograph of the implemented 65 nm CMOS FD receiver with non-magnetic circulator and additional analog BB SI cancellation (left), and measured two-tone SI test with SI suppression across circulator, analog BB and digital domains (right)

BB signals through the N-path filter capacitor nodes as shown previously in the literature [35].

A 610–850 MHz FD receiver IC prototype incorporating the non-magnetic N-path-filter-based passive circulator and additional analog baseband (BB) SI cancellation (shown in Figs. 11.6 and 11.7) was also designed and fabricated in the 65 nm CMOS process [36]. SI suppression of 42 dB is achieved across the circulator and analog BB SIC over a bandwidth of 12 MHz. Digital SIC has also been implemented in Matlab after capturing the BB signals using an oscilloscope (effectively an 8-bit 40 MSa/s ADC) (Fig. 11.7). The digital SIC cancels not only the

main SI but also the IM3 distortion generated on the SI by the circulator, receiver, and canceller. A total 164 canceller coefficients are trained by 800 sample points. After digital SIC, the main SI tones are at the −92 dBm noise floor, while the SI IM3 tones are 8 dB below for −7 dBm TX average power. This corresponds to an overall SI suppression of 85 dB for the FD receiver.

11.3 Full-Duplex Testbed and Performance Evaluation

To experimentally evaluate the developed RF cancellers at the system-level, we prototyped two generations of FD radios using the National Instruments (NI) Universal Software Radio Peripheral (USRP) software-defined radios (SDRs). Figure 11.8 shows the block diagram of a prototyped FD radio with an RF SI canceller and a USRP SDR, where the RF SI canceller taps a reference signal at the output of the power amplifier (PA) and performs SIC at the input of the low-noise amplifier (LNA) at the RX side. Since interfacing the RFIC cancellers described in Sect. 11.2 to an SDR presents numerous technical challenges, we designed and implemented RF cancellers emulating their RFIC counterparts using discrete components on printed circuit boards (PCBs).

The Gen-1 FD radio [37] includes a frequency-flat amplitude- and phase-based RF canceller, which emulates its RFIC counterpart presented in [38]. An improved version of the Gen-1 RF SI canceller has been recently integrated in the open-access ORBIT testbed [39, 40] to support research. The Gen-2 FD radio [41, 42] includes a wideband frequency-domain equalization- (FDE-) based RF canceller, which emulates its RFIC counterpart presented in [25]. In this section, we review the design and implementation of the RF cancellers, and their integration with USRP SDRs and performance evaluation.

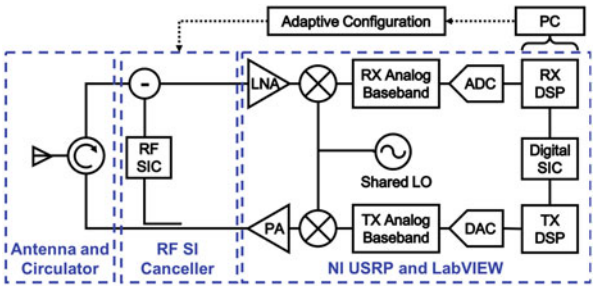


Fig. 11.8 Block diagram of a prototyped FD radio with an antenna, a circulator, an RF SI canceller, and a USRP SDR

11.3.1 Gen-1 Full-Duplex Radio with a Frequency-Flat Amplitude- and Phase-Based RF Canceller

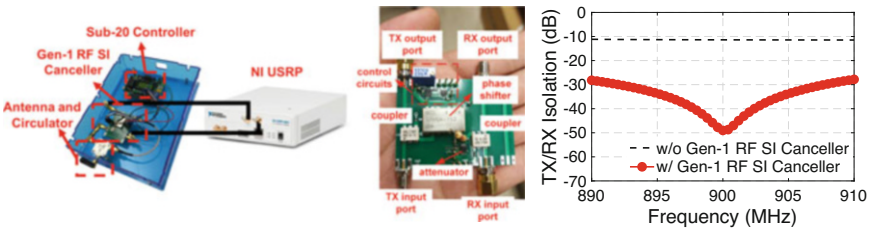
Figure 11.9(a) shows the prototyped Gen-1 FD radio, which consists of an antenna, a circulator, a Gen-1 RF SI canceller, and an NI USRP-2932. The operating frequency of the NI USRP is configured to be 0.9 GHz, which is the same as the operating frequency of both the circulator and the RF SI canceller. The USRP is controlled from a PC that runs NI LabVIEW, which performs digital signal processing.

The implemented Gen-1 RF SI canceller depicted in Fig. 11.9(b) operates from 0.8 to 1.3 GHz and is configured by a SUB-20 controller through the USB interface. In particular, (1) the attenuator provides an attenuation range from 0 to 15.5 dB with a 0.5 dB resolution, and (2) the phase shifter is controlled by an 8-bit digital-to-analog converter (DAC) and covers the full 360° range with a resolution of about 1.5°. In the rest of the section, we describe the adaptive RF canceller configuration, the digital SIC algorithm, and the FD wireless link demonstration.

An Adaptive Gen-1 RF SI Canceller Configuration Scheme

We model the frequency-flat amplitude- and phase-based RF SI canceller depicted in Fig. 11.9(b) by a transfer function $H = Ae^{(-j\phi)}$, in which A and ϕ are the amplitude and phase controls of the RF canceller that need to be configured to match with that of the antenna interface at a desired frequency. Note that the Gen-1 RF SI canceller can only emulate the antenna interface at a single frequency point, resulting in narrowband RF SIC. As shown in Fig. 11.9(c), 40 dB RF SIC is achieved across 5 MHz bandwidth.

Ideally, only two measurements with different configurations of (A, ϕ) are needed to compute the optimal configuration, $(A^\star, \phi^\star)$. However, in practice, the USRP has an unknown RF front-end gain, denoted by G_{USRP}, which complicates the estimation of the amplitude and phase that the RF SI canceller should mimic. Therefore, we implemented an adaptive RF canceller configuration scheme using four measurements for the three unknowns A, ϕ, and G_{USRP}. After an initial



(a) (b) (c)

Fig. 11.9 (**a**) The Gen-1 FD radio composed of an antenna, a circulator, a conventional frequency-flat amplitude- and phased-based RF SI canceller, and an NI USRP, (**b**) the Gen-1 0.8–1.3 GHz frequency-flat amplitude and phase-based RF SI canceller, and (**c**) the measured TX/RX isolation where 40 dB RF SIC is achieved across 5 MHz bandwidth

configuration is obtained, a local tuning is followed to search for the optimal (A, ϕ). This scheme is described below and consists of two phases. While operating, if the FD radios encounter noticeable changes in the measured residual SI power level, the adaptive configuration scheme is triggered to recompute the canceller configuration.

1. *Initial Configuration*: To obtain the initial RF SI canceller configuration, denoted by (A_0, ϕ_0), the FD radio takes four measurements with different configurations of (A, ϕ): $(0,\ 0°)$, $(A',\ 0)$, $(A',\ 90°)$, and $(A',\ 270°)$, where A' is a known attenuation set manually. Denote by r_i $(i = 1, 2, 3, 4)$ the residual SI power with the i^{th} configuration, (A_0, ϕ_0) can be obtained (in closed-form) by solving the following equations

$$\begin{aligned} G_{\text{USRP}} \cdot (r_1)^2 &= (A_0)^2, \\ G_{\text{USRP}} \cdot (r_2)^2 &= (A_0 \cos\phi_0 - A')^2 + (A_0 \sin\phi_0)^2, \\ G_{\text{USRP}} \cdot (r_3)^2 &= (A_0 \cos\phi_0)^2 + (A' - A_0 \sin\phi_0)^2, \\ G_{\text{USRP}} \cdot (r_4)^2 &= (A_0 \cos\phi_0)^2 + (A' + A_0 \sin\phi_0)^2. \end{aligned}$$

   From our experiments, the RF SI canceller with the initial configuration, (A_0, ϕ_0), can provide around 15 dB RF SIC across 5 MHz bandwidth.
2. *Local Adjustments*: After obtaining initial configuration, the FD radio performs a finer grained local tuning around (A_0, ϕ_0) to further improve the performance of RF SIC.

Digital SIC

The residual SI after isolation and cancellation in the antenna and RF domains is further suppressed in the digital domain. The digital SI canceller is modeled as a truncated Volterra series and is implemented based on a nonlinear tapped delay line to cancel both the main SI and the inter-modulation distortion generated on the SI. Specifically, the output of the discrete-time SI canceller, y_n, can be written as a function of the current and past TX digital baseband signals, x_n and x_{n-k} (k represents the delay index), i.e.,

$$y_n = \sum_{k=0}^{N} h_{1,k} x_{n-k} + \sum_{k=0}^{N} h_{2,k} {x_{n-k}}^2 + \sum_{k=0}^{N} h_{3,k} {x_{n-k}}^3, \tag{11.1}$$

in which N corresponds to the maximum delay in the SI channel and $h_{i,k}$ $(i = 1, 2, 3)$ is the ith order digital canceller coefficient. Depending upon the SI channel, higher order nonlinear terms can be included (the model in (11.1) only includes up to the 3rd-order nonlinearity). Using a pilot data sequence, the digital SI canceller coefficients can be found by solving the least-square problem.

An FD Wireless Link Demonstration

In [37], we demonstrated an FD wireless link consisting of two Gen-1 FD radios. In particular, each FD radio transmits a 5 MHz multi-tone signal with 0 dBm average

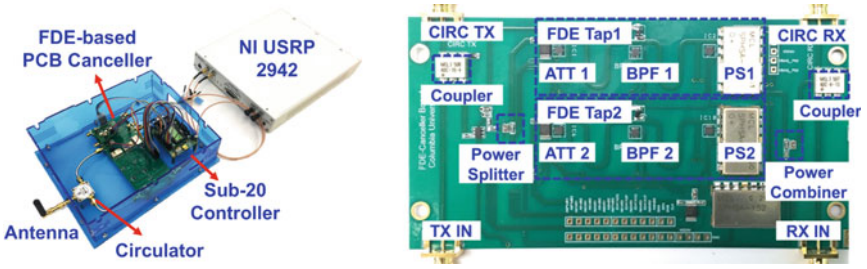
TX power and +10 dBm peak TX power, and the SI signal is canceled to the −90 dBm USRP RX noise floor after SIC in both the RF and digital domains.

In particular, 40 dB SI suppression is provided by the circulator and the Gen-1 RF SI canceller before the USRP RX. The digital SIC achieves an additional 50 dB suppression, after which the desired signal is detected.

11.3.2 Gen-2 Full-Duplex Radio with a Frequency-Domain Equalization-Based RF Canceller

Figure 11.10a shows the prototyped Gen-2 FD radio, which consists of an antenna, a circulator, a Gen-2 wideband FDE-based RF SI canceller, and an NI USRP-2942.

Figure 11.10b shows the Gen-2 FDE-based RF SI canceller with 2 FDE taps implemented using discrete components. In particular, a reference signal is tapped from the TX input using a coupler and is split into two FDE taps through a power divider. Then, the signals after each FDE tap are combined and RF SIC is performed at the RX input. Each FDE tap consists of a reconfigurable 2nd-order BPF, as well as an attenuator and phase shifter for amplitude and phase controls. The BPF is implemented as an RLC filter with impedance transformation networks on both sides, and is optimized around 900 MHz operating frequency. The center frequency of the BPF in the ith FDE tap can be adjusted through a 4-bit digitally tunable capacitor in the RLC resonance tank. In order to achieve a high and adjustable BPF quality factor, impedance transformation networks including transmission-lines (T-Lines) and 5-bit digitally tunable capacitors are introduced. In addition, the programmable attenuator has a tuning range of 0–15.5 dB with a 0.5 dB resolution, and the passive phase shifter is controlled by a 8-bit digital-to-analog converter (DAC) and covers full 360° range.



(a) (b)

Fig. 11.10 (**a**) The Gen-2 FD radio composed of an antenna, a circulator, a wideband FDE-based RF SI canceller, and an NI USRP, (**b**) the Gen-2 wideband FDE-based RF SI canceller implemented using discrete components

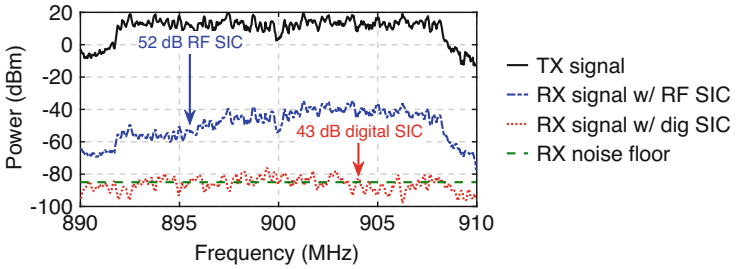


Fig. 11.11 Power spectrum of the received signal after SIC in the RF and digital domains with +10 dBm average TX power, 20 MHz bandwidth, and −85 dBm receiver noise floor

Optimized Gen-2 RF SI Canceller Configuration

Consider a wideband OFDM-based PHY layer and let $f_k (k = 1, 2, \ldots, K)$ be the frequency of the k^{th} subcarrier. Denote by $H_{\text{SI}}(f_k)$ and $H^{\text{FDE}}(f_k)$ the frequency responses of the SI channel[1] and the FDE-based RF SI canceller, respectively. The optimized RF canceller configuration can be obtained by solving the following optimization problem:

$$\min : \sum_{k=1}^{K} \left| H_{\text{SI}}(f_k) - H^{\text{FDE}}(f_k) \right|^2$$

$$\text{s.t.} : \text{constraints on configuration parameters of } H^{\text{FDE}}(f_k), \ \forall k.$$

In particular, the goal is to select the RF canceller configuration (i.e., the values of the attenuator, phased shifter, and digitally tunable capacitors in each FDE tap) so that it best emulates the SI channel. In [42], we developed and experimentally validated a mathematical model of the frequency response of the implemented FDE-based RF SI canceller, which can be pre-computed and stored for obtaining the optimized RF canceller configuration. In practice, a finer grained local tuning is also included to further improve the RF SIC.

Overall SIC

Figure 11.11 shows the power spectrum of the received signal at the Gen-2 FD radio after RF SIC and digital SIC, respectively, where the digital SIC is implemented using the same method as described in Sect. 11.3.1. The results show that an average 95 dB SIC can be achieved by the Gen-2 FD radio across 20 MHz bandwidth, supporting a maximum average TX power of 10 dBm (a maximum peak TX power of 20 dBm) with the −85 dBm USRP receiver noise floor. In particular, 52 dB and 43 dB are obtained in the RF and digital domains, respectively.

[1]The SI channel here refers to the circulator TX–RX leakage after calibration of the USRP RF front-end.

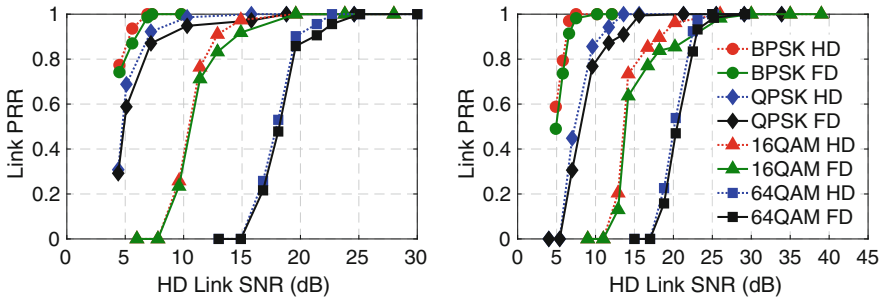


Fig. 11.12 HD and FD link packet reception ratio (PRR) with varying HD link SNR and modulation and coding schemes (MCSs). (**a**) Code rate 1/2. (**b**) Code rate 3/4

SNR-PRR Relationship at the Link-Level

We now evaluate the relationship between link SNR and link packet reception ratio (PRR). We set up a link with two Gen-2 FD radios at a fixed distance of 5 m with equal TX power. In order to evaluate the performance of our FD radios with the existence of the FDE-based RF canceller, we set an FD radio to operate in HD mode by turning on only its transmitter or receiver. We conduct the following experiment for each of the 12 modulation and coding schemes (MCSs) in both FD and HD modes,[2] with varying TX power levels and 20 MHz bandwidth. In particular, the packets are sent over the link simultaneously in FD mode or in alternating directions in HD mode (i.e., the two radios take turns and transmit to each other). In each experiment, both radios send a sequence of 50 OFDM streams, each OFDM stream contains 20 OFDM packets, and each OFDM packet is 800-Byte long.

We consider two metrics. The *HD (resp. FD) link SNR* is measured as the ratio between the average RX signal power in both directions and the RX noise floor when both radios operate in HD (resp. FD) mode. The *HD (resp. FD) link PRR* is computed as the fraction of packets successfully sent over the HD (resp. FD) link in each experiment. We observe from the experiments that the HD and FD link SNR and PRR values in both link directions are similar.

Figure 11.12 shows the relationship between link PRR values and HD link SNR values with varying MCSs. It can be seen that with sufficient link SNR values (e.g., 8 dB for BPSK-1/2 and 28 dB for 64QAM-3/4), the FDE-based FD radio achieves a link PRR of 100%. With insufficient link SNR values, the average FD link PRR is 6.5% lower than the HD link PRR across varying MCSs. This degradation is caused by the minimal link SNR difference when the radios operate in HD or FD mode [42]. Since packets are sent simultaneously in both directions on an FD link, this average PRR degradation is equivalent to an average FD link throughput gain

[2]We consider BPSK, QPSK, 16QAM, and 64QAM with coding rates of 1/2, 2/3, and 3/4.

of 1.87× under the same MCS. In [42], we also experimentally evaluated the FD gains under various network settings. These results can serve as building blocks for developing higher layer (e.g., MAC) protocols.

11.4 Conclusion

Numerous recent research efforts within the Columbia FlexICoN project and elsewhere have been focusing on IC-based FD transceivers spanning RF to millimeter-wave, reconfigurable antenna cancellation, non-magnetic CMOS circulators, and MAC layer algorithms based on realistic hardware models. While exciting progress has been made in the last few years by the research community as a whole, several problems remain to be solved before FD wireless can be widely deployed and applied. Continued improvements are necessary in IC-based FD transceivers toward increased total cancellation over wide signal bandwidth and support for higher TX power levels through improved circulator and RX linearity. Incorporation of FD in large-scale phased-array transceivers and the extension of IC-based SIC concepts to MIMO transceivers is an important and formidable challenge, due to the large number of SI channels between each pair of TX and RX. Our preliminary results on incorporating FD in phased-array and MIMO transceiver ICs within the Columbia FlexICoN project were reported in [43–45]. At the higher layers, extensive research has focused on understanding the benefits and rate gains provided by FD under different network settings. Particularly, in [46, 47], we developed and evaluated distributed scheduling algorithms with provable performance guarantees in heterogeneous networks with both half- and FD users. However, there are still several important open problems related to efficient and fair resource allocation, as well as scheduling algorithms for both cellular and Wi-Fi type of random access networks, while taking into the account the special PHY layer characteristics of FD radios. It is also important to consider interference management in these networks jointly across different layers in the network stack.

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