Chapter 77
Analysis of Three-Phase Quasi-Switched Boost Inverter Topology for Renewable Energy Applications

P. Sriramalakshmi, A. Arvindh, S. R. Sanjay Kumar, M. Prasanth and V. T. Sreedevi

Abstract A class of single-phase quasi-switched boost inverter (qSBI) topology is developed for low power renewable energy source (RES) applications. This paper analyzes a three-phase embedded-type qSBI (E-qSBI) topology which is capable of boosting and inverting the available DC voltage in a single stage. The operating modes, steady-state analysis, and pulse width modulation (PWM) control of the boost inverter topology are discussed in detail in this work. The E-qSBI supplying, 100 W RL load is designed and simulated with MATLAB/Simulink software tool. The fast Fourier transform analysis (FFT) of output voltage waveform is carried out and the harmonic profile is presented. The simulation results are presented to show the effectiveness of single-stage embedded-type qSBI topology.

Keywords Switched boost inverter (SBI) · Embedded-type quasi-switched boost inverter (E-qSBI) · Simple boost control · Shoot through · Z-source inverter (ZSI)

77.1 Introduction

Renewable energy is considered highly essential for meeting present and future energy demands. Solar photovoltaic is probably the best technology among all energy

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sources because of its clean and unlimited source of energy [1]. The voltage source inverter (VSI) performs as a power electronic interface between RES and grid [2, 3]. It is essential to connect a classical boost converter in cascade with the VSI to avail of the boosted AC voltage when the available DC source voltage is insufficient. So the resulting power converter structure becomes bulky and costly. In conventional VSI, both the upper and lower power devices in a single leg should not be on simultaneously since it causes short circuit in power supply. Dead time, shoot through and electromagnetic interference (EMI) are the major issues in traditional VSI.

To overcome all the above-mentioned issues, Z-source inverter (ZSI) are proposed in 2002 [4–6] which can perform both boosting and inversion actions in a single stage using shoot through. ZSI uses a lattice network that consists of two symmetrical LC components to boost the available voltage. Modified topologies of ZSI, like quasi-ZSI (q-ZSI), extended boost ZSI/q-ZSI [7] are presented to obtain continuous input current. In case of trans-Z-source inverter (trans-ZSI), high boosted voltage can be obtained with the help of a transformer with less number of capacitors [8]. In traditional ZSI, inductors are used to attain high-voltage gain, whereas switched inductor cells are used in switched inductor ZSI [9]. The tapped inductor ZSI (TL-ZSI [10]) and TZ-source inverter (TZSI) possess all the advantages of traditional ZSI by using transformer. There are cascaded TZSIs, cascaded multi-cell trans-ZSIs, alternate cascaded switched/tapped inductor cells that are available in the literature [11–14]. But the practical implementation of the symmetrical impedance network in ZSI is not possible. Due to the asymmetrical network, ZSI has high magnetic requirements and poor transient response [15, 16].

All the above-mentioned ZSI topologies are of bulky in size, heavy, and of large volume. The large value of passive components causes high loss and reduced efficiency. So ZSI may not be best suited for nano-grid-connected photovoltaic applications. To eliminate the complexities addressed under ZSI and its modified topologies, switched boost inverters (SBI) are proposed in [15–18]. The SBI is basically derived from Watkins–Johnson topology. The SBI inherits all the properties of ZSI. The SBI has reduced passive components count and an additional power device compared to ZSI. Also, SBI can provide AC and DC voltages simultaneously. But its input current is discontinuous.

To eliminate the drawbacks of SBI, current-fed switched inverter (CFSI) is suggested in [19]. The CFSI has the boost factor (1-D) times more than that of SBI. To produce high-voltage gain, CFSI needs to be operated at high shoot through duty ratio which makes the modulation index very less. Due to the decrement in modulation index, the total harmonic distortion (THD) in the load voltage and load current is increased and the overall gain is reduced. A family of single-phase quasi-switched boost inverter (qSBI) is proposed in [20]. There are basic qSBI, embedded qSBI, DC linked qSBI discussed in [20].

In this study, a three-phase embedded-type qSBI (E-qSBI) is designed to feed 100 W RL load. The modified simple boost PWM control technique is adopted to analyze the modes of operation. The MATLAB/Simulink tool is used for analyzing the topology, and the simulation results are presented. With the input voltage of 32 V and output AC peak voltage of 150.36 V, the gain of 4.6 is obtained. The performance

comparison between three-phase basic SBI and three-phase embedded-type qSBI is discussed. The harmonic content in the output voltage is analyzed and presented.

77.2 Conventional ZSI, SBI, E-qSBI Topologies

Figure 77.1 shows the conventional ZSI topology proposed in [4]. It consists of a diode, a LC network, and an inverter bridge. Figure 77.2 shows the conventional SBI topology proposed in [15]. In basic SBI, both the source and inverter bridges are sharing the common ground. It consists of a pair of diode (D_1, D_2), single inductor and capacitor (L, C), a single power switch (S), and an inverter bridge. The expression for boost factor in conventional ZSI and SBI is derived as [4],

$$B = \frac{1 - D}{1 - 2D} \tag{77.1}$$

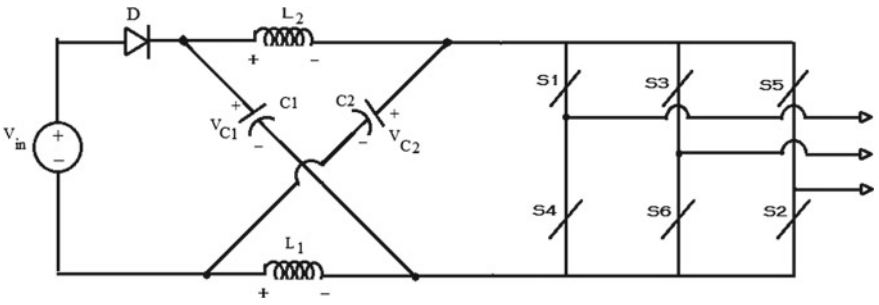

Fig. 77.1 Z-source inverter topology

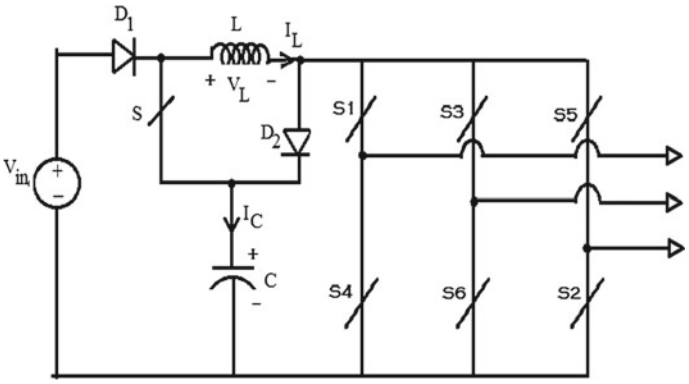

Fig. 77.2 Switched boost inverter (SBI) topology

77.3 Three-Phase Embedded-Type qSBI Operating Condition

Figure 77.3 shows the circuit diagram of E-qSBI. It consists of a single inductor L and a capacitor C, eight diodes, seven power devices and a RL load (R_l and L_l).

Figure 77.4a shows the shoot through state during which the inverter leg is shorted by turning ON both the upper and lower switches. The time interval of shoot through state is $D \cdot T_S$ where D is the duty ratio and T_S is the switching time period.

During this period, the switch S is ON and D_1, D_2 are reverse biased. The capacitor C charges the inductor. The voltage across the inverter bridge is zero. There is no power flow across the load.

The non-shoot through state is shown in Fig. 77.4b. During this state, the inverter has six active states and two open states. The time duration for this mode is $(1 - D) \cdot T_S$, and during this state, D_1, D_2 are forward biased and active switch S is kept OFF. The inductor transfers energy to the inverter circuit while the capacitor is getting charged. During this interval, the capacitor voltage is equal to the voltage across the inverter bridge. During shoot through state, the voltage across the inductor and the current through the capacitor are given by,

$$V_L = V_{in} + V_C, \tag{77.2}$$

$$I_C = -I_L. \tag{77.3}$$

where V_L is voltage across the inductor; V_{in} is the input voltage; V_C is the voltage across the capacitor; I_C is the current through the capacitor; I_L is the current through the inductor.

During non-shoot through state, the inductor voltage and capacitor current are given by

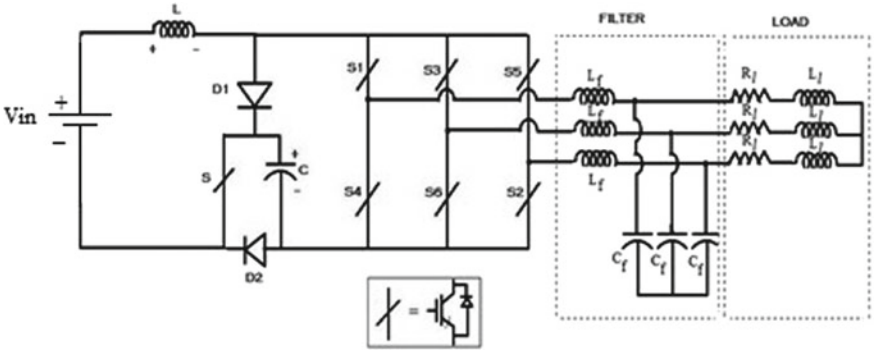

Fig. 77.3 Three-phase embedded-type qSBI supplying RL load

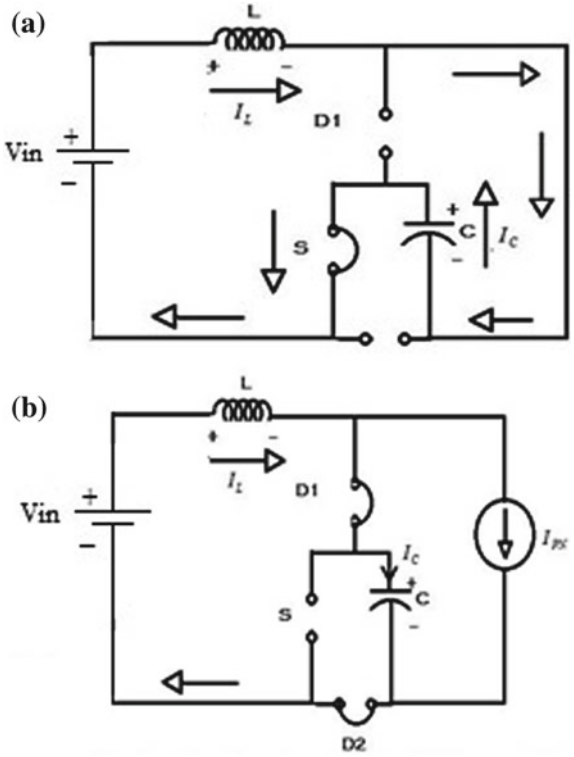

Fig. 77.4 **a** Shoot through mode of E-qSBI. **b** Non-shoot through mode of E-qSBI

$$V_{\mathrm{L}} = V_{\mathrm{in}} - V_{\mathrm{C}} \tag{77.4}$$

$$I_{\mathrm{C}} = I_{\mathrm{L}} - I_{\mathrm{PN}} \tag{77.5}$$

where I_{PN} is the inverter bridge current.

After applying volt second balance to the voltage across the inductor

$$D(V_{\mathrm{in}} + V_{\mathrm{C}}) + (1 - D)(V_{\mathrm{in}} - V_{\mathrm{c}}) = 0 \tag{77.6}$$

After applying charge second balance to the current through the capacitor

$$D(-I_{\mathrm{L}}) + (1 - D)(I_{\mathrm{L}} - I_{\mathrm{PN}}) = 0 \tag{77.7}$$

The expression for voltage across the capacitor is given by

$$V_{\mathrm{C}} = \frac{1}{1 - 2D} \cdot V_{\mathrm{in}} \tag{77.8}$$

The expression for current through the DC link is given by

$$I_{\mathrm{PN}} = \frac{1-2D}{1-D} \cdot I_{\mathrm{L}} \tag{77.9}$$

The peak DC link voltage that appears across the inverter circuit is given by

$$V_{\mathrm{PN}} = V_{\mathrm{C}} = \frac{1}{1-2D} \cdot V_{\mathrm{in}} \tag{77.10}$$

The boost factor (B) is expressed by

$$B = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{1}{1-2D} \tag{77.11}$$

77.4 The PWM Strategy of Three-Phase Embedded-Type qSBI [21]

Figure 77.5 shows the simple boost modulation technique of three-phase E-qSBI [21]. The shoot through state of the inverter bridge is required to obtain higher boost in the embedded-type qSBI.

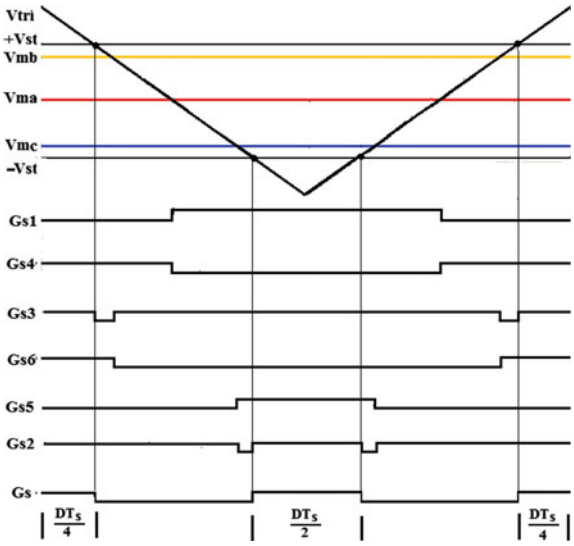

Fig. 77.5 Simple boost PWM control of three-phase E-qSBI

For that the additional active switch S needs to be operated along with the power switch in the inverter bridge.

The conventional sinusoidal PWM technique cannot be applied to generate gate signals of three-phase E-type qSBI. There are three modulation signals V_{ma}, $V_{mb,}$ V_{mc}.

The pulses for the switching devices in the inverter bridge circuit are produced by comparing these three sinusoidal signals and triangular carrier signal (V_{tri}) with high frequency.

The positive and negative shoot through envelopes $+V_{st}$ and $-V_{st}$ are compared with the triangular pulse V_{tri} to produce gate signals for switch S. The gate control signals at $\omega t = 0$ is shown in Fig. 77.5.

The fundamental peak ac load voltage is given by

$$\hat{V}_{ac} = M \cdot \frac{1}{1-2D} \cdot V_{in} \tag{77.12}$$

The voltage gain is expressed as

$$G = \frac{M}{(2 \cdot M) - 1} \tag{77.13}$$

In the modified simple boost PWM control, the sum of M and D should not exceed the value of unity so that the shoot through gating pulses can be accommodated into the conventional zero states. The above-discussed PWM control strategy can provide only the open-loop control of E-qSBI. The closed-loop control technique explained in [18] is applicable to E-qSBI also.

77.5 Design of Passive Components

The inductance and capacitance values are calculated by considering the inductor ripple current and capacitor ripple voltage as

$$\Delta I_L = \frac{V_{in} + V_C}{L} \cdot D \cdot T_S, \tag{77.14}$$

$$\Delta V_C = \frac{I_L}{C} \cdot D \cdot T_S. \tag{77.15}$$

The filter inductor L_f and capacitor C_f are designed at fundamental frequency of 50 Hz with unity gain [19].

77.6 Simulation Results

To analyze the performance of three-phase E-qSBI, simulations are done with MATLAB/Simulink. The simulated output voltage, load current, DC link boosted voltage, capacitor voltage, input current are presented with RL load. The DC voltage of 32 V is boosted and inverted with the modulation index of $M = 0.5$, shoot through duty ratio of $D = 0.453$ and switching frequency of $f_S = 10$ kHz for all power switches. Table 77.1 presents the design parameters of three-phase E-qSBI.

The input voltage and current waveforms of three-phase embedded-type qSBI are given in Fig. 77.6. The voltage stress across the switch S is presented in Fig. 77.7. The entire DC link voltage of about 282 V appears as the voltage stress across the switch.

The voltage across the capacitor and current through the inductor is presented in Fig. 77.8a, b.

Figure 77.9 presents the DC link voltage across the inverter bridge. Figure 77.10a,

Table 77.1 Design specification

Heading level	Example
Supply voltage	32 V
RMS output voltage	110 V
Capacitor	470 μF
Inductor	3 mH
Filter capacitor	10 μF
Filter inductor	3 mH
RL load	$R_l = 100\ \Omega$, $L_l = 5$ mH.

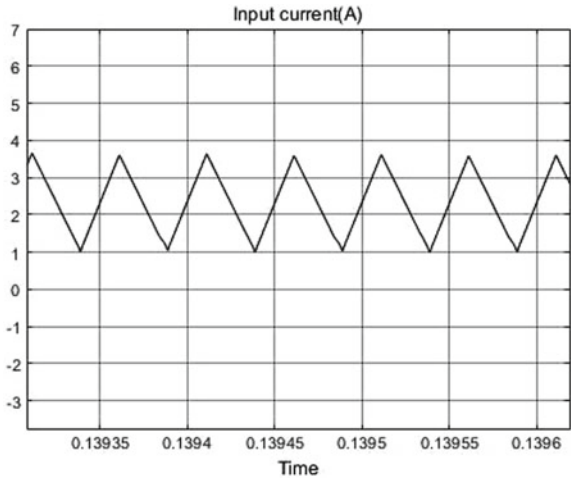

Fig. 77.6 Input voltage and input current waveform of three-phase E-qSBI

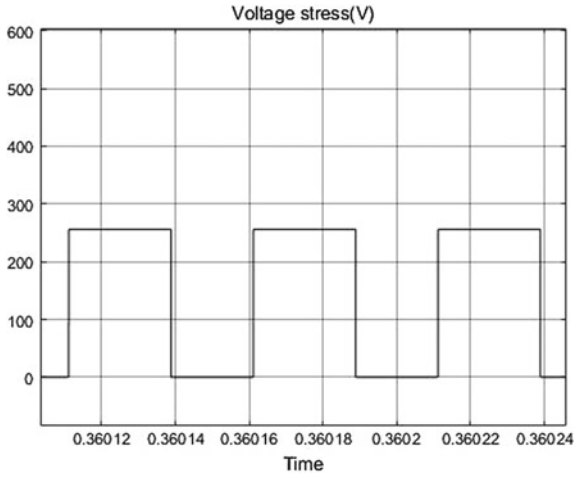

Fig. 77.7 Voltage stress across switch *S* three-phase E-qSBI

b shows the three-phase filtered load voltage and load current waveforms across the load terminals. It is understood that the input of 32 V provides the filtered AC peak output voltage of 150.36 V (rms voltage of 106.32 V) and the peak load current of 0.75 A.

The converter provides the output power of 97.5 W and gives the efficiency of 97.5% for the specification given in Table 77.1. Due to the snubber resistances and capacitances in switching devices, there are power losses which reduced the designed output load voltage.

77.7 Performance Evaluation of Three-Phase Embedded-Type qSBI with Classical ZSI and SBI

The output RMS voltage of conventional VSI, SBI, and embedded-type qSBI with $V_{in} = 32$ V, $M = 0.5$, $D = 0.453$ is obtained as follows [22]:

RMS line voltage of classical

$$\text{VSI} = \frac{\sqrt{3} \cdot M \cdot V_{in}}{2 \cdot \sqrt{2}} = 10.77 \text{ V} \tag{77.16}$$

RMS line voltage of traditional

$$\text{SBI} = \frac{\sqrt{3} \cdot M \cdot V_{in}}{2 \cdot \sqrt{2}} \cdot \frac{1 - D}{1 - 2D} = 57.205 \text{ V} \tag{77.17}$$

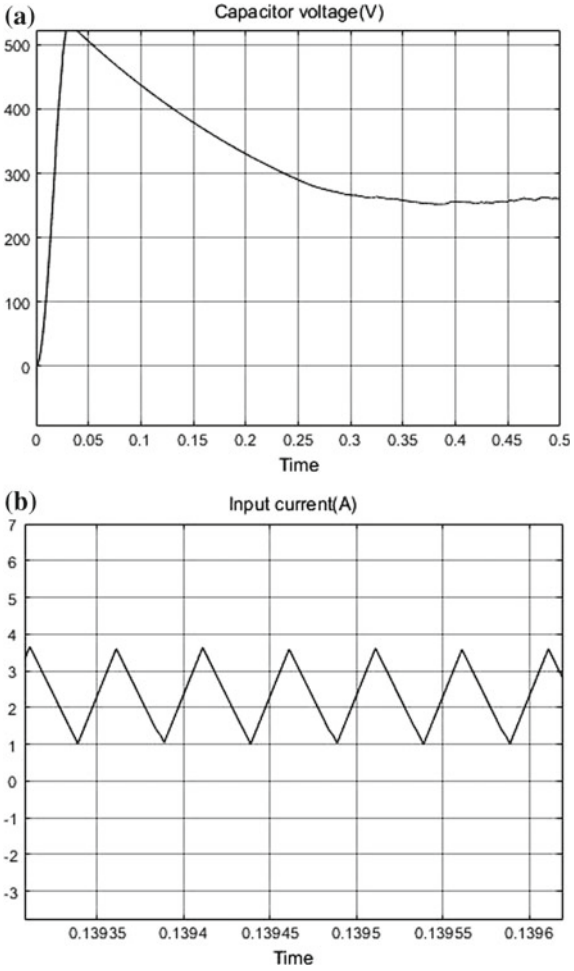

Fig. 77.8 **a** Capacitor voltage (V) waveform. **b** Inductor current (A) waveform

RMS line voltage of embedded-type

$$\text{qSBI} = \frac{\sqrt{3} \cdot M \cdot V_{\text{in}}}{2 \cdot \sqrt{2}} \cdot \frac{1}{1 - 2D} = 106.32 \text{ V}. \tag{77.18}$$

From the above expressions, it can be concluded that for same supply voltage and modulation index, the three-phase embedded-type qSBI can provide higher AC output voltage. If a DC load is connected in parallel to the capacitor, DC power could be supplied to the load. Thus, this topology can produce both DC and AC voltages as well.

Figure 77.11 shows the comparison between boost factor and duty ratio of three-

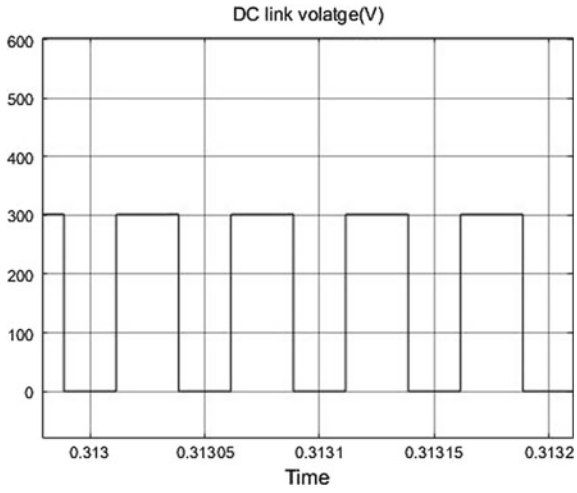

Fig. 77.9 DC link voltage across inverter bridge

phase SBI and three-phase embedded-type qSBI.

Figure 77.12 shows the harmonic profile of load voltage of E-qSBI. It is explicit that the total harmonic distortion (THD) of E-qSBI for the above-mentioned design specifications is 4.74% which meets the IEEE standard.

77.8 Conclusion

The working principle and steady-state analysis of three-phase embedded-type quasi-switched boost inverter (E-qSBI) are explained in detail. The implementation of PWM control of embedded-type qSBI is also elaborated in this paper. The measured efficiency of the three-phase E-qSBI is 97.5% with the duty ratio of $D = 0.453$ and the output power of 97.5 W. The harmonic profile of filtered load voltage is negligible due to the absence of dead time. The simulation results obtained are very well in consistent with theoretical expressions, and it can be concluded that E-qSBI is best suited for renewable source-based high-voltage gain applications. The results can further be verified with the hardware implementation. This work can be extended to detain the dynamic stability by implementing a suitable closed-loop control technique.

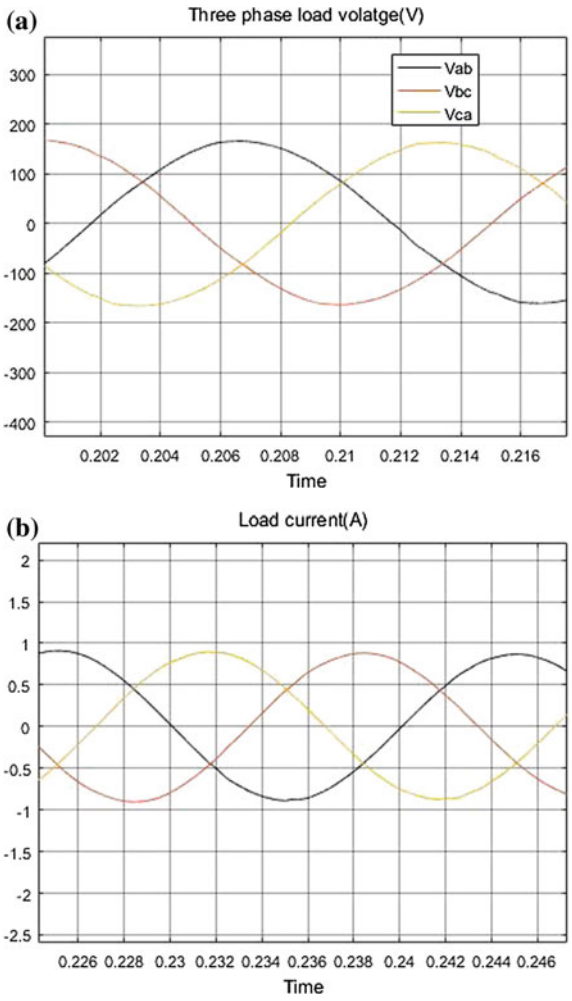

Fig. 77.10 **a** Three-phase output voltage across load terminals. **b** Three-phase current waveform across load terminals

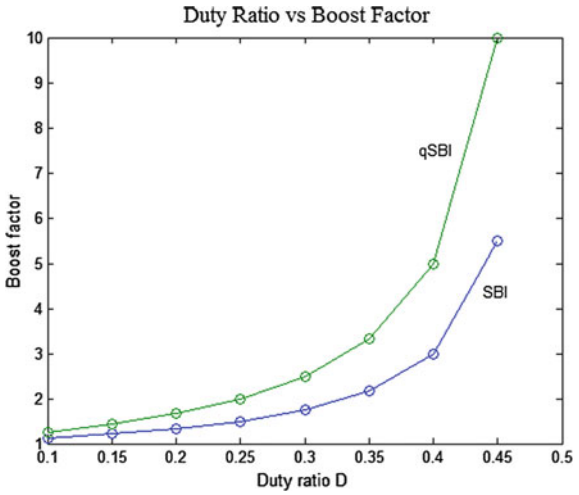

Fig. 77.11 Comparison between boost factor and duty ratio

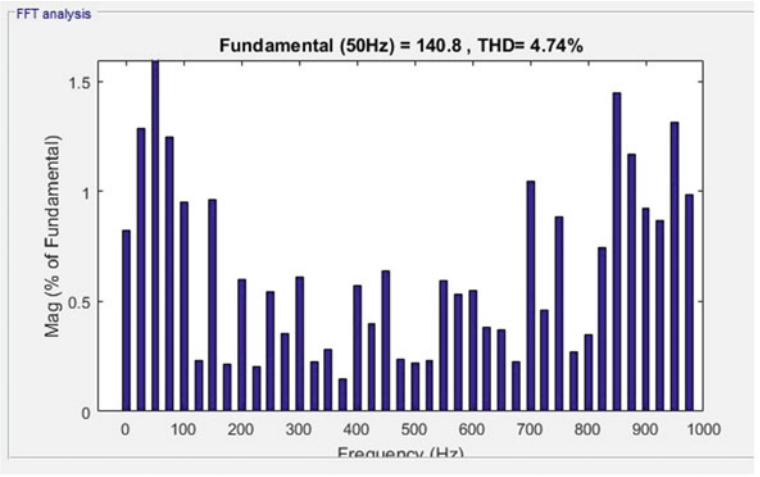

Fig. 77.12 Harmonic profile of load voltage of E-qSBI

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