Performance Analysis of Asymmetrical Cascaded H-Bridge Multilevel Inverter Using Multicarrier Pulse-Width Modulation Techniques

D. Naveen Kumar and P. V. Kishore

Abstract Multilevel inverters are desirable in the earlier years because of their ability to produce waveforms with enhanced harmonic spectrum and realize necessary voltage. The significant benefits of multilevel inverters are reasonable cost, good performance, lower EMI and less harmonic content. The most prevalent multilevel inverter topologies are diode-clamped, flying capacitor and cascaded H-bridge inverter. Among the multilevel inverters, cascaded H-bridge multilevel inverter has been appealed for middle-level and high-voltage renewable-energy-generating systems such as PV system because of its modular nature. Performance analysis of cascaded multilevel inverter topologies with different DC sources and different carrier-based PWM techniques is presented in this paper.

Keywords Cascaded H-bridge · Level shift · Phase shift and phase disposition

1 Introduction

Multilevel power converters condense more advantages compared to a conventional two-level converter. Multilevel inverters have engaged a foremost role in most systems such as high-rated motor drives, FACTS and renewable energy systems [1–3]. They offer output voltage with low distortion, reduced dv/dt stress, reduced switching frequency and lower peak inverse voltage (PIV) on switches [4–7]. There are chiefly three multilevel converter topologies so-called diode-clamped, flying capacitor [8] and cascaded H-bridge [9]. Cascaded MLIs are customarily used for medium-voltage and larger power requirement applications because of reliability and nature of modularity. Pulse-width modulation techniques are applied to control the gating signals of multilevel inverters so that desired voltage is obtained. The performance analysis of cascaded H-bridge multilevel inverter using carrier-based

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pulse-width modulation is presented in this paper. Without escalating the amount of level, high power can be transferred by using asymmetrical cascaded multilevel inverters [10].

2 Multilevel Inverter

The three most widespread multilevel inverters are as follows: 1. diode-clamped multilevel inverter, 2. flying capacitor multilevel inverter and 3. cascaded H-bridge multilevel inverter.

2.1 Diode-clamped multilevel inverter: The diode-clamped multilevel inverter was projected by Nabae et al. in 1981. This is the extensively used multilevel inverter. If n is the quantity of levels of the output, then the $(n - 1)$ number of capacitors and the $(n - 1)(n - 2)$ quantity of clamping diodes are required. The drawback of diode-clamped multilevel inverter is when the 'n' level increases, then the number of clamping diodes also increases.

2.2 Flying capacitor multilevel inverter: Flying capacitor multilevel inverter is analogous to the diode-clamped, but instead of using diodes for clamping, capacitors are used. For n levels, $(n - 1)$ number of DC-side capacitors and $(n - 1)(n - 2)/2$ number of auxiliary capacitors are used. Here also as the 'n' level increases, the amount of clamping capacitors also increases.

2.3 Cascaded H-bridge multilevel inverter: CHB-MLI consists of series of H-bridges which are supplied by isolated DC sources. For 'n' number of levels, $(n - 1)/2$ numbers of bridges are required. Cascaded H-bridge structure, due to its modularity, can be simply made extensive to higher number of levels. However, this requires isolated DC sources. The conduction losses are more in this inverter.

3 Multicarrier-Based PWM Techniques

Sinusoidal pulse-width modulation is the most popular method of switching the power converters. In this, a reference signal is related to carrier signal to produce the gating signals. To increase the performance of the multilevel inverters, multicarrier pulse-width modulation is implemented. Basically, the vertical shift in the carrier is called as level-shifted PWM, and horizontal shift is called as phase-shift PWM. The proposed model is presented in Fig. 1, and the corresponding switching states of the inverter are presented in Table 1.

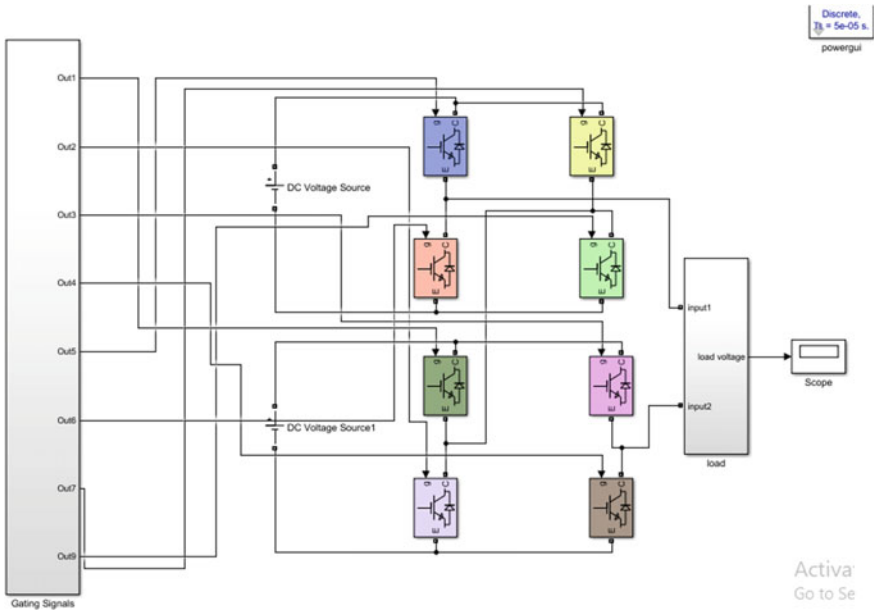

Fig. 1 Proposed Simulink model for cascaded seven-level H-bridge inverter

Table 1 Switching states of the proposed model

Module A output	Module B output	MLI output	Switching states			
			S11	S12	S13	S14
V_{dc}	0	V_{dc}	1	1	0	0
$-V_{dc}$	$2V_{dc}$		0	0	1	1
0	$2V_{dc}$	$2V_{dc}$	0	0	0	0
V_{dc}	$2V_{dc}$	$3V_{dc}$	1	1	0	0
$-V_{dc}$	0	$-V_{dc}$	0	0	1	1
$-V_{dc}$	$-2V_{dc}$	$-3V_{dc}$	0	0	1	1
0	$-2V_{dc}$	$-2V_{dc}$	0	0	0	0
0	0	0	0	0	0	0

3.1 Level-Shifted PWM Technique

In level-shifted PWM, the gating signals are created by the comparison of $(n - 1)$ number of carrier signals with the sinusoidal reference signal. The gating signals are given to the IGBTs in sequence, so that multilevel output is obtained. Level-shifted PWM techniques are classified as follows: 1. PD technique, 2. POD technique and 3. APOD technique.

3.2 Phase-Shifting PWM Technique

In phase-shifting PWM, the carrier signals are having equal peak-to-peak amplitude with same frequency but are phase-shifted by an angle.

Simulink model of seven-level cascaded H-bridge inverter is shown in Fig. 1 which needs six carrier signals, and the frequency of output waveform is determined by the reference signal waveform.

The output voltage and the FFT analysis for different modulation strategies are given below.

3.3 Phase Disposition-PWM

In phase disposition technique, the six carrier signals are in phase, whereas in level, they are shifted with same peak-to-peak amplitude. The PWM signals are shown in Fig. 2.

The output waveform of the load voltage is shown in Fig. 3.

The FFT analysis of the output waveform shown in Fig. 4 indicates the complete harmonic distortion of the output waveform.

3.4 Phase Opposition Disposition-PWM

In phase opposition disposition technique, the carrier signals below zero are 180° in phase opposite to the carrier signals above zero maintaining the same peak-to-peak amplitude as shown in Fig. 5.

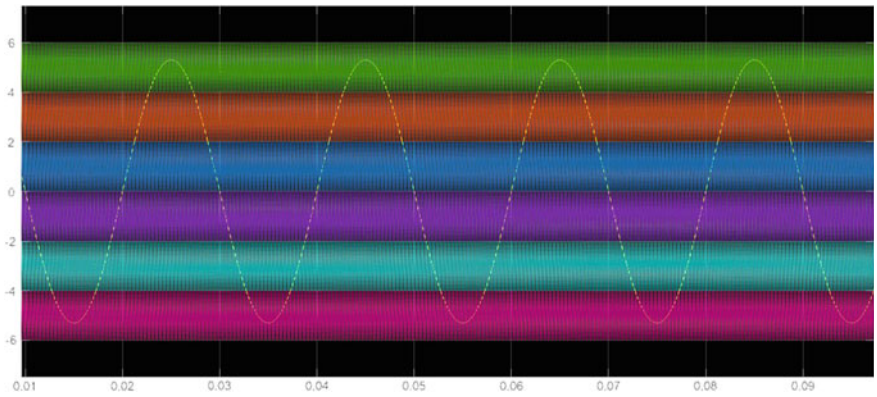

Fig. 2 Gating signals using PD-PWM

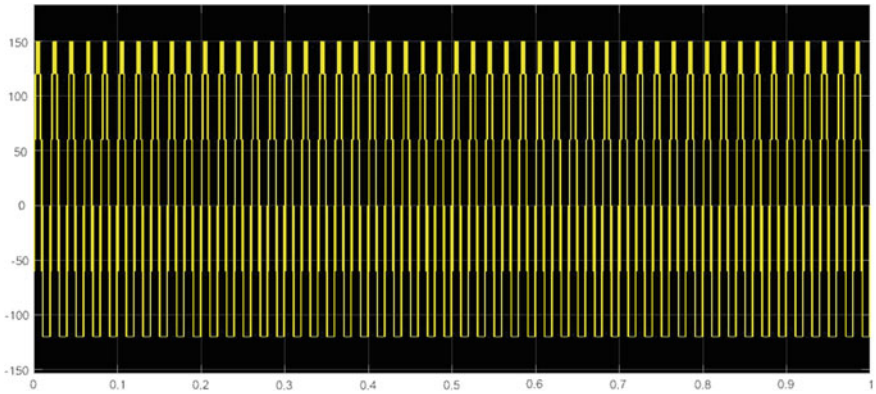

Fig. 3 Load-voltage waveform using PD-PWM

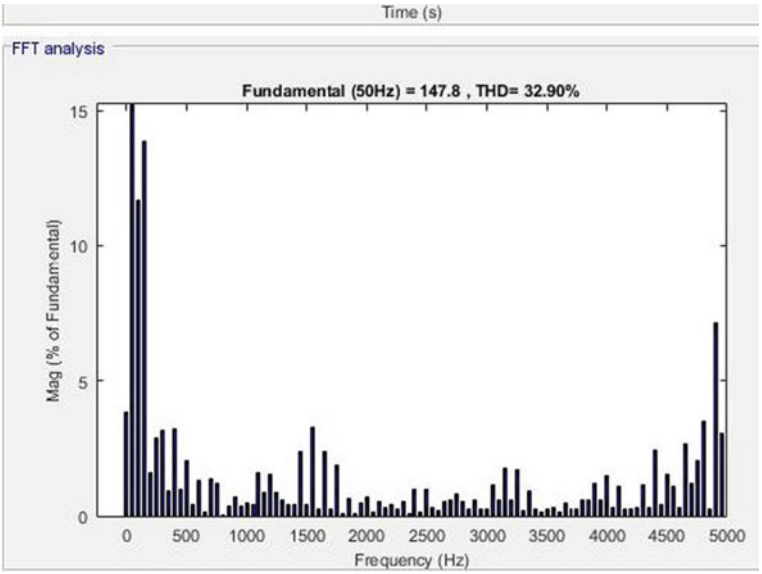

Fig. 4 PD-PWM load-voltage FFT

The output waveform of the load voltage using POD is shown in Fig. 6.

The FFT analysis of the output waveform indicates the total harmonic distortion of the output waveform as shown in Fig. 7 which displays the harmonic content in the load voltage.

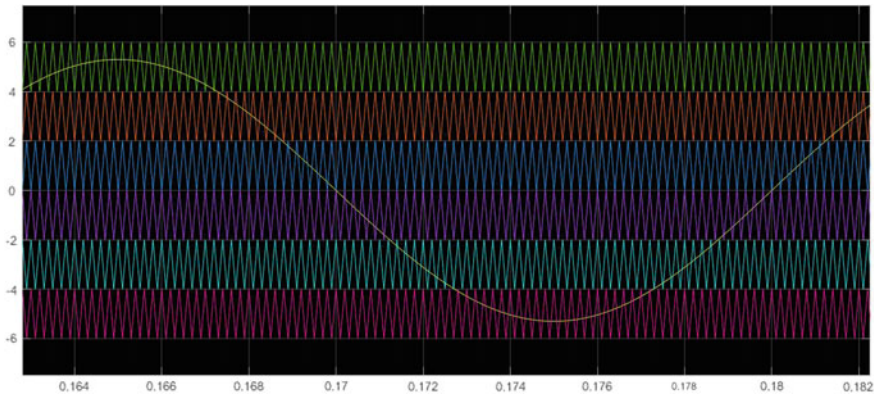

Fig. 5 Gating signals using POD-PWM

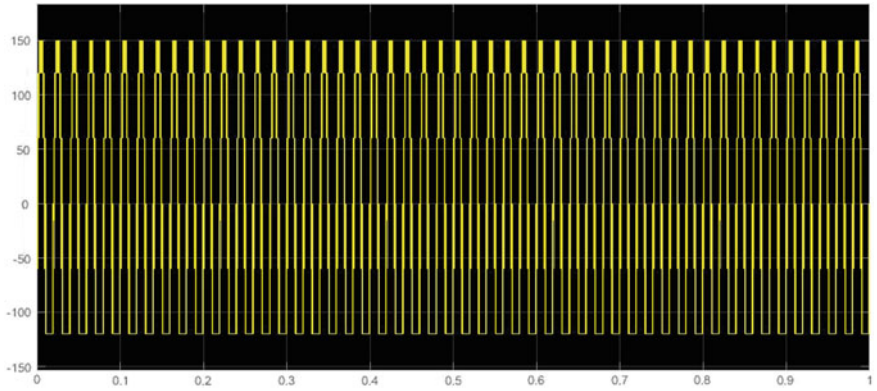

Fig. 6 Load-voltage waveform using POD-PWM

3.5 Alternate Phase Opposition Disposition-PWM

In alternate phase opposition disposition technique, among the six carrier signals, three are adjacent to each other 180° apart (Fig. 8).

The output waveform of the load voltage is shown in Fig. 9.

The FFT analysis of the output waveform as shown in Fig. 10 indicates the total harmonic distortion of the output waveform.

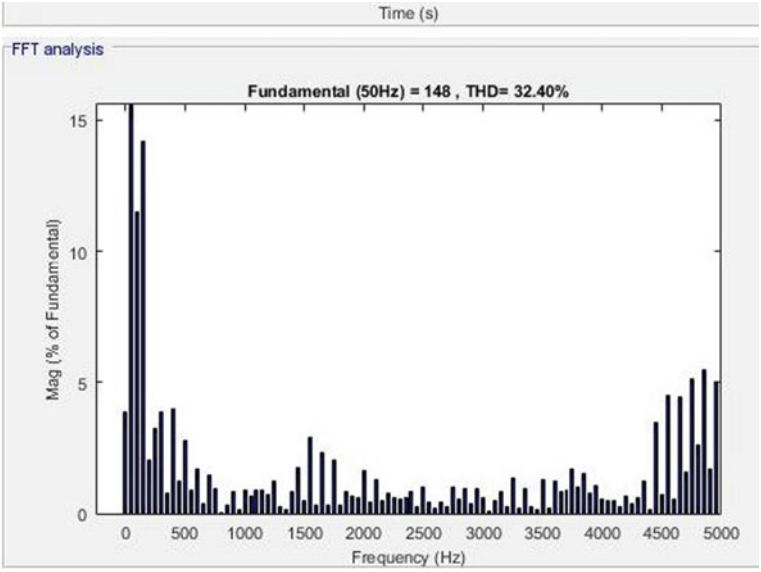

Fig. 7 POD-PWM load-voltage FFT

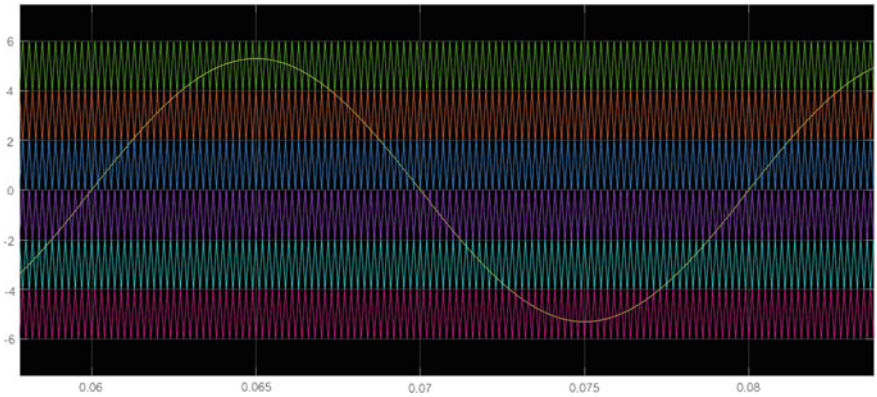

Fig. 8 Gating signals using APOD-PWM

4 Conclusion

In this paper, a seven-level cascaded H-bridge inverter supplied by asymmetrical DC sources is simulated through advanced multicarrier PWM techniques. Comparison has been performed with regard to the total harmonic distortion in the

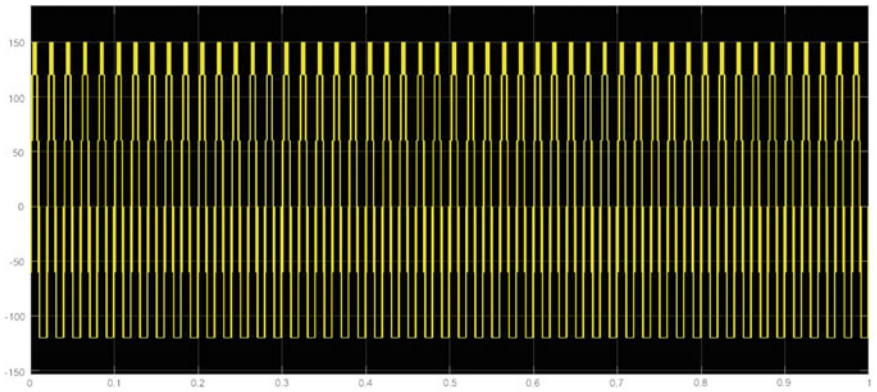

Fig. 9 Load-voltage waveform using APOD-PWM

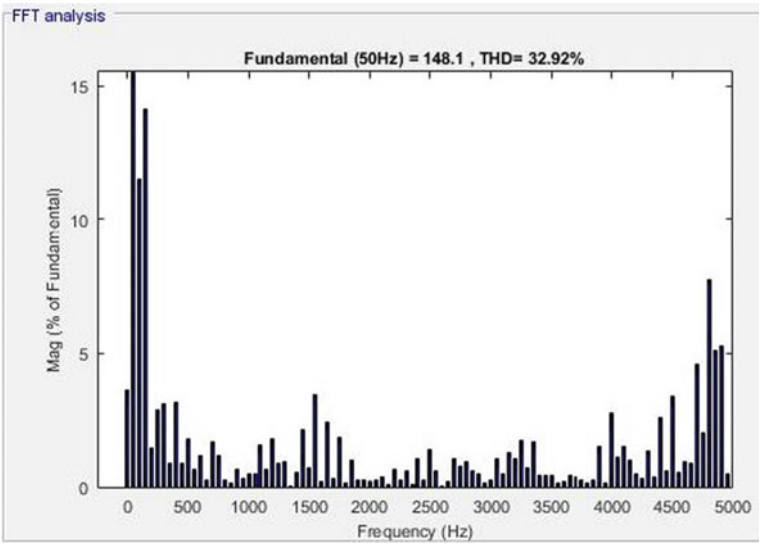

Fig. 10 APOD-PWM load-voltage FFT

output voltage waveform. Among all the multicarrier PWM techniques, phase opposition disposition technique is superior in terms of less harmonic content and smoother load voltage.

References

1. J.S. Lai, F.Z. Peng, Multilevel converters—a new breed of power converters. IEEE Trans. Ind. **32**(3), 509–517 (1996)
2. P. Lezana, J. Rodriguez, D.A. Oyarzun, Cascaded multilevel inverter with regeneration capability and reduced number of switches. IEEE Trans. Ind. Electron. **55**(3), 1059–1066 (2008)
3. P. Panagis, F. Stergiopolos, P. Marabeas, S. Manios, Comparison of state of the art multilevel inverters, in *Proceeding power electronics specialist's Conference PESC 2008*. (IEEE, 2008), pp. 4296–301
4. T.A. Meynard, H. Foch, F. Forest, et al. Multicell converters: derived topologies. IEEE Trans. Ind. Electron. **49**(5), 978–87 (2002)
5. Z. Du, L.M. Tolbert, B. Ozpineci, J.N. Chiasson, Fundamental frequency switching strategies of a seven-level hybrid cascaded H-bridge multilevel inverter. IEEE Trans. Power Electron. **24**(1), 25–33 (2009)
6. K.A. Corzine, Y.L. Familiant, A new cascaded multilevel H-bridge drive. IEEE Trans. Power Electron. **17**, 125–131 (2002)
7. E. Babaei, S.H. Hosseini, G.B. Gharehpetian, M. Tarafdar Haque, M. Sabahi, Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology. Electr. Power Syst. Res. **77**, 1073–1085 (2007)
8. J. Rodriguez, J.S. Lai, F.Z. Peng, Multilevel inverter: a survey of topologies, controls, and applications. IEEE Trans. Ind. Electron. **49**(4), 724–738 (2002)
9. E. Barcenas, S. Ramirez, V. Cardenas, Echavarria, Cascaded multilevel inverter with only one dc source. in *Proceeding VIII IEEE Inttech Proceeding CIEP* (2002), pp. 171–176
10. K.S. Chandra Gupta Mauryan, G. Sivagnanam, R. Purrnimaa Siva Sakthi, Design of nine level diode clamped multilevel inverter. J. Emerg. Technol. Innov. Res. **6**(1), 513–518 (2019)