Design of Five-Level Cascaded H-Bridge Multilevel Inverter

S. Swathy, N. Niveditha and K. S. Chandragupta Mauryan

Abstract The abstract of this paper is to design a five-level cascaded H-bridge multilevel inverter using phase disposition pulse width modulation (PD-PWM) technique, to obtain optimal switching angles for harmonic reduction and to compare the THD content of the output waveform of the five-level cascaded H-bridge multilevel inverter for different modulation index by using mathematical approach and MATLAB/SIMULINK.

Keywords Multilevel inverter · Modulation techniques · Selective harmonic elimination · Total harmonic distortion · FPGA

1 Introduction

Demand for energy is getting increased day by day. The key source of energy available now is from non-renewable sources like fossil fuels. The over utilization of these sources to meet our daily requirements have put it in a degradation state [1, 2]. Hence, there is a rapid development in the research to produce energy from alternate sources, such as wind, solar, tidal, etc. Among them, energy taken from photovoltaic systems plays an important role. The energy which is taken from a photovoltaic system (PV system) is DC in nature. Most of the equipments are used for domestic and industrial purposes which work on an AC source, the DC output from a PV system is converted into an AC and for this purpose, power inverters play a major role.

S. Swathy (✉) · N. Niveditha
Department of Electrical and Electronics Engineering, Karpagam College of Engineering, Coimbatore, Tamil Nadu, India

K. S. Chandragupta Mauryan
Department of Electrical and Electronics Engineering, Guru Nanak Institution Technical Campus, Hyderabad, Telangana, India

H. S. Saini et al. (eds.), *Innovations in Electrical and Electronics Engineering*,
Lecture Notes in Electrical Engineering 626,
https://doi.org/10.1007/978-981-15-2256-7_7

2 Multilevel Inverter Concepts

Multilevel inverters concept attracts academia as well as industry over wide range. They combine switched waveforms with lower levels of harmonic distortion than an equivalently rated two-level converter [1–3]. It found that with the increase in level, the steps increases and the output waveform approaches to a near sinusoidal waveform. Thus, it reduces the THD with a disadvantage of complex control and voltage imbalance problem. They are employed mainly for high-power, high-voltage/medium-power applications. They create more switching states, thereby stepping up output inverter voltages in small increments. These smaller voltage steps help in creating high-quality waveforms, lower dv/dt and reduced electromagnetic compatibility. But in order to increase the number of levels, more number of components are required and same will make the circuit complex [2]. High switching frequency employed in multilevel inverters helps in minimizing the output harmonics and reducing the passive component size in the power circuit. Figure 1 shows different number of voltage-level output waveform of MLI.

There are also different topologies of multilevel inverters that generate a stepped output voltage waveform and that are suitable for different applications. By designing multilevel circuits in different ways, many topologies with properties have been developed. The basic multilevel inverter topologies include: Diode-clamped multilevel inverter, capacitor-clamped multilevel inverter, cascaded H-bridge (CHB) multilevel inverter.

2.1 Cascaded H-Bridge Multilevel Inverter (CHB-MLI)

The concept of multilevel inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. Figure 2 shows a full-bridge inverter. One full-bridge is itself a three-level cascaded H-bridge multilevel inverter and every module added in cascade which extends the inverter with two voltage levels. Each full-bridge inverter can create three voltages V_{DC}, 0 and $-V_{DC}$. To change one level of voltage cascaded H-bridge multilevel inverter turns one switch ON and other switch OFF in one full-bridge inverter. For example, to achieve voltage $+V_{dc,}$

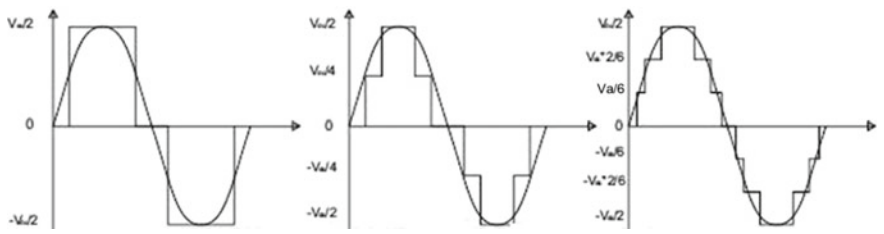

Fig. 1 3, 5, 7 level output waveform of multilevel inverter at fundamental frequency

switches S_1 and S_2 are turned ON, for $-V_{dc}$, the switches S_3 and S_4 are turned OFF. When there is no current following through the full-bridge, then 0 voltage level is achieved [3, 4].

The output voltage in each bridge is the summation of the voltage that is generated by each cell. The number of output voltage levels are $2n + 1$, where n is the number of cells. The cascaded H-bridge multilevel inverter is capable of producing the total voltage source magnitude in both positive and negative half cycles, while many other topologies can only produce half the total DC-bus voltage source magnitude. Full-bridge inverter that is connected in series can contribute with the same voltage, thus meets topology. There is possibility to charge every module in a cascaded H-bridge multilevel inverter with different voltages.

In Fig. 3, there are two full-bridge inverters connected in series for obtaining five different output voltage levels, $-2V_{DC}$, V_{DC}, 0 $-V_{DC}$ and $+2V_{dc}$. The advantages of this type of multilevel inverter are that it needs less number of components comparative to the diode clamped or the flying capacitor. However, the number of sources is higher, for the phase-leg to be able to create a number if m voltage level and switches $2 * (m - 1)$ [1, 2, 4].

3 Modulation Techniques for Multilevel Inverter

Multilevel inverters have different modulation techniques for obtaining a better output voltage response with minimum harmonic distortions. There are basically two groups of methods: modulation with fundamental switching frequency or high switching frequency pulse width modulation (PWM) [5–11].

3.1 Pulse Width Modulation Techniques

A multilevel pulse width modulation method uses high switching frequency carrier waves in comparison to the reference waves to generate a sinusoidal output wave as

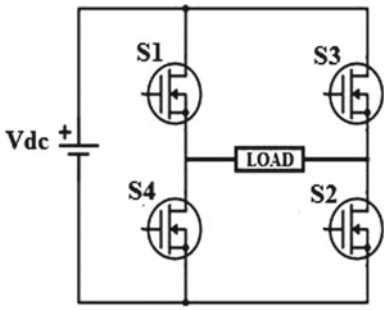

Fig. 2 Single-phase full-bridge inverter

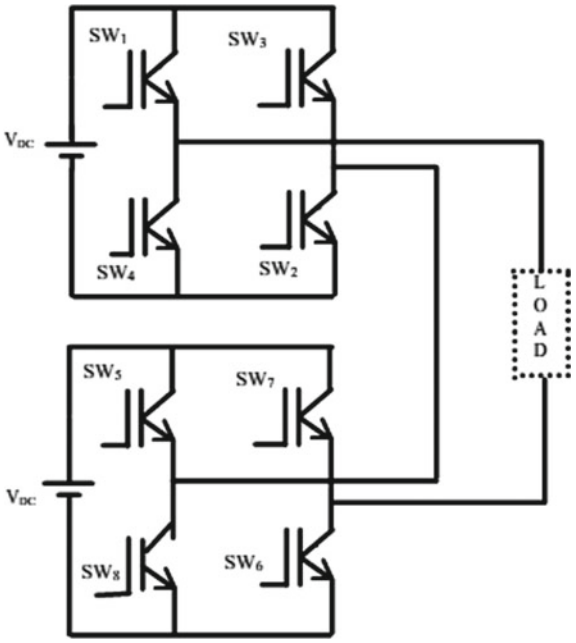

Fig. 3 Single-phase five-level multilevel inverter

such in the two-level PWM case. To reduce harmonic distortions in the output voltage waveform, phase-shifting techniques are used [12–20].

The carrier-based pulse width modulation techniques can be broadly classified into:

- Phase-shifted modulation
- Level-shifted modulation.

In both modulation techniques, for an m-level inverter, (m-1) triangular carrier waves are required and all the carrier waves should have the same frequency and same peak-to-peak magnitude.

Phase Disposition Pulse Width Modulation: In phase disposition modulation technique, all the triangular carriers are in phase and are arranged one over the other as shown in Fig. 4. These arranged triangular carriers are compared with reference wave to obtain the pulses for the multilevel inverter switches. This technique is generally accepted as the method that creates the lowest harmonic distortion in line-to-line voltage.

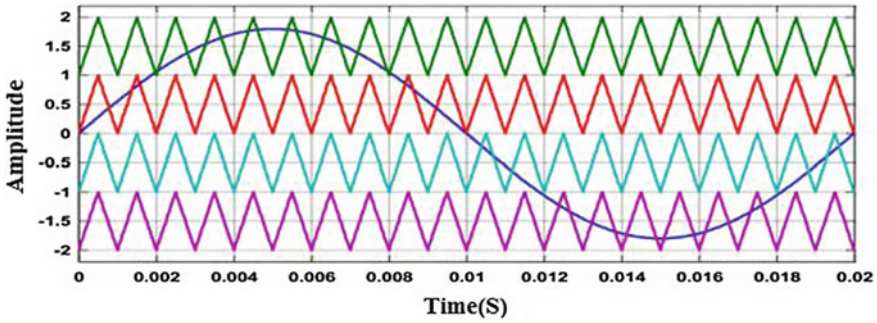

Fig. 4 Reference and carrier wave for a five-level cascaded H-bridge multilevel inverter with PD-PWM

4 Operating Modes of Five-Level Cascaded H-Bridge Multilevel Inverter

Mode1: +2V$_{dc}$: Figure 5 shows the operating mode for getting output voltage of $+2V_{dc}$. In this mode, switches SW_1, SW_2, SW_5 and SW_6 are ON and all the other switches SW_3, SW_4, SW_7 and SW_8 are OFF.

Mode2: +V_{dc}: Figure 6 shows the operating mode for getting output voltage of $+V_{dc}$. In this mode, switches SW_1, SW_2, SW_8 and SW_6 are ON and all the other switches SW_3, SW_4, SW_7 and SW_5 are OFF.

Mode3: 0: Figure 7 shows the operating mode for getting output voltage of zero. The lower-leg switches are triggered; hence, there will no flow of current in the power circuit.

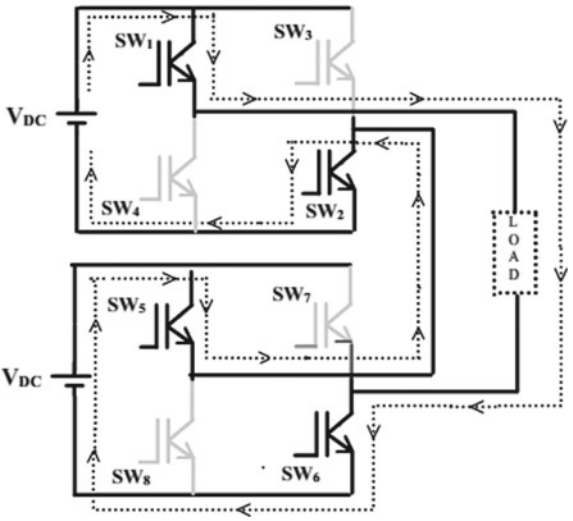

Fig. 5 Operating mode for getting output voltage of $+2V_{dc}$

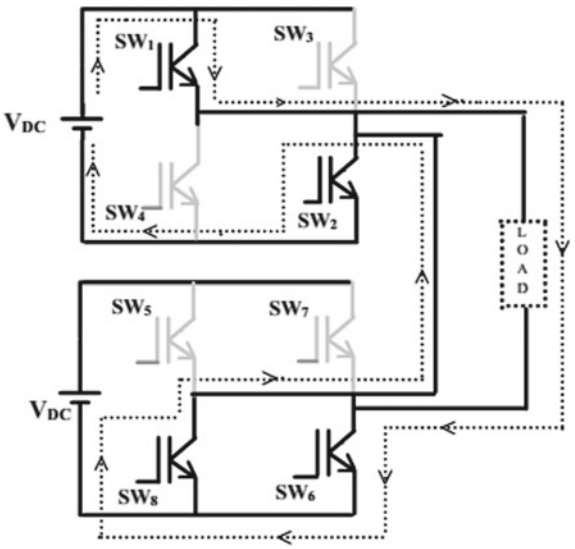

Fig. 6 Operating mode for getting output voltage of $+V_{dc}$

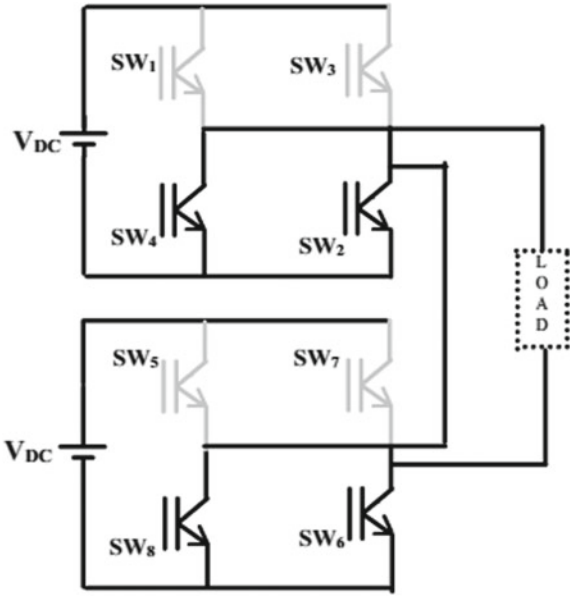

Fig. 7 Operating mode for getting output voltage of zero

Mode4: $-V_{dc}$: Figure 8 shows the operating mode for getting output voltage of $-V_{dc}$. In this mode, switches SW_3, SW_4, SW_8 and SW_6 are ON and all the other switches SW_1, SW_2, SW_7 and SW_5 are OFF. The flow of current is opposite to the load current.

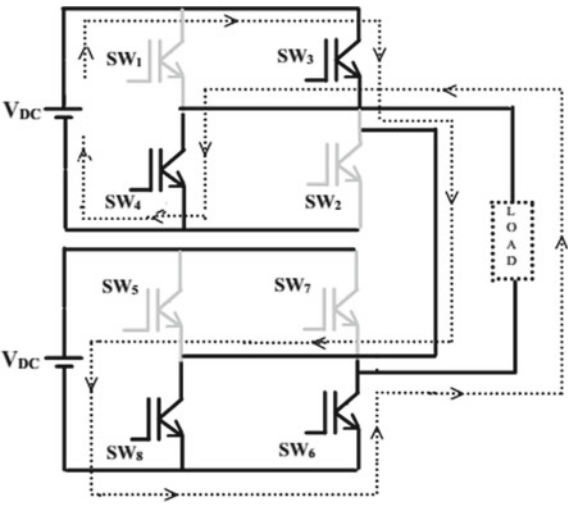

Fig. 8 Operating mode for getting output voltage of $-V_{dc}$

Mode5: -2V$_{dc}$: Figure 9 shows the operating mode for getting output voltage of $-2V_{dc}$. In this mode, switches SW_3, SW_4, SW_8 and SW_7 are ON and all the other switches SW_1, SW_2, SW_6 and SW_5 are OFF. The flow of current is opposite to the load current.

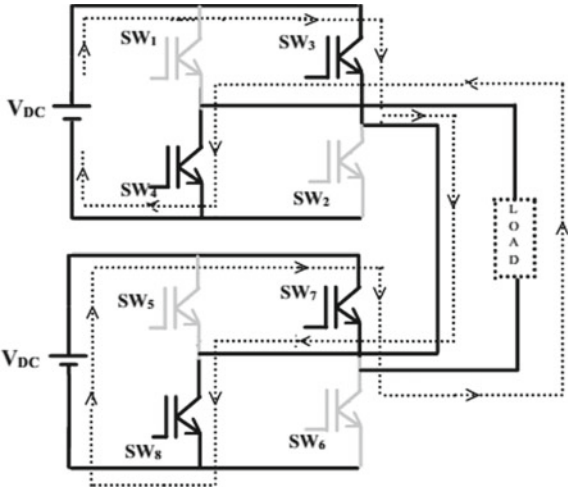

Fig. 9 Operating mode for getting output voltage of $-2V_{dc}$

5 Fourier Analysis of PD-PWM Technique

The concept of a two-level pulse width modulated converter system is that a low-frequency reference waveform is compared against a high-frequency carrier waveform and the compared output is used to control the switches. The consequence of switching process has fundamental component, the reference waveform and also incorporates a series unwanted harmonics. Determination of harmonic frequency components is complex and it is often done by fast Fourier transform analysis of a simulated time-varying waveform. This approach also reduces mathematical effort but uncertainly, it leaves error. In contrast, an analytical solution which exactly identifies the harmonic component of a PWM waveform ensures that precisely the harmonics are being considered when various PWM strategies are compared against each other [21–27]. Table 1 gives the switching function condition of a five-level multilevel inverter.

$$\begin{aligned} f(t) = & \frac{A_{oo}}{2} + \sum_{n=1}^{\infty}[A_{\text{on}}\cos([n\omega_o t]) + B_{\text{on}}\sin([n\omega_o t])] \\ & + \sum_{m=1}^{\infty}[A_{mo}\cos([n\omega_c t]) + B_{mo}\sin([m\omega_c t])] \\ & + \sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty}[A_{mn}\cos([m\omega_c t + n\omega_o t]) \\ & + B_{mn}\sin([n\omega_c t + n\omega_o t]) \end{aligned}$$

m carrier index variable
n base-band index variable.

The final expression for harmonic components can be obtained by on substituting the equation

Table 1 Switching function condition of a five-level multilevel inverter

$F(x, y)$	When $-\pi \leq x \leq 0$	When $0 < x \leq \pi$
$+2V_{\text{DC}}$	$M\cos y > \frac{1}{2} - \frac{\pi}{2\pi}$	$M\cos y > \frac{1}{2} + \frac{\pi}{2\pi}$
$+V_{\text{DC}}$	$-\frac{\pi}{2\pi} < M\cos y < \frac{1}{2} - \frac{\pi}{2\pi}$	$\frac{\pi}{2\pi} < M\cos y < \frac{1}{2} + \frac{\pi}{2\pi}$
0	$-\frac{1}{2} - \frac{\pi}{2\pi} < M\cos y < -\frac{\pi}{2\pi}$	$-\frac{1}{2} + \frac{\pi}{2\pi} < M\cos y < \frac{\pi}{2\pi}$
$-V_{\text{DC}}$	$-1 - \frac{\pi}{2\pi} < M\cos y < -\frac{1}{2} - \frac{\pi}{2\pi}$	$-1 + \frac{\pi}{2\pi} < M\cos y < -\frac{1}{2} + \frac{\pi}{2\pi}$
$-2V_{\text{DC}}$	$M\cos y < -1 - \frac{\pi}{2\pi}$	$M\cos y < -1 + \frac{\pi}{2\pi}$

$$
\begin{aligned}
V_{az}(t) = {} & 2MV_{dc}\cos\omega_0 t + \frac{8V_{dc}}{\pi^2}\sum_{m=1}^{\infty}\frac{1}{2m-1}\sum_{k=1}^{\infty}\frac{1}{2k-1}J_{2k-1}([2m-1]2\pi M) \\
& * \{1 + 2\sin([2k-1]\varphi\cos k\pi\} * \cos([2m-1]\omega_c t) \\
& + \frac{2V_{dc}}{\pi}\sum_{m=1}^{\infty}\frac{1}{2m}\sum_{n=-\infty}^{\infty}J_{2n+1}(4m\pi M)\cos n\pi\cos(2m\omega_c t + [2n+1]\omega_0 t) \\
& + \frac{4V_{dc}}{\pi^2}\sum_{m=1}^{\infty}\frac{1}{2m-1}\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty}\sum_{k=1}^{\infty}[J_{2k-1}([2m-1]2\pi M)\cos k\pi \\
& * \left\{\frac{\cos([n-k]\pi) + 2\sin([2k-1-2n]\varphi)}{[2k-1-2n]} + \frac{\cos([n-k]\pi) + 2\sin([2k-1+2n]\varphi)}{[2k-1+2n]}\right\}\Bigg] \\
& * \cos([2m-1]\omega_c t + 2n\omega_0 t)
\end{aligned}
$$

6 Simulation Results of Cascaded H-Bridge Multilevel Inverter Using PD-PWM Technique

The simulation is carried out using MATLAB/SIMULINK software. The simulation diagram is shown in Fig. 10.

Table 2 gives the design parameters for cascaded H-bridge multilevel inverter. Figure 11 shows the output voltage and output current of five-level cascaded H-bridge multilevel inverter for switching frequency of 2 kHz M = 1 and Fig. 12

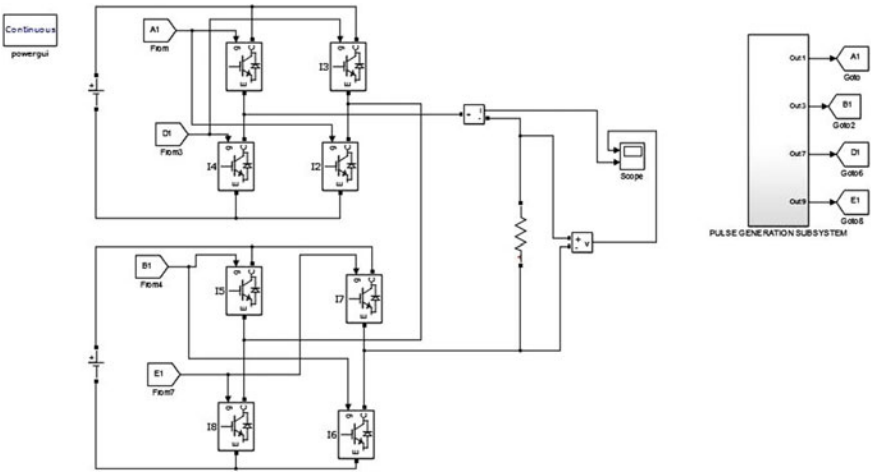

Fig. 10 Simulation diagram of cascaded H-bridge multilevel inverter using PD-PWM technique

Table 2 Design parameters for cascaded H-bridge multilevel inverter

S. No.	Parameter	Five-level cascaded H-bridge inverter
1	Input voltage	130 V
2	Load	$R = 50\ \Omega$
3	Switching frequency	1 and 2 kHz
4	Modulation index	0.8 and 1

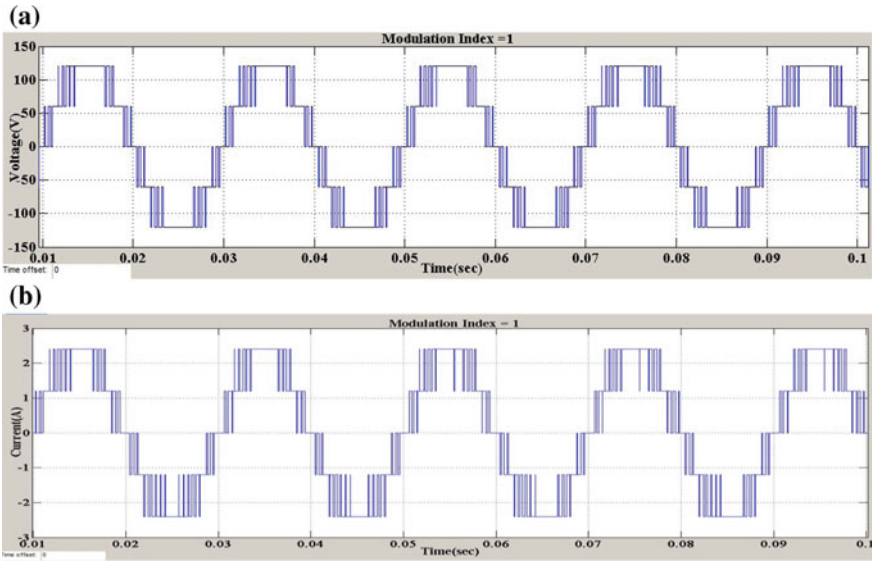

Fig. 11 **a** Output voltage and **b** Output current of five-level cascaded H-bridge multilevel inverter for switching frequency of 2 kHz M = 1

shows the harmonic spectrum of output current of five-level cascaded H-bridge multilevel inverter for the switching frequency of 2kH and modulation index, $M = 0.8$ and $M = 1$.

Comparison of THD values for modulation index 0.8 and 1 and switching frequencies of 1 kHz and 2 kHz are given in Table 3. Also the Comparison of THD for PDPWM and SHE technique is for 0.8 and 1 modulation index and 1 and 2 kHz switching frequencies is given in Table 4.

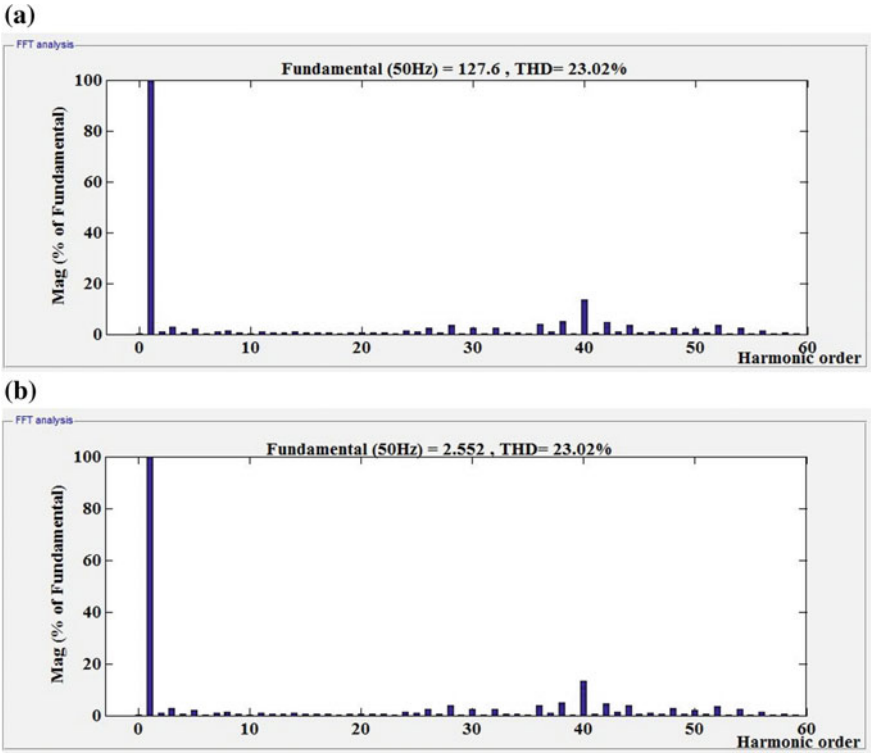

Fig. 12 Harmonic spectrum of output current of five-level cascaded H-bridge multilevel inverter (2 kHz) **a** $M = 0.8$ **b** $M = 1$

Table 3 Comparison of THD for various modulation index and switching frequencies

Parameter	Switching frequency (1 kHz)		Switching frequency (2 kHz)	
	Modulation index		Modulation Index	
	0.8	1	0.8	1
Voltage (%THD)	38.07	26.64	36.74	23.02
Current (%THD)	38.07	26.64	36.74	23.02

Table 4 Comparison of THD for PD-PWM and SHE techniques

Total harmonic elimination	PD-PWM	SHE		
		Third harmonic elimination	Fifth harmonic elimination	Seventh harmonic elimination
%THD for voltage	26.64	18.54	23.38	22.59
%THD for current	26.64	18.54	23.38	22.59

7 Hardware Implementation

FPGA Kit

The control signal for the power switches of a five-level cascaded H-bridge multilevel inverter is developed with the help of SPARTAN 6-XC6SLX25 trainer kit. Figure 13 shows the schematic of SPARTAN 6 FPGA kit.

Design specification for hardware implementation of a five-level cascaded H-bridge multilevel inverter is given in Table 5. Output voltage and output current for switching frequency of 1 kHz and modulation index of 0.8 are shown in Fig. 14a and b. Also the FFT of output voltage and current for switching frequency of 1 kHz and modulation index of 0.8 is shown in Fig. 15a, b.

The harmonic spectrum with R-Load for switching frequency of 1 kHz and modulation index of 0.8 is shown in Fig. 16 for output voltage, current and power. The comparison of different modulation indices and switching frequency is given in Table 6.

Fig. 13 SPARTAN 6-FPGA kit

Table 5 Design specification for hardware implementation of a five-level cascaded H-bridge multilevel inverter

S. No.	Parameters	Specification
1	Input voltage	130 V
2	Load	50 Ω
3	Switching frequency (f_s)	1 and 2 kHz
4	Voltage and current measurement	Digital storage oscilloscope
5	Harmonic measurement	Fluke 43B

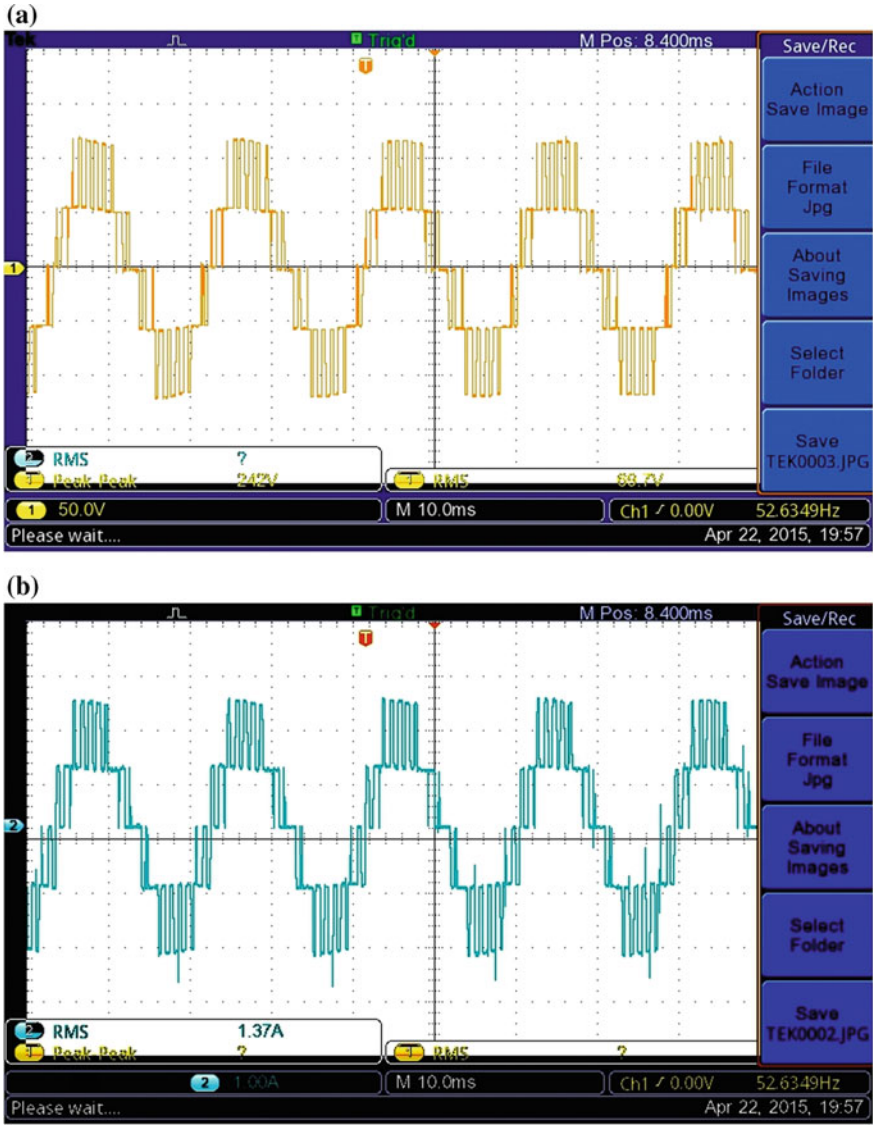

Fig. 14 **a** Output voltage and **b** Output current of five-level cascaded H-bridge multilevel inverter

8 Conclusion

In this work, a single-phase five-level cascaded H-bridge multilevel inverter is studied and analyzed in terms of output voltage, output current and harmonic spectrum. Phase disposition PWM modulation technique is used to generate

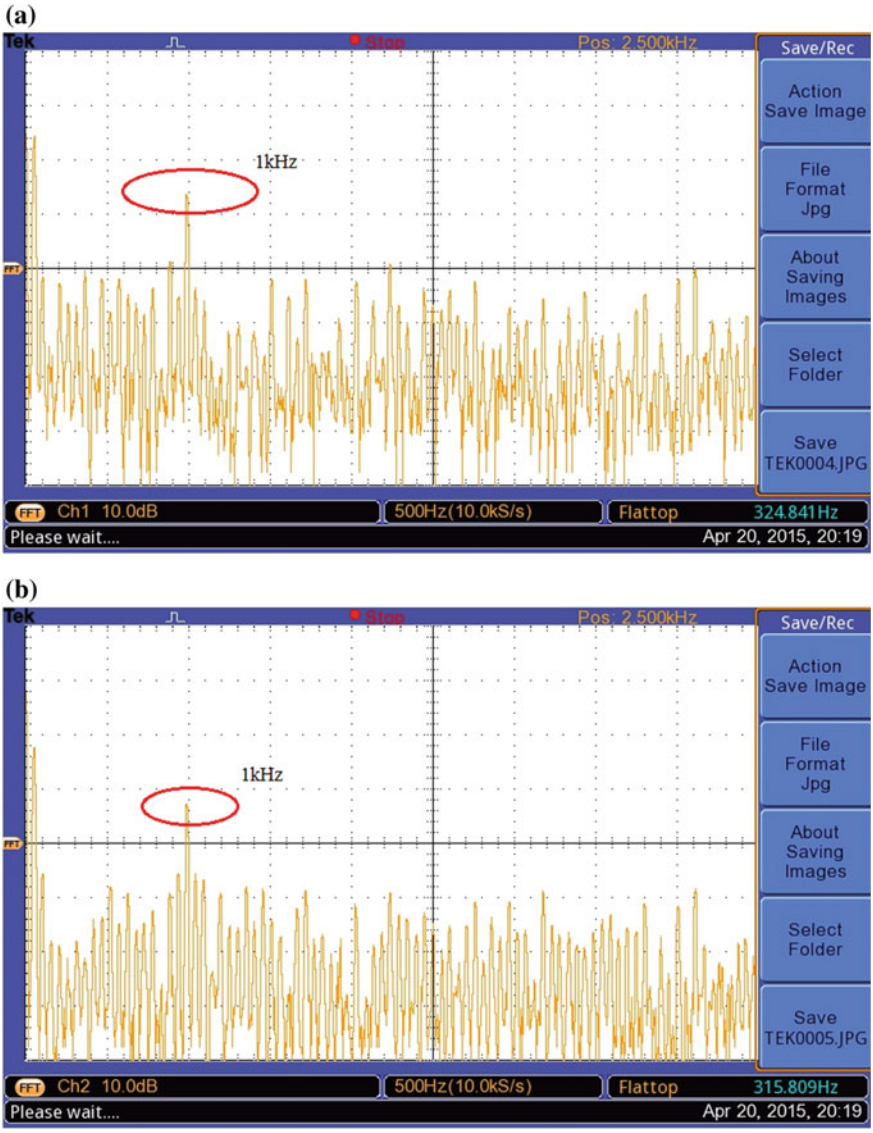

Fig. 15 FFT of **a** Output voltage and **b** Output current

switching pulses for the inverter. Further, optimal switching angles for the inverter are calculated for harmonic reduction (third harmonic, fifth harmonic and seventh harmonic). Results are verified using simulation done in MATLAB/SIMULINK. The five-level cascaded H-bridge multilevel inverter is implemented as a hardware prototype. The pulses for cascaded H-bridge multilevel inverter are generated using Spartan-6 XC6SLX25 FPGA kit. A comparison of the output THD with

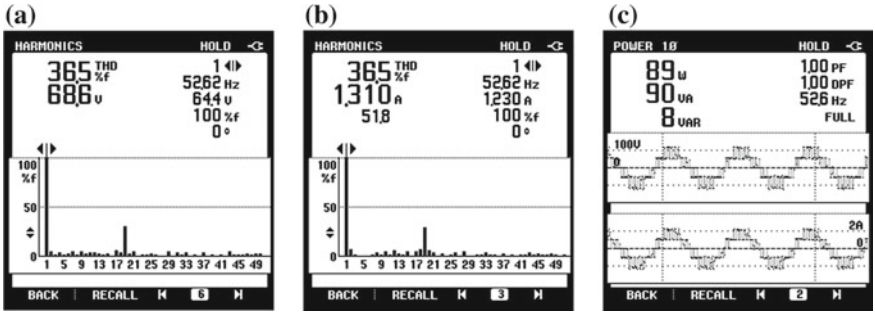

Fig. 16 Harmonic spectrum of **a** Output voltage, **b** Output current and **c** Power

Table 6 Comparison of different modulation indices and switching frequency

Parameters	Switching frequency (1 kHz)		Switching frequency (2 kHz)	
	Modulation index		Modulation index	
	0.8	1	0.8	1
Voltage (%THD)	36.5	26.5	33.2	21.1
Current (%THD)	36.5	26.5	32.9	21.2
Power (W)	89	144	93	134

modulation index of 0.8 and 1, and switching frequencies 1 and 2 kHz is carried out. As a future scope, multilevel inverter can be analyzed for different output levels by changing modulation index and switching frequency. By designing suitable filters, the total harmonic distortion can further be reduced on the output, to meet IEEE harmonic standards.

References

1. A.R. Beig, R.Y. Udaya Kumar, V.T. Ranganathan, A novel fifteen level inverter for photovoltaic power supply system, in *Industry Applications Conference, 39th IAS Annual Meeting*, vol. 2. (2004), pp. 1165–1171
2. J. Rodriguez, J.-S. Lai, Multilevel inverters: a survey of topologies, controls, and applications. Ind. Electron. IEEE Trans. **49**(4), 724–738 (2002)
3. M.H. Rashid, *Power Electronics Circuits, Devices, and Applications*, 3rd edn. (Pearson Prentice Hall, 2004)
4. P. Palanivel, S.S. Dash, Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques. IET Power Electron. **4**(8), 951–958 (2011)
5. A.K. Panda, Y. Suresh, Research on cascaded multilevel inverter with single DC source by using three-phase transformers. Electr. Power Energy Syst. 409–420 (2012)
6. Y. Suresh, A.K. Panda, Research on a cascaded multilevel inverter by employing three-phase transformers. IET Power Electron. **5**(5), 561–570 (2012)

7. J. Wang, D. Ahmadi, A precise and practical harmonic elimination method for multilevel inverters. IEEE Trans. Ind. Appl. **46**(2) (2010)
8. Y. Suresh, A.K. Panda, Research on cascaded multilevel inverter with reduced dc sources. Renew. Sustain. Energy Rev. 2649–2659 (2013)
9. R. González, J. López, L. Marroyo, Transformerless single-phase multilevel-based photovoltaic inverter. IEEE Trans. Ind. Electron. **55**(7) (2008)
10. E. Villanueva, P. Correa, Control of a single phase cascade H-Bridge multilevel inverter for grid-connected photovoltaic systems. IEEE Trans. Ind. Electron. **56**(11) (2009)
11. S. Daher, J. Schmid, F.L. Antunes, Multilevel inverter topologies for stand-alone PV systems. IEEE Trans. Ind. Electron. **55**(7) (2008)
12. P. Roshankumar, L.G. Franquelo, A five level inverter topology with single-DC supply by cascading a flying capacitor inverter and an H-Bridge. IEEE Trans. Power Electron. **27**(8) (2012)
13. N. Bodo, E. Levi, M. Jones, Investigation of carrier-based, pwm techniques for a five-phase open-end winding drive topology. IEEE Trans. Ind. Electron. **60**(5) (2013)
14. S. Mariethoz, Systematic design of high-performance hybrid cascaded multilevel inverters with active voltage balance and minimum switching losses. IEEE Trans. Power Electron. **28** (7) (2013)
15. Z. Pan, F.Z. Peng, A sinusoidal PWM method with voltage balancing capability for diode-clamped five-level converters. IEEE Trans. Ind. Appl. **45**(3) (2009)
16. A. Nasrudin Rahim, K. Chaniago, J. Selvaraj, Single-phase seven-level grid-connected inverter for photovoltaic system. IEEE Trans. Ind. Electron. **58**(6) (2011)
17. W. Bin, *High Power Converters and AC Drives*. IEEE Press, Wiley-Interscience, A John Wiley and Sons Inc., Publications (2006)
18. T.A. Meynard, H. Foch, Multilevel conversion: high voltage choppers and voltage source inverters, in *Proceeding IEEE PESC* (1992), pp. 397–403
19. S.H. Hosseini, M. Ahmadi, S. Ghassem Zadeh, Reducing the output harmonics of cascaded H-bridge multilevel inverter for electric vehicle applications, in *8th International Conference on Electrical Engineering/ Electronics, Computer Telecommunications and Information Technology (ECTI-CON 2011)* (Thailand, 2011), pp. 752–755
20. Y. Huang, J. Wang, A universal selective harmonic elimination method for high-power inverters. IEEE Trans. Power Electron. **26**(10), 2743–2752 (2011)
21. G. Holmes, T.A. Lipo, Pulse width modulation for power converters (2003)
22. A.R. Beig, A. Dekka, Experimental verification of multilevel inverter-based standalone power supply for low-voltage and low-power applications. IET Power Electron. **5**(6), 635–643 (2012)
23. D.W. Kang, S. Hyun, Simple harmonic analysis method for multi-carrier PWM techniques using output phase voltage in multi-level inverter. IEEE Proc. Electron. Power Appl. **152**(2) (2005)
24. K.K. Gupta, S. Jain, Topology for multilevel inverters to attain maximum number of levels from given DC sources. IET Power Electron. **15**(4), 435–446 (2012)
25. D.W. Kang, J. Rodríguez, Direct torque control with imposed switching frequency in an 11-level cascaded inverter. IEEE Trans. Ind. Electron. **51**(4) (2004)
26. F. Wanmin, W. Bin, A Generalized and formulation of quarter wave symmetry SHE-PWM problems for multilevel inverters. IEEE Trans. Power Electron. **24**(7) (2009)
27. R. Gupta, A. Joshi, Multiband hysteresis modulation and switching characterization for sliding-mode-controlled cascaded multilevel inverter. IEEE Trans. Ind. Electron. **57**(7) (2010)