Analysis and Design of Extended Range Zero Voltage Switching (ZVS) Active-Clamping Current-Fed Push–Pull Converter

Koyelia Khatun and Akshay Kumar Rathore

Abstract This paper proposes extended soft-switched active-clamped type current-fed isolated push–pull voltage DC–DC converter. Proposed topology retains soft-switching for extended operating range. Steady-state analysis and simulation results are demonstrated. The turn-off voltage spike is eliminated. The higher load voltage is achieved with the help of voltage doubler on the load side. To validate the proposed analysis, design, and performance evaluation, simulation results are presented.

Keywords Fuel cells · DC–DC power conversion · Soft-switching

1 Introduction

In recent years, developing low-cost, high-efficient and small-size power conversion systems for renewable energy sources is getting more attention, due to environmental aspects and limitation of global energy sources. Fuel cells are popular alternative energy resources as they provide continuous power in all seasons and are not dependent on weather condition unlike solar and wind energy sources.

The proposed paper introduces an extended range soft-switched small-size, lightweight and low-cost converter. The main concern is to maintain soft-switching over the wide operating range of source voltage and load current owing to fuel flow and fuel cell stack temperature.

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H. S. Saini et al. (eds.), *Innovations in Electrical and Electronics Engineering*,
Lecture Notes in Electrical Engineering 626,
https://doi.org/10.1007/978-981-15-2256-7_5

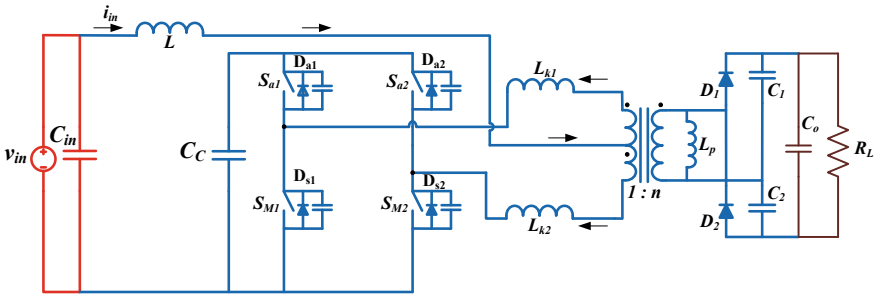

Fig. 1 Active-clamped L–L type pulse width modulated current-fed push-pull DC–DC voltage doubler

Many DC–DC circuits are presented for this application [1–15], but hardly, any of them were able to maintain soft-switching over the complete load and source variation. Converter proposed in [1] is voltage-fed secondary controlled voltage doubler with additional devices and control requirements with high circulating current. Voltage-fed converters with inductive output filter come with variety of problems such as duty cycle loss, secondary resonance, snubber across secondary and limited soft-switching capability. The ZVS is achieved by using many extra components including resonant tank or auxiliary transition circuits making the circuit complex and less efficient. A detailed study of ZVS DC/DC converters is reported in [5]. Majority of the converters lose soft-switching with supply voltage variation. Current-fed half-bridge DC/DC converter topology [4, 6, 7] was justified for such applications requiring high voltage gain. However, hard-switching and switch turn-off voltage spike are the major limitations. An active-clamping [8, 12–15] based solution was proposed, analyzed and designed for device voltage clamping and soft-switching. Auxiliary active-clamping circuit limits the voltage overshoot effectively along with achieving soft-switching but fails to maintain ZVS for the extended operating range of load current and source voltage. In order to achieve extended range soft-switching operation, variable frequency switching approach is usually adapted and that is complex.

Maintaining soft-switching over wide operating range of source voltage and load current, while maintaining high efficiency, notably for high voltage gain applications is a challenge. This article avails magnetizing inductance energy of the transformer to elevate the soft-switching range of the semiconductor devices and introduces a new design. An active-clamped current-fed push–pull voltage doubler is proposed for higher voltage gain is illustrated in Fig. 1. Steady-state operation, mathematical analysis, circuit design and simulation results of this converter are illustrated.

2 Operation and Analysis of the Converter

The proposed configuration as illustrated in Fig. 1 is obtained from the hard-switched push–pull converter by adding two auxiliary switches S_{a1}, S_{a2} and one high-frequency capacitor Cc. For simplicity, transformer with single winding on the secondary side is used.

The transformer is used to provide isolation and voltage matching. Converter consists of two main switches S_{M1} and S_{M2}, two anti-parallel diodes D_{S1} and D_{S2}, two auxiliary clamping switches S_{al} and S_{a2}, two clamping diodes D_{a1} and D_{a2} and a clamping capacitor $C_{C.}$ Besides, the current feeding is provided by the constant voltage source V_{in} in series with the input inductor L. The push–pull transformer is represented by center-taped primary windings L_{P1} and L_{P2} and the secondary windings L_s. The leakage inductances are reflected on the primary side by L_{K1} and L_{K2}. Finally, the output is constituted by the voltage doubler diodes D_1 and D_2, voltage doubler capacitors C_1, C_2, output filter capacitor C_o and the output resistance R_o. C_{s1}, C_{s2}, C_{a1} and C_{a2} are being the snubber capacitors of their respective switches. The purpose of using voltage doubler on the secondary side is to increase the voltage at the output with less components count. Voltage doubler is electrically controlled circuit which charges the capacitor from input voltage through switches and develops 2 × the voltage across the load as its input (voltage on secondary side of transformer). Figure 2 indicates the gate pulses V_{gM1}, V_{ga1} for switches S_{M1} and S_{a1}, respectively. The two main switches S_{M1} and S_{M2} are operated with gating pulses delayed by half switching cycle with an overlap. Complimentary gating pulses control the auxiliary switches. Operational waveforms are illustrated in Fig. 3.

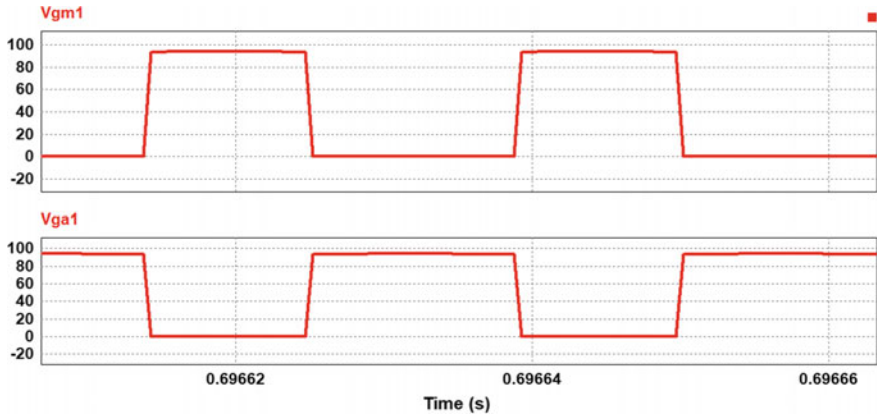

Fig. 2 Gating signals for the devices

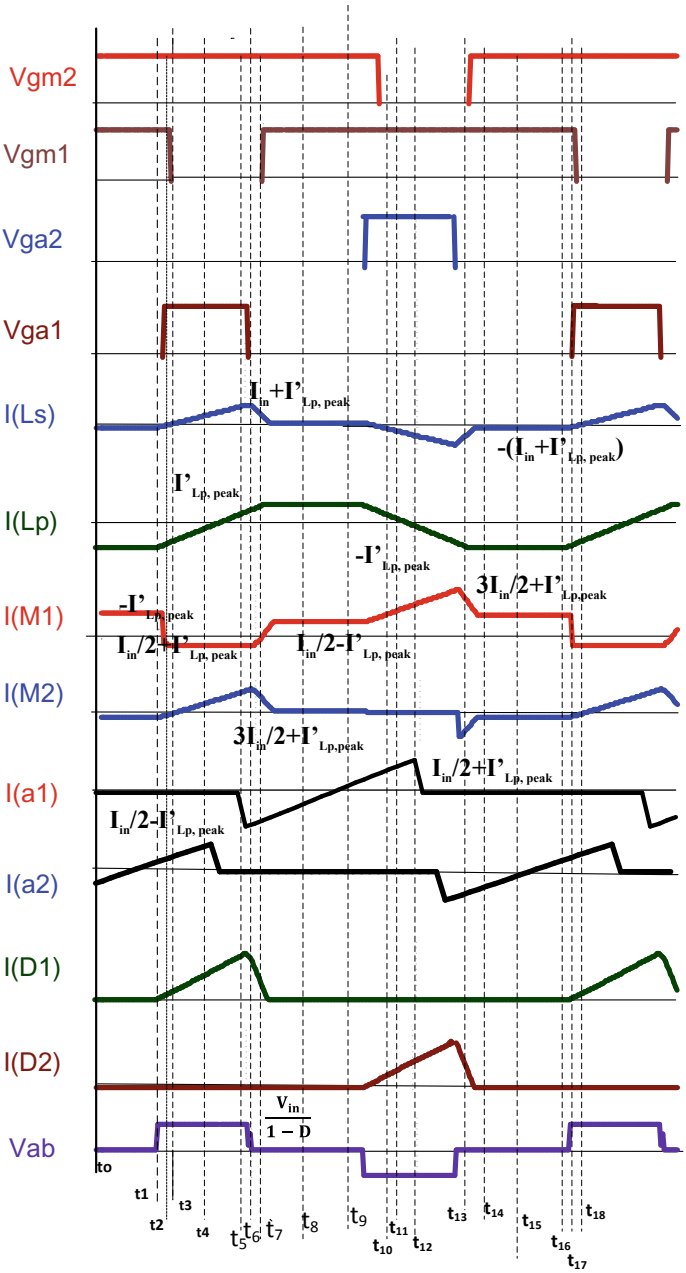

Fig. 3 Operational waveforms of proposed converter configuration

3 Design

In this section, converter design is explained for the following: Rated load power P_o (Full load) = 1kW, input voltage V_{in} = 22 to 41 V, output voltage V_o = 400 V, minimum load R_o = 160 Ω, output power P_o (10% load) = 100 W, minimum load R_o = 1600 Ω, switching frequency f_s = 40 kHz, converter's efficiency η = 95%.

1. Average input current:

$$\text{Input current } I_{in} = \frac{P_o}{\eta . v_{in}} = 47.8\,\text{A} \tag{1}$$

$$D = 1 - \frac{n.V_{in}}{V_0}$$

2. D_{max} is selected at minimum input voltage, i.e., V_{in} = 22 V and full load based on maximum switch voltage rating $V_{SW(max)}$ using

$$V_{max} = 1 - \frac{V_{in(max)}}{V_{SW(max)}} \tag{2}$$

For $V_{SW(max)}$ = 140 V, D_{max} = 0.85
Transformer turns ratio:
$0.5 < D < D_{max}$

$$0.5 < 1 - \frac{n.V_{in}}{V_0} < 0.85$$

$2.7 < n < 9.1$
Lower turns ratio reduces the range of ZVS. Higher high turns ratio increases the conduction loss.
n = 4.5 for D = 0.77 is chosen.

3. Inductor values L and L_p

$$L.\frac{\Delta I_{in}}{\Delta T} = V_{in} \tag{3}$$

$$\Delta I_{in} = 2.5\% \text{ of } I_{in} = 1.25\,\text{A}$$

$$L = 125\,\mu\text{H} \tag{4}$$

$$L_p = K.4.5^2.1.34\,\mu\text{H} \tag{5}$$

4. Values of leakage inductances:

$$\begin{aligned} L_{\text{LK}}.\frac{I_{\text{in}}}{(1-D)T_s} &= \frac{1}{2}\left(\frac{V_{\text{in}}}{1-D} - \frac{V_{\text{o}}}{n}\right) \\ \text{L}_{\text{LK}} &= \frac{1}{2}\left(\frac{V_{\text{in}}}{1-D} - \frac{V_{\text{o}}}{n}\right).\frac{1-\text{D}}{I_{\text{in}}.f_{\text{s}}} \end{aligned} \tag{6}$$

$$L_{LK1} = L_{LK2} = 1.3\,\mu\text{H}$$

5. Clamping capacitor:

$$C = \frac{I_{\text{in}}.(1-D)^2.T_s}{0.02(V_{\text{in}})} \tag{7}$$

$$C_c = 60\,\mu\text{F}$$

6. Voltage doubler diodes:

Diodes voltage rating
$V_{D(\max)} = V_0 = 400$ V
Average voltage doubler current:

$$I_{D(\text{avg})} = \frac{P_{\text{o}}}{2.V_{\text{o}}} \tag{8}$$

$$I_{D(\text{avg})} = 1.25\,\text{A}$$

7. Output capacitor:

$$C_{\text{o}} = \frac{I_o.(0.5-D).T_s}{\Delta V_{\text{o}}} \tag{9}$$

$C_{\text{o}} = 22$ μF; $C_1 = C_2 = 44$ μF

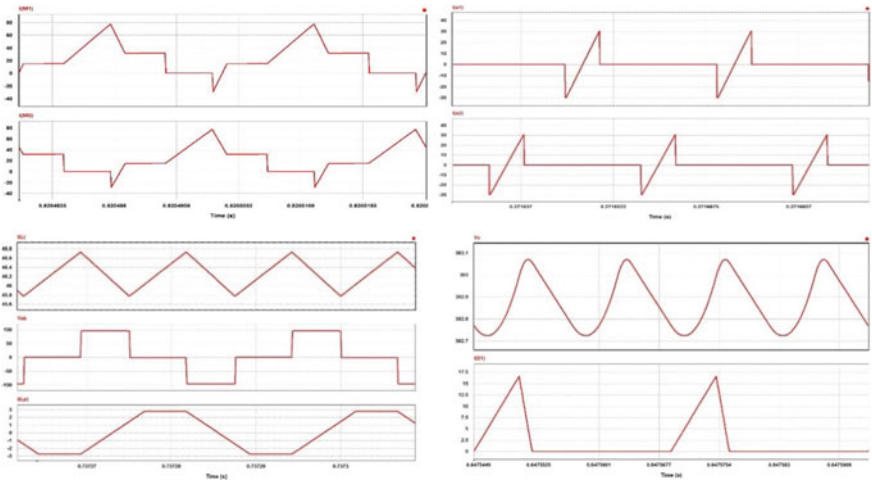

Fig. 4 Simulation waveform at V_{in} = 22 V and full load: main switch current $I(M1)$ and $I(M2)$, auxiliary switch current $I(a1)$ and $I(a2)$, diode current $I(D1)$, output voltage V_o, voltage V_{ab}, inductor current $I(L)$, parallel inductor current $I(L_p)$, output voltage (V_o) and diode current $I(D1)$

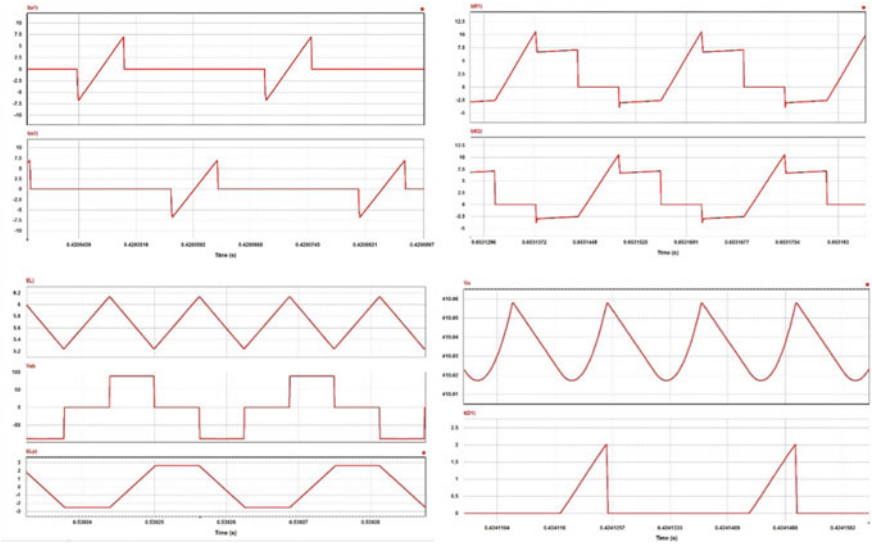

Fig. 5 Simulation waveform at V_{in} = 22 V and 10% full load: main switch current $I(M1)$ and $I(M2)$, auxiliary switch current $I(a1)$ and $I(a2)$, current across inductor $I(L)$, voltage V_{ab}, current across parallel inductor $I(Lp)$, output voltage V_o and current across diode $I(D1)$

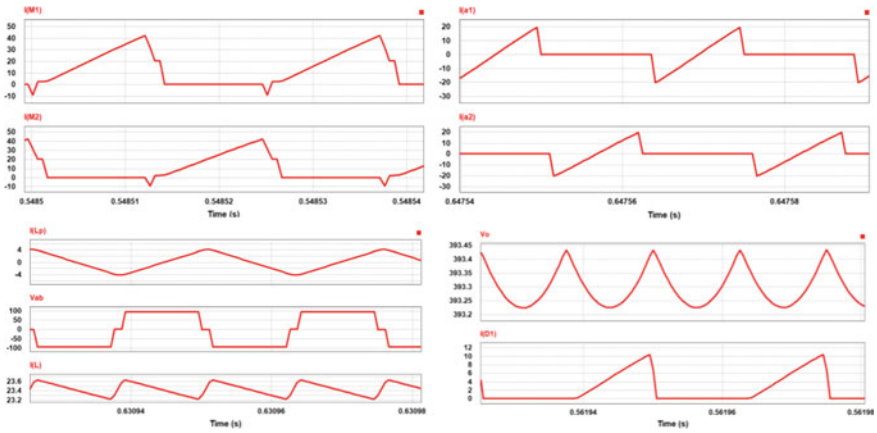

Fig. 6 Simulation waveform at V_{in} = 41 V and full load: current for two main switches $I(S_{M1})$ and $I(S_{M2})$ and current for two auxiliary switches $I(S_{a1})$ and $I(S_{a2})$, parallel inductor current $I(L_p)$, voltage V_{ab}, inductor current $I(L)$, output voltage V_o and diode current $I(D_1)$

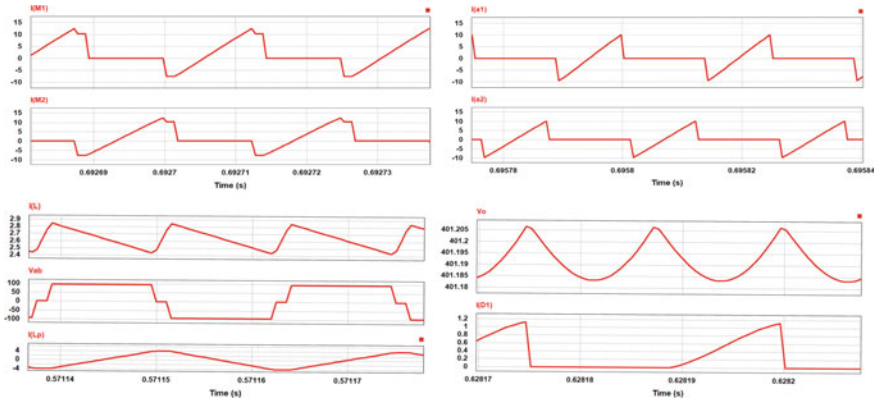

Fig. 7 Simulation waveform at V_{in} = 41 V and 10% load: current for two main switches $I(S_{M1})$ and $I(S_{M2})$ and current for two auxiliary switches $I(S_{a1})$ and $I(S_{a2})$. Parallel inductor current $I(L_p)$, voltage V_{ab}, inductor current $I(L)$, output voltage V_o and diode current $I(D_1)$

4 Simulation Results

The converter is designed and simulated for 1 kW using PSIM 11. Simulation results for four operating conditions of V_{in} = 22 V, rated power and 10% of rated power, V_{in} = 41 V, full load and 10% load are presented in Figs. 4, 5 6 and 7, respectively. At higher voltage and light-load condition, the duty cycle is low to maintain the same output voltage, and therefore, V_{AB} appears for longer time. It makes the currents I_{Ls} and I_{Lp} to be constant for a very small duration, and their

appearance looks like triangular. To achieve zero voltage switching, the body diodes (main and auxiliary) should conduct prior to the conduction of corresponding switches causing zero voltage turn-on. Cording to simulation results, turn-on ZVS is achieved. It should be observed that the duty cycle is reduced with increase in input voltage and/or reduction in load current. Therefore, it causes increase in peak value of parallel inductor current (magnetizing), which adds to series inductor current and helps extended ZVS operation of the converter.

5 Summary and Conclusion

To achieve ZVS over wide source voltage variation and varying output power/load while maintaining high efficiency has been a challenge, particularly for low voltage high current input specifications.

Simulation results using PSIM 11 have been presented. Because of high $L_p \triangleleft L_s$ ratio, the circulating current is very low compared to voltage-fed converters. Traditional and even advanced converters lose soft-switching at partial load current and higher supply voltage resulting in reduced partial load efficiency. Proposed current-fed push–pull converter offers wide range ZVS, high voltage gain and better light-load efficiency resulting in less fuel (hydrogen) demand or better fuel utilization, which further reduces the cost of energy due to fuel savings. Detailed study on steady-state operation and design is reported. Simulation results are presented to evaluate converter performance for extended operating range.

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