Power Quality Enhancement Using DSTATCOM with Reduced Switch-Based Multilevel Converter

Sudheer Vinnakoti, Anusha Palisetti and Venkata Reddy Kota

Abstract From the past few decades, the increased usage of non-conventional energy sources and nonlinear loads alarmed the researchers more concern about the power quality (PQ). Distribution static compensator (DSTATCOM) is voltage source inverter (VSI)-based shunt compensating custom power devices (CPD) used for current harmonic mitigation and also for reactive power compensation. The features of traditional multilevel inverters at high levels motivated the researchers to implement reduced switch topologies (RST) as they aim for reduction in cost, volume and to improve reliability of the system. This paper proposes a five-level RST-based DSTATCOM, which reduces the switch count to 33% compared to conventional multilevel converters. %THDs of five-level diode-clamped converter (DCC) and the proposed RST-based DSTATCOMs under same loading conditions are compared to show the potency of the converter. All the simulations will be carried out in MATLAB/Simulink software.

Keywords Power quality (PQ) · Custom power devices (CPD) · Distribution static compensator (DSTATCOM) · Reduced switch topology (RST) · Synchronous reference frame (SRF) · Total harmonic distortion (THD)

1 Introduction

From past few decades, the increased automobile and large-scale industries are demanding for high quality power. The growing power demand and degradation of conventional fossil fuels made the researchers to focus on alternate power-generating sources. Natural sources (such as solar, wind and biomass) are found to

S. Vinnakoti · A. Palisetti (✉)
Department of E.E.E, Raghu Engineering College (Autonomous), Dakamarri, Visakhapatnam, Andhra Pradesh, India

V. R. Kota
Department of E.E.E, University College of Engineering, JNTUK, Kakinada, Visakhapatnam, Andhra Pradesh, India

H. S. Saini et al. (eds.), *Innovations in Electrical and Electronics Engineering*, Lecture Notes in Electrical Engineering 626,
https://doi.org/10.1007/978-981-15-2256-7_11

be the best alternate sources due to their continuous availability with time and less environmental effects. Renewable energy sources [1, 2] united to the grid through electronic converters are causing some power quality issues. With the advent of semi-conductor-based sensitive loads, the concern for power quality increased from industries to consumers as the distorted supply results in malfunction of the equipment and reduces its efficiency. The passive filters used to suppress the harmonics have limited applications in high power due to their bulkiness in size, tuning problems and fixed range of reactive power compensation [3, 4]. Flexible AC transmission system [FACTS] [5] and custom power devices [CPD] introduced later gave better performance than passive filters and help in maintaining the desired power quality. FACTS devices help in improving the reliability and stability of the transmission system whereas compensating-type CDP is widely used in distribution networks for harmonic mitigation, VAR compensation, power quality and power factor improvement. It is researched and proven that (DSTATCOM) [6, 7] effectively mitigates all the current-related PQ issues when connected in shunt. It generally injects compensated currents 180° phase out with the harmonics in load current and makes the supply current harmonic free. In addition to the harmonic mitigation, DSTATCOM compensates reactive power, thereby aids in improving the power factor.

The traditional two-level inverter-based DSTATCOMs are predominantly suitable for small scale and utility grid due to their low output levels and high harmonics. The multilevel inverters [MLI] [8, 9] introduced later overcome the drawbacks of two-level as they produce high multistepped output with low THDs and are appropriate for coupling the RES to grid. Baker in his patent on MLI explained the generation of multistepped waveform, by cascading the single-phase H-bridge inverter fed with distinct DC sources. Later, several new topologies such as diode clamped or neutral point, flying capacitor were configured. These conventional MLIs have improved power factor, high-voltage levels with low device ratings, reduced stress and switching losses, lower THD, hence offering wide range of applications. But at very high level, the MLIs require more switching components, and the gate control circuitry associated with it becomes complex and effects the reliability of the system. The improved features of conventional MLI motivated researchers to configure new topologies with reduced switch count as they aim for improving the structure, reliability and efficiency with reduced size, cost and volume. THD is the other important factor which the researchers need to focus along with reduction in switch count and can be maintained low by proper control techniques. This paper proposes a new reduced switch topology [RST] which generates a five-level output.

The control techniques enhances the performance of the CPD [10], that they generate the reference current signals. The switching pulses to voltage source inverter (VSI) are generated by the controller based on error between the reference currents generated by the control algorithms and actual currents. The time-domain controls are commonly used due to its less computational time. Prominent control schemes are instantaneous reactive power theory (IRP), synchronous reference frame theory (SRF) [10–12], artificial neural network (ANN) [13], fuzzy logic controller (FLC) [14, 15], etc.

In this paper, the performance of RST-based DSTATCOM is analyzed in three-phase distribution system with nonlinear loads using SRF control. The THDs of source current of proposed RST-based DSTATCOM are measured and compared with traditional five-level DCC-based DSTATCOM using MATLAB/SIMULINK software. In this paper, Sect. 2 deals with the basic operating principle of DSTATCOM, and Sect. 3 explains multilevel concept with reduced switch count. SRF control scheme for DSTATCOM is discussed in Sect. 4. All the simulation results are discussed in Sect. 5. Work concludes with Sect. 6.

2 Distribution Static Compensator

Distribution static compensator [6] is a VSI-based shunt compensating device whose configuration is similar to the STATCOM but used in distribution systems. It is generally connected at point of common coupling (PCC) to reduce the current harmonics injected in systems due to nonlinear loads. It can be operated in both voltage and current control modes. In the former case, it balances the load voltage and maintains a constant value in order to protect the equipment from the voltage fluctuations. In the later case, it nullifies the harmonics in the supply current by injecting the distorted currents at PCC but in phase opposition to the harmonics introduced in load current. In addition to the harmonic filtering, it compensates reactive power, corrects power factor and enhances the power quality. The size selection and optimal location of the DSTATCOM play a pivotal role in reducing the cost and providing an effective compensation. The basic configuration of DSTATCOM involves (i) three-phase VSI which converts DC capacitor voltage into three-phase AC required by the system (ii) a coupling inductor which smoothens the output from ripples and (iii) DC bus capacitor. Figure 1 shows the block diagram representation of two-level inverter-based DSTATCOM with nonlinear load.

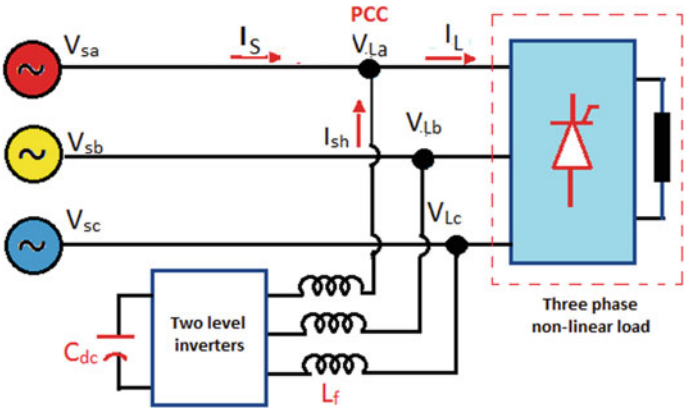

Fig. 1 Block diagram of two-level inverter-based DSTATCOM

In the equivalent model for DSTATCOM in Fig. 2a, V_s represents supply voltage, V_{sh} represents shunt compensated voltage of DSTATCOM, and I_{sh} represents the current injected at PCC. The basic operating principal of DSTATCOM can be explained in three modes based on the supply voltage and shunt voltage generated by DSTATCOM.

(i) If the output voltage V_{sh} of DSTATCOM and the supply voltage are of equal magnitudes and are in phase, then DSTATCOM neither injects nor absorbs the reactive power.
(ii) If the injected voltage V_{sh} is less than the V_s, then the shunt current I_{sh} lags the supply voltage V_S by certain angle as shown in Fig 2b. In this case, the DSTATCOM acts in inductive mode, i.e., it absorbs the reactive power.
(iii) In Fig. 2c, I_{sh} leads the supply voltage V_S by certain angle as V_{sh} generated by DSTATCOM is more than the supply voltage V_s. Here, the DSTATCOM acts in capacitive mode and supplies all the reactive power required by the

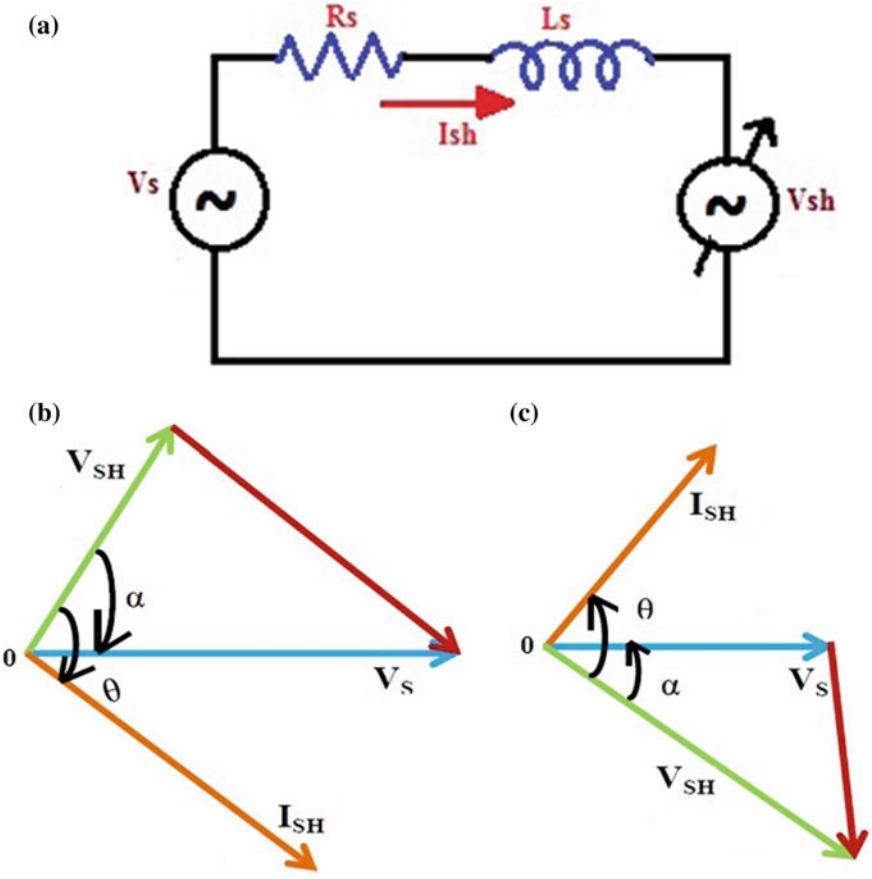

Fig. 2 **a** Equivalent model of DSTATCOM **b** Inductive mode **c** Capacitive mode

load. Thus, from the above discussion, we can summarize that DSTATCOM can either inject or absorb the reactive power, and its magnitude depends on the angle between V_{sh} and $V_{S.}$

The design of DC bus capacitor plays a prominent role and should be maintained at least 0.9 p.u. The DC bus capacitance (C_{DC}) value depends on the DC bus voltage (V_{DC}) which should be maintained twice the peak value of phase voltage to reduce voltage ripples and avoid resonance problems. The minimal values of V_{DC} and C_{DC} to be maintained for effective compensation are given by Eqs. (1, 2), respectively.

$$V_{DC} = \frac{2\sqrt{2}V_{LL}}{\sqrt{3}m} = \frac{2\sqrt{6}V_{ph}}{\sqrt{3}m} \tag{1}$$

$$\frac{C_{DC}}{2} = \frac{3V_{ph}I_s ta}{\left[(V_{DC})^2 - (V_{DC1})^2\right]} \tag{2}$$

where V_{LL} is the line voltage; V_{ph} is the phase voltage: m is the modulation index whose value is between $0 < m < 1$; t is the response time, a is the overloading factor, V_{DC} is the DC bus capacitor voltage, and V_{DC1} is the dip in voltage.

3 Reduced Switch Multilevel Inverter

The output generated with conventional two-level inverters is low with more harmonics, and hence, its application to high power is limited. In high-power applications, these conventional two-level inverters need to operate at high frequency, which increases voltage stress and temperature, reducing the efficiency of the system. Multilevel inverters (MLI) introduced by Baker in 1975 are found to be well suited for interfacing the RES with grid. As they generate high-level multi-stepped output by using different pulse width modulation (PWM) techniques, their application extended to medium and large-scale industries. Baker explained the synthesis of staircase waveform by adding of single-phase full bridges each fed with distinct DC sources hence named cascaded MLI, and later, he proposed another new topology by using clamping diodes and named as diode-clamped multilevel inverter (DCMLI). In 1992, Foch and Meynard replaced all the clamping diodes with clamping capacitors and named it as flying capacitor (FC) MLI. The advantages of MLI over two-level are high efficiency, reduced switch stress, reduced switching loss, low harmonic content which reduces the filtering cost. Table 1 compares the components of conventional topologies for m-levels. From the table, it is clear that with the increase in levels, the components required increase, and the control of gate circuitry associated with it becomes complex affecting the systems reliability. The above drawbacks and features of MLI made

Table 1 Comparison of components among the conventional MLI

Converter type	Diode-clamped	Flying capacitors	Cascaded H-Bridge
Main switching devices	(m − 1) × 2	(m − 1) × 2	(m − 1) × 2
Main diodes	(m − 1) × 2	(m − 1) × 2	(m − 1) × 2
Clamping diodes	(m − 1) × (m − 2)	0	0
DC bus capacitors	(m − 1)	(m − 1)	(m − 1)/2
Balancing capacitors	0	(m − 1) × (m − 2)/2	0

the researchers to focus on new inverter topologies generating high output levels with reduced switch count as they reduce cost, size and volume. THD is the other important factor that can be minimized by implementing proper control technique.

This paper uses a well-known three-phase VSI. The basic configuration of proposed RST using three groups of conventional three-phase two-level VSI [16] generating a five-level output is shown in Fig 3b. The two inverter groups in RST are cascaded in such a way that a five-level voltage appears across open-ended primary winding of transformer. As the two ends of the open-ended primary are fed with two separate VSIs, zero sequence currents circulation is avoided, and the maximum possible voltage that can be generated by combination of inverter switches in proposed RST is $2V_{DC}$ with an input of V_{DC}. The voltages V_1 V_2 and V_3 are five levels ($+2V_{DC}$, $+V_{DC}$, 0, $-V_{DC}$, $-2V_{DC}$) generated by making the following connections: the first leg of inverter 1 is connected to the second leg of inverter 3

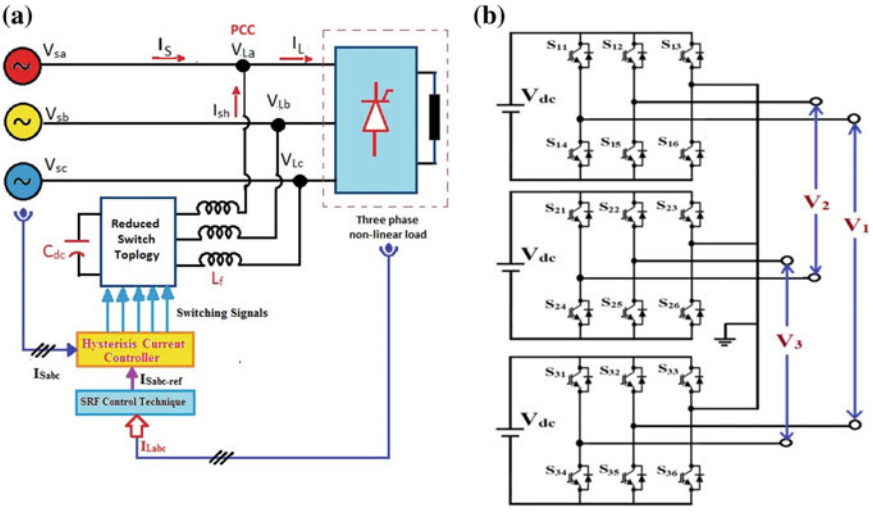

Fig. 3 Block diagram of RST-based DSTATCOM

Table 2 Comparison between conventional MLI and proposed RST

Comparison	Conventional cascaded MLI	Proposed RST
Maximum voltage	$2V_{DC}$	$2V_{DC}$
No. of switches	6 single phase	3 three phase
No. of switches	24	18

for generating V_1. Similarly, the voltage V_2 is generated by connecting the first leg of inverter 2 to the second leg of inverter 1, and the voltage V_3 is measured by connecting the first leg of inverter 3 to the second leg of inverter 2. The triggering pulses to the inverter switches are generated by PWM current controller based on error between the reference current signals extracted by control schemes and actual current signals.

Table 2 compares between conventional cascaded MLI and proposed RST. The conventional cascaded H-bridge multilevel inverter uses six single-phase bridges, whereas the proposed RST uses exactly half the number but in three-phase module for generating same voltage levels. Table 2 shows that proposed RST uses lesser number of switches compared to conventional MLI and reduces the cost and switching losses associated with switches. The block diagram of RST-based DSTATCOM is shown in Fig. 3a.

4 Synchronous Reference Frame Theory

Control techniques play a prominent role in deciding the performance of DSTATCOM, and they generate the reference current signals based on which the pulses are given to the switches. The control algorithms are available in both time and frequency domains. Nowadays, some soft computing techniques are also been used for extraction of reference signals. In this paper, the time-domain control is being implemented as they involve mathematical calculations and require less time. SRF theory is commonly used traditional method to mitigate all the current and voltage-related harmonics and can operate in transient and steadystate mode to control active power filters. In this theory, the sensed harmonic load currents in three phase (i_{la}, i_{lb}, i_{lc}) are first converted into the stationary two-phase frame (α-β-0 frame) and later into the synchronously rotating d-q-0 frame by using different transformation techniques as depicted in Fig. 4. The input voltage signals (V_a, V_b, V_c) are passed through the phase-locked loop (PLL) to generate the signals in terms of sine and cosine functions. The currents i_d and i_q in d-q plane involve average ($\bar{i}_d$ and $\bar{i}_p$) and oscillatory components ($\tilde{i}_d$ and $\tilde{i}_p$). The oscillatory components are undesirable as they cause harmonic currents and are filtered by using the low-pass filters (generally a second-order Butterworth LPF) so that only DC components are extracted. The average DC components are transferred back to (a-b-c) by reverse transformation techniques. The transformation and reverse transformation

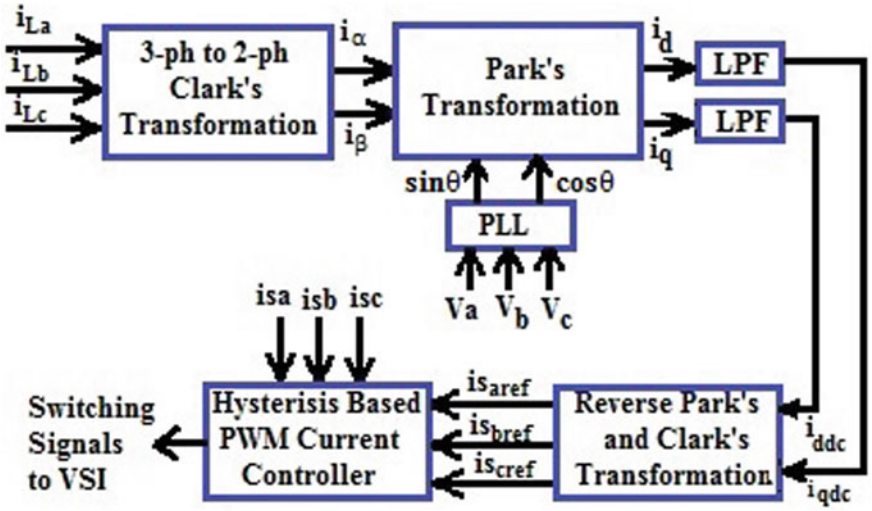

Fig. 4 Block diagram representation for reference currents generation by using SRF control

techniques used for converting the three-phase quantities into synchronously rotating two phase are given by Eqs. 3 and 4, respectively. A comparison between reference source current and the source currents generates an error signal, based on which hysteresis current controller generates the triggering pulses to VSI given in Fig. 4.

$$\begin{bmatrix} I_{S0} \\ I_{Sd} \\ I_{Sq} \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ \sin(wt) & \sin\left(wt - 2\pi/3\right) & \sin\left(wt + 2\pi/3\right) \\ \cos(wt) & \cos\left(wt - 2\pi/3\right) & \cos\left(wt + 2\pi/3\right) \end{bmatrix} \begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix} \tag{3}$$

$$\begin{bmatrix} I_{Saref} \\ I_{Sbref} \\ I_{Scref} \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1/\sqrt{2} & \sin(wt) & \cos(wt) \\ 1/\sqrt{2} & \sin\left(wt - 2\pi/3\right) & \cos\left(wt - 2\pi/3\right) \\ 1/\sqrt{2} & \sin\left(wt + 2\pi/3\right) & \cos\left(wt + 2\pi/3\right) \end{bmatrix} \begin{bmatrix} I_{S0} \\ I_{Sd} \\ I_{Sq} \end{bmatrix} \tag{4}$$

In Fig. 5, the reference currents generation by using SRF control under nonlinear loads is shown. The DC link capacitor voltage must be maintained constant for effective compensation. This can be attained by proper tuning of the by proper tuning of the gains of the PI controllers. These controllers are generally used for estimating the losses in DC bus. For SRF theory, the output of PI controller is added to *d*-axis component. The PLL used in SRF works effectively under low distortion, as its performance is poor in case of high distortions. To overcome this, modified PLL is used to improve the system performance under unbalance and high distortion conditions.

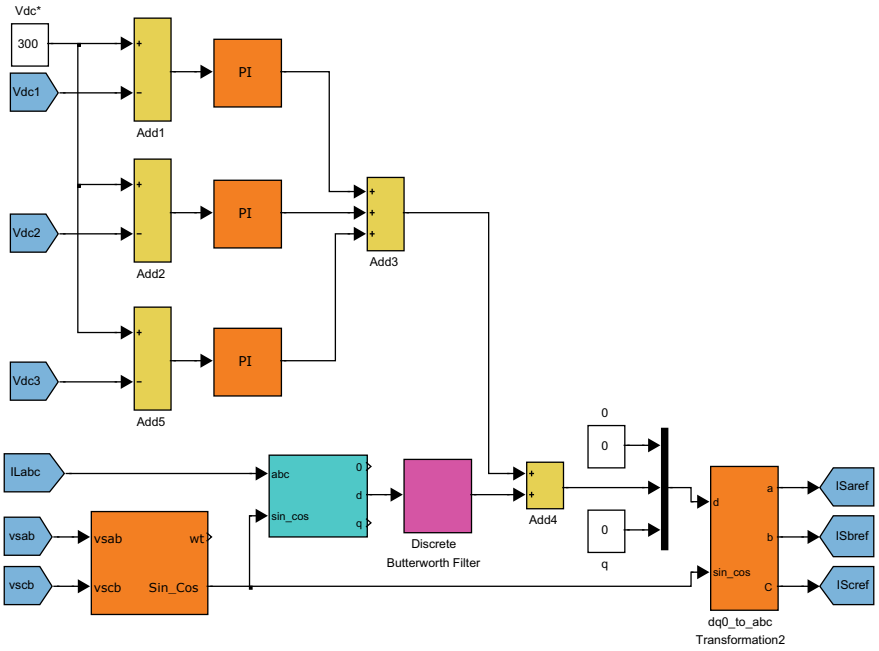

Fig. 5 Reference currents generation by using SRF control under nonlinear load in Simulink model

5 Simulation Results

The proposed RST-based DSTATCOM with SRF control in three-phase distribution system with nonlinear loads is designed in MATLAB/SIMULINK software. Figure 6 depicts the supply voltage (V_{Sabc}), load current (I_{Labc}) and supply current (I_{Sabc}) before and after connecting RST-based DSTATCOM. The proposed RST-based DSTATCOM is connected at 0.2 s. Compensating currents are injected by the RST-based DSTATCOM at PCC in phase opposition to the harmonics generated by nonlinear loads, thereby making the source current (in Fig. 6c) harmonic free. For current harmonic mitigation, a constant voltage of 700 V needs to be maintained across each DC bus capacitors which can be maintained by proper tunning of PI controllers.

Extension to above, analysis also concentrated on the reactive and active powers. It can be noticed that before connecting the proposed RST-based DSTATCOM, i.e., from 0 to 0.2 s, the source caters entire active power requirement of load, i.e., 8 KW. Figure 7a, b and c gives the complete active power profiles of supply, load and RST-based DSTATCOM, respectively, before and after compensation. After connecting the RST-based DSTATCOM, it mitigates the supply current harmonics by consuming 0.997 KW active power from the supply. It can be clearly observed

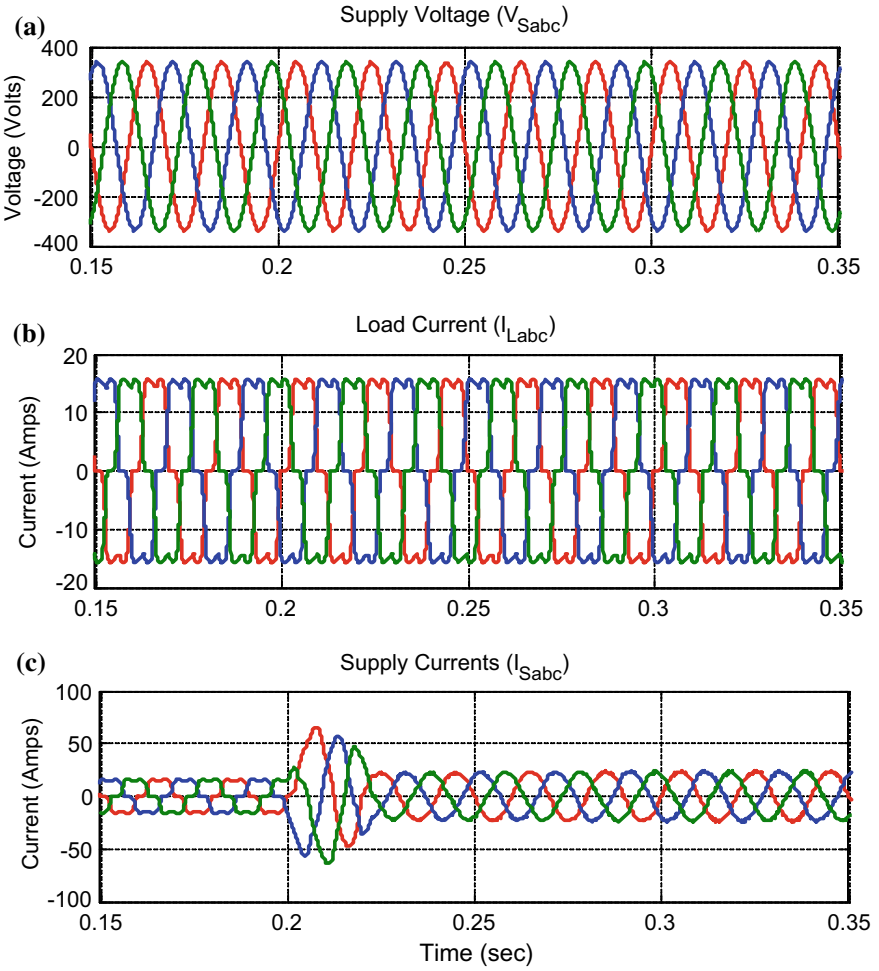

Fig. 6 Effect of compensation on **a** supply voltage **b** load current and **c** supply current

from Fig. 7a that the supply active power is increased from 8 to 10 KW during the time period 0.25–0.4 s. The dynamic state of system can be observed during the interval 0.2–0.25 s.

Similarly, Fig. 8 shows the complete analysis of reactive power at load and supply before and after connecting the RST-based DSTATCOM. From Fig 8a, it is observed that source supplies all the 2.2 kVAR reactive power needed by the load during the period 0–0.2 s, whereas the proposed RST-based DSTATCOM remains at 0 KAVR as it is not connected to system. After connecting proposed RST-based DSTATCOM at 0.2 s, the DSTATCOM itself delivers all the reactive power needed by the load making the source to deliver only the active power needed by load. The reactive power at supply and load before and after connecting proposed

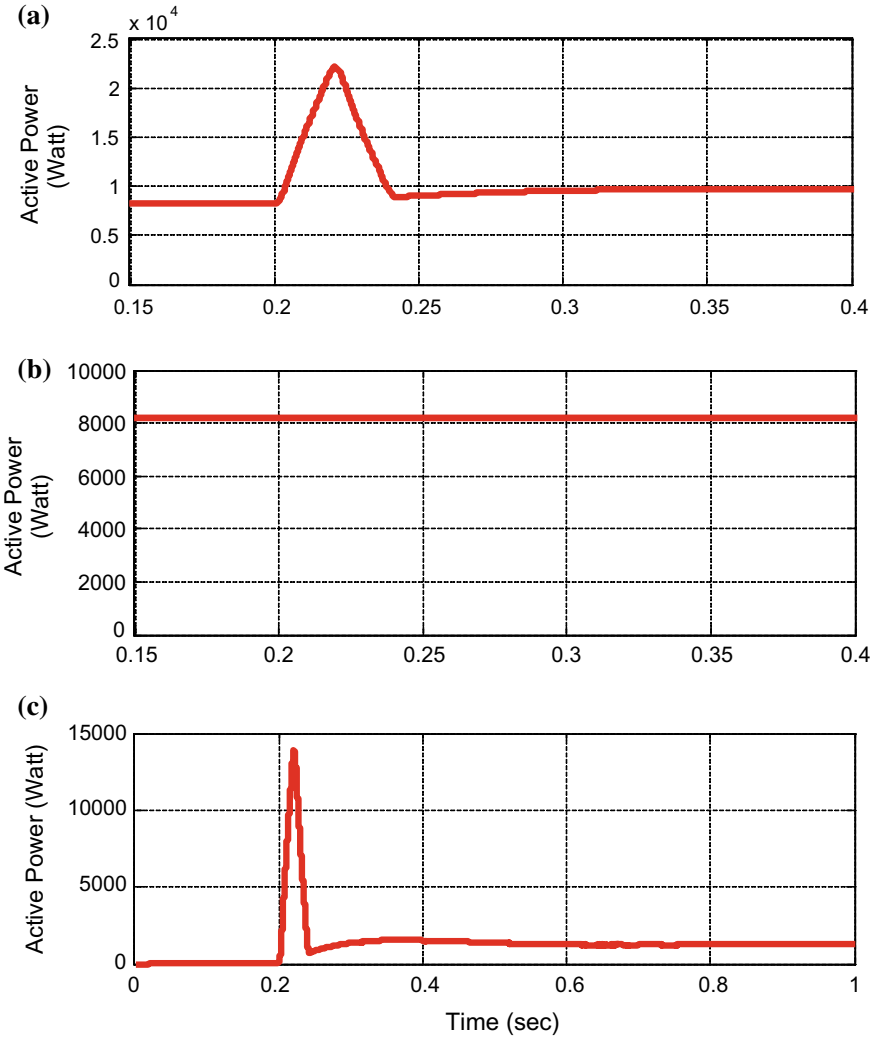

Fig. 7 Active power at **a** supply **b** load **c** DSTATCOM

RST-based DSTATCOM is shown in Fig 8a, b, respectively. The proposed RST-based DSTATCOM alone delivering all the reactive power required by load is shown in Fig. 8c.

It can be noticed from Table 3 that %THD of supply currents in respective phases before compensation are 20.81% with their fundamental components as 16.61%. After connecting the RST-based DSTATCOM, it is clearly observed that the % THD of phase A, phase B and phase C of supply current are lowered to 3.00, 3.19 and 3.10% with an increase in their fundamental component as shown in

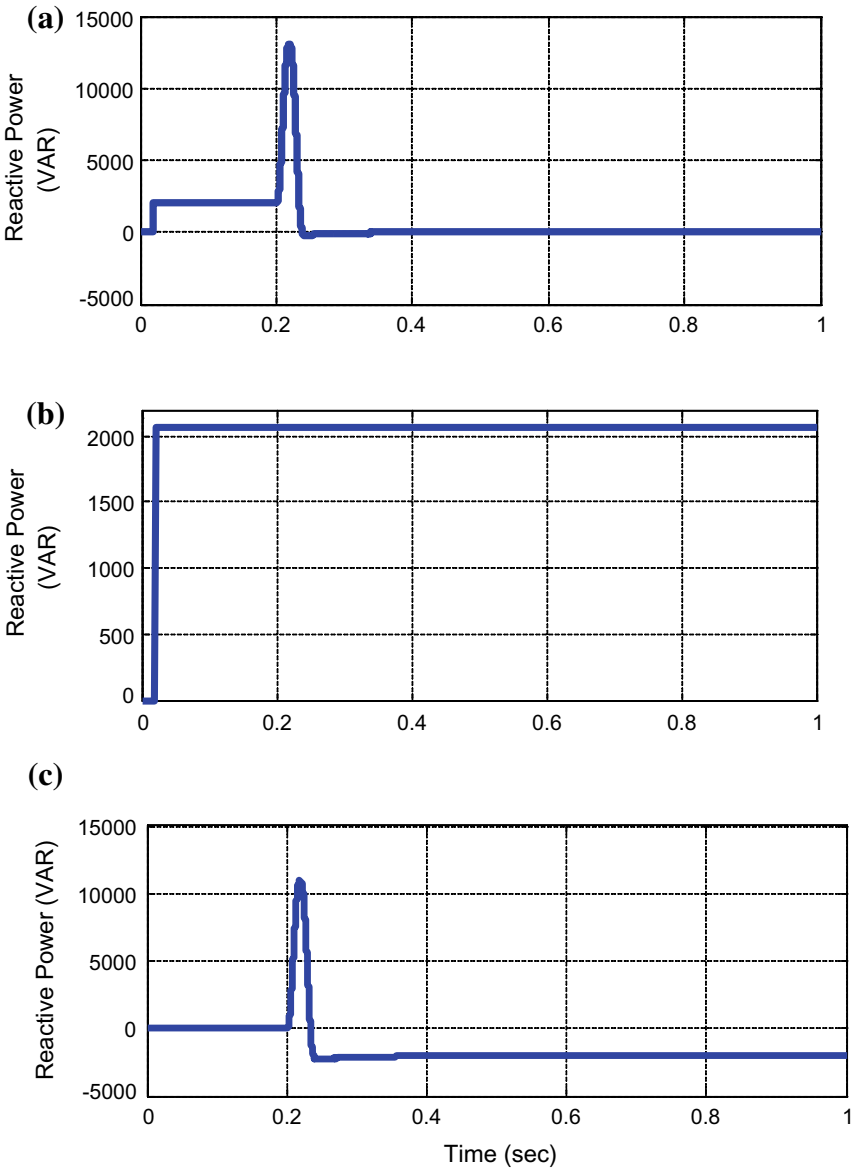

Fig. 8 Reactive power at **a** supply **b** load c DSTATCOM

Table 3. In addition to the above, the study is also conducted on conventional five-level diode-clamped MLI, and the observed results are compared with proposed RST to prove the effectiveness of the topology.

Table 3 Comparison between conventional MLI and proposed RST-DSTATCOMs using SRF

Nonlinear load		SRF controller			
		Fundamental component (A)		% THD	
		Before	After	Before	After
Five-level DCC DSTATCOM	I_{Sa}	16.61	**18.72**	20.81	**3.47**
	I_{Sb}	16.61	**18.52**	20.81	**3.46**
	I_{Sc}	16.61	**17.83**	20.81	**3.23**
Proposed RST-DSTATCOM	I_{Sa}	16.61	**18.74**	20.81	**3.00**
	I_{Sb}	16.61	**18.31**	20.81	**3.19**
	I_{sc}	16.61	**17.78**	20.81	**3.10**

6 Conclusion

The performance of the proposed RST-based DSTATCOM is examined under nonlinear load with SRF control technique. Then, the potential of the proposed RST-based DSTATCOM is compared with that of conventional multilevel inverters by using MATLAB/SIMULINK software. From the results, it is clearly noticed that the proposed RST-based DSTATCOM mitigates all the supply current harmonics effectively compared to the traditional multilevel inverters (DCC). Further, it can be noted that the %THD of the supply currents are minimized after the compensation. Hence, from the above discussion, it can be concluded that the proposed RST-based DSTATCOM has improved performance over the conventional MLI with reduced switching cost and losses.

References

1. J. Benedek, T.T. Sebestyen, B. Bartok, Evaluation of renewable energy sources in peripheral areas and renewable energy-based rural development. Renew. Sustain. Energy Rev. **90**, 516–535 (J. Elsevier, Romania, 2018)
2. S. Guo, Q. Liu, J. Sun, H. Jin, A review on the utilization of hybrid renewable energy. Renew. Sustain. Energy Rev. **91**, 1121–1147 (J. Elsevier, China, 2018)
3. O. Prakash Mahela, A. Gafoor Shaik, Topological aspects of power quality improvement techniques: a comprehensive overview. Renew. Sustain. Energy Rev. **58**, 1129–1142 (J. Elsevier, India, 2016)
4. W.U. Tareen, S. Mekhilef, M. Seyedmahmoudian, B. Horan, Active power filter (APF) for mitigation of power quality issues in grid integration of wind and photovoltaic energy conversion system. Renew. Sustain. Energy Rev. **70**, 635–655 (J. Elsevier, Australia, 2017)
5. F.H. Gandoman, A. Ahmadi, A.M. Sharaf, P. Siano, J. Pou, B. Hredzak, V.G. Agelidis, Review of FACTS technologies and applications for power quality in smart grids with renewable energy systems. Renew. Sustain. Energy Rev. **82**, 502–514 (J. Elsevier, Australia, 2018)

6. O. Prakash Mahela, A. Gafoor Shaik, A review of distribution static compensator, renewable and sustainable energy reviews. Renew. Sustain. Energy Rev. **50**, 531–546 (J. Elsevier, Jodhpur, India, 2015)
7. B. Singh, P. Jayaprakash, D.P. Kothari, A. Chandra, K. Al Haddad, Comprehensive study of DSTATCOM configurations. IEEE Trans. **10**, 854–870 (India, 2014)
8. A. Sinha, K.C. Jana, M.K. Das, An inclusive review on different multi-level inverter topologies, their modulation and control strategies for a grid connected photo-voltaic system. Solar Energy **170**, 633–657 (J. Elsevier, Dhanbad, India, 2018)
9. N. Prabaharan, K. Palanisamy, A comprehensive review on reduced switch multilevel inverter topologies, modulation techniques and applications. Renew. Sustain. Energy Rev. **76**, 1248–1282 (J. Elsevier, Tamil Nadu, India, 2017)
10. R. Kumar, H.O. Bansal, Shunt active power filter: current status of control techniques and its integration to renewable energy sources. Sustain. Cities Soc. (J. Elsevier, Rajasthan, India, 2018)
11. R.S. Herrera, P. Salmeron, H. Kim, Instantaneous reactive power theory applied to active power filter compensation: different approaches, assessment, and experimental results. IEEE Trans. **55**(1), 184–196 (Chungnam, Korea, 2008)
12. B. Singh, J. Solanki, A comparison of control algorithms for DSTATCOM. IEEE Trans. **56** (7), 2738–2745 (New Delhi, India, 2009)
13. M. Qasim, P. Kanjiya, V. Khadkikar, Artificial-neural-network-based phase-locking scheme for active power filters. IEEE Trans. **61**(8), 3857–3866 (Abu Dhabi, UAE, 2014)
14. D. Amoozegar, DSTATCOM modelling for voltage stability with fuzzy logic PI current controller. Electr. Power Energy Syst. **76**, 129–135 (J. Elsevier, Shiraz, Iran, 2016)
15. J. Fattahi, H. Schriemer, B. Bacque, R. Orr, K. Hinzer, J.E. Haysom, High stability adaptive microgrid control method using fuzzy logic. Sustainable Cities Soc **25**, 57–64 (J. Elsevier, Ontario, Canada, 2016)
16. V.F. Pires, A. Cordeiro, D. Foito, J.F. Silva, Three-phase multilevel inverter for grid-connected distributed photovoltaic systems based in three three-phase two-level inverters. Solar Energy **174**, 1026–1034 (J. Elsevier, Setubal, Portugal, 2018)