

Digital-Controlled Dual-Mode Switching Mode Power Supply for Low-Power Applications



K. Shubha Rao  and Veena S. Chakravarthi 

Abstract This paper discusses the modeling of a multi-mode digitally controlled switching mode buck converter to power a system-on-chip (SOC). It operates in digital pulse width modulation mode under heavy and medium load conditions, whereas in digital pulse frequency modulation mode it operates under light load conditions to obtain high-power conversion efficiency over a wide range of load current. In PWM mode of operation, $\Sigma-\Delta$ modulator-based digital pulse width modulator (DPWM) is implemented which provides high-resolution, low-power architecture to supply accurate, precise and low ripple content voltage to SOCs. A type III compensator is designed to improve the dynamic performance of the buck converter. Maximum efficiency of 88.48% is obtained at 0.2 A under PWM mode of operation. An output voltage accuracy of 0.25% is achieved against a target value of 1%. The load current and line voltage transient responses are verified by considering the different range of load current and line voltage variations. As an example, for a load variation from 150 to 400 mA, the undershoot is 30 mV, and when the load varies from 400 to 150 mA, the overshoot is 32 mV. The % peak overshoot/undershoot is around 3%. The response time of the power supply when load variations occur (150–400 mA and vice versa) is 3 μ s. The steady-state output voltage is 1.002 V, when the input battery voltage varied from 2.5 to 3.2 V and vice versa; in addition, the undershoot and overshoot in output voltage are 20 and 25 mV, respectively. The time taken by the power supply to settle to a steady value of 1.0025 is 10 μ s. Light load or power save mode efficiency is improved by using a DPFM mode of operation. The minimum efficiency obtained is 66.62% at 0.001 A. The % efficiency lies between 66.62 and 85% for a load current range of 0.001–0.1 A

Keywords Buck converter · Digital pulse width modulation · Digital pulse frequency modulation

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1 Introduction

As technology evolves, more functionalities are being added to the SOCs. At the same time, the speed of operation of the system needs to be high with operating and stand-by power loss maintained low. Latest systems-on-chip and networks-on-chip are multi-core systems and they need efficient power supply regulators that provide a well-regulated constant DC voltage to increase their performance, reliability and lifespan. In addition, the regulated output voltage should contain minimum ripple. It is very challenging to design such highly efficient power supply regulators that deliver a low voltage with fewer ripples to a load varying over a wide range.

Changes in load current occur when SOC switches between various modes of operation. When SOC is operating in active mode, the load current demand is high whereas in sleep mode it is low. Since there are billions of transistors involved in a SOC operation, voltage regulators must have a fast transient response, to respond quickly to the changes in load current.

Efficiency is a good measure of the superiority of power supply circuitry. If the power efficiency is low, it would result in large power dissipation and hence enormous amount of heat gets generated. This large heat generation needs expensive cooling systems which increase the area occupied by the system. Hence a high-efficiency converter is essential so that elements can be packaged with high density, resulting in small size and weight, and low temperature rise.

Accordingly, this paper explains the modeling of a buck switching mode power supply that achieves regulated voltage with less ripple content, high frequency of operation and high efficiency. The switching mode power supply is controlled digitally and it operates in two modes of operation according to the load current. It operates in PWM mode during medium and heavy load condition and in PFM mode during light load/sleep mode of operation to achieve high power efficiency over the entire range of load condition.

The paper is organized as follows: Section 2 discusses the structural view of the multi-mode buck converter. Section 3 provides modeling of DPWM mode buck converter. Section 4 explains modeling of DPFM mode of operation. The results are analyzed in Sect. 5, and conclusions are drawn in Sect. 6.

2 Digital Multi-Mode Buck Switching Mode Power Supply

Figure 1 shows the digital power supply regulator using a buck converter. It operates in two modes of operation, namely PWM and PFM. PWM mode consists of digital type III compensator and second-order sigma–delta modulator, whereas PFM comprises hysteretic comparator. As closed-loop control is a digital controller, the analog voltage V_{out} is converted into a digital/discrete signal. This is done with the help of analog to digital converter (ADC). The compensator block generates a discrete signal which is proportional to the duty ratio. This discrete signal is given to DPWM

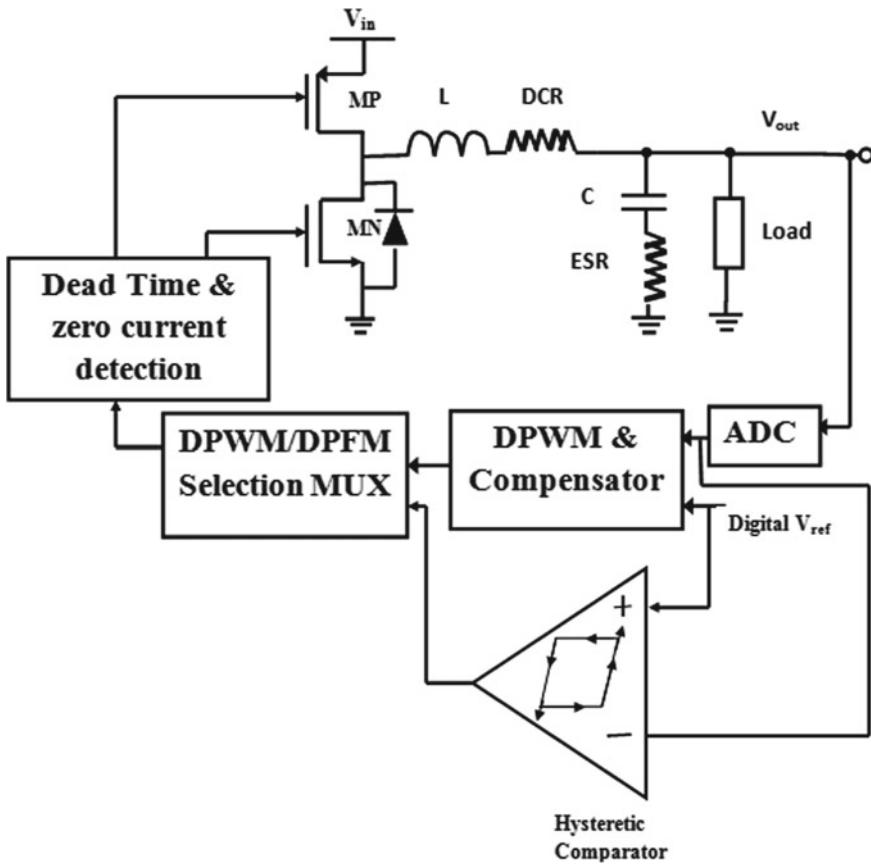


Fig. 1 Block diagram of the digital multi-mode buck power supply module

block wherein the discrete signal is converted back into an analog signal to drive the switches of the buck converter to maintain the output voltage to the desired value [1].

The PWM mode of operation is used under heavy and medium load conditions. The PFM mode of operation comprises a hysteretic comparator which compares the output voltage with an upper and lower threshold voltage to generate PFM pulses [2]. A multiplexer is used to select the PWM or PFM mode of operation depending on load condition [3, 4]. Finally, we have a dead time generator to generate two non-overlapping pulses to drive power MOSFETs. Under light load condition, a zero current detection is done to operate the buck converter in discontinuous current mode (DCM) of operation. The buck converter is designed to provide 1 V, 800 mA output from an energy source, that is, battery with an input voltage of 3.2 V.

Considering 20% current ripple, 1% voltage ripple and 5% maximum output voltage overshoot, the synchronous buck converter is designed. A MATLAB program is written to find the values of the LC filter. Table 1 shows the main specifications of the synchronous buck converter.

3 PWM Mode of Operation of the Buck Converter

In PWM architecture, the desired output voltage is obtained by varying the duty cycle D of the switching elements. The frequency of operation is kept constant which simplifies the design of the feedback loop and the output LC low-pass filter. PWM method of control also results in high efficiency and low output ripple content during moderate and heavy load conditions. However, in PWM control technique the efficiency of the converter reduces drastically under light load conditions as the switching losses which are load independent becomes predominant over the conduction losses. The two main components of PWM mode of operation of buck converter are DPWM and type III compensator, which will be explained in the following sections.

3.1 Design of 13-Bit $\Sigma - \Delta$ Modulator DPWM

A high-resolution DPWM is necessary to achieve precise output voltage and avoid limit-cycle oscillations [5–7]. In this paper, a 13-bit DPWM structure which consists of a second-order $\Sigma - \Delta$ modulator having 6-bit resolution and a counter-comparator block with the 7-bit resolution is designed. The hybrid architecture consists of one

Table 1 Buck converter specifications

Parameter	Minimum	Nominal	Maximum
Input voltage (V_{in})	1.8 V	3.2 V	3.6 V
Output voltage (V_{out})	0.9 V	1 V	1.2 V
Output current (I_{out})	2 mA		800 mA
Switching frequency (f_s)	–	10 MHz	–
Output inductor (L)		1 μ H with DCR = 1 $m\Omega$	
Output capacitor (C_0)		2 μ f with ESR = 9 $m\Omega$	

hardware method (counter comparator DPWM) and one soft method ($\Sigma-\Delta$ modulator) to ease or lessen the requirement of high clock frequency and hence reduce power consumption [8, 9]. Figure 2 shows the structural representation of the hybrid DPWM.

Figure 3 shows the structural configuration of the $\Sigma-\Delta$ modulator-based DPWM. The effective resolution of the 7-bit core DPWM is increased to 13-bit by 6-bit $\Sigma-\Delta$ modulator by using noise shaping concept. The hybrid $\Sigma-\Delta$ modulator-based DPWM is modeled in the digital domain using Xilinx system generator tool and timing simulation is performed to verify the design.

3.2 Design of Type III Compensator

A type III compensator provides three poles (one at the origin) and two zeroes which results in phase boost to offset the phase lag introduced by output LC filter complex pole [10]. The poles and zeroes of the type III compensator network should be carefully placed and selected to achieve the desired crossover frequency, sufficient phase margin, good steady-state output and fast transient response. The transfer function in the digital domain is obtained as:

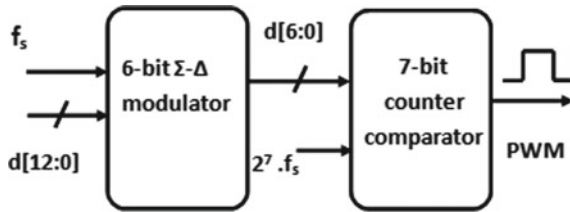


Fig. 2 Structure of $\Sigma-\Delta$ DPWM

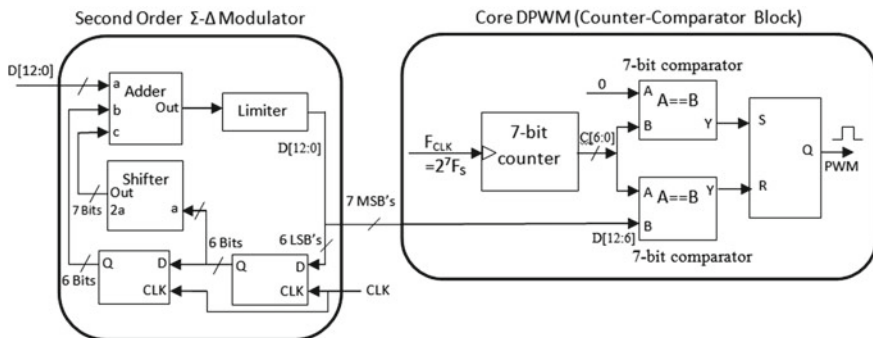


Fig. 3 The architecture of high-resolution $\Sigma-\Delta$ modulator-based DPWM

$$G_{TYPE3}(z) = K + \frac{R_1}{(z - P_1)} + \frac{R_2}{(z - P_2)} + \frac{R_3}{(z - P_3)} \tag{1}$$

Based on the specifications of the buck converter as given in Table 1, pole placement technique is used to designing type III compensator for a phase margin of 70° and a crossover frequency of 1/16 of switching frequency. A MATLAB program is written to obtain a digital representation of type III compensator and Fig. 4 shows its bode plot. The phase margin and crossover frequency of buck converter without compensator is 12.3° and 1.44 × 10⁶ rad/s, respectively, and is increased to 62.2° and 4.16 rad/s by using type III compensator.

Once the compensator is designed, it is implemented digitally in a parallel configuration for a buck converter. In order to perform digital control of buck converter, Xilinx system generator tool is used, which is as shown in Fig. 5.

4 PFM Mode of Operation of the Buck Converter

PFM is a nonlinear control method in which a train of pulses is applied to the converter switches to maintain the output voltage within the predetermined voltage range. The frequency of operation is reduced in PFM method, which in turn lowers the switching

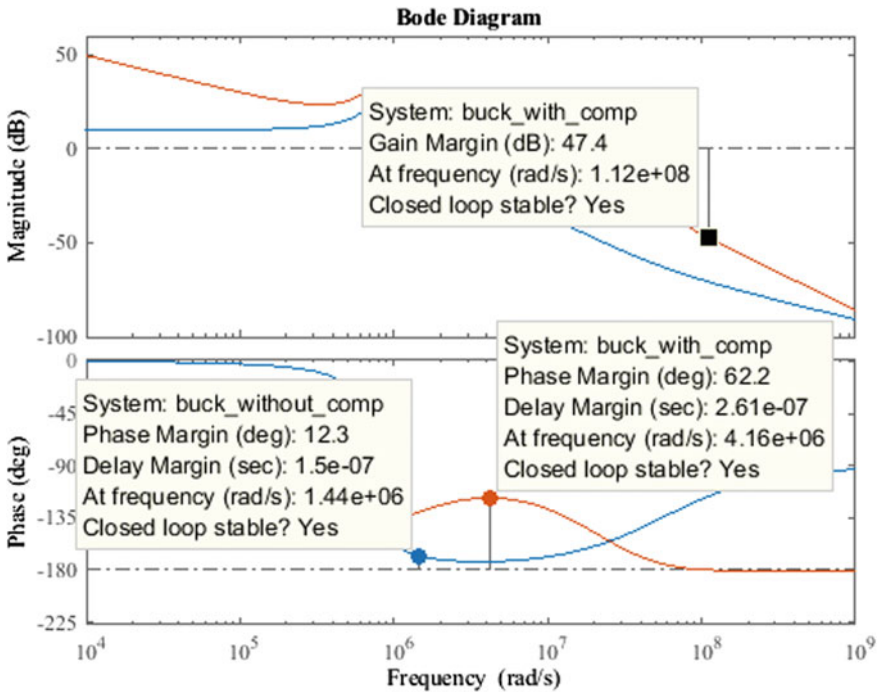


Fig. 4 Bode plot for buck converter with type III compensator

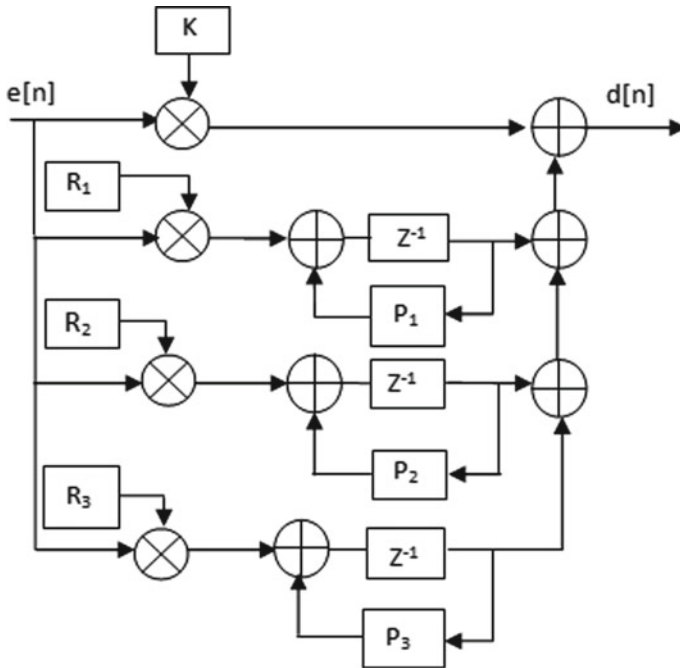


Fig. 5 Type III compensator architecture

losses and increases the efficiency under light load condition. The PFM converter circuits do not require loop compensators and hence they are simple and easy to design. Digital PFM architecture is implemented using a hysteretic comparator which compares the output voltage with upper and lower threshold voltages to control the ON–OFF of the power MOSFET switches. A zero inductor current detector algorithm is implemented to prevent negative inductor current. Figure 6 shows the DPFM architecture.

5 Results and Its Analysis

The hardware–software co-simulation of digital power supply regulator is performed in the MATLAB/Simulink environment using the Vivado system generator tool to validate the design. The co-simulation is carried out with type III compensator, 13-bit $\Sigma-\Delta$ DPWM and digital reference voltage with soft start in PWM mode of operation to analyze its performance under various load and line transient conditions. The power supply module operates under PWM mode of operation during medium and heavy load conditions and under PFM mode of operation during light load conditions (<0.1 A) to obtain good efficiency. Figure 7 shows the digital power supply regulator

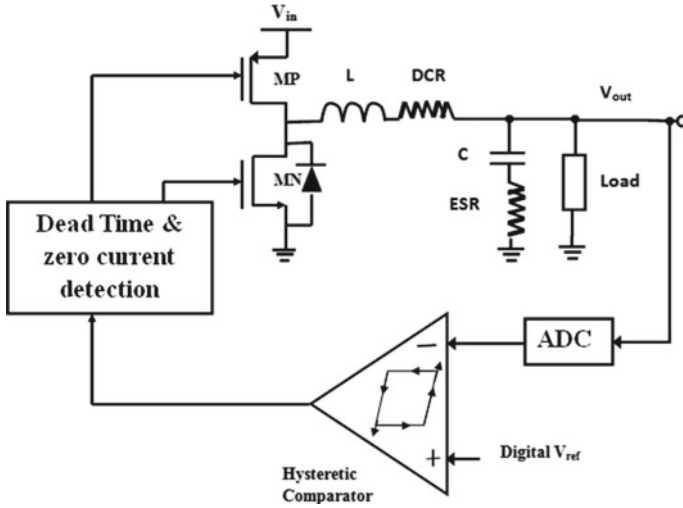


Fig. 6 The architecture of hysteresis DPFM control

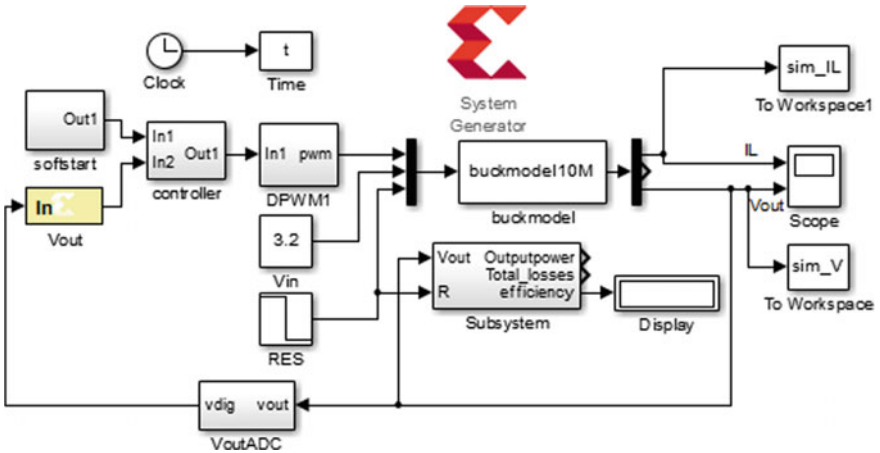


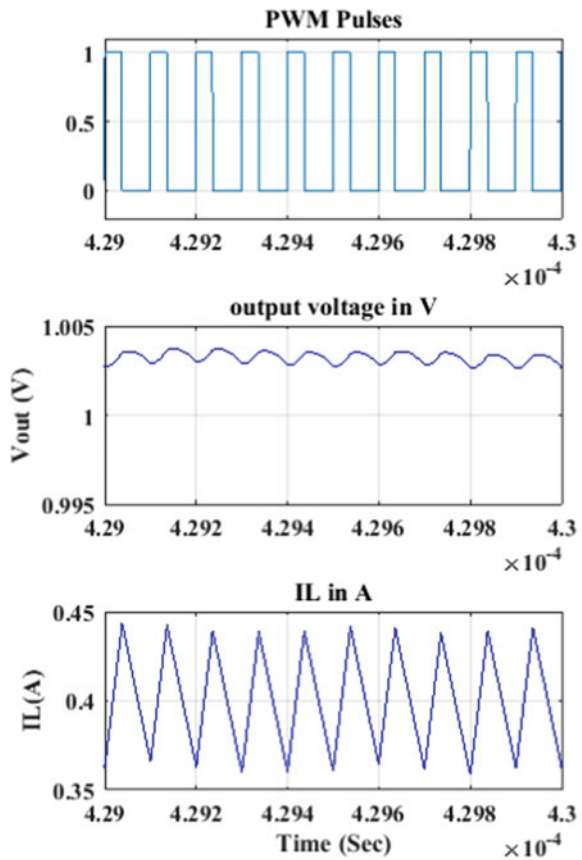
Fig. 7 The hardware–software modeling of a digital power supply regulator

hardware/software model in the Simulink environment.

5.1 Static Performance Analysis

The performance of the buck switching mode power supply under various load conditions for three different input voltage conditions are analyzed and results are tabulated. Figure 8 shows the PWM pulses, output voltage and inductor current at a load current of 0.4 A. It is observed that the output voltage obtained is 1.0024 V, the ripple content in inductor current is between 70 and 85 mA and ripple content in output voltage is 0.8 mV. Figure 9 shows the plot of output voltage against various load conditions for three input voltages ($V_{in} = 3.2, 2.5$ and 1.8 V). The average accuracy of 0.24% is obtained which is within the limit of the desired accuracy of 1%.

Fig. 8 PWM pulses, output voltage and inductor current response when the load current is 0.4 A



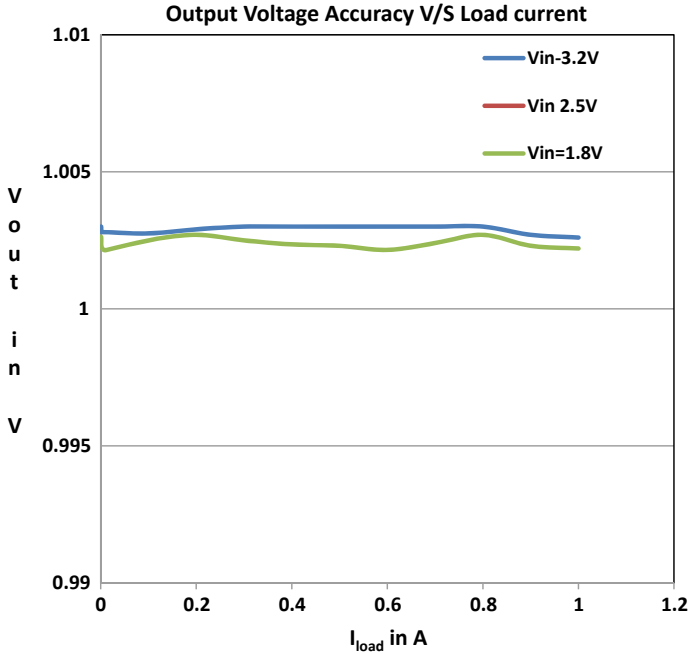


Fig. 9 Output voltage accuracy versus load current

5.2 Dynamic Performance Analysis

The dynamic performance of digitally controlled switching mode buck converter for different load and input battery voltage variations is analyzed, compared and the results are tabulated.

Figure 10a shows the load transient, output voltage and inductor current when load conditions change from 150 to 400 mA and vice versa. It is observed that undershoot in output voltage when the load varies from 150 to 400 mA is 30 mV and overshoot when the load varies from 400 to 150 mA is 32 mV. The % peak overshoot/undershoot is around 3%. The response time of the power supply when load variations occur (150–400 mA and vice versa) is 3 μ s. The steady-state output voltage is 1.002 V. Figure 10b shows the output voltage transient response when the input battery voltage is varied from 2.5 to 3.2 V and vice versa. The undershoot and overshoot in output voltage are 20 and 25 mV, respectively. The time taken by the power supply to settle to a steady value of 1.0025 is 10 μ s.

The DPFM mode of operation is used to improve the efficiency under light load condition. In this paper, the DPFM mode of operation is chosen to load current values of <0.1 A. Figure 11 shows the %Efficiency versus load current in DPFM mode of operation. The minimum efficiency obtained is 66.62% at 0.001 A. Figure 12 shows the power conversion efficiency for forced DPWM and DPFM mode of operation.

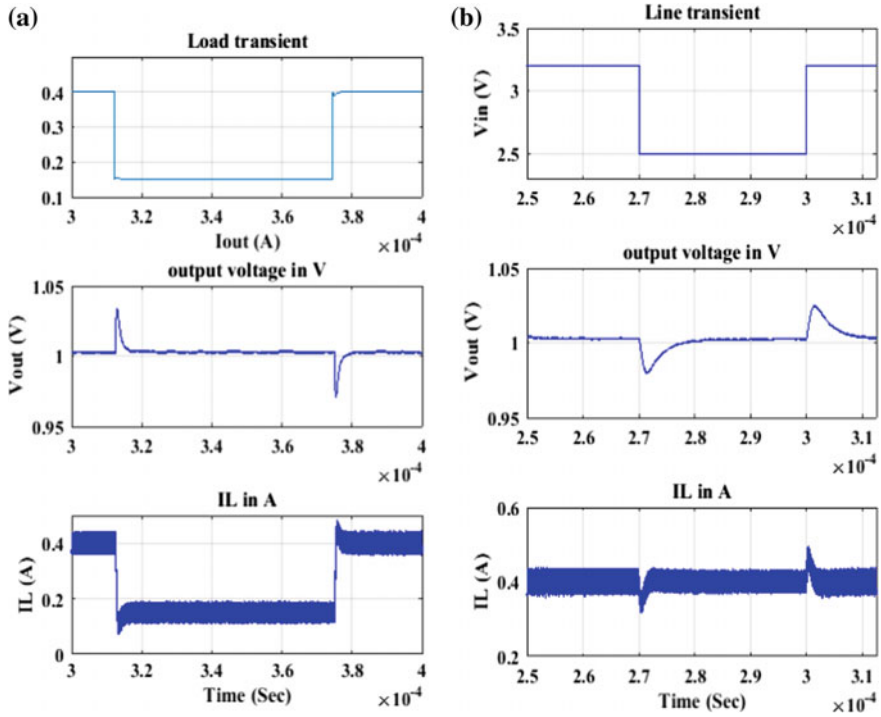


Fig. 10 a Load transient response for load variations of 150–400 mA and vice versa. b Transient response for an input battery voltage change of 2.5–3.2 V

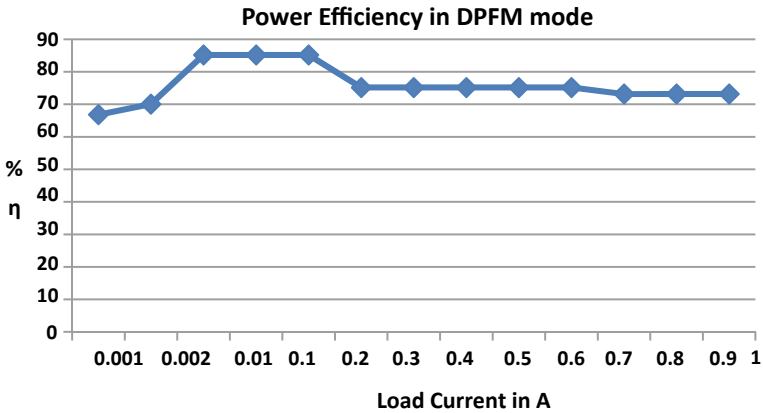


Fig. 11 Power efficiency versus load current for DPFM mode of operation

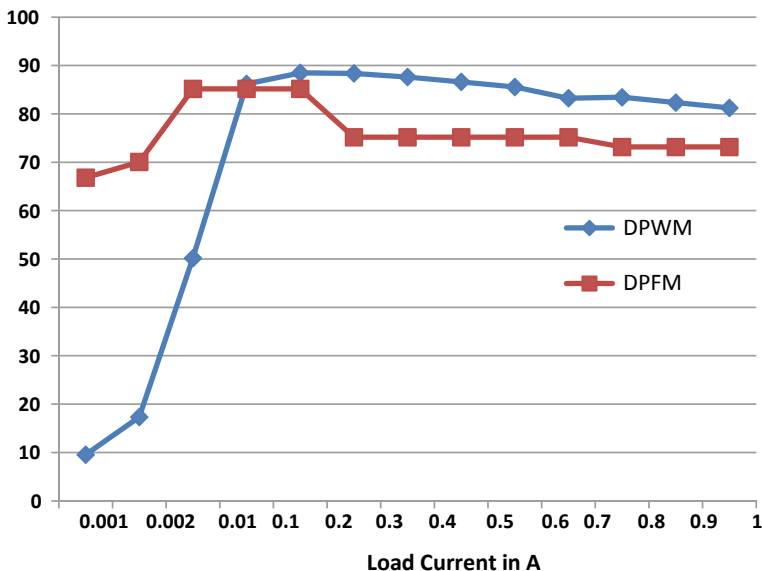


Fig. 12 Power efficiency versus load current for DPFM and DPWM mode of operation

The DPFM has a much higher efficiency of 66.82–85% for load currents <0.1 A. The forced DPWM has a power conversion efficiency of merely 10% at 0.001–86% at 0.1 A. Hence power supply circuitry is operated in DPFM mode of operation for load currents <0.1 A.

6 Conclusion

A multi-mode digitally controlled switching mode buck converter is implemented to power system-on-chip (SoC). It operates in DPWM mode under heavy and medium load conditions, whereas in DPFM mode under light load conditions to obtain high power conversion efficiency over a wide range of load current. Maximum efficiency of 88.48% is obtained at 0.2 A under PWM mode of operation. An output voltage accuracy of 0.25% is achieved against a target value of 1%. The load current and line voltage transient responses are verified by considering the different range of load current and line voltage variations. Light load or power save mode efficiency is improved by using a DPFM mode of operation. The minimum efficiency obtained is 66.62% at 0.001 A. The %Efficiency lies between 66.62 and 85% for a load current range of 0.001–0.1 A. The voltage ripples during DPFM mode of operation are observed to be 3 mVpp, which is within the desired value of 10 mVpp.

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