Design of Reversible Binary-to-Gray Code Converter in Quantum-Dot Cellular Automata

I. Gassoumi, L. Touil and B. Ouni

Abstract At nanoscale, for digital systems, the device density and power constraint of the circuit are essential issues. Quantum-dot cellular automata (QCA) is an incipient nanotechnology, which leads to build circuits at nanoscale. It offers various features such as minimal power dissipation, very high-operating frequency, and nanoscale feature size. Besides, reversible computation can lead to the development of low-power systems without loss of information. Thus, reversible QCA logic can provide a powerful and efficient computing platform for digital applications. This paper presents a QCA code converter. Feynman gate is used as a fundamental building block to perform the proposed design of code converter. QCADesigner version 2.0.3 is used to validate the accuracy of the proposed circuit. QCAPro, a very widespread power estimator simulation engine, is applied to estimate the power depletion of the proposed circuit.

1 Introduction

The thermal energy discharged by circuit transistors is one of the most important issues faced while designing VLSI circuits. Although the recent VLSI technology is based on CMOS technology. However, this technology entails many challenges. High-power density levels, high leakage currents, and constraint of speed in GHz are some of the problems that CMOS is faced [1, 2]. In the 1960s, Landauer proved

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that if information processing has performed at an irreversible process, then energy will be lost and a loss of information leads to loss in energy [3]. It has proved that the loss of any bit of information would be at least 0.6931 KbT joules, where T is the temperature of the environment in which computation is performed. These truths lead to look beyond traditional approaches in order to reduce the power depletion. Hence, various alternative technologies were found like Carbon Nanotube Field-effect Transistors (CNTFET), Single-electron Transistor (SET), and Resonant-tunneling Diodes (RTD) [4].

QCA is an incipient nanotechnology and potential substitute to orthodox CMOS archetypes at nano extent that assures to conceive digital circuits with minimal power, extreme speed, and particularly dense structures. This approach can operate at a higher frequency (in the order of THz) than the conventional solution [5–7]. Apart from that, reversible approach is also considered as an alternative technology that can mitigate the issues, which are anticipated for CMOS devices due to the heat dissipation [8, 9]. A system is reversible if its output values define its input values, i.e., it performs a bijective function. The inputs may be reproduced from the outputs and vice versa. Thus, without wasting of information, no energy dissipation occurs. This design strategy aims toward the development of digital designs with ideally zero power dissipation. Then, the design of reversible logic circuits used in this new emerging nanotechnology (QCA) leads to ultra-low-power systems and architectures. Reversible QCA logic can provide high-performance and low-power solutions for digital designs. Recently, it is used as the best method to reduce power depletion [10–15]. As well known that the fundamental components of each logic circuits are logic gates which are used to perform any Boolean functions. Thus, reversible circuits can easily be realized that can perform complex logical and arithmetic operations using reversible logic gates. Some gates have been employed by several reversible logic designs such as Feynman, Fredkin, and Toffoli gates. In recent years, several efforts have been made toward to conceive of reversible QCA digital circuits [16–18].

This chapter describes the design of reversible binary-to-gray code converter in QCA. The basic building block of the proposed design is Feynman gate. In this chapter, the major contributions of our work can be summarized as follows:

- A novel reversible Feynman gate (FG) based on QCA technology has been proposed.
- The proposed FG has been exploited to realize the design of reversible code converter circuit in QCA technology.
- The simulation results of the designed circuit have been correctly obtained.
- Power dissipation of the proposed design has been estimated.

The rest of this work is systematized as follows: Sect. 2 reviews the QCA technology. Section 3 presents the background work. The designed circuit is discussed in Sect. 4. Section 5 shows the performance comparisons with power depletion analysis. Finally, the chapter is concluded in Sect. 6.

2 Background

2.1 QCA Devices

The QCA approach is an emerging technology designed as an appropriate alternative to conventional technology. It contains an array of cells. Cells in the QCA technology include four cavities located in four corners of the square. Only two electrons diametrically opposite are injected into a cell due to Coulombic interaction [19]. Through Coulombic effects, two possible polarizations (labeled –1 and 1) can be shaped. These polarizations are represented by binary "0" and binary "1" as depicted in Fig. 1. Figure 2 illustrates the propagation of logic "0" and logic "1", respectively, between input and output in QCA binary wires due to the Coulombic repulsion. Generally, in neighboring cells, the Coulombic interaction between electrons is used to implement many logic functions, which are controlled by the clocking mechanism [20].

The main logic components in the QCA technology are majority and inverter gates, which are composed by some QCA cells as depicted in Fig. 3 [21, 22]. The 3-input majority voter consists of five QCA cells. Furthermore, the majority gate and inverter are operated for realizing QCA circuit performances. A majority gate can operate a 3- or 5-input logic functions as presented in Fig. 3.

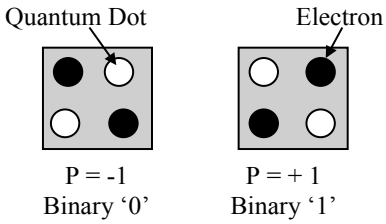

Fig. 1 Two different polarization of quantum-dot cell

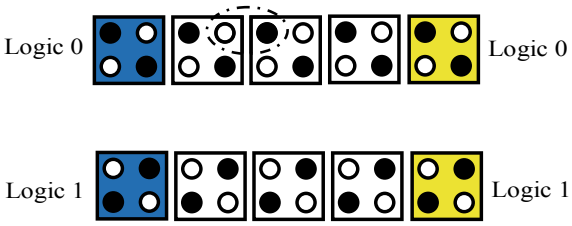

Fig. 2 QCA binary wire

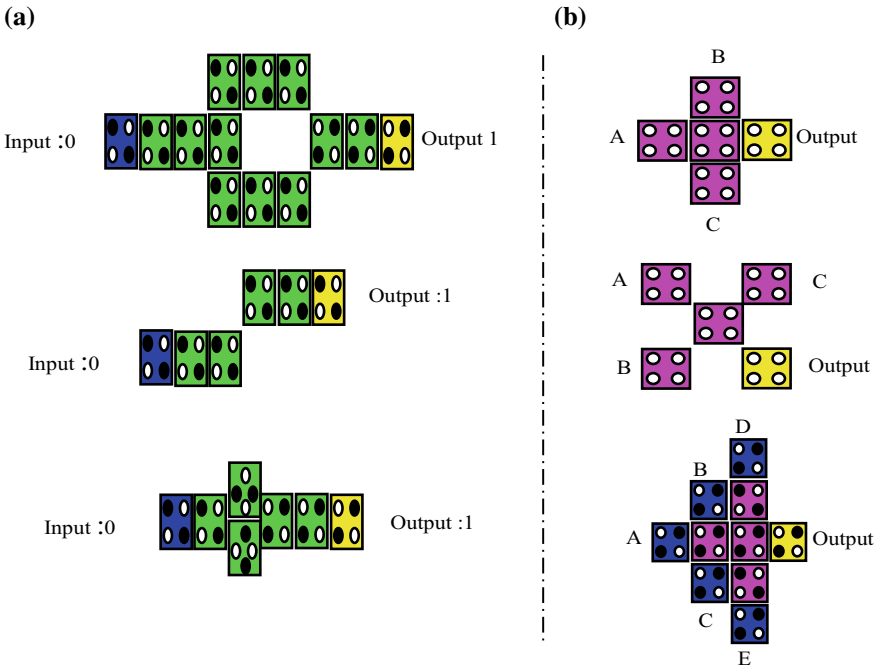

Fig. 3 **a** Types of inverter gate, **b** majority gate

2.2 *QCA Clocking*

Clocking plays an important role in QCA designs. Every single clock has four periods, namely, switch, hold, release, and relax, which are essential for appropriate circuit implementations as illustrated in Fig. 4 [23, 24].

- In switch phase, QCA cell is beginning to shift from unpolarized status to polarize status, and the blockades of the dots are lifted.
- In hold phase, blockade of the cell is in the highest value, electron cannot channel within dots, and cell preserves their existing statuses specifically, stable polarization.
- In release phase, the blockade is lessened, electron can channel within dots, and statuses of the cell turn into unpolarized.
- In the final phase, blockade stays lessened and cell remains in unpolarized status.

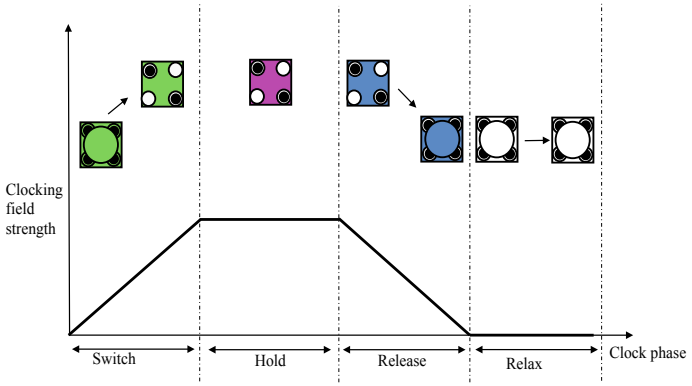

Fig. 4 QCA clock zones

3 Feynman Gate

The reversible designs are one of the most promising solutions, which are capable of overcoming the limitations of the applications based on the CMOS technology. Additionally, reductions in energy dissipation comprise one of the important goals of nanotechnology-based methods, including QCA and so it is desirable to consider reversibility in the design of QCA circuits. The Feynman gate (FG) is employed by many reversible logic circuits. It is a 2 × 2 universal gate (Fig. 5) and any logical reversible design can easily be implemented by using it. The FG is named as a self-inverse one, i.e., to a circuit that is capable to return to any previous state in reverse order. The truth table of the Feynman gate is shown in Table 1. Figure 6 illustrates the proposed QCA design and the simulated outcome of Feynman gate.

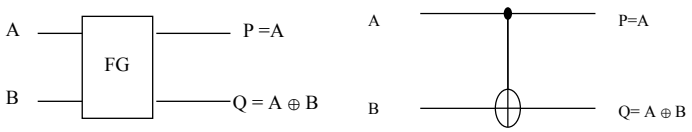

Fig. 5 Feynman gate and its quantum realization

Table 1 Truth table of FG

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

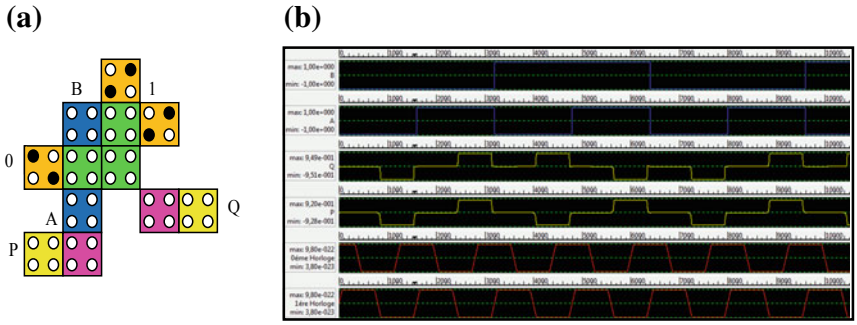

Fig. 6 **a** Proposed QCA layout of Feynman gate, **b** its simulation outcome

The proposed Feynman gate contains 12 QCA cells and covers an area of 0.01 μm^2. Here, the suppression of majority voter leads to QCA structures with less power consumption and hardware complexity.

4 Reversible Binary-to-Gray Code Converter

In this section, a new reversible code converter design by using QCA is explored. A binary-to-gray Code converter is a combinational circuit which is a non-weighted code. This conversion method is useful to reduce the rapid switching activity. In order to generate the 3-bit binary-to-gray code converter, only two FGs have been used. The corresponding block representation and QCA diagram of the proposed circuit is depicted in Figs. 7 and 8, respectively. It has one garbage bit. The proposed design contains 29 cells, extent 0.04 μm^2. It needs two clock zones to generate the correct outputs.

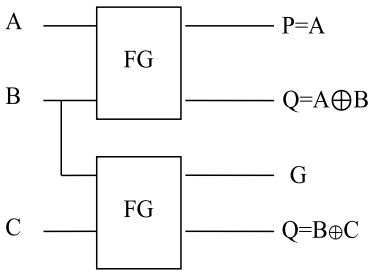

Fig. 7 Schematics of 3-bit reversible binary-to-gray code converter

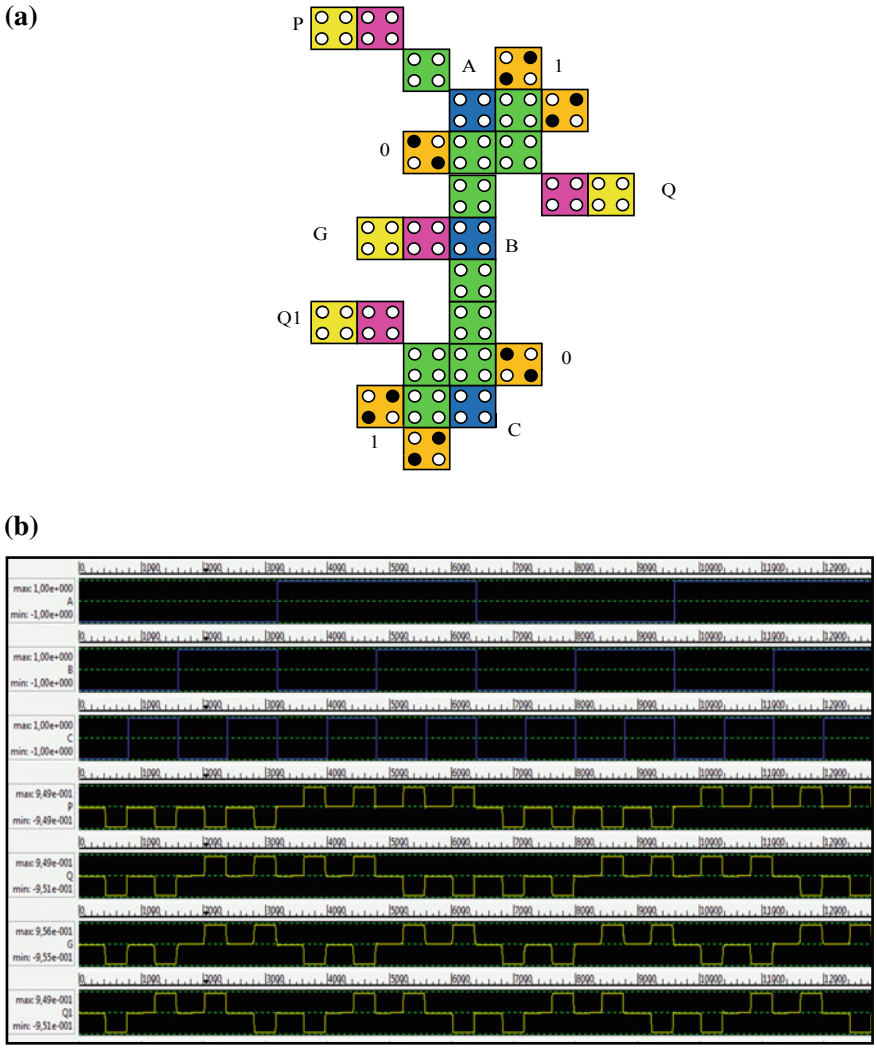

Fig. 8 **a** QCA layout of 3-bit reversible binary-to-gray code converter, **b** its Simulation outcome

5 Results and Discussions

QCADesigner software is used to verify and simulate the proposed hardware design [25]. The utilized parameters for the simulation are shown in Table 2. The Feynman gate is the basic building blocks of the proposed circuit. Therefore, the foremost benefit of the designed gate is that no multilayer and rotating crossing is applied, which will lead to the efficient design of reversible binary-to-gray code converter. Table 2 illustrates the comparison result of the designed gate (FG) with some

Table 2 Simulation parameters

Parameter	Value
Number of samples	12,800
Convergence tolerance	0.001000
Radius of effect	65,000,000 (nm)
Relative permittivity	12,900,000
Clock low	3,800,000e-023(J)
Clock high	9,800,000e-022(J)
Clock shift	0,000,000e + 000
Clock amplitude factor	2,000,000
Layer separation	11,500,000
Maximum iterations per sample	100

existing designs in the literature. It can be perceived that the proposed gate excels all the best reported designs presented in [26]. Table 3 depicts the quantum cost (QC) of the suggested circuits. Clearly, the QCA designs have less QC than that of classical implementation as shown in Table 4. In addition, the proposed design consists of 29 cells, occupies 0.04 μm^2 area and 0.5 latency. The QCAPro software, a probabilistic designing engine [27], has been applied for power depletion study.

Table 3 Comparison of various Feynman gates

Design	Cell count	Area (μm^2)	Clock no. cycle
Feynman gate [11]	54	0.037	0.75
Feynman gate [14]	43	0.038	0.75
Feynman gate [15]	13	0.02	0.5
Feynman gate [26]	14	0.01	0.5
Proposed Feynman gate	12	0.01	0.5
3-bit reversible binary-to-gray code converter [28]	118	0.0926	4
3-bit reversible binary-to-gray code converter [29]	117	0.0953	10
3-bit reversible binary-to-gray code converter [30]	75	0.0554	4
Proposed binary-to-gray code converter	29	0.04	0.5

Table 4 Quantum cost of the proposed reversible sub-circuit versus corresponding QCA layout

Proposed reversible circuit	Quantum cost	Quantum cost of QCA circuit (area. $latency^2$)
Feynman gate	1	0.0025
Reversible binary-to-gray code converter	2	0.01

Table 5 Power dissipation analysis of the proposed circuits

Proposed QCA circuit	Dissipation of power T = 2.0 K		
	γ = 0.5 Ek	γ = 1 Ek	γ = 1.5 Ek
Feynman gate	9.55	15.76	22.73
Reversible binary-to-gray code converter	19.39	31.52	45.98

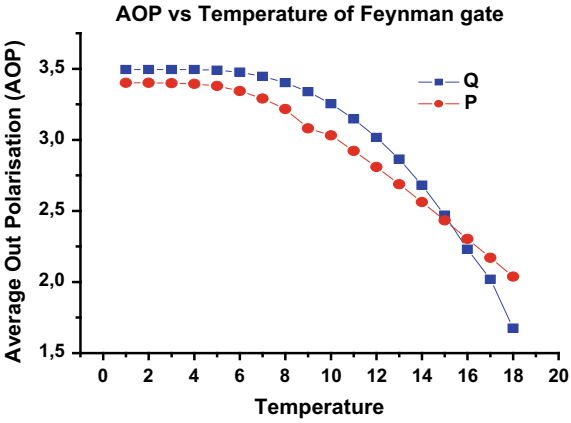

Fig. 9 The effect of temperature on output polarization of Feynman gate

Table 5 explains the overall power depletion study of the proposed design. The estimation is performed at three tunneling energy levels (EK) at T = 2 K. The temperature impact on the output polarization of designed gate is performed. The proposed diagram function readily in the temperature range of 1–6 K, and the AOP for each cell is reformed very little in this estimate as demonstrated in Fig. 9, which is analyzed at different temperatures by QCADesigner Tool.

6 Conclusion

Recently, QCA technology has attracted researchers' attention for implementing reversible computing. Reversible QCA logic has become a promising technology in the implementation of digital design. In this chapter, we have presented a QCA architecture based on reversible logic, which performs binary-to-gray code converter. Feynman gate is used to achieve the proposed design. The results of the comparison demonstrated significant improvements. The designed circuit is more efficient in terms of extent, cell complexity, quantum cost, and delay.

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