Robust SRAM Cell Development for Single-Event Multiple Effects

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Abstract. As the transistor size scales down exponentially to Nanometric dimensions, the susceptibility of electronic circuits to radiation increases drastically. Static-Random-Access Memories (SRAMs) are applicable in the areas of aerospace and space applications where their performance must meet the increased data rates and must be resilient to radiation exposures to guarantee reliability. Therefore, development of resilient SRAM is a challenging and demanding problem. In this paper a robust 10T SRAM (RHD10T) is proposed and compared with the existing radiation hardened (rad-hard) SRAM circuits. The proposed RHD10T SRAM is more robust towards Single Event Multiple Effects (SEME's) compared with the recently published literature. Further, it takes 29% lesser area with respect to the standard DICE cell. In contrast to latest rad-hard SRAM cells, the proposed RHD10T cell is delivering 99.8% less failure probability for the applied charge distribution. Process variations (PV) show least effects when compared to 6T SRAM cell.

Index Terms: Single event upset · Radiation hardening · Single-Event Multiple Effect (SEME) · Robust SRAM cell

1 Introduction

Soft errors induced by radiation, threats the basic functionality of logic cells. A high energetic ionized particle, when crashes with a memory cell, changes the stored logic resulting in the bit flip. This circumstance is defined as a Single Event Upset (SEU) [1]. Static Random-Access Memories (SRAMs) are more vulnerable to these radiations induced SEUs. As the CMOS technology scales down, there is an increase in the susceptibility of memory cells to the induced soft errors which kindles the new concerns like Single Event Multiple Effects (SEMEs) [2–4]. SEMEs are of serious issue in safety and critical applications like aerospace and space navigation [5]. In SEMEs when an ionized particle strikes the node of robustious SRAM like DICE cell [6], more than one node will get affected resulting in the bit flip. Different system level strategies like error detection and correcting codes have been suggested in the literature to get rid

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of multi-bit flips [7], which doesn't highlight reason behind the bit-flip. In these system level techniques, authors have expected ionized particle hit results in one or more upsets and further they are not interested by what means a radiation hit results an upset in a SRAM cell. In circuit level strategies, design engineer, emphases on resilient memory cells in which a radiation strike hitting several nodes of the cell will not result in a bit flip. This work presents a circuit level strategy to tackle SEME. According to the recent research and study, little effort in design of SEME resilient SRAM cells was carried out [2, 8]. In cache memories where performance, power consumption and cell area are important features, SRAM cells are used. Using system level strategies like correcting codes and fault design of VLSI circuits [9] on the speed and power consumption of RHD10T and 6T SRAM cells. The paper outline is as follows: Sect. 2 comprises an explanation of model for a SEU and former rad-hard SRAM cells. In Sect. 3, working of robust rad-hard SRAM cell (RHD10T) is presented. In Sect. 4, analysis of SEU, SEME robustness of proposed and considered cells for comparison is presented. In Sect. 5, overheads of RHD10T SRAM cell in contrast to recently published rad-hard SRAM cells are presented. In Sect. 6 PV analysis and its discussion is presented. Finally, Sect. 7 consists of conclusion.

2 Introduction to of Radiation Effects

2.1 SEU and Critical Charge

The minimum charge needed to alter the stored state of any logic circuit is known as the Critical Charge (Qcrit) [4, 5]. The moment, charge at the radiation affected node of SRAM cell exceeds the Qcrit, an SEU occurs. The model of the charge induced by the radiation strike is double exponential current pulse [9] and applied by numerous researchers [2, 3, 5]. Equation (1) shows the mathematical equation of double exponential current pulse.

$$I_{inj}(t) = \frac{Q_{inj}}{T_1 - T_2}\left(e^{\frac{-t}{T_1}} - e^{\frac{-t}{T_2}}\right) \tag{1}$$

Here, the Qinj is the quantity of imparted charge in the hit area. In Eq. (1), τ1 as well as τ2 are material reliant time constants [9]. 1/τ1 is the accumulation time constant of the node. We can calculate τ1 as shown in Eq. (2) [10]. It depends on doping concentration of silicon substrate (ND). We presumed the value of τ2 as 5×10^{-11} s in (1) and is insignificant in comparison to τ1 [5, 11, 12]. In (1), Iinj is the quantity of charge we injected as SEU for the targeted junction. To introduce the effect of ionized particle strike at a junction, we attach a current source [specified by (1)] to that junction.

$$\frac{1}{T_1} = \frac{K\varepsilon_0}{q\mu N_D} \tag{2}$$

Similar to [3, 4, 8, 13] for a radiation strike that disturbs two neighboring junctions, we used two current sources one at each junction.

2.2 Previous Work

Author in [14] showed RHD13T SRAM is more robust towards SEU's and SEME's than 13T and 11T in [8, 11] respectively. He also displayed low area overhead of RHD13T SRAM over dice cell [6], 13T and 11T. RHD13T cell has more shared critical charge over 13T SRAM cell. Still, the disadvantage of RHD13T is it cannot tolerate an SEME. Author in [15] proposed AS8 SRAM cell and displayed increase in its critical charge when compared to 6T SRAM. The disadvantage of AS8 is its inability to withstand radiation strikes in its two nodes. Authors in [6] proposed 12 transistors SRAM namely DICE cell, which is successful in with standing SEU but is unable to hold data in the presence of SEMEs. To address SEME we proposed a 10 transistors SRAM cell namely RHD10T in this paper. By understanding the withstanding ability of RHD10T SRAM over radiation induced current pulse we will be able to classify the difference between proposed and standard 6T SRAM.

3 RHD 10T SRAM Cell

As SRAM memories must be fast and consume small area, the radiation hardened SRAM cells that involve high penalty of area and performance would not be widely applicable. Also, until SRAM connects to power supply, it preserves the data stored in it. Working of the proposed RHD10T SRAM cell is same as conventional 6T-SRAM cell. Our proposed rad-hard SRAM cell consists of ten transistors. The basic latch of the circuit which preserves the data is the entire circuit, apart from transistors Xn5 and Xn6. The latch consists of four CMOS inverters whose arrangement is as shown in Fig. 1(a). Word Line (WL) is the control for access transistors Xn5 and Xn6. Figure 1 (a) shows the output of two inverters formed by Xn1, Xp1 and Xn2, Xp2 are at NODE1, their input at NODE2. And, output of another two inverters formed by Xn3, Xp3 and Xn4, Xp4 are at NODE2 and their input at NODE1. This forms a feedback, which strengthens the inverters to their respective states. The access transistors bit line (BL), bit line bar (BLB) and WL are used to read and write, from and to the cell. In idle state WL will be at low, making access transistors off, in this state NODE1 and stronger therefore they can switch the inverter transistors. Disabling access transistors concludes writing the SRAM. Figure 1(b) shows write '1' and write '0' operations performed for RHD10T SRAM cell. Pre-charging the BL and BLB to Vdd and applying a high pulse on WL begins reading the SRAM. A non-zero current starts flowing into BL or BLB through access transistor and ON state pull down transistors, (through a node which holds logic zero). This current leads to a voltage drop in the bit-line whose access transistor end is storing a logic low value. But, the bit-line whose access transistor other end stores Vdd, experiences no drop-in voltage from pre-charged voltage. This result in voltage difference in bit-lines, using which sense amplifier identifies the data stored. By running HSPICE simulations of proposed and recently published rad-hard SRAM cells and after analyzing the simulations, results are shown in next section. RHD10T SRAM cell is a SEU-resilient compared to other previously proposed rad-hard cells. However, like all other estimated SRAM cells, RHD10T SRAM cell could not with stand the radiation strikes affecting two junctions. If a high intensity radiation strike, disturbs the

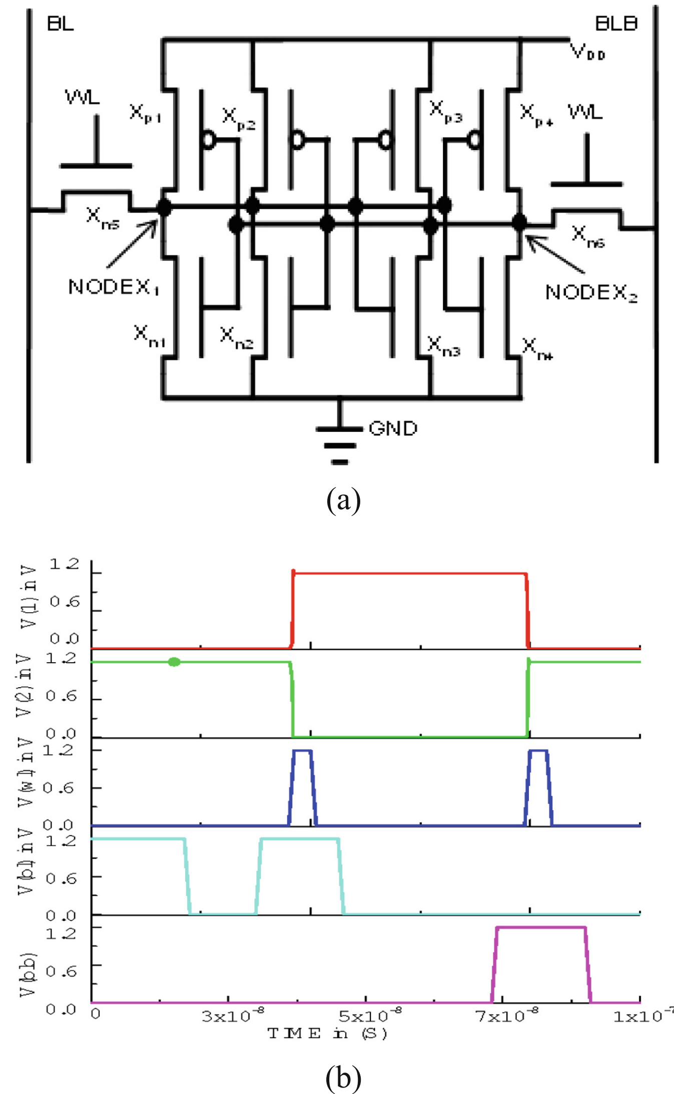

Fig. 1. RHD10T SRAM cell: (a) circuit diagram; (b) normal operation diagram.

junction pair X1–X2 the stored value could be altered. The next section is displaying that our proposed rad-hard SRAM cell on contrast to recently published rad-hard SRAM cells is delivering higher critical charge that is greater immunity to voltage variations and transient noise. It is also displaying that our proposed SRAM cell is more SEMU tolerant than DICE cell. For RHD10T SRAM cell an increase in read delay by 9:8% and an increase in write delay by 6:1% compared to 6T SRAM cell were observed. Critical charge of the proposed rad-hard SRAM is more than recently proposed SRAM and is achieved at the cost of higher power consumption (as explained in

Sect. 4). For assessing RHD10T SRAM and other important rad-hard cells, we made a set of simulations. HSPICE is used to perform simulations of SRAM cells with PTM libraries [16]. We set the temperature to 25 °C and source voltage to 1.2 V. The objective of RHD10T SRAM is to increase the internal resistance towards the current pulse induced by radiation strike. Proposed RHD10T SRAM cell consists of two extra CMOS inverters in parallel to the existing inverters of 6T SRAM as explained in Sect. 3. Because of added inverter the node's capacitance increases which strengthens to uphold stored data by dragging the signal back to the initial state [15]. The critical charge at the node increases because of charge sharing by gates of added transistors. Now consider if radiation strikes occur at any reverse biased drain junction of the inverter of SRAM. The current pulse formed at the drain node of the radiation affected set of inverters of SRAM. At this stage, output of first set of inverters strengthens the corrupted data until settling at certain inappropriate state. If the critical charge of the SRAM cell is higher than the injected charge because of a particle hit, the induced glitch will disappear after the strike and the cell holds its original state [15]. Our method is strengthening the feedback mechanism, resulting in radiation hardened design by mitigating the corrupting affect because of an ionized particle strike. Thus, the influence of ionized particle strikes on our proposed SRAM is unresponsive and limited by added inverters.

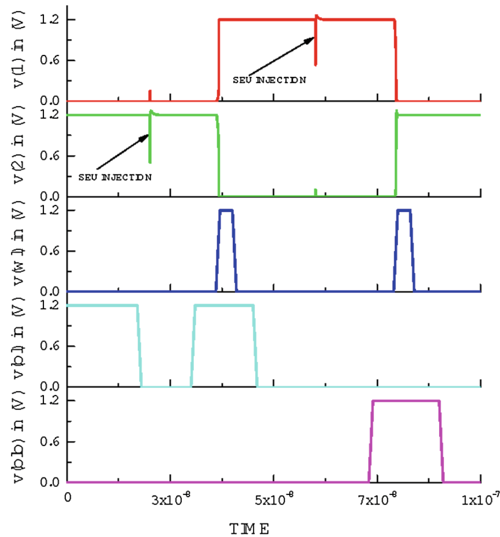

Fig. 2. SEU radiation strikes to nodes of RHD10 SRAM cell.

The smallest charge needed to alter the stored data will get increases in our proposed SRAM which boosts the resistance of SRAM cell against SE of inverters of SRAM. At this stage, output of first set of inverters strengthens the corrupted data until settling at certain inappropriate state. If the critical charge of the SRAM cell is higher

Table 1. Critical charge of various susceptive nodes

Technology	65 nm		
SRAM type	Node	SEU critical charge in femto coulomb	SEME critical charge in femto coulomb
6T	X1	18.729(1)	15.8156
	X2	18.729(1)	15.8156
AS8 [14]	X1	18.729	15.8156
	X2	35.7932	30.042
RHD13T [15]	X1	10.8212	8.831
	X3	24.5	19.43
	X4	26.63	20.049
Proposed	X1	37.0418(1)	31.215
	X2	36.6256(1)	31.215(1)
DICE [06]	X1	-	16.648(1)
	X2	-	16.648

than the injected charge because of a particle hit, the induced glitch will disappear after the strike and the cell holds its original state [15]. Our method is strengthening the feedback mechanism, resulting in radiation hardened design by mitigating the corrupting affect because of an ionized particle strike. Thus, the influence of ionized particle strikes on our proposed SRAM is unresponsive and limited by added inverters. The smallest charge needed to alter the stored data will get increases in our proposed SRAM which boosts the resistance of SRAM cell against SEU.

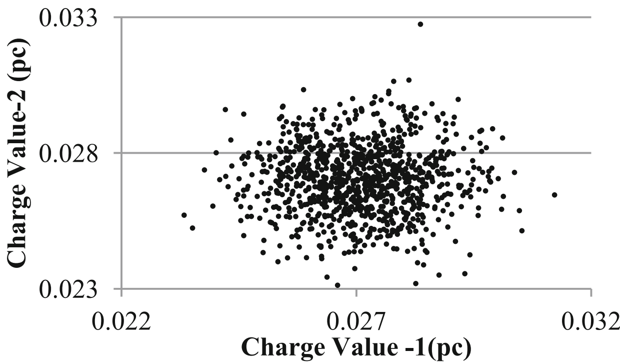

Fig. 3. 1000 randomly sample charge pairs used foe Monte Carlo simulation from normal distribution

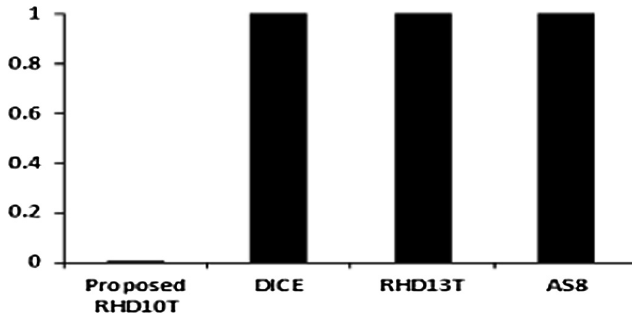

Fig. 4. Evaluation for probability of failure of SRAM cells in existence of SEME for charge distribution shown in Fig. 3.

4 Evaluation

4.1 Single Event Single Node Effect

To study SEU resilient ability of RHD10T SRAM and other rad-hard SRAM cells, we introduce transient faults (model discussed in Sect. 2.1) to drain nodes of inverter which holds logic high. Based on the displayed results in Fig. 2 we can state that, RHD10T SRAM is accepting high-power radiation hits to any of its junctions. Table 1 displays an assessment of critical charges of nodes of our proposed cell and other rad-hard SRAM's like RHD13T, RHD11T and DICE cell. We can identify from Table 1 that critical charge of RHD10T SRAM cell is higher compared to the recently proposed rad-hard cells.

4.2 Single Event Multiple Node Effects

To examine and compare the Single Event Multiple Effect tolerance ability of RHD10T SRAM cell with other RHD SRAMs, we introduce double exponential current pulses into two sensitive nodes (critical pair). We found the sensitive node pairs by introducing SEU injections to all probable junction pairs. Assessment of the critical charges of sensitive node pairs of RHD10T SRAM cell in contrast to other considered RHD SRAM cells is shown in Table 1. From Table 1. we can conclude that Dice cell is purely SEU tolerant but is not SEME tolerant. The critical charges for primary and secondary nodes of any other SRAM cell is clearly much lesser than RHD10T, which states that RHD10T cell is more robust towards SEMEs. As shown in simulation results, RHD10T SRAM cell displays significantly greater strength against SEME compared with former rad-hard SRAM cells. Also, our projected SRAM displays reasonably higher robustness than the RHD11T and RHD13T cells. We planned Monte Carlo (MC) simulations for a quantitative investigation for SEME tolerance ability of the rad-hard SRAM cells. 1000 randomly generated charge pairs from two normal distributions will be using as radiation strike induced deposited charges in MC simulations. A charge pair thus created is applied on identified sensitive nodes pairs

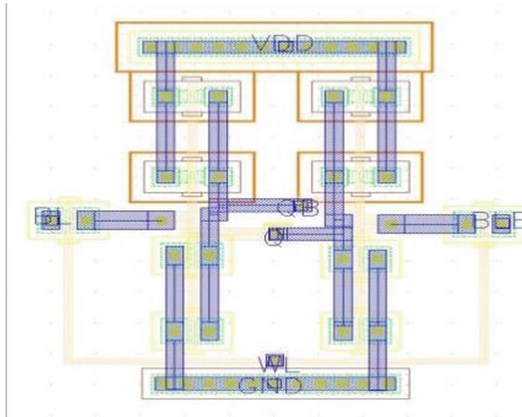

Fig. 5. Layout of RHD10T SRAM cell

(primary and secondary nodes) of SRAM cells. For the circuit under simulation, selecting the node pairs is done from the sensitive nodes identified in previous section. To find the Probability of Failure (POF) for the SRAM under simulation the numbers of bit flips for each simulation were counted. Figure 5 displays the layout of our aimed rad-hard RHD10T cell. In [17–19], particular approaches for increasing the robustness of the rad-hard SRAM cell with respect to SEMEs in layout level are recommended. Like in [17], by keeping enough distance among sensitive junction pairs, when the primary junction is struck by the radiation, possibility of consequential effects at secondary junction will be insignificant. Normal distributions displayed in Fig. 3. Were used for performing MC simulations. By noticing the MC simulation results, displayed in Fig. 4 for the applied charge distribution in Fig. 3 one can state that RHD10T delivers greater robustness to SEMEs when compared with former rad-hard SRAM cells. As in [17], the effects at secondary junctions can be minimized when a primary node is struck with a radiation hit, by keeping sufficient spacing between sensitive junction pairs. Figure 5 displays the layout of RHD10T cell. In [17–20], particular approaches for increasing the robustness of the rad-hard SRAM cell for SEMEs in layout level are recommended. Figure 6 shows the Static Noise Margins for SRAM's under simulation at various supply voltages. Static Noise margin is measure of SRAM's ability to tolerate noise voltages at the inputs of its inverters. RHD10T is delivering highest SNM than all the considered SRAMs after RHD13T. This indicates its noise withstanding ability.1000 randomly generated charge pairs from two normal distributions will be using as radiation strike induced deposited charges in MC simulations. A charge pair thus created is applied on identified sensitive nodes pairs (primary and secondary nodes) of SRAM cells. For the circuit under simulation, selecting the node pairs is done from the sensitive nodes identified in previous section. To find the Probability of Failure (POF) for the SRAM under simulation the numbers of bit flips for each simulation were counted. Figure 5 displays the layout of our aimed rad-hard RHD10T cell.

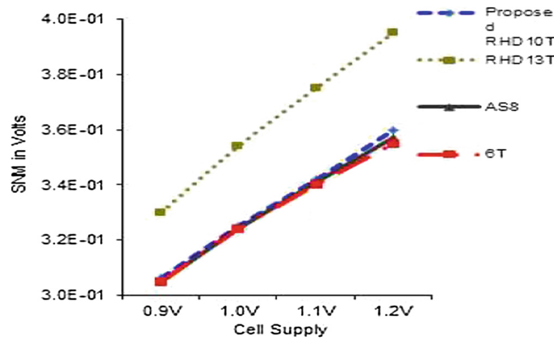

Fig. 6. SNM versus cell supply voltage

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Table 2. Comparative factors of SRAM Cells for 65 nm Standardized to 6T SRAM

	AS8	RHD 13	Proposed
Power	1.211	1.7121	1.676
Write delay	1.326	1.9653	1.061
Read delay	0.986	0.9194	0.902
PDP	1.398	2.4822	1.676
Area	1.124	1.88	1.24

5 Comparative Analysis

Reliability may be achieved at the cost of drop in speed, increase in area, and increased energy consumption. Also, SRAM memories are applied in many small budget applications for example cache memories. That is, strict constraints for energy-consumption;

speed and area are our main concern. We examined the 6T, RHD11T, RHD13T, DICE and RHD10T SRAM cells. By the attained results displayed in Table 2 about area overhead, we will state that, RHD10T SRAM cell occupies low area compared with considered rad-hard SRAM cells. Along with simulations in 65 nm, various available technologies were used for assessment and comparison of power and delay factors. Figure 7 shows results for 32, 45, 65 nm technology simulations.

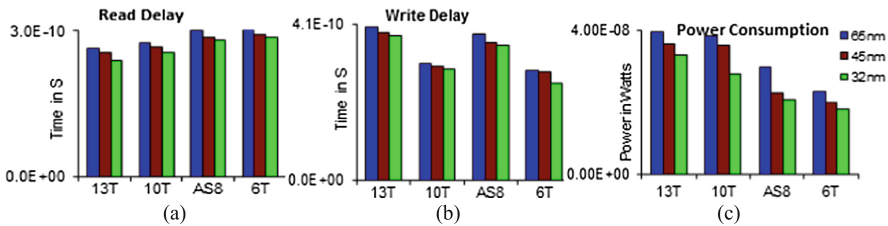

Fig. 7. Assessment for power and delay factors in different technologies: (a) read delay; (b) write delay; (c) power

6 Process Variations

The new challenge in design of VLSI circuits is their dependence on process variations. We assessed process variations effects on delay (average of write and read delays) and power consumption of RHD10T SRAM cell and compared with 6T SRAM cell. MC simulations were carried out on RHD10T SRAM cell and 6T to evaluate the process variation of design parameters. In the simulations performed, we applied a normal distribution for transistor dimensions (W/L) and threshold voltage (Vth. The performed simulations were carried out using Synopsys HSpice with 65-nm Predictive Technology Model (PTM) library [15]. Power consumption and delay (average of read and write delay) were evaluated for RHD10T and 6T SRAMs under process variations. We made 1000 MC simulations. 20% maximum deviation was allowed for W/L as well as for Vth. A normal distribution with maximum 20% deviation was allowed for each MC simulation, two values were allotted for every transistor for its Vth and W/L deviations. Figures 8 and 9 displays the effects of Vth and W/L variation on delay and power for 6T and RHD10T SRAM cells. In Fig. 8 the horizontal axis displays the variation of the maximum allowed deviation from original value. And vertical axis displays the effect of process variation on delay and power of the RHD10T and 6T SRAM cells in the associated set of MC simulations [21, 22]. Figures 8 and 9 determines that, process variation (on Vth and W/L) can impact both power consumption and delay of SRAM cells. Still, for all the circumstances, the sensitivities of RHD10T SRAM cells aren't higher compared to 6T SRAM cell.

In Fig. 8 average standard deviation of power consumption because of W/L variation, is 0.07 and 0.06 on 6T and RHD10T cells. This effect gets respectively 0.04 and 0.02 average standard deviation of delay for the mentioned cells. Also, in Fig. 9 the average standard deviation of power from the initial value resulted by Vth variation is

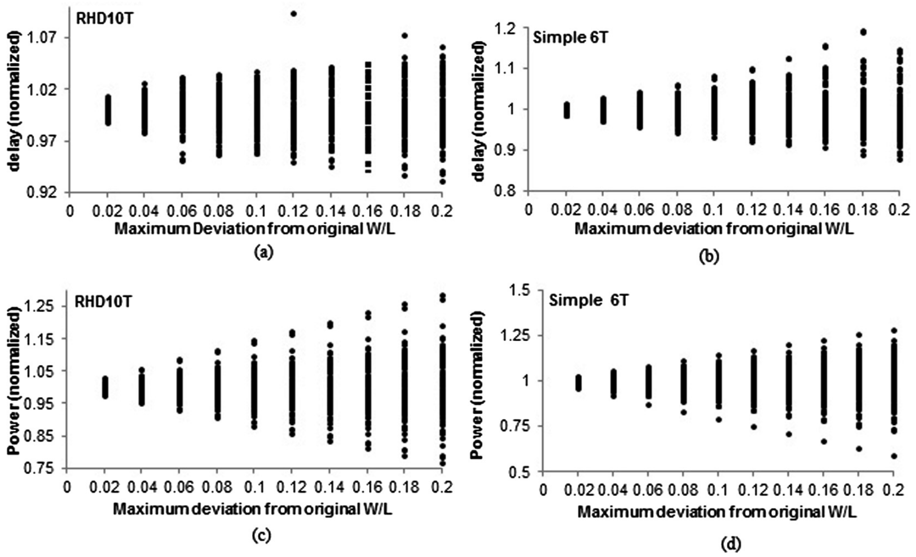

Fig. 8. Impact of WL variation on delay of (a) RHD10T SRAM, (b) simple 6T, and Impact of WL variation on power of (c) RHD10T SRAM, (d) simple 6T

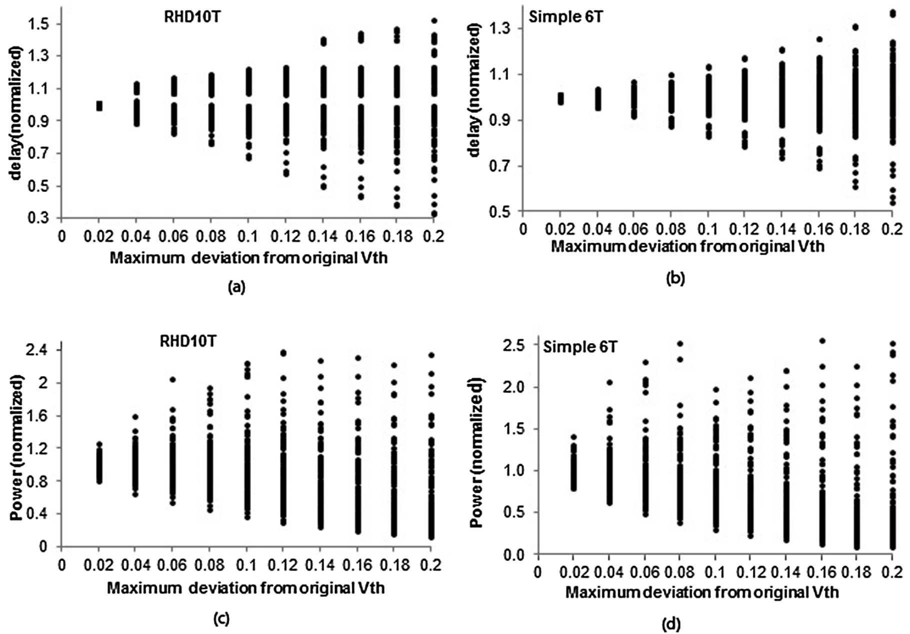

Fig. 9. Impact of Vth variation on delay of (a) RHD10T SRAM, (b) simple 6T, and impact of Vth variation on power of (c) RHD10T SRAM, (d) simple 6T

0.55 and 0.45 for 6T and RHD10T cells respectively. Also, the delay of 6T and RHD10T cells has an average deviation of 0.19 and 0.15 for Vth variations.

7 Conclusion

A new SRAM cell namely RHD10T is developed in this paper. After simulation, analysis and comparison of the proposed rad-hard SRAM cell and previous reported rad-hard SRAM cells we can conclude that our RHD10T cell is more robust towards SEU and SEMU by providing smaller area overhead.

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