



High-Speed Circuit Power Integrity Design Based on Impedance Characteristic Analysis

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Abstract. Power integrity (referred to as PI) issues have become increasingly important in today's high-speed circuit designs, at the same time, the complexity of power integrity analysis has increased. Based on the two-port network model, paper establishes the small signal model of the power system and the transmission matrix model of the PCB power supply ground plane system, innovatively combines power supply design and PCB design to realize the impedance control of the power distribution system and improve the power integrity of the circuit. Taking the design of a certain type of network card as an example, based on the impedance model, through simulation, the target impedance is controlled in different frequency bands. The method is verified by measuring the dynamic characteristics and noise of the chip power supply.

Keywords: Power integrity · Small signal model · Transmission matrix
Impedance control

1 Introduction

With the development of ultra-large-scale integrated circuit technology, the operating voltage of the chip is getting lower and lower, and the working speed is getting faster and faster, the power consumption is getting larger and larger, the density of the single-board is also getting higher and higher, the operation of each transistor inside the chip is usually synchronized by the core clock or on-chip peripheral clock, but due to the internal delay difference, the state transition of each transistor can not be strictly synchronized [1], when some transistors have completed the state transition, other transistors may still be in the conversion process in. A high-level gate inside the chip will transmit power noise to the input of other gates, if the gate receiving power noise is in an unstable state of level shifting at this time, the power supply noise may be amplified and the output of the gate circuit generates a rectangular pulse disturbance, which in turn causes a logic error in the circuit. Noise at the external power supply pins of the chip propagates through the internal gate circuitry and may also trigger internal register generation. In addition to affecting the operating state of the chip itself, power supply noise also affects other parts, for example, power supply noise affects the jitter characteristics of the crystal, PLL, and DLL, and the conversion accuracy of the AD conversion circuit.

Now, the clock frequency of the microprocessor's core and peripherals has exceeded 800 MHz, and the internal transistor's level conversion time has dropped

below 800 ps, therefore, higher requirements are placed on the stability of the power supply system in the entire operating frequency band. The level of PI design directly affects the performance of the system, such as overall reliability, signal-to-noise ratio and bit error rate, EMI/EMC and other important indicators. Excessive board-level power channel impedance and synchronous switching noise SSN excessively contribute to severe power integrity issues, which can have fatal effects on device and system operation stability.

2 Research Status

PI design is to ensure that the quality of board-level power supply meets the requirements of the device and product through reasonable planar capacitance, discrete capacitance, and planar segmentation applications, ensuring signal quality and stable operation of devices and products. Figure 1 shows the characteristic diagram of a typical power distribution system for a high-speed circuit system. In the figure, we divide the entire power supply band into parts. In the low frequency range, the power supply noise mainly depends on the power conversion chip VRM to filter; in the frequency range of a few MHz to several hundred MHz, the power supply noise is mainly filtered by the board-level discrete capacitors and the PCB's power ground plane pair; in the high frequency part, the power supply noise is mainly filtered by the decoupling capacitor system and the high-frequency capacitors inside the chip [2, 3]. When the transient current of the load is changed, because the internal transistor level of the load chip is extremely fast, the load chip must be supplied with enough current in a very short time, but the voltage regulator source cannot respond to the change of the load current quickly. There are usually many capacitors placed around the load chip to meet the load transient current requirements.

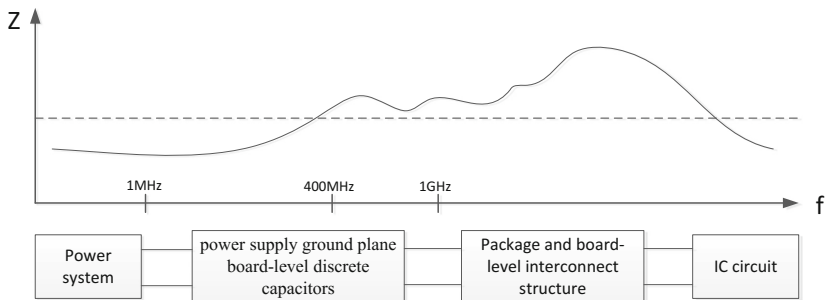


Fig. 1. Power distribution system features

It is relatively intuitive to understand the principle of power supply decoupling from the perspective of energy storage, but it does not help the circuit design. Understanding capacitive decoupling from the perspective of impedance can allow us to design the circuit in a rule-based manner. From the chip point of view, the power

supply system, PCB power ground plane and capacitive decoupling system can be called a composite power supply system, when the PI design is carried out, it is necessary to ensure that the voltage of the power supply system remains stable regardless of how the load current of the chip changes. It is required that the impedance of the power supply system in the characteristic frequency band be sufficiently low. Because of the limitation of volume, efficiency and switching frequency, the power system bandwidth is usually lower than 20 MHz, the loop design needs to ensure the dynamic characteristics within the working bandwidth. Output filter capacitors, inductors and other power devices are mainly selected on the output load current and ripple requirements, so the impedance analysis of the power system is mainly concentrated in the working bandwidth, based on the small signal modeling of the power system; Through the reasonable setting of PCB copper foil size, grid distribution shape, board-level discrete capacitors, pcb power ground plane and board-level discrete capacitors can well suppress the mid-range 20 M–1000 M noise; At high frequencies, due to the black box characteristics of the chip, the high-frequency capacitance distribution inside the chip package cannot be known. Therefore, the ground plane and in-package capacitance of the PCB power supply are generally used to suppress high-frequency noise.

The power system, PCB power ground plane, and decoupling capacitor system can all be equivalent to a two-port transmission matrix network. The network has four main parameters: input impedance, output impedance, reverse current gain, and audio attenuation rate. The input and output impedances are reflected its coupling relationship with other cascade systems, so based on the impedance characteristics to analyze the coupling characteristics of the cascade system can reflect some of the system’s essential problems, Fig. 2 shows the parameters of the dual-port network model, the input can be expressed as the Norton equivalent circuit and the output can be expressed as the Thevenin equivalent circuit.

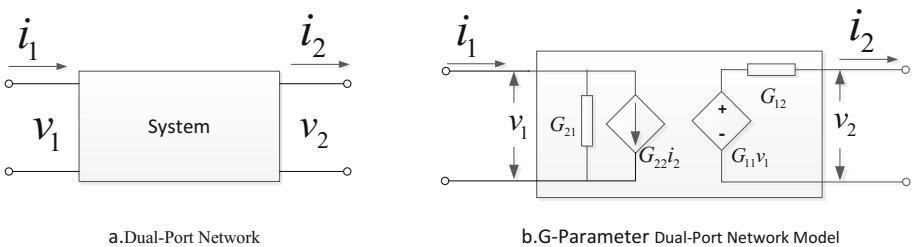


Fig. 2. System dual-port network structure

Among them, G_{11} is the voltage audio attenuation rate, G_{12} is the output impedance, G_{21} is the input admittance, and G_{22} is the reverse current gain. The parameter transfer function can be obtained by measuring the frequency response of the port to

describe the dynamic characteristics of the DC/DC converter. Equation (1) describes the relationship between the input and output variables of the converter.

$$\begin{bmatrix} v_2 \\ i_1 \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ i_2 \end{bmatrix} \tag{1}$$

3 Method and Model

When the power system operates near a certain steady-state operating point, the relationship between the small-signal disturbance quantities of the circuit state variables exhibits a linear characteristic [4]. Through perturbation and linearization, small-signal AC equations can be obtained. The small signal AC model of the basic DC power system can be unified into a standard form called a unified circuit model. As shown in Fig. 3. The dotted line box is a DC/DC conversion system, and the rear stage is schematic express a board-level discrete capacitor, PCB power supply ground plane system or decoupling capacitor system.

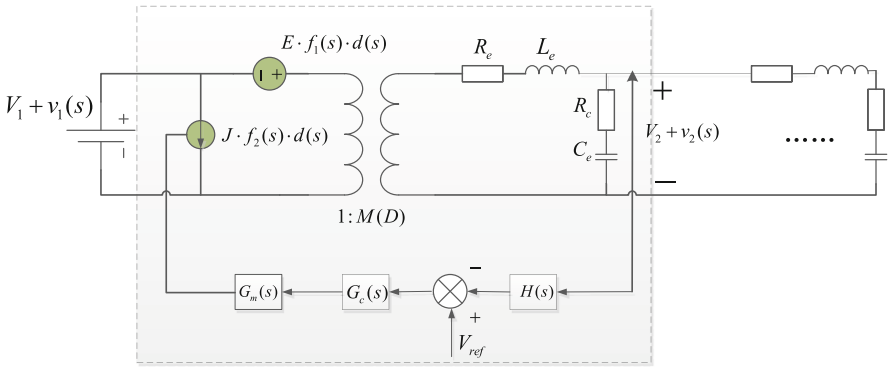


Fig. 3. Unified circuit model of power system

Assume that the input reference voltage perturbation $v_{ref}(s) = 0$, in the case of $v_1(s) = 0$, as shown in Fig. 4, a simplified small signal model system block diagram [5] is established for the output current to the output voltage, deduces the transfer function of the output impedance from the definition of the output impedance, which results in:

$$G_{12CL} = \frac{G_{12OL}}{1 + T} \tag{2}$$

Among them, G_{12OL} is closed loop output impedance, G_{12OL} is open loop output impedance, T is loop gain.

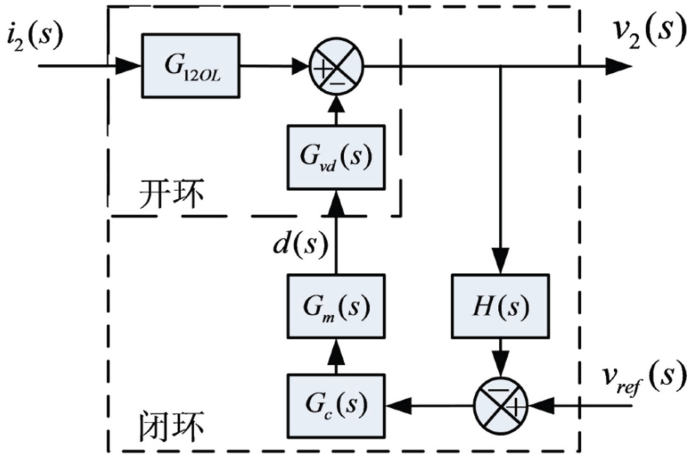


Fig. 4. Simplified small signal model system block diagram for output current to output voltage in $v_1(s) = 0$

The actual size of the planar PCB power supply ground plane is very important for its performance. Figure 5 shows a pair of power/ground plane RLCG equivalent circuits with $M * N$ cell grid equivalent circuits [6], where the equivalent circuit model of the cell grid uses the π model. To ensure the accuracy of the model, the size of the cell grid is less than 1/10 of the shortest wavelength in the band to be analyzed.

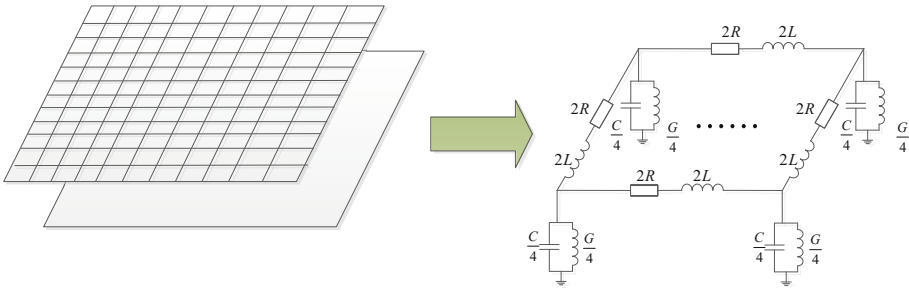


Fig. 5. RLCG equivalent circuit for power/ground plane

The package and PCB power ground plane can be represented by the cascade of the equivalent circuit of the cell grid. Therefore, the two-port transmission matrix method can be used to perform efficient analysis and simulation of arbitrary shapes and complex power/ground planes, as shown in Fig. 5, the power/ground plane is divided

into $(M-1) * (N-1)$ cell grids, the transmission matrix has $M * N$ inputs and $M * N$ outputs, and the transmission matrix can be simplified as:

$$T_p = \begin{bmatrix} A_p & B_p \\ C_p & D_p \end{bmatrix} = \begin{bmatrix} I & 0 \\ C_p & I \end{bmatrix} \tag{3}$$

Among them, I represents unit matrix, 0 identifies 0 matrix, C_p is a $(M * N) * (M * N)$ matrix. The decoupling capacitor and transmission matrix of the through hole can be obtained by the same method [7]. After obtaining the transmission matrix of each part of the multilayer power/ground plane, it can be expressed as a total transmission matrix representing multilayer power/ground plane. Figure 6 shows the input and output of the entire model. According to Fig. 6, the total transmission matrix can be calculated. The impedance matrix can be obtained by the relationship between the transmission matrix and the impedance matrix.

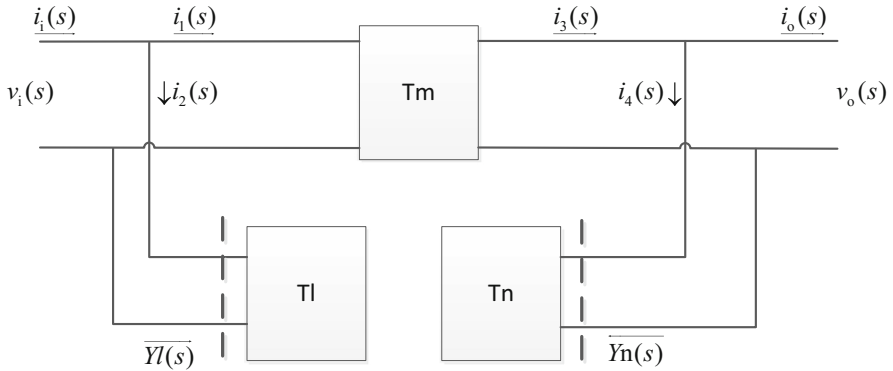


Fig. 6. Block diagram of a multi-layer power/ground plane system

According to the transmission matrix of each part, the required impedance matrix can be expressed as:

$$Z = \begin{bmatrix} Z_A & Z_B \\ Z_C & Z_D \end{bmatrix} = \begin{bmatrix} R_n \times C_{inv} \times D_l & A_n \times C_{inv} \times D_l \\ A_n \times C_{inv} \times D_l & A_n \times C_{inv} \times R_l \end{bmatrix} \tag{4}$$

Among,

$$C_{inv} = \left([C_l \quad D_l] \times \begin{bmatrix} A_m & B_m \\ C_m & D_m \end{bmatrix} \times \begin{bmatrix} A_n \\ C_n \end{bmatrix} \right)^{-1}, R_n = A_m \times A_n + B_m \times C_n, R_l = C_l \times B_m + D_l \times D_m$$

4 Simulation and Test

Take a certain type of 10G fiber network adapter module as an example to illustrate the high-speed system power supply integrity design based on impedance analysis [8]. The module core chip uses a T5 network card chip, 5VDC single power input, and the power required by the device is obtained through DC-DC conversion. The chip manual requires the power supply accuracy is within $\pm 4\%$ under any operating conditions, including DC voltage drop and AC disturbances. Based on the DC-DC power supply and the PCB's operating characteristics, in the process of controlling the impedance on full-band, the DC voltage drop, the voltage output overshoot when the load step changes, and the resonance of the possible output line near the operating frequency, may all cause the voltage output to overflow [9]. The above conditions need special consideration.

In the low frequency range, the DC voltage drop is reflected by the load regulation rate, which is usually expressed as a percentage of the output voltage divided by the output voltage variation when the output current changes from 0 to the rated maximum current; the load step change will cause the voltage transients to overshoot, the step signal can be decomposed into DC component and AC component attenuated with frequency by Fourier transform, in order to ensure the voltage stability under the above two conditions, the low frequency band impedance of the power supply must be strictly controlled. Because of the power output filtering. characteristic, output discrete filter capacitors, filter inductors have large parasitic resistance, open-loop output impedance low frequency band characteristics can not be well controlled, according to formula (3–1), by increasing the amplitude of the low band loop gain, people can effectively reduce the closed loop output impedance of the power system in low frequency band. when designing power, we usually increase add the integral link, the inertial link turning frequency and the proportion of the link factor to achieve target impedance, in practice, the work is done by establishing the power open loop model by Matlab. Low frequency band design process is shown in Fig. 7.

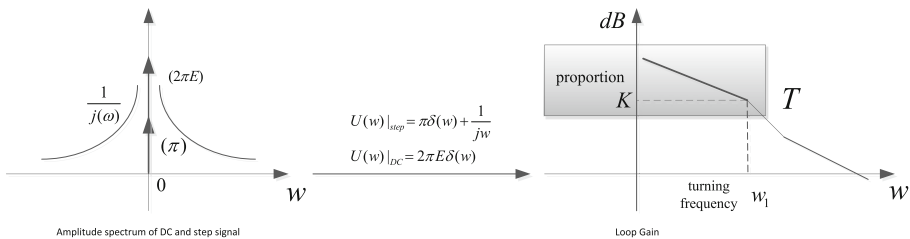


Fig. 7. Low-band impedance control diagram for power system

In the mid-range, to avoid band noise in the power supply coupling into the power supply loop, an inertia section in the middle band is required to reduce the mid-range noise gain, and the loop gain amplitude rapidly decreases [10]. Therefore, in order to control the closed-loop output impedance of the middle band, the output filter transfer

function must be controlled to reduce the open-loop output impedance, thereby the closed-loop output impedance is controlled. Based on Figs. 3 and 4, combined with the loop gain, a closed-loop model of the power supply is built in Matlab. The mid-band design flow is shown in Fig. 8.

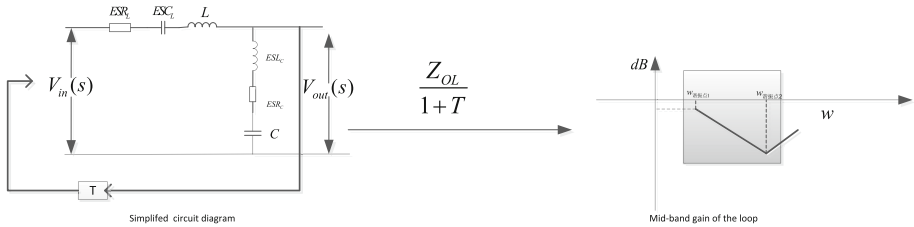


Fig. 8. Mid-range band impedance control diagram in power system

Set up the power system model in Saber simulation software for time domain simulation. Use the constant current source analog power supply at the power load end to simulate the output varies from 20% light load to 80% heavy load to 20% light load. Compare the impedance of output before and after, the voltage overshoot is significantly reduced. The result is as shown in Fig. 9.

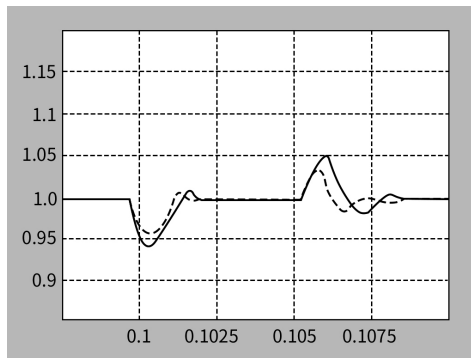


Fig. 9. Comparison of voltage dynamic characteristics in two conditions

In the mid-high band, the characteristics of the power supply and discrete components are inductive. In order to control the output impedance, impedance control in the mid-high frequency band is usually achieved by establishing a reasonable power supply system structure [11]. Since the power supply ground plane forms a resonant cavity in the PCB structure, if the resonant frequency point appears near the operating frequency, it may easily cause abnormal operation of the chip. Based on Fig. 6, passive simulation of the PCB design model is performed through Ansoft SIwave, S-parameters and resonance mode analysis are performed, the resonance occurrence

region and frequency are viewed, and the mid-high frequency band is improved by lowering the capacitance (0.1 to 0.01 uF) or making a thin dielectric layer PCB impedance [12], Fig. 10 shows a comparison of PCB parameters before and after the improvement of S-parameters. The resonance is significantly suppressed.

The PI test is performed on the actual module after the impedance control [13, 14], ripple and noise waveform in mid-high frequency band (20–1000 MHz) are as shown in Fig. 11, load point voltage waveform switching between 20% light load and 80% heavy load is shown in Fig. 12. The waveform proves that the power supply system has good static and dynamic characteristics.

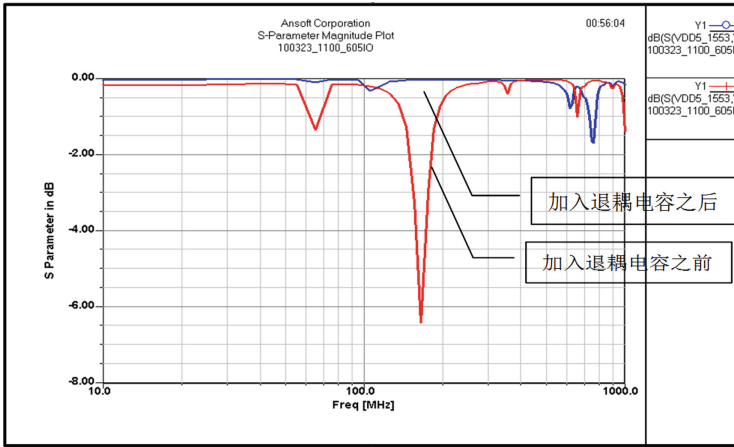


Fig. 10. S-parameter comparison chart

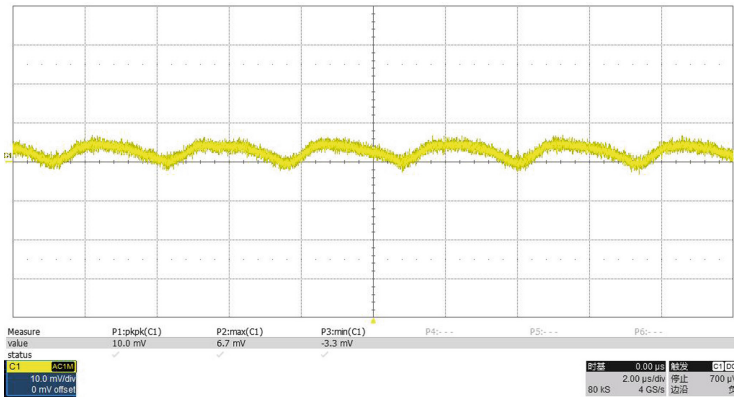


Fig. 11. Measured waveform by oscilloscope (ripple and noise in 20–1000 MHz)

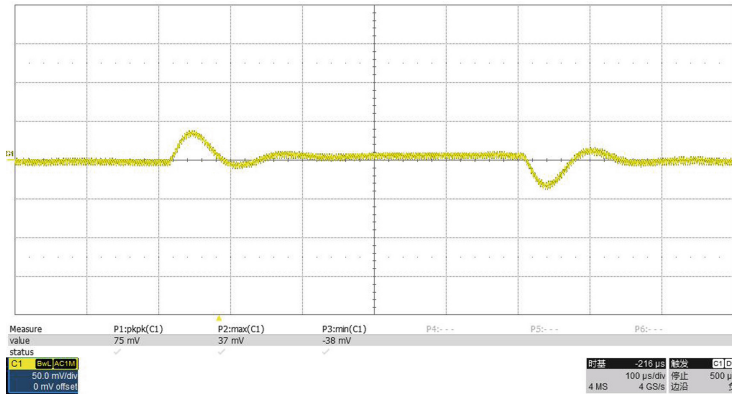


Fig. 12. Measured waveform by oscilloscope (switching between 20% light load and 80% heavy load)

5 Summary

The paper innovatively combines power supply design and PCB design, Conduct impedance analysis and control from the whole process of design. Paper takes the high-speed circuit power integrity design as the background, and studies the method of improving power integrity from the perspective of impedance. Based on the concept of port network, the power system small signal model and PCB power ground plane system impedance model are established, from the low frequency band, the middle frequency range, and the medium high band, the impedance control method was proposed in the aboved three aspects of the frequency band. Using a certain type of network card as a design example, the correctness of the impedance control method is verified by measuring the dynamic characteristics of the power supply and the noise distribution. Based on the research of the paper, in the future [15], a more efficient and dynamic model of the power distribution system needs to be established for precise impedance control in order to improve the power supply efficiency and reduce the development cost.

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