Filter Design for a Nine Level Voltage Source Inverter for Renewable Energy Applications

Ibrahim Haruna Shanono, Nor Rul Hasma Abdullah and Aisha Muhammad

Abstract The rapid deflation of fossil reserves coupled with environmental pollution and degradation caused by direct and indirect crude oil-related activities has resulted in the need for a sustainable alternative and environmentally friendly means of energy generation. The quest triggers the upsurge of research in the field of Renewable energy sources and its conversion. Multilevel voltage converters serve as the main interface between the renewable energy source (solar, wind etc.) and the utility grid. The converter nonlinear nature results in the need for special modulation techniques and output filters that will minimise or eliminates the output harmonics to comply with the IEEE 519 standards. Therefore, this paper aims at assessing and comparing the harmonic content of a nine-level voltage source converter using four passive filters i.e. LC, LCL, LCL with series and parallel resistance. The output voltage and current waveforms, frequency spectrum and total harmonic distortion (THD) of all the filters are compared and analysed. It is found that all the filters have THD less than 5% with LCL with parallel resistor having the least THD content of 1.82%. The investigation is carried out via simulation using PSIM and Matlab software.

Keywords Multilevel converters · Harmonic distortion · Passive filter Voltage source inverters (VSI)

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1 Introduction

Multilevel inverter (MLI) prominence in Renewable energy conversion has exceeded that of it conventional two-level counterpart. This is attributable to the vast limitations of the later it has overcome and the inherent advantages it possesses. The converter modular nature makes it possible to integrate smaller rated power electronic switches to achieve high power capability [\[1\]](#page-14-0). It also eases maintenance and allows the possibility of incorporating redundancy. MLI increased output step level minimises the output harmonics, and this translates to smaller output filter size, smaller cooling system due to reduced system losses which consequently improved the overall system efficiency.

Several new MLI topologies were recently developed, most of which are modifications or hybrid of the famous three conventional topologies namely Diode Clamp (DC), Flying Capacitor (FC) and Cascaded H-bridge configurations [\[2–](#page-14-1)[4\]](#page-14-2). Depending on the inverter topology and its control strategy; a suitable output power filter is designed and then interfaced between the inverter circuit and the grid as depicted in Fig. [1.](#page-1-0)

From Fig. [1,](#page-1-0) it can be seen that the filter form an integral part of Renewable Energy System (RES). As the name implies, its main function is to remove or mitigates unwanted signals in the output of any system [\[5\]](#page-14-3). In the field of power systems and power electronics, non-linear loads tend to inject unwanted signals called harmonics into the system, which are said to be integer multiples of the fundamental frequency (2nd, 3rd, 4th, … etc.). These harmonics are harmful pollutants to the entire system in that it results in overheating of devices and pulsating torque in motors. Hence, affects both system performance and efficiency. Harmonics are generated due to the non-linear characteristic properties of some electronic equipment involved. Due to quarter wave symmetry theorem of AC signals, even harmonics (2nd, 4th, 6th, … etc.) cancel each other in the output, leaving behind the odd harmonics [\[6,](#page-14-4) [7\]](#page-14-5).

Filters are broadly classified into active and passive based on the type of component (active or passive) used in constructing it. The most commonly used is the passive filter, due to its availability and cheapness of components, less design complexity and its ability to effectively performed it-desired task [\[8,](#page-14-6) [9\]](#page-14-7). There are quite a

Fig. 1 System block diagram

number of filter design procedures the likes of ripple calculation, iterative algorithms and power losses optimisation [\[10](#page-14-8)[–12\]](#page-14-9).

The objective of this paper is to design and compare the THD elimination capability of four sets of passive filters on the output of a Cascaded H-bridge Nine-level voltage source inverter presented in $[1]$. The filters considered in this work are LC, LCL and LCL with series and parallel damping. Their stability characteristics are analysed using frequency response obtained through bode plot. The manuscripts equally justify the efficacy of selective harmonic elimination (SHE) technique in eliminating selected lower order harmonics. Therefore, aiding in achieving smaller size filter inductors by pushing up the filter cut off frequency (fc).

2 Materials and Methods

This section explains the inverter topology principles of operation, how the switching angles are obtained, and the switching function used to generate the required nine level voltage waveform.

2.1 Inverter Circuit Description

The circuit shown in Fig. [2](#page-3-0) is the inverter topology used in generating the nine-level output waveform. The circuit comprises of two Cascaded H-bridge topology modules that shared the same input source with their output connected to a transformer having two independent primary and series connected secondary windings with 1:1, and 1:3 turns ratio respectively. The single DC input source could be either Photovoltaic, lithium ion batteries or fuel cells. IGBT modules $(S_1 \text{ to } S_8)$ are used as the power switches. Each of the gating terminal is controlled using pre-calculated switching angles stored in a pulse generator $(G_1 \text{ to } G_8)$. With an appropriate control signal, each of the H- module is capable of generating three voltage steps $(-V_{DC}, 0,$ and V_{DC}). Table [1](#page-3-1) gives the state of each switch and the corresponding terminal voltages. The transformer turns ratio gives the opportunity of increasing the number of steps from the usual five level in conventional topology to nine level, which is one of the novelties of the proposed circuit [\[1\]](#page-14-0).

However, the circuit configuration did not depict the filter in the output, but each designed filter is connected between the inverter output and the load.

Figure [3](#page-4-0) is the sketch of the nine level voltage waveform to be generated by the converter topology. The first module is used for level generation as it adds more notches to the waveform while the majority of the power is transferred through the second module. Note that the research is not intended to address switching and power balancing among the electronic switches and transformers; it is a separate study on its own.

Fig. 2 Converter circuit topology

Voltage	Switching states								
	c D.	S_2	S_3	S_4	S_5	S_6	S_7	S_8	
		0		0				0	
$+E$		Ω	θ					θ	
$+E$		$\mathbf{0}$		θ					
	0		θ		0				
-Е	0			θ				0	
– F.		0		$\overline{0}$	Ω			θ	

Table 1 Switching combinations

2.2 Switching Angles

The multilevel inverter is controlled using Selective harmonic elimination (SHE) pulse width modulation (PWM) technique. Therefore, the switching angles are obtained by optimally solving the generated non-linear transcendental equations using a Genetic Algorithms optimisation technique. Equation [\(1\)](#page-4-1) shows the generalised output waveform equation. There are twelve angles with each representing a single notch (N) added per-quarter waveform at predetermined points. The equation representing the fundamental component $(n=1)$ is equated to a specific value,

Fig. 3 Nine level waveform with 3/3/3/3 distribution ratio

whereas all other equations are equated to zero meaning all harmonic amplitudes are zeros. Based on selective harmonic elimination theory, the converter eliminates $(N - 1)$ harmonics, which means that all the 11 lower order odd harmonics(3rd, 5th, 7th, 9th, 11th, 13th, 15th, 17th, 19th, 21st, 23rd) are eliminated in the output [\[1\]](#page-14-0).

$$
h_1 = \frac{4 * E}{n\pi} \{ \cos(n\alpha_1) - \cos(n\alpha_2) + \ldots \pm \cos(n\alpha_{12}) \}
$$
 (1)

Table [2](#page-4-2) shows the twelve switching angles in degrees. The remaining angles were calculated based on quarter wave symmetry theorem.

3 Filter Design

This section discusses the four types of filters used in this research, their circuits configuration and the design steps.

3.1 LC Filter

An LC filter is classified as a second order filter in that it has two energy storage components. Unlike it first order counterpart (L), it has an additional capacitor connected in parallel to the grid. This makes it have a better attenuation factor of 40 dB per decade. It attenuates higher frequencies above the filter cutoff frequency (fc), whereas the lower frequency harmonics were selectively eliminated using the SHE modulation technique. The optimum goal is to realise a THD of less than 5% hence, satisfying the IEEE. 519 standard. The switching method used is capable of eliminating the first 11 lower order odd harmonics. Consequently, the most dominant harmonic in the output is the 25th order. As such, the filter cut off frequency (fc) is chosen to be 1250 Hz. The filter inductance L is selected such that the voltage drop across it is less than 3% of the inverter output voltage. Figure [4](#page-5-0) is the circuit arrangement for the LC filter. Equations (2) and (3) are the expressions used in selecting the inductor and capacitor values.

$$
I_{Lmax} * X_L = I_{Lmax} * (2\pi Lf) < 0.03 * V_{in}
$$
 (2)

$$
C = \frac{1}{L * (2\pi f c)^2}
$$
 (3)

Fig. 4 LC filter

ILmax is the current through the inductor and f is the fundamental frequency (50 Hz), while Vin is the RMS value of the inverter output voltage.

Base on the circuit configuration, the filter input-output relation is given by the transfer function below. The values of the L and C are substituted in the transfer function which will be used to obtain the filter frequency response.

$$
G_{(s)} = \frac{Vg}{Vin} = \frac{1}{1 + LCS^2} = \frac{1}{1.622e - 8S^2 + 1}
$$
(4)

3.2 LCL Filter

Due to the large inductor size, time delay and resonance issues associated with the LC filter, LCL filter was introduced to address the said problems [\[13\]](#page-14-10). It is a third order filter because it has three energy storage components with an attenuation factor of 60 dB per decades. Its circuit is distinct from LC filter in that it has an additional series connected inductance between the capacitor and the grid. This filter effectively addresses the problem of size and time delay but still has resonance issues, which if not addressed can cause instability in the voltage and current at the resonance frequency. Figure [5](#page-6-0) shows the LCL filter circuit arrangement.

The below expression gives the above circuit transfer function. It is used to analyse the filter stability margin using a bode plot.

Fig. 5 LCL filter

The resonance issue is addressed by damping the system. The damping is achieved by connecting a resistor either in series or parallel to the filter capacitor. Figure [6a](#page-7-0), b represents the two filter circuit arrangements respectively. The circuits transfer function for both the two circuits are given in Eqs. (4) and (5) . The resistance value needs to be carefully selected to minimise losses due to I^2R .

The transfer function for series damping configuration.

$$
G_{(s)} = \frac{I2}{Vin} = \frac{1 + RCS}{(L1 + L2)S + (L1 + L2)RCS^{2} + L1L2CS^{3}}
$$

=
$$
\frac{3.16e - 6S + 1}{1.035e - 11S^{3} + 2.022e - 9S^{2} + 0.00064S}
$$
(6)

While the parallel connection transfer function is given by:

$$
G_{(s)} = \frac{12}{\text{Vin}} = \frac{R}{(L1 + L2)RS + (L1L2)S^2 + L1L2RCS^3}
$$

=
$$
\frac{2}{2.071e - 11S^3 + 6.55e - 8S^2 + 0.00128S}
$$
 (7)

Some rules and approximations need to be followed when designing an LCL filter. One of which is that the inductor voltage drop should not exceed 5–10% of the network root mean square of the rated voltage [\[14\]](#page-14-11). Whereas the current ripples, should not be more than 25% of the rated current. In most cases, it lies within the range of $15-25\%$ [\[15\]](#page-14-12). Lastly, the reactive power absorbed by the capacitor (Oc) should be less than the generated active power (Pg). With the help of the above assumptions, the below expressions are derived.

$$
I_{Lmax} * X_L = I_{Lmax} * (2\pi Lf) < 0.05 * V_{in}
$$
 (8)

$$
Qc = \frac{Vg^2}{Xc} = \text{Vir} * (2\pi \text{ Cf}) = 0.05 * \text{Pg}
$$
 (9)

$$
L_1 = 4L_2 \tag{10}
$$

$$
Wres = \sqrt{\frac{(L1 + L2)}{L1 + L2 + C}}
$$
 (11)

Fig. 6 a Series damped filter, **b** parallel damped filter

Filter type	$L1$ (mH)	L2(mH)	$C(\mu F)$	$R(\Omega)$
LC	4.8	-	3.38	-
LCL	0.512	0.128	158	
LCL series damped	0.512	0.128	158	0.02
LCL parallel damped	0.512	0.128	158	2.00

Table 3 List of filter components

Fig. 7 a Unfiltered inverter output voltage and current waveform, **b** unfiltered voltage and current FFT

$$
R = \frac{1}{3Wres C}
$$
 (12)

The passive components of all the four set of filters are calculated using Eqs. [\(2\)](#page-5-1) and [\(3\)](#page-5-2), [\(8](#page-7-1)[–12\)](#page-8-0). The parameters obtained are presented in Table [3.](#page-8-1)

4 Simulation Results and Discussion

This section presents the inverter output current and voltage waveforms along with their respective FFT. Based on the inverter output, three sets of filters were design and analysed. The stability margin for all the filters is ascertain using bode plot.

4.1 Inverter Output Without a Filter

The proposed inverter topology is simulated in PSIM software controlled using the obtained switching angles to generate the nine-level output voltage. Figure [7a](#page-8-2) shows the current and voltage waveforms across a resistive load. The benefit of SHE-PWM technique is it reduces the inverter output harmonic contents by eliminating lower

Fig. 8 a LC filtered inverter output voltage and current waveform, **b** LC filtered voltage and current FFT, **c** LC filter bode plot

order harmonics. Figure [7b](#page-8-2) shows the Fast Fourier Transform (FFT) for both the output voltage and current. As seen, all the lower harmonics are eliminated in both waveforms. Harmonics become visible at the 25th order, which is not within the SHE-PWM elimination range. Hence, this results in the need for a smaller size filter with cutoff frequency 1250 Hz. The Inverter Total Harmonic Distortion (THD) is 16.1%, which is higher than the acceptable 5%.

4.2 Inverter Output with LC Filter

To make the inverter output closer to a sinusoid, an LC filter is designed and integrated into the system. Figure [8a](#page-9-0) shows the filtered output current and voltage waveforms. The filter eliminates all the remaining higher order harmonics above the 1250 Hz in the output, as seen in the output FFT plot in Fig. [8b](#page-9-0). This results in the THD decline from 16.1% to 2.70%. Therefore, the inverter satisfies the IEEE.519 standard requirement. The drawback with this filter is it sizeable passive component size, time delay, poor stability margin and resonance issue. The bode plot in Fig. [8c](#page-9-0) depicts the filter frequency response with peaky amplitude overshoot occurring at the resonance frequency.

4.3 Inverter Output with LCL Filter

To address the LC filter drawbacks, an LCL filter is designed. Figure [9a](#page-10-0) shows the inverter output current and voltage waveforms. The waveform appears to be smoother than that of LC filter. LCL is capable of solving the inductor size problem and as well reduces the total harmonic distortion (THD) to 2.06%. Figure [9b](#page-10-0), c represents the output FFT and the filter bode plot respectively. Even though the filter is not able to address resonance effects, but there is a significant improvement in the filter frequency response due to an increase in the filter phase margin and reduction in the resonance overshoot period.

Fig. 9 a LCL filtered inverter output voltage and current waveform, **b** LCL filtered voltage and current FFT, **c** LCL filter bode plot

4.4 LCL Filter with Series Damping

To solve the resonance problem associated with the LCL filter, damping resistance is connected in series with the filter capacitor. Figure [10a](#page-11-0) shows the output waveform with slightly reduced ripples, which results in a harmonic reduction to 2.05%. Figure [10b](#page-11-0) shows it FFT plot, which has no visible physical changes from that of LCL. This is because only slight THD improvement occurs (down by 0.01%). It can be seen from Fig. [10c](#page-11-0) that the filter was able to suppress the resonance effect by damping the overshoot. This results in better stable frequency response and smooth phase transition at the resonance frequency. The drawback of this filter arrangement is high losses due to Ic^2R , as such the resistance value needs to be carefully selected.

Fig. 10 a LCL series resistance filtered Inverter output voltage and current waveform, **b** LCL series resistance filtered voltage and current FFT, **c** LCL series resistance filter bode plot

4.5 LCL Filter with Parallel Damping

The filter-damping factor can as well be improved by connecting a resistor in parallel with the capacitor. This arrangement appears to have the least amount of THD value standing at 1.82%. Figure [11a](#page-12-0), b shows the smooth inverter output waveforms and harmonic free FFT plot. The filter frequency response in Fig. [10c](#page-11-0) has significantly improve with almost zero overshoot at the resonance frequency and has better phase and gain margins.

Table [4](#page-13-0) present the THD summary obtained for the four filters along with the one obtained without filter.

Fig. 11 a LCL parallel resistance filtered Inverter output voltage and current waveform, **b** LCL parallel resistance filtered voltage and current FFT, **c** LCL parallel resistance filter bode plot

5 Conclusion

In this paper, four sets of filters were designed for a 9-level cascaded H-bridge inverter with a cascaded transformer. The inverter is controlled using an optimised SHE-PWM modulation technique, which successfully eliminates the dominant lower order odd harmonics in the output. The output THD of the inverter is very high above the IEEE acceptable standard, therefore requires a filter to eliminate the remaining higher harmonics. The filters harmonic elimination capability was evaluated by measuring the THD values obtained in both the voltage and current output waveforms across a resistive load. Figure [12](#page-13-1) presents the THD **comparison** chart of the inverter output without a filter and with the four filters.

All the filters THD value falls below 5%, therefore satisfying the IEEE 0.519 standard. In addition to that, the filters frequency response, phase and gain margins were obtained using a bode plot. Even though both LC and LCL filters satisfy the IEEE requirements, they still have poor stability margin due to resonance effect. This problem was addressed by connecting an appropriate resistance value in either series or parallel to the filter capacitance. This helps in damping the sudden overshoot that occurs at the filter resonance frequency. Out of all the four filters, LCL with parallelconnected resistance has the least THD value and better stability margin. Hence, making it more compatible with our inverter topology and control strategy.

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Tabl

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