An Analytical Surface Potential Model for Highly Doped Ultrashort Asymmetric Junctionless Transistor

Nipanka Bora and Rupaban Subadar

Abstract Here, we present an analytical solution for surface potential of a heavily doped ultralow channel Double-Gate Asymmetric Junctionless Transistor (DG AJLT). The gate-oxide-thickness and flatband voltage asymmetry were taken into considerations; further, while solving 2D Poisson's equation both fixed and mobile charges in the silicon region regions were considered. To solve the 2D Poisson equation for the asymmetric DG junctionless transistor, we separate the solution of the channel potential into basic and perturbed terms. The equations derived from a general symmetric DG junctionless transistor are considered as basic terms, and using Fourier series a solution related to the perturbed terms for the asymmetric structures was obtained. The electrical characteristics predicted by the analytical model shows an excellent agreement with that of commercially available 3D numerical device simulators.

Keywords Analytical model · Perturbation technique · Asymmetric double-gate junctionless transistor (ADG JLT) · Surface potential

1 Introduction

A Junctionless Transistor (JLT) does not have the very high doping concentration gradients or junctions at the source and drain junctions, thereby making fabrication processes easier than MOSFETs with junctions. JLTs has many other advantages like low OFF-state currents, near ideal subthreshold slope (SS ~ 60 mV/dec), high ON-state to OFF-state current ratio, DIBL effects, etc. [1]. Thus, JLTs are potential candidate for sub 20 nm technology nodes and beyond. There are several models for JLT available for the Symmetric Double-Gate (SDG) structures. Colinge et al. [2] proposed the first JL transistor. Duarte et al. [3] studied the electrostatic behavior

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of JL DG transistor using analytical modeling scheme. Subsequently, Lin et al. [4] developed an analytical model of an electric potential of a double-gated fully depleted junctionless transistor. A universal model for symmetric double-gate JL transistor has been reported [5]. However, all these models have been derived by assuming both gates to be perfectly symmetric but in reality, this may not be possible due to process variations and uncertainties which can affect surface potential and other parameters of SDG junctionless transistor. The JLT can be seen as an Asymmetric Double-Gate (ADG) device structure. Thus, a suitable analytical model is very much essential in incorporating these effects. Lu and Taur [6] proposed analytical models for an asymmetric DG MOSFET to reflect these variations. However, these analytical models work with a 1D Poisson equation, which is valid for the potential distribution of long-channel devices; such models are not suitable for the characteristics of asymmetric short-channel devices. A very few analytical models are available in the literature like the model by Jin et al. [7] for asymmetric model based on symmetric structure for junctionless transistors which cannot be considered as a full analytical model ADG JLT. Since the working principle for junctionless transistor is different, same models are not valid for ADG JLT and such models are rare in available literature. Moreover, to develop a JLT without source and drain junction regions is to make the transistor as small as possible which will increase the chip functionality. Because of all these reasons, models which can predict the behavior of ADG JLTs should be developed.

2 Model Derivation

The coordinates, x and y, are as shown in Fig. 1. The Poisson's equation in the silicon region considering both mobile and bulk fixed charges can be written as

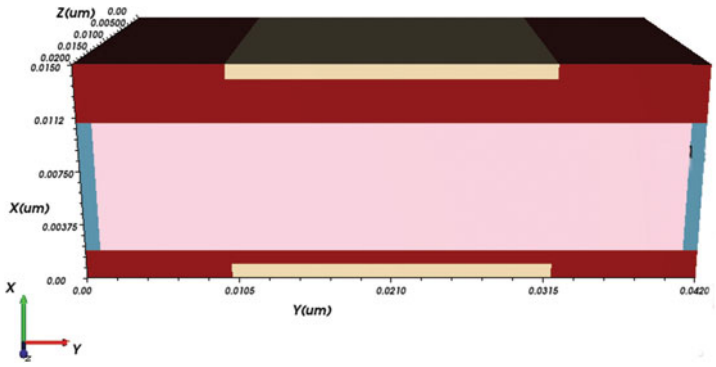

Fig. 1 A 3-D asymmetric junctionless DG MOSFET structure

$$\frac{\partial^2\psi(x,\,y)}{\partial x^2}+\frac{\partial^2\psi(x,\,y)}{\partial y^2}=\frac{q}{\varepsilon_{si}}\left(-N_b+N_b e^{\frac{q(\psi-\psi_f)}{kT}}\right) \tag{1}$$

Equation (1) has no direct analytical solution. Since n-type JL MOSFET is assumed, the body is doped with n-type impurity and the source and the drain are also heavily doped with n-type impurity, where N_b is the bulk doping concentration, $\psi(x,\,y)$ is the channel potential, ε_{si} is the silicon permittivity, ψ_f is the electron quasi-Fermi potential, and q is the electron charge. As Eq. (1) is not directly solvable, we will divide the 2D potential as

$$\psi(x,\,y)=\psi_I(y)+\psi_{II}(x,\,y) \tag{2}$$

where $\psi_I(y)$ is a 1-D function of y and $\psi_{II}(x,\,y)$ is a 2-D function of both x and y. Here, $\psi_{II}(x,\,y)$ is the potential where asymmetric nature has been included. The boundary conditions at the interface between the gate oxide and the silicon body for asymmetric JLT can be written as

$$\begin{aligned}&V_{gs}-V_{fb}+\Delta_{fb}-\psi\left(\frac{t_b}{2},\,y\right)+(t_{ox}-\Delta t_{ox})\frac{\varepsilon_{si}}{\varepsilon_{ox}}\frac{\partial\psi(t_b/2,\,y)}{\partial x}=0\\&V_{gs}-V_{fb}-\psi\left(-\frac{t_b}{2},\,y\right)-t_{ox}\frac{\varepsilon_{si}}{\varepsilon_{ox}}\frac{\partial\psi(t_b/2,\,y)}{\partial x}=0\end{aligned} \tag{3}$$

where V_{gs}, V_{fb} are gate to source and flat band voltage, respectively, ε_{ox} is the oxide permittivity, t_{ox}, t_b are oxide, and body thickness, respectively, Δt_{ox}, Δ_{fb}, are the asymmetries in the oxide thickness and flatband voltage, respectively. The boundary condition near the drain/source contact can be written as

$$\begin{aligned}&\psi(x,\,L)=V_{ds}+V_{bi}\\&\psi(x,\,0)=V_{bi}\end{aligned} \tag{4}$$

where L is the gate length, V_{bi} is the built-in voltage between the silicon body and source/drain contact. These two functions should satisfy the following equations and the corresponding boundary conditions, respectively. Now the Poisson's equation for $\psi_I(y)$ can be written as

$$\frac{\partial^2\psi_I(y)}{\partial y^2}=\frac{q}{\varepsilon_{si}}\left(-N_b+N_b e^{\frac{q(\psi-\psi_f)}{kT}}\right) \tag{5}$$

The solution of this equation for JLTs which normally operates in the depletion region can be given as [8]

$$\psi_I(y) = V_{gs} - V_{th} - \frac{qN_bT_b}{8C_{si}} - V_{th}\,\text{Lambert W}\left[\frac{q^2N_bT_b}{4C_{ox}KT}e^{\left(\frac{q(V_{gs}-V_{th}-\psi_f}{KT}\right)}\right] \tag{6}$$

where Lambert W is the Lambert W-function, V_{th} is the threshold voltage, and C_{si}, C_{ox} are Silicon and oxide capacitors, respectively.

The 2D Poisson's equation for $\psi_{II}(x, y)$ is where asymmetric conditions are used can be given as

$$\frac{\partial^2\psi_{II}(x,y)}{\partial x^2} + \frac{\partial^2\psi_{II}(x,y)}{\partial y^2} = 0 \tag{7}$$

The solution of the above equation can be obtained as

$$\psi_{II}(x,y) = \sum_{n=1}^{\infty}\left[K_n\cos\left(\frac{n\pi x}{L}\right) + R_n\cos\left(\frac{n\pi x}{L}\right)\right]\sin\left(\frac{n\pi y}{L}\right) \tag{8}$$

where K_n and R_n are the coefficients. They can be expressed as

$$K_n = \frac{Num1 - Num2}{Den1 - Den2} \tag{9}$$

$$Num1 = \left(1 + \frac{n\varepsilon_{si}\pi t_{ox2}}{\varepsilon_{ox}L}\right)\cos\left(\frac{n\pi t_b}{2L}\right)A_n$$

$$Num2 = \left(1 - \frac{n\varepsilon_{si}\pi t_{ox1}}{\varepsilon_{ox}L}\right)\cos\left(\frac{n\pi t_b}{2L}\right)B_n$$

$$Den1 = \left(1 + \frac{n\pi\varepsilon_{si}t_{ox1}}{\varepsilon_{ox}L}\right)\left(1 + \frac{n\pi\varepsilon_{si}t_{ox2}}{\varepsilon_{ox}L}\right)\cos\left(\frac{n\pi t_b}{L}\right)$$

$$Den2 = \left(1 + \frac{n\pi\varepsilon_{si}t_{ox1}}{\varepsilon_{ox}L}\right)\left(1 + \frac{n\pi\varepsilon_{si}t_{ox2}}{\varepsilon_{ox}L}\right)\cos\left(\frac{n\pi t_b}{L}\right)$$

$$R_n = \frac{Num11 - Num22}{Den11 - Den22} \tag{10}$$

$$Num11 = \left(1 - \frac{n\varepsilon_{si}\pi t_{ox2}}{\varepsilon_{ox}L}\right)\cos\left(\frac{n\pi t_b}{2L}\right)A_n$$

$$Num22 = \left(1 + \frac{n\varepsilon_{si}\pi t_{ox1}}{\varepsilon_{ox}L}\right)\cos\left(\frac{n\pi t_b}{2L}\right)B_n$$

$$Den11 = \left(1 - \frac{n\pi\varepsilon_{si}t_{ox1}}{\varepsilon_{ox}L}\right)\left(1 - \frac{n\pi\varepsilon_{si}t_{ox2}}{\varepsilon_{ox}L}\right)\cos\left(\frac{n\pi t_b}{L}\right)$$

$$Den22 = \left(1 + \frac{n\pi\varepsilon_{si}t_{ox1}}{\varepsilon_{ox}L}\right)\left(1 + \frac{n\pi\varepsilon_{si}t_{ox2}}{\varepsilon_{ox}L}\right)\cos\left(\frac{n\pi t_b}{L}\right) \tag{11}$$

where

$$A_n = \frac{2qN_bL^2[\cos(n\pi)-1]}{\varepsilon_{si}n^3\pi^3} + 2V_{ds}\frac{\cos(n\pi)}{n\pi} - 2(V_{gs1} - V_{fb1} - V_{bi})\frac{\cos(n\pi)-1}{n\pi}$$
$$B_n = \frac{2qN_bL^2[\cos(n\pi)-1]}{\varepsilon_{si}n^3\pi^3} + 2V_{ds}\frac{\cos(n\pi)}{n\pi} - 2(V_{gs2} - V_{fb2} - V_{bi})\frac{\cos(n\pi)-1}{n\pi} \quad (12)$$

K_n and R_n are decided by the material parameters such as ε_{si} and ε_{ox} and design parameters such as L, N_b, t_{ox1}, t_{ox2}, t_b and also influence of biases such as V_{ds} and $V_{gs1} - V_{fb1}$, $V_{gs2} - V_{fb2}$. For the solution of $\psi_{II}(x, y)$ till third-order terms taken to get higher accuracies; once $\psi_I(y)$, $\psi_{II}(x, y)$ are calculated, the final expression for potential in channel for ADG JT becomes

$$\psi(x, y) = \psi_I(y) + \psi_{II}(x, y) \quad (13)$$

3 Model Verification and Discussions

To validate the analytic model for surface potential, we had considered the 3D device as shown in Fig. 1. To include the dependence on the impurity concentrations as well as the transverse and longitudinal electric field values, Lombardi mobility model is employed. For leakage currents issue, the Shockley–Read–Hall (SRH) recombination model is included in the simulation. Fermi–Dirac carrier statistics without impact ionization is utilized in the simulations, but Quantum effect is not considered. Doping concentration in channel N_D of 5×10^{19} and 1×10^{20} cm^{-3}, silicon body thickness (T_b)= 10 nm are considered for TCAD simulation. Channel width (W) is 10 nm. In addition, p-type polysilicon is used having doping concentration 10^{22} cm^{-3}.

A comparative surface potential variation along the channel direction for SDG and ADG JLTs is shown in Fig. 2. Here, for SDG, the oxide thicknesses (t_{ox}) are kept same at 1 nm for both top and bottom gates, while for ADG JLT, oxide thicknesses for top gate were kept at similar to SDG JLT, i.e., 1 nm while that of bottom gate kept at 2 nm, the channel lengths for both the transistors were kept at 20 nm. From Fig. 2, we can observe that the characteristic curve for the potential variation is same for both top and bottom surfaces for SDG JLT and also the top surface where we had kept t_{ox} same (1 nm). The bottom surface for ADG JLT shows a lower potential curve which is evident from higher t_{ox} (2 nm) which leads to lower capacitive action from bottom gate and thus low surface potential compared to the top gate. Moreover, the variations in surface potential curves occur mainly due to two reasons. First, when the device is not in use, nonzero oxide field is present in the silicon dioxide layer. Second, the potential difference between the gate and the source and the potential difference between gate and the drain are different. These two factors contribute to the bending

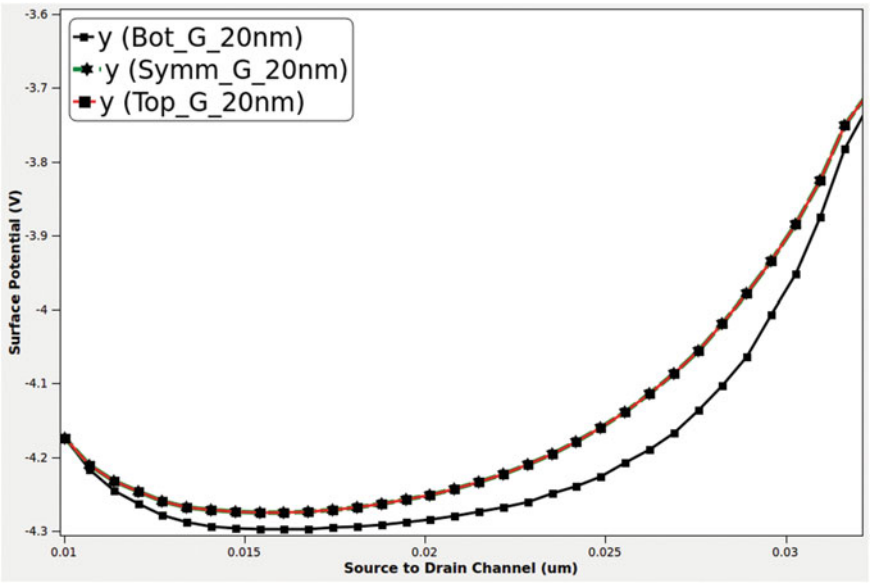

Fig. 2 Potential variation along Y-direction of the SDG/ADG device

of the potential curve between the source and the drain. With the decrease in the length of the device, the band bending increases which is shown in Fig. 3. Potential variations from source to drain for different channel lengths (20, 10 nm) and similar oxide thicknesses (top 1 nm, back 2 nm) of the ADG JLT are plotted in Fig. 3. From Fig. 3, we can observe that the band bending for channel length ($L_g = 20$ nm) shown is lesser than that in case for channel length ($L_g = 10$ nm). In case of the device ($L_g = 10$ nm) compared to that of device with ($L_g = 20$ nm), the source and the device are in greater proximity [2]. To observe the severity on surface potential with change in oxide thickness, we have considered different thicknesses of the oxide layers. For first case, we had taken t_{ox} top as 1 nm and that of bottom as 2 nm, while for the second case we had correspondingly taken 1 nm and 5 nm, respectively. From Fig. 4, it was evident that for top surface potential, both the cases were almost similar but that of bottom surface potential changes drastically as we go for 2–5 nm. Figure 5 shows the variations of surface potential of ADG JLT for different bias voltages (V_{GS}) with channel length 20 nm and t_{ox} front 1 nm and bottom 2 nm. This curve shows that with increase in gate potential, the differences in top and bottom surface potential bending are reduced. This can be explained by the fact that with increase in gate potential more number of charge carriers will be available in the channel; moreover, in the bottom surface, the t_{ox} is more, so lesser will be surface potential. This difference gets reduced correspondingly as we increase the gate voltages.

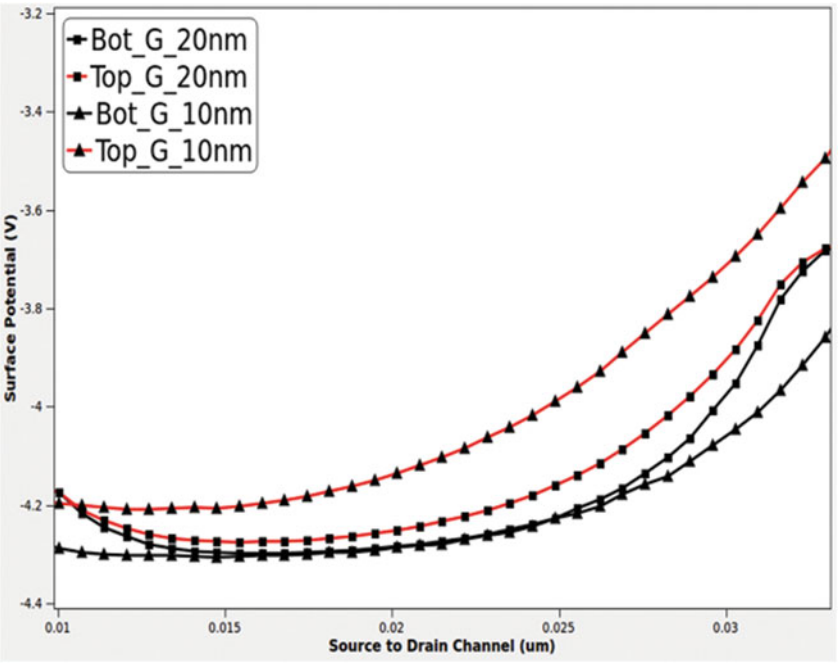

Fig. 3 Potential variation along Y-direction for different L for ADG JLT

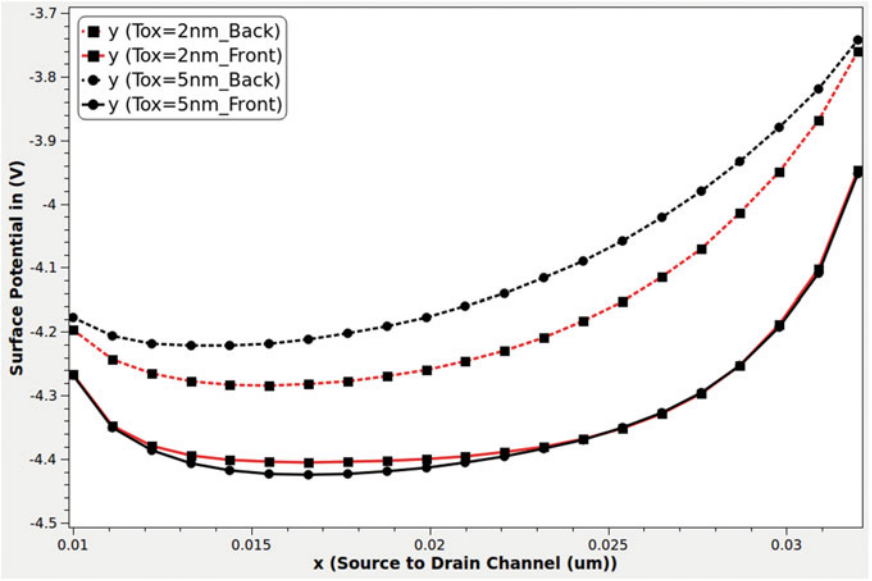

Fig. 4 Surface potential for different t_{ox} for a 20 nm ADG JLT device

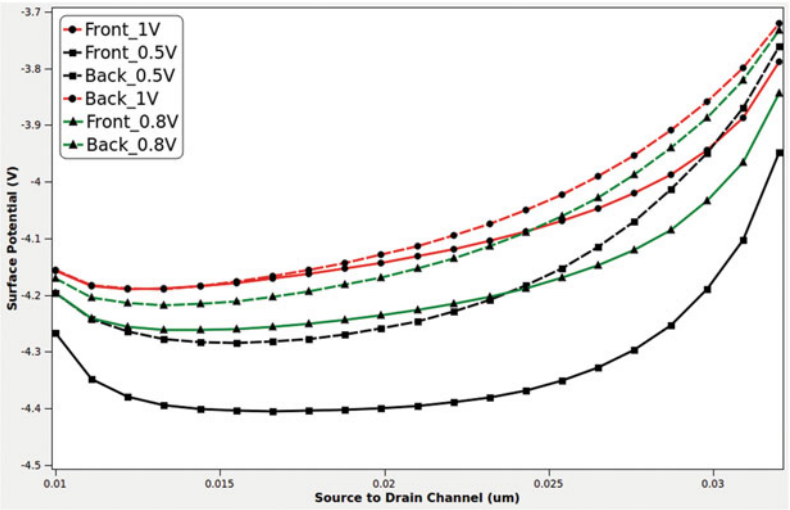

Fig. 5 Potential variation along Y-direction for different V_{gs} for ADG JLT

4 Conclusion

Here, we have proposed an analytical model of surface potential for Double-Gate Asymmetric Junctionless Transistor (DG AJLT). The model can accurately predict the surface potential including the flatband asymmetry and gate-oxide-thickness asymmetry. The variations of electrical characteristics because of structural asymmetry like the differences of gate oxide thicknesses and gate biases between the top gate and bottom gate oxide can be explained. Further, the models predict the variation of design parameters like body thickness and channel length variations with high accuracy. The models proposed show a very good agreement with the results obtained from 3D TCAD device simulation.

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