Design of Digital-to-Analog Converter Using Dual Pair Differential Amplifier in 180 nm CMOS Technology

Preeti Prajapati and Trailokya Nath Sasamal

Abstract Designing Digital-to-Analog Converter (DAC) using dual differential pair as a current-to-voltage converter has been analysed in this paper. Current-steering topology is used since it enables high conversion rate and linearity. The proposed circuit uses binary-weighted architecture rather than segmentation as binary-weighted structure has high SFDR and less tolerant to poor design. It also uses rail-to-rail operation using Gilbert cell. This rail-to-rail circuit provides 60 dB gain with a phase margin of 63°. A current range of 89.79 μA–8.32 mA is obtained with total power consumption of 15 mW. The design and simulations are done using Cadence Virtuoso on 180 nm CMOS technology.

Keywords DAC · Cadence · Low power · Current steering · Gilbert cell · Rail-to-Rail operation

1 Introduction

Data converters are widely used in telecommunication system, video signal processing, cellular network and in many other applications. DAC performs the conversion between digital and analog [1]. DAC can be implemented in several ways that consist of active components and passive components. In early days, resistor array [2] and charge-redistribution DAC [3] are used, though it provides good linearity but it suffers from various drawbacks like large chip size and large power. Some examples of active component are current cell matrix [4], weighted current source [5] and switched-current D/A converters [6]. Though these converters occupy a large area,

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they are implemented to consider device matching [7]. Because of the parallel input, it provides high speed but power consumption is large. The switched-current DAC has simple architecture and has low power consumption. Due to serial input, it has shortcoming at high speed.

Instead of using active and passive component, segmentation architecture can also be used. In [8], segmentation is done in such a way that 5 bits are unary and another 5 bits in binary-weighted form. Similarly, in [9], 12 bits are divided into 7 MSBs that is implemented in equally weighted current sources and the 5 LSBs in binary-weighted current sources. Segmentation depends on a number of bits used in unary coding, leads to complexity and large power, and also degrades the performance of the circuit instead of improving. So rather than using the concept of segmentation, the proposed circuit uses only binary-weighted structure that achieves high SFDR at high clock frequency. The power consumption is low and simple in design and achieves compatible static and dynamic performance.

The current-steering topology has number of advantages like high resolution, high accuracy, small chip area, compatibility with CMOS technology and optimum power consumption [10]. So, the proposed circuit uses current-steering binary implementation that has merits of both, viz., binary architecture and current-steering one. It describes digital part of the circuit.

In typical DACs, operational amplifier acts as a current-to-voltage converter but two-stage operational amplifiers comprise differential stage which provides high gain stage to the system. Two-stage op-amps have two poles. Due to this, system is unstable and phase margin is low that creates oscillations in the system. So instead of using op-amp, dual differential amplifier called Gilbert cell is used which performs the same function. Also, to maximize the dynamic range of the circuit and for a favourable SNR in the analog section of a system-on-chip, rail-to-rail operation is used that is achieved by placing dual differential pair of p-channel and n-channel MOSFET in parallel. It resolves the problem of limited voltage headroom and poor dynamic range since the signal has to be kept as wide as possible. Rail-to-rail operations find widespread application in video signal processing and multimedia systems [11, 12]. This depicts the analog part of the circuit.

The remainder of paper is organized in the following section: Sect. 2 describes the system architecture. In Sect. 3, simulation results are shown and compared with the other DACs. Finally, conclusion is described in Sect. 4.

2 System Architecture

Current-steering architecture offers high speed so it is used in almost any field. Since it requires no buffer and uses load resistor directly for current, the proposed DAC consists of analog part and digital part. Switch driver, switch, array and a current source array implement the analog part of the circuit, while decoder, the latches and a clock driver defines the digital part of the circuit. It is a binary-weighted DAC that

uses a repeating cascaded structure of current source with a dual differential amplifier which acts as a current-to-voltage converter.

2.1 Current Source

It is a basic unit of DAC that directly affects the performance. In the proposed circuit, cascade stage is used since it acts as a constant current source. It has high output impedance that is useful for static and dynamic performance. It also reduces transient voltage fluctuations at node M7 of the current source. This 10-bit DAC uses 10 current source cells. Every cell has cascaded current source with a latch circuit and then carries a current corresponding to 1LSB and increases in binary-weighted form. V_{b1}, V_{b2} and V_{b3} are bias voltages and their values find out by calculations are given as 0.85 V, 1.4 V and 1.65 V, respectively.

2.2 Switch Driver

The size of switch is small so that parasitic capacitance is less. The schematic of switch is shown in Fig. 1. The deglitching circuit on the current source adjusts the crossing point of two switch controls so that differential switches are not turned off simultaneously. Transistors M2 to M5 form the differential Goliath inverters and inverters U1, U2 form the differential David inverters [13]. Transistor M3, M6 acts as inverter for the right part, and transistor M1, M5 acts as inverter for left part of differential circuit. The left inverter buffers the digital input, so it acts as an inverting buffer. If size of the buffer is increasing, then switching speed also increases. So in this work, there is a trade-off for speed. This latch is faster, simpler and consumes low power. Transistors M2, M7, M9 to M12 act as a cascode stage. Input is *INL* and its complement is *INR*. *INL* and *INR* are the inputs that are applied through M1 and M8, respectively. *IL* and *IR* are the currents that are applied in NMOS and PMOS Gilbert cell as input.

2.3 Gilbert Cell Design

With reference to the conventional Gilbert cell topology, dual differential pair with active load was designed using p-channel and n-channel MOSFET as described in Fig. 2 and Fig. 3, respectively.

It uses the current mirror topology. The input stage of Gilbert cell shows a non-linear behaviour that becomes critical at lower bias current, and hence the linearity of Gilbert cell is not good. So we can achieve better linearity using current mirror since it shows linear behaviour regardless of the bias current [14]. The transistors M5, M6

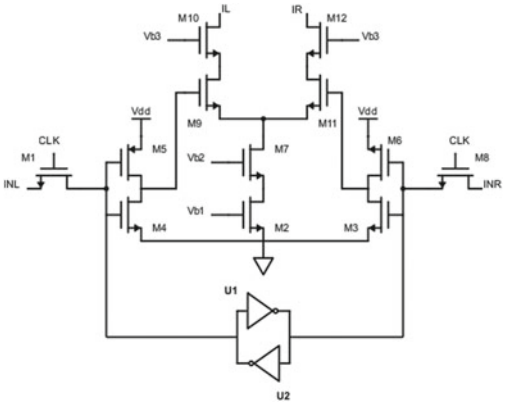

Fig. 1 Schematic of switch

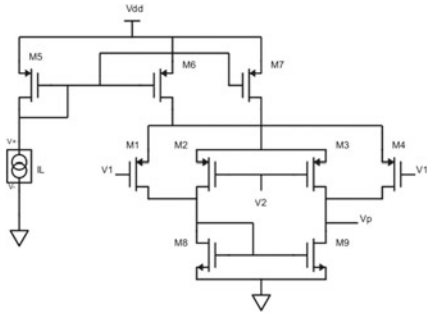

Fig. 2 MOS version of Gilbert cell using p-channel transistor

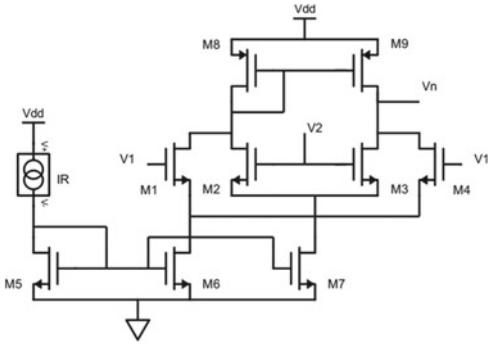

Fig. 3 MOS version of Gilbert cell using n-channel transistor

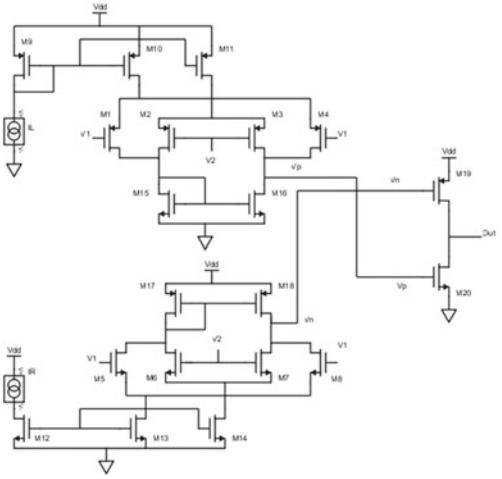

Fig. 4 Rail-to-rail Gilbert cell

and M7 act as a current mirror for n-type and p-type, respectively, for a wide range of input voltage. This results in a constant transconductance so that a good linearity performance can be achieved.

The current rail also provides sufficient current to drive Gilbert cell in saturation region. There are two differential inputs named as V1 and V2 applied to the cross-connected differential pairs. The above Gilbert cell has dual differential amplifier stages that consist of transistors M1–M4 for n-type and p-type in which transistors M5–M7 used for current mirror and transistors M8–M9 acts as active load depicts in Fig. 2 and Fig. 3, respectively. Currently, *IL* and *IR* are used to drive the input stage of PMOS and NMOS Gilbert cell. So *IL* and *IR* are the currents that split between the differential pairs. Gilbert cell has two important properties. The first one is that the tail current drives the small signal gain of the circuit. The second property tells that the two transistors in a differential pair provide a simple means of steering the tail current to one of the two destinations [15].

2.4 Rail-to-Rail Operation

The outputs V_n and V_p are connected in a cross-coupled common source configuration that allows full rail-to-rail input range. A p-channel pair of Gilbert cell is in parallel with an n-channel pair of Gilbert cell so that one pair is conducting at a time and covers full input common mode range as depicted in Fig. 4.

The input common mode range of n-type MOSFET is

$$V_{cn} > V_{ss} + V_{gsn} + V_{dsn}$$

where V_{gsn} represents the voltage drop between gate to source and V_{dsn} represents the voltage drop between drain–source of the NMOS transistor, respectively.

Similarly, the input common mode range of p-type MOSFET is given as follows:

$$V_{cp} < V_{DD} - V_{gsp} - V_{dsp}$$

where V_{gsp} is the voltage drop between gate and source and V_{dsp} represents the voltage drop between drain–source, respectively.

For full rail-to-rail input, at least one of the input pairs should be on that means

$$V_{cp} > V_{cn}$$
$$\text{i.e } V_{DD} - V_{SS} > V_{gsp} + V_{dsp} + V_{gsn} + V_{dsn} > 2V_{th}$$

There exist a common mode input voltages in which both pairs are on. In this case, it creates a serious issue. It can be observed that the transconductance is almost double when only one of the input pairs is on and is given as follows:

$$g_m = 2\sqrt{K\frac{W}{L}I}$$

where g_m is the transconductance, K' is the transconductance parameter, I is the drain current of the transistor, W is the width and L is the length of the transistor, which makes optimal frequency compensation very difficult. For improvement of the gain and to enhance signal-to-noise ratio, input stage should have large transconductance.

3 Simulation Results

We have used Cadence spectre for simulation using Cadence Virtuoso tool for standard 180 nm CMOS process under 1.8 V supply voltage. We have also included current mirror circuit in our simulations. Threshold voltages of −0.5 V and 0.45 V are considered for PMOS and NMOS, respectively. The transient output waveform of the circuit is shown in Fig. 5. The plot of spurious-free dynamic range (SFDR) versus frequency is depicted in Fig. 6. The net power consumption is 15 mW. Frequency response of rail-to-rail circuit is also shown in Fig. 7. This rail-to-rail circuit provides 60 dB gain with a phase margin of 63°. Table 1 summarizes the comparison of results of proposed circuit from previously reported DAC.

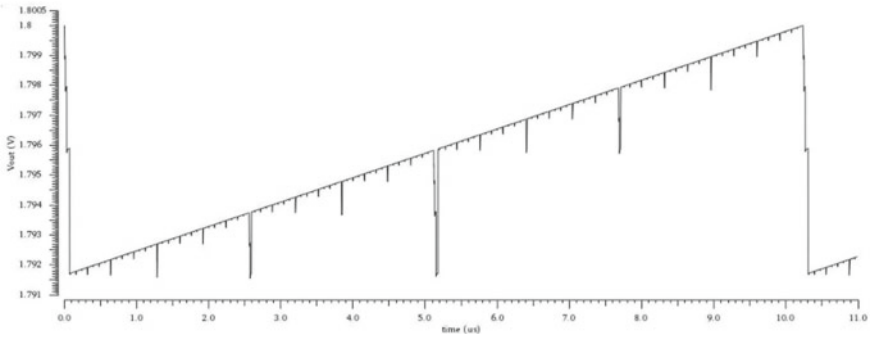

Fig. 5 Transient output waveform

Fig. 6 Measured SFDR versus frequency

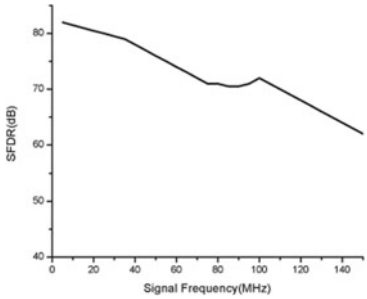

Fig. 7 Frequency response of rail-to-rail circuit

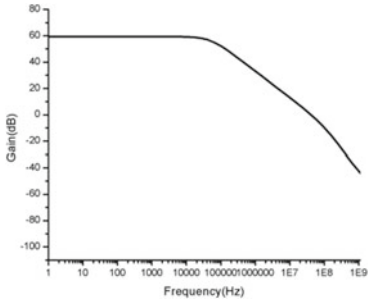

Table 1 Comparison of results from previously reported DAC

Parameters	This work	Ref. [16]	Ref. [17]
Technology (nm)	180	180	180
Supply voltage (V)	1.8	1.8	1.8
Resolution (Bits)	10	10	10
Sample rate (MS/s)	100	250	250
SFDR (dB)	82	58	61.2
Power (mW)	15	19	22
FOM (10^9)	6826	13473	11636

4 Conclusion

In this brief, we developed a new architecture for implementing digital-to-analog converter using dual differential pair. From the analysis, it can be inferred that binary-weighted architecture has very simple decoder and due to this, it consumes less power. Our result also shows that the proposed circuit has SFDR of more than 50 dB.

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